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VMIPCI-4320
8-Channel PCI bus Analog Output Board

Product Manual

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500-854320-000 Rev. B

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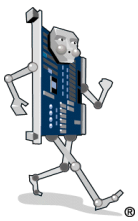
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Overview

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Introduction

The VMIPCI-4320 12-bit PCI bus Analog Output board provides eight high-quality analog output channels. The channels are jumper-selectable for voltage outputs, current loop outputs, or a combination of voltage and current loop outputs. Each output range is jumper-selectable. On-board ±15 V DC-to-DC Converters are used to supply ±15 V. An illustration of the board is shown in Figure 1 on page 13. Figure 2 on page 14 is a block diagram of the VMIPCI-4320. The following brief overview of principal features illustrates the flexibility and the performance that is available with the VMIPCI-4320 board:

- Sixteen analog output channels
- Jumper-selectable voltage or current outputs
- 12-bit DAC resolution
- Output current ranges of 4 to 20 mA, 0 to 20 mA, and 5 to 25 mA (4 to 12 mA, 0 to 10 mA, and 5 to 15 mA are also available)
- Output voltage ranges of ±2.5 V, ±5.0 V, ±10 V, 0 to +10 V, and 0 to +5 V
- Output short-circuit protection
- Back panel outputs on P1, a 37-pin D-shell subminiature connector
- Top edge Fail LED indicator for initial verification
- Full size PCI bus PC / AT board form factor
- P1 input for optional 30 V (maximum) external current source power

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Functional Description

The VMIPCI-4320 is a self-contained, 8-channel, 12-bit PCI bus Analog Output Board. Each of the eight channels are programmable by the user using eight 12-bit SRAM locations. Each SRAM location corresponds to an output channel. The VMIPCI-4320 periodically fetches the 12-bit binary values out of the SRAM locations and uses them as the inputs to the on-board DAC. The output of the DAC is distributed to the sample-and-hold circuits associated with each output channel. The board has a refresh rate of 1.262.6 Hz which is the default rate, and provides settling to 0.01 percent for stepped outputs at each update. The maximum settling time to 1 LSB is 792 µsec.

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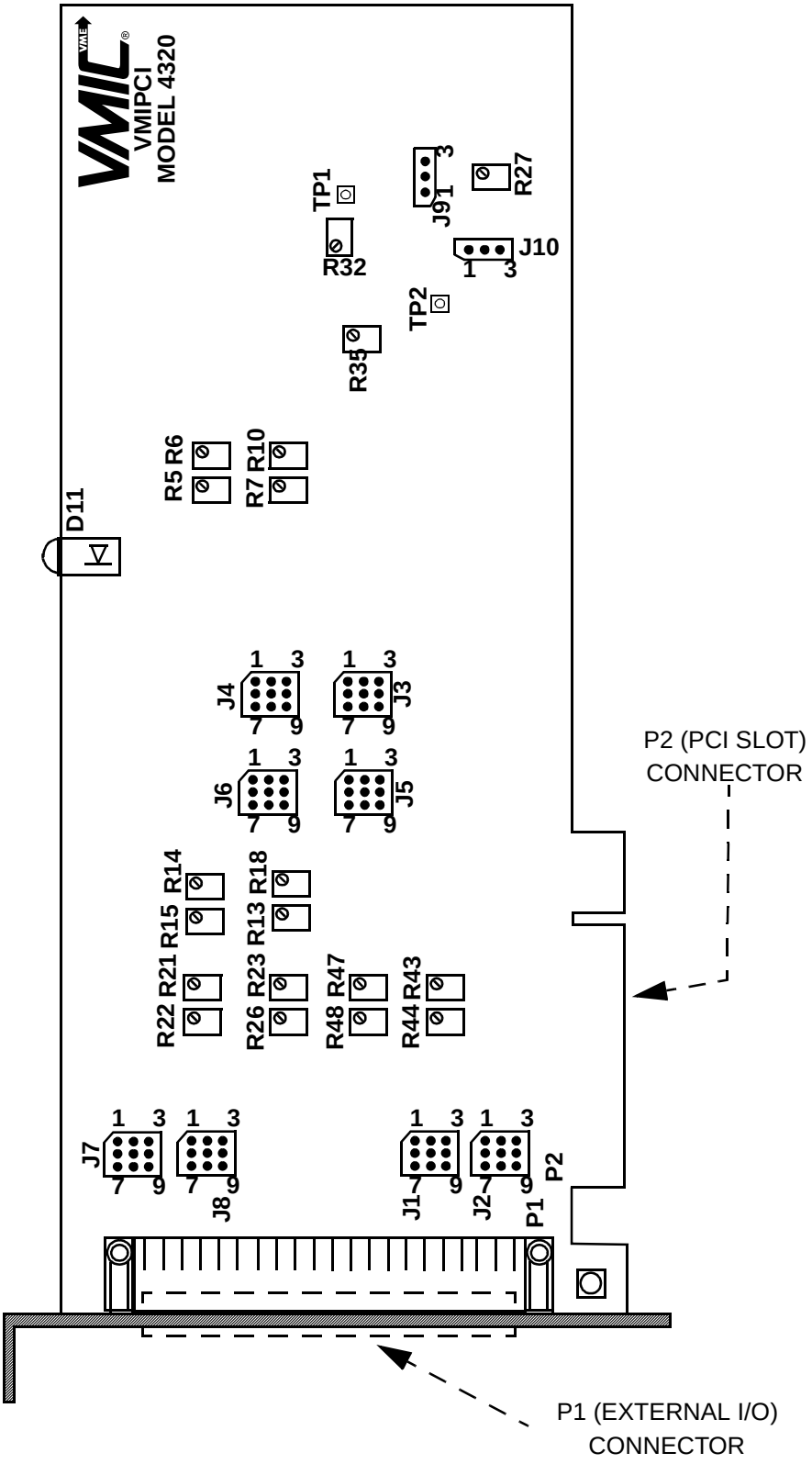


Figure 1 VMIPCI-4320 Analog Output Board

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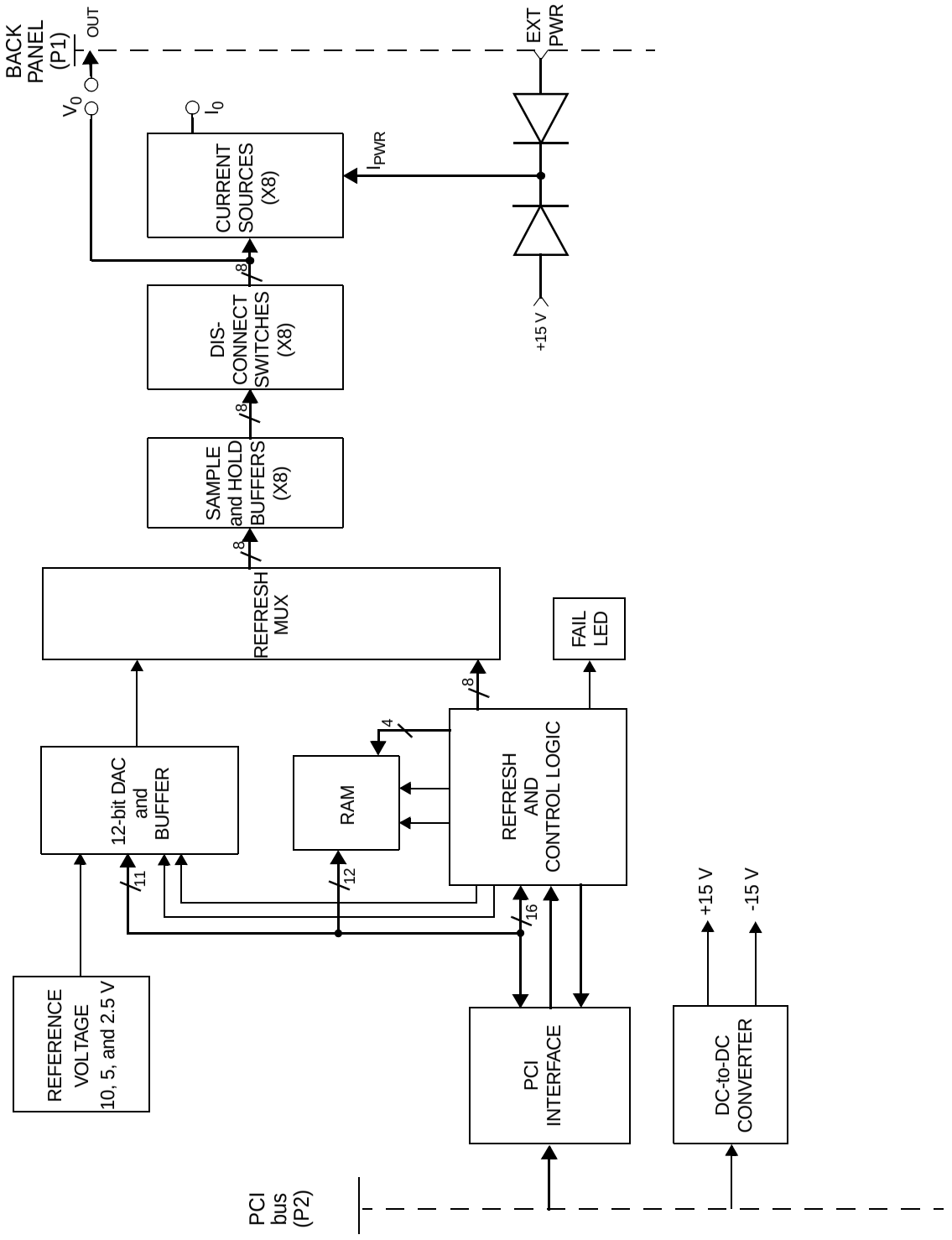


Figure 2 VMIPCI-4320 Functional Block Diagram

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Reference Material List

For detailed information on the PCI Local bus refer to:

PCI Local Bus Specification, Revision 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
PH: (800) 433-5177 (U.S.)
(503) 797-4207 (International)

Physical Description and Specification

Refer to 800-854320-000 Specification

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Intended Audience

Knowledge of CompactPCI bus protocol is assumed. Additionally, you should be familiar with standard network protocol and configuration of a shared memory interface.

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

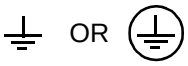
Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual

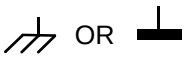
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



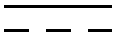
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).



The STOP symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING Denotes a hazard. It calls attention to a procedure, a practice, or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution Denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

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Note Denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER

1

Theory of Operation

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Introduction

The VMIPCI-4320 is an 8-channel, 12-bit Analog Output Board that is designed to operate in a computer supporting the 5 V PCI Local Bus interface.

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Internal Functional Organization

For the purpose of discussion, the VMIPCI-4320 can be divided into two major blocks; the PCI bus Interface, and the Analog-to-Digital Circuitry. The Analog-to-Digital Circuitry is further divided into the following sections:

a. Data storage
b. DAC and analog multiplexer
c. Analog output buffers and switches
d. Voltage-to-current converters
e. Analog outputs refresh logic
f. Power converter

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PCI Bus Interface

The VMIPCI-4320 is implemented with a PCI bus-compliant interface device. The VMIPCI-4320 operates as a PCI bus "target" and supports standard PCI bus configuration capability.

PCI bus Configuration Registers

Each PCI bus device contains a pre-defined group of configuration registers. This group of registers implements the primary PCI bus functions of identification, PCI bus command and status, and board configuration. Several of the standard registers, though present in the PCI bus interface device, do not apply to the VMIPCI-4320 board. However, registers that do apply are listed in Table 1-1.

Table 1-1 PCI Configuration Registers

Configuration Address Offset (HEX)	Abreviation	Register Name	VMIPCI-4320 Value (HEX)	Type
00 to 01	VID	Vendor Identification	114A	read only
02 to 03	DID	Device Identification	4320	read only
04 to 05	PCICMD	PCI Command Register	0001	read / write
06 to 07	PCISTS	PCI Status Register	varies	read / wr.clear
08	RID	Revision ID Register	0	read only
09 to 0B	CLCD	Class Code Register	FF	read only
10 to 13	BADR0	Base Address Register 0	varies	read / write
14 to 17	BADR1	Base Address Register 1	varies	read / write
18 to 21	BADR2	Base Address Register 2	varies	read / write

PCI bus Operation Registers

Base Address Register 0 (BADR0) contains a 32-bit address, which points to a second group of 16 DWORD (32-bit) registers. These registers are called the PCI bus Operation Registers and may or may not be involved in VMIPCI-4320 operations.

VMIPCI-4320 Function Registers

Two of the PCI bus configuration registers called Base Address Register 1 (BADR1) and Base Address Register 2 (BADR2), contain a 32-bit address, which is the base address of registers that apply to VMIPCI-4320. Two groups of 64 byte addresses are dedicated to these functions. Of the 64 byte address, only the 32 even addresses should be used since all VMIPCI-4320 function-specific registers are organized as 16 bits wide. Any of the first eight even byte addresses, with offsets $0 through $E,

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access the VMIPCI-4320 Control and Status Register (CSR). The next 16 even addresses, with offsets $10 through $2E, access 16 SRAM locations. The first eight of these SRAM locations store the digital values that represent the eight analog outputs. The second eight SRAM locations are spares. All the byte address offsets ($30 through $3F) are reserved.

Note Either register can be used to access the Control and Status Register. This means a software programmer can make either I/O or memory mapped accesses to the CSR. Additionally, writing to either BADR 1 or BADR 2 automatically updates the other one.

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Digital-to-Analog Circuitry

Besides the PCI interface, the VMIPCI-4320 board can be subdivided into the following blocks:

- Refresh and control circuit
- Small SRAM
- Single 12-bit DAC
- Eight-channel analog multiplexer
- Eight sample-and-hold buffers
- Eight disconnect switches
- Eight voltage-to-current converters
- Eight corresponding output pins on the P1 connector

The selection of either the voltage or current output and the selection of scale ranges are performed through a series of user-configurable jumpers on the board.

A periodic refresh cycle consists of several events. First, a 12-bit value is read from the appropriate location in SRAM. With all channels of the analog multiplexer open, the SRAM data is written into the DAC, which in turn slews and settles to the new value. Once the DAC output is fully settled, the analog multiplexer gates the output of the DAC to the appropriate sample-and-hold buffer. After an additional settling time, the analog multiplexer is opened again, a channel counter is incremented, and the cycle is repeated for the next channel.

In voltage output mode, the output of the sample-and-hold buffers passes through disconnect switches and jumpered directly to the output connector P1. Optionally, in the current output mode the board can be jumpered such that the outputs of the disconnect switches are routed to the inputs of eight voltage-to-current converters. The outputs of these converters then appear on the appropriate P1 connector pins.

Digital-to-Analog Converter (DAC) Circuit

A single 12-bit DAC services all eight outputs. The circuit also contains a precision reference voltage jumper selectable as 2.5, 5, or 10 V output. In addition, this circuit contains a buffer amplifier with a gain of two, and a jumper which selects either bipolar or unipolar operations. Various combinations of the two jumpers, result in the available voltage ranges.

Analog Multiplexer

The Analog Multiplexer consists of eight independent analog switches which are enabled, one at a time, by the refresh and control circuit.

Sample-and-Hold Buffers

Each sample-and-hold buffer consists of a storage capacitor and a low leakage operational amplifier. Each amplifier can supply ±10 mA of current over the full scale range of ±10 V and can withstand sustained short circuits to ground.

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Disconnect Switches

A low resistance, solid state switch network follows each of the sample-and-hold buffers. The switches disconnect the buffers from the P1 outputs (as well as the voltage-to-current converters). All eight disconnect switches are controlled by a single bit in the CSR. Upon any board reset, the disconnect switches assume the open state and must be enabled by setting the appropriate bit in the CSR to a logical "1."

Beside switching the outputs of the amplifiers, a second analog switch also switches the feedback of the amplifier from the source or load side of the output switch to compensate for voltage drops across the output switch. Clamping diodes protect the buffers and switches from line transients by shunting transients above ±15 V to the power supply rails.

Voltage-to-Current Converters

The voltage outputs at the disconnect switches can be jumpered to the inputs of eight voltage-to-current converters. Typically the DAC voltage range is set to 0 to +10 V to produce the 4 to 20 mA, 0 to 20 mA, or 5 to 25 mA ranges. A DAC voltage range of 0 to +5 V can be selected to produce the 4 to 12 mA, 0 to 10 mA, or 5 to 15 mA ranges. Additional jumpers select between the three current output ranges for each of the DAC voltage ranges.

The voltage-to-current converters are sourced through a diode by the +15 V on-board converter. This configuration provides a maximum compliance voltage of +11 V. This equates to a maximum load resistance of 550 Ω for the typical 0 to 20 mA range. If this compliance voltage is insufficient, the VMIPCI-4320 provides a pair of pins on the P1 (pins 19 and 37) connector that can be tied to an external power source of up to 30 V maximum. The external power source *must* be capable of sourcing a minimum of 200 mA.

Data SRAM and Refresh Control

The VMIPCI-4320 contains 16 SRAM locations; each location is 12 bits wide. All 16 locations can be written and read by the PCI bus. However, only the first eight locations correspond to the eight analog outputs. Each PCI bus SRAM access takes approximately 330 nsec.

Each channel refresh cycle takes 99.0 µsec to complete. To refresh all eight output channels, multiply 8 x 99.0 µsec for a value of 792 µsec. Therefore, each output is refreshed once every 792 µsec. See Figure 1-1 on page 28 for a flowchart of the refresh cycle.

At the beginning of each 99.0 µsec refresh cycle, the refresh control circuit reads the SRAM for a period of 450 nsec. In the event that both the PCI bus and refresh control circuit attempt to access the SRAM at the same time, an arbitration circuit halts the latter of the two until the first access is finished. If the PCI bus access is the latter, the delay may cause the access to exceed the maximum 16 PCI bus clock cycles. In this event, the PCI bus interface device will issue a Target Requested Retry and the PCI bus master completes the access. Regardless of whether an SRAM access collision occurs or not, each refresh cycle remains 99.0 µsec.

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Built-in Power Converter

Power for the VMIPCI-4320 analog circuitry is supplied by a DC-to-DC Converter. The converter converts 5 V from the PCI bus to regulated and isolated ±15 VDC. Including the current sourced to the eight voltage-to-current circuits, the load current on the +15 V is approximately 350 mA while the load current on the -15 V is approximately 130 mA.

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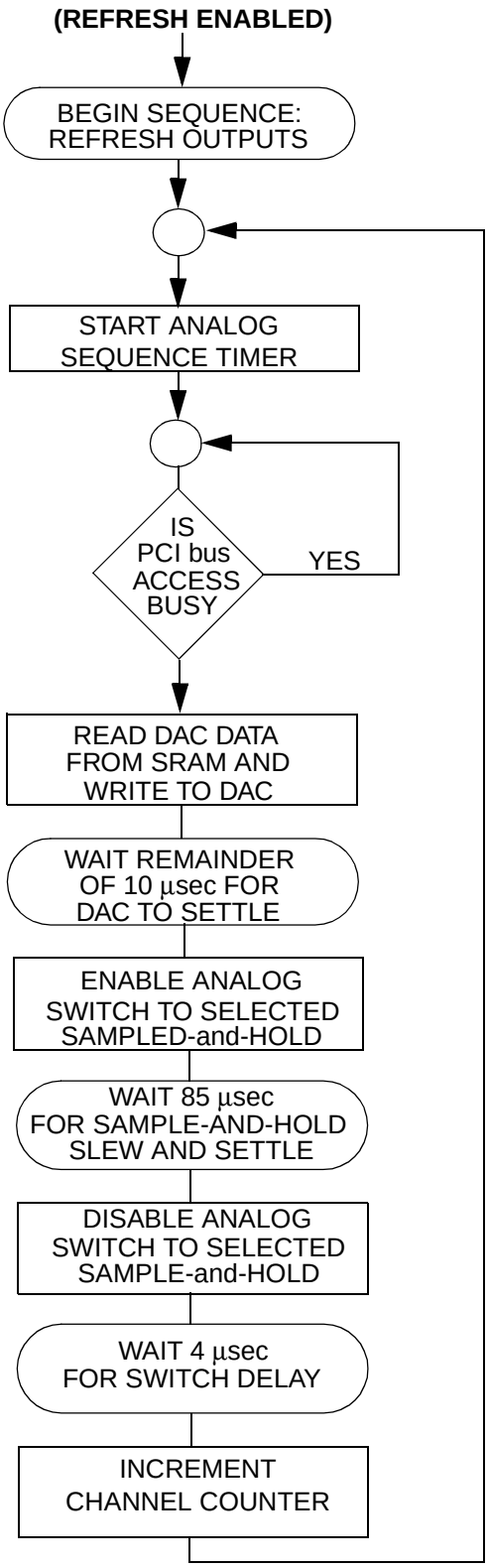


Figure 1-1 Refresh Cycle Timing Diagram

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Configuration and Installation

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Introduction

The VMIPCI-4320 Analog Output Board provides eight high-quality analog output channels. The VMIPCI-4320 has 12-bit resolution with an on-board DC-to-DC Converter.

Data for each analog output channel is written directly into an on-board SRAM location dedicated to a specific channel. The data is then periodically retrieved from SRAM and converted to an analog voltage which is then transferred to one of eight output sample-and-hold out buffers.

The VMIPCI-4320 board is designed with on-board memory that can be tested by executing a memory diagnostic for operational verification. With a Fail LED that is located on the front panel of the board, it gives the user initial verification when installing the board. If an error condition occurs during diagnostics, a software-controlled LED can be illuminated to visually indicate a failure. The LED is illuminated by system reset at power up and is extinguished by the user upon successful diagnostic execution if desired. The LED is for user defined purpose only, and can be used for whatever purpose the user desires.

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Unpacking Procedures

Caution Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

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Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position, except the CPU slot, which is reserved for the system controller.

Caution Do not install or remove the board while power is Applied.

1. Prior to installing board, verify that jumpers are configured as described in the section titled "Factory Installed Jumpers" on page 32.
2. Remove the PC housing cover. Refer to the your PC manual(s) for details.
3. PCI bus systems can conform to one of several standards based on either 5 V or 3.3 V operation, and based on a 32-bit or a 64-bit PCI bus. The PCI bus motherboard slots are keyed and the PCI bus card edge connectors are keyed to ensure compatibility. The VMIPCI-4320 was designed for a 5 V 32-bit PCI system. However, it is also compatible with a 5 V 64-bit PCI bus system as well. Refer to your PC manual(s) for information on compatible PCI bus card types. In addition, examine the PCI bus slot that the VMIPCI-4320 is to be installed. Verify that the location of the key in the PCI bus slot corresponds to the key in the card edge connector.
4. Remove the blank back panel mounting bracket corresponding to the PCI bus slot into which the VMIPCI-4320 is to be installed.
5. Insert the VMIPCI-4320 card edge connector into the desired PCI bus slot and install the retaining screw in the rear support bracket.

Before Applying Power: Checklist

1. Have the sections pertaining to theory and programming, Chapters 1 and 3, been reviewed and applied?
2. Have the jumpers, as described in Table 2-1 of this chapter been installed correctly?
3. Has the I/O cable with the proper mating connector been installed in I/O port P1?
4. Calibration has been performed at the factory. If recalibration should be required, refer to the section titled "Calibration" on page 35.

After the checklist above has been completed, the board can be powered on in a PCI Local bus system.

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Operational Configuration

As with other PCI bus boards, the I/O address space, through which the VMIPCI-4320 operates, is assigned dynamically by the PC system BIOS and is not predefined by jumpers. The VMIPCI-4320 does contain numerous jumpers that define the output type(s) and scale range(s).

Factory Installed Jumpers

Each VMIPCI-4320 board is configured at the factory with the specific jumper arrangement shown in Table 2-1 below. This factory configuration establishes the following baseline. See Figure 2-1 on page 33 for jumper configuration.

1. Current loop outputs on all channels.
2. 4 to 20 mA current range on all channels

Table 2-1 Programmable Jumper Functions

Jumper	Function	Factory Configuration
J10-1,2	Unipolar Operation	Installed
J10-2,3	Bipolar Operation	Omitted
J9-2,3	5 V Full-Scale Operation	Omitted
J9-1,2	10 V Full-Scale Operation	Installed
J9-(none)	20 V Full-Scale Operation (±10 V Only)	No Jumper installed
J8	Ch 8 Voltage / Current and Current Range	(4 to 20 mA)
J7	Ch 7 Voltage / Current and Current Range	(4 to 20 mA)
J6	Ch 6 Voltage / Current and Current Range	(4 to 20 mA)
J5	Ch 5 Voltage / Current and Current Range	(4 to 20 mA)
J4	Ch 4 Voltage / Current and Current Range	(4 to 20 mA)
J3	Ch 3 Voltage / Current and Current Range	(4 to 20 mA)
J2	Ch 2 Voltage / Current and Current Range	(4 to 20 mA)
J1	Ch 1 Voltage / Current and Current Range	(4 to 20 mA)

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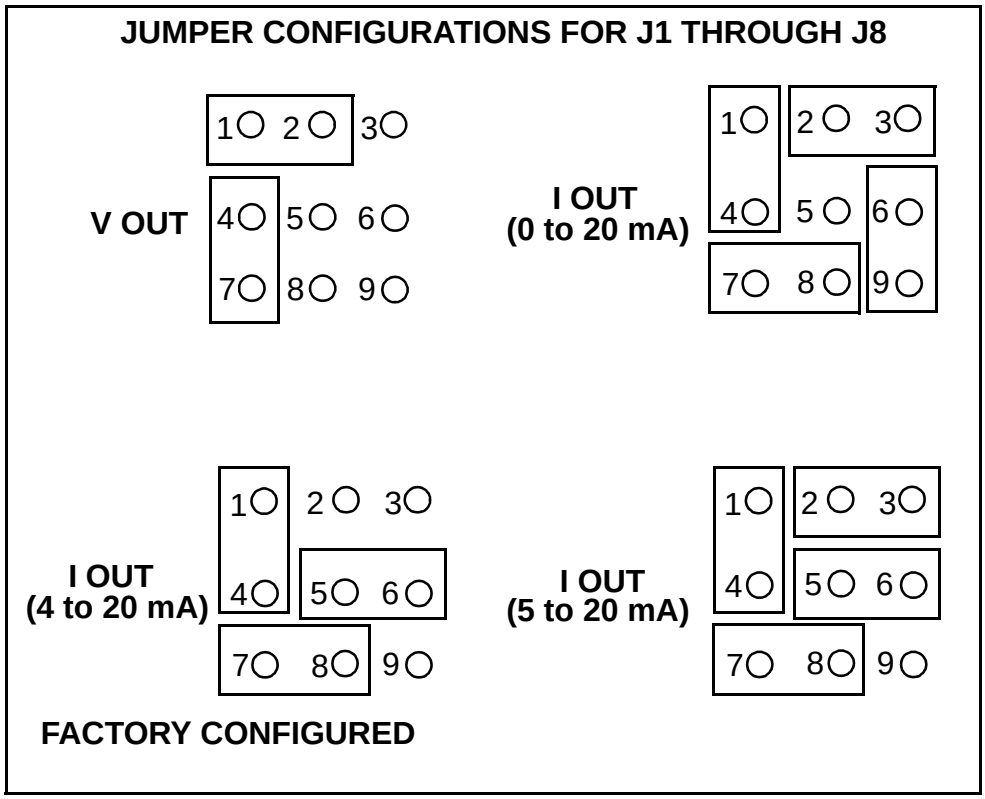


Figure 2-1 Jumper Configurations for Voltage and Current Outputs

Analog Voltage Output Mode

Figure 2-1 illustrates how to configure each individual channel for a voltage output mode.

Output Voltage Range

The output voltage range is controlled by jumper J9. The maximum full scale range is 20 V. To modify the full scale range to either 5 or 10 VDC range, configure jumper J9 as indicated in Table 2-1 on page 32.

Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog voltage outputs is selected with jumper J10, as indicated in Table 2-1 on page 32.

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Analog Current Output Mode

Figure 2-1 on page 33 shows how to configure each individual channel for any of the specified ranges. In order to produce current loop outputs, jumper J10 must be configured for unipolar operation. In addition, J9 jumper is typically set to the 10 V full-scale range to produce the 4 to 20 mA, 0 to 20 mA, or the 5 to 25 mA range. Jumper J9 is set to the 5 V full-scale range to produce the 4 to 12 mA, 0 to 10 mA, or 5 to 15 mA range.

Mixed Output Mode Operation

This manual presumes that all outputs are configured for either voltage or current modes. There is nothing preventing a mix of both current and voltage outputs. However, as indicated in the previous section, only a limited combination of voltage and current loop outputs are compatible. Depending on the current loop range desired, the voltage outputs can be either 0 to 10 V or 0 to 5 V full scale.

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Calibration

Before delivery from the factory, the VMIPCI-4320 board is fully calibrated and conforms to all specifications. Should recalibration be required, perform the appropriate procedures beginning on page 34. The test equipment is listed below. The locations of all adjustments and test points are shown in Figure 2 on page 49. Adjustment potentiometers and their functions are listed in Table 2-2.

Table 2-2 Potentiometer Adjustments

Current Adjustments		
Channel No.	**Zero Offset Adjust**	**Span Adjustments**
0	R47	R48
1	R43	R44
2	R10	R7
3	R6	R5
4	R13	R14
5	R15	R18
6	R21	R22
7	R23	R26

Voltage Adjustments	
Potentiometer	**Function**
R27	Bipolar Outputs Zero Adjustment
R35	Unipolar Outputs Zero Adjustment
R32	Voltage Output Gain Adjustment

Equipment Required

a. **Digital Multimeter (DMM):** ±1.0000 and ±10.000 VDC ranges; voltage measurement accuracy of ±0.005 percent, 10 MΩ minimum input impedance, and current measurements at 1 µA resolution; five or more digits.

b. **PCI bus Host System:** The PCI bus Host System requires, as a minimum, one open PCI bus slot capable of accommodating a full sized PCI bus board, one 3.5-inch floppy disk drive plus interface, monitor, keyboard, and the associated power supply.

c. **PCI bus Extender Board:** Depending on the arrangement of the PCI bus host system, it may be necessary to use a PCI bus extender board to ensure access to the adjustment potentiometers.

d. **Test Cables:** Test cables for the equipment listed above.

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Base Address Determination

With the VMIPCI-4320 installed in the PCI bus host system and using a protected-mode debugger or equivalent software, the individual performing the calibration must first “find” where in the I/O space the system BIOS has located the VMIPCI-4320 Base Address Register 1. The three parameters usually required to find the base addresses are the VENDOR ID, which is $114A, the DEVICE ID, which is $4320, and the REV ID, which is $C0. The Base Address Register 1 along with the information in Table 3-1 on page 52 (Programming), establishes the location of the CSR and SRAM, which are necessary to operate this board.

Calibration Procedures

The following sections provide calibration procedures for all voltage and current ranges of the VMIPCI-4320. The calibration procedures are based on the assumption that all outputs have been jumpered for the desired output mode and range. During the calibration procedures, the FAIL LED off bit (bit 11 of the Control Register) is set to a one and the TWO’S COMP bit (bit 10 of the Control Register) is set to a zero.

Refer to the following Sections for the specific calibration procedure:

0 to 10 V Output Range	Refer to "Calibration Procedure for 0 to 10 V Output Range" on page 37.
0 to 5 V Output Range	Refer to "Calibration Procedure for 0 to 5 V Output Range" on page 38.
±2.5 V Output Range	Refer to "Calibration Procedure for ±2.5 V Output Range" on page 39.
±5 V Output Range	Refer to "Calibration Procedure for ±5.0 V Output Range" on page 40.
±10 V Output Range	Refer to "Calibration Procedure for ±10.0 V Output Range" on page 41.

Note Calibration of the outputs to a specific range does not ensure that the outputs shall remain calibrated if the jumpers are then reconfigured.

Note Word or 16-bit writes to SRAM do not store the four Most Significant Bits (MSB.) This is due to the fact that the on-board Digital-to-Analog Converter (DAC) only uses 12 bits of data input.

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Calibration Procedure for 0 to 10 V Output Range

Setup:

1. Configure jumpers J9 and J10 for a unipolar and 10 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for voltage as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the FAIL LED off, straight binary format, and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustments (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the jumper installed across pin 4 of jumper blocks J1, J3, J4, J5, J6, J7, and J8. In each instance, the DMM should read +4.9988 ±0.0010 VDC.
9. Calibration of the analog outputs is completed. Remove power and all test connections.

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Calibration Procedure for 0 to 5 V Output Range

Setup:

1. Configure jumpers J9 and J10 for the unipolar and 5 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for voltage output as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install board in PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, which is the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0A80 to the CSR at relative address 0. This configures the boards for the Fail LED off, straight binary format and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +4.9988 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to jumper installed across pin 4 of jumper blocks J1, J3, J4, J5, J6, J7, and J8. In each instance, the DMM should read +2.4994 ±0.0010 VDC.
9. Calibration of the analog outputs is completed. Remove power and all test connections.

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Calibration Procedure for ±2.5 V Output Range

Setup:

1. Configure jumpers J9 and J10 for the bipolar and 5 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for voltage output as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, which is the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0A80 to the CSR at relative address 0. This configures the boards for the fail LED off, straight binary format, and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight (8) SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $800 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +2.4988 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the jumper installed across pin 4 of jumper blocks J1, J3, J4, J5, J6, J7, and J8. In each instance, the DMM should read +0.0000 ±0.0010 VDC.
9. Calibration of the analog outputs is completed. Remove power and all test connections.

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Calibration Procedure for ±5.0 V Output Range

Setup:

1. Configure jumpers J9 and J10 for the bipolar and 10 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for voltage, as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the FAIL LED off, straight binary format, and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $800 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R27 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +4.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the jumper installed across pin 4 of jumper blocks J1, J3, J4, J5, J6, J7, and J8. In each instance, the DMM should read +0.0000 ±0.0010 VDC.
9. Calibration of the analog outputs is completed. Remove power and all test connections.

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Calibration Procedure for ±10.0 V Output Range

Setup:

1. Configure jumpers J9 and J10 for the bipolar and 20 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for voltage as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0A80 to the CSR at relative address 0. This configures the board for the fail LED off, straight binary format, and voltage outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $800 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R27 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9951 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.
8. To verify that all channels are operational, sequentially move the DMM positive (+) lead to the jumper installed across pin 4 of jumper blocks J1, J3, J4, J5, J6, J7, and J8. In each instance, the DMM should read +0.0000 ±0.0010 VDC.
9. Calibration of the analog outputs is completed. Remove power and all test connections.

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Calibration Procedure for 4 to 20 mA Current Range

Setup:

1. Configure jumpers J9 and J10 for the unipolar and 10 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for the 4 to 20 mA current output as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0B80 to the CSR at relative address 0. This configures the board for the FAIL LED off, straight binary format, voltage and current outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.

Current Output Adjustments:

1. Disconnect the DMM from the previous setup. Program the DMM for current measurements with a range capable of reading 20 mA with a 1 µA resolution.
2. Connect the DMM positive (+) lead to CH0 output at pin 1 of the P1 connector. Connect the DMM negative (-) lead to AGND return at pin 20 of the P1 connector. (See Table 2-3 on page 50 for the P1 I/O connector pin assignments.)
3. Write $0800 to all eight SRAM locations representing the eight (8) outputs. Then write zero to the relative address of the SRAM location corresponding to the channel currently being calibrated (see Table 3-1). For CH0 the relative address is $10.
4. Locate the offset adjustment potentiometer corresponding to the channel being calibrated as indicated in Table 2-2 on page 35 and Figure 2-3 on page 50. Adjust this potentiometer for a DMM reading of 4.000 ±0.001 mA.
5. Write $0FFF to the relative address of the SRAM location corresponding to the channel being calibrated.

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6. Locate the Span adjustment potentiometer corresponding to the channel being calibrated as indicated in Table 2-2 on page 35 and Figure 2 on page 49. Adjust this potentiometer for a DMM reading of 19.996 ±0.002 mA.
7. The span adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore steps 3 through 6 must be repeated as many times as required.
8. Repeat steps 2 through 7 for all the appropriate channels 1 through 7.
9. Calibration is completed. Remove power and all test connections.

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Calibration Procedure for 0 to 20 mA Current Range

Setup:

1. Configure jumpers J9 and J10 for the unipolar and 10 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for the 0 to 20 mA current output as shown in Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0B80 to the CSR at relative address 0. This configures the board for the FAIL LED off, straight binary format, voltage and current outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.

Current Output Adjustments:

1. Disconnect the DMM from the previous setup. Program the DMM for current measurements with a range capable of reading 20 mA with a 1 µA resolution.
2. Connect the DMM positive (+) lead to CH0 output at pin 1 of the P1 connector. Connect the DMM negative (-) lead to AGND return at pin 20 of the P1 connector. See Table 2-3 on page 50 for the P1 I/O connector pin assignments.
3. Write $0800 to all eight SRAM locations representing the eight outputs. Then write zero to the relative address of the SRAM location corresponding to the channel currently being calibrated (see Table 3-1). For CH0, the relative address is $10.
4. Locate the offset adjustment potentiometer corresponding to the channel being calibrated as indicated in Table 2-2 on page 35 and Figure 2 on page 49. Adjust this potentiometer for a DMM reading of 0.005 ±0.001 mA.
5. Write $0FFF to the relative address of the SRAM location corresponding to the channel being calibrated.

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6. Locate the Span adjustment potentiometer corresponding to the channel being calibrated indicated in Table 2-2 on page 35 and Figure 2 on page 49. Adjust this potentiometer for a DMM reading of 19.995 ±0.002 mA.
7. The span adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, steps 3 through 6 must be repeated as many times as required.
8. Repeat steps 2 through 7 for all the appropriate channels 1 through 7.
9. Calibration is completed. Remove power and all test connections.

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Calibration Procedure for 5 to 25 mA Current Range

Setup:

1. Configure jumpers J9 and J10 for the unipolar and 10 V span as described in Table 2-1 on page 32.
2. Configure all appropriate outputs for the 5 to 25 mA current output as shown in Table 2-1 on page 32 and Figure 2-1 on page 33.
3. Install the board into a PCI bus host system, using the PCI bus extender board if necessary.
4. Connect the DMM positive (+) lead to the jumper installed at J2 pin 4, the output of the sample-and-hold buffer for channel 1. Connect the DMM negative (-) lead to the jumper installed at J2 pin 2, which is a local ground reference point.
5. Turn *ON* the PCI bus host system.

DAC Output Adjustments:

1. Write $0B80 to the CSR at relative address 0. This configures the boards for the FAIL LED off, straight binary format, voltage and current outputs enabled.
2. Write $800 to all the relative addresses corresponding to the eight SRAM / channel locations. This sets all outputs to the mid-scale setting.
3. Write $0 to CH1 SRAM location at relative address $12.
4. Adjust potentiometer R35 for a DMM reading of 0.000 ±0.0010 VDC.
5. Write $0FFF to CH1 SRAM location at relative address $12.
6. Adjust potentiometer R32 for a DMM reading of +9.9976 ±0.0010 VDC.
7. The gain adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, repeat steps 3 through 6 as many times as required.

Current Output Adjustments:

1. Disconnect the DMM from the previous setup. Program the DMM for current measurements with a range capable of reading 20 mA with a 1 µA resolution.
2. Connect the DMM positive (+) lead to CH0 output at pin 1 of the P1 connector. Connect the DMM negative (-) lead to AGND return at pin 20 of the P1 connector. See Table 2-3 on page 50 for the P1 I/O connector pin assignments.
3. Write $0800 to all eight SRAM locations representing the eight outputs. Then write 0 to the relative address of the SRAM location corresponding to the channel currently being calibrated (see Table 3-1). For CH0, the relative address is $10.
4. Locate the offset adjustment potentiometer corresponding to the channel being calibrated indicated in Table 2-2 on page 35 and Figure 2 on page 49. Adjust the potentiometer for a DMM reading of 5.000 ±0.001 mA.
5. Write $0FFF to the relative address of the SRAM location corresponding to the channel being calibrated.

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6. Locate the Span adjustment potentiometer corresponding to the channel being calibrated as indicated in Table 2-2 on page 35 and Figure 2 on page 49. Adjust the potentiometer for a DMM reading of 24.995 ±0.002 mA.
7. The span adjustment (steps 5 and 6) can alter the offset adjustment (steps 3 and 4) therefore, steps 3 through 6 must be repeated as many times as required.
8. Repeat steps 2 through 7 for all the appropriate channels 1 through 7.
9. Calibration is completed. Remove power and all test connections.

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Connector Descriptions

The VMIPCI-4320 has two connectors, P1 and P2. P1 is the external I/O connector, located on the rear mounting bracket. P2 is the PCI bus card slot connector.

Note Refer to your host computer's manual(s) for information on compatible mating connectors.

PCI Bus Connector (P2)

PCI bus systems can conform to one of several standards based on either 5 V or 3.3 V operation with a 32- or 64-bit PCI bus access. The PCI bus motherboard slots are keyed and the PCI bus card edge connectors are slotted to ensure compatibility. The VMIPCI-4320 was designed for a 5 V 32-bit PCI bus system. However, it is also compatible with a 5 V 64-bit PCI bus system.

Refer to your host computer's manual(s) for information on compatible PCI card types. Figure 2 on page 49 illustrates the P2 connector along with the Jumper locations. Signals marked with N/C have no connection on the VMIPCI-4320. The pin with reference designation "B1" is located on the component side of the board and is the pin closest to the rear mounting bracket. Likewise, the "A1" pin is located on the back side of the board and is the pin closest to the rear mounting bracket.

I/O Connector (P1)

P1 is a 37-pin D-Shell Subminiature Connector. Figure 2-3 on page 50 provides a view of the P1 connector, Table 2-3 on page 50 details the connector pinout assignments.

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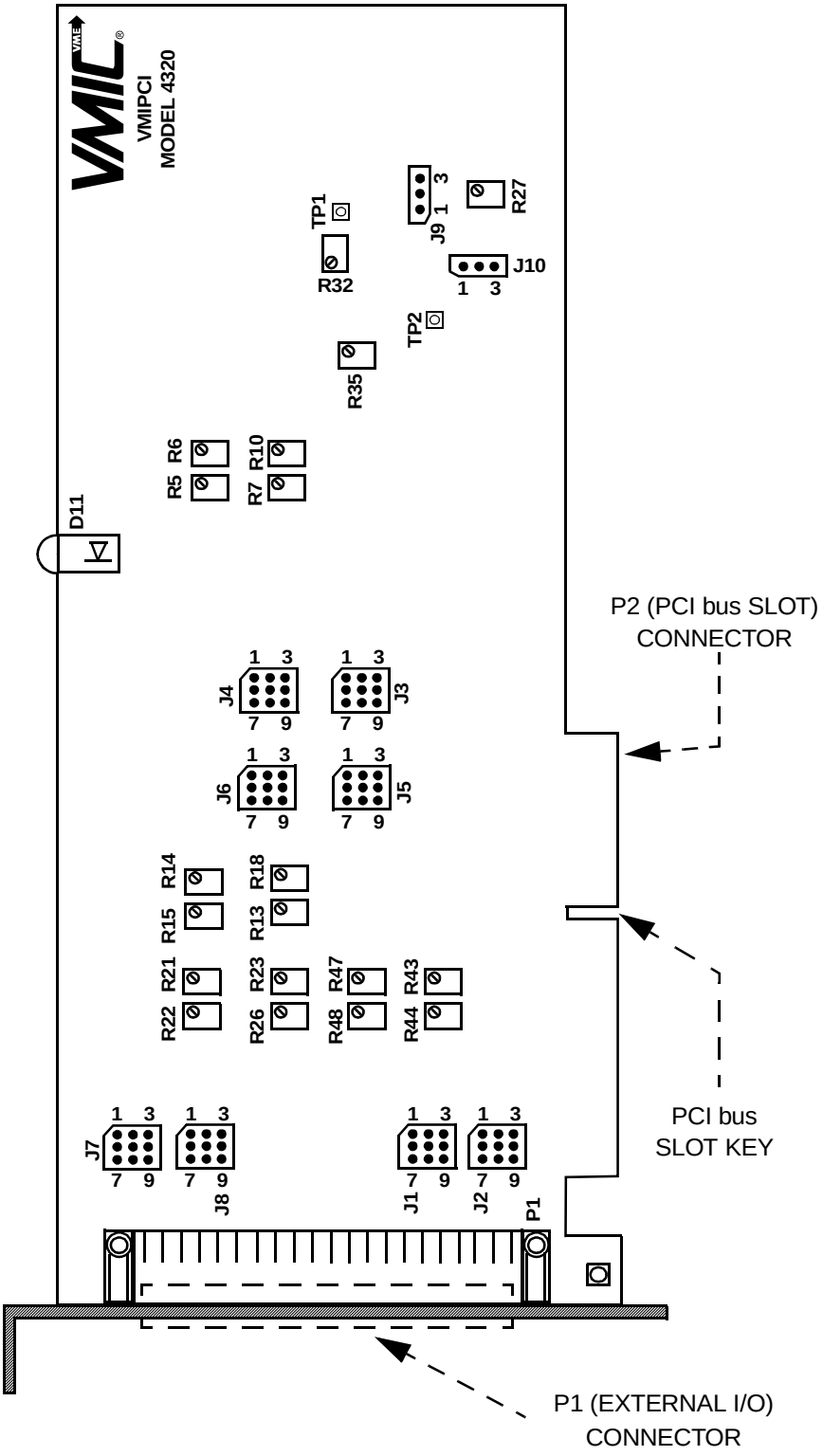


Figure 2-2 VMIPCI-4320 Jumper Locations, Potentiometers, and Test Points

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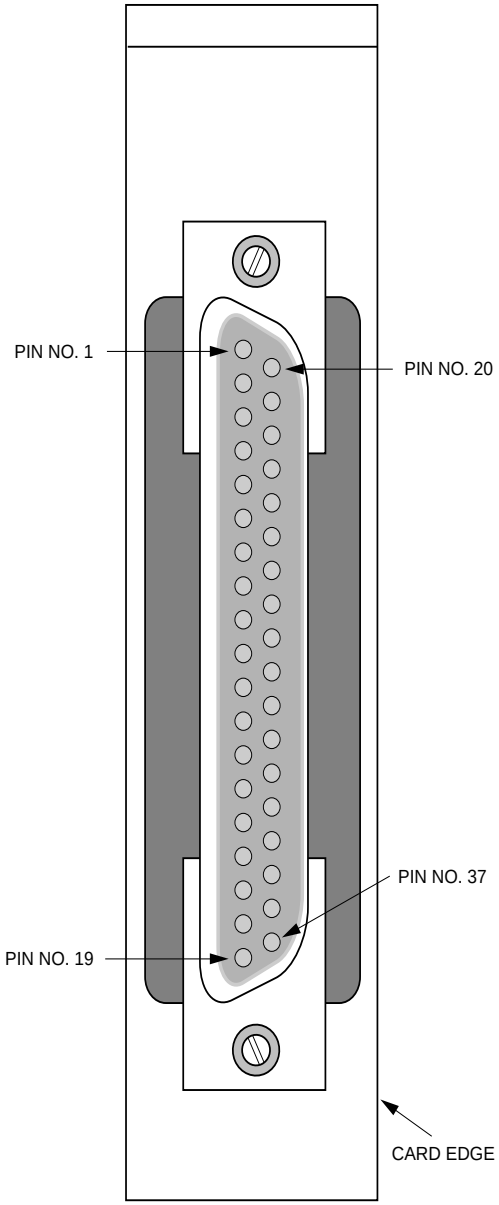


Figure 2-3 P1 Connector

Table 2-3 P1 Connector Pinout

Pin No.	Signal	Function
1	CHOUT0	Chan. 0 Output
2	CHOUT1	Chan. 1 Output
3	CHOUT2	Chan. 2 Output
4	CHOUT3	Chan, 3 Output
5	CHOUT4	Chan. 4 Output
6	CHOUT5	Chan. 5 Output
7	CHOUT6	Chan. 6 Output
8	CHOUT7	Chan. 7 Output
9	N / C	N / A
10	N / C	N / A
11	N / C	N / A
12	N / C	N / A
13	N / C	N / A
14	N / C	N / A
15	N / C	N / A
16	N / C	N / A
17	AGND	Analog Ground
18	N / C	N / A
19	EXT+V	EXT. Current Loop+
20	AGND	Analog Ground
21	AGND	Analog Ground
22	AGND	Analog Ground
23	AGND	Analog Ground
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AGND	Analog Ground
27	AGND	Analog Ground
28	AGND	Analog Ground
29	AGND	Analog Ground
30	AGND	Analog Ground
31	AGND	Analog Ground
32	AGND	Analog Ground
33	AGND	Analog Ground
34	AGND	Analog Ground
35	AGND	Analog Ground
36	N / C	N / A
37	EXT+V	EXT. Current Loop+

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System Considerations

Output Cables

Optimum performance is obtained if the cables consist of individually twisted and shielded pairs. Short of individually shielded pairs, twisted pairs with a group or bundle shield is recommended. P1 pins 17 and 20 through 35 serve as signal returns and to tie cable shields to the board AGND.

General Guidelines

The grounding scheme used can have a major effect on system performance. Each system has its own unique interface considerations, but the following general guidelines will apply in most cases.

1. Keep cables short, particularly in voltage output mode with high currents, to avoid voltage drops in cables.
2. Each output should have a separate AGND return to the VMIPCI-4320. An ample number of pins on the P1 connector were devoted to AGND for this purpose.

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CHAPTER

3

Programming

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Introduction

The PCI configuration registers, called Base Address Register #1 (BADR1) and Base Address Register #2 (BADR2), each contain a 32-bit address. This is the base address of the registers that apply to VMIPCI-4320. See Figure 3-1 on page 54 for a typical example of the Base Address Register addressing. A group of 64 byte addresses are dedicated to these functions. Of the 64 byte addresses, only the 32 even addresses should be used since all VMIPCI-4320 function-specific registers are organized as 16 bits wide. Any of the first eight even byte addresses with offsets $0 through $E access the VMIPCI-4320 Control and Status Register (CSR). The next 16 even addresses with offsets $10 through $2E access 16 SRAM locations. The first eight of these SRAM locations store the digital values that represent the eight analog outputs. The second eight SRAM locations are spares. All the byte address offsets $30 through $3F are reserved. A memory map of the VMIPCI-4320 is shown in Table 3-1 on page 54.

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Table 3-1 VMIPCI-4320 Memory Map

Relative Address (hex)	Function	Access Type
00 Through 0E	Control / Status Register (CSR)	Read / Write
10	SRAM Location 0 (Analog Output Channel 0 Data)	Read / Write
12	SRAM Location 1 (Analog Output Channel 1 Data)	Read / Write
14	SRAM Location 2 (Analog Output Channel 2 Data)	Read / Write
16	SRAM Location 3 (Analog Output Channel 3 Data)	Read / Write
18	SRAM Location 4 (Analog Output Channel 4 Data)	Read / Write
1A	SRAM Location 5 (Analog Output Channel 5 Data)	Read / Write
1C	SRAM Location 6 (Analog Output Channel 6 Data)	Read / Write
1E	SRAM Location 7 (Analog Output Channel 7 Data)	Read / Write
20 Through 2E	SRAM Location 8 through 15 (Spare)	Read / Write
30 Through 3E	(Reserved)	----------

Example: If either BADR1 or BADR2 contain the address 3040h, then the Control and Status Register is found at the address starting at 3040h and proceeds through 304Eh. The first SRAM location, location 0, is found at 3050h, with SRAM 1 at 3052h, SRAM 2 at 3054h, ending with SRAM 7 at location 305Eh. Each of these SRAM address contains a 16-bit data word that indicates the digital input voltage value coming in over the PCI bus. These values are sent to the on-board DAC and ultimately are sent to the analog output pins on the board's P1 connector as analog values of the digital input signals stored in each of the SRAM location.

```
-> f  114a 4320  0

Bus#  =  0                          Device_function# = 68
Dev  ID  =  4320                    Vendor ID = 114a
Status  =  0                        Command = 107
Class Code  =  ff0000               Rev ID = 80
Base Addr Req 0 = fe81
Base Addr Req 1 = fd81
Base Addr Req 2 = ffafff40
Base Addr Req 3 = 0
Base Addr Req 4 = 0
Base Addr Req 5 = 0
Exp ROM Base    = 0
Int pin = 0                         Int line = 0
->
```

Figure 3-1 Typical I/O (Regs 0 and 1) and Memory (Reg 2) Mapped Base Address Registers

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Control and Status Register Description

A PCI bus write to any of the first eight relative addresses (or base address + offset) loads the data into the Control Register. A PCI read of the first eight relative addresses returns the VMIPCI-4320 status. Several of the status bits echo the states of the corresponding bits in the Control Register while other status bits provide additional information or are fixed to a constant one or zero state.

Control Register Bit Assignments

Only five of the 16 possible data bits in the Control register have assigned functions. Those functions are detailed below:

Table 3-2 Control Register Bit Map

Control Register (Offset $00 through $0E) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved				LED_OFF	TWO'S COMP	V OUT ENABLE	I OUT ENABLE

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SCAN ENABLE	Reserved						

Control Register Bit Definitions

Bits 15 through 12 Reserved: Write to zero.

Bit 11 LED_OFF: When set to a logical "1", the fail LED is turned off.

Bit 10 Two's Complement: Setting this bit to a logical "0" causes the DAC coding format to be straight binary, a logical "1" sets the data format to two's complement of data bit 12.

Bit 09 V Out Enable: Setting this bit to a logical "1" enables the voltage outputs, setting this bit to "0" disables the voltage outputs.

Bit 08 I Out Enable: Setting this bit to a logical "1" enables the current outputs, setting this bit to "0" disables the current outputs.

Bit 07 Scan Enable: The refresh (scan) cycle is enabled when this bit is set to a logical "1".

Bits 06 through 00 Reserved: Write to zero.

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Status Register Bit Assignments

All 16 data bits of the status word are defined as either true status or a fixed state. The bit map and bit descriptions are detailed below:

Table 3-3 Status Register Bit Map

Status Register (Offset $00 through $0E) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fixed High				LED_OFF	TWO'S COMP	V OUT ENA	I OUT ENA

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SCAN ENABLE	Fixed Low				CHAN COUNT		

Status Register Bit Definitions

Bits 15 through 12 Fixed High: These four bits (MSBs) are factory fixed high and each will read as a logical "1."

Bit 11 LED_OFF: When read, this bit indicates the state of the Control Register bit 11 (fail LED).

Bit 10 Two's Complement: When read, this bit indicates the state of the Control Register bit 10 (Two's Complement).

Bit 09 V Out Enable: When read, this bit indicates the state of the Control Register bit 09 (V Out Enable).

Bit 08 I Out Enable: When read, this bit indicates the state of the Control Register bit 08 (I Out Enable).

Bit 07 Scan Halt: When read, this bit indicates the state of the Control Register bit 07 (I Out Enable).

Bits 06 through 03 Fixed Low: These four bits are factory fixed low and each will read as a logical zero "0".

Bits 02 through 00 CHAN Count: When read, these three bits indicate the current state of the channel counter.

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Initialization

When a system reset is applied to the board, all Control Registers are cleared to “zero.” Therefore the Fail LED shall be on, the voltage outputs are disconnected, the current outputs assume the minimum level appropriate for the jumpered mode, and the refresh cycle is disabled. The SRAM locations, upon power up, assume unknown states and should, therefore, first be prewritten through PCI writes before the Control Register output enables are asserted.

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Controlling the Analog Outputs

The eight analog output channels appear to the controlling processor as eight consecutive 12-bit words in the I/O or memory space assigned to the VMIPCI-4320 board. The memory map shown in Table 3-1 on page 54 lists the board-relative address of each output channel. Each analog output SRAM location supports both *read* and *write* operations, eliminating the need for corresponding shadow latches in the processor Random Access Memory (RAM) space.

Setting the Analog Outputs

Digital codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four Most Significant Bits (MSBs) (D15 to D12) will be ignored, and will not be retained for read back. Each output will respond to a new code within 792 µsec after the code is written to the output register. The Digital-to-Analog (D/A) coding conventions used by the D/A Converter (DAC) are shown below. A few examples are given in Table 3-4 on pages 56 and 57.

OUTPUT (straight binary) = (DAC_INPUT/4096) x (MAX_OUT - MIN_OUT) + MIN_OUT

where

DAC_INPUT ranges from 0 to 4095 decimal (0 to FFF HEX), MAX_OUT is the DAC output with FFF HEX as the input and MIN_OUT is the DAC output with "000" as the input.

OUTPUT (two's complement) = (MAX_OUT - MIN_OUT)/2 + (DAC_INPUT/4096) x (MAX_OUT - MIN_OUT)

where

DAC_INPUT ranges from -2048 to 2047 decimal (800 to 7FF HEX), MAX_OUT is the DAC output with 7FF HEX as the input and MIN_OUT is the DAC output with 800 HEX as the input.

Table 3-4 DAC Data Format and Coding

DAC DATA FORMAT							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	D	D	D	D

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
D	D	D	D	D	D	D	D

x = Undefined

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Table 3-4 DAC Coding (Continued)

UNIPOLAR RANGES			STRAIGHT BINARY			
OUTPUT	**0 TO +10 V**	**0 TO +5 V**	**D15**			**D0**
+FS LSB	+9.9975 V	+4.9988 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	XXXX	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001

BIPOLAR RANGES				OFFSET BINARY			
OUTPUT	**+10 V**	**+5 V**	**+2.5 V**	**D15**			**D0**
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	1000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	0000	0000	0000

BIPOLAR RANGES				TWO'S COMPLEMENT			
OUTPUT	**+10 V**	**+5 V**	**+2.5 V**	**D15**			**D0**
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	0111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	1000	0000	0000

CURRENT RANGES				STRAIGHT BINARY			
OUTPUT	**0 TO 20 mA**	**4 TO 20 mA**	**5 TO 25 mA**	**D15**			**D0**
+FS LSB	19.9951 mA	19.9951 mA	24.9951 mA	XXXX	1111	1111	1111
+1 / 2 FS	10.0000 mA	12.0000 mA	15.0000 mA	XXXX	1000	0000	0000
+1 LSB	0.0049 mA	4.0039 mA	5.0049 mA	XXXX	0000	0000	0001
ZERO	0.0000 V	4.0000 mA	5.0000 mA	XXXX	0000	0000	0000

x = Undefined

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Off-Line Operation

Setting the V Out Enable bit in the CSR connects and enables all channels configured as voltage outputs. While the V Out Enable bit is low, the voltage outputs are disconnected via an analog switch and appear as high impedance.

To enable outputs configured as current sources, both the V Out Enable bit (CSR bit 9) and the I Out Enable bit (CSR bit 8) must be set high. With the V Out Enable bit high (logical 1), setting the I Out Enable bit low (logical 0) forces all outputs configured as current sources to assume the minimum scale value for the jumpered range.

As mentioned earlier, the SRAM locations assume unknown states upon power up. To keep the outputs from assuming unpredictable levels, it is advisable to load the desired starting output levels into the SRAM prior to enabling the V Out Enable or I Out Enable bits.

Scan Enable

Setting the Scan Enable bit in the CSR high enables the refresh scanning cycles. If Scan Enable is set low with the outputs enabled, the outputs will quickly and unpredictably drift from their last set values. Under normal operation, the SRAM is first loaded with the initial values, then this control bit is set high and left high.

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Maintenance

Maintenance

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

1. Software
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components of adjacent boards are disturbed when inserting or removing the board from the PCI board slot
8. Quality of cables and I/O connections

User level repairs are not recommended. If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. *This RMA Number must be obtained prior to any return*.

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Maintenance Prints

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

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