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VMIPCI-5576
Fiber-Optic Reflective Memory with Interrupts

- High-speed, easy-to-use fiber-optic network (170 Mbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Up to 2,000 m between nodes and up to 256 nodes
- Data transferred at 6.2 Mbyte/s without redundant transfer
- Data transferred at 3.2 Mbyte/s with redundant transfer
- Any node on the network can generate an interrupt in any other node on the network or in all network nodes with a single command
- Error detection
- Redundant transmission mode for suppressing errors
- No processor overhead
- No processor involvement in the operation of the network
- Up to 1 Mbyte of Reflective Memory
- D32:D16:D8 memory access
- Single PCI 5 V slot, standard long card
- PCI target data bursts supported with 44 Mbyte/s transfer rates
- PCI master DMA controller. DMA transfer rates of 132 Mbyte/s maximum and 33 Mbyte/s sustained.
- Configurable endian conversions for multiple CPU architectures on the network
- Communication link compatible with VMIVME-5576 and VMIMB1-5576
- Software-addressable digital output bit available at output connector for use with optical switch board or any user-defined purpose
- Windows NT® OS driver available which operates the VMIPCI-5576 as a network interface board. Allows TCP/IP and other protocol connectivity on a network of VMIPCI-5576 or VMIVME-5576 nodes.

INTRODUCTION — The VMIPCI-5576 is a PCI bus board which may be used with other VMIC 5576 family boards to form a high-performance, daisy-chained, fiber-optic network. Data is transferred by writing to on-board global RAM. The data is automatically sent to the same location in memory on all Reflective Memory boards on the network. The Reflective Memory network can include PCI, VME, and Multibus systems. The network-compatible members of the 5576 family include the VMIVME-5576 and VMIMB1-5576.

PRODUCT OVERVIEW — The Reflective Memory concept provides a very fast and efficient way of sharing data across distributed computer systems.

VMIC's VMIPCI-5576 Reflective Memory interface allows data to be shared between up to 256 independent systems (nodes) at rates up to 6.2 Mbyte/s. Each Reflective Memory board may be configured with 256 Kbyte to 1 Mbyte of on-board SRAM. The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed fiber-optic data path to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize CPU and bus performance to maintain high data throughput.

The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. Three separate, user-definable interrupts may be used to synchronize a system process, or used to follow any data. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.



Ordering Options

January 14, 1998 800-855576-000 B	A	B	C	–	D	E	F
VMIPCI-5576 –			1	–			

A = Memory Options
0 = 256 Kbyte
1 = 512 Kbyte
2 = 1 Mbyte
B = FIFO Option
0 = 512 Transfer FIFO
1 = 4 K Transfer FIFO
C = 1 (Option reserved for future use)

Connector Data

Compatible Connector	*ST Connector*
PC Board Fiber-Optic Transmitter/Receiver	Fiber-Optic Receiver HFBR-2100 (Hewlett-Packard) Fiber-Optic Transmitter HFBR-1100 (Hewlett-Packard)

Cable Specifications

Fiber-Optic Cable – Multimode; 62.5 Micron core.
Transmitters operate at 1,300 nm at 170 Mbaud.
Maximum attenuation between nodes is 9 dB.
Minimum attenuation between nodes is .5 dB.

Fiber-Optic Cable Assemblies	A	B	C	–	D	E	F
VMICBL-000-F3 –				–			

A = Fiber-Optic Connector Type
0 = Ceramic Ferrule ST Connector
1 = Stainless Steel Ferrule ST Connector
BC = Cable Lengths

00 = Not Used	09 = 1,000 ft (304.8 m)
01 = 5 ft (1.5 m)	10 = 1,500 ft (457.3 m)
02 = 25 ft (7.6 m)	11 = 2,000 ft (609.7 m)
03 = 50 ft (15.2 m)	12 = 2,460 ft (750.0 m)
04 = 100 ft (30.4 m)	13 = 3,280 ft (1,000 m)
05 = 150 ft (45.7 m)	14 = 4,100 ft (1,250 m)
06 = 200 ft (60.9 m)	15 = 4,920 ft (1,500 m)
07 = 350 ft (106.7 m)	16 = 5,740 ft (1,750 m)
08 = 500 ft (152.4 m)	17 = 6,560 ft (2,000 m)

Note

VMIC offers single fiber cable assemblies that are compatible with the VMIVME-5576 in length ranging from 1.5 to 2,000 m. These cable assemblies are U.L./NEC-rated OFNP and have a 2.5 mm ST-style bayonet connector on each end.

For Ordering Information, Call:
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The VMIPCI-5576 requires no initialization unless interrupts are being used or endian byte swapping is desired.

Each node on the system has a unique identification number between 0 and 255. The node number is established during hardware system integration by placement of jumpers on the board. This node number can be read by software by accessing an on-board register. In some applications, this node number would be useful in establishing the function of the node.

In order to achieve an aggregate throughput of 6.2 Mbyte/s, nodes capable of writing to the Reflective Memory network at an aggregate rate of 6.2 Mbyte/s must be present.

LINK ARBITRATION — The VMIPCI-5576 system is a fiber-optic daisy chain ring as shown in Figure 1. Each transfer is passed from node-to-node until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives except those that it originated. Nodes are allowed to insert transfers between transfers passing through.

INTERRUPT TRANSFERS — In addition to transferring data between nodes, the VMIPCI-5576 will allow any processor in any node to generate an interrupt on any other node. These interrupts would generally be used to indicate to the receiving node that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving node is ready for new data.

Three interrupts are available. The user may define the function for each interrupt. Any processor can generate an interrupt on any other node on the network. In addition, any processor on the network can generate an interrupt on all nodes on the network. Interrupts are generated by simply writing to a VMIPCI-5576 register.

All data and interrupt command transfers contain the node number of the node that originated the transfer. This information is used primarily so the originating node can remove the transfer from the network after the transfer has traversed the ring. The node identification is also used by nodes receiving interrupt commands. When a node receives an interrupt command for itself, it places the identification number of the originating node in a FIFO. Up to 512 interrupts can be stacked in the FIFO. During the interrupt service routine, the identification of the interrupting node can be read from the FIFO.

PCI INITIATOR/DMA CAPABILITIES — The DMA capability is initiated by a PCI host. After the DMA engine is initialized by a host, the VMIPCI-5576 will request the PCI bus as appropriate and move up to 1 Mbyte as a PCI initiator. This capability removes the CPU from the responsibility of requesting the PCI bus and moving the data itself. This feature is very useful for moving large blocks of data. The PCI architecture ensures that the VMIPCI-5576 does not monopolize the PCI bus during this process. Large DMA blocks will automatically be split into smaller bursts on the PCI bus by the DMA engine. The VMIPCI-5576 can be programmed to issue a PCI interrupt at the conclusion of a DMA transfer or the host can poll the status of the DMA process. The status of the DMA can be accessed from the board, if required. Although the DMA engine can do both DMA reads and DMA writes, they cannot occur simultaneously. The VMIPCI-5576 can burst data onto the PCI bus at a maximum rate of 132 Mbyte/s and a sustained rate of 33 Mbyte/s. If the target operates at a slower rate, the PCI handshaking capabilities will throttle the data rate.

ERROR MANAGEMENT — Errors are detected by the VMIPCI-5576 with the use of the error detection facilities of the TAXI chipset and additional parity encoding and checking. When a node detects an error, the erroneous transfer is removed from the system and a PCI bus interrupt is generated, if enabled. The error rate of the VMIPCI-5576 is a function of the rate of errors produced in the optical portion of the system. This optical error rate depends on the length and type of fiber-optic cable. Assuming an optical error rate of 10^{-12}, the error rate of the VMIPCI-5576 is 10^{-10} transfers/transfer.

The VMIPCI-5576 can be operated in a redundant transfer mode in which each transfer is transmitted twice. In this mode of operation, the first of the two transfers is used unless an error is detected in which case the second transfer is used. In the event that an error is detected in both transfers, the node removes the transfer from the system. The probability of both transfers containing an error is 10^{-20}, or about one error every 3,731,000 years at maximum data rate.

ENDIAN CONVERSIONS — Data lane steering can be configured in a Control Register to allow CPUs of different architectures to communicate. Byte swap, Word swap, and Byte-Word swap options are available.

PROTECTION AGAINST LOST DATA — Data received by the node from the fiber-optic cable is error checked and placed in a receive FIFO. Arbitration with accesses from the PCI bus then takes place, and the data is written to the node's SRAM and to the node's transmit FIFO. Data written to the board from the PCI bus is placed directly into SRAM and into the transmit FIFO. Data in the transmit FIFO is transmitted by the node over the fiber-optic cable to the next node. Data could be lost if either FIFO were allowed to become full.

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The product is designed to prevent either FIFO from becoming full and overflowing. It is important to note the only way that data can start to accumulate in FIFOs is for data to enter the node at a rate greater than 6.2 Mbyte/s or 3.2 Mbyte/s in redundant mode. Since data can enter from the fiber and from the PCI bus, it is possible to exceed these rates. If the transmit FIFO becomes half-full, a bit in the Status Register is set. This is an indication to the node's software that subsequent WRITEs to the Reflective Memory should be suspended until the FIFO is less than half-full. If the half-full indication is ignored and the transmit FIFO becomes full, then writes to the Reflective Memory will be acknowledged with a STOP*. No data will be lost.

If the receive FIFO is allowed to become over half-full, there is a danger the receiver FIFO may overflow resulting in data loss. In order to prevent this situation, all PCI writes will be acknowledged by a STOP* until the receive FIFO is less than half-full.

NETWORK MONITOR — There is a bit in a Status Register that can be used to verify that data is traversing the ring (that is, the ring is not broken). This can also be used to measure network latency.

VMIC offers single fiber cable assemblies that are compatible with the VMIPCI-5576 in length ranging from 1.5 to 2,000 m. These cable assemblies are U.L./NEC-rated OFNP and have a 2.5 mm ST-style bayonet connector on each end.

SOFTWARE DRIVER — A Windows NT OS driver for the VMIPCI-5576 is available. The driver is NDIS compliant and supports the protocols configured into the Windows NT OS including TCP/IP. The driver operates the VMIPCI-5576 as a network interface board. A portion of the Reflective Memory is reserved by the driver for network use, and the remainder of memory is available as simple user-shared memory. When used as a network interface board, the VMIPCI-5576 has a dual role; the board provides both network connectivity as well as fast shared memory for distributed applications.

SPECIFICATIONS

PCI Transfer Rate: 44 Mbyte/s as a Target,
As DMA Initiator: 132 Mbyte/s maximum, 33 Mbyte/s sustained

Network Transfer Rate: 6.2 Mbyte/s (longword accesses) without redundant transfer
3.2 Mbyte/s (longword accesses) with redundant transfer

Memory Size: 256 Kbyte, 512 Kbyte, or 1 Mbyte
The 256 Kbyte, 512 Kbyte, and 1 Mbyte memory options of the VMIPCI-5576 all use 1 Mbyte of address space to locate data in the local node. Since the PCI bus is an automapped bus, all of these memory options must occupy 1 Mbyte of memory space on the PCI bus. This mapping structure allows these options to be compatible with VMIVME-5576 Reflective Memories of size 1 Mbyte and smaller.

INTERCONNECTION

Cable Requirements: Two fiber-optic cables

Cable Length: 2,000 m maximum between nodes

Configuration: Daisy chain ring up to 256 nodes

Power Requirements: 5.0 A maximum at +5 VDC

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 65 °C, operating with forced air cooling. -40 to 85 °C, storage.

Relative Humidity: 20 to 80 percent, noncondensing

DATA TRANSFERS

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the VMIPCI-5576 is shown in Figure 2.

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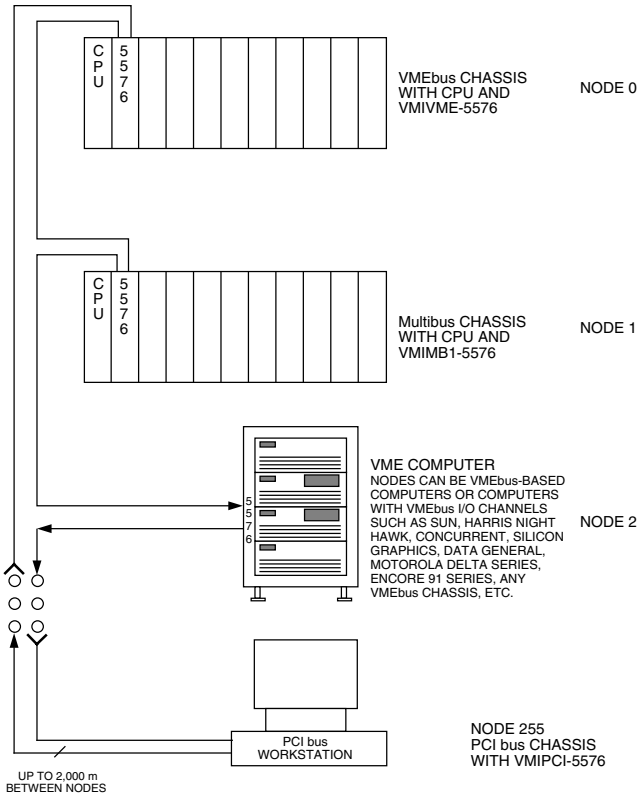


Figure 1. Network Example Using Reflective Memory System

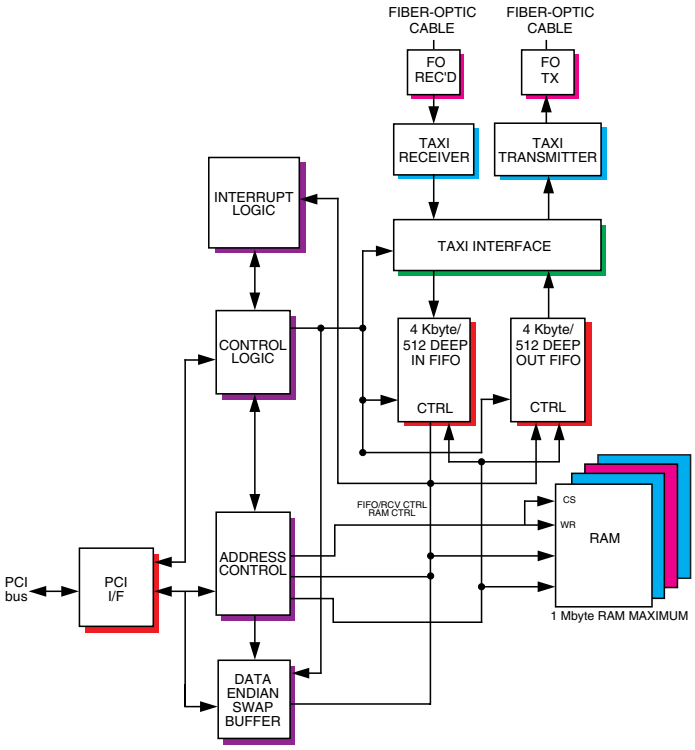


Figure 2. VMIPCI-5576 Functional Block Diagram

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