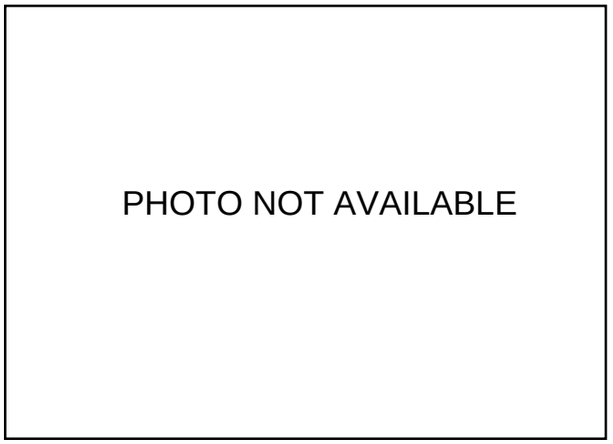
VMISBS-5521L
SBus-to-VMEbus Adapter

- Supports A32, A24, A16, D32, D16, D8 master(s) and slave(s) in the VMEbus chassis
- User-configured software transparent default address mapping mode
- Software-controlled dynamic address mapping mode
- Generates all VMEbus signals required of a VMEbus master
- Link consists of one 6U VMEbus board, one single-slot SBus board, and a variety of cable lengths
- Meets ANSI/IEEE STD 1014-1987 and SBus specification B.0



PRODUCT OVERVIEW — The VMISBS-5521L is a high performance SBus-to-VMEbus link. This link allows an SBus host, such as an SPARC workstation, to function as a VMEbus master in a remote VMEbus chassis. The VMISBS-5521L can function as a master controlling an external VMEbus chassis; or if placed in slot one of the VMEbus, can function as the only master in the chassis.

CONFIGURATION — The VMISBS-5521L consists of two boards and an interconnecting cable. One board is an interrupting SBus single-slot slave and the other board is a 6U form factor VMEbus master. Figure 1 is a block diagram of the VMISBS-5521L.

OPERATION — All single SBus cycles to the slot containing the SBus slave board are repeated to memory-mapped cycles in the VMEbus chassis. SBus burst transfers and VMEbus block transfers are not supported. If the cycle addresses a VMEbus slave, the link completes the SBus cycle with the correct SBus acknowledgement. If no slave is addressed, or does not respond within 4 µs, the SBus cycle is completed with an error acknowledge. VMEbus interrupts may be individually configured by the user for handling by the SBus CPU or by a local VMEbus CPU.

SOFTWARE TRANSPARENT AND/OR DYNAMIC ADDRESS MAPPING — The VMISBS-5521L provides mapping registers for translating SBus slot address cycles into VMEbus address space cycles. The user may configure the power up default values for the Mapping Registers. Thus, when the number of mapping regions described below are sufficient for the application, the link is completely software transparent at power up and requires no additional initialization. When access to additional VMEbus address spaces are required, the user-defined default values in the Mapping Registers may be dynamically modified under program control.

VMEbus ADDRESS MAPPING — In A25 SBus systems, the VMISBS-5521L register space and the VMEbus supervisory and nonprivileged short I/O (A16) address spaces are mapped into the SBus slot address space by default. In addition, three user-configurable mapping regions provide access for up to 8 Mbyte of VMEbus address space each. One mapping region provides access to supervisory or nonprivileged VMEbus standard (A24) data space. Another mapping region provides access to supervisory or nonprivileged VMEbus standard (A24) data space. The third mapping region provides access to any VMEbus address space, except for VMEbus block transfer spaces.

In A28 SBus systems, the VMISBS-5521L register space, the VMEbus supervisory and nonprivileged short I/O (A16) address spaces, and the supervisory and nonprivileged VMEbus standard (A24) data spaces are available by default. In addition, two user-configurable mapping regions provide access for up to 16 Mbyte of VMEbus address space each. One mapping region provides access to supervisory or nonprivileged extended (A32) data space. The other mapping region provides access to any VMEbus address space, except for VMEbus block transfer spaces.

VMEbus BUS MASTER OPERATION — The VMISBS-5521L operates in single cycle mode. Each access to the VMEbus may require the VMISBS-5521L to arbitrate for VMEbus mastership. This will extend the Bus cycle. The VMISBS-5521L is a Release-on-Request (ROR)

Ordering Options

Feb. 18, 1994 800-605521-000 D	A	B	C	–	D	E	F
VMISBS-5521L –	0			–			

ABC = Cable Lengths
010 = 10-foot Cable
020 = 20-foot Cable
025 = 25-foot Cable

Note

VMISBS-5521L-025 consists of a VMEbus Board, an SBus Board, and a 25-foot cable.

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VMEbus master, thus, arbitration may not be required every cycle. VMEbus arbitration will never be required when the VMISBS-5521L is the only bus master in the VMEbus chassis.

EXPANSION — VMIC offers a variety of VME-to-VME repeaters, VME-to-VME DMA links, and Reflective Memory products that provide data communications between VMEbus chassis.

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to +55 °C, operating
-20 to +85 °C, storage

Relative Humidity Range: 20 to 80 percent, noncondensing

Cooling: Convection

Size: Double Eurocard form factor (VMEbus Board)
SBus form factor (SBus Board)

POWER

Requirement:
5 V at 4.5 A (estimate for VME board)
5 V at 1.5 A (estimate for SBus board)

TIMING

	Read	Write
Interface Overhead:		
SBus SEL*(L) to VMEbus DSA*	790 ns	830 ns
VMEbus DTACK*(L) to SBus ACK (2:0)	460 ns	340 ns

Transfer Rate*:
1.88 µs per read cycle (2.1 Mbyte/s)
1.37 µs per write cycle (2.9 Mbyte/s)

Maximum VMEbus Slave Response Time Tolerated: 4 µs (maximum)

CONNECTION

Requirement: One 80-conductor round cable, up to 25 feet long

TRADEMARKS

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* This specification item was measured using the following system configuration:
a. A Force SRAM-5 Memory board as the target slave.
b. The VMEbus portion of the VMISBS-5521 is in Slot 1 of the VMEbus chassis.
c. The SBus portion of the VMISBS is in a SUN IPC workstation.
d. The cable length is 25 feet.

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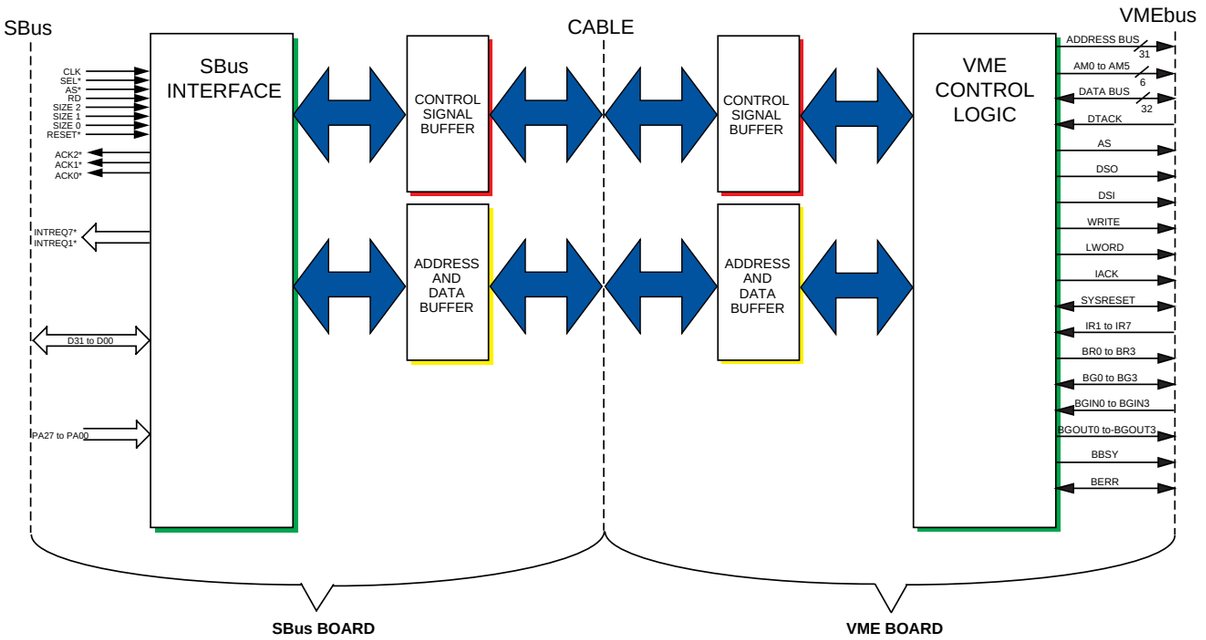

Figure 1. VMISBS-5521L Block Diagram

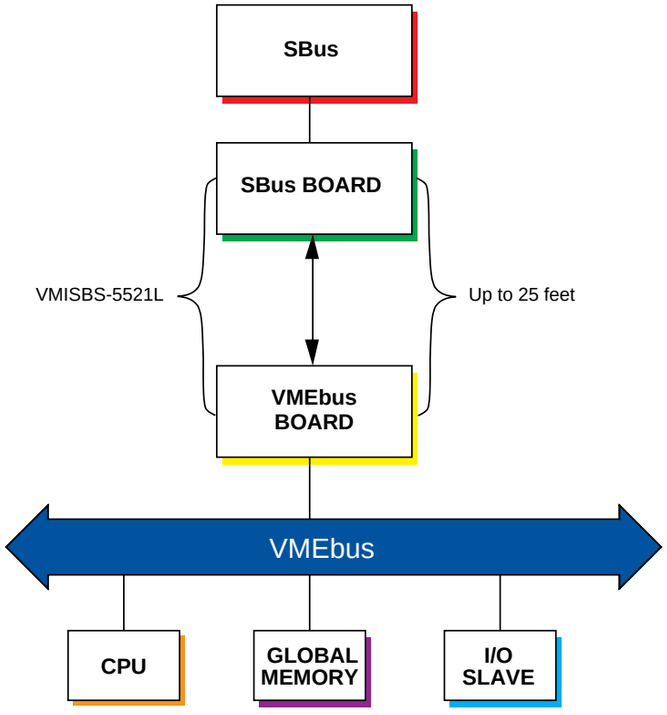

Figure 2. Typical Configuration Utilizing the VMISBS-5521L Extender Link