ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Abaco Systems / VMIC VMIVME-1160A-123* at our website: *Click HERE*

VMIVME-1160
32-BIT OPTICALLY COUPLED DIGITAL INPUT WITH CHANGE-OF-STATE INTERRUPTS

FEATURES

- 32 OPTICALLY COUPLED DIGITAL INPUTS
- 5 V TO 48 VDC INPUT RANGE
  - VOLTAGE SOURCING
  - CURRENT SINK/CONTACT SENSE
- HIGH ISOLATION
- INPUT DEBOUNCING OPTION
- CHANGE-OF-STATE INTERRUPTS ON ANY OF SEVEN LEVELS ELIMINATE CPU POLLING OVERHEAD
- POSITIVE OR NEGATIVE TRUE INPUT OPTIONS
- NON-PRIVILEGED OR SUPERVISORY SHORT I/O TRANSFERS
- HIGH RELIABILITY DIN TYPE CONNECTORS
- 8- OR 16-BIT TRANSFERS
- DOUBLE EUROCARD FORM FACTOR

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 South Memorial Parkway
Huntsville, Alabama 35803
(205) 880-0444 Fax No.: (205) 882-0859
1-800-322-3616

Revised 24 April 1992
Specifications subject to change without notice.
Copyright © January 1986 by VMIC
Document No.: 800-001160-000 C

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-1160
32-BIT OPTICALLY COUPLED DIGITAL INPUT WITH CHANGE-OF-STATE INTERRUPTS

SPECIFICATIONS

FUNCTIONAL CHARACTERISTICS

COMPATIBILITY: The VMIVME-1160 is a standard, double height printed circuit board that is electrically and mechanically compatible with the VMEbus

INPUT ORGANIZATION: Four input ports, each eight bits wide. The ports are arranged as four contiguous 8-bit, read only registers.

ADDRESSING SCHEME: Four 8-bit ports, individually addressable on 8-bit or 16-bit boundaries

BOARD ADDRESS: The board address is selected by on-board DIP switches. Operation is supported in any slot on the VMEbus backplane, except slot one.

VMEbus ACCESS: Address modifier bits are decoded to support either short supervisory or non-privileged short I/O access. A single jumper is provided to support this option, and is factory-configured for short supervisory I/O access.

DATA TRANSFER TYPE: D8, D16

ACCESS TIME: 250 ns maximum

DATA POLARITY: Order as positive true or negative true*

INTERRUPTS

TYPE: VMEbus slave/interrupter; ROAK

LEVELS: Any of the seven available interrupt levels I(1) - I(7)

INTERRUPT EVENT: Each 8-bit input port is assigned an interrupt level. A COS of any bit(s) in a port causes an interrupt to be generated at the assigned level.

INTERRUPT VECTOR LOCATION: D08(O)

INPUT CHARACTERISTICS

SIGNAL CONDITIONING: Inputs can be either voltage sourcing or current sink/contact sense with voltages accepted in the range from 5 V to 48 V.

INPUT VOLTAGE OPTIONS: Input voltage can be ordered as 5 V, 12 V, 24 V, or 48 V. Typical input circuit configurations are illustrated in Figure 1. Detailed specifications are provided in Tables 1 through 4.

INPUT CONFIGURATIONS:
- Voltage Sensing
- Voltage Source or Logic Level
- Current Sink or Contact Sense

*Refer to definition on page 2.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DEBOUNCE SELECTION:	Debounce capacitors for all 32 inputs are available, with standard time constants of 2 µs, 10 µs, or 1 ms
ISOLATION:	10 Megohms, minimum
ISOLATION VOLTAGE:	1,000 V maximum sustained voltage; 7,500 V for one second

PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

DIMENSIONS:	Standard VME double width board (166 mm x 233.4 mm x 12 mm)
INPUT CONNECTOR:	One 64-pin DIN connector
AMBIENT TEMPERATURE:	Operating, 0 °C to +55 °C Storage, -20 °C to +85 °C
HUMIDITY:	20 percent to 80 percent, non-condensing
COOLING:	Convection
POWER REQUIREMENTS:	+5 VDC @ 1.1 Amps (typical), 2.1 Amps (maximum)

OPERATIONAL OVERVIEW

This product is designed with standard COS control and interrupt logic that detects any COS and provides an interrupt vector to the byte level. It incorporates an MC68153 Bus Interrupter Module (BIM) and interrupts are supported on any of seven levels.

Each byte (8 bits) of input may have a unique interrupt vector that is generated upon a COS in any bit of that byte. This product also has an Interrupt Enable Register which is used to allow interrupts to be enabled on a byte-by-byte basis. The input data may be accessed as a D8 or D16 transfer.

A functional block diagram of this product is shown in Figure 2. Interrupts are generated on any COS (positive or negative transition). Polarity is determined by reading the input port after the COS interrupt.

NOTE

STATE CHANGES THAT OCCUR DURING THE INTERRUPT PROCESSING WINDOW (INTERNAL REQUEST TO INTERRUPT ACKNOWLEDGE CYCLE COMPLETE) WILL NOT BE DETECTED. THE TIME BETWEEN USER INPUT STATE CHANGES MUST NOT BE LESS THAN THE COMPUTER INTERRUPT PROCESSING TIME; OTHERWISE, THE STATE CHANGES WILL BE LOST.

POSITIVE/NEGATIVE TRUE ORDERING INFORMATION

This board may be ordered with positive or negative true data. For positive true boards, when current flows in the opto-isolator diode a logical "one" will be presented to the VMEbus.

For negative true boards when current flows in the opto-isolator diode a logical "zero" will be presented to the VMEbus. In either case the data sent to the BIM is always positive true and not affected by the ordering option.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

RELATED PRODUCTS AND APPLICATIONS

VMIC offers a broad range of digital I/O products for VMEbus systems and supports these products with comprehensive appplications information. Contact the factory for a description of current products.

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Board Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

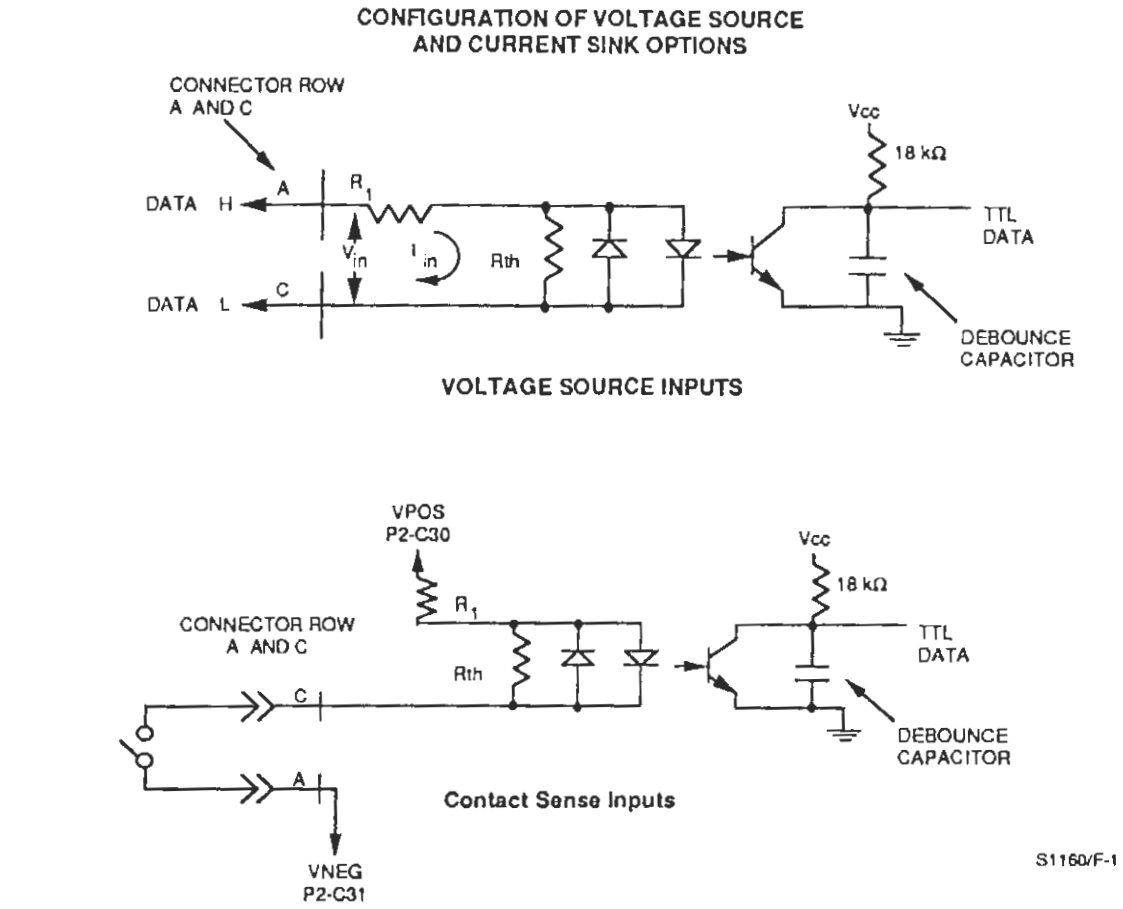


Figure 1. Typical Voltage Source and Contact Sense Signal Conditioning

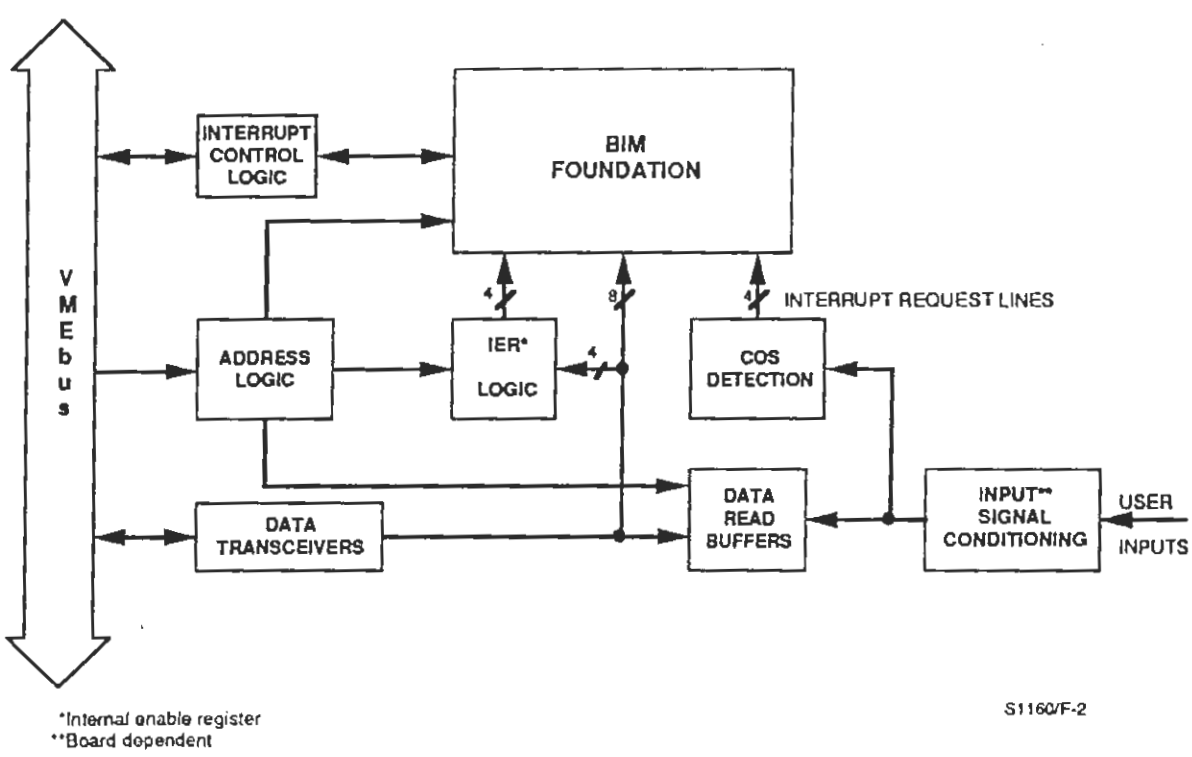


Figure 2. VMIVME-1160 Functional Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 1. 5-V Option

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IH} - HIGH THRESHOLD VOLTAGE	————	3.6	2.6	—	V
V_{IL} - LOW THRESHOLD VOLTAGE	————	—	2.6	1.6	V
I_{IH} - HIGH VOLTAGE CURRENT	VIN = 5 VDC	—	—	3.1	mA
I_{IL} - LOW VOLTAGE CURRENT	VIN = $V_{IL(MIN)}$	—	—	0.7	mA

Typical turn-on current is 1.43 mA at VIN = 2.6 V.
Absolute maximum input voltage is ± 12 VDC.

S1160/T-1

Table 2. 12-V Option

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IH} - HIGH THRESHOLD VOLTAGE	————	9.2	5.9	—	V
V_{IL} - LOW THRESHOLD VOLTAGE	————	—	5.9	3.4	V
I_{IH} - HIGH VOLTAGE CURRENT	VIN = 12 VDC	—	—	3.4	mA
I_{IL} - LOW VOLTAGE CURRENT	VIN = $V_{INL(MIN)}$	—	—	0.7	mA

Typical turn-on current is 1.43 mA at VIN = 5.9 V.
Absolute maximum input voltage is ± 22 VDC.

S1160/T-2

Table 3. 24-V Option

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IH} - HIGH THRESHOLD VOLTAGE	————	21.3	12.9	—	V
V_{IL} - LOW THRESHOLD VOLTAGE	————	—	12.9	6.9	V
I_{IH} - HIGH VOLTAGE CURRENT	VIN =24 VDC	—	—	2.9	mA
I_{IL} - LOW VOLTAGE CURRENT	VIN = $V_{INL(MIN)}$	—	—	0.7	mA

Typical turn-on current is 1.43 mA at VIN =12.9 V.
Absolute maximum input voltage is ± 34 VDC.

S1160/T-3

Table 4. 48-V Option

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IH} - HIGH THRESHOLD VOLTAGE	————	43.2	27.0	—	V
V_{IL} - LOW THRESHOLD VOLTAGE	————	—	27.0	13.9	V
I_{IH} - HIGH VOLTAGE CURRENT	VIN = 48 VDC	—	—	2.7	mA
I_{IL} - LOW VOLTAGE CURRENT	VIN = $V_{INL(MIN)}$	—	—	0.7	mA

Typical turn-on current is 1.43 mA at VIN = 27.0 V.
Absolute maximum input is ± 50 VDC.

S1160/T-4

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

32-bit OPTICALLY COUPLED DIGITAL INPUT WITH CHANGE-OF-STATE

ORDERING INFORMATION

VMIVME - 1160 - ABC

- **A** — FILTER OPTIONS
  - 0 = No Filter
  - 1 = 2 µs Filter
  - 2 = 10 µs Filter
  - 3 = Reserved Filter
  - 4 = 1 ms Filter
- **B** — INPUT VOLTAGE
  - 0 = TTL and 5 VDC
  - 1 = 12 VDC
  - 2 = 24 VDC
  - 3 = 48 VDC
- **C** — DATA POLARITY, INPUT TYPE
  - 1 = Positive True, Voltage Source, Logic Input*
  - 2 = Negative True, Voltage Source/Logic Input*
  - 3 = Positive True, Contact Sense
  - 4 = Negative True, Contact Sense
- **VMIVME - 1160** — MODEL NO.

*TTL compatible.

CONNECTOR DATA

COMPATIBLE CABLE CONNECTOR	PANDUIT NO. 120-964-435E
STRAIN RELIEF	PANDUIT NO. 100-000-032
P.C. BOARD HEADER CONNECTOR	PANDUIT NO. 120-964-033A

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-1160

32-BIT OPTICALLY COUPLED DIGITAL INPUT BOARD WITH CHANGE-OF-STATE DETECTION

INSTRUCTION MANUAL

DOCUMENT NO. 500-001160-000

10 August 1992

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, AL 35803-3308
(205) 880-0444
1-800-322-3616

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, VMIC assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

VMIC reserves the right to make any changes, without notice, to this or any of VMIC's products to improve reliability, performance, function, or design.

VMIC does not assume any liability arising out of the application or use of any product or circuit described herein; nor does VMIC convey any license under its patent rights or the rights of others.

VME Microsystems International Corporation

All Rights Reserved

This document shall not be duplicated, nor its contents used for any purpose, unless granted express written permission from VMIC.

Copyright © January 1986 by
VME Microsystems International Corporation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIC

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	10/10/88	Release Manual	88-0048
B	11/08/88	Appendix B	88-0321
C	04/11/89	Cover, page ii, Section 6, and Appendix A	88-0370
D	07/25/89	Cover, page ii, and Appendix A	89-0057
E	08/14/89	Cover, page ii, and Appendix A	89-0113
F	02/16/90	Cover, page ii, and Appendix A	89-0184
G	10/17/90	Cover, page ii, and Appendix A	90-0143
H	10/17/90	Cover, pages ii, 1-1, 1-3, 5-5, 5-8, and Appendix A	90-0169
J	02/21/91	Cover, pages ii, 1-3, Section 2, 3-2, 4-2, 4-3, 4-4, Section 6, and Appendix A	91-0011
K	04/05/91	Cover, pages ii, and 2-9	91-0107
L	10/21/91	Cover, page ii, and Appendix A	91-0255
M	04/24/92	Cover, page ii, Sections 2, 6, and Appendix A	92-0093
N	08/10/92	Cover, pages ii, and 5-9	92-0284

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SAFETY SYMBOLS

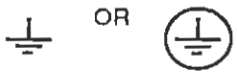
General Definitions of Safety Symbols Used in this Manual.



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



OR

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



OR

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-1160

32-BIT OPTICALLY COUPLED DIGITAL INPUT BOARD WITH CHANGE-OF-STATE DETECTION

TABLE OF CONTENTS

Page

SECTION 1. INTRODUCTION

1.1 INTRODUCTION 1-1
1.2 FUNCTIONAL DESCRIPTION 1-3
1.3 REFERENCE MATERIAL LIST 1-4

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. THEORY OF OPERATION

3.1 BLOCK DIAGRAMS 3-1
3.2 INTERRUPT FUNCTIONS 3-1
3.3 PRIORITY INTERRUPT SUBSYSTEM 3-11

SECTION 4. PROGRAMMING

4.1 OPERATIONAL OVERVIEW 4-1

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 CONFIGURATION SWITCHES 5-1
5.4 CURRENT SINK, VOLTAGE SOURCE SELECTION 5-3
5.5 EXTERNAL PULL-UP VOLTAGE 5-3
5.6 ADDRESS MODIFIERS 5-3
5.7 ADDRESS SELECTION SWITCHES 5-3
5.8 CONNECTOR PIN CONFIGURATION 5-4
5.9 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION 5-5

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE OF CONTENTS (CONTINUED)

Page

SECTION 6. MAINTENANCE AND WARRANTY

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1
6.3 WARRANTY 6-1
6.4 OUT-OF-WARRANTY REPAIR POLICY 6-2
6.4.1 Repair Category 6-3
6.4.2 Repair Pricing 6-3
6.4.3 Payment 6-3
6.4.4 Shipping Charges 6-4
6.4.5 Shipping Instructions 6-4
6.4.6 Warranty on Repairs 6-4
6.4.7 Exclusions 6-4

LIST OF FIGURES

Figure Page

1.1-1 Typical COSMODULE™ Functional Block Diagram 1-2
3.1-1 VMIVME-1160 Functional Block Diagram 3-2
3.1-2 Address Section Block Diagram 3-3
3.1-3 Control Section Block Diagram 3-4
3.1-4 Data Section Block Diagram 3-5
3.1-5 VMEbus Signal Lines Used by the VMIVME-1160 3-6
3.1-6 BIM Foundation Section Block Diagram 3-7
3.1-7 Typical IER Logic Section 3-8
3.1-8 Typical Change-of-State Detection Logic Section 3-8
3.1-9 Input Data Registers Block Diagram 3-9
3.1-10 Signal Conditioning Block Diagram 3-10
4.1-1 VMIVME-1160 Programming Flow Diagram 4-5
5.3-1 Locations of Jumpers and Address Switches 5-2
5.7-1 Data Register Address Select Switches 5-4
5.8-1 Typical Input Channel 5-4
5.9-1 Cable Connector Configuration 5-6
5.9-2 P3 Connector Pin Layout 5-7
5.9-3 P2 Connector Pin Layout 5-8

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE OF CONTENTS (Concluded)

LIST OF TABLES

Table		Page
1.1-1	COSMODULE™ Product Line Summary	1-3
4.1-1	Register Map	4-1
4.1-2	Typical Input Data Register Bit Maps	4-2
4.1-3	Typical BIM Control Register Map	4-3
4.1-4	Typical BIM Vector Register Map	4-4
5.9-1	P2 Connector Pin Assignment	5-9
5.9-2	P3 Pin-Channel Assignment	5-10

APPENDICES

A Assembly Drawing, Parts List, and Schematic
B MC68153 BIM Data Sheet

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 1

INTRODUCTION

1.1 INTRODUCTION

VME Microsystems International Corporation (VMIC) manufactures a complete line (see Table 1.1-1) of Change-of-State Boards (COSMODULES™). Each COSMODULE™ is designed with standard Change-of-State (COS) control and interrupt logic that detects any change-of-state and provides an interrupt vector to the byte level. Each board incorporates an MC68153 Bus Interrupter Module and interrupts are supported on any of the seven levels.

A block diagram of a typical COSMODULE™ is shown in Figure 1.1-1. Input signal conditioning is option-dependent and provides a wide variety of inputs ranging from standard TTL to high voltage DC or AC. The COSMODULE™ product line provides optically coupled inputs, voltage sourcing inputs, or current sinking inputs, for applications in limit switch sensing, low voltage detection, relay contact monitoring, relay coil voltage monitoring, and out-of-limits detection (two channels of the VMIVME-1001 are required).

Interrupts are generated on any change-of-state (positive or negative transition). Polarity is determined by reading the input port after the change-of-state interrupt.

NOTE:
STATE CHANGES THAT OCCUR DURING THE INTERRUPT PROCESSING WINDOW (INTERNAL REQUEST TO INTERRUPT ACKNOWLEDGE CYCLE COMPLETE) WILL NOT BE DETECTED. THE TIME BETWEEN USER INPUT STATE CHANGES MUST NOT BE LESS THAN THE COMPUTER INTERRUPT PROCESSING TIME; OTHERWISE, THE STATE CHANGES WILL BE LOST.

A Change-of-State Application Guide that describes the complete COSMODULE™ product line, VMIC's Document No. 825-000000-002, is available from VMIC. A summary of the COSMODULE™ product line is provided in Table 1.1-1 for reference.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

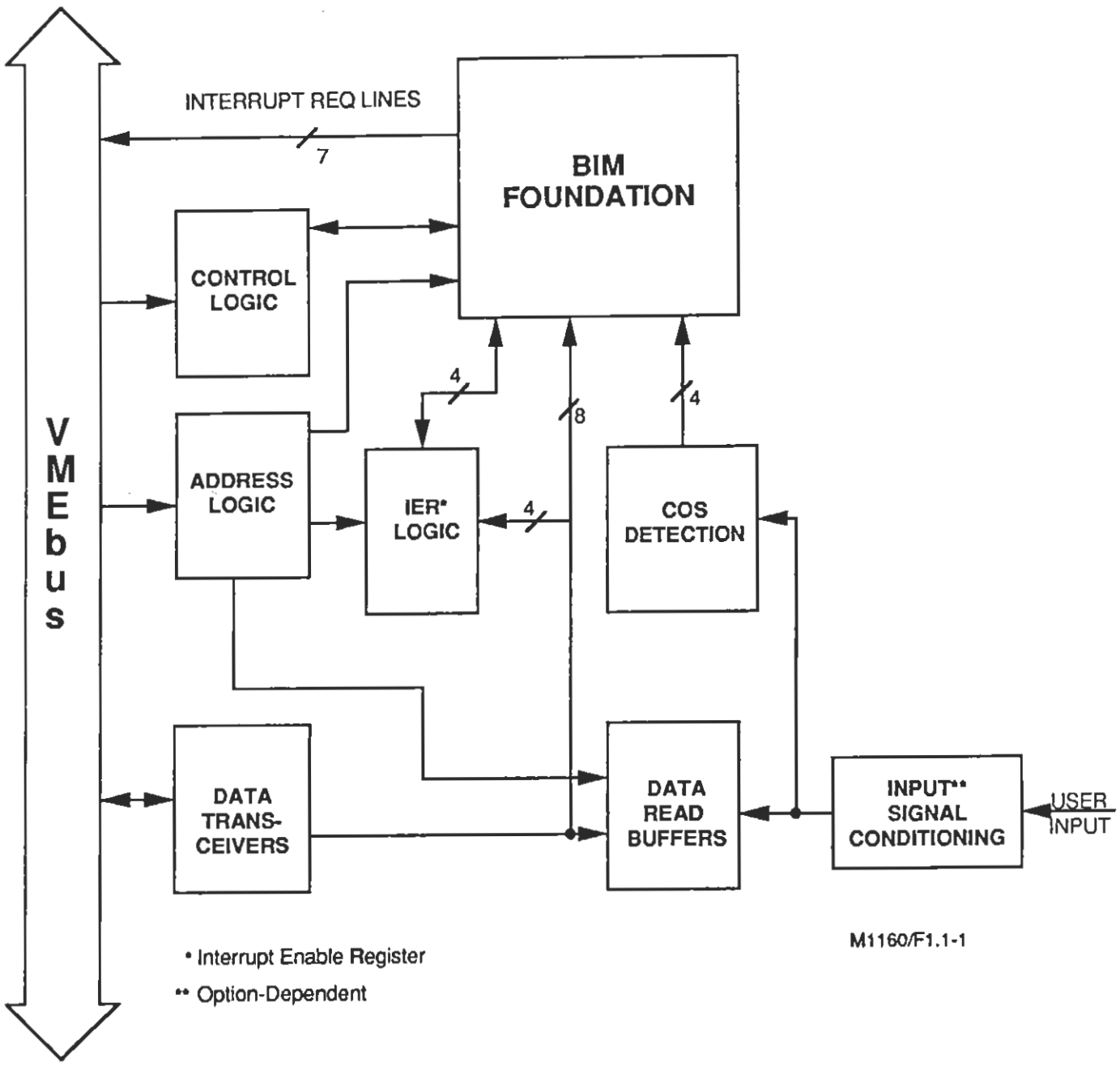


Figure 1.1-1. Typical COSMODULE™ Functional Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 1.1-1. COSMODULE™ Product Line Summary

ITEM NO.	DESCRIPTION	MODEL NO.	TRANSFER TYPE
1.	16-Channel AC or DC High Voltage (5 V to 240 V) Optically Coupled Input with Change-of-State Interrupt	VMIVME-1001	D8,D16
2.	32-Bit TTL Digital Input with Change-of-State Interrupt	VMIVME-1101	D8,D16
3.	32-Bit High Voltage (5 V to 50 V) Digital Input with Change-of-State Interrupt	VMIVME-1180	D8,D16
4.	32-Bit Optically Coupled Digital Input with Change-of-State Interrupt	VMIVME-1160	D8,D16

M1160/T1.1-1

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-1160 provides 32 high voltage, optically coupled inputs with change-of-state detection and vectoring to the byte level. The interrupt functions are supported by an MC68153 Bus Interrupter Module. The major features of the VMIVME-1160 are:

a. Quad 8-bit ports
b. Change-of-State port identified with interrupt vector
c. Voltage sourcing or current sinking signal conditioning
d. Double-wide Eurocard form factor with front panel
e. 8-, 16-bit transfers
f. 64-pin DIN type input connector
g. Jumper-selectable supervisory or nonprivileged data transfers
h. Optically coupled inputs

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-001160-000 SPECIFICATION

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

The VMIVME-1160 consists of eight functional building blocks as illustrated in Figure 3.1-1. The eight sections of the VMIVME-1160 are: (1) Address Logic; (2) Control Logic; (3) Data Logic; (4) Bus Interrupter Module (BIM) Logic; (5) Interrupt Enable Logic; (6) Change-of-State Detection Logic; (7) Input Data Registers; and (8) Input Buffers. Each section of the design is illustrated in further detail in Figures 3.1-2 through 3.1-10.

3.2 INTERRUPT FUNCTIONS

Interrupts are generated on any Change-of-State (positive or negative transition). The polarity is determined by reading the input port after a Change-of-State interrupt occurs.

NOTE

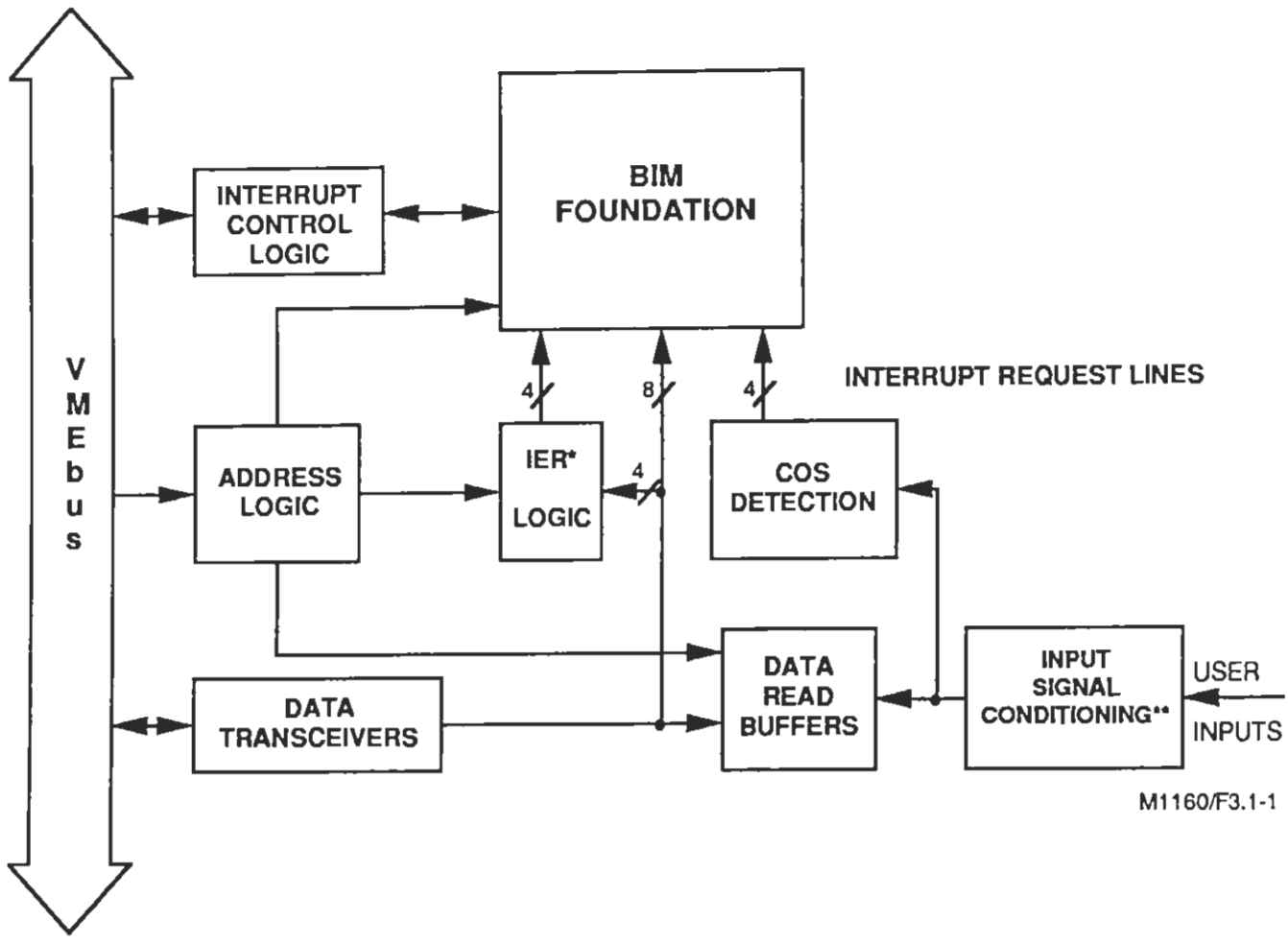
STATE CHANGES THAT OCCUR DURING THE INTERRUPT PROCESSING WINDOW (INTERNAL REQUEST TO INTERRUPT ACKNOWLEDGE CYCLE COMPLETE) WILL NOT BE DETECTED. THE TIME BETWEEN USER INPUT STATE CHANGES MUST NOT BE LESS THAN THE COMPUTER INTERRUPT PROCESSING TIME; OTHERWISE, THE STATE CHANGES WILL BE LOST.

The reader should refer to "The VMEbus Specification" for a detailed explanation of the priority interrupt bus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The data transfer bus, the arbitration bus, and the interrupt bus are all used in the process of generating and handling bus interrupts.

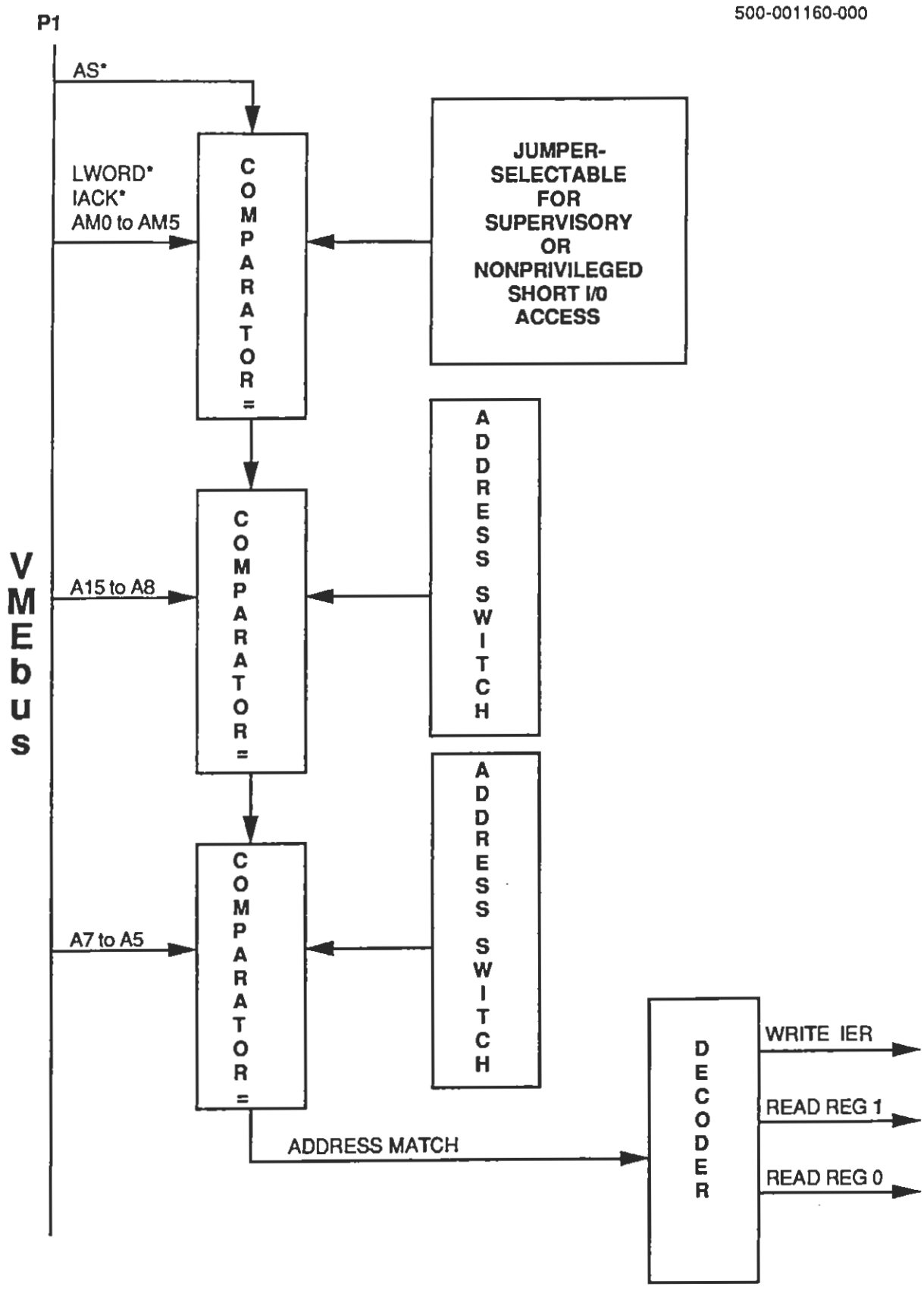
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



*Internal Enable Register
**Board Dependent

Figure 3.1-1. VMIVME-1160 Functional Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



M1160/F3.1-2

Figure 3.1-2. Address Section Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

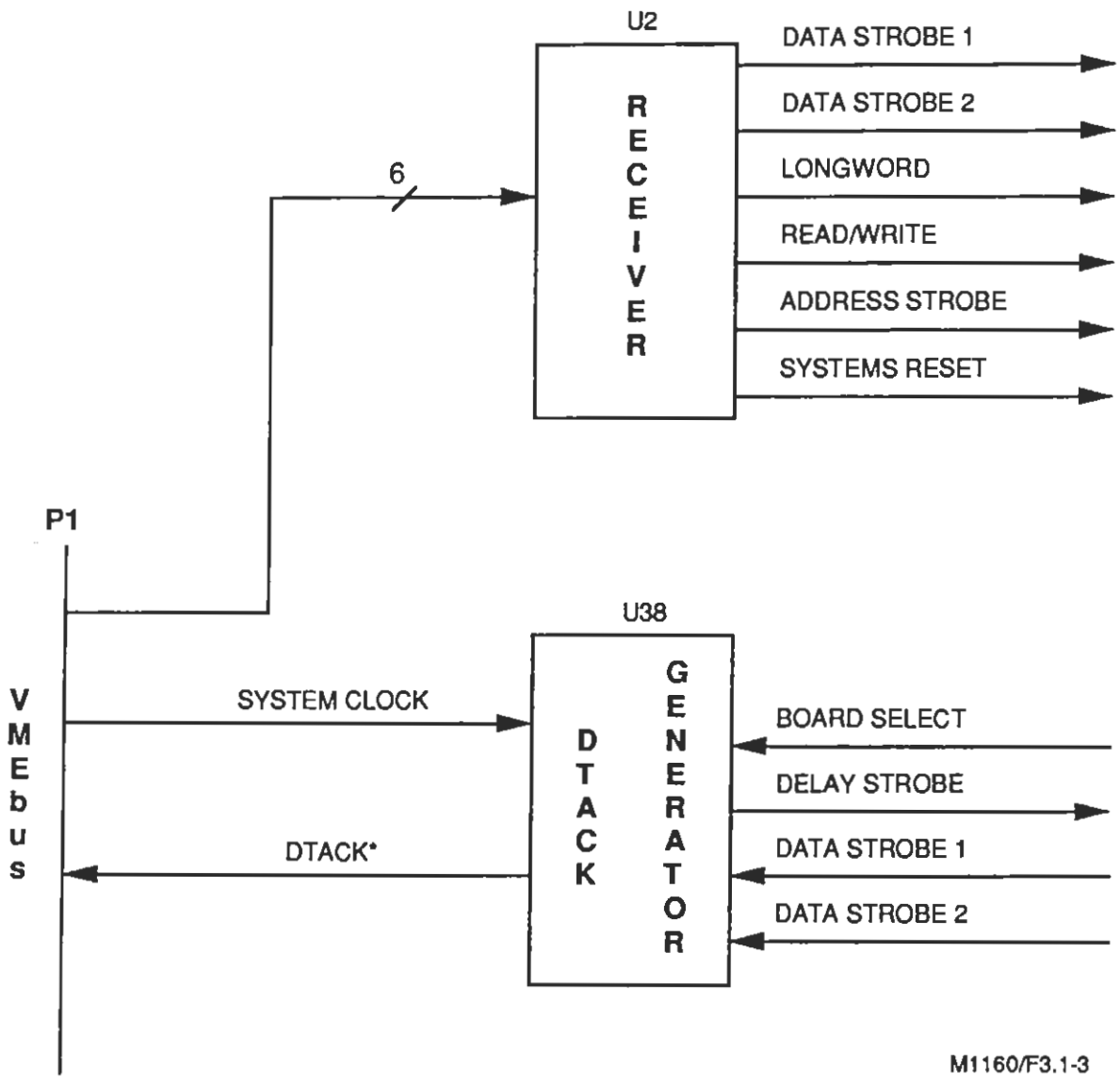


Figure 3.1-3. Control Section Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

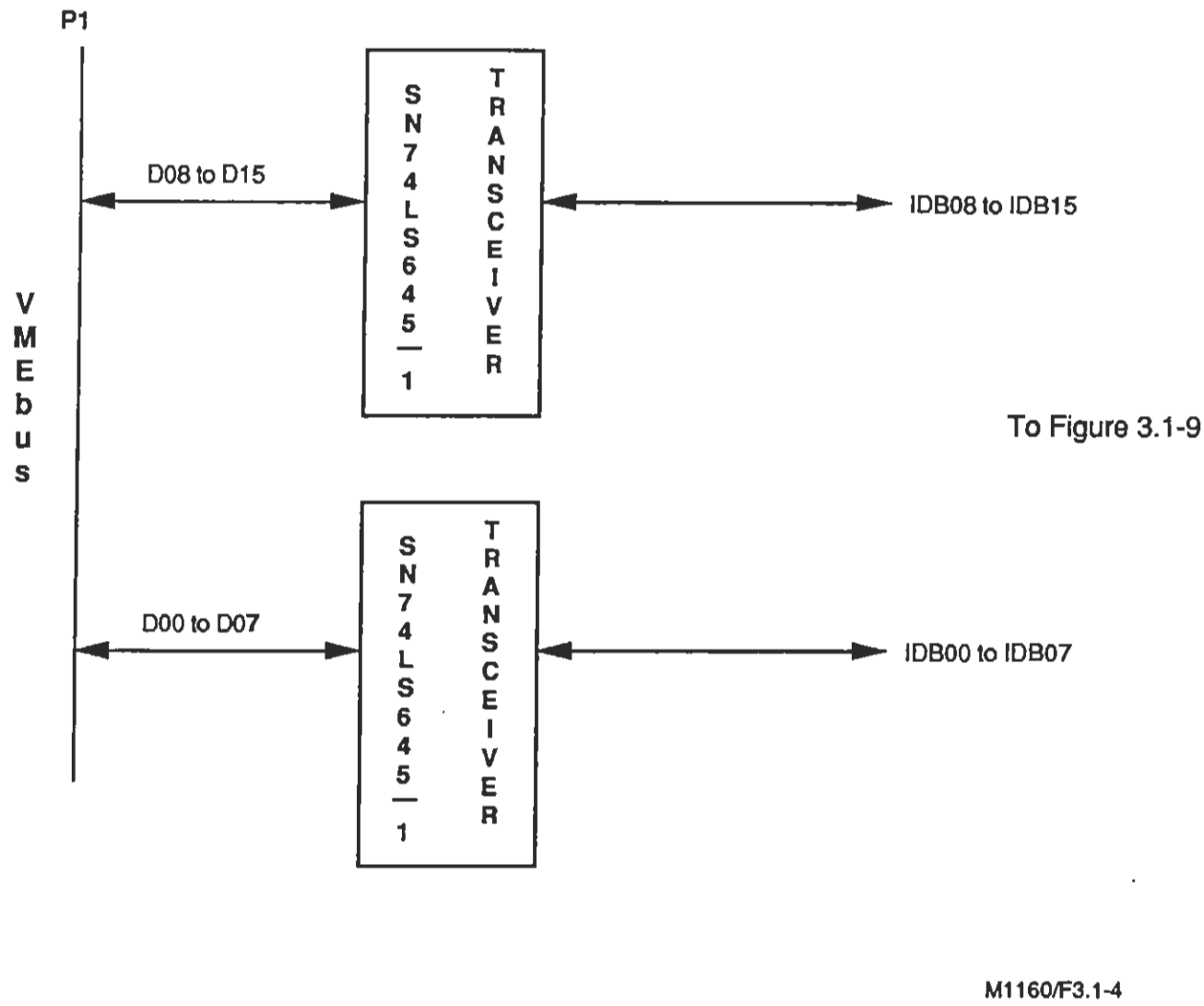
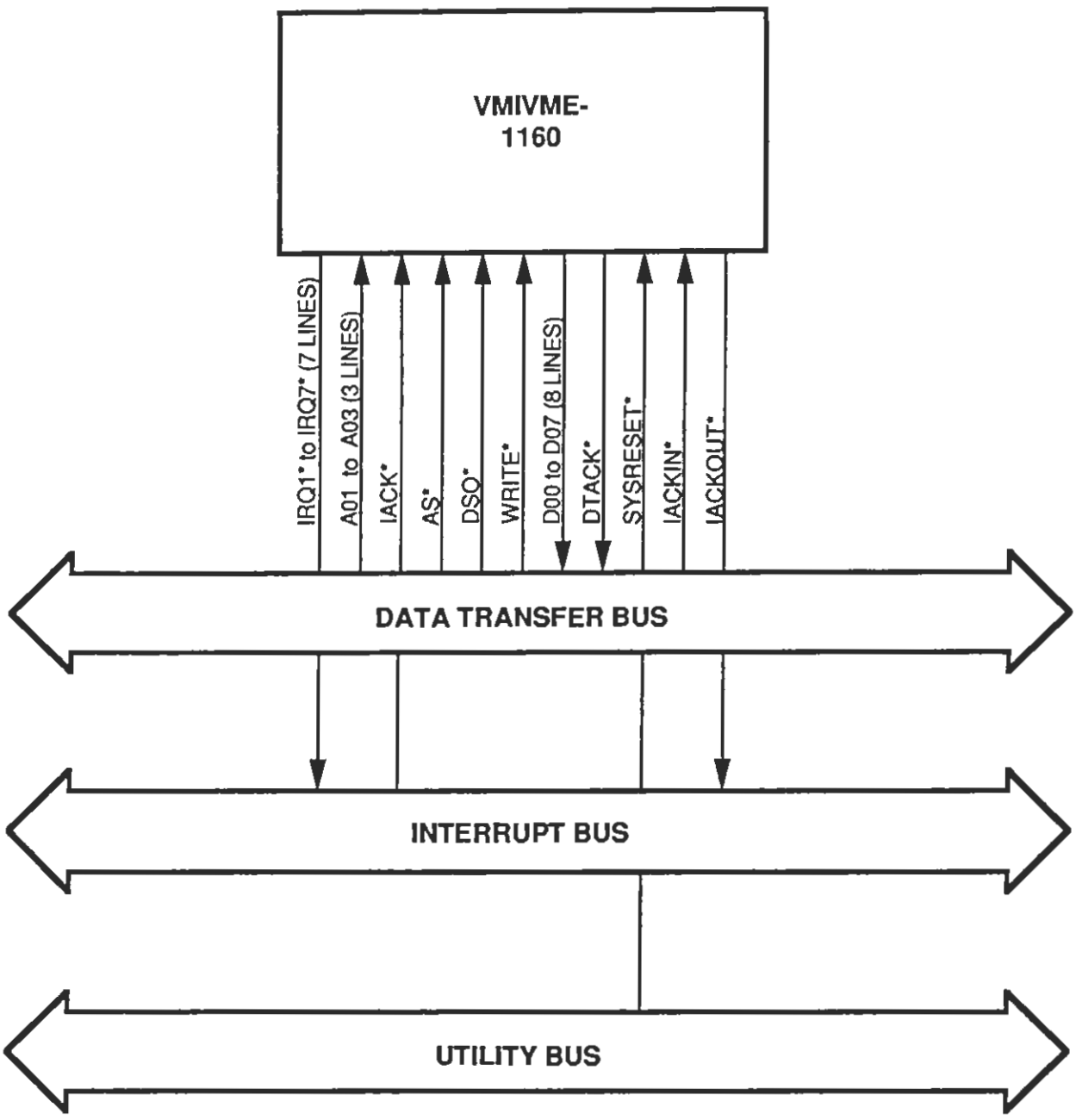


Figure 3.1-4. Data Section Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



M1160/F3.1-5

Figure 3.1-5. VMEbus Signal Lines Used by the VMIVME-1160

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

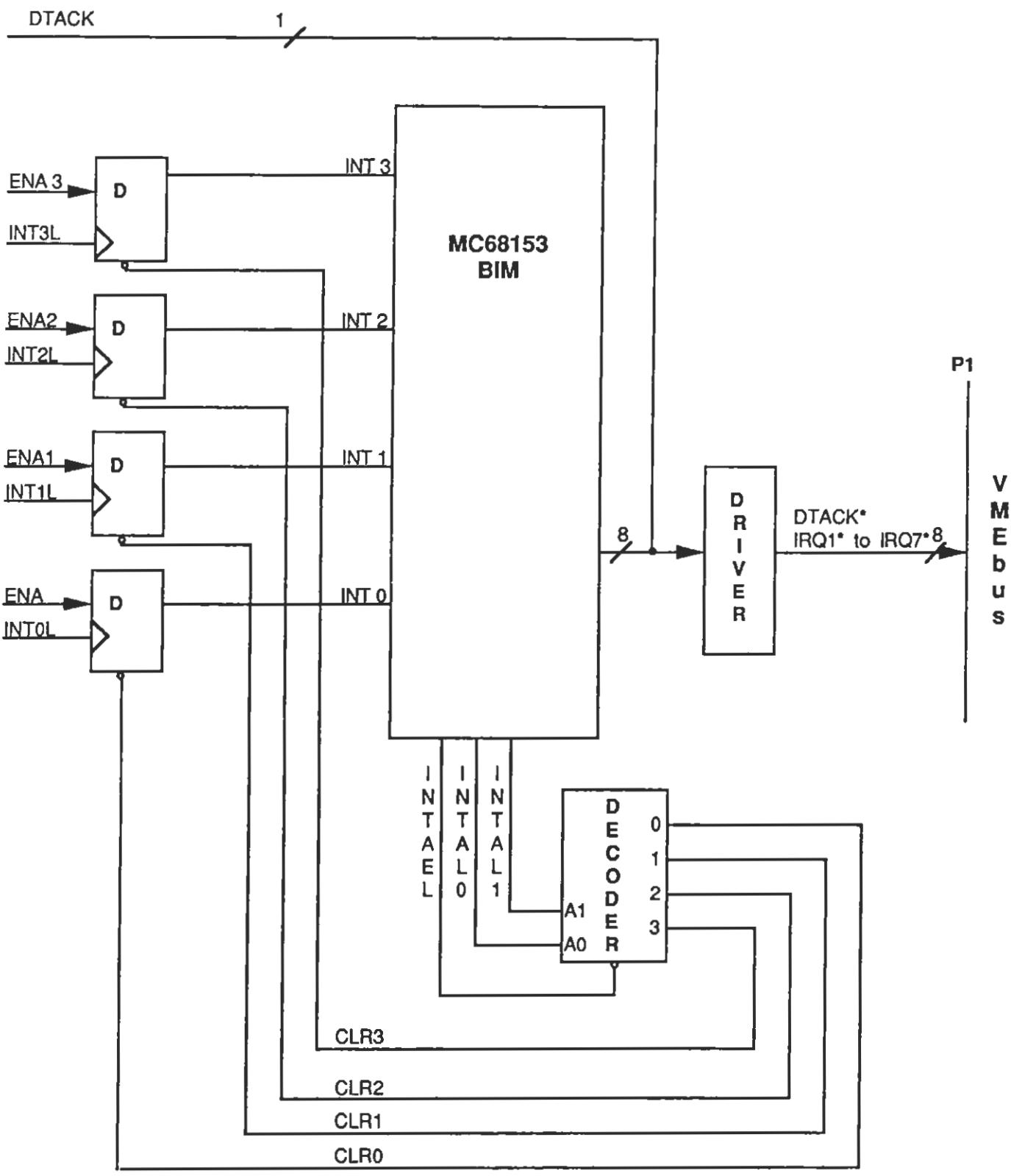


Figure 3.1-6. BIM Foundation Section Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

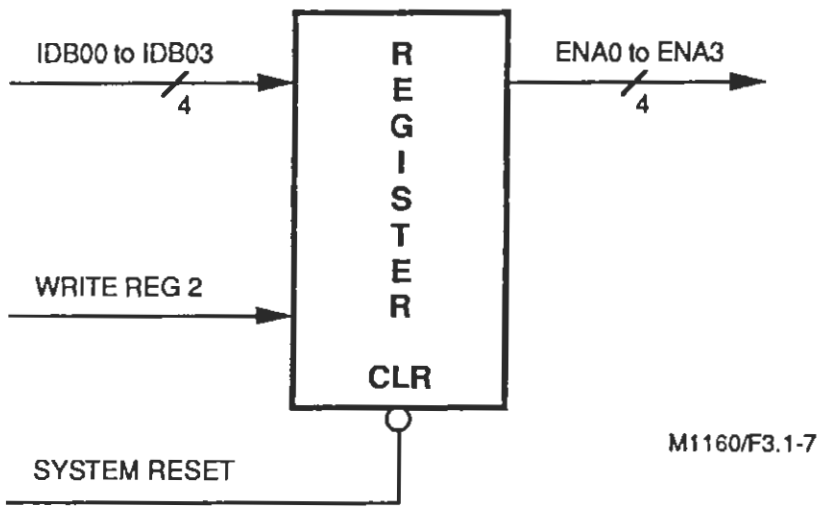


Figure 3.1-7. Typical IER Logic Section

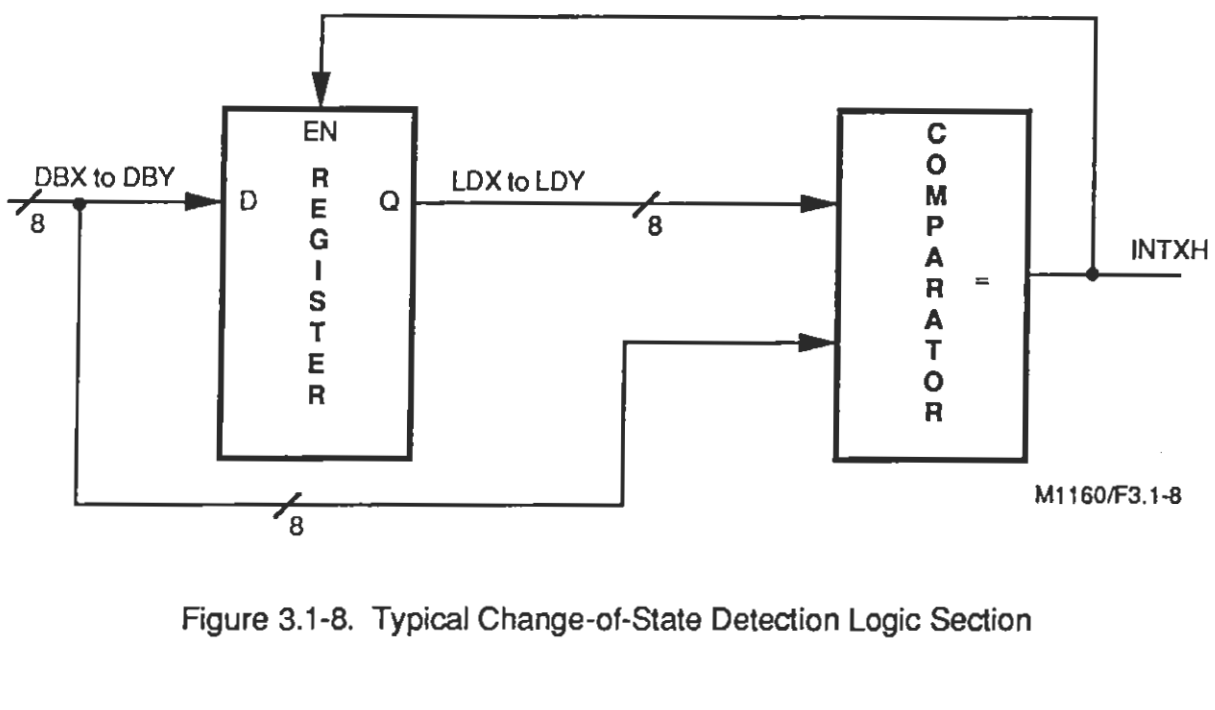


Figure 3.1-8. Typical Change-of-State Detection Logic Section

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

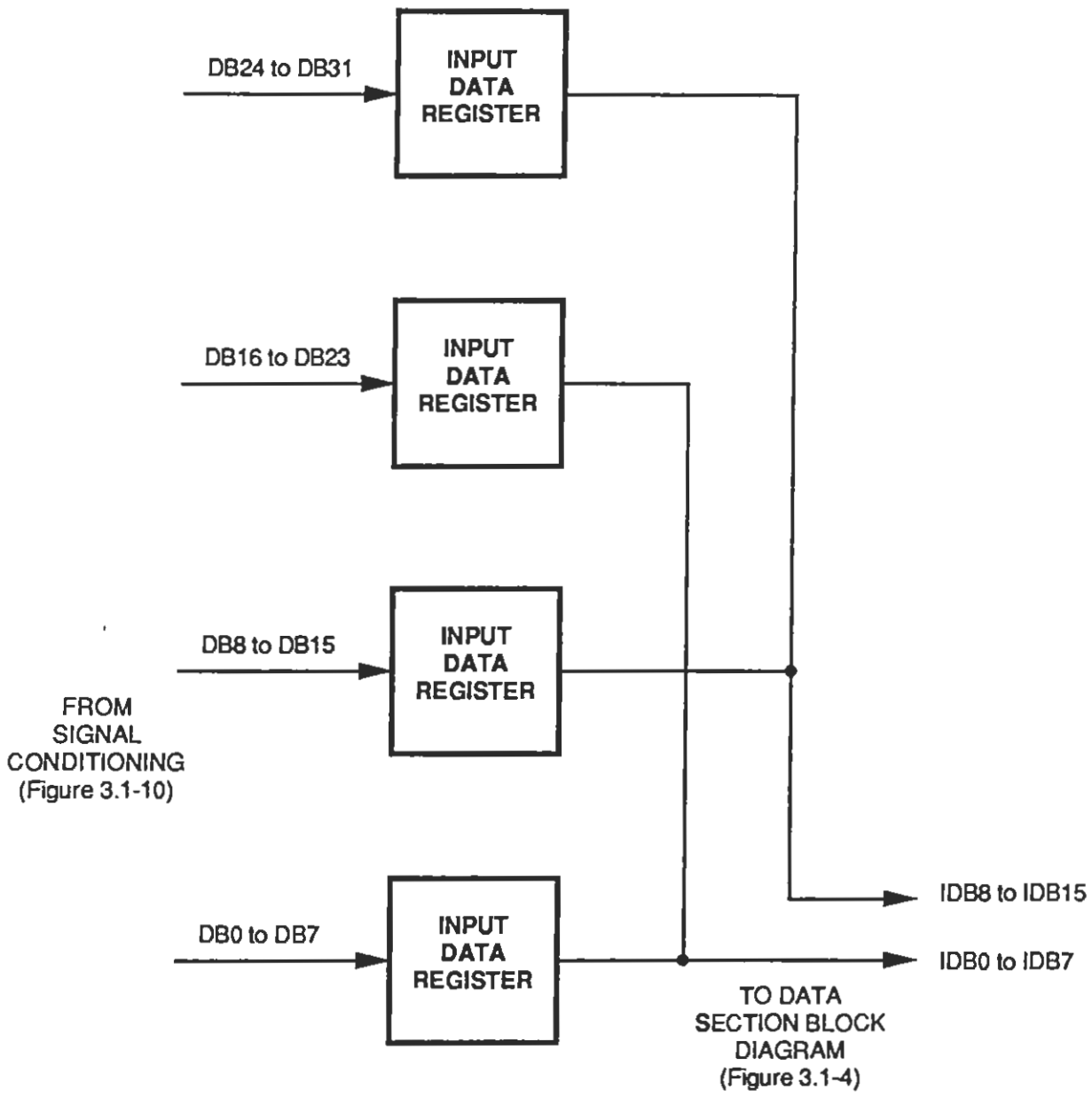


Figure 3.1-9. Input Data Registers Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

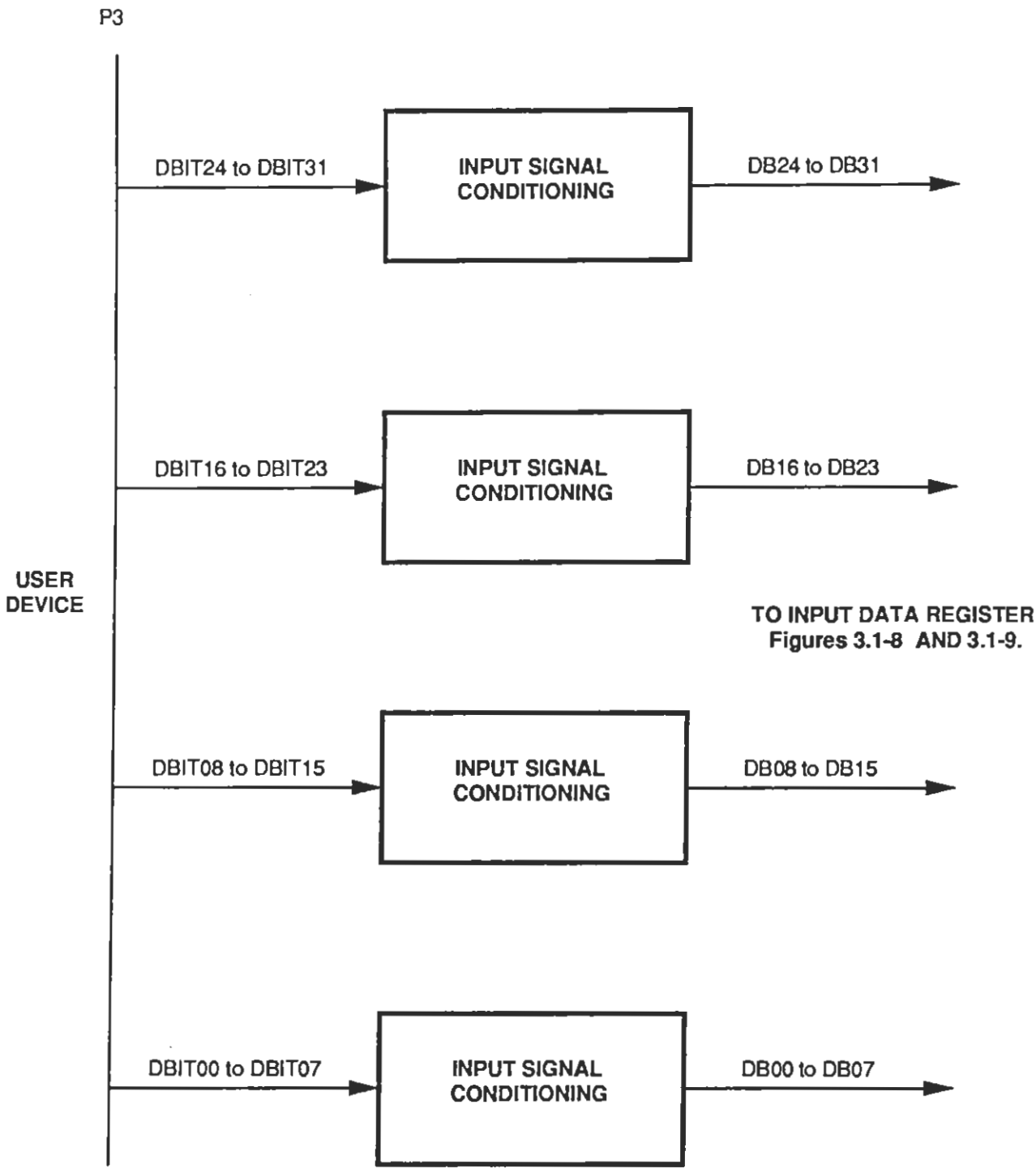


Figure 3.1-10. Signal Conditioning Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.3 PRIORITY INTERRUPT SUBSYSTEM

The following overview of the priority interrupt subsystem assumes that the reader understands the operation of both the data transfer bus and the arbitration bus.

The interrupt bus consists of seven interrupt request signal lines, one daisy-chain signal line, and one interrupt acknowledge line:

IRQ1*	IRQ4*	IRQ7*
IRQ2*	IRQ5*	IACK*
IRQ3*	IRQ6*	IACKIN*/IACKOUT*

Each interrupt request line may be driven low by the VMIVME-1160 Board or other interrupter to request an interrupt. In a single handler system, these interrupt request lines are prioritized, with IRQ7* having the highest priority.

The IACK* line runs the full length of the bus and is connected to the IACKIN* pin of slot A1. When it is driven low, it initiates a low-going transition down the interrupt acknowledge daisy-chain. This may not occur immediately, since additional constraints are placed on the propagation of IACKIN*/IACKOUT*.

Each of the seven interrupt request lines may be shared by two or more interrupter boards. Because of this, some method must be provided to ensure that only one of the boards is acknowledged. This is done by means of the interrupt acknowledge daisy-chain. The daisy-chain line passes through each board on the VMEbus. When an interrupt is acknowledged, IACKIN* is driven low at slot A1. Each board that is driving an interrupt request line low must wait for the low level down the daisy-chain, thereby guaranteeing that only one board will be acknowledged.

The VMIVME-1160 uses one of the seven IRQX* lines to request an interrupt. It then monitors the DTB address bus, IACK*, and the IACKIN*/IACKOUT* daisy-chain to determine when its interrupt is being acknowledged. When acknowledged, it places its status/ID byte on the lower eight lines of the data bus and signals the byte's validity to the interrupt handler via the DTACK* line.

The VMEbus signal lines used by the VMIVME-1160 are shown in Figure 3.1-4.

The reader should refer to Appendix B, which contains Motorola's application note on the MC68153, for a detailed explanation of the Bus Interrupter Module (BIM).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 4

PROGRAMMING

4.1 OPERATIONAL OVERVIEW

The VMIVME-1160 is designed to provide 32 channels of high voltage, optically coupled inputs with change-of-state detection. Each eight bits (byte) of input may have a unique interrupt vector that is generated upon a change-of-state of any bit in that byte. The VMIVME-1160 also has an Interrupt Enable Register which is used to allow interrupts on change-of-state to be enabled on a byte basis. The channels of input data may be accessed as two 16-bit words or four 8-bit bytes.

A register map is shown in Table 4.1-1. Detailed register bit definitions are shown in Tables 4.1-2, 4.1-3, and 4.1-4. A typical flow diagram is shown in Figure 4.1-1.

Table 4.1-1. Register Map

RELATIVE ADDRESS	MNEMONIC	NAME/FUNCTION	
$XX00	DR0	Data Register 0	
$XX01	DR1	Data Register 1	
$XX02	DR2	Data Register 2	
$XX03	DR3	Data Register 3	
$XX05	IER	Interrupt Enable Register	
$XX11	CR0	Control Register 0	MC68153 BIM REGISTERS
$XX13	CR1	Control Register 1	
$XX15	CR2	Control Register 2	
$XX17	CR3	Control Register 3	
$XX19	VR0	Vector Register 0	
$XX1B	VR1	Vector Register 1	
$XX1D	VR2	Vector Register 2	
$XX1F	VR3	Vector Register 3	

M1160/T4.1-1

The reader may want to refer to Appendix B for detailed programming characteristics of the MC68153 BIM.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.1-2. Typical Input Data Register Bit Maps

$XX00 DR0

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
INPUT DATA							
ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24

$XX01 DR1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16

$XX02 DR2

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
INPUT DATA							
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

$XX03 DR3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

$XX05 IER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				INTERRUPT ENABLE*			
RESERVED				DR0	DR1	DR2	DR3

* A "one" in the BIT location will enable the interrupts for the stated Data Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.1-3. Typical BIM Control Register Map

$XX11 CONTROL REGISTER 0 (Control for DR3 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX13 CONTROL REGISTER 1 (Control for DR2 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX15 CONTROL REGISTER 2 (Control for DR1 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX17 CONTROL REGISTER 3 (Control for DR0 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

M1160/T4.1-3

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.1-4. Typical BIM Vector Register Map

$XX19 VR0 (Vector for DR3 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

$XX1B VR1 (Vector for DR2 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

$XX1D VR2 (Vector for DR1 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

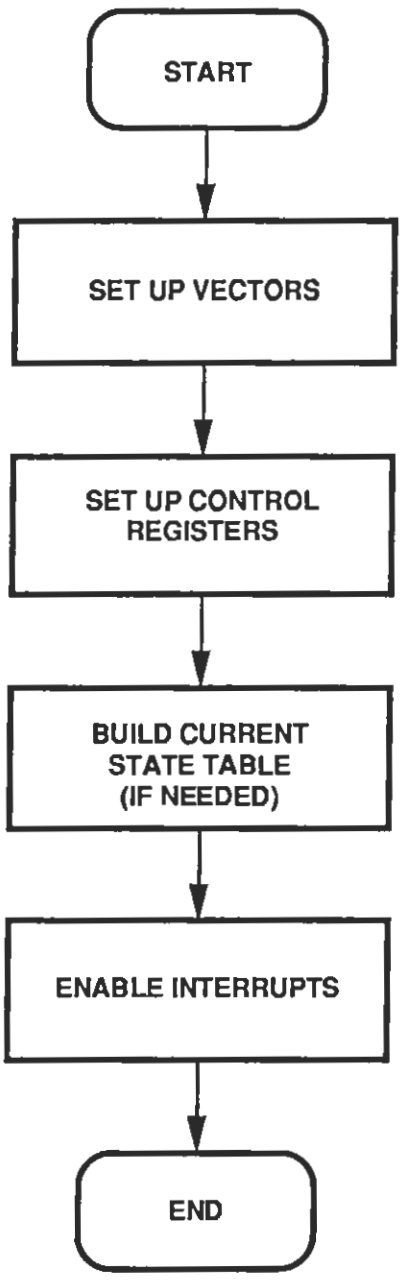
$XX1F VR3 (Vector for DR0 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

*COS = Change-of-State

M1160/T4.1-4

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



M1160/F4.1-1

Figure 4.1-1. VMIVME-1160 Programming Flow Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

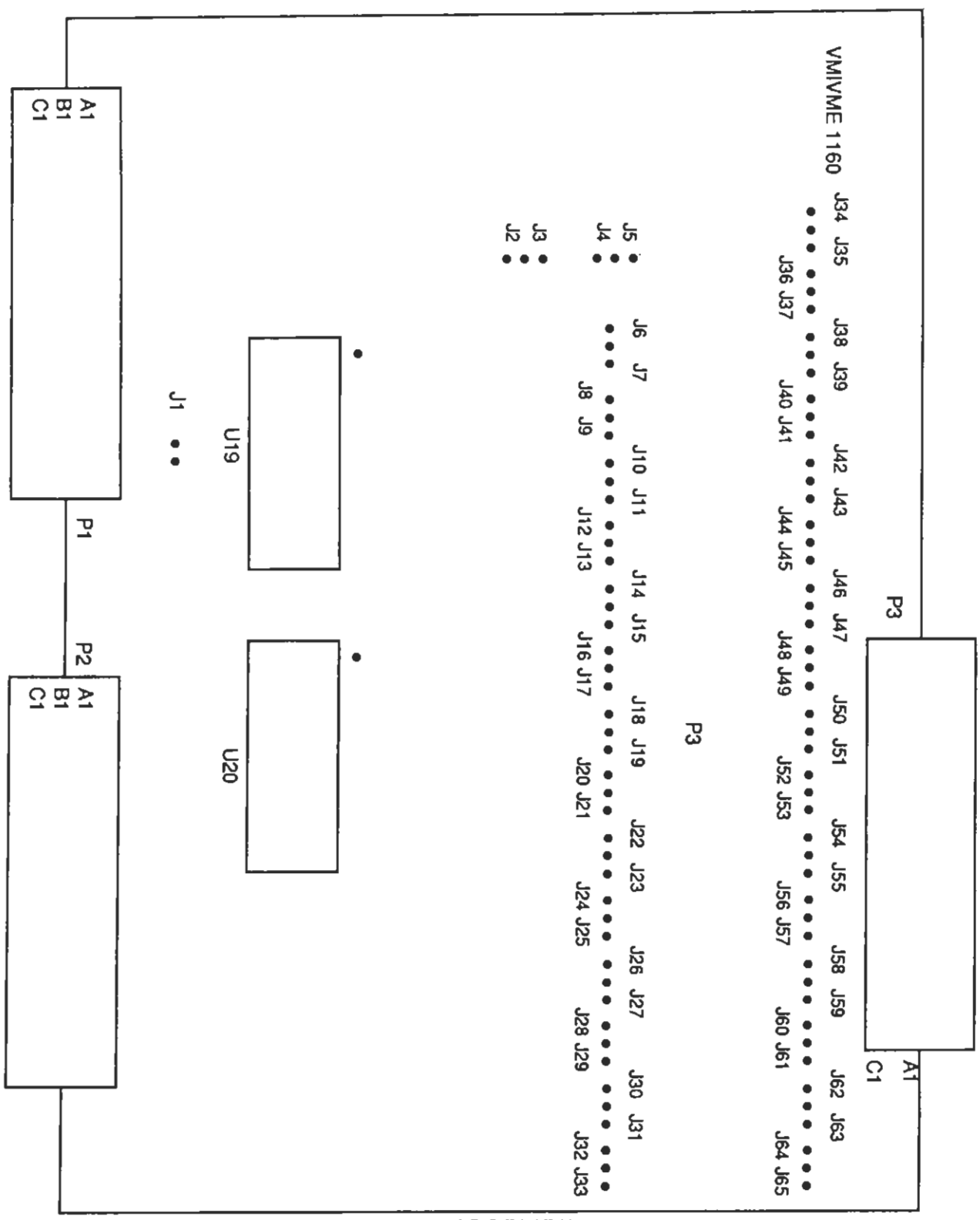
DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 CONFIGURATION SWITCHES

The reader should refer to Figure 5.3-1 for the locations of jumpers and address switches.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



COMPONENT SIDE VIEW

M1160/F5.3-1

Figure 5.3-1. Locations of Jumpers and Address Switches

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

REMOVED

5.4 CURRENT SINK, VOLTAGE SOURCE SELECTION

The VMIVME-1160 may be ordered with its input signal conditioning electronics factory configured for voltage source or current sink input options as shown in Table 2.1-6, in Section 2. A wide range of input V (5 to 48 V) are supported, and the user may select from a variety of input filters.

In Figure 5.8-1 Jx is the contact sense jumper. This jumper is installed at the factory when a contact sense board is ordered. Jx corresponds to the even numbered jumpers (J2, J4, etc.) on the schematic in the appendix of this manual. Jy is the voltage source jumper. It is installed for voltage source boards and corresponds to the odd numbered jumpers (J3, J5, etc.) except for jumper J1, which is the address modifier jumper.

5.5 EXTERNAL PULL-UP VOLTAGE

External voltage is connected through the P2 connector on pins C30, and C31 (VPOS uses P2 pin C30, VNEG uses P2 pin C31). This voltage is required on contact sense configurations only.

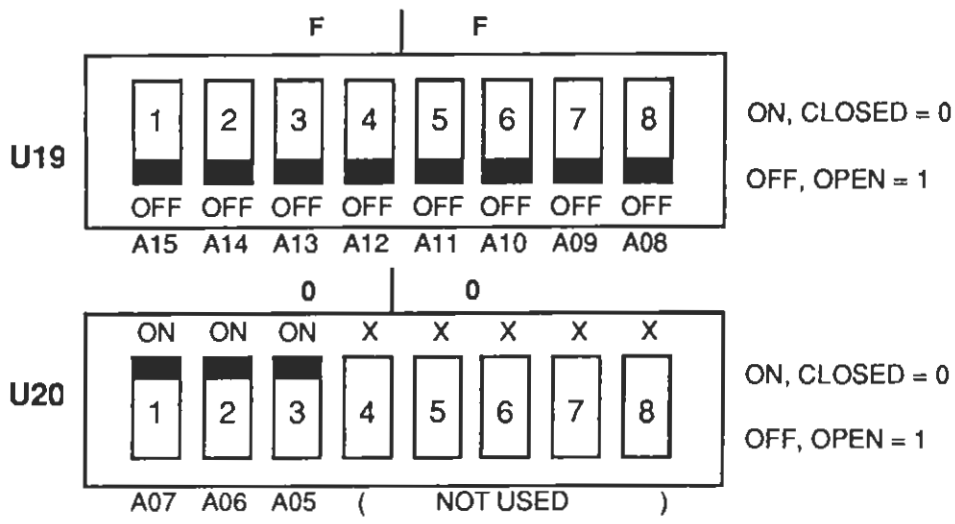
5.6 ADDRESS MODIFIERS

The VMIVME-1160 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing the jumper J1 to enable the board to respond to short nonprivileged I/O access.

5.7 ADDRESS SELECTION SWITCHES

Figure 5.7-1 shows the two addressing DIP switches on board the VMIVME-1160 and their use in the addressing scheme.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



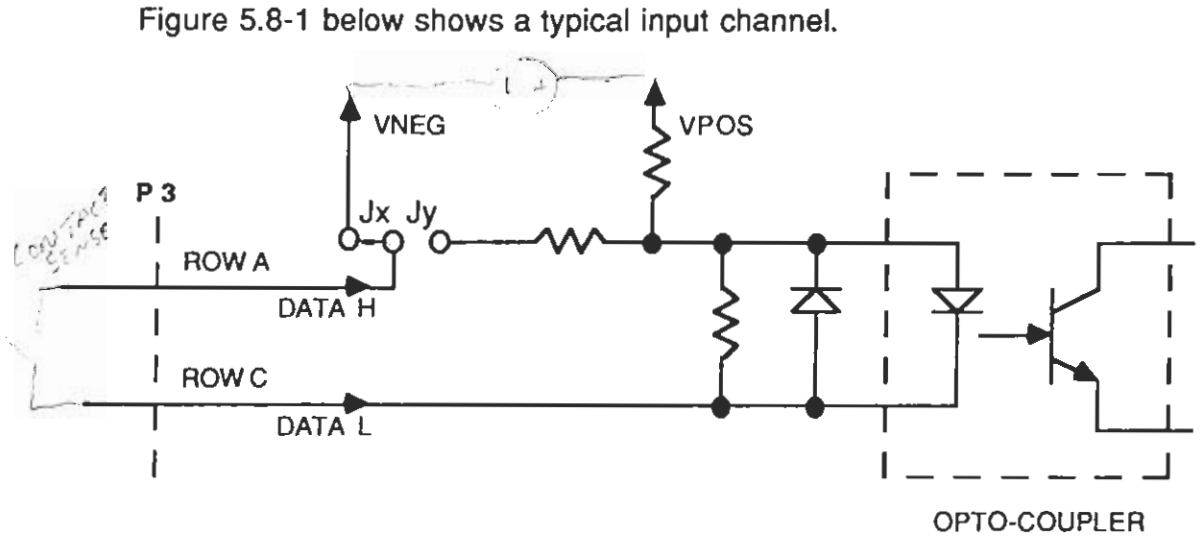
A base address FF00 HEX is shown in this example.

M1160/F5.7-1

Figure 5.7-1. Data Register Address Select Switches

5.8 CONNECTOR PIN CONFIGURATION

Figure 5.8-1 below shows a typical input channel.



M1160/F5.8-1

Figure 5.8-1. Typical Input Channel

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The input connector, P3, is a 64-pin connector designed with pins in two rows, Row A and Row C. Connection is accomplished by connecting the appropriate row pin to the appropriate user signal. For example, in the voltage source case the user will probably connect the equipment ground to the Row C pins, and bring each signal input in through Row A pins.

5.9 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION

The I/O connector (P3) on the VMIVME-1160 is a 64-pin DIN standard and was selected by VMIC because of its unique keying features and high quality. The keying features of this connector provide the user with the capability of uniquely keying I/O cables on each board and connector in a system. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC's Document 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning I/O connections are shown in Figure 5.9-1. Conductor No. 1 is shown at the bottom of the connector as it plugs into the header, because pin No. 1 of P3 is mounted as shown.

A compatible flat-ribbon cable connector for the VMIVME-1160 is Panduit No. 120-964-455E, and strain relief, Panduit No. 100-000-032. The Header Connector soldered to the PC board is Panduit No. 120-964-053A. Figure 5.9-2 shows the pin out of connector P3. Table 5.9-2 shows the P3 connector pin assignments for the inputs to the board. Figure 5.9-3 shows the pin out of connector P2. Table 5.9-1 shows the pertinent pin assignments for connector P2.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

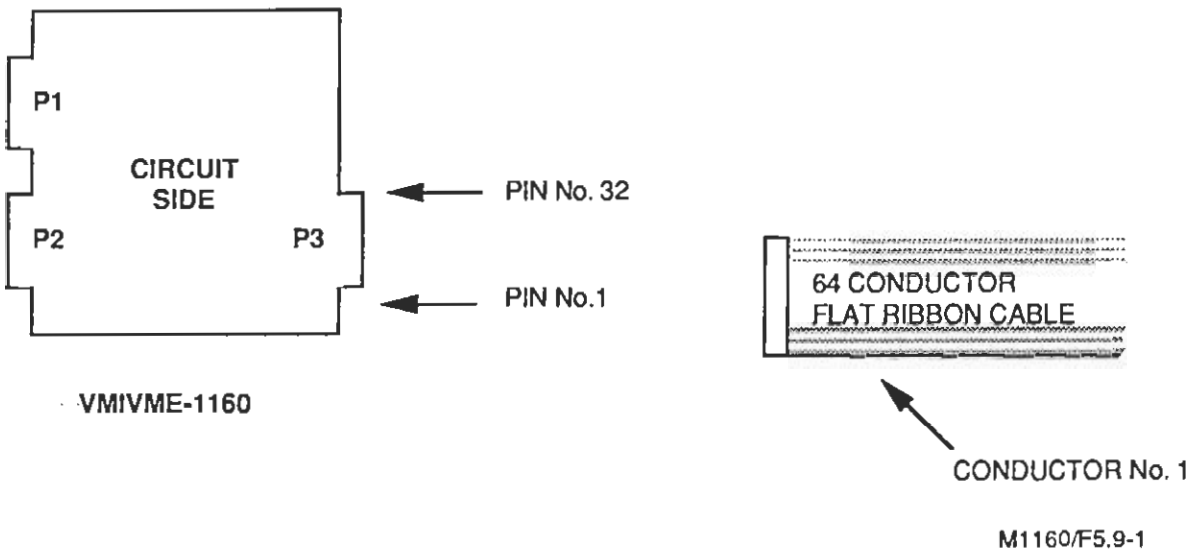


Figure 5.9-1. Cable Connector Configuration

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

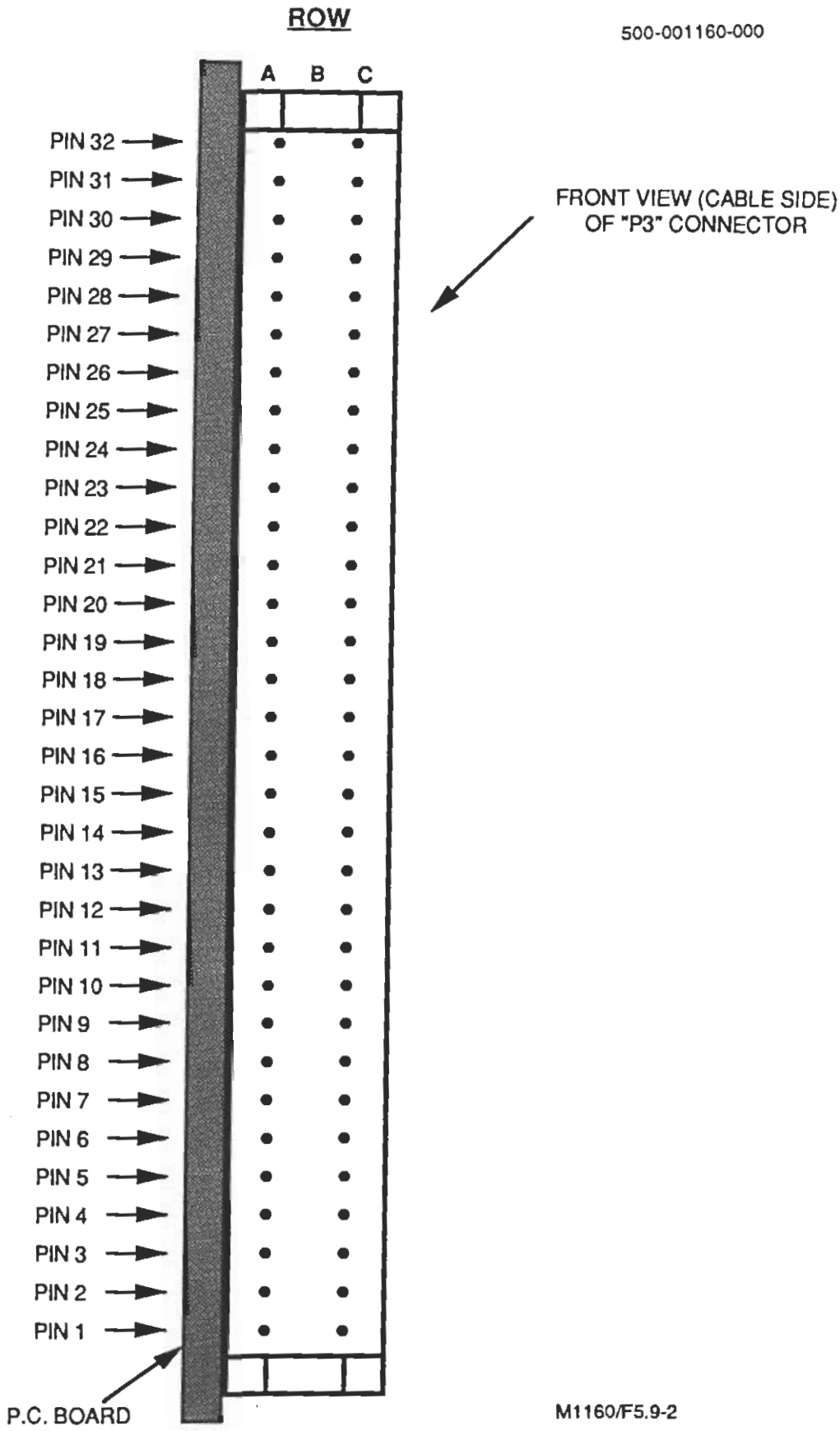


Figure 5.9-2. P3 Connector Pin Layout

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

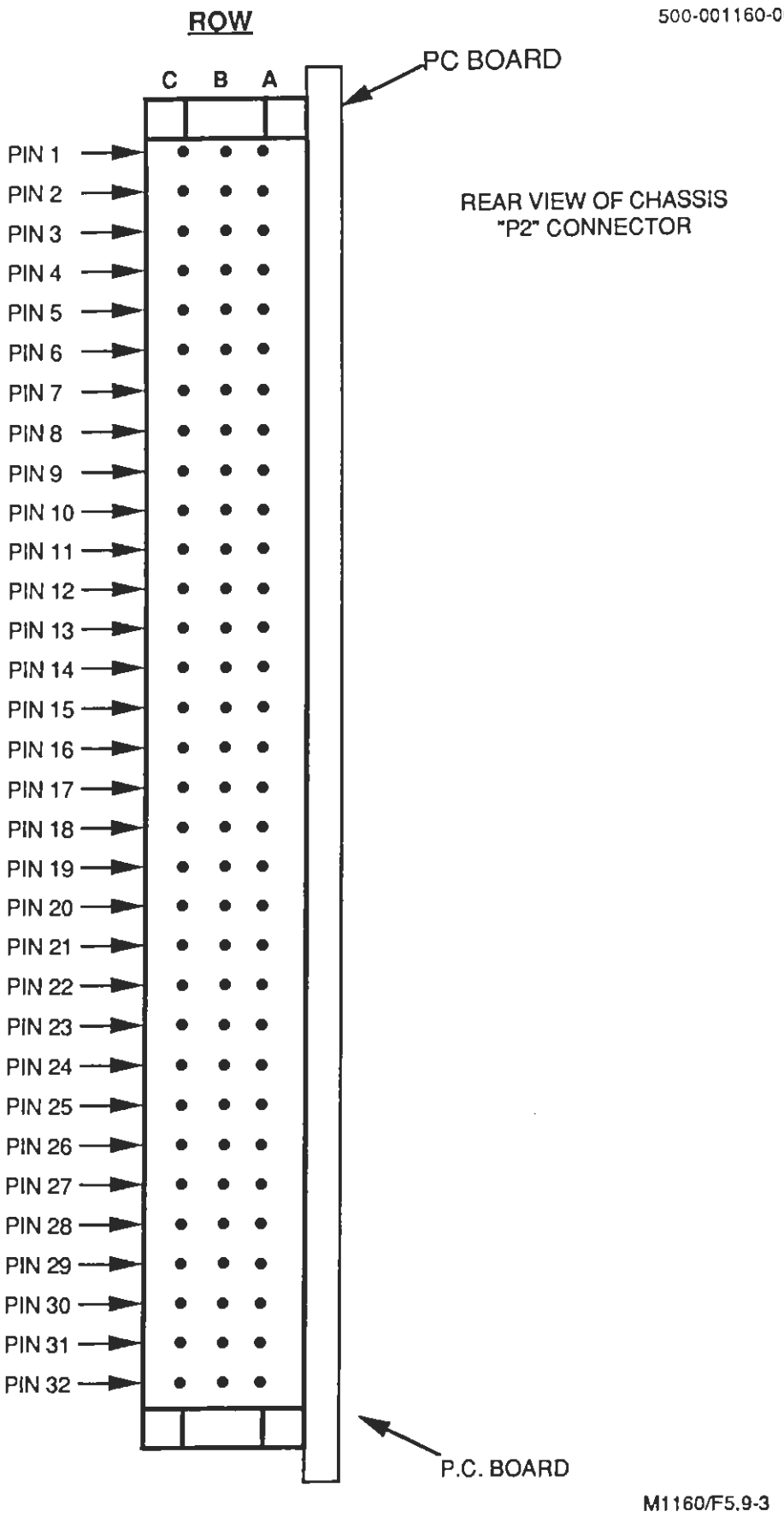


Figure 5.9-3. P2 Connector Pin Layout

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 5.9-1. P2 Connector Pin Assignment

PIN NO.	ROW A[1]	ROW B[2]	ROW C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30			V POS
31		GND	V NEG
32		+5 V	

M1160/T5.9-1

NOTES: 1. External reference is supplied by the user.
2. Inputs to the board - not required.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 5.9-2. P3 Pin-Channel Assignment

P3	
ROW A PIN	CHANNEL NO.
32	31
31	30
30	29
29	28
28	27
27	26
26	25
25	24
24	23
23	22
22	21
21	20
20	19
19	18
18	17
17	16

P3	
ROW A PIN	CHANNEL NO.
16	15
15	14
14	13
13	12
12	11
11	10
10	09
09	08
08	07
07	06
06	05
05	04
04	03
03	02
02	01
01	00

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX B

MC68153 BIM DATA SHEET

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC68153

Advance Information

BUS INTERRUPTER MODULE

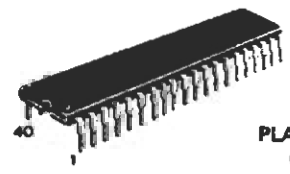
The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to 4 independent sources of interrupt requests and is fully programmable.

- VERSAbus/VMEbus Compatible
- MC68000 Compatible
- Handles 4 Independent Interrupt Sources
- 8 Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

TTL

BUS INTERRUPTER MODULE

ADVANCED LOW POWER SCHOTTKY

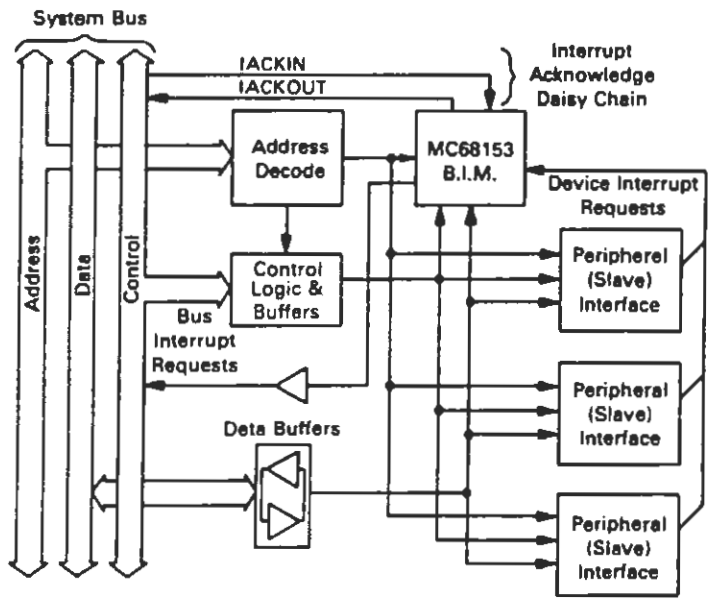


P SUFFIX
PLASTIC PACKAGE
CASE 711-03



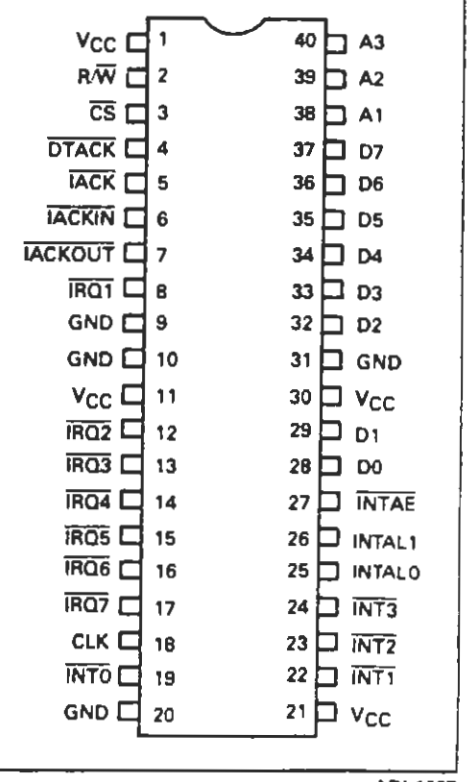
L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM



VERSAbus is a trademark of Motorola.

PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

© MOTOROLA INC. 1984

ADI-1057

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired.)

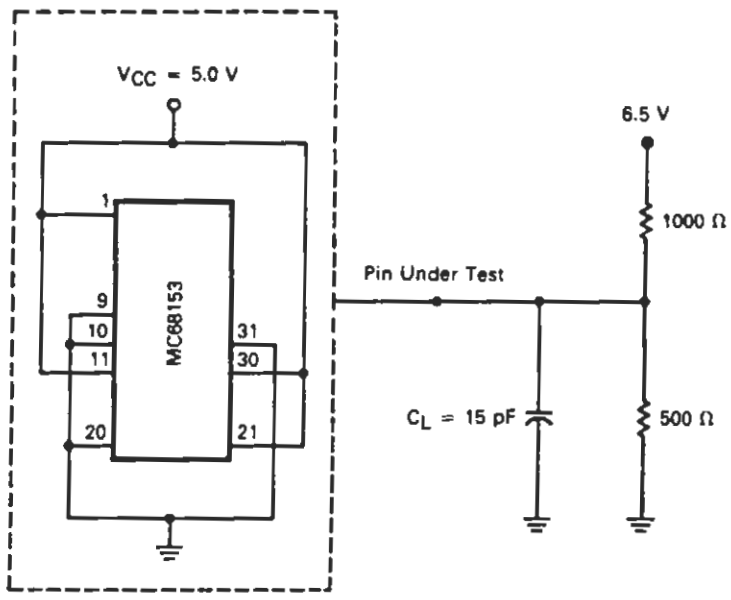
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Input Current	I_{in}	−30 to +5.0	mA
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{OL}	Twice Rated I_{OL}	mA
Storage Temperature	T_{stg}	−65 to +140	°C
Junction Operating Temperature	T_J	−55 to +140	°C

BURN-IN LIMITS: A maximum T_J of +175°C may be used for periods not to exceed 250 hours.

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	—	V	
Low Level Input Voltage	V_{IL}	—	0.8	V	
Input Clamp Voltage	V_{IK}	—	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
High Level Output Voltage(1)	V_{OH}	2.7	—	V	V_{CC} = MIN, I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}	—	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Output Short Circuit Current(2)	I_{OS}	−15	−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
High Level Input Current	I_{IH}	—	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
Low Level Input Current	I_{IL}	—	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
Supply Current	I_{CC}	225	385	mA	V_{CC} = MAX
Output Off Current (High)	I_{OZH}	—	20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
Output Off Current (Low)	I_{OZL}	—	−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V

AC TEST CIRCUIT — AC Testing of All Outputs



NOTES:
1. Not applicable to open-collector outputs.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. $\overline{IACK}$ Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Test Number(5)	Max (ns)
CLK High to Data Out Valid (Delay)(3)	1	55
CLK High to $\overline{\text{DTACK}}$ Low (Delay)(3)	2	40
$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay)	3	35
CLK High to Data Out Valid (Delay)(4)	4	55
CLK High to $\overline{\text{INTAE}}$ Low (Delay)(4)	5	40
$\overline{\text{IACK}}$ High to Data Out High Impedance (Delay)	6	60
$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay)	7	45
$\overline{\text{CS}}$ High to Data Out High (Delay)	8	45
$\overline{\text{CS}}$ High to IRQ High (Delay)	9	60
$\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay)	10	35

GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VERSAbus, VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{\text{INT0}}$ – $\overline{\text{INT3}}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{\text{IRQ1}}$ – $\overline{\text{IRQ7}}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to/from the system bus. These are active high, 3-state pins. D7 is the most significant bit.

ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

CHIP SELECT — $\overline{\text{CS}}$

$\overline{\text{CS}}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

READ/WRITE — R/$\overline{\text{W}}$

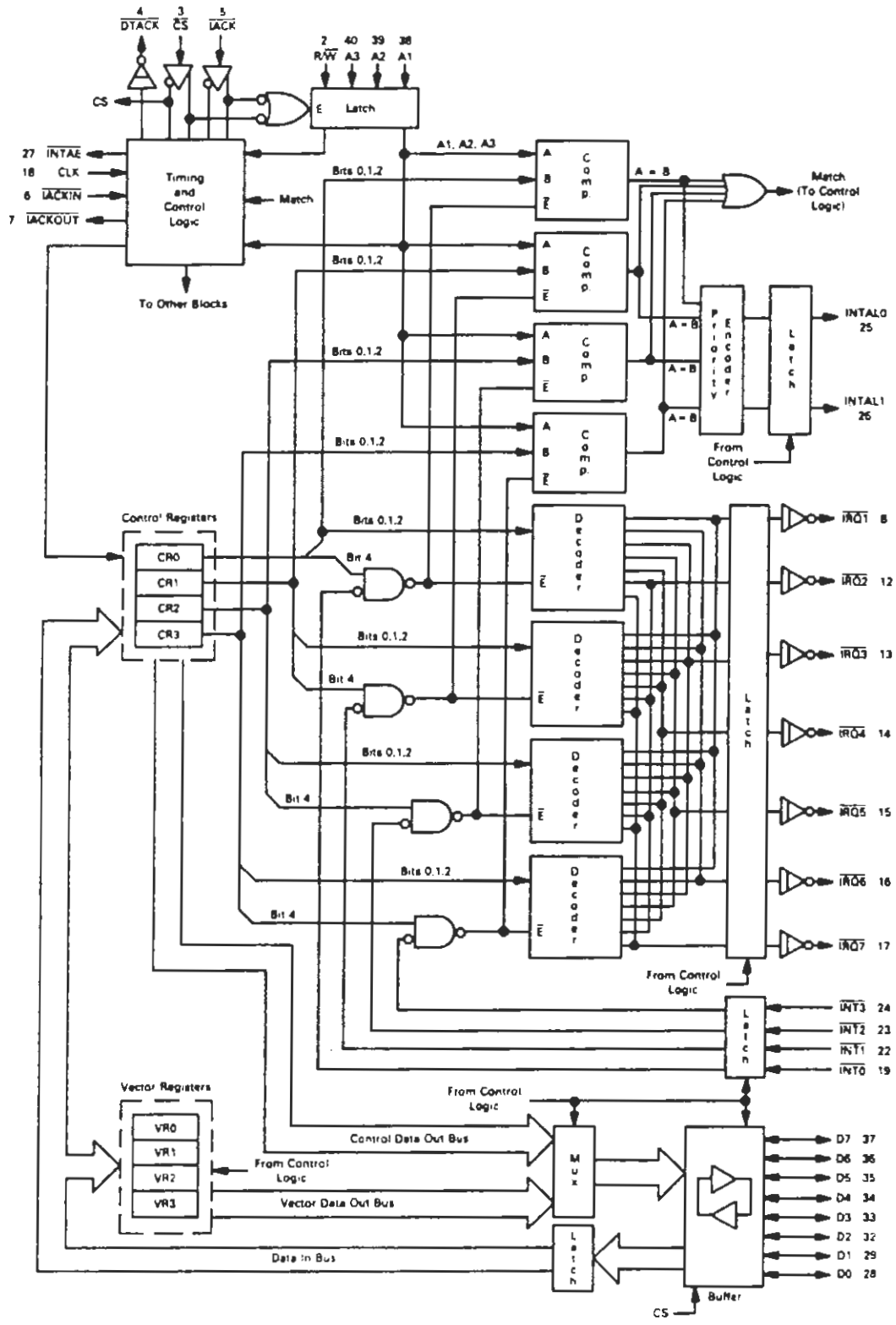
The R/$\overline{\text{W}}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

DATA TRANSFER ACKNOWLEDGE — $\overline{\text{DTACK}}$

$\overline{\text{DTACK}}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{\text{DTACK}}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{\text{DTACK}}$ high between bus cycles.

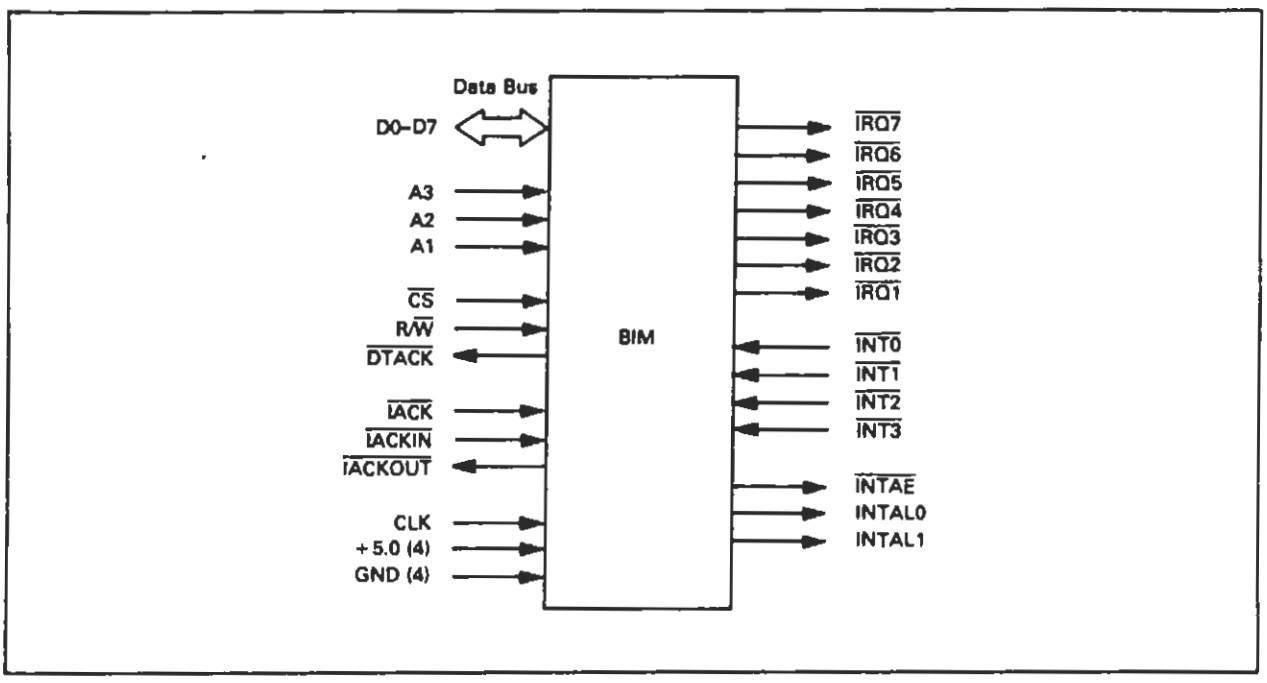
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 3 — LOGICAL PIN ASSIGNMENT



INTERRUPT ACKNOWLEDGE SIGNALS — IACK, IACKIN, IACKOUT

These three pins support the interrupt acknowledge cycle. A low level on the IACK input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After IACK is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally and determines if a match exists. Then, if input IACKIN is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output IACKOUT if *no* match exists.

IACKIN and IACKOUT form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until IACKIN is asserted and not pass the signal on (assert IACKOUT) if it is to complete the interrupt acknowledge cycle.

BUS INTERRUPT REQUEST SIGNALS — IRQ1 – IRQ7

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain IRQ1 – IRQ7 high between interrupt requests.

DEVICE INTERRUPT REQUEST SIGNALS — INT0 – INT3

INT0 – INT3 are active low inputs used to indicate to the BIM that a device wants a bus interrupt.

INTERRUPT ACKNOWLEDGE ENABLE — INTAE

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt (INTx) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a DTACK signal.

INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when INTAE is asserted low.

CLOCK — CLK

The CLK input is used to supply the clock for internal operations of the MC68153.

RESET — CS, IACK

Although a reset input is not supplied, an on-board reset is performed if CS and IACK are asserted simultaneously.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 4 — MC68153 REGISTER MODEL

ADDRESS BIT A3	A2	A1	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME
0	0	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0
0	0	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1
0	1	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2
1	1	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3
1	0	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0
1	0	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1
1	1	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2
1	1	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3
			7	6	5	4	3	2	1	0	REGISTER BIT

REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device. The other four (VR0 – VR3) are vector registers that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

A value of zero in the field disables the interrupt.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{INTX}$ line is asserted and IRE is cleared, *no* interrupt request ($\overline{IRQX}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To reenable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{IN}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{IN}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{DTACK}$ signal, i.e., an internal response. If X/$\overline{IN}$ is set, the vector is not supplied and no $\overline{DTACK}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{IN}$) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. Tha control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

The MC68153 can be used with many system buses, however, it is primarily intended for VMEbus, VERSAbus and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to esk for an interrupt of other processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (such as the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

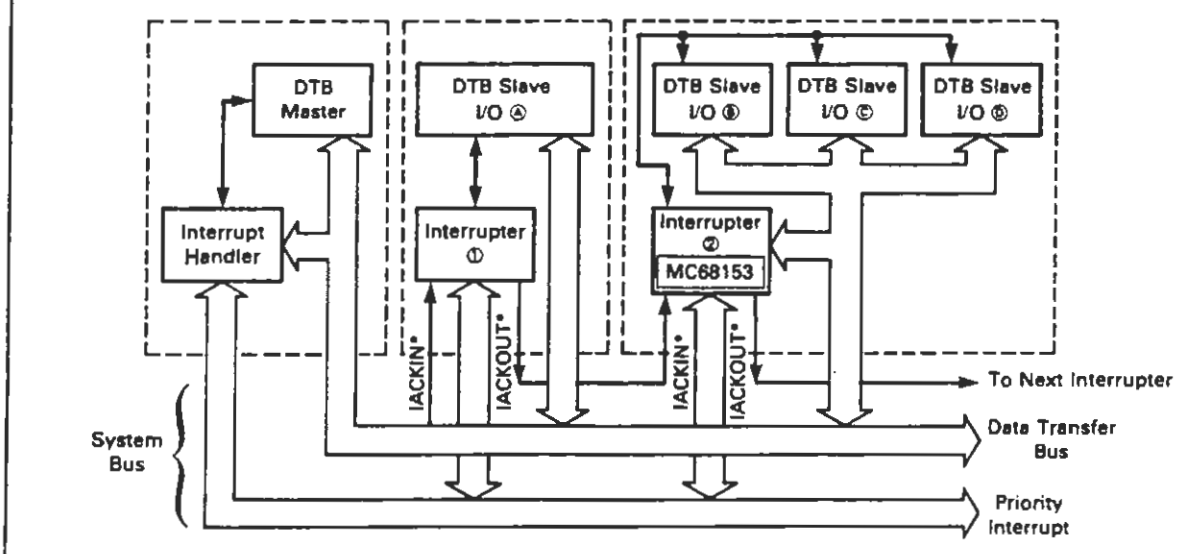
The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritizes interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DSO* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

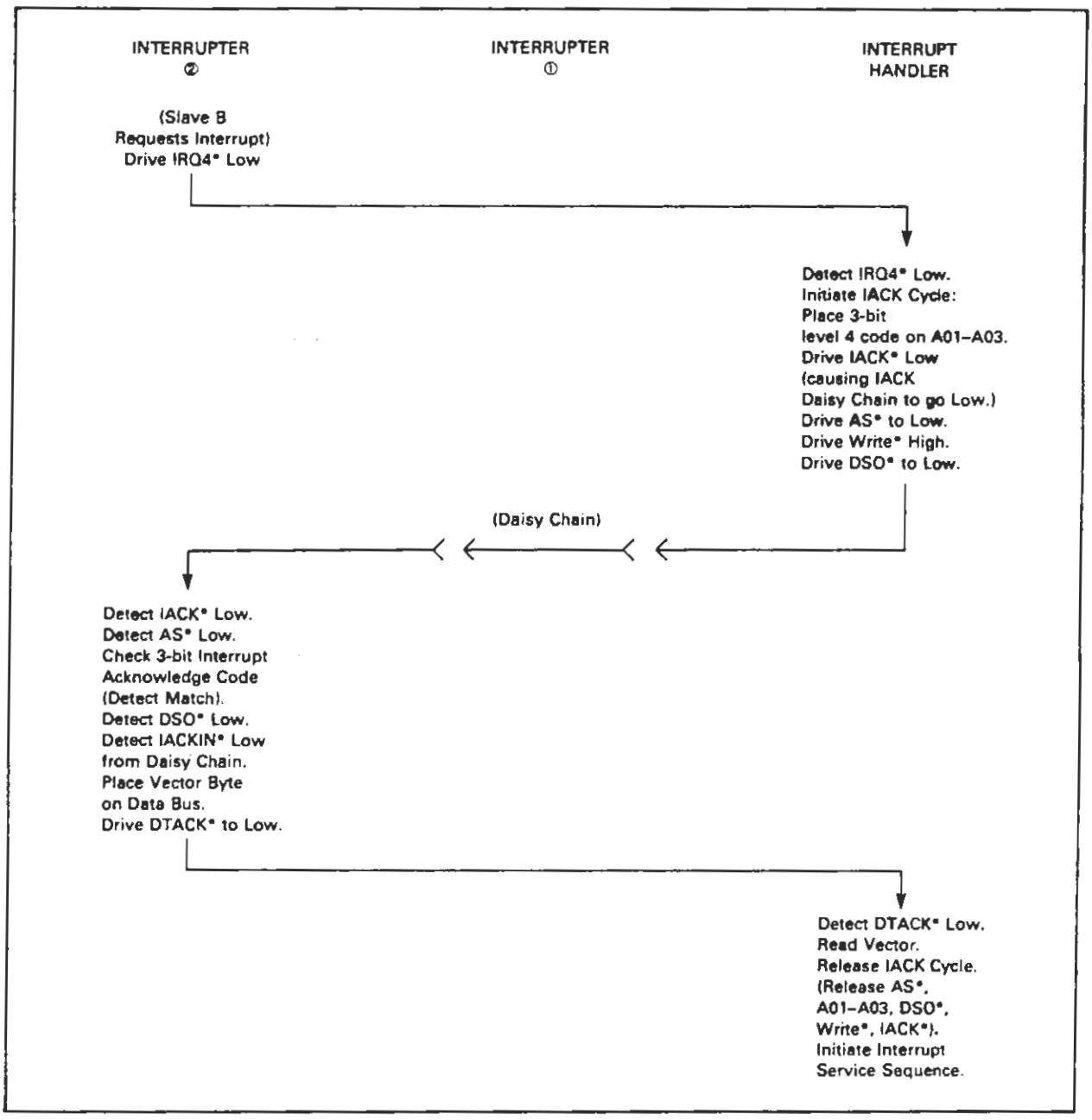


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector determines where its starting address is stored.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification MVMEBS or VERSAbus Specification M68KVBS. Also, the MC68153 can be used with other buses having similar interrupt structures.

BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the MC68153 interface to VERSAbus or VMEbus. Address Decode and Control Logic are dependent on the application and must be designed to guarantee BIM ac specifications. It is possible in most cases that the decode logic can be shared with the slave devices. Buffers are provided where shown to comply with bus loading and drive specifications. It is also possible that buffers can be shared with the slave bus interface.

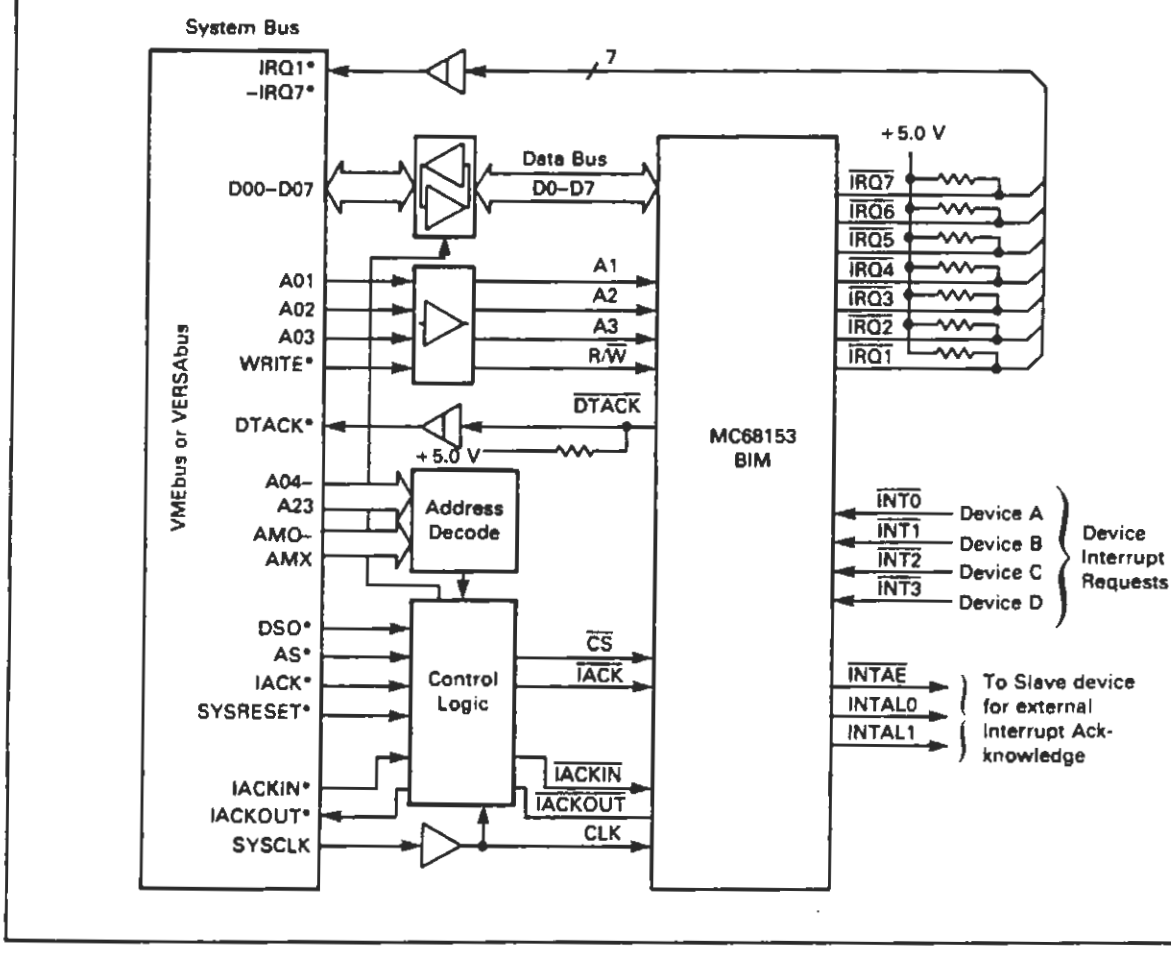
READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following BIM signals generate read and write cycles: Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{DTACK}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{W}$ and A1–A3 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{DTACK}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{W}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for $\overline{DTACK}$ is dependent on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus/VERSAbus INTERFACE BLOCK DIAGRAM



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 8 — READ CYCLE

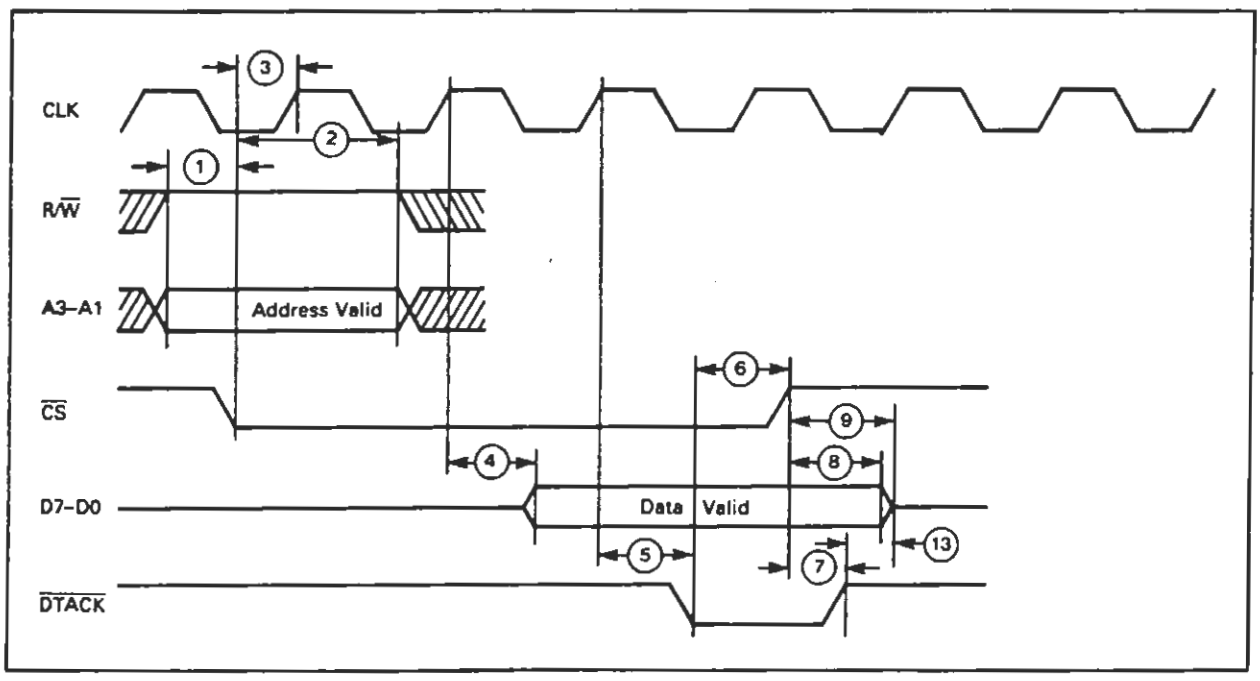
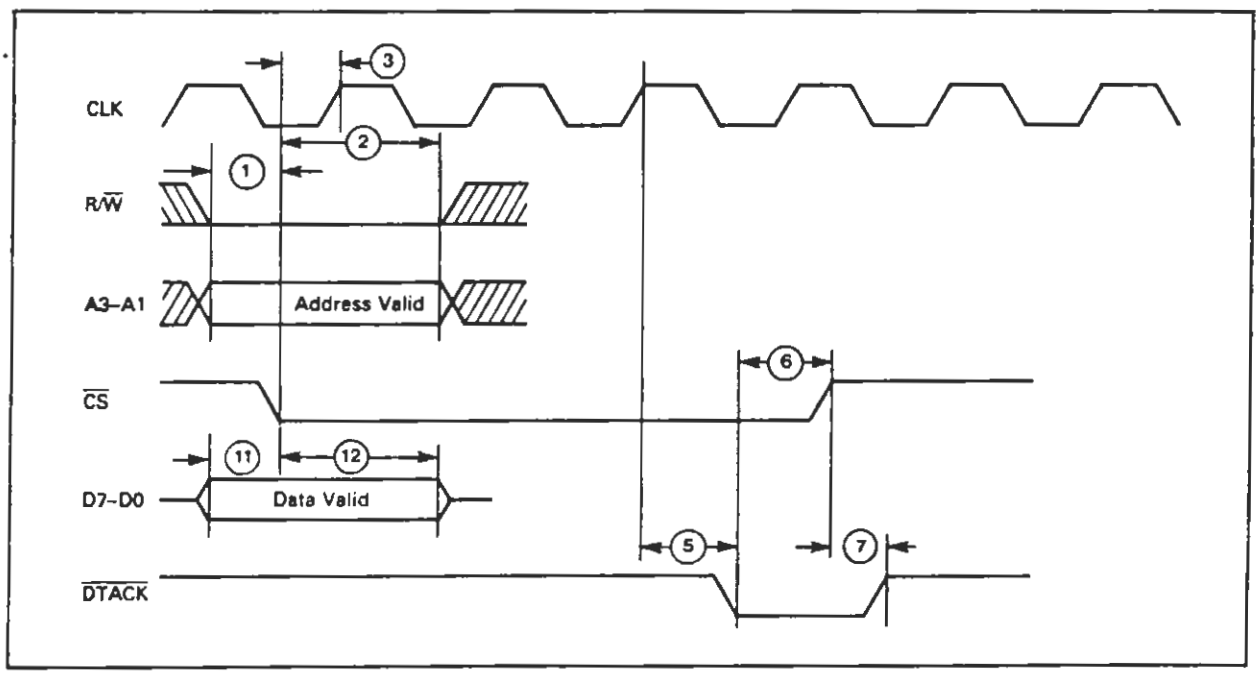


FIGURE 9 — WRITE CYCLE



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, and $\overline{INT3}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{IRQ1}$–$\overline{IRQ7}$) is asserted. The asserted $\overline{IRQX}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. The corresponding $\overline{IRQX}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{IACK}$ low. R/$\overline{W}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{IACKIN}$ is not asserted. Asserting $\overline{IACK}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{IACKIN}$ is not asserted), another Interrupter has responded to the $\overline{IACK}$ cycle. The cycle will end, the chip $\overline{IACK}$ is negated, and no additional action is required.

2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{IACKIN}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{IACKOUT}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.

3. Respond internally — For this case, $\overline{IACKIN}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{DTACK}$ signal asserted. $\overline{IACKOUT}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{INTERNAL}$ control register bit (X/$\overline{IN}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{IN}$ bit sets this response either internally (X/$\overline{IN}$ = 0) or externally (X/$\overline{IN}$ = 1).

4. Respond externally — For the final case, $\overline{IACKIN}$ is also asserted, a match is found and the associated control register has X/$\overline{IN}$ bit set to one. The MC68153 does not assert $\overline{IACKOUT}$ and does assert $\overline{INTAE}$ low. $\overline{INTAE}$ signals that the requesting device must complete the IACK cycle (supplying a vector end $\overline{DTACK}$) and that the 2-bit code conteined on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

1. One or more device interrupt inputs ($\overline{INT0}$–$\overline{INT3}$) has been asserted and corresponding control bit IRE value is one.

2. $\overline{IACK}$ asserted.

3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the highest number requester, that is, $\overline{INT3}$ has highest priority and $\overline{INT0}$ has lowest.

4. Control register bit X/$\overline{IN}$ of matching interrupt source must be zero.

5. $\overline{IACKIN}$ asserted.

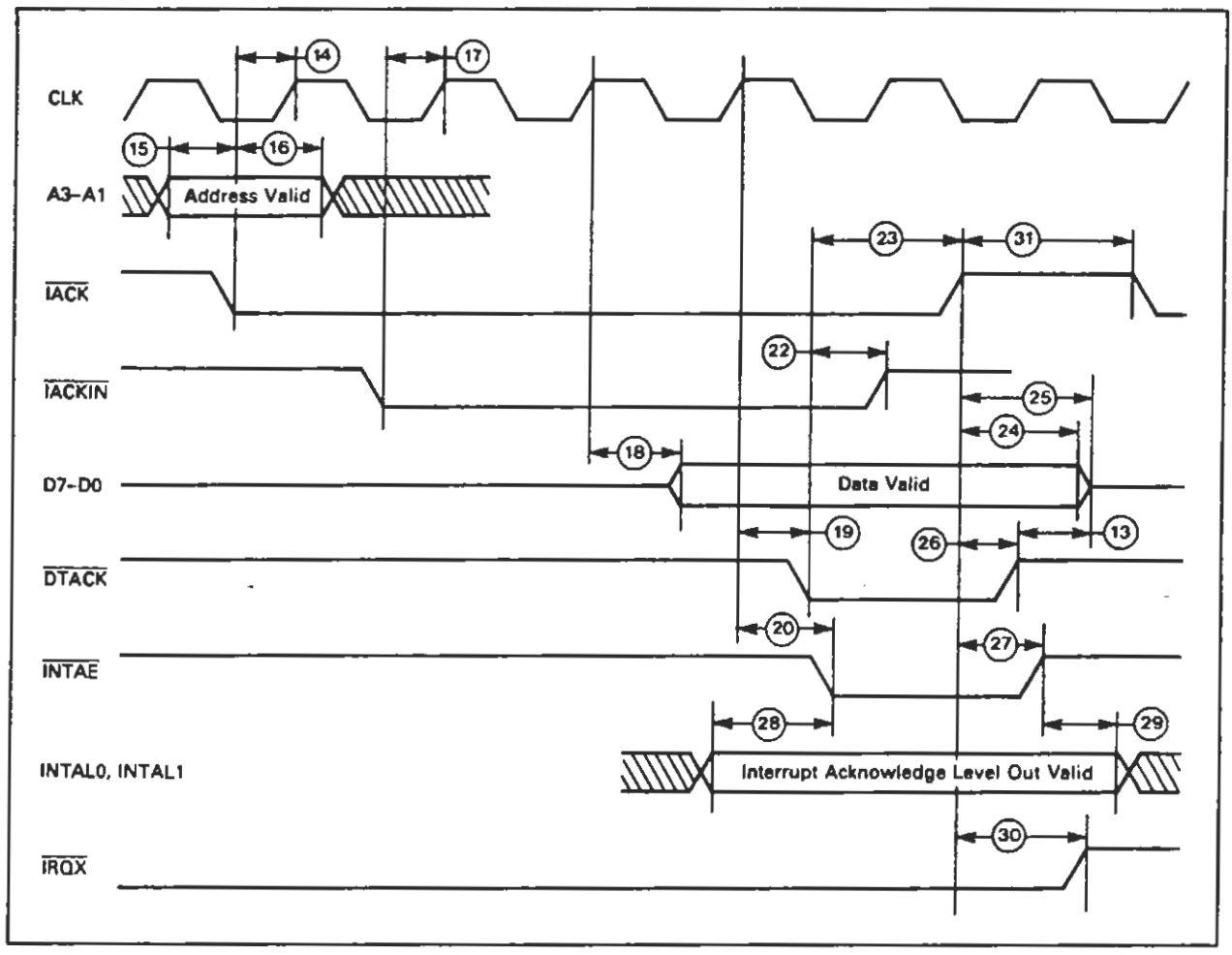
The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{DTACK}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{INTAE}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{DTACK}$ released) after $\overline{IACK}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{IRQX}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{IACKOUT}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{INT0}$–$\overline{INT3}$ after $\overline{IACK}$ is asserted are locked out to prevent any race conditions on the daisy chain.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR



External Interrupt Acknowledge

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{IN}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{DTACK}$ must be supplied by an external device. $\overline{INTAE}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{DTACK}$. The cycle is terminated after $\overline{IACK}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{IACKOUT}$ is not asserted and new device interrupts are disabled for reasons discussed above.

Pass On IACK Daisy Chain

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{IACKIN}$ is asserted. The following conditions are thus met:

1. $\overline{IACK}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{IACKIN}$ is asserted.

$\overline{IACKOUT}$ is asserted if these conditions are valid. This output drives $\overline{IACKIN}$ of the next Interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{IACKOUT}$ is negated after $\overline{IACK}$ is negated.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

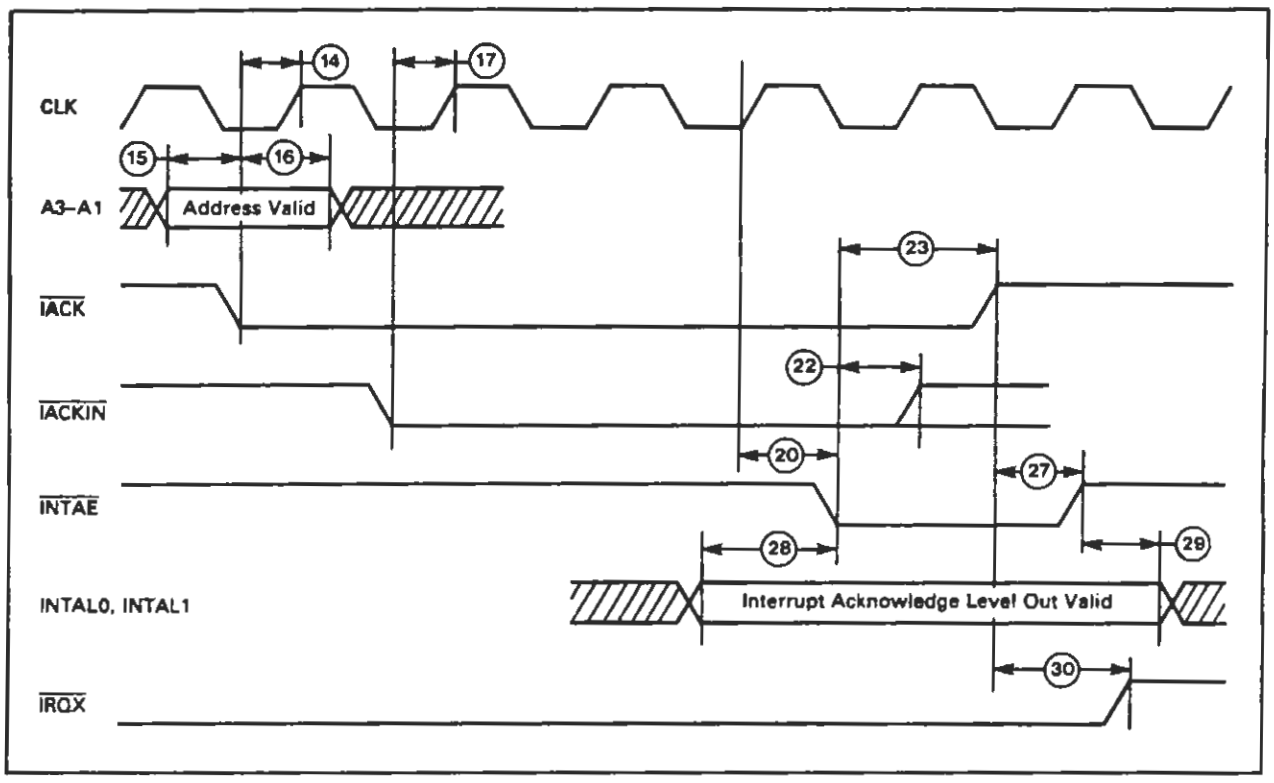
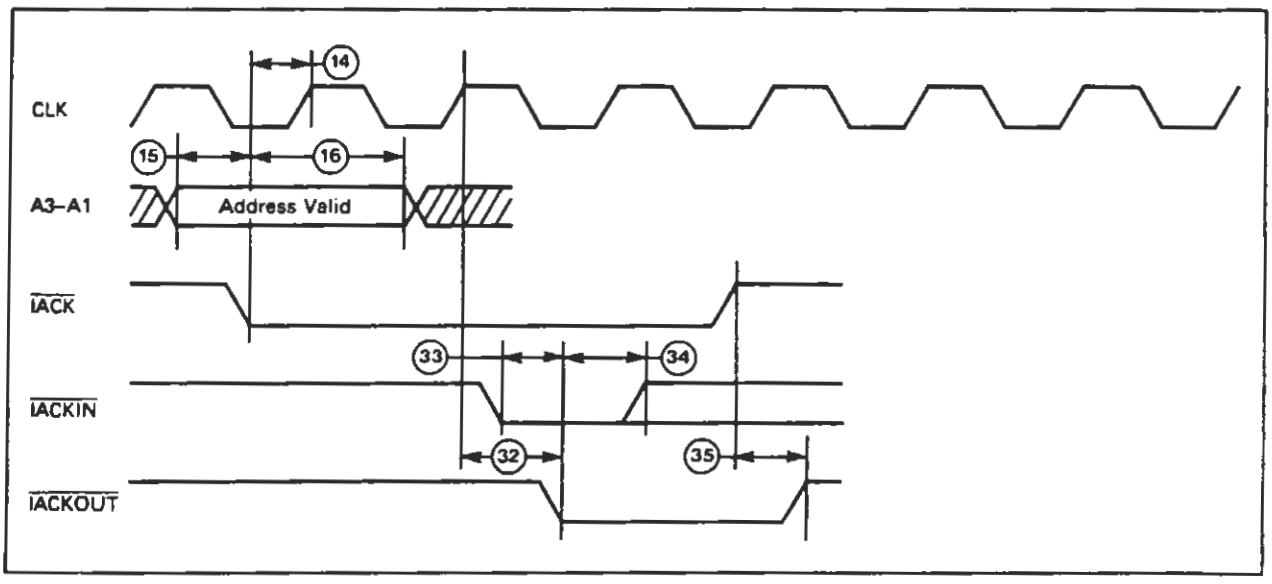


FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — IACKOUT



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus and VERSAbus applications derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14).

FIGURE 13 — RESET

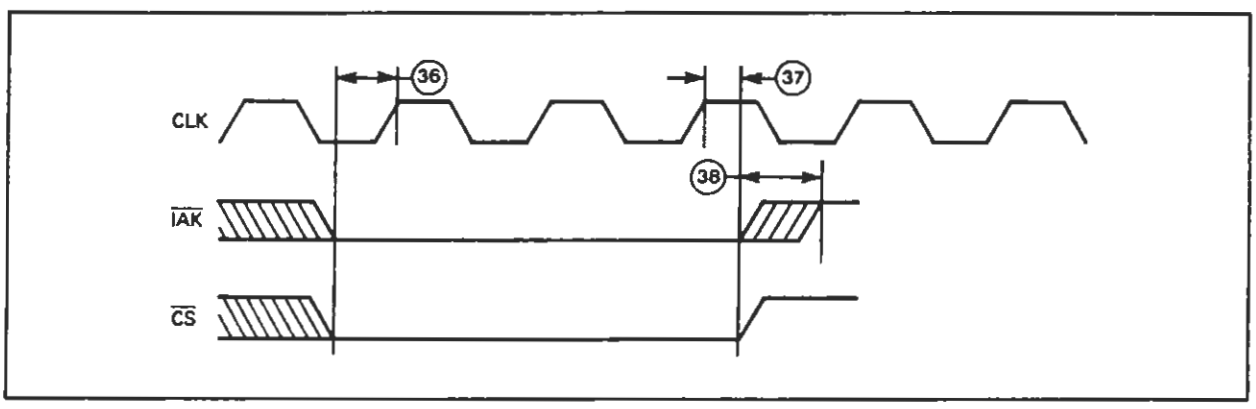
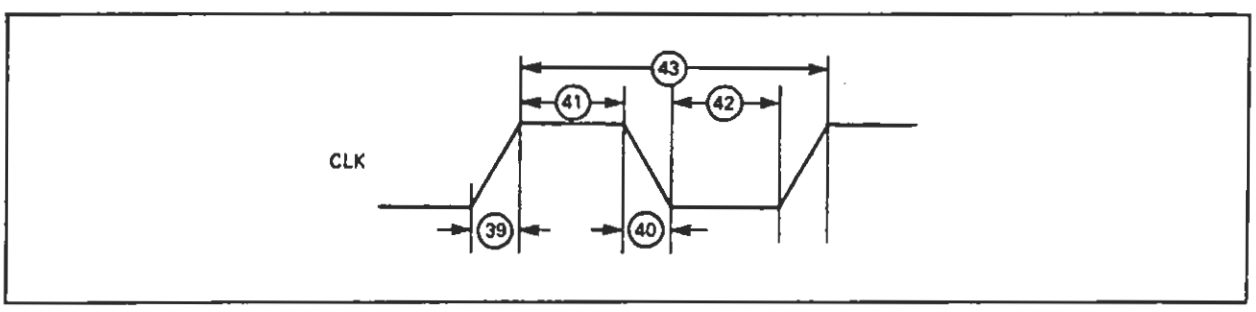


FIGURE 14 — CLOCK WAVEFORM



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 1
AC PERFORMANCE SPECIFICATIONS
(V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

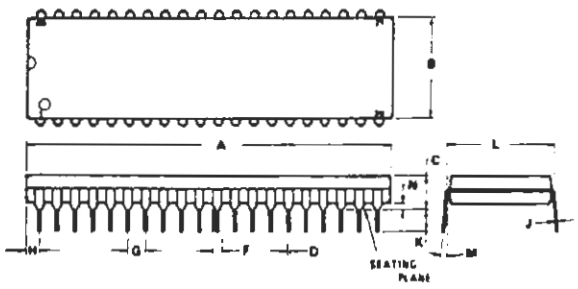
Number	Characteristic	Min	Max	Units	Notes
1	R/$\overline{W}$, A1–A3 Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
2	$\overline{CS}$ Low to R/$\overline{W}$, A1–A3 Invalid (Hold Time)	5.0	—	ns	
3	$\overline{CS}$ Low to CLK High (Setup Time)	15	—	ns	1
4	CLK High to Data Out Valid (Delay)	—	55	ns	2
5	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	2
6	$\overline{DTACK}$ Low to $\overline{CS}$ High	0		ns	
7	$\overline{CS}$ High to $\overline{DTACK}$ High (Delay)	—	35	ns	10
8	$\overline{CS}$ High to Data Out Invalid (Hold Time)	0	—	ns	
9	$\overline{CS}$ High to Data Out High-Impedance (Hold Time)	—	50	ns	
10	$\overline{CS}$ High to $\overline{CS}$ or $\overline{IACK}$ Low	20	—	ns	
11	Data In Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
12	$\overline{CS}$ Low to Data In Invalid (Hold Time)	5.0	—	ns	
13	$\overline{DTACK}$ High to Data Out High-Impedance	—	25	ns	10
14	$\overline{IACK}$ Low to CLK High (Setup Time)	15	—	ns	1
15	A1–A3 Valid to $\overline{IACK}$ Low (Setup Time)	10	—	ns	
16	$\overline{IACK}$ Low to A1–A3 Invalid (Hold Time)	5.0	—	ns	
17	$\overline{IACKIN}$ Low to CLK High (Setup Time)	15	—	ns	1, 8
18	CLK High to Data Out Valid (Delay)	—	55	ns	3
19	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	3
20	CLK High to $\overline{INTAE}$ Low (Delay)	—	40	ns	3
22	$\overline{DTACK}$ Low to $\overline{IACKIN}$ High	0	—	ns	8
23	$\overline{DTACK}$ Low to $\overline{IACK}$ High	0	—	ns	
24	$\overline{IACK}$ High to Data Out Invalid (Hold Time)	0	—	ns	
25	$\overline{IACK}$ High to Data Out High Impedance (Delay)	—	60	ns	
26	$\overline{IACK}$ High to $\overline{DTACK}$ High (Delay)	—	45	ns	10
27	$\overline{IACK}$ High to $\overline{INTAE}$ High (Delay)	—	35	ns	
28	INTAL0, INTAL1 Valid to $\overline{INTAE}$ Low (Setup Time)	1.0	2.0	CLK Per	
29	$\overline{INTAE}$ High to INTAL0, INTAL1 Invalid (Hold Time)	1.0	2.0	CLK Per	
30	$\overline{IACK}$ High to $\overline{IRQx}$ High (Delay)	—	50	ns	7, 10
31	$\overline{IACK}$ High to $\overline{IACK}$ or $\overline{CS}$ Low	20	—	ns	
32	CLK High to $\overline{IACKOUT}$ Low (Delay)	—	40	ns	5
33	$\overline{IACKIN}$ Low to $\overline{IACKOUT}$ Low (Delay)	—	30	ns	4, 8
34	$\overline{IACKOUT}$ Low to $\overline{IACKIN}$, $\overline{IACK}$ High	0	—	ns	8
35	$\overline{IACK}$ High to $\overline{IACKOUT}$ High (Delay)	—	35	ns	
36	$\overline{IACK}$ and $\overline{CS}$ both Low to CLK High (Setup Time)	15	—	ns	9
37	CLK High to $\overline{IACK}$ or $\overline{CS}$ High (Hold Time)	0	—	ns	
38	$\overline{IACK}$ or $\overline{CS}$ High to $\overline{IACK}$ and $\overline{CS}$ High (Skew)	—	1.0	CLK Per	6
39	Clock Rise Time	—	10	ns	
40	Clock Fall Time	—	10	ns	
41	Clock High Time	20	—	ns	
42	Clock Low Time	20	—	ns	
43	Clock Period	40	—	ns	

NOTES:

1. This specification only applies if the V8IM had completed all operations initiated by the previous bus cycle when $\overline{CS}$ or $\overline{IACK}$ was asserted. Following a normal bus cycle, all operations are completed within 2 clock cycles after $\overline{CS}$ or $\overline{IACK}$ have been negated. If $\overline{IACK}$ or $\overline{CS}$ is asserted prior to completion of these operations, the new cycle, and hence, $\overline{DTACK}$ is postponed.
   If the $\overline{IACK}$, $\overline{IACKIN}$ or $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later (i.e. $\overline{IACK}$ will not be recognized until the next rising edge of the clock).
2. Assumes that 3 has been met.
3. Assumes that 14 and 17 have both been met.
4. Assumes that 14 has been met. ($\overline{IACKOUT}$ cannot go low prior to $\overline{IACKIN}$ going low).
5. Assumes that 14 has been met and $\overline{IACKIN}$ has been low for at least the amount of time specified by 33.
6. 38 is the minimum skew between the last moment when both $\overline{IACK}$ and $\overline{CS}$ are asserted to when both are negated, to insure that an access cycle is not unintentionally started.
7. Assumes no other $\overline{INTx}$ input is causing $\overline{IRQx}$ to be driven low.
8. In non-daisy chain systems, $\overline{IACKIN}$ may be tied low.
9. Failure to meet this spec. causes RESET to be ignored for 1 clock period. It is then necessary to keep these signals low for 3 clock periods instead of 2.
10. Delay time is specified from input signal to Open-Collector Output pulled High thru 1.0 kΩ resistor to +6.5 V.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

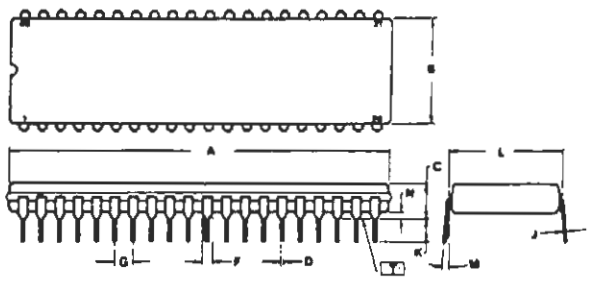
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 711-03
PLASTIC PACKAGE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌀ 0.25 (0.010) M T A M
3. T IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 1973.

CASE 734-04
CERAMIC PACKAGE

TYPICAL THERMAL CHARACTERISTICS

Package	θJA (Junction to Ambient) Still Air	Junction Temperature Still Air @ 70°C Ambient
L Suffix	40°C/W	147°C
P Suffix[1]	35°C/W	137°C

NOTES:
1. For reliable system operation the maximum allowable junction temperature (T_J) for plastic encapsulated packages has been limited to + 140°C. Exceeding this limit will accelerate "wear-out" mechanisms associated with industry standard assembly methods using thermosonic ball bonds to attach gold (Aμ) bond wire to aluminum (Al) bond pads on the die surface.
2. At T_J = 140°C, time to 0.1% failure due to Aμ/Al interconnect = 8,920 Hours.

Motorola reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Employment Opportunity/ Affirmative Action Employer.

MOTOROLA *Semiconductor Products Inc.*
BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DOCUMENTATION EVALUATION FORM

VMIC welcomes your comments and suggestions.

Please return this form to:

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
(205) 880-0444
1-800-322-3616

Evaluation: Please rate the following areas on a scale of 1 to 5 (1 = Poor; 5 = Excellent).

DOCUMENT NO.: _____
REVISION DATE: _____

READABILITY	_____	ILLUSTRATIONS	_____
ORGANIZATION	_____	PROGRAMMING INFORMATION	_____
ACCURACY	_____	SPECIFICATIONS	_____
COMPLETENESS	_____	MAINTENANCE DIAGRAMS	_____

SPECIFIC PROBLEMS: **PAGE(s)**

( ) CLARIFICATION REQUIRED _____

( ) NOT ENOUGH INFORMATION GIVEN _____

( ) TYPOGRAPHICAL ERRORS _____

( ) TECHNICAL ERRORS (EXPLAIN): _____

_____

DOCUMENT USE: (check all that apply)

( ) HARDWARE	( ) SOFTWARE	( ) PRODUCT EVALUATION
( ) OPERATION	( ) MAINTENANCE	( ) TRAINING

ADDITIONAL COMMENTS: _____

_____

_____

_____

YOUR NAME: _____
TITLE: _____
COMPANY: _____
MAIL STOP: _____
STREET: _____
CITY, STATE, ZIP: _____
PHONE: _____

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP