VMIVME-3123

16-bit High Throughput Analog Input Board,16 Channels with Simultaneous Sample-and-Hold Inputs

Product Manual

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500-003123-000 Rev. E

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General Description

The VMIVME-3123 board is a member of VMIC's extensive family of analog input/output products for the VMEbus. The board boasts 16-bit digitizing resolution on 16-channels, simultaneous sample/hold, software programmable channel select and sampling rate, and a data buffer up to 8 Mbytes. The VMIVME-3123 board provides exceptional dynamic range and high aggregate sampling rate. Various operating modes are supported including transient capture (burst mode) and continuous sample modes, both of which can be configured with internal or external synchronization.

The VMIVME-3123 performs a calibration upon host command of all the analog input channels and stores the corresponding gain and offset correction values in memory. These correction values are then applied to the individual data samples before they are loaded into the DRAM data buffer. Multiple boards can be synchronized together to enable as many as three boards to sample simultaneously. An Interval Timer, Bus Interrupter, DRAM and status flags simplify the monitoring of data within the dual port data buffer. The broad range of system applications that can benefit from the VMIVME-3123 capabilities include factory automation, process control, data acquisition systems, training simulators and laboratory instrumentation.

VMIVME-3123 Features

The following brief overview of principal features illustrates the flexibility and performance available with the VMIVME-3123 board:

- 16 differential analog inputs
- 16-bit A / D conversion, one converter per channel
- Simultaneous sample-and-hold
- 381 Hz to 100 kHz selectable sampling rate from internal timer
- Auto calibration upon host demand (no channel trimmers)
- Analog input channel ranges of ± 5 V, ± 10 V
- 1 or 4 Mbyte sample data buffer (2 or 8 Mbytes)
- Control registers in short I / O (A16), DRAM data buffer in standard (A24) or extended (A32) data space
- Host controlled data buffer size
- Optional low pass anti-aliasing input filters
- Transient capture (burst) and continuous sampling modes
- Choice of external or internal clocking of data samples
- Bus interrupter for buffer control and status
- Board self-test using built-in-test circuitry. Internal reference applied to channel inputs and all active devices tested

Functional Description

The VMIVME-3123 (Figure 1) is a high speed, high-resolution, 16-bit, 16-channel analog digitizing input board with simultaneous sample and hold for VMEbus system applications. A large DRAM data buffer, programmable on-board timer, calibration, and VMEbus interrupter module enable the VMIVME-3123 board to support extensive analog input traffic with a minimum of host processor involvement.

All 16 analog input channels are simultaneously sampled and digitized. During this time, the previous sample (sample n-1) is read from the ADC's, corrected, and stored in the data buffer (if the channel is enabled). The data may then be accessed anytime from the VMEbus. Data correction consists of applying a gain and offset value determined during calibration to the digitized sample. The analog input voltage ranges are software selectable as ±5 and ±10 V.

The user has control of the analog conversion timing by way of the VMEbus. The A / D converter sample clock source can be chosen from a programmable timer on the VMIVME-3123 or an external sample clock supplied through the P5 front panel connector. The trigger (indicates when board is to store samples in the data buffer) source can be software selectable from a hardware I / O register (host controlled), the P5 front panel connector (external), or from the Digital Signal Processor (DSP checking for a threshold value on a particular input channel). The VMIVME-3123 can operate as a stand alone digitizer, or in tandem with other VMIVME-3123's in a master / slave configuration.

The digitized samples are placed in a DRAM data buffer available in 2 or 8 Mbyte sizes which hold 1 and 4 Mword samples, respectively. The actual buffer size used is dependent upon the number of channels sampled and the programmed buffer size. When using the transient capture mode, the store trigger position is software selectable to allow pre -, mid -, or post-collection of data.

When using the continuous sample mode of operation, the board's VMEbus interrupter module provides a buffer half-full and a buffer full flag that can be used in a polling manner or to generate VMEbus interrupts.

The VMIVME-3123's VMEbus interface locates the board's registers in short I / O space and the DRAM data buffer in standard / extended addressing space. The registers consist of four hardware registers which are available at all times to the host, and DSP controlled firmware registers which are available only during IDLE mode. The DRAM data buffer can be enabled / disabled via host software allowing multiple boards to reside in the same addressing space. The VMEbus data interface supports block transfer (BLT) accesses to aid the user in high speed transfer of large quantities of data.

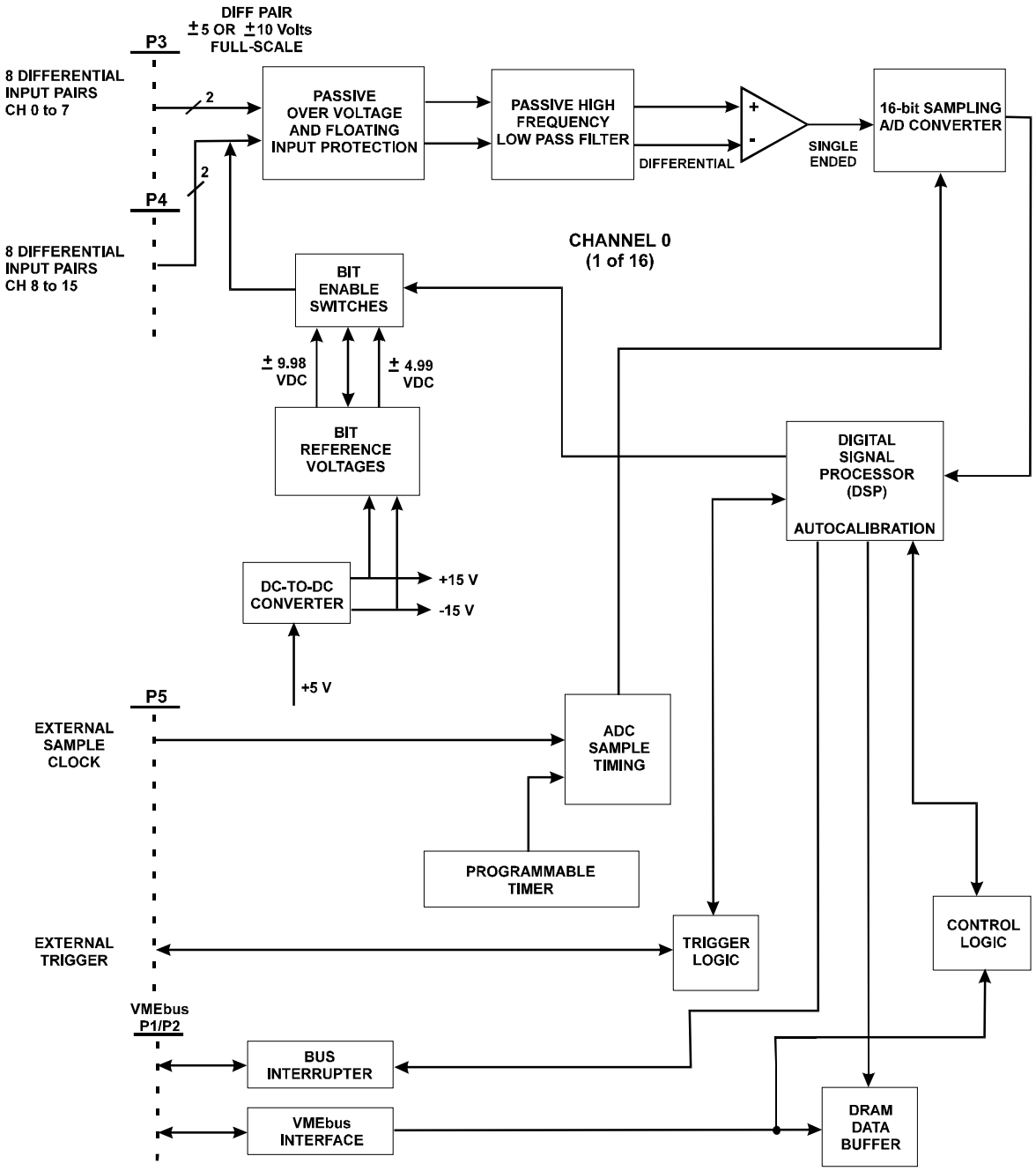

Figure 1 VMIVME-3123 Functional Block Diagram

Reference Material List

For a detailed explanation of the VMEbus and its characteristics, refer to "The VMEbus Specification" available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(602) 951-8866
FAX: (602) 951-0720
www.vita.com

Physical Description and Specifications

Refer to Product Specification, 800-003123-000 available from:

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

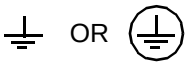
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

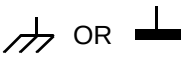
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



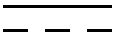
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

STOP: Informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: Denotes a hazard. It calls attention to a procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: Denotes a hazard. It calls attention to an operating procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER

1

Theory of Operation

Contents

Introduction

This section describes the internal organization of the VMIVME-3123 board and reviews the general principles of operation. The major board functions are summarized in the remainder of Chapter 1 and supplemented by programming details in Chapter 3.

The VMIVME-3123 board contains the following principal hardware functions:

- Analog input circuitry and digitizing
- Sample clock sources
- Trigger sources
- Correction of digitized data
- DRAM buffer memory
- VMEbus interface
- VMEbus interrupter
- Power converters

Analog Input Circuitry

The analog circuitry is responsible for interfacing to the external field wiring, for signal conditioning, and for digitizing the samples. Several blocks make up the analog circuitry and will be described in detail. These blocks are:

- Built-in-Test Circuit (BIT)
- Input switching and instrumentation amplifier
- Fourth-order active filter
- Analog-to-Digital Converter (ADC)

Built-In-Test (BIT) Circuitry

The Built-In-Test (BIT) circuit contains a precision reference which supplies the input circuitry with a known voltage for calibration of each channel. The available voltages from the BIT circuit are ±9.98, ±4.99, and 0.00 volts. The desired voltage is selected using four bits available in the Analog Configuration register on page 64.

Input Switching and Instrumentation Amplifier

Each input contains a passive RC filter followed by a quad SPDT (single pole, double throw) switch. The switch is used to disconnect the field inputs and apply the BIT voltages during calibration. The switch is also used to control the gain of the input depending on the input range selected. The input range is selected by the Analog Configuration register. Each input contains an Instrumentation Amplifier (IA) which converts the differential input signal to single-ended for further processing and digitizing. The IA also provides common-mode rejection.

Fourth-order Active Filter

Each input contains a fourth-order active filter with factory-optional Butterworth or Bessel response. The frequency cut-off is also factory-optional as listed in the Specification.

Analog-to-Digital Converter

Each input has its own Analog-to-Digital Converter (ADC). The ADC is a 16-bit No Missing Codes successive-approximation device. It has its own internal reference and track / hold circuitry and requires only a convert and clock signal. The ADC outputs the previously converted data in a serial two's complement format while the present sample is being converted. The serial data is converted to parallel for input to the DSP for gain and offset correction.

Sample Clock Sources

The VMIVME-3123 board uses sample clock sources to start the ADC conversion process. The host may choose from an internal 14-bit timer derived from a 12.5 MHz clock, VMEbus I/O command, or an external host supplied clock signal.

The chosen clock source is divided into two clock signals, sample 0 and sample 1, which provide the sampling signals for analog input channels 7-0 and 15-8, respectively. The VMIVME-3123 also allows the user to choose a clock doubling feature which routes the input clock source through a phase splitting flip-flop and staggers the sampling of channels 7 through 0 and 15 through 8. Channels 0 and 8, 1 and 9, etc. become paired and should be connected to the same input signal. The sample clock input source can now be increased above 100 kHz (up to 200 kHz) and the effective sample rate of the channel increases to that rate while the actual sampling rate on the individual ADC does not go beyond 100 kHz.

The user can choose to use multiple boards in parallel. The host should set the multi-board bit (bit 3) to a logic "1" in the Trigger Configuration register on all the boards and set the master bit (in the same register) to a logic "1" on the master board and to a logic "0" on the slave boards. This configures all the boards to receive the clock source selected on the master board.

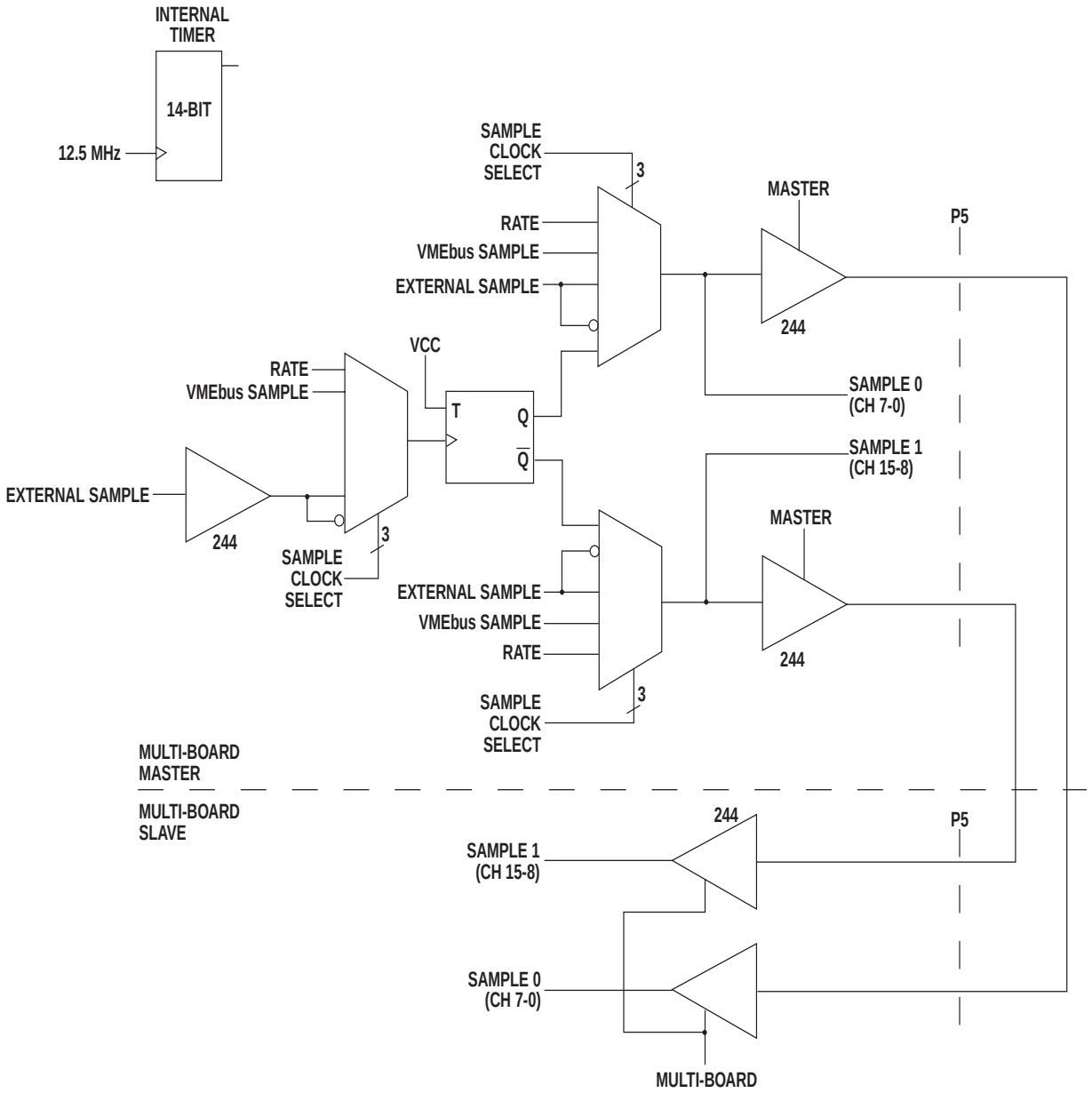


Figure 1-1 VMIVME-3123 Sample Clocks

Trigger Sources

The VMIVME-3123 board uses trigger sources as an indication of when to conclude data capture during the Transient Capture mode of operation. The trigger sources are only used during Transient Capture mode. Figure 1-2 on page 26 shows the structure of the trigger circuitry, including a second board set-up as a slave if a multi-board configuration is needed. First, the host should set the multi-board bit (Bit 3) and the master bit (Bit 4) of the Trigger Configuration register to initialize the buffers used in multi-board operation. When the multi-board bit is a logic "0", the buffer receiving the bussed trigger signal is off. When the multi-board bit is a logic "1" and the master bit is a logic "0", the board will receive the bussed trigger signal. If both the multi-board and master bits are set to a logic "1", both the receiving and driving buffer will be enabled.

The trigger select bits are used to select the desired trigger from a choice of a differential RS-422 external source (both positive or negative pulse), an I/O trigger bit from the CSR1, or the DSP trigger which compares a host selected input channel with a host selected threshold value. When using an external source, the trigger pulse should be greater than 500 nanoseconds. During the course of correcting and storing the sampled data, the DSP monitors the Flag In (FI) pin connected to the trigger circuitry output. Upon receiving a trigger signal from the trigger output circuitry, the Flag Out (FO) pin will be set. The DSP will then proceed to either stop processing sampled data and return to IDLE mode if the pre-trigger setup was selected, or finish collecting and storing data and return to IDLE mode if mid- or post-trigger options were selected. See Chapter 3 for more information on triggering.

NOTE: The board must be initialized prior to entering Transient Capture mode. Before beginning the sampling process, the board clears the trigger circuitry. This process takes approximately 1.27 msec. The user needs to make sure the trigger event does not occur sooner than 1.27 msec after the board is put into Transient Capture mode.

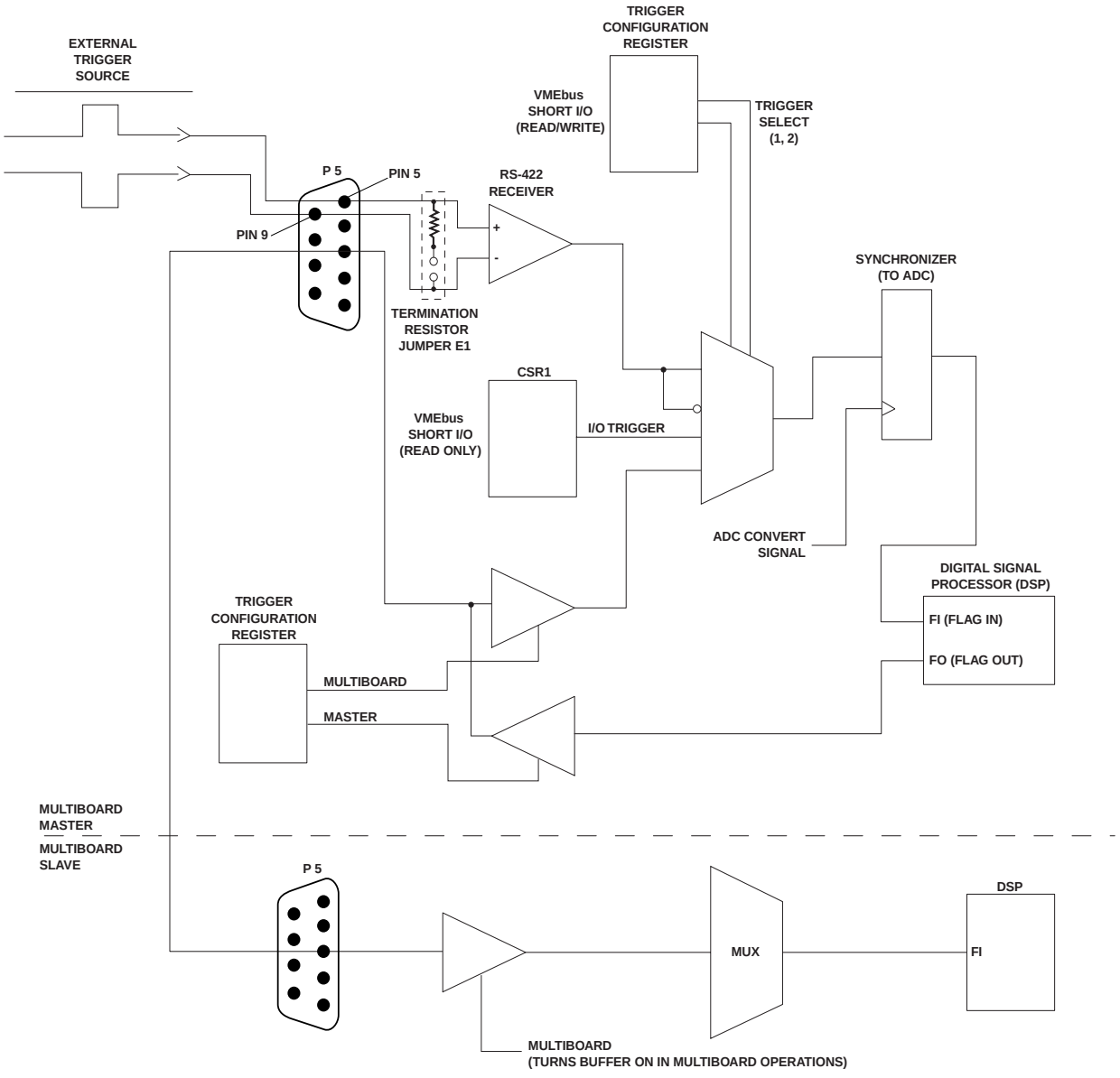


Figure 1-2 VMIVME-3123 Trigger Operation

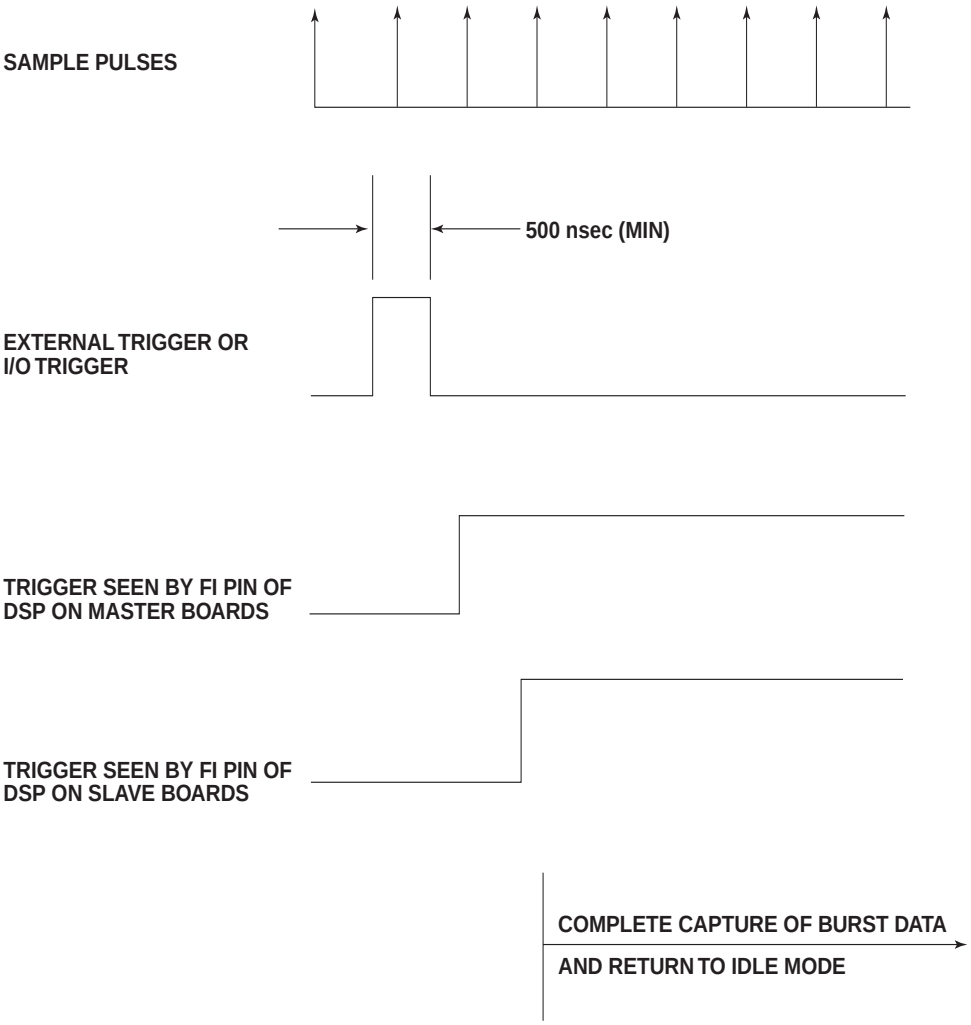


Figure 1-3 Trigger Timing Wave Forms

Correction of Digitized Data

Correction of the digitized data is performed by an on-board Digital Signal Processor (DSP). The digitized data from the previous sample period (n-1) is output serially from each of the ADCs and parallel to serial conversion is performed to format the data for reception by the DSP. The DSP sequentially reads the digitized parallel data and performs a gain and offset correction using coefficients determined during the calibration mode. After correcting the data, the DSP checks for channel enables in determining which channel's data will be placed in DRAM, checks for buffer half-full and full conditions, and performs other assorted firmware tasks. The DSP then writes the corrected samples to a FIFO and informs an on-board state machine to load the data into the DRAM. The state machine requests the DRAM from the memory bus arbiter and bursts the samples into DRAM when the memory bus is granted to it.

DRAM Buffer Memory

The DRAM Buffer Memory consists of either a 2 Mbyte x 32 (8 Mbyte) or 512 K x 32 (2 Mbyte) SIMM module loaded on the VMIVME-3123 board. There are three functions that use the memory and need to be arbitrated. The highest priority function is the DSP's sample data load. The DSP loads data into a FIFO and then instructs a hardware state machine to burst load the data from the FIFO to the DRAM. This data load operation may hold-off a VMEbus DTACK up to 1.5 µsec. This operation occurs at the same rate the channels are being sampled. The second highest priority function is DRAM refresh. A refresh will occur every 16 µsec and will hold the memory occupied for approximately 500 nanoseconds. VMEbus accesses by the host have the lowest priority. The VMIVME-3123 must use the same size SIMM module it was configured with originally because internal programming of the EPLD's must match the installed SIMM module. See Figure 1-4 for the DRAM Buffer Memory Block Diagram.

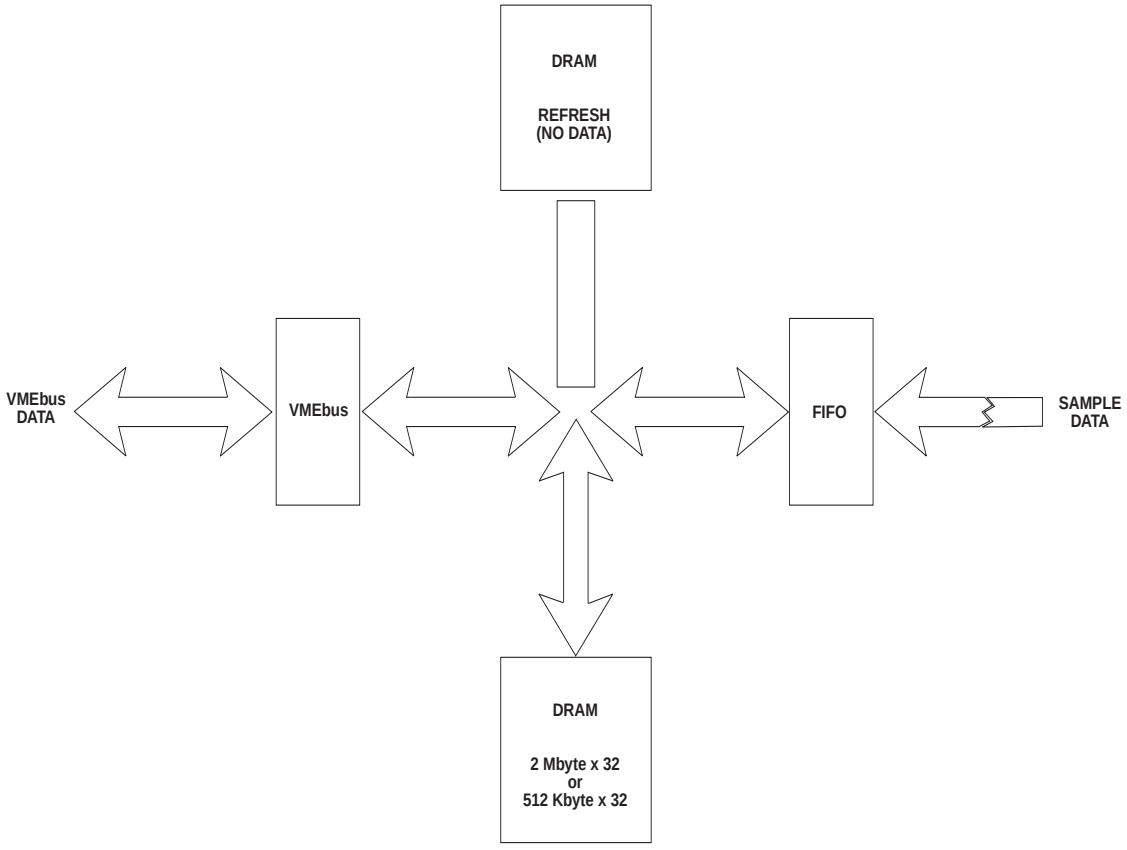


Figure 1-4 DRAM Buffer Memory Block Diagram

VMEbus Interface

The VMIVME-3123 VMEbus slave interface consists of a VMEbus short I/O interface used for communicating with the Control and Status registers, and a VMEbus standard/extended interface used to read the accumulated data samples (see Figure 1-5 on page 31). The short I/O interface communicates with four hardware registers and numerous firmware. The hardware registers are physically located in programmable logic and their contents are available at all times. The access times for these registers are in the order of hundreds of nanoseconds because no firmware interaction is involved. The firmware registers are physically located in the DSP's SRAM and are only available when the VMIVME-3123 board is operating in IDLE mode. IDLE mode allows the firmware enough time to service the VMEbus requests. The access times of the firmware registers is in the order of 1.5 to 3 msec due to the fact that the DSP firmware is involved with servicing these requests.

The VMIVME-3123 board's VMEbus standard and extended interface is used to retrieve the stored sample data contained in the DRAM, and is under host control. The access to the interface is controlled by the CSR0, the Data Buffer Address register and the Memory Configuration register. The buffer enable bit located in CSR0 either enables or disables the entire memory from access by the VMEbus. The Data Buffer Address register allows the host to choose either standard (A24) or extended (A32) addressing space, the access type and the address offset desired. The Memory Configuration register is a read-only register allowing the host to determine the size of the DRAM used with the board.

Data can be read/written as either 32, 16 or 8 bits and includes VMEbus BLT (block transfers) support as well. The VMEbus BLT hardware allows the board to use the enhanced page mode feature of the DRAM on VMEbus read cycles, thereby increasing the VMEbus data rate by pre-reading the next piece of data (if requested). On VMEbus BLT write accesses, the page mode operation does not result in faster access times. Refer to the VMIVME-3123 Specification for actual access times.

NOTE: The firmware registers are word (16-bit) oriented which allows them to be read in a byte or word format but written to in a word format only. Byte writes to firmware registers will return a DTACK* to the host but leave the contents of the register unchanged. The short I/O interface uses hardware jumpers to set-up its configuration in VMEbus space.

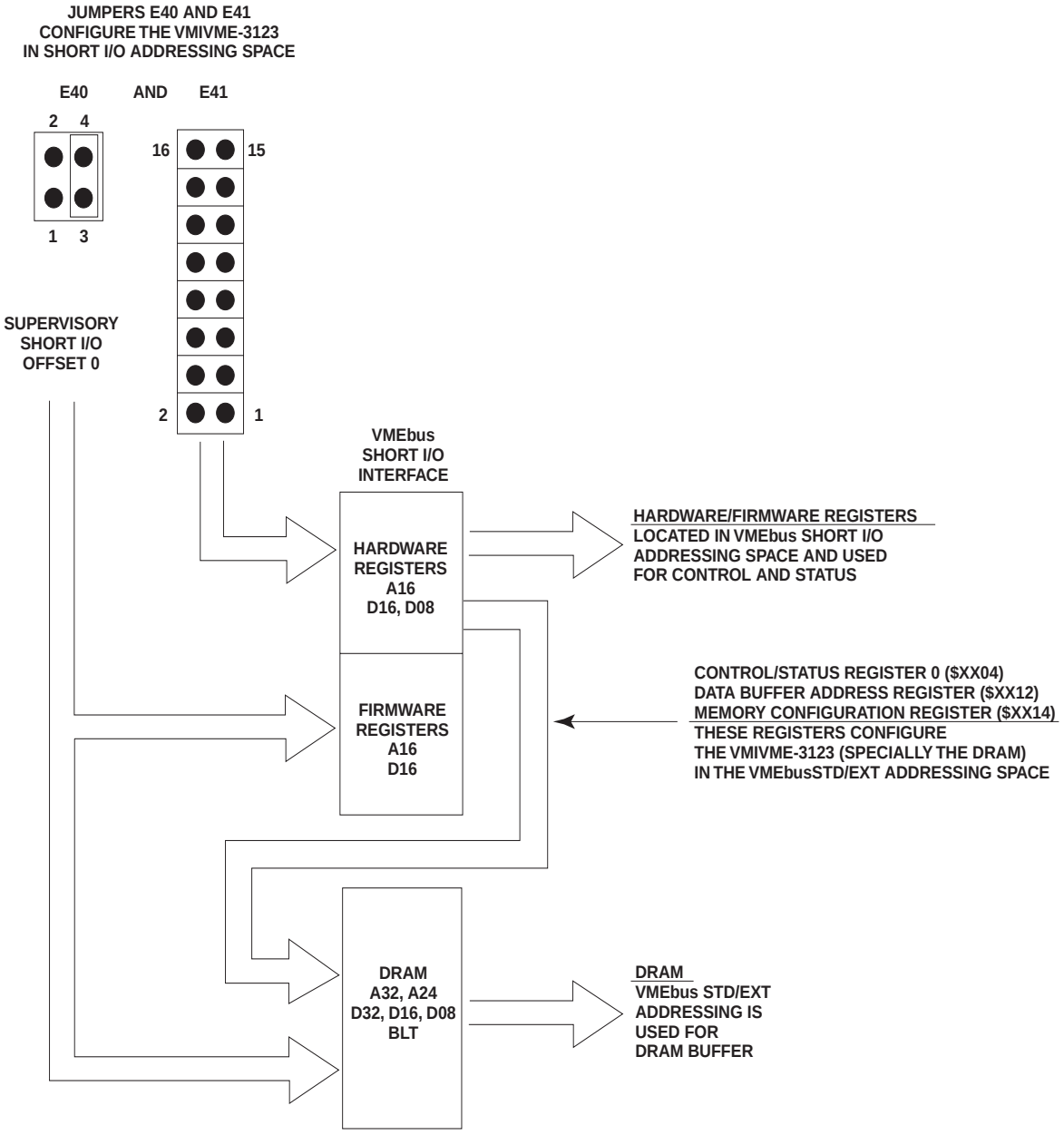


Figure 1-5 VMIVME-3123 VMEbus Interface Block Diagram

VMEbus Interrupter

The VMIVME-3123 Interrupter circuit is shown in Figure 1-6. The Control and Status Register 1 and the Interrupt Vector register are used in controlling interrupt operations. The interrupt flags A and B located in CSR1 are controlled by the action of the DSP and are set according to the operating mode chosen. The flag can be polled by reading CSR1. The act of reading CSR1 clears the interrupt A and B flags. An additional set of flip-flops are latched when an interrupt A or B flag is set and generates a VMEbus interrupt according to the interrupt level bits if the interrupt level bits in CSR1 are non-zero. At this point, the host hardware generates a VMEbus IACK cycle which clears the interrupt generating flip-flops and returns a pre-programmed interrupt vector to the host. The host should then clear the interrupt flags in its interrupt service routine by reading CSR1. Hardware circuitry handles the IACKIN*/IACKOUT* daisy chain, as well as generating the DTACK* signal.

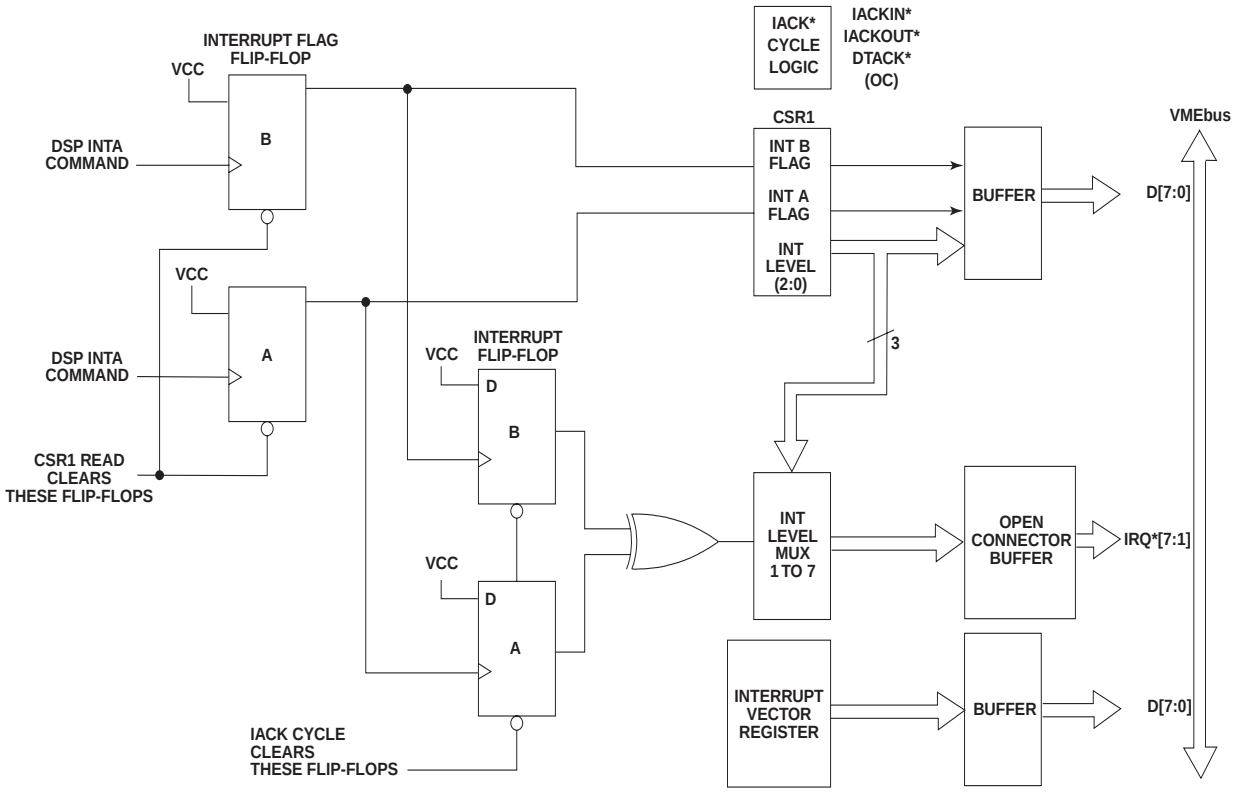


Figure 1-6 VMEbus Interrupter Circuitry

Power Converters

The VMIVME-3123 uses DC to DC converters on-board to convert +5 VDC logic power from the VMEbus into isolated and regulated ±15 and +5 VDC for the analog networks. This method allows the user to disregard the optional ±12 VDC on the VMEbus backplane.

CHAPTER 2

Configuration and Installation

Contents

Introduction

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

WARNING: Do not install or remove boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Before Applying Power: Checklist

Before applying power to the VMEbus chassis in which the board is installed, execute the following checklist to ensure that the board has been correctly prepared for operation.

1. Verify that the sections pertaining to Chapter 3 have been reviewed and applied to system requirements._____
2. Review the *Operational Configuration* on page 37 and Table 2-1 on page 39 to verify that all jumpers are configured correctly for the application. _____
3. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to *Connector Descriptions* on page 41. _____
4. Physical installation should have been completed as described in that section. _____
5. Ensure that all system cable connections are correct._____
6. Ensure that no empty slots are between the system controller and the VMIVME-3123 or that the interrupt daisy chain jumpers are properly installed.

Operational Configuration

The VMIVME-3123 is designed to minimize the number of field programmable jumpers to be set by the user. VMEbus Short I/O address offset and access modes are controlled by field replaceable jumpers. In addition to these jumpers, the board contains a RS-422 termination resistor jumper. This section describes the use of these jumpers, and their effects on board performance. Locations and functions of all VMIVME-3123 jumpers are shown in Figure 2-1 on page 38 and Table 2-1 on page 39.

Factory-Installed Jumpers

Each VMIVME-3123 board is configured at the factory with its Short I/O (A16) jumpers configured for the following:

- Board Identification is located at $0000 in the **Short I/O space.**
- The board access is jumpered to respond to either supervisory or nonprivileged.
- The external trigger's RS-422 receiver termination resistor is off.
- Digital ground is not provided to connector P5 (E2 is removed).

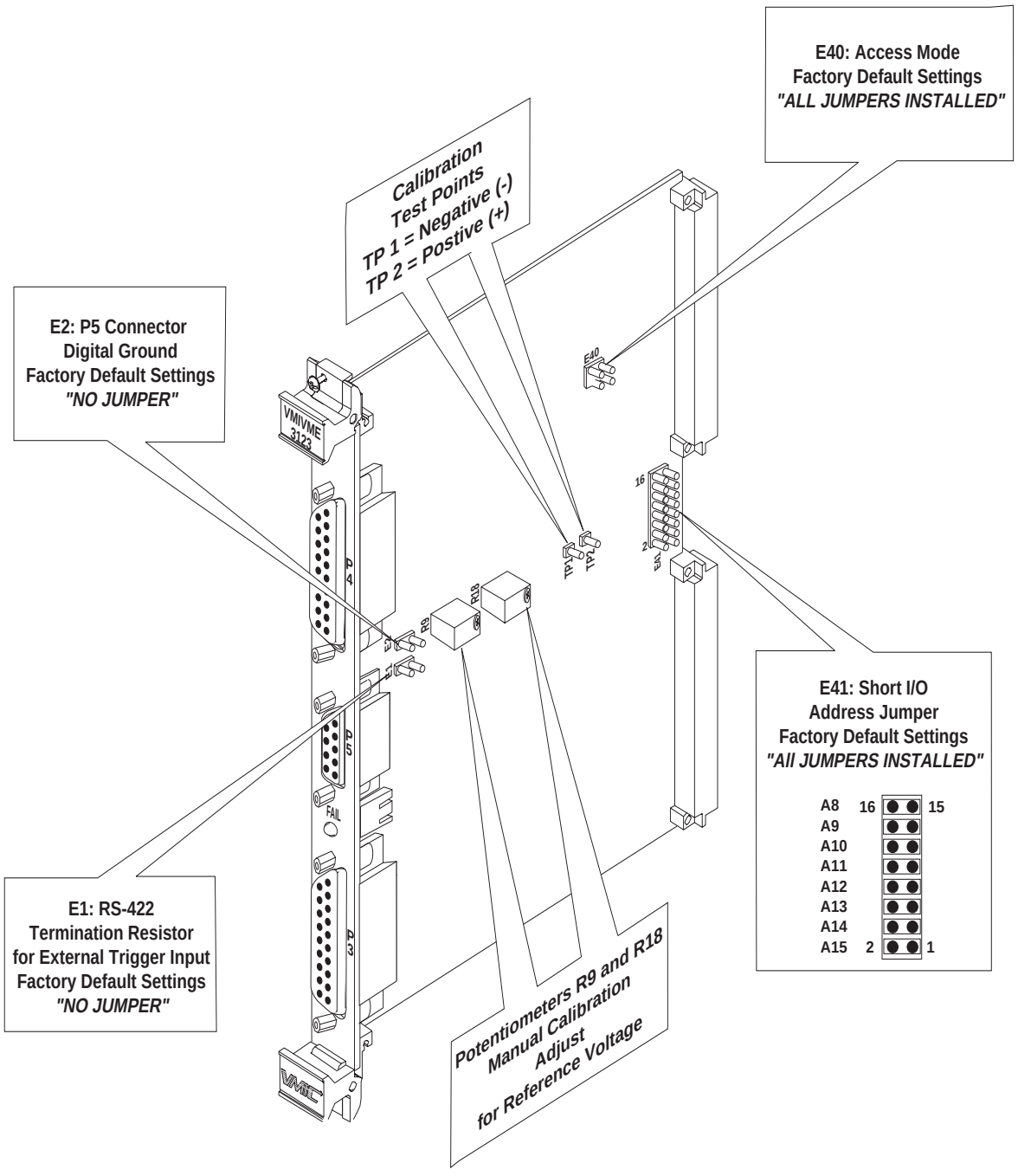


Figure 2-1 Locations of User Configurable Jumpers, Calibration Potentiometers and Test Points

Table 2-1 Programmable Jumper Functions

Jumper IDENT	Function (Installed)	Factory CONFIG
E1 -1, 2	RS-422 Termination Resistor (EXT Trigger)	Removed
E2 -1, 2	Connector P5 Digital Ground	Removed
E40 -1, 2	Access Mode, Nonprivileged*	Installed
E40 -3, 4	Access Mode, Supervisory*	Installed
E41-1, 2	Address Bit A15 = 0	Installed
E41-3, 4	Address Bit A14 = 0	Installed
E41-5, 6	Address Bit A13 = 0	Installed
E41-7, 8	Address Bit A12 = 0	Installed
E41-9, 10	Address Bit A11 = 0	Installed
E41-11, 12	Address Bit A10 = 0	Installed
E41-13, 14	Address Bit A9 = 0	Installed
E41-15, 16	Address Bit A8 = 0	Installed

* See “Access Modes” below for more details.

NOTE: To be consistent with conventional VMEbus development system nomenclature, hexadecimal numbers in this document are designated a "$" prefix unless otherwise indicated. Decimal numbers are presented without a prefix.

Access Modes

Short I/O address space, supervisory (privileged) and user (nonprivileged) access are selected by jumper E40. Figure 2-2 shows the jumper location and access mode.

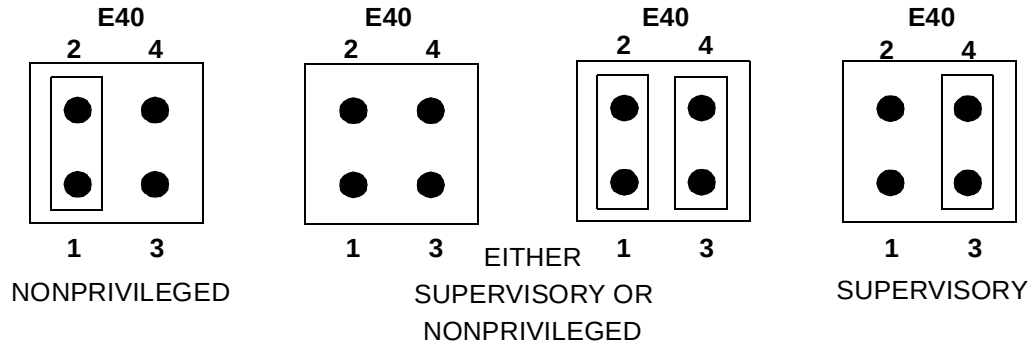


Figure 2-2 Supervisory, Nonprivileged Access Mode, and Jumper Locations for Short I/O Space

Board Address

The board's short I/O address is configured by jumper E41. The jumper corresponding to the address bits are shown in Figure 2-3.

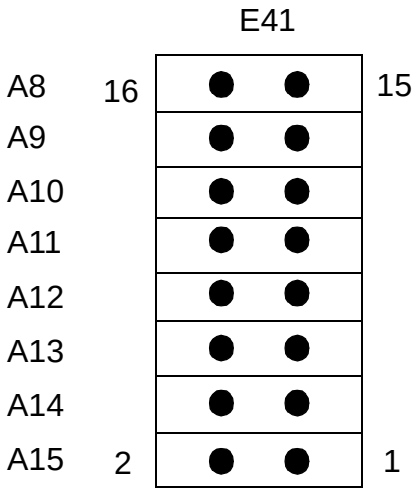


Figure 2-3 Board Configuration Jumper

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in jumper block E41, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A8 is the least significant address bit that can be jumper-selected, and has a weight of 256 bytes.

RS-422 Termination Resistor

The External Trigger circuitry includes a RS-422 differential receiver to accommodate trigger sources some distance from the board. The host may jumper E1 to include the 200W termination resistor located on its differential input side of the receiver when the application warrants it. (see Figure 2-4).

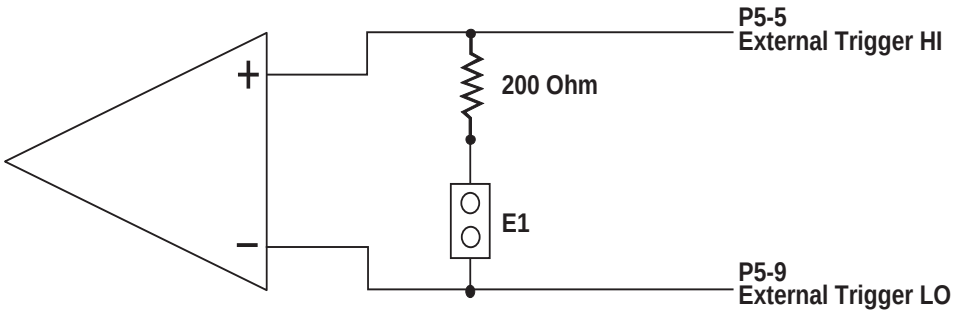


Figure 2-4 RS-422 Termination Resistor

Calibration

Auto-Calibration

The VMIVME-3123 features a host controlled auto-calibration. The calibration coefficients are stored in volatile memory on auto-calibration. Therefore, the host is required to initiate an auto-calibration after power-up. The VMIVME-3123's uncalibrated performance may only run approximately 1 percent. The host has the option of performing calibration, reading the coefficients from the VMIVME-3123 board, and storing them in nonvolatile memory of its own. The host can then load the coefficients into the proper locations on the VMIVME-3123 in lieu of performing an auto-calibration.

Built-In-Test (BIT) Reference Voltage Calibration Procedure

1. Attach the voltmeter's positive lead to TP2 and negative lead to TP1 (see Figure 2-1 on page 38 for location of test points and adjustment potentiometers).
2. Write hexadecimal value 0x4000 to the Analog Configuration register at offset address 0x0016.
3. Adjust potentiometer R18 for a reading of 9.980000 ± .000200 VDC.
4. Write hexadecimal value 0x6000 to the Analog Configuration register at offset address 0x0016.
5. Adjust potentiometer R9 for a reading of 4.990000 ± .000150 VDC.
6. Repeat steps 2 through 5 as many times as required for calibration accuracy.
7. Apply "Red GLPT Insulating Varnish" available from GC Electronics P / N 10-9002 (or equivalent) to potentiometers R18 and R9.

Connector Descriptions

Connector Functions

Electrical connections to the VMIVME-3123 Board are made through two 96-pin DIN connectors (P1 and P2), two 25-pin D-Subminiature connectors (P3 and P4), and one 9-pin D-Subminiature connector (P5). The P1 and P2 connectors attach the VMIVME-3123 Board to the VMEbus backplane, and contain power, address, data, control lines and all additional signals necessary to control VMEbus functions related to the board. Connectors P3 and P4 include the differential analog inputs for channels 0 thru 15. Connector P5 contains the external trigger and sample clock signals as well as the multi-board synchronization signals.

VMEbus Connectors, P1 and P2

The signal names and connectors are shown in Figure 2-6 on page 44 for the P1 connector, and Figure 2-7 on page 45 for the P2 connector.

Analog Input Connectors, P3 and P4

The signal names for connectors P3 and P4 are shown in Figure 2-8 on page 46 and Figure 2-9 on page 47. These are female 25-pin D-Subminiature connectors whose shells are connected via the board to the front panel allowing the user to continue the connection to the chassis if desired.

Connector P3 contains the analog input signals for channels 7 through 0 and connector P4 contains the analog input signals for channels 15 through 8.

It is recommended that all unused analog input channels be properly grounded. Proper grounding can be achieved by connecting HI to LO to Guard for each unused channel.

For some input signals, it may be necessary to connect the Guard pin to the LO pin. This is absolutely necessary for isolated input signal sources.

External Trigger and Sample Clock Connector, P5

The signal names and connector P5 are shown below. This connector is a female 9-pin D-Subminiature connector whose shell is connected via the board to the front panel allowing the user to continue the connection to the chassis.

P5 Pin Assignments	
Pin No.	**Signal**
5	External Trigger HI
9	External Trigger LO
4	*No Connect / Digital GND
8	External Sample CLK IN
3	Multi-Board Trigger
7	*No Connect / Digital GND
2	*No Connect / Digital GND
6	Multi-Board Sample CLK1
1	Multi-Board Sample CLK 0
Each of the signals is described on the following pages.	

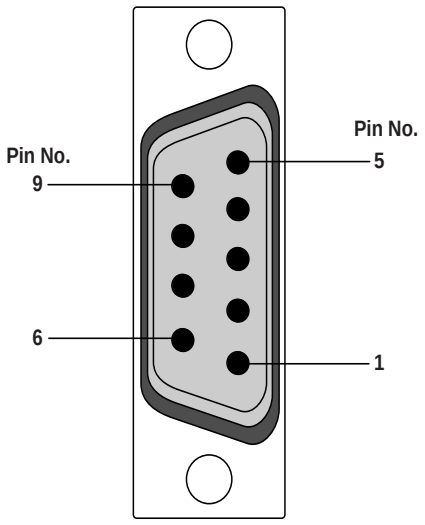


Figure 2-5 P5 Connector and Pinout

External Trigger HI (P5, Pin 5)
External Trigger LO (P5, Pin 9)

The External Trigger HI and LO signals are differential inputs to a RS-422 receiver that continues into the board's triggering circuitry. The user may connect the optional 200W termination resistor (See "RS-422 Termination Resistor" on page 40) if the application warrants it. The Trigger Configuration register's Bits 5 and 6 are used to select this trigger input if desired.

External Sample CLK In

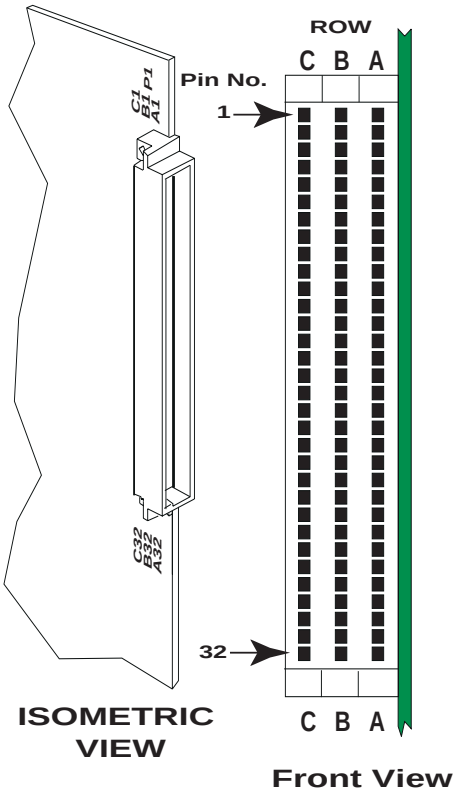
The External Sample CLK In signal is a TTL type input used to accept an external clocking source. The length of the connection from the external clocking source to the VMIVME-3123's P5 connector should be kept as short as possible. The Trigger Configuration Register's Bits 2, 1, and 0 are used to select this sample clock source if desired. The maximum clock frequency allowed is 200 kHz when channel doubling is selected. The effective sampling rate will be doubled by utilizing both edges of the clock.

Multi-Board Sample CLK 0 (P5, Pin 1)
Multi-Board Sample CLK 1 (P5, Pin 6)

The Multi-Board Sample CLK 0 and 1 are TTL level signals that should be bussed across all boards used in a multi-board configuration. The host will initialize the master board which will drive the signals as outputs. The host will also initialize the slave or slaves which will receive the signals as inputs.

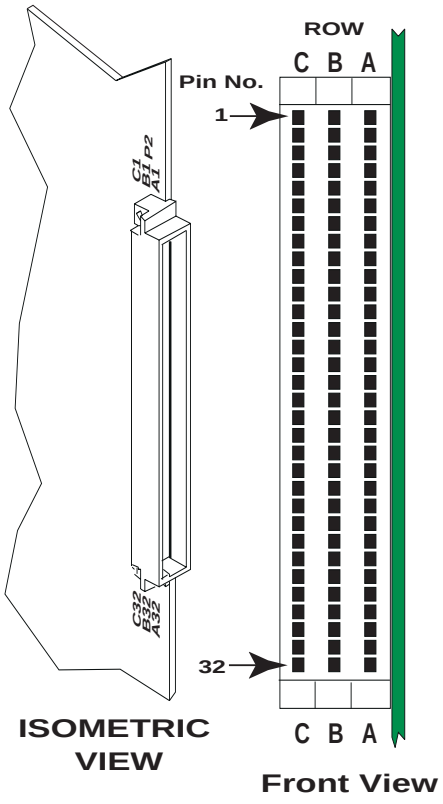
Multi-Board Trigger (P5, Pin3)

The Multi-Board Trigger is a TTL level signal that should be bussed across all boards used in a multi-board configuration. The host will initialize the master board which will drive the signal as an output. The host will also initialize the slaves which will receive the signal as an input.



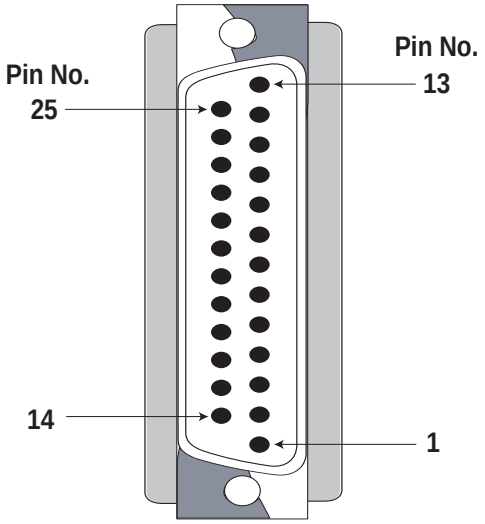
Pin No.	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 VDC	+5 STDBY	-12 VDC
32	+5 VDC	+5 VDC	+5 VDC

Figure 2-6 P1 Connector and Pinout



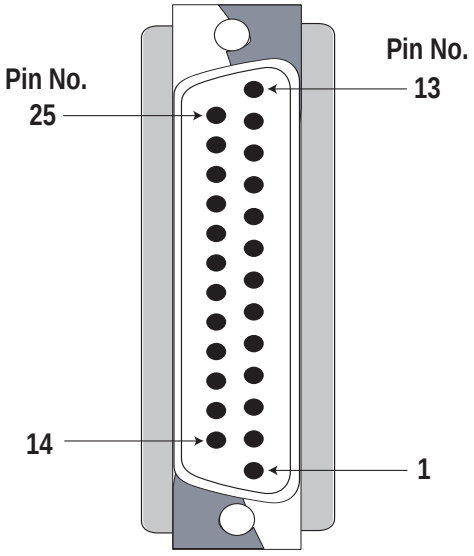
Pin No.	Row A	Row B	Row C
1	User Defined	+5 VDC	User Defined
2	.	GND	.
3	.	Reserved	.
4	.	A24	.
5	.	A25	.
6	.	A26	.
7	.	A27	.
8	.	A28	.
9	.	A29	.
10	.	A30	.
11	.	A31	.
12	.	GND	.
13	.	+5 VDC	.
14	.	D16	.
15	.	D17	.
16	User Defined	D18	User Defined
17	.	D19	.
18	.	D20	.
19	.	D21	.
20	.	D22	.
21	.	D23	.
22	.	GND	.
23	.	D24	.
24	.	D25	.
25	.	D26	.
26	.	D27	.
27	.	D28	.
28	.	D29	.
29	.	D30	.
30	.	D31	.
31	.	GND	.
32	User Defined	+5 VDC	User Defined

Figure 2-7 P2 Connector and Pinout



P3 Pin Assignments	
Pin NO.	Signal
13	Analog (GND)
25	Channel 7 LO
12	Channel 7 HI
24	Guard (GND)
11	Channel 6 LO
23	Channel 6 HI
10	Guard (GND)
22	Channel 5 LO
09	Channel 5 HI
21	Guard (GND)
08	Channel 4 LO
20	Channel 4 HI
07	Guard (GND)
19	Channel 3 LO
06	Channel 3 HI
18	Guard (GND)
05	Channel 2 LO
17	Channel 2 HI
04	Guard (GND)
16	Channel 1 LO
03	Channel 1 HI
15	Guard (GND)
02	Channel 0 LO
14	Channel 0 HI
01	Guard (GND)

Figure 2-8 P3 Connector and Pinout



P4 Pin Assignments	
Pin NO.	Signal
13	Analog (GND)
25	Channel 15 LO
12	Channel 15 HI
24	Guard (GND)
11	Channel 14 LO
23	Channel 14 HI
10	Guard (GND)
22	Channel 13 LO
09	Channel 13 HI
21	Guard (GND)
08	Channel 12 LO
20	Channel 12 HI
07	Guard (GND)
19	Channel 11 LO
06	Channel 11 HI
18	Guard (GND)
05	Channel 10 LO
17	Channel 10 HI
04	Guard (GND)
16	Channel 9 LO
03	Channel 9 HI
15	Guard (GND)
02	Channel 8 LO
14	Channel 8 HI
01	Guard (GND)

Figure 2-9 P4 Connector and Pinout

CHAPTER 3

Programming

Contents

Introduction

This section of the manual deals with the VMEbus software interface to the VMIVME-3123 board. Programming the VMIVME-3123 assumes a properly installed board accessed from an appropriate VMEbus system controller. Installation and hardware jumper configuration requirements are described in Chapter 2.

The VMIVME-3123 is physically addressed in two places within VMEbus addressing space: configuration, status and control activity takes place through the registers in A16 short I/O space, while the converted data is available through a much larger DRAM data buffer in A24 standard or A32 extended address space. The base address location for the control registers in A16 short I/O is programmed with hardware jumpers described in Chapter 2. The address, size and addressing mode of the data buffer, however, must be programmed via the short I/O registers. A bus interrupter is also available to generate interrupt requests, although interrupts are not necessary.

Software configuration is necessary before using the VMIVME-3123. After powerup or hardware reset, the VMIVME-3123 enters IDLE mode, without generating converted analog signal data but, making all registers and software control structures available. Host software can configure the board while IDLE, select the appropriate analog conversion mode, and begin reading data from the data buffer. If enabled, interrupts are handled via hardware registers without halting data conversion. Software returns the board to IDLE mode only to interact with various firmware registers, such as when re-configuring the board.

Register Descriptions

The VMIVME-3123 Configuration and Control registers occupy 256 bytes of VMEbus short I/O address space, although some of this space is unused. The register's base address and VMEbus access mode within short I/O space are set by hardware jumper fields described in Chapter 2.

Table 3-1 details the register map, including register names, sizes and access restrictions. Note that most registers are implemented by the board's firmware. Although hardware registers are always valid and available, firmware registers are only valid when the board's operating mode is set to IDLE (See Control/Status Register 0 for details on setting the operating mode). ***Unless the VMIVME-3123 operating mode is IDLE, any values written to or read from firmware registers are meaningless.***

Table 3-1 VMIVME-3123 Board Register Map

Short I/O Offset Address	Size	Access	Register Name	Type	Suggested Mnemonic
$0000	Word	Read-Only	Board Identification Register	Firmware	BID
$0002	Word	Read-Only	Firmware Revision Register	Firmware	REV
$0004	Word	Read/Write	Control/Status Register 0	Hardware	CSR0
$0006	Word	Read/Write	Control/Status Register 1	Hardware	CSR1
$0008	Word	Read/Write	Interrupt Vector Register	Hardware	IVR
$000A	Word	Read/Write	Trigger Configuration Register	Hardware	TRIG
$000C	Word	Read/Write	Trigger Delay Register	Firmware	TDEL
$000E	Word	Read/Write	Trigger Threshold Register	Firmware	TTHLD
$0010	Word	Read/Write	DSP Trigger Options/Buffer Configuration Register	Firmware	DTOBC
$0012	Word	Read/Write	Data Buffer Address Register	Firmware	DBAR
$0014	Word	Read/Write	Memory Configuration Register	Firmware	MCR
$0016	Word	Read/Write	Analog Configuration Register	Firmware	AC
$0018	Word	Read/Write	Analog Channel Enable Register	Firmware	CHEN
$001A	Word	Read/Write	Analog Conversion Rate Register	Firmware	RATE
$001C	Word	Read/Write	Test Select/Status Register	Firmware	TEST
$001E-$0020			Reserved		
$0022	Word	Read-Only	Error Register	Firmware	ERROR
$0024	Word	Read-Only	Buffer Start Address Register LSB	Firmware	BSARL
$0026	Word	Read-Only	Buffer Start Address Register MSB	Firmware	BSARM
$0028	Word	Read-Only	Buffer End Address Register LSB	Firmware	BEARL
$002A	Word	Read-Only	Buffer End Address Register MSB	Firmware	BEARM

Table 3-1 VMIVME-3123 Board Register Map (Continued)

Short I/O Offset Address	Size	Access	Register Name	Type	Suggested Mnemonic
$002C	Word	Read-Only	Trigger Address LSB	Firmware	TAL
$002E	Word	Read-Only	Trigger Address MSB	Firmware	TAM
$0030-$003E			Reserved		
$0040-$005E	Word(X16)	Read / Write	±10 V Gain Correction Factors (Channels 0-15)	Firmware	GCFHI00-GCFHI15
$0060-$007E	Word(X16)	Read / Write	±10 V Offset Correction Factors (Channels 0-15)	Firmware	OCFHI00-OCFHI15
$0080-$009E	Word(X16)	Read / Write	±5 V Gain Correction Factors (Channels 0-15)	Firmware	GCFLO00-GCFLO15
$00A0-$00BE	Word(X16)	Read / Write	±5 V Offset Correction Factors (Channels 0-15)	Firmware	OCFLO00-OCFLO15
$00C0-$00DE	Word(X16)	Read-Only	Analog Channel Errors Register	Firmware	AERR00-AERR15
$00E0-$00FE			Reserved		

NOTES: Short I/O Offset Addresses are offset relative to the base address defined by a jumper field. See Chapter 2 for jumper details. **Size** is the binary size of the register. Hardware registers can be read and written to as bytes or words. Firmware Registers can be only written to as a word. Byte writes to firmware registers will leave the register unchanged. Firmware registers can be read as a byte or word. **Access** indicates intended function only: most firmware "read-only" registers may actually be written, but any data written is volatile. **Type** describes how the register is implemented. Hardware registers are always available. Firmware registers are only valid in IDLE mode (see the Control / Status Register 0 for mode details). ***In any mode except IDLE mode, values written to or read from firmware registers are meaningless.*** **Reserved** bits and registers will read indeterminate values. If a bit marked Reserved must be written, it should always be cleared (binary 0).

Board Identification Register (BID)

The Board Identification Register is a read only firmware word at offset $0000. It contains the fixed value $3DXX, which uniquely identifies this product from other VMIC VMEbus boards. Like all Firmware registers, this register is only valid in IDLE mode. Table 3-2 details this register's bit map.

Table 3-2 Board ID Register Bit Map

Board ID Register (Offset $0000) Read-Only Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	1	1	1	0	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							

Power-up / Reset Default = $3DXX

Firmware Revision Register (REV)

The Firmware Revision Register is a read-only firmware word at offset $0002. It contains a single value which identifies the on-board firmware revision number. Like all firmware registers, this register is only valid in IDLE mode. Table 3-3 details the register's bit map.

Table 3-3 Firmware Revision Register Bit Map

Firmware Revision Register (Offset $0002) Read-Only Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Rev 7	Rev 6	Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							

Power-up / Reset Default = $RR00
RR = Revision

Control/Status Register 0 (CSR0)

Control / Status Register 0 is a read / write hardware word at offset $0004. It contains several flags and bit fields which indicate and control various overall aspects of board operation. Perhaps most importantly, this register controls the general operating mode of the entire board. Like all hardware registers, this register is always valid and available to the host. Table 3-4 details this register's bit map.

Table 3-4 Control/Status Register 0 Bit Map

Control/Status Register 0 (Offset $0004) Read/Write Hardware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
LED Off	Halt	Hardware Reset	Memory Enable	Board Not Ready	OpMode 2	OpMode 1	OpMode 0

Power-up / Reset Default = $XX00

Control/Status Register 0 Bit Definitions

Bit 07: **LED Off -** A logical "1" written to this bit location causes the front panel status LED to turn off. A logical "0" written to this bit location causes the front panel status LED to be turned on. (Default is logic "0").

Bit 06: **Halt -** A logical "1" written to this write-only bit stops data conversion and returns the board to IDLE mode. After issuing a halt, host software should poll the OpMode bits (described below) and wait until they are all clear (indicating IDLE mode) before proceeding. At that time, the Halt bit is also cleared. It should not take the board longer than 5 msec to return to IDLE mode after Halt is set. If a "1" is written to this bit when the board is in IDLE mode, the Halt bit will not be cleared.

Bit 05: **Hardware Reset -** A logical "1" written to this write-only bit performs a total hardware reset of the board. All power-up functions are performed, just as if the VMEbus SYSRESET had been toggled. After issuing a hardware reset, host software should poll the Board Not Ready bit (described below) to determine when the reset has completed. Reset should not take more than 5 msec.

Bit 04: **Memory Enable -** A logical "1" written to this bit location will enable the DRAM buffer to become available. A logical "0" written to this bit location causes the DRAM buffer to be disabled to host VMEbus accesses. When disabled, VMEbus accesses to the DRAM area will not DTACK*. Turning this bit on / off does not affect the DRAM address / data.

Bit 03: **Board Not Ready -** This is a read-only status bit which indicates the VMIVME-3123 is powered up and ready to respond to the host. A logical "1" indicates the board is not ready to respond to host accesses. After the on-board DSP has powered-up and initialized, it will clear this bit to a logic "0".

Control/Status Register 0 Bit Definitions (Continued)

Bits 02 through 00: **OpMode [2:0] -** Operating Mode control bits. Write a value to this field to place the VMIVME-3123 into the desired operating mode according to Table 3-5. Note that in any operating mode except IDLE, these mode bits are read-only, indicating the current mode. Refer to Operating Modes below for a more detailed discussion of the operating modes.

NOTE: All other applicable registers must be programmed prior to entering the desired operation mode.

Table 3-5 Operating Modes

Operating Mode and Number	OpMode2	OpMode1	OpMode0	Operating Mode and Number
IDLE	0	0	0	0
Transient Capture	1	0	0	1
Continuous Sample	2	0	1	0
Reserved	3	0	1	1
Calibration	4	1	0	0
Self-Test	5	1	0	1
Reserved	6	1	1	0
Reserved	7	1	1	1

Operating Mode Descriptions

IDLE (Mode 0) - IDLE mode is the power-up / reset default mode and is the only mode in which firmware registers can be accessed. IDLE mode is used by the host for configuration of the other registers prior to commanding the board to run in one of the functional modes. After completing a functional mode, hardware reset or halt, the board returns to IDLE mode without disturbing the other registers contents. Note that unlike the other modes, the user should never attempt to enter IDLE mode by writing to these mode bits. Use the Halt bit instead, and poll the mode bits. The mode bits will all be clear when IDLE mode is achieved.

Transient Capture (Mode 1) - Transient Capture mode is generally used to capture a transient event. In this mode, the board looks for a trigger marking an event (pre-programmed according to the Trigger Configuration Register and related registers), fills the DRAM sample buffer, and then returns to IDLE mode.

Continuous Sample (Mode 2) - Continuous Sampling mode is used when the host wants to collect a continuous stream of data. The data is stored in the DRAM buffer sequentially and the buffer rolls over when full (that is, the data buffer becomes a continuous ring buffer).

Calibration (Mode 4) - Calibration mode is used to generate the gain and offset correction values for the board. A board calibration is **NOT** performed on power-up. The user may perform calibration after power-up (from IDLE mode) or download pre-determined gain and offset values into DSP memory.

Self-Test (Mode 5) - Self-Test mode performs the selected tests in the Test Select / Status Register and stores the results in the status portion of the same register.

Reserved Modes (Modes 3, 6 & 7) - These modes are reserved for future expansion.

Control/Status Register 1(CSR1)

Control / Status Register 1 is a read / write hardware word at offset $0006. It contains several flags and bit fields which indicate and control various overall aspects of board operation, especially regarding interrupts and sample triggering. Like all hardware registers, this register is always valid and available to the host. Table 3-6 details this register's bit map.

Table 3-6 Control/Status Register 1 Bit Map

Control/Status Register 1 (Offset $0006) Read/Write, Hardware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Filling Upper Buffer	I / O Trigger	I / O Sample Clock	Interrupt B	Interrupt A	Interrupt Level 2	Interrupt Level 1	Interrupt Level 0

Power-up / Reset Default = $XX00

Control/Status Register 1 Bit Definitions

Bit 07: **Filling Upper Buffer** - This read only bit indicates which buffer is presently being filled. A logical "0" indicates the lower-half of the DRAM data buffer is being filled and a logical "1" indicates that the upper-half is being filled. This bit is meant to be used with Continuous Sample mode only.

Bit 06: **I/O Trigger -** A logical "1" written to this write only bit causes a trigger strobe to occur when the I / O Trigger source is selected in the Trigger Configuration register.

Bit 05: **I/O Sample CLK -** A logical "1" written to this write only bit creates a sample clock strobe to occur when the I / O Sample Clk source is selected in the Trigger Configuration Register.

Bit 04: **Interrupt B -** This read only bit is used to indicate when the DSP has filled the data buffer during Continuous Sample mode as well as other functions. An interrupt will be generated if enabled. If interrupts are disabled this bit can be used in a polling manner to determine when the data buffer is full. A read of CSR1 will clear this bit. The following lists the functions that generate a B interrupt:

a. Transient Capture Mode - data buffer full, mode completed

b. Continuous Sample Mode - data buffer is full

c. Calibration mode - Calibration completed, mode completed

d. Self-Test Mode - Self-Test complete, mode completed

Control/Status Register 1 Bit Definitions (Continued)

Bit 03: **Interrupt A -** This read only bit is used to indicate the following:

a. Transient Capture Mode - data buffer full, mode completed

b. Continuous Sample Mode - data buffer is **half-full**

c. Calibration Mode - Calibration completed, mode completed

d. Self-Test Mode - Self-Test complete, mode completed

As with interrupt B, this bit can be used to generate an interrupt or it can be polled by the host. A read of CSR1 will clear this bit.

Bits 02 through 00: **Interrupt Level -** Interrupt Level configuration bits. (Default is logic $000). This field is used to select the VMEbus interrupt request level as shown below:

Table 3-7 VMEbus Interrupt Request Levels

VMEbus Interrupt Level	Interrupt Level 2	Interrupt Level 1	Interrupt Level 0
Disable Interrupts	0	0	0
IRQ 1	0	0	1
IRQ 2	0	1	0
IRQ 3	0	1	1
IRQ 4	1	0	0
IRQ 5	1	0	1
IRQ 6	1	1	0
IRQ 7	1	1	1

Interrupt Vector Register (IVR)

Table 3-8 Interrupt Vector Register Bit Map

Interrupt Vector Register (Offset $0008) Read/Write Hardware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
IVECT 7	IVECT 6	IVECT 5	IVECT 4	IVECT 3	IVECT 2	IVECT 1	IVECT 0

Power-up / Reset Default = $XX00

Interrupt Vector Register Bit Definitions

Bits 07 through 00: **IVECT [7:0] -** Interrupt Vector (Status / ID). (Default is $XX00). Contents of this Interrupt Vector register are supplied as a data byte (D07 through D00) on the data bus during the board's Interrupt Acknowledge cycles. The function of the Interrupt Vector is determined by the system user.

Trigger Configuration Register (TRIG)

Table 3-9 Trigger Configuration Register Bit Map

Trigger Configuration Register (Offset $000A) Read/Write, Hardware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Watchdog Timer Flag	Trigger Select 1	Trigger Select 0	Master	Multi-Board	Sample Clock Select 2	Sample Clock Select 1	Sample Clock Select 0

Power-up / Reset Default = $XX00

Trigger Configuration Register Bit Definitions

Bit 07: **Watchdog Timer Flag** - A logical "1" in this read only bit indicates that a hardware reset due to a watchdog timer time-out occurred. A power-up or hardware reset will clear this bit.

Bits 06 and 05: **Trigger Select [1:0] -** The Trigger Select bits choose the desired source for the triggering functioning to be used in the Transient Capture mode (see Table 3-10 on page 58).

Trigger Configuration Register Bit Definitions (Continued)

Table 3-10 Trigger Select

Mode	Trigger Select 1	Trigger Select 0
External Trigger	0	0
Inverted External Trigger	0	1
I/O Trigger	1	0
DSP Trigger	1	1

Bit 04: **Master -** This bit is used in configuring the trigger and sample clock hardware operations. The default setting is a logical "0" for slave mode which configures the hardware on this board to receive the triggers and sample clock from the master board thru the P5 connector. A logical "1" configures the hardware to drive the same signals out the P5 connector for use by slave boards. If the single/multi-board bit (Bit 03) is set to single board, this bit is a “don't care”.

Bit 03: **Multi Board -** A logical "0" written to this bit indicates the board is to be used in a stand-alone fashion. A logical "1" written to this bit indicates this board is to be used in a multi-board configuration. When set to a logical "1" the master/slave bit (Bit 04) should be set to the desired master/slave value. The default value for this bit is a logical "1" single board.

Bits 02 through 00: **Sample Clock Select [2:0] -** The Sample Clock Select bits choose the desired source to be used for sampling. Each rising edge of the selected source causes the following sequence of events:

a. Sample/hold circuits read/hold input value for sample n
b. A/D Converter serial port transmits last sample (n-1)
c. A/D Converter digitizes analog sample n
d. DSP performs data correction on sample n-1
e. DSP deposits, enabled channels data into DRAM buffer for sample n-1

This sequence of events is performed on all 16-channels on each rising edge. Each sample clock source can be configured to use the 2x channel doubling option except the I/O Sample Clock mode. Also, channel doubling is only available if a VMIVME-3123 board with 16-channels is being used. The channel doubling option will not operate with an 8-channel board. See Table 3-11 on page 59.

Table 3-11 Sample Clock Select

Sample Clock Mode	Sample Clock Select 2	Sample Clock Select 1	Sample Clock Select 0
Internal Timer	0	0	0
Internal Timer (2X,channel double)	0	0	1
I/O Sample Clock	0	1	0
N/A Do Not Use	0	1	1
External Sample Clock	1	0	0
External Sample Clock (2X, channel double)	1	0	1
Inverted External Sample Clock	1	1	0
Inverted External Sample Clock (2X, channel double)	1	1	1

Trigger Delay Register (TDEL)

Table 3-12 Trigger Delay Register Bit Map

Trigger Delay Register (Offset $000C) Read/Write, Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Delay 15	Delay 14	Delay 13	Delay 12	Delay 11	Delay 10	Delay 09	Delay 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Delay 07	Delay 06	Delay 05	Delay 04	Delay 03	Delay 02	Delay 01	Delay 00

Power-up/Reset Default = $0000

Trigger Delay Register Bit Definitions

Bits 15 through 00:

Delay [15:0] - The Trigger Delay register is used in Transient Capture mode only to insert sample delays from the trigger event. This register is active at all times during Transient Capture mode and has a default value of $0000 which produces no delay. When programmed to a non zero value, this register instructs the firmware to delay the trigger event by the value in this register. Valid values range from 0 to $FFFF ($2^{16}$-1).

Trigger Threshold Register (TTHLD)

Table 3-13 Trigger Threshold Register Bit Map

Trigger Threshold Register (Offset $000E) Read/Write, Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
TTHLD 15	TTHLD 14	TTHLD 13	TTHLD 12	TTHLD 11	TTHLD 10	TTHLD 09	TTHLD 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TTHLD 07	TTHLD 06	TTHLD 05	TTHLD 04	TTHLD 03	TTHLD 02	TTHLD 01	TTHLD 00

Power-up / Reset Default = $0000

Trigger Threshold Register Bit Definitions

Bits 15 through 00: **TTHLD[15:0]** - The Trigger Threshold register is only used in the Transient Capture mode when the DSP trigger is chosen. The DSP trigger option involves using the DSP firmware to compare a pre-selected analog input channel with the threshold value contained in this register. If the threshold value is exceeded, the firmware will recognize a trigger occurred and complete the capture of the signals and return to IDLE mode. The user must pre-program the threshold, trigger position, trigger slope and the trigger channel prior to entering Transient Capture mode when using the DSP trigger. This value is always a two's complement value.

DSP Trigger Options/Buffer Configuration Register (DTOBC)

Table 3-14 DSP Trigger Options/Buffer Configuration Register Bit Map

DSP Trigger Options/Buffer Conf Register (Offset $0010) Read/Write Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Trig Ch Sel 3	Trig Ch Sel 2	Trig Ch Sel 1	Trig Ch Sel 0	Reserved	Slope	Trigger Position 1	Trigger Position 0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved			Buffer Size 4	Buffer Size 3	Buffer Size 2	Buffer Size 1	Buffer Size 0

Power-up / Reset Default = $0017(8 Mbyte memory option)
= $0015 (2 Mbyte memory option)

DSP Trigger Options/Buffer Configuration Register Bit Definitions

Bits 15 through 12: **Trig Ch Sel [3:0]** - The Trigger Channel Select bits are set by the host to indicate which analog input channel is to be monitored when using the DSP trigger option in Transient Capture mode.

Bit 10: **Slope** - The Slope bit is used to indicate whether a DSP trigger should be acknowledged when the analog input channel being monitored (selected using the TRIG CH SEL bits) either exceeds or drops below the threshold value stored in the Trigger Threshold register. A logic "0" indicates a trigger will be produced when the analog input value drops below the threshold value (zero = negative slope), and a logic "1" indicates a trigger will be produced when the analog input value exceeds the threshold value (one = positive slope).

Bits 09 through 08: **Trigger Position [1:0]** - The Trigger Position bits indicate where in the data buffer the trigger will occur when using Transient Capture mode. The Trigger Position bits are valid for all trigger options. The bit definitions are shown in Table 3-15.

The post-trigger position implies that the analog input data is to be collected after a valid trigger event has occurred. The pretriggering position implies that the analog input data is to be collected prior to a valid triggering event. The mid-trigger position implies that the analog input data is to be collected both before and after a valid trigger event with the trigger occurring in the middle of the data stream.

Table 3-15 Trigger Positions

Trigger Positions	Trigger Position 1	Trigger Position 0
Will default to pre-trigger	1	1
Post-Trigger	1	0
Mid-Trigger	0	1
Pre-Trigger	0	0

Bits 04 through 00: **Buffer Size [4:0]** - The Buffer Size bits determine the size of the DRAM data buffer that will be filled with data.

Data Buffer Address Register (DBAR)

Table 3-16 Data Buffer Address Register Bit Map

Data Buffer Address Register (Offset $0012) Read/Write Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
A31	A30	A29	A28	A27	A26	A25	A24

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
A23	A22	A21	Reserved	Reserved	Access Mode 1	Access Mode 0	Extended Address

Powerup / Reset Default = $0000

Data Buffer Address Register Bit Definitions

Bits 15 through 08: **A[31:24] -** These address bits are used to select the board's DRAM data buffer address offset when the VMEbus extended addressing option is chosen.

Bit 07: **A23 -** This address bit is used in selecting the board's DRAM data buffer address offset in VMEbus extended and standard address space. This bit is used with both the 8 and 2 Mbyte DRAM options. When using the 2 Mbyte DRAM option, the A[22:21] bits described below need to be initialized as well.

Bits 06 through 04: **A[22:21] -** These address bits are used in selecting the board's DRAM data buffer address offset when the 2 Mbyte (1 Mbyte sample) option is chosen for the DRAM data buffer. These bits are a "don't care" on 8 Mbyte (4 Mbyte sample) boards.

Bits 02 and 01: **Access Mode[1:0] -** The Access Mode bits select the desired VMEbus access mode for use with the DRAM buffer. The access modes are shown in Table 3-17.

Table 3-17 Data Buffer Address Register Access Modes

VMEbus Access Mode	Access Mode 1	Access Mode 0
Both	1	1
Supervisory	0	1
Nonprivileged	1	0
Both (Default)	0	0

Bit 00: **Extended Address -** This bit is used to select either extended or standard addressing modes for the DRAM buffer. A logical "0", the default value, selects standard addressing, and a logical "1" selects the extended addressing mode.

Memory Configuration Register (MCR)

Table 3-18 Memory Configuration Register Bit Map

Memory Configuration Register (Offset $0014) Read Only Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved						Memory Config 1	Memory Config 0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CAL Settling DEL 7	CAL Settling DEL 6	CAL Settling DEL 5	CAL Settling DEL 4	CAL Settling DEL 3	CAL Settling DEL 2	CAL Settling DEL 1	CAL Settling DEL 0

Power-up / Reset Default = $02A0 - 8 Mbyte, $01A0 - 2 Mbyte

Memory Configuration Register Bit Definitions

Bits 09 and 08: **Memory Config[1:0]** - The Memory Configuration bits are read only bits indicating the DRAM size loaded on the board. These bits are derived from the presence detect signals located on the DRAM SIMM modules. See Table 3-19 for Memory Configuration.

Table 3-19 Memory Configuration

Configuration 1	Configuration 0	Size
1	1	Reserved
1	0	8 Mbyte
0	1	Reserved
0	0	2 Mbyte

Bits 07 through 00: **CAL Settling Delay[7:0]** - The Cal Settling Delay bits are read / write bits used to vary the amount of time elapsed between data gathering for the different reference points. This allows the user to increase the settling time if desired or to shorten the settling time thus shorting the calibration time as well. This time period associated with each bit weight is 10 milliseconds. There are six switches in reference voltage, the total calibration time is listed as follows:

Total Calibration Time = Cal Settling Delay value x 10 ms x 6

The default value of hex “A0” gives an individual settling time of 1.6 seconds between voltage switches with a total calibration time of approximately 9 to 10 seconds.

Analog Configuration Register (AC)

Table 3-20 Analog Configuration Register Bit Map

Analog Configuration Register (Offset $0016) Read/Write Firmware, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved	Enable BIT	BIT Voltage Select A2	BIT Voltage Select A1	BIT Voltage Select A0	Reserved	Eight Channels	Data Format

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Range 7 CH 7 & 15	Range 6 CH 6 & 14	Range 5 CH 5 & 13	Range 4 CH 4 & 12	Range 3 CH 3 & 11	Range 2 CH 2 & 10	Range 1 CH 1 & 9	Range 0 CH 0 & 8

Power-up / Reset Default = $0000 - 16 CH, = $0200 - 8 CH

Analog Configuration Register Bit Definitions

Bit 14: **Enable BIT** - This read / write bit must be set to allow the selected Built-In-Test, or BIT voltage to be applied to the ADC inputs. A logic "0" connects the field inputs from the front panel connector to the ADC, and a logic "1" connects the BIT voltage generation circuitry. The user should use the BIT voltage select bits below in choosing the particular voltage desired.

Bits 13 through 11: **BIT Voltage Select [A2:A0]** - The value in this bit field determines the BIT voltage stimulus to the ADC according to Table 3-21.

Table 3-21 BIT Voltage Select

A2	A1	A0	Voltage	Range
0	0	0	+9.98 VDC	10 V
0	0	1	0 VDC	10 V
0	1	0	-9.98 VDC	10 V
0	1	1	0 VDC	10 V
1	0	0	+4.99 VDC	5 V
1	0	1	0 VDC	5 V
1	1	0	-4.99 VDC	5 V
1	1	1	0 VDC	5 V

Bit 09: **Eight Channel** - This read only bit indicates whether the board is configured for 8- or 16-channel operation. A logic "0" indicates that the board contains a full 16 analog input channels and a logic "1" indicates that the board contains only 8 analog input channels.

Bit 08: **Data Format** - The Data Format bit selects the format the converted data will appear as in the DRAM buffer. If the bit is a logic "0," the data will appear as binary two's complement. If the bit is a logic "1," the data will appear as offset binary. The default value is binary two's complement data.

Analog Configuration Register Bit Definitions (Continued)

Bits 07 through 00: **Range [7:0]** - The Range bits select the analog input voltage range for a pair of analog input channels. Channels are paired together per the bit definitions above to accommodate the 2x sampling option which uses the input channels in pairs. A logic "1" sets the channel pair to the ±5 V range. A logical “0” sets the channel pair to the ±10 V range.

Analog Channel Enable Register (CHEN)

Table 3-22 Analog Channel Enable Register Bit Map

Analog Channel Enable Register (Offset $00018) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Ch En 15	Ch En 14	Ch En 13	Ch En 12	Ch En 11	Ch En 10	Ch En 09	Ch En 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Ch En 07	Ch En 06	Ch En 05	Ch En 04	Ch En 03	Ch En 02	Ch En 01	Ch En 00

Power-up / Reset Default = $FFFF or $00FF

Analog Channel Enable Register Bit Definitions

Bits 15 through 00: **Ch En [15:0] -** The Analog Channel Enable bits are used to select which individual analog input channels will be digitized and stored in the DRAM buffer. The board will process and deposit sequentially into the buffer memory the channels selected, beginning with channel 0, and progressing upward until the last enabled channel is reached. The user may choose to enable channels in quantities of 16, 8, 4, 2 or 1. If the 8-channel board is used, only quantities of 8, 4, 2 or 1 can be enabled. For example, the user may want to enable four channels and choose channels 1, 4, 7 and 14.

Analog Conversion Rate Register (RATE)

Table 3-23 Analog Conversion Rate Register Bit Map

Analog Conversion Rate Register (Offset $001A) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	Rate 14	Rate 13	Rate 12	Rate 11	Rate 10	Rate 09	Rate 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Rate 07	Rate 06	Rate 05	Rate 04	Rate 03	Rate 02	Rate 01	Rate 00

Power-up / Reset Default = $007C

Analog Conversion Rate Register Bit Definitions

Bits 14 through 00: **Rate [14:0]** - The Analog Conversion Rate register is an internal timer on the board which can be selected by the sample clock select bits of the Trigger Configuration register. The timer will provide the sample rate chosen for use by the ADC circuitry. The sample rate can be determined by the equation:

Sample Rate = (12.5 MHz / rate[] + 1)

(for $007C <= rate [] <= $7FFF) 1x clock select option

*(for $003F <= rate [] <= $7FFF) - 2x clock select option

* Sample Clock Select bits equal to "001"

Example 1: Set sampling rate to be 80 kHz

Rate [] + 1 = 12.5 MHz / sampling rate

Rate [] + 1 = (12.5E6 / 80E3)

Rate [] + 1 = 156.25 decimal = $009C

Rate [] = $009B

The user should load $009B into the Analog Conversion Rate Register.

Example 2: Set sampling rate at 200 kHz per channel using a 16 channel board with channels 0 and 8, 1 and 9, 2 and 10, etc., connected together at the field inputs. The sample clock select bits of the Trigger Configuration Register should be set to a logic "001", selecting internal timer, 2x option. The internal timer will be set to the following value as shown below:

Rate[] + 1 = 12.5 MHz / 200 kHz

Rate[] + 1 = 12.5 E6 / 200 E3

Rate[] + 1 = 62.5 (decimal) = 63 decimal (rounded) = $003F

Rate[] = $003F

The user should load $003F into the Analog Conversion register

The internal timer will be running at 198,412.6 Hz. The timer will then be run through a phase splitter which generates a 99,206.3 Hz clock, opposite phase to channel pairs 0 and 8, 1 and 9, etc., which will give an effective sampling rate of 198,412.6 Hz for each of the 2x channels.

Test Select/Status Register (TEST)

See “Operating Modes”, Self-Test (Mode 5) for more information.

Table 3-24 Test Select/Status Register Bit Map

Test Select/Status Register (Offset $001C) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
DO CAL	COEF Test	BIT Volt Test	DRAM ADDR Test	DRAM Pat Test	Reserved		

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CAL Done	COEF Test Pass	BIT Volt Test Passed	DRAM ADDR Test Passed	DRAM Pat Test Passed	Reserved		

Test Select/Status Register Bit Definitions

Bits 15 and 07: **DO CAL and CAL Done** - Setting Bit 15 instructs the VMIVME-3123 to perform calibration. After calibrating the board, firmware sets Bit 07 to a logical "1", indicating that calibration was performed.

Bits 14 and 06: **COEF Test and COEF Test Passed** - Setting Bit 14 instructs the VMIVME-3123 to check the gain and offset correction values for both the 10 V and 5 V ranges. The firmware compares the values against a pre-determined limit and sets a bit in the corresponding channel's analog error register. Bit 06 is set to a logical "1" if this test passes, and remains a logical "0" if the test fails.

Bits 13 and 05: **BIT Volt Test and BIT Volt Test Passed** - Setting Bit 13 instructs the VMIVME-3123 to use the BIT voltage reference to verify the analog input channels. The firmware inputs the +9.98 VDC, -9.98 VDC, +4.99 VDC, -4.99 VDC, and GND signals, reads the converted values, and verifies that the values meet a pre-determined tolerance. A bit is set in the corresponding channel's analog error register if an error occurs. Bit 05 is set to a logical "1" if this test passes, and remains a logical "0" if the test fails.

Bits 12 and 04: **DRAM ADDR Test and DRAM ADDR Test Passed** - Setting Bit 12 instructs the firmware to perform an address test of the DRAM buffer. The test writes a pseudo-random number pattern to the DRAM that is read and checked, then sets Bit 04 to a logical "1" if the test passed, and remains a logical "0" if the test fails.

Bits 11 and 03: **DRAM Pat Test and DRAM Pat Test Passed** - Setting Bit 12 instructs the firmware to perform a pattern test of the DRAM buffer. The test fills memory with four different patterns and verifies the data after each fill. The firmware sets Bit 03 to a logical "1" if the test passes, and remains a logical "0" if the test fails.

Error Register (ERROR)

The Error Register is an aid to the user indicating various configuration or programming errors. The bits relating to programming errors are cleared as a mode is entered and set prior to exiting the mode. The firmware will exit a mode and return to IDLE mode if a programming error occurs.

Table 3-25 Error Register Bit Map

Error Register (Offset $0022) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved		CS Invalid Buf Cfg	CS Wrong # of Ch	Reserved	TC Invalid Buf Cfg2	TC Invalid Buf Cfg1	TC Wrong # of Ch

Power-up / Reset Default = $0000

Error Register Bit Definitions

Bit 05: **CS Invalid Buf Cfg** - This bit indicates that an invalid buffer configuration programming error occurred when using the Continuous Sample mode. If this bit is set, either the buffer size bits in the DSP Trigger Options / Buffer Configuration register or the bits in the Analog Channel Enable register are programmed incorrectly.

Bit 04: **CS Wrong # of Ch** - This bit indicates an invalid number of channels were enabled in the Analog Channel Enable register, when using the Continuous Sample mode. Valid quantities of enabled channels include 16, 8, 4, 2 and 1 when using a 16 channel board and 8, 4, 2 and 1 when using an 8 channel board.

Bit 02: **TC Invalid Buf Cfg 2** - This bit indicates an invalid buffer configuration programming error when using the Transient Capture mode. Transient Capture mode requires the buffer to be configured for at least 2 sample periods worth of data. If the buffer is configured for only one sample period (row), this bit will be set. This restriction involves the pre-, mid-, and post-triggering circuitry and does not apply to Continuous Sample mode.

Bit 01: **TC Invalid Buf Cfg1** - Same as Bit 5 of this register except it applies to Transient Capture mode.

Bit 00: **TC Wrong # of Ch** - Same as Bit 4 of this register except it applies to Transient Capture mode.

Buffer Start Address Registers (MSB and LSB)

The Buffer Start Address registers (MSB and LSB) are combined to form a single 23-bit address indicating where the data buffer starts when using Transient Capture mode. The location pointed to by these registers will contain the first sample of the buffer. These registers are used with Transient Capture mode only and will normally be a nonzero value since the board has to collect data prior to the store trigger event, thus making it necessary to implement the DRAM buffer as a continuous ring buffer.

Table 3-26 Buffer Start Address Register MSB Bit Map

Buffer Start Address Register MSB (Offset $0026) Read Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	Start AD 22	Start AD 21	Start AD 20	Start AD 19	Start AD 18	Start AD 17	Start AD16

X = Don't Care. Power-up / Reset Default = $0000

Buffer Start Address Register MSB Bit Definitions

Bits 06 through 00: **ST AD [22:16] -** Buffer Start Address. These bits are the upper 7 bits of the DRAM buffer starting address.

Table 3-27 Buffer Start Address Register LSB Bit Map

Buffer Start Address Register LSB (Offset $0024) Read Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Start AD 15	Start AD 14	Start AD 13	Start AD 12	Start AD 11	Start AD 10	Start AD 09	Start AD 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Start AD 07	Start AD 06	Start AD 05	Start AD 04	Start AD 03	Start AD 02	Start AD 01	Start AD 00

Power-up / Reset Default = $0000

Buffer Start Address Register LSB Bit Definition

Bits 15 through 00: **Start AD [15:0] -** Buffer Start Address bits. These bits are the lower 16 bits of the DRAM buffer starting address as described in the BSARL bit definition.

Buffer End Address Registers (MSB and LSB)

The Buffer End Pointer Address registers (MSB and LSB) are combined to form a single 23-bit address indicating where the data buffer ends when using Transient Capture mode. The location pointed to by these registers will contain the first sample at the end of the buffer. These registers are used with Transient Capture mode only and will normally be a nonzero value since the board has to collect data prior to the store trigger event, thus making it necessary to implement the DRAM buffer as a continuous ring buffer.

Table 3-28 Buffer End Address Register MSB Bit Map

Buffer End Address MSB (Offset $002A) Read-Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	End AD 22	End AD 21	End AD 20	End AD 19	End AD 18	End AD 17	End AD 16

X = Don't Care. Power-up / Reset Default = $0000

Buffer End Address Register MSB Bit Definitions

Bits 06 through 00: **END AD [22:16] -** Buffer End Address. These bits are the upper 7 bits of the ending DRAM buffer address.

Table 3-29 Buffer End Address Register LSB Bit Map

Buffer End Address Register LSB (Offset $0028) Read-Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
End AD 15	End AD 14	End AD 13	End AD 12	End AD 11	End AD 10	End AD 09	End AD 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
End AD 07	End AD 06	End AD 05	End AD 04	End AD 03	End AD 02	End AD 01	End AD 00

Power-up / Reset Default = $0000

Buffer End Address Register LSB Bit Definitions

Bits 15 through 00: **End AD [15:0] -** Buffer End Address. These bits are the lower 16 bits of the ending DRAM buffer address.

Trigger Address Registers (MSB and LSB)

The Trigger Address registers (MSB and LSB) are combined to form a single 23-bit address indicating where the trigger occurred when using Transient Capture mode. The location pointed to by these registers will contain the first sample at the end of the buffer. These registers are used with Transient Capture mode only and will normally be a nonzero value since the board has to collect data prior to the store trigger event thus, making it necessary to implement the DRAM buffer as a continuous ring buffer.

Table 3-30 Trigger Address MSB Bit Map

Trigger Address MSB (Offset $002E) Read-Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	Trigger AD 22	Trigger AD 21	Trigger AD 20	Trigger AD 19	Trigger AD 18	Trigger AD 17	Trigger AD 16

X = Don't Care. Power-up / Reset Default = $0000

Trigger Address MSB Bit Definitions

Bits 06 through 00: **Trigger AD [22:16] -** Trigger Address bits. These bits are the upper 7 bits of the DRAM buffer trigger address.

Table 3-31 Trigger Address LSB Bit Map

Tr1gger Address LSB (Offset $002C) Read-Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Trigger AD 15	Trigger AD 14	Trigger AD 13	Trigger AD 12	Trigger AD 11	Trigger AD 10	Trigger AD 09	Trigger AD 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Trigger AD 07	Trigger AD 06	Trigger AD 05	Trigger AD 04	Trigger AD 03	Trigger AD 02	Trigger AD 01	Trigger AD 00

Power-up / Reset Default = $0000

Trigger Address LSB Bit Definitions

Bits 15 through 00: **Trigger AD [15:0] -** Trigger Address bits. These bits are the lower 16 bits of the DRAM buffer trigger address.

Gain & Offset Correction Factors (Channels 0-15)

The following bit definitions correspond to the gain and offset coefficients for the ±10 and ±5 V analog input ranges. There will be 16 values (sixteen 16-bit values, one for each channel) for each correction factor in each voltage range. These values are calculated by the DSP when calibration is run. You have the ability to generate your own correction factors using the BIT voltages or precision voltages you choose through the field inputs, and placing them in these locations for use by the board.

Table 3-32 ±10 V Gain Correction Factors CH 0 through 15 Bit Map

±10 V Gain Correction Factors CH 0 through 15 (Offset $0040-$005E) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
10 V Gain Cor 15	10 V Gain Cor 14	10 V Gain Cor 13	10 V Gain Cor 12	10 V Gain Cor 11	10 V Gain Cor 10	10 V Gain Cor 9	10 V Gain Cor 8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
10 V Gain Cor 7	10 V Gain Cor 6	10 V Gain Cor 5	10 V Gain Cor 4	10 V Gain Cor 3	10 V Gain Cor 2	10 V Gain Cor 1	10 V Gain Cor 0

Power-up / Reset Default = $0000

±10 V Gain Correction Factors CH 0 through 15 Bit Definitions

Bits 15 through 00: **±10 V Gain Cor [15:0]** - The ±10 V gain correction values are 16-bit values used in the data correction process when the ±10 V range is selected. There are 16 correction values beginning at location XX40, one for each channel. Address XX40 contains the correction value for channel 0, XX42 contains the value for channel 1, and so on.

Table 3-33 ±10 V Offset Correction Factors CH 0 through 15 Bit Map

±10 V Offset Correction Factors CH 0 through 15 (Offset $0060-$007E) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
10 V Offset Cor 15	10 V Offset Cor 14	10 V Offset Cor 13	10 V Offset Cor 12	10 V Offset Cor 11	10 V Offset Cor 10	10 V Offset Cor 9	10 V Offset Cor 8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
10 V Offset Cor 7	10 V Offset Cor 6	10 V Offset Cor 5	10 V Offset Cor 4	10 V Offset Cor 3	10 V Offset Cor 2	10 V Offset Cor 1	10 V Offset Cor 0

Power-up / Reset Default = $0000

±10 V Offset Correction Factors CH 0-15 Bit Definitions

Bits 15 through 00: **±10 V Offset Cor [15:0]** - The ±10 V offset correction values are 16-bit values used in the data correction process when the ±10 V range is selected. There are 16 correction values beginning at location XX60, one for each channel. Address XX60 contains the correction value for channel 0, XX62 contains the value for channel 1, and so on.

Table 3-34 ±5 V Gain Correction Factors CH 0-15 Bit Map

±5 V Gain Correction Factors CH 0 through 15 (Offset $0080-$009E) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
5 V Gain Cor 15	5 V Gain Cor 14	5 V Gain Cor 13	5 V Gain Cor 12	5 V Gain Cor 11	5 V Gain Cor 10	5 V Gain Cor 9	5 V Gain Cor 8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
5 V Gain Cor 7	5 V Gain Cor 6	5 V Gain Cor 5	5 V Gain Cor 4	5 V Gain Cor 3	5 V Gain Cor 2	5 V Gain Cor 1	5 V Gain Cor 0

Power-up / Reset Default = $0000

±5 V Gain Correction Factors CH 0 through 15 Bit Definitions

Bits 15 through 00: **±5 V Gain Cor [15:0]** - The ±5 V gain correction values are 16-bit values used in the data correction process when the ±5 V range is selected. There are 16 correction values beginning at location XX80, one for each channel. Address XX80 contains the correction value for channel 0, XX82 contains the value for channel 1, and so on.

Table 3-35 ±5 V Offset Correction Factors CH 0-15 Bit Map

±5 V Offset Correction Factors CH 0 through 15 (Offset $00A0-$00BE) Read/Write, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
5 V Offset Cor 15	5 V Offset Cor 14	5 V Offset Cor 13	5 V Offset Cor 12	5 V Offset Cor 11	5 V Offset Cor 10	5 V Offset Cor 9	5 V Offset Cor 8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
5 V Offset Cor 7	5 V Offset Cor 6	5 V Offset Cor 5	5 V Offset Cor 4	5 V Offset Cor 3	5 V Offset Cor 2	5 V Offset Cor 1	5 V Offset Cor 0

Power-up / Reset Default = $0000

±5 V Offset Correction Factors Bit Definitions

Bits 15 through 00: **±5 V Offset Cor [15:0]** - The ±5 V offset correction values are 16-bit values used in the data correction process when the ±5 V range is selected. There are 16 correction values beginning at location XXA0, one for each channel. Address XXA0 contains the correction value for channel 0, XXA2 contains the value for channel 1, and so on.

Analog Channel Errors Register (Channels 0 through 15)

These registers are used to supplement the self-test information in the Self-Test Select / Status register. If an error occurs during one of the selected analog tests, a bit will be set in one of these registers according to the test and channel that failed. These registers can be used as an aid in isolating a channel dependent problem.
See Table 3-36 for bit definitions.

Table 3-36 Analog Channel Errors Register CH 0-15 Bit Map

Analog Channel Errors Register CH 0 through 15 (Offset $00C0-$00DE) Read Only, Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
10 V Gain	10 V Offset	5 V Gain	5 V Offset	10 V Range +9.98 V	10 V Range GND	10 V Range -9.98 V	Reserved

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
5 V Range +4.99 V	5 V Range GND	5 V Range -4.99 V	Reserved				Not Cal'ed

Power-up / Reset Default = $0001

Analog Channel Errors Register (CH 0 through 15) Bit Definitions

Bit 15: **10 V Gain** - Indicates channel's 10 V range gain coefficient does not meet the board's limits.

Bit 14: **10 V Offset** - Indicates channel's 10 V range offset coefficient does not meet the board's limits.

Bit 13: **5 V Gain** - Indicates channel's 5 V range gain coefficient does not meet the board's limits.

Bit 12: **5 V Offset** - Indicates channel's 5 V range offset coefficient does not meet the board's limits.

Bit 11: **10 V Range +9.98 V** - Indicates channel's 10 V range +9.98 VDC BIT voltage circuit is inaccurate or defective.

Bit 10: **10 V Range GND** - Indicates channel's 10 V range ±9.98 VDC ground circuit is inaccurate or defective.

Bit 09: **10 V Range -9.98 V** - Indicates channel's 10 V range -9.98 VDC BIT voltage circuit is inaccurate or defective.

Bit 07: **5 V Range +4.99 V** - Indicates channel's 5 V range +4.99 VDC BIT voltage circuit is inaccurate or defective.

Bit 06: **5 V Range GND** - Indicates channel's 5 V range ±4.99 VDC ground circuit is inaccurate or defective.

Bit 05: **5 V Range -4.99 V** - Indicates channel's 5 V range -4.99 VDC BIT voltage circuit is inaccurate or defective.

Bit 00: **Not Cal'ed** - Indicates that board has not had calibration run at this time. This bit is a logic "1" on powerup and is set to a logic "0" by the calibration routine.

Operating Modes

The VMIVME-3123 board contains three mode bits (Bits 2,1 and 0) located in the Control / Status Register 0 that indicate to the user the present mode of the board. The mode bits are read / write and can be read at any time, however, they can only be written to in the IDLE mode (bits are 000). The board powers up in IDLE mode and is ready for host commands once the board not ready bit (Bit 3 of the Control / Status Register 0) is set to a logic "0". At this time the host has access to all registers located in short I / O space and should initialize the registers according to the desired task. After initializing the registers, the host may place the board into the desired mode by writing the three mode bits.

A desired mode can only be entered by way of the IDLE mode. A non-IDLE mode can not be entered from another non-IDLE mode. Once the board is placed into a non-IDLE mode (nonzero mode), the three mode bits become read only. The board will remain in the chosen mode until the Halt bit is set, Hardware Reset bit is set, the board receives a system reset, or the board completes the task associated with the chosen mode (for example, completes calibration mode and returns to IDLE mode). If the Halt bit is set, the host should monitor the mode bits for indication that the board has returned to IDLE mode. The board will automatically return to IDLE mode after completion of Calibration mode, Transient Capture mode, Self-Test mode, and any programming error. The board must be halted whenever termination of Continuous Sample mode is desired.

The registers located in short I / O space consist of both hardware and firmware registers. Hardware registers are accessible by the host at all times, and are implemented with hardware logic, and do not require interaction with the on-board DSP. The firmware registers are accessible only during IDLE mode, are implemented using the DSP's internal memory, and require interaction with the on-board DSP. Non-IDLE mode firmware register accesses will result in a DTACK* from the board, but the data will be invalid. Table 3-5 on page 54 lists the operating modes which are described in more detail in the following sections.

IDLE (Mode 0) - See "Control / Status Register 0 (CSR0)" on page 53, *"IDLE (Mode 0)"*.

Transient Capture (Mode 1) - Transient Capture mode is generally used for capturing a transient event marked by the trigger source. After the host initializes the registers and enters this mode, the board's DSP uses the information in the registers to initialize the board and begins sampling the inputs and storing them sequentially in the DRAM buffer. The board also looks for the trigger event as it is sampling. When a trigger event occurs, the board completes filling the circular buffer in DRAM and returns to IDLE mode. After the buffer fills, the buffer flags are set and will generate interrupts if enabled. After the board has filled the circular buffer and the board is in IDLE mode, the buffer start, end, and trigger addresses can be read from the board's VMEbus short I / O registers and the sampled data read out of the DRAM buffer*****. The trigger circuitry allows the collection of pre-, mid-, or post trigger data. The host can use the halt bit in the Control / Status Register 0 to prematurely return the board to IDLE mode.

*****Actually, the DRAM contents can be read by the host during capture of the signals if desired, there is nothing preventing this. However, it is not

recommended to access the DRAM during sampling in order to mimimize the number of sources of noise to the sampling process.

NOTE: There is a 1.27 msec delay from the time the host places the board in the Transient Capture mode and the board is ready for the first sample. There will be a 700 µsec delay from the time this board completes transient capture or is given a halt command until the mode bits read a logic "000" indicating the board is in Idle mode.

Continuous Sample (Mode 2) - The Continuous Sample mode is similar to the Transient Capture mode in that data is collected and stored sequentially in the DRAM buffer. The same channel enable and buffer sizing operations apply, as well as the buffer half-full and full flags. The Continuous Sample mode does not use the triggering circuitry, but begins sampling data and storing it once the DSP has initialized itself. The buffer start, end and trigger address registers are not applicable to this mode because the buffer functions as a continuous ring buffer whose start address is always $000000. The buffer end address is based on the buffer size chosen by the host. Once the buffer fills up, it rolls over and begins writing data at address $000000 again. The host is required to read the data from the buffer before it rolls over or the data will be written over.

NOTE: There is a 1.27 msec delay from the time the host places the board in the Transient Capture mode and the board is ready for the first sample. There will be a 700 µsec delay from the time this board completes transient capture or is given a halt command until the mode bits read a logic "000" indicating the board is in Idle mode.

Calibration (Mode 4) - Calibration mode is used to generate the gain and offset correction values for the board. It is recommended that this calibration mode be exercised before converting analog data. Calibration is under host control and can be called at anytime after power-up while in IDLE mode. Calibration of the board can also be included while running the Self-Test mode by setting a bit in the Test Select / Status register. The host is required to command a calibration at each power-up or to store the calibration values in a host controlled nonvolatile memory and then write these values to the board at each power-up. An uncalibrated board can be expected to be accurate to approximately 1 percent. When calibration mode is called, the board's firmware disconnects the field inputs from the input channels and inserts three test voltages used in generating the data for the curve fitting routine. The calibration routine generates gain and offset correction values for both the ±10 V and ±5 V input ranges. These values are then stored in the gain and offset value registers located in the VMEbus short I / O space. When Calibration mode is complete, it sets both the interrupt A and interrupt B bits in the Control / Status Register 1, clears the Not Cal'ed bit in the Analog Channel Errors registers, and returns to IDLE mode. The user can prematurely exit the calibration mode by setting the halt bit in the Control / Status Register 0.

Self-Test (Mode 5) - Self-Test mode allows the host to instruct the board to perform a calibration and self check on itself. Different tests in the Test Select / Status register can be enabled and will be executed when Self-Test mode is entered. After the board completes executing the selected self tests, the host can

check the results in the status portion of the Test Select / Status register. A bit is included to allow the board to perform a calibration using the Self-Test mode. The host should always perform a calibration or set the D0 CAL bit in the Test Select / Status register prior to performing the check of the calibration values test. When Self-Test mode is complete, it sets both the interrupt A and B bits in the Control / Status Register 1 and returns to IDLE mode.

The user can prematurely exit the calibration mode by setting the halt bit in the Control / Status Register 0. The user should be aware that to run all the self tests will take up to 5 minutes depending on the memory option chosen. The following lists the routines included in the Self-Test and the relative length of time they take to execute:

a. Calibration - several seconds
b. Coefficient Test - several seconds
c. BIT Voltage Test - several seconds
d. DRAM Address Test - 1 minute
e. DRAM Pattern Test - 2 minutes

Data Buffer Operation

The VMIVME-3123 board uses 8 Mbytes of DRAM (2 Mbyte option available) to buffer the sampled data. The registers below are used to set up and control the data buffer:

Memory Configuration Register (MCR, $XX14) - Read only register containing the two memory configuration bits based on the amount of DRAM loaded on the board.

Control/Status Register 0 (CSR0, $XX04) - This register contains the memory enable bit which allows the host to read the sample data from the DRAM.

Data Buffer Address Register (DBAR, $XX12) - This register is used to set up the board's memory interface to the VMEbus.

DSP Trigger Options/Buffer Configuration Register (DTOBC, $XX10) - This register contains the buffer size bits that determine the actual amount of DRAM used for storage of the sampled data.

Analog Channel Enable Register (CHEN, $XX18) - This register contains the individual bits used to enable the individual analog channels.

The data buffer is used to store the sampled data and is located in the on-board DRAM. The data buffer can be as large as the available DRAM or down sized if the application warrants it. The data buffer size is determined by the buffer size bits (4..0) located in the DSP Trigger Options / Buffer Configuration Register. The buffer size bits correspond to the exponent n in the equation below:

Data buffer size (in bytes) = 2^n n = value of buffer size bits

Refer to Table 3-37 on page 80 for valid values of the buffer size bits. An invalid value will cause the board to set an invalid buffer configuration bit in the Error Register and return to IDLE mode.

The Channel Enable Register allows the host to enable any channels in totals of 1, 2, 4, 8 or 16. The board digitizes all the input channels but checks the channel enable bit for each channel to determine if the sample should be deposited into the DRAM. Enabled samples are loaded into DRAM sequentially, starting with channel 0 and moving up to channel 15. If an invalid quantity of channels are enabled, the board will set an invalid channel quantity bit in the Error Register and return to IDLE mode.

Figure 3-1 on page 79 shows how the data buffer is configured and loaded with sample data. The buffer size bits determine the actual size of the data buffer (in bytes). The quantity of enabled channels determines the number of columns in the array, and dividing the data buffer size by the number of enabled channels determines the number of rows (or number of sample periods). Remember to divide the data buffer size by two to change from units of bytes to data samples (16-bit data samples).

Sample data is loaded into the data buffer sequentially and will overwrite old data when the buffer is filled. The data buffer operates as a continuous ring buffer.

Data is deposited into the DRAM starting at location $0000 0000. Address $0000 0000 will always be the beginning address of the data buffer and the end address of the data buffer is determined by the buffer size bits. Note that the buffer start, end, and Trigger Pointer Address registers refer to the buffer in the operational sense relating to the storing of sampled data. These values are constantly changing as the circular buffer is operating, but data is physically being deposited from location $0000 0000 up to the address determined by the buffer size bits.

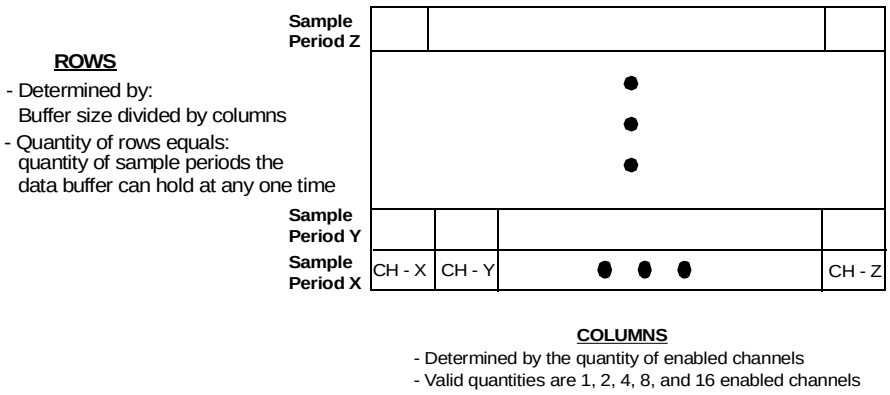


Figure 3-1 Data Buffer Array Configuration

The Buffer Start Address, Buffer End Address and Trigger Pointer Address registers are updated when the Transient Capture mode is run. These registers contain the address of the first sample of the particular row the register is pointing to. Figure 3-2 shows the registers pointing to the applicable portion of the buffer when the mid-trigger option is selected.

When the pre-trigger option is selected, the Trigger Pointer Address will be the same as the Buffer End Address indicating that the trigger data was the last sample stored and all other sampled data occurred prior to the trigger data. When the post-trigger option is selected, the Trigger Pointer Address will be the same as the Buffer Start Address indicating that the trigger data was the first sample stored in this buffer and all other sampled data occurred after the trigger data. The nature of pre- and mid-triggering requires the board to re-store samples and use a circular buffer whose start and end address move sequentially until the trigger occurs.

The Continuous Sample mode does not use the Buffer Start, End and Trigger Pointer Address registers because of the continuous nature of the mode. The Continuous Sample mode buffer start address is always at $000000 and the end address is at the end of the buffer, determined by the buffer size bits.

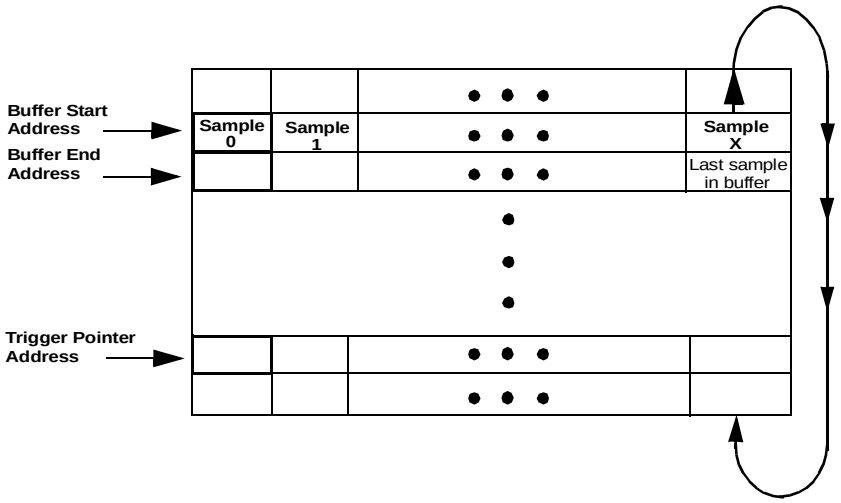


Figure 3-2 Data Buffer Pointers, Mid-Trigger Selected

Table 3-37 Buffer Size Values

Buffer Size 4..0	Exponent's Decimal Value	2^x	Buffer Size (In Bytes)	Total Number of Samples
11111 thru 11000	31 thru 24	**Do Not Use, Not Applicable, Will Set Bit in Error Register**		
10111	23	2^{23}	8388608 (8M)	4194304
10110	22	2^{22}	4194304 (4M)	2097152
10101	21	2^{21}	2097152 (2M)	1048576
10100	20	2^{20}	1048576 (1M)	524288
10011	19	2^{19}	524288 (512k)	262144
10010	18	2^{18}	262144 (256k)	131072
10001	17	2^{17}	131072 (128k)	65536
10000	16	2^{16}	65536 (64k)	32768
01111	15	2^{15}	32768 (32k)	16384
01110	14	2^{14}	16384 (16k)	8192
01101	13	2^{13}	8192 (8k)	4096
01100	12	2^{12}	4096 (4k)	2048
01011	11	2^{11}	2048 (2k)	1024
01010	10	2^{10}	1024 (1k)	512
01001	9	2^9	512	256
01000	8	2^8	256	128
00111	7	2^7	128	64
00110	6	2^6	64	32
00101	5	2^5	32	16
00100	4	2^4	16	8
00011	3	2^3	8	4
00010	2	2^2	4	2
00001	1	2^1	2	1
00000	0	**Do Not Use. Not Applicable, Will Set Bit in Error Register**		

NOTE: A buffer size of 00001 may be used with Continuous Sample mode, but can not be used with Transient Capture mode. Transient Capture mode requires a buffer size of at least 2

Power Up and Resets

The VMIVME-3123 board uses the VMEbus SYSRESET* signal and the Hardware Reset bit (Bit 5 of CSR0) to reset the board. When SYSRESET* is released, or the Hardware Reset bit is set, the Board Not Ready bit (Bit 3 of CSR0) will be set. This bit remains set while the board's DSP goes through the process of boot loading the DSP's firmware, and executing its initialization routine. At the conclusion of this process, the DSP clears the Board Not Ready bit (logic "0" indicating the board is ready) and enters IDLE mode. At this time the board is completely operational. The user should note that although the board is not completely operational during the boot up period, the hardware registers are always available to the host. The time required for boot up is approximately 1.7 msec. The board also contains a Halt-bit (Bit 6 in the CSR0) which allows the host to terminate a non-IDLE mode prematurely, if desired.

Triggers and Sample Clocks

The VMIVME-3123 board uses two types of host selectable signals in collecting data, a trigger and a sample clock. Both of these signals should be setup prior to entering the applicable non-IDLE mode of operation. The trigger signal is only used in the Transient Capture mode and is used to indicate when the data capture process should complete. The sample clock signal is used to generate the periodic timing necessary for repetitive sampling of the input channels.

Setting Multi-Board and Master Bits

NOTE: The host should program the Trigger Configuration registers Multi-board and Master bits prior to setting the other bits associated with this section (Control Hardware Buffer and Driver Enables).

The Multi-Board and Master bits located in the trigger Configuration register are used to control the hardware buffers and driver IC's used to interface the boards to trigger and sample clocks as well as board to board in a multi-board setup. The multi-board bit powers up at a default value of logic "0" indicating a single board operation. The Master bit is a "don't care" when the board operates as a single board. If the multi-board bit is set to a logic "1" indicating multi-board operation, the Master bit should be initialized to indicate whether the board is the only master generating the trigger and clock signals or one of the slaves receiving the trigger and clock signals.

Trigger Select

The actual trigger source is host selectable using the Trigger Configuration register's Trigger Select bits. The host can choose the external trigger accessible through connector P5, the VMEbus I/O trigger accessible by setting bit 6 (write only) of CSR1 to a logic "1", or the DSP trigger which monitors and triggers on a selected analog input channel. The external trigger is host selectable by way of the Trigger Select bits as either rising edge or falling edge. The DSP trigger slope bit located in the Trigger Option/Buffer Configuration register provides the same function for the DSP trigger. The DSP trigger also requires the user to select a channel to be monitored and a voltage threshold value. The channel used for triggering can be, but is not required to be, a channel enabled for sampling and is selected using the Trig Ch Sel [3:0] bits of the Trigger Options/Buffer Configuration register. The threshold value is a two's complement number placed in the Trigger Threshold register. The host can use the Trigger Delay register to delay the capture of the target waveforms. A value up to 64 K can be loaded into this register and the board will delay a corresponding number of samples before triggering.

The host must choose the position in the buffer they would like the trigger to appear by setting the Trigger Position bits (Bits 1 and 0) of the Trigger Option register. Sample data can be viewed prior to the trigger event by choosing the pre-trigger option, viewed on equal sides of the trigger event by choosing the mid-trigger option, or viewed after the trigger event by choosing the post-trigger option. When operating in a multi-board configuration as a slave, the Trigger Select bits become a "don't care"

(trigger is performed on the master board) but the Trigger Position bits should be set to the same value as the master boards.

Sample Clock Select

The sample clock is used to generate the rising edge the ADC control circuitry is looking for to initiate a data conversion. The Trigger Configuration register's Sample Clock Select bits (Bits 2, 1 and 0) allow the host to select from three sample clock sources: the on-board 14-bit timer, the I/O Sample Clock bit (write a logic "1" to Bit 5 of CSR1), or the external TTL level clock input located on connector P5. The host can choose to use either the rising or falling edge of the external clock. The host can choose to use the 2x (or channel double option) with the internal timer or external sample sources, if they are using a 16-channel board (not available with an 8-channel board). This clocking option allows the board to sample signals at twice the selected rate (maximum 200 kHz rate) with a net reduction in the number of channels available.

When using the 2x sampling option, the host must connect channels 0 and 8, 1 and 9, etc., together because both edges of the clock are being used for sampling (rising edge initiates a channel 0 conversion, falling edge initiates channel 8 conversion). When using the external sample clock in 2x mode, the sample clock must have a 50/50 duty cycle for the sampling to occur accurately. Refer to Chapter 2, *"External Trigger and Sample Clock Connector"* for details regarding connector P5 and its associated signals. The user can refer to Chapter 1 for more theory of operation information on the circuitry, or refer to Chapter 2 for more cabling and setup information.

Interrupts

The VMIVME-3123 board uses two flags located in the CSR1, Interrupt A and Interrupt B, to coordinate data retrieval with the host. These two flags, the Interrupt Level bits, and the Interrupt Vector Register comprise the interrupt control for the board. The Interrupt Level bits located in CSR1 are used to select the interrupt level on the VMEbus. The board's VMEbus interrupter logic supports one interrupt level at a time which requires the host to read the CSR1 to identify the interrupting flag. The host may wish to use register polling rather than interrupts to interface with the board and may do so by disabling the interrupter by setting the Interrupt Level bits to logic "000" and polling CSR1 for the appropriate flag.

The Interrupt Vector Register is an 8-bit read / write hardware register that the host may use in supporting VMEbus interrupt operation. The host should initialize the register per the host's application requirements. The contents of the Interrupt Vector Register will then be placed on the VMEbus data bus during a VMEbus Interrupt Acknowledge (IACK) cycle. The interrupt A and B flags are used by all modes but differ in their functions in Continuous Sample mode. Both the interrupt A and B flag bits will be set when Transient Capture mode, Calibration mode, or Self-Test mode conclude. The flag bits are used in these modes to indicate a mode has come to an end. In Continuous Sample mode, the function of the two bits differ. The interrupt A flag is used to indicate when the sample buffer is half-full. The on-board Digital Signal Processor (DSP) monitors the loading of the sample buffer (the sample buffer is determined by the Buffer Size bits and may or may not include all the on-board DRAM) and sets the interrupt A flag when half the buffer has been filled with data samples. The interrupt B flag will be set when the buffer is full and begins its rollover to begin filling again at address $000000.

Typical Programming Examples

The following examples of VMIVME-3123 programming illustrate typical applications for various operating modes.

Example 1

Perform calibration using Calibration mode, enable interrupt level 6, interrupt enabled.

Step 1. Initialize CSR1 for interrupt level 6. This also enables interrupts.

loc $XX06 = $0006

Step 2. Initialize IVR with VMEbus interrupt vector equal to hex 55.

loc $XX08 = $0055

Step 3. Place board into calibration mode.

loc $XX04 = $0004

The host will be interrupted when calibration has ended. Both the interrupt A and B flags will be set. The VMEbus IACK cycle will return a 55 to the host processor. The host should read CSR1 to clear the A and B flags during the host's interrupt service routine.

Example 2

Do a board self-test. Perform all tests as well as calibration. Do not enable interrupts.

Step 1. Initialize the Test Select / Status register to run all tests.

loc $XX1C = F800

Step 2. Disable the interrupter

loc $XX06 = 0000

Step 3. Start board self-test

loc $XX04 = 0005

The host can poll CSR1 for an indication of self-test completion by looking at the A or B flag. Both flags will be set when self-test completes. The host should perform a dummy read of CSR1 prior to polling in order to clear the A and B flags.

The host can poll CSR0 and check the mode bits b "000" (IDLE mode).

Upon completion of self-test, the host should read the Test Select / Status register again and look at the least significant 8 bits for the test results. If all tests passed, the register should read "$F8F8". If the analog tests failed, further debug information down to the channel level is available in the Analog Channel Errors registers.

Example 3

Set up and capture a transient event using the following:

- Interrupts disabled.
- Use the board's internal timer at a 75 kHz rate.
- Use the DSP trigger with a "$500" sample delay, threshold at GND, trigger position in the middle of the buffer and triggering on a positive edge on channel 1.
- Use all the DRAM for the buffer and place the DRAM in extended addressing space.
- Enable channels 0, 1, 2 and 3 as well as channels 9, 10, 11 and 13.
- Set the range for channels 0, 1, 2, 3, 8, 9, 10 and 11 to ±10 V and the range for channels 4, 5, 6, 7, 12, 13, 14 and 15 to ±5 V.

Step 1. Initialize IVR to disable interrupts.

loc $XX06 = 0000

Step 2. Initialize the Trigger Configuration register to select the DSP trigger option and the internal timer as the sample clock source.

loc $XX0A = 0060

Step 3. Initialize the internal timer sample rate for 75 kHz.

loc $XX1A = 00A5

Step 4. Initialize the trigger delay register to place the trigger point at a location h "500" samples after the trigger event.

loc $XX0C = 0500

Step 5. Initialize the Trigger Threshold register to trigger at GND. This value is always a two's complement number.

loc $XX0E = 0000

Step 6. Initialize the DSP Trigger Options / Buffer Configuration register to select channel 1 as the channel compare register, to trigger on a positive transition through the threshold value, to place the trigger (in this case delayed trigger) in the middle of the buffer, and to make the sample buffer as large as the entire DRAM (DRAM = 8 Mbytes).

loc $XX10 = 1517

Step 7. Initialize the DRAM to appear at an address of $55000000 in VMEbus extended address space and respond to both supervisory and nonprivilege access code.

loc $XX12 = 5501

Step 8. Initialize analog input channels 0,1, 2, 3, 8, 9, 10 and 11 for ±10 V range and channels 4, 5, 6, 7, 12, 13, 14 and 15 for ±5 V range. Data format will be two's complement.

loc $XX16 = 00F0

Step 9. Enable channels 0, 1, 2, 3, 9, 10, 11 and 13.

loc $XX18 = 2E0F

Step 10. Setup is complete, place the board in the Transient Capture mode, and enable the DRAM.

loc $XX04 = 0011

The board is now sampling the selected channels and filling the buffer with the samples. As the buffer is filled it rolls over and begins filling again. When a trigger event occurs on channel 1 (voltage moves above GND), the board will finish capturing the rest of the data and return to IDLE mode. The host can monitor the A and B flags in CSR1 or the mode bits in CSR0 for an indication that the transient is captured. The buffer start and end addresses as well as the trigger address are located in their respective registers and are available when the board returns to IDLE mode.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com .

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.

CHAPTER

A

Calibration Data

Contents

Introduction

Appendix A covers the raw calibration data stored in the DRAM buffers.

Raw Calibration Data

The VMIVME-3123 board will deposit raw precision reference values gathered during calibration mode into the DRAM buffer. These values are meant to be used as an aid in troubleshooting or to help the user to determine the boards general health. These samples are not used by the board in any manner.

The values are deposited sequentially beginning at the lowest DRAM address of XX000000 (hex). The samples are divided into a pair of six groups containing 256 samples and are separated by the following marking bytes: BEF1 (hex), BEF2 (hex), BEF3 (hex), BEF4 (hex), BEF5 (hex), BEF6 (hex) and BEEF (hex). The voltages are sampled in the following order: -9.98 VDC, -9.98 VDC, GND, GND, +9.98 VDC, +9.98 VDC, -4.99 VDC, -4.99 VDC, GND, GND, +4.99 VDC and +4.99 VDC. The first group of a particular voltage is disregarded in order for the voltage to settle completely before using the values for calibration.

Table A-1 Precision Reference Voltages

XX000000	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1
XX000010	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1
XX000020 to XX000210	Dummy -9.98 VDC samples, Not Used for Calibration							
XX000220	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2
XX000230	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2	BEF2
XX000240 to XX000430	-9.98 VDC samples used for calibration							
XX000440	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3
XX000450	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3	BEF3
XX000460 to XX000650	Dummy GND samples, Not Used for Calibration							
XX000660	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4
XX000670	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4	BEF4
XX000680 to XX000870	GND samples used for calibration							
XX0017A0 to XX001990	+4.99 VDC samples used for Calibration							
XX0019A0	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF
XX0019B0	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF	BEEF

The individual channels are deposited into the rows sequentially starting with channel 0 and ending with channel 15 as shown in Table A-2.

Table A-2 Channels 0 through 15

XX000000	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1
XX000010	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1	BEF1
XX000020	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7
XX000030	Ch 8	Ch 9	Ch 10	Ch 11	Ch 12	Ch 13	Ch 14	Ch 15
XX000040	Ch 0	Ch 1	ETC	ETC	ETC	ETC	ETC	ETC