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VMIVME-4116

8-channel 16-bit Digital-to-Analog Converter Board

Product Manual

A GE Fanuc Company

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500-004116-000 Rev. U

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Table of Contents

List of Figures 7

List of Tables 9

Overview 11

Features 11

Functional Description 14

References 15

Physical Description and Specification 15

Safety Summary 16

Warnings, Cautions and Notes 17

Chapter 1 - Theory of Operation 19

Immediate DAC Update Mode 21

Delayed DAC Update Mode 22

Program Control Update Mode 22

External Trigger Update Mode 22

VMIVME-4116 Test Mode Description 23

Using the VMIVME-4116 to Test the Multiplexer Channels of the VMIVME-3200 25

VMEbus Interface Description 26

P2 Connector I/O Signal Definition 28

Chapter 2 - Configuration and Installation 29

Unpacking Procedures 30

Configuration 31

Before Applying Power: Checklist 32

DAC Board Installation 32

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Board Address Selection Switches 33
Example 33
Address Modifier Response Selection 35
Digital Code Selection 36
Program Controlled And External Start Convert Mode 37
Connector Descriptions 38
Analog Output Accuracy When Optional Output Isolation Hardware is Used 39
DAC Zero Offset and Gain Calibration 44

Chapter 3 - Programming 47

DAC Board Programming Options 51
Introduction 51
Immediate DAC Update Mode 51
Example 52
Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions 53
Delayed DAC Update Mode 55
Test Mode Programming 56
MC68000 Assembly Language Programming of the VMIVME-4116 DAC Board 57
Program Example (Delayed DAC Update Mode) 58

Chapter 4 - Maintenance 63

Maintenance 63
Maintenance Prints 64

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List of Figures

Figure 1 VMIVME-4116 8-channel DAC Board 13

Figure 1-1 VMIVME-4116 Board Functional Block Diagram 20
Figure 1-2 VMIC High Performance Analog Input/Output Configuration 24
Figure 1-3 Optional Analog Output Isolation Switches 24
Figure 1-4 Test Bus Logic 25
Figure 1-5 VMEbus Interface Logic and Interface Signals 27
Figure 1-6 DAC Board Power 28

Figure 2-1 Address Selection Switches 33
Figure 2-2 Jumper and Switch Locations on the VMIVME-4116 34
Figure 2-3 Digital Code Selection 36
Figure 2-4 P2 Connector - Pin Assignments 40
Figure 2-5 P3 Connector - Pin Assignments 42
Figure 2-6 Calibration Adjustment Locations 45

Figure 3-1 DAC Programming Sequence (Immediate DAC Start Convert Mode) 59
Figure 3-2 Program Example (Immediate DAC Update Mode) 60
Figure 3-3 DAC Programming Sequence (Delayed DAC Update Mode) 61
Figure 3-4 Program Example (Delayed DAC Update Mode) 62

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List of Tables

Table 2-1 VMIVME-4116 Factory Preset Configuration 31
Table 2-2 P2 Connector 41
Table 2-3 P3 Connector 43
Table 2-4 VMIVME-4116 Calibration Table 44

Table 3-1 VMIVME-4116 Control and Status Register (CSR) (Read/Write) Address Map 47
Table 3-2 VMIVME-4116 DAC Channels (0 to 7) (Write) Address Map 48
Table 3-3 DAC Data Format Analog Output versus Digital Input (±10 V Scale) 51
Table 3-4 Control Register Data Format and Definitions 52
Table 3-5 Analog Output Over TEST BUS 1 (AINTESTBS) 53
Table 3-6 Analog Output Over TEST BUS 2 (AOTESTBS) 53
Table 3-7 Analog Output Over TEST BUS 2 and Over P3 Connector to Field-connected Device (Used for Real-time Fault Detection of DACs) 54
Table 3-8 Analog Output Over P3 Connector Only 54
Table 3-9 Analog Output Control in Immediate Update Mode 60
Table 3-10 Analog Output Control in the Delayed DAC Update Mode 62

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Overview

Introduction

This document will primarily describe the operation of the DAC board, but some details of the VMIVME-3100 ADC Board and the VMIVME-3200 32-channel multiplexer (MUX) board will be included for clarity. It is also intended to give the user a better understanding of the test capabilities of a data acquisition system using the DAC board in conjunction with the VMIC MUX expander board, (VMIVME-3200) and the ADC board, (VMIVME-3100). For a thorough understanding the reader should have access to the following documents:

- *VMIVME-3200 32-Channel Analog Input (MUX) Instruction Manual* (Document No. 500-003200-000)
- *VMIVME-3100 12-Bit Analog-to-Digital Converter (ADC) Board Instruction Manual* (Document No. 500-003100-000)

Features

Listed below are the primary features of the VMIVME-4116 DAC board:

- 16-Bit resolution
- Buffered voltage output (±10 V @ 5 mA)
- Double-buffered data latches
- Four or eight channels (option dependent)
- Eight 16-Bit DACs (one per channel)
- Front panel Fail LED
- High reliability DIN type output connector
- Multiplexed programmable outputs for testing analog input multiplexer boards
- Multiplexed programmable outputs for testing analog outputs
- Jumper-selectable synchronized update control
- Double Eurocard form factor

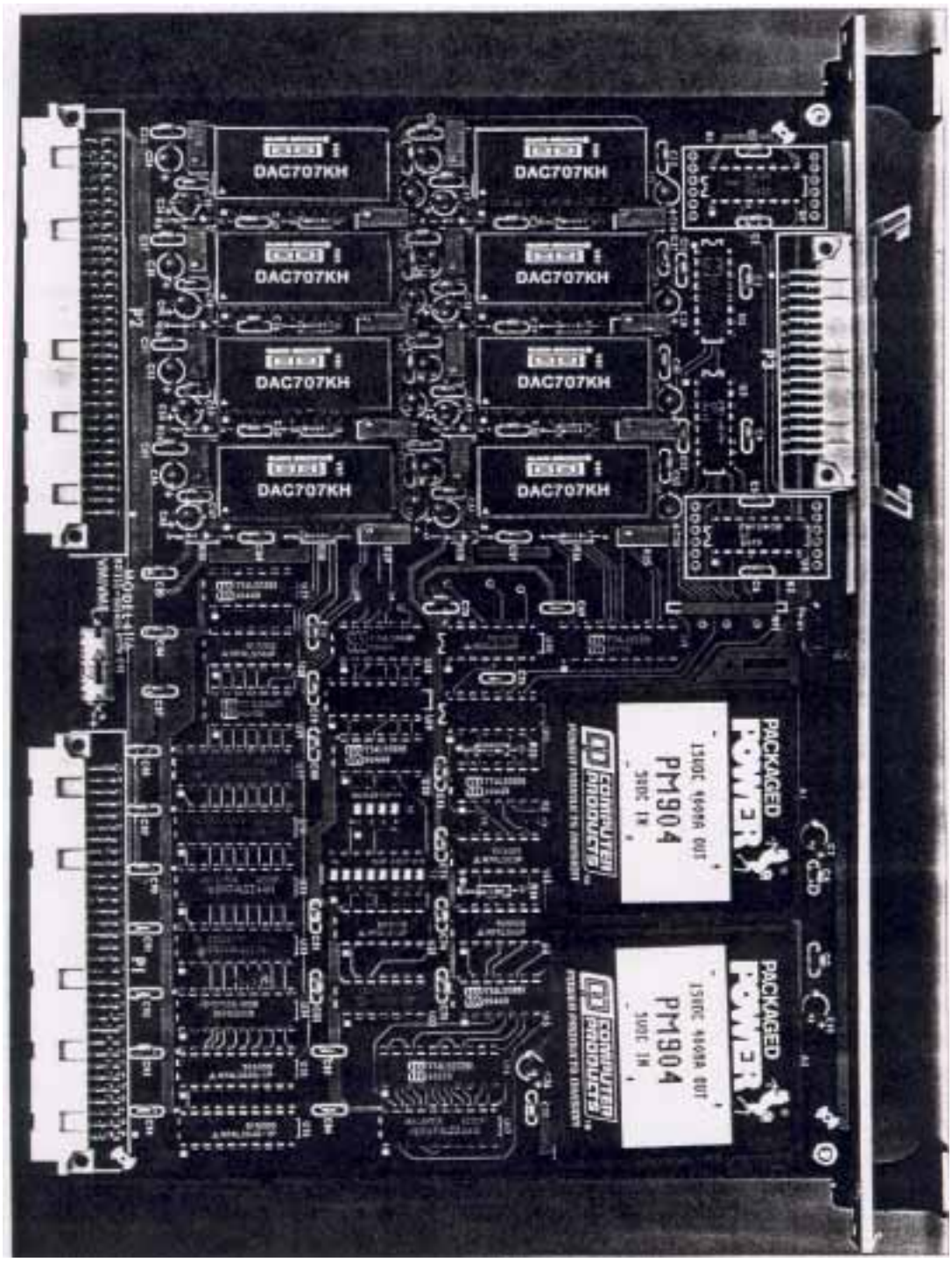
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- Selectable external update control input provides single update strobe for all DAC outputs
- Fast settling: 10 µs maximum to ±0.0003 percent of FSR
- Requires VMIVME-3100 ADC for Built-in-Test

A unique feature of the VMIVME-4116 DAC Board is the Built-in-Test logic that allows the testing of any one of the analog output channels through the use of an on-board multiplexer and the VMIVME-3100 ADC Board. When in test mode the field connections through connector P3 may be isolated and any of the eight channels may be routed to the 8-bit VMIVME-3100 ADC board via VMIC's analog backplane (AMXbus™). At the VMIVME-3100 ADC, board under program control, the analog signal may be converted to a 12-bit digital word and compared with the original 16-bit word written to the DAC board. In this manner each of the eight analog output channels may be verified without disturbing the field connected devices. However, the full accuracy of the analog outputs cannot be determined by a 12-bit VMIVME-3100 ADC. The analog output channels may also be multiplexed to the analog test bus simultaneously while controlling the P3 connected field devices, providing real-time fault detection of the outputs. If a board fails the self-test, a Fail LED on the front panel may be turned ON to indicate the board is in a failed condition. The complete operation and the requirements for the self-test mode are explained in detail in “Theory of Operation” on page 19 and “Programming” on page 47 of this manual.

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Figure 1 VMIVME-4116 8-channel DAC Board



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Functional Description

The VMIVME-4116 internal organization is illustrated in the functional block diagram shown in Figure Figure 1-1 on page 20.

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References

For a detailed description and specification of the VMEbus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook
VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

The following application and configuration guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products.

Digital Input Board Application Guide (Document No. 825-000000-000)

Change-of-State Application Guide (Document No. 825-000000-002)

Digital I/O (with Built-in-Test) Product Line Description (Document No. 825-000000-003)

Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide (Document No. 825-000000-004)

Analog I/O Products (with Built-in-Test) Configuration Guide (Document No. 825-000000-005)

Physical Description and Specification

Refer to VMIC's Specification No. 800-004116-000 for detailed specifications.

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

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CHAPTER

1

Theory of Operation

Introduction

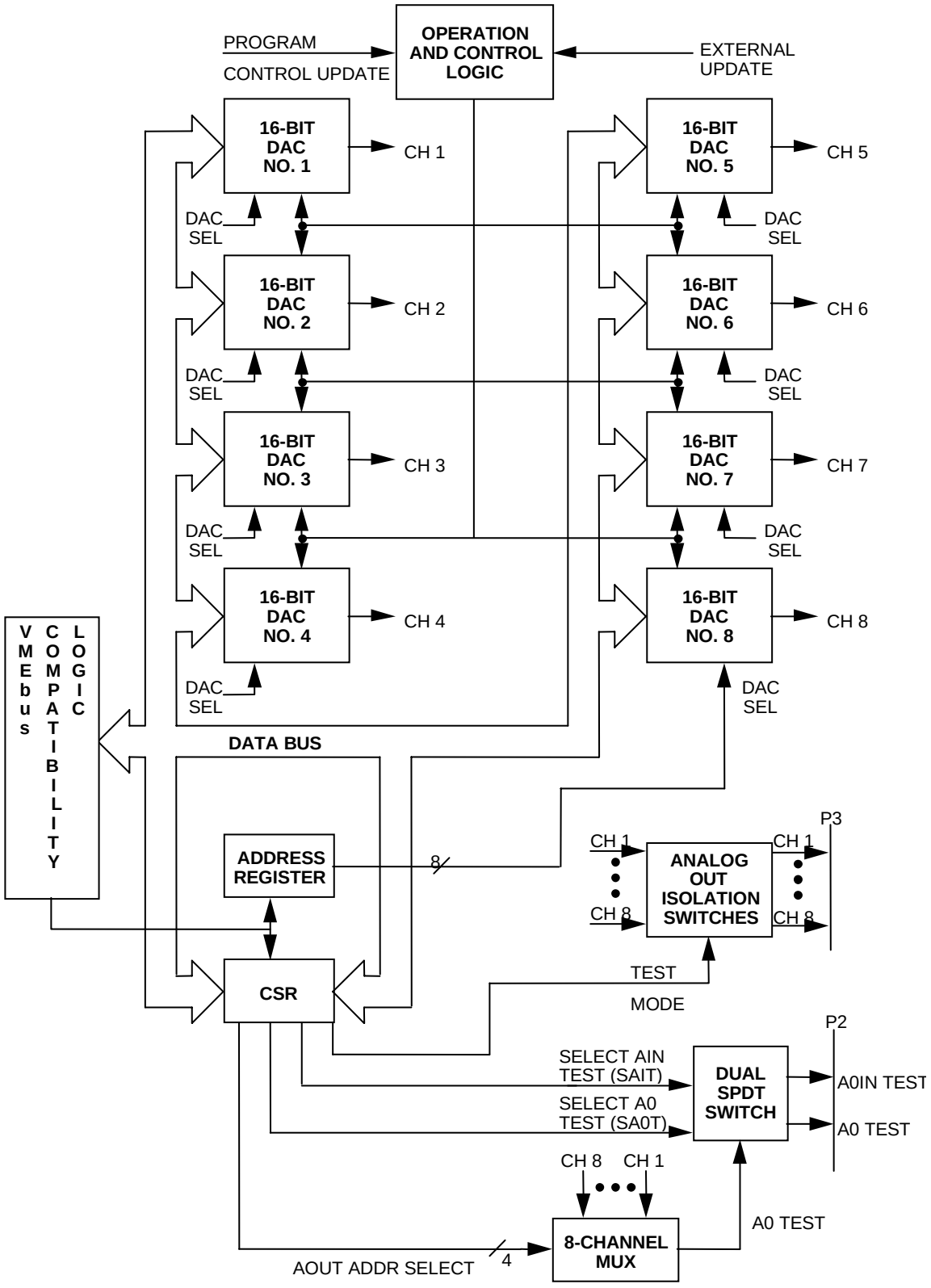
The VMIVME-4116 Digital-to-Analog Converter (DAC) Board performs digital-to-analog conversion on 16-bit positive true offset binary or two's complement coded words, with an analog output range of -10 to +10 V. This provides for a resolution of 305 µV for each digital input of 1 LSB change. The buffered output voltage settles to within 1/2 LSB in 10 µs.

The DAC offers a Digital-to-Analog Integrated Circuit (IC) per channel. A Control and Status Register (CSR) is loaded by the processor and this register controls the functioning of the board. The CSR can be read by the processor at any time. The DAC board functional block diagram is shown in Figure 1-1 on page 20. Each of the eight DACs is preceded by double-buffered data latches. The data latches allow versatility in the way that the DAC analog output may be updated.

There are three methods by which new data can be converted by a DAC. Each method is enabled/disabled by on-board jumpers and is further controlled by a CSR that must be loaded by the user (the CSR contents are described in Table 3-4 on page 52 and Table 3-5 on page 53).

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Figure 1-1 VMIVME-4116 Board Functional Block Diagram



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Immediate DAC Update Mode

The processor unit sends the 16-bit word to be converted to the first register of the selected DAC. If that DAC channel has previously been jumpered to, it will automatically pass the contents of the first DAC register into the second register and update the analog output. There is one jumper that enables / disables all eight DAC channels to be in the IMMEDIATE UPDATE MODE as described above, or in the DELAYED UPDATE MODE. Jumper definition and locations are described in “Program Controlled And External Start Convert Mode” on page 37.

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Delayed DAC Update Mode

In the DELAYED DAC UPDATE MODE, the processor sends the 16-bit word to be converted to the first DAC register of the selected DAC. The data is stored there and transferred to the second DAC register in one of two possible methods which are described in "Program Control Update Mode" and "External Trigger Update Mode" below.

Program Control Update Mode

One way for the transfer to occur is by writing a "one" to the Control Register bit D09. When the data is transferred to the second register, digital-to-analog conversion begins and the analog output settles to within 1/2 LSB in 10 µs. This method of updating the analog output is useful when more than one DAC channel output is desired to change at a precise time. All eight DAC outputs could be synchronized to change at certain periodic intervals under software control.

External Trigger Update Mode

The second method to update the second storage register and the DAC output by an external TTL compatible trigger. This trigger must first have the external trigger circuitry enabled by installing an on-board jumper as described in “Program Controlled And External Start Convert Mode” on page 37. The PROGRAM CONTROL UPDATE MODE must also be enabled (refer to “Program Controlled And External Start Convert Mode” on page 37). When the external trigger is received (active low for a minimum of 150 ns), the value stored in the first DAC register will be transferred to the second DAC register and begins a conversion. Using this method of updating all conversions can be synchronized to an external device.

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VMIVME-4116 Test Mode Description

The test mode hardware is optional (for options refer to Document 800-004116-000) and is only needed when the DAC is used along with the VMIVME-3100 ADC Board as a minimum, and possibly the VMIVME-3200 MUX Board. Both these boards support the Built-in-Test capabilities of the DAC and will be further explained here. A typical data acquisition configuration with Built-in Test capabilities is shown in Figure 1-2 on page 24. Up to 16 multiplexer boards or 16 DAC boards may be interconnected with one ADC board. Thus, a single chassis system could accommodate 128 analog outputs, or up to 528 single-ended analog inputs.

If testing the functioning of the analog output channels of the DAC is desired, then an ADC board is required. The ADC board will only test the DAC board to 12-bits of accuracy. These two boards must exist in the same VMIC (P2) analog backplane, VMIC has three low-noise Analog Multiplexer Bus backplanes (AMXbus™). They are available in 5-, 9-, and 19-slot widths to accommodate different analog I/O sizing requirements.

The AMXbus™ allows DAC analog outputs to be routed to the ADC board where they can be digitized and compared with the 16-bit word originally written to the DAC board. This digital-to-analog back-to-digital loopback test can be done with the field devices (at P3 Connector) connected or disconnected. This is accomplished by optional analog isolation switches (Figure 1-3 on page 24) at the output of the DACs. These switches are turned ON or OFF by the outputs of the on-board CSR.

Each of the DAC outputs may be multiplexed one at a time via the test MUX shown in Figure 1-4 on page 25. First, a control word must be written to the CSR to establish whether the analog output is to be connected or disconnected from the P3 connector and which one of two test buses the output is to be routed to. The DAC channel to be tested has test data written to it in the IMMEDIATE UPDATE MODE. Address bits A01 through A04 are automatically latched into the Address Register when the board is written to. The outputs of this Address Register selects the DAC channel that has just been updated via the test MUX. Test control information previously latched in the CSRs passes the DAC output through the analog test switch to the test bus 2. Test bus 2 is routed via the analog backplane (AMXbus™) to the input of the ADC board where it is available for analog-to-digital conversion. When the ADC completes its conversion, it sends an end-of-convert signal down the P2 backplane to the DAC. This signal removes either of the two test bus outputs from the analog backplane. Along with the test bus 2 signal being sent to the ADC board the analog ground (GND SEN) is switched out to the ADC board. This provides an input to the ADC board which is similar to a differential signal and is called pseudo-differential. Pseudo-differential solves some of the associated common mode error problems with single-ended signals. The input to the ADC board is referenced to the ground of the DAC board instead of the local ground at the ADC board, effectively cancelling out common mode errors associated with different ground potentials at each of the boards.

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Figure 1-2 VMIC High Performance Analog Input/Output Configuration

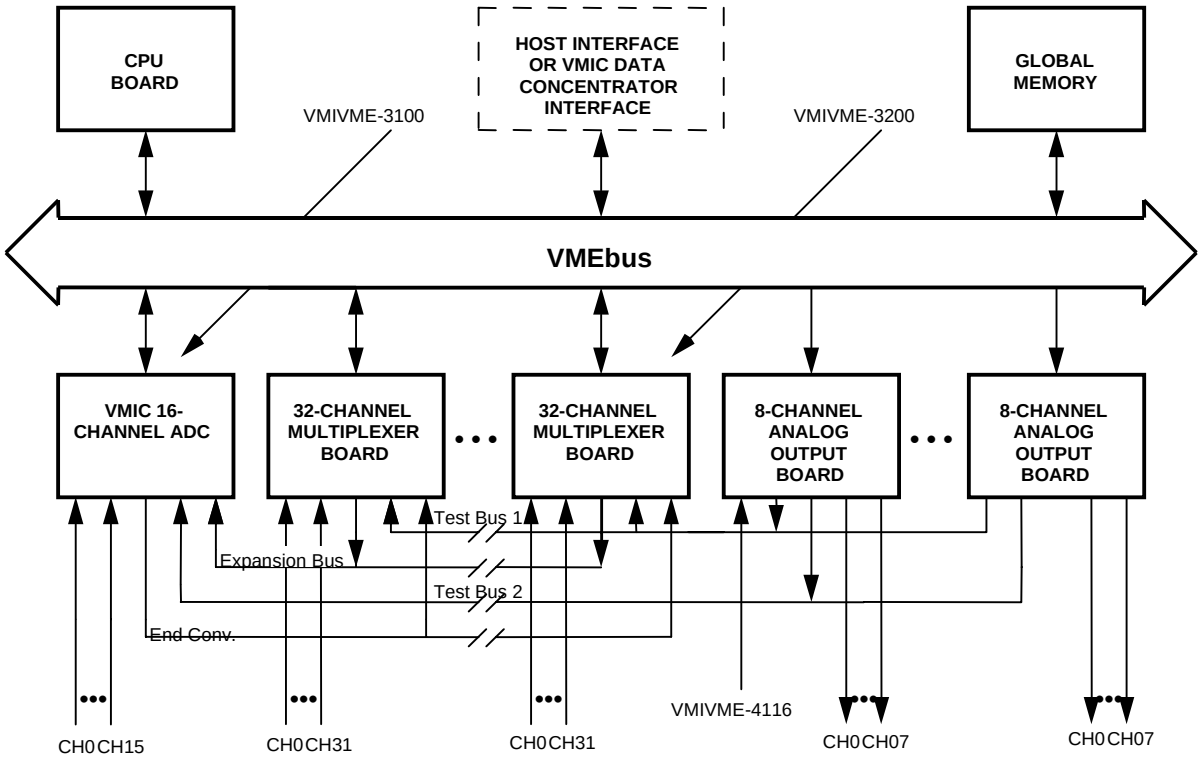
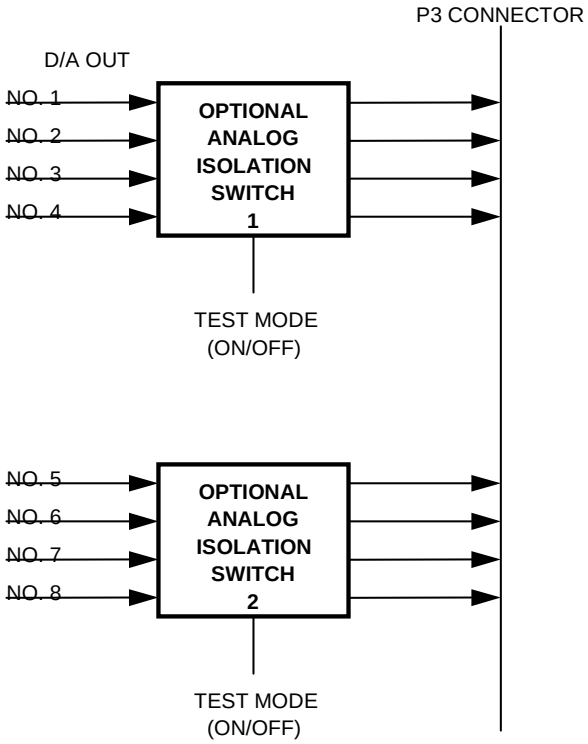
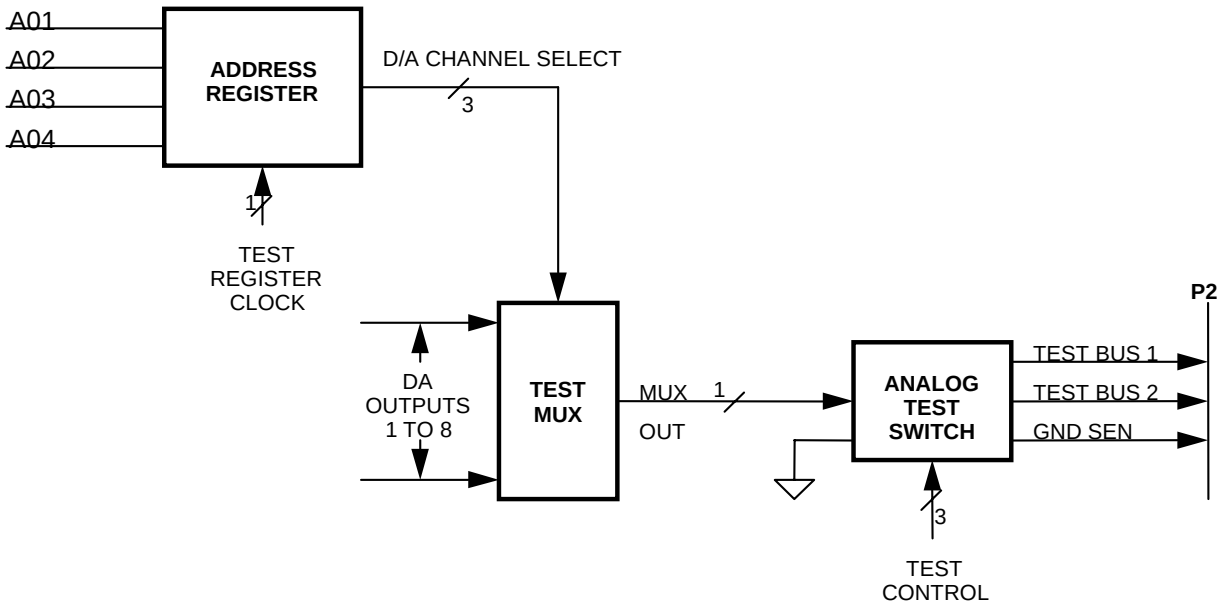


Figure 1-3 Optional Analog Output Isolation Switches



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Figure 1-4 Test Bus Logic



Using the VMIVME-4116 to Test the Multiplexer Channels of the VMIVME-3200

In a similar way as described in “Delayed DAC Update Mode” on page 22, any one of the DAC outputs can be selected via the test VMIVME-3200 MUX Board and analog test switch (Figure 1-4) to be routed out a separate dedicated analog bus entitled test bus 1. This test bus is a dedicated input to any MUX that resides in the same VMIC analog backplane. This test bus can be used by the MUX board to verify each of the 32 multiplexer channels by multiplexing the test bus inputs one at a time through a selected channel of the MUX onto the ADC board. For more details refer to VMIC's *VMIVME-3200 23-Channel Analog Input (MUX) Board Instruction Manual* (Document No. 500-003200-000) and the *VMIC Low Level Analog Data Acquisition System Manual.*

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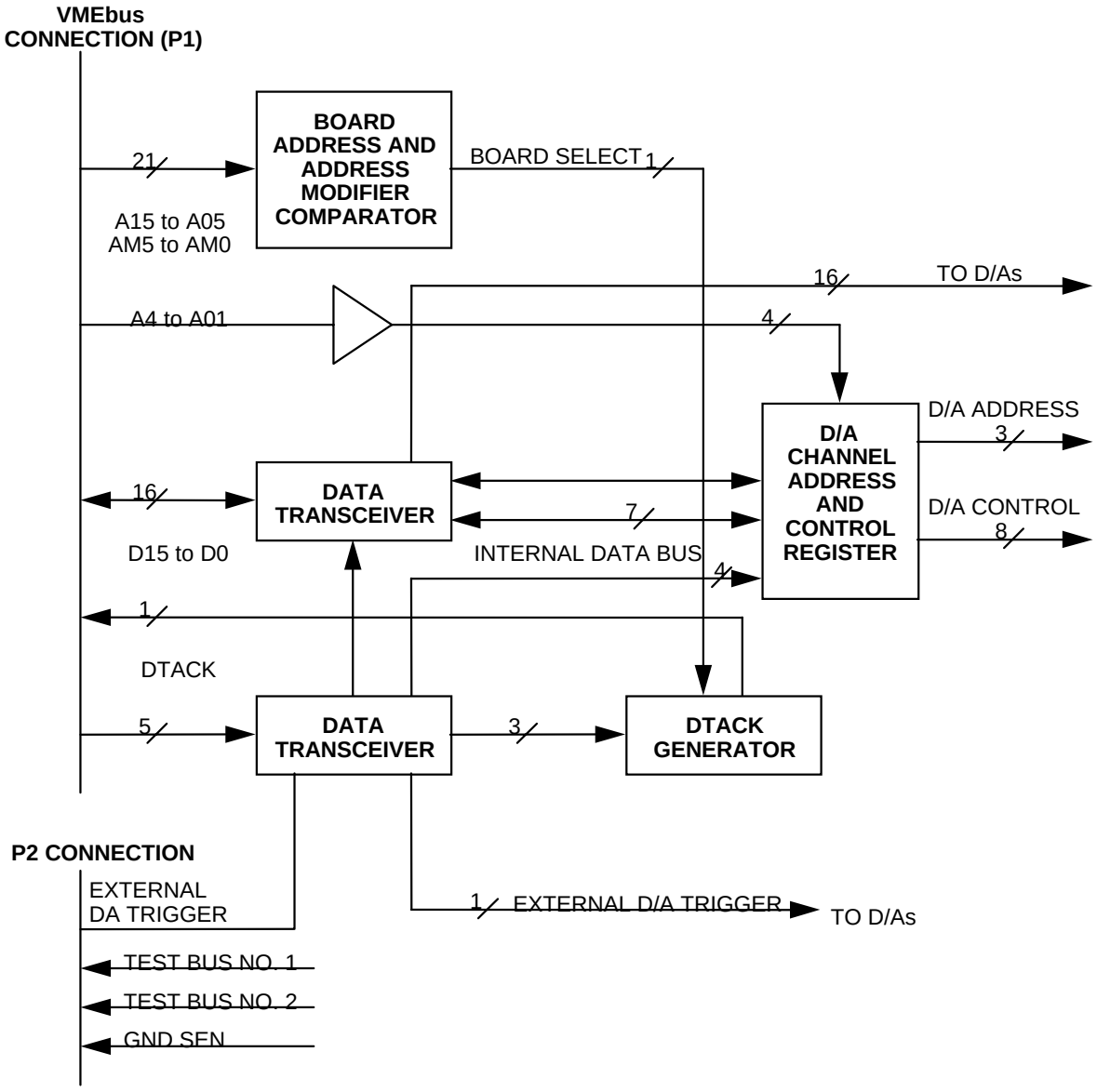
VMEbus Interface Description

The VMEbus interface (Figure 1-5 on page 27) contains the necessary logic to interface a DAC board to the VMEbus. The DAC is memory mapped in the VMEbus short I/O address space. During a *Write* cycle to the board, address bits A05 through A15 are compared with the previously selected board address. The board address is selected by DIP switches. If the address compares, then a board select signal is issued. This signal along with the control signals received at the board, gate the data (D0 to D15) to a selected DAC or the CSR on the DAC. Address bits A01 through A03 select one of the eight DAC channels. Data D0 through D15 is latched into the selected DAC Register. Address bit A04 is used to select the CSR.

The DAC circuitry requires +5 V, +15 V, and -15 V, the +5 V is supplied to the board via the P1 and P2 connectors. An on-board DC-to-DC converter generates the +15 V and -15 V for the analog circuitry (refer to Figure 1-6 on page 28). Thus, the DAC board only needs +5 V from the chassis power supply.

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Figure 1-5 VMEbus Interface Logic and Interface Signals



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P2 Connector I/O Signal Definition

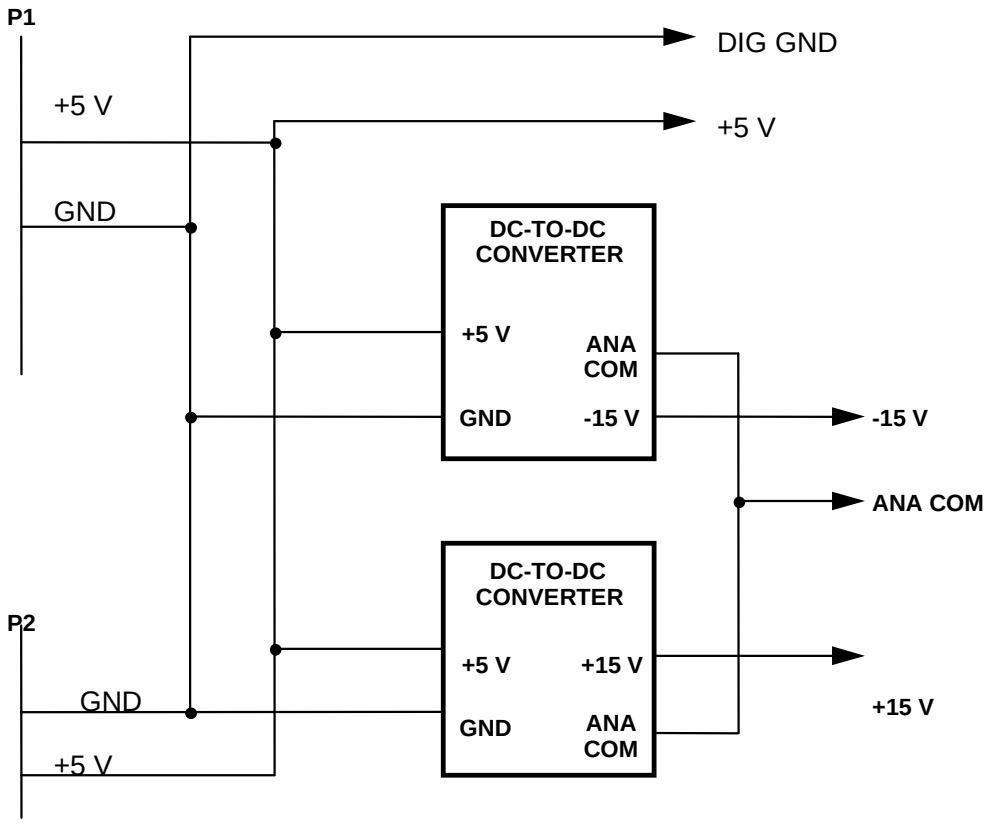
AINTESTBS (Test Bus 1) — An analog test signal that originates from the DAC board and is optionally used by the MUX expander board to verify the multiplexer channels. Test bus 1 may be multiplexed through each channel of the MUX board to an ADC board for conversion.

AOTESTBS (Test Bus 2) — A second analog test bus from the DAC board, used in conjunction with the ADC board, to verify the 8 analog output channels of the DAC board.

EXTSCL (External Start Convert-Low) — An externally provided, active low input. When this line is input low, any word stored in the DAC first rank registers will begin analog conversion. To initiate a conversion EXTSCL must go to a TTL low state for at least 150 ns before returning to a TTL high state. The board must have previously been jumpered to enable the board to receive an External Start Convert Signal (see Section 5).

GNDSEN — In test mode when test bus 2 is used, an analog ground from the DAC board is routed out the GND SEN line. The GND SEN line provides for a pseudo-differential input to a receiving ADC board.

Figure 1-6 DAC Board Power



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CHAPTER 2

Configuration and Installation

Contents

Unpacking Procedures 30
Configuration 31
Board Address Selection Switches 33
Address Modifier Response Selection 35
Digital Code Selection 36
Program Controlled And External Start Convert Mode 37
Connector Descriptions 38
Analog Output Accuracy When Optional Output Isolation Hardware is Used 39
DAC Zero Offset and Gain Calibration 44

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

NOTE: Do not install or remove board while power is applied.

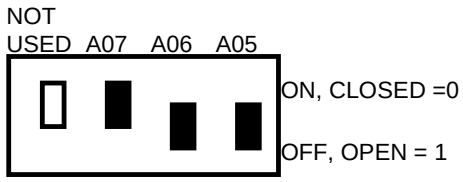
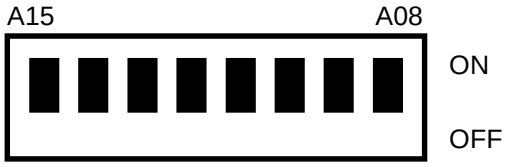
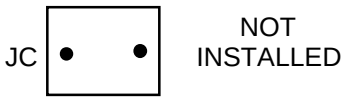
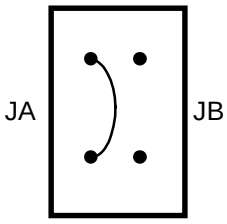
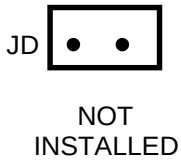
De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated. Review "Configuration" on page 31 and "Before Applying Power: Checklist" on page 32 before operating the board.

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Configuration

This section of the manual describes the VMIVME-4116 Digital-to-Analog Converter (DAC) Board set up procedure and jumper configuration. The board select base address and board jumper configuration is factory preset and shown in Table 2-1. The base address selection switches (S1 and S2) are factory configured at XXXX0060 HEX.

Table 2-1 VMIVME-4116 Factory Preset Configuration

Jumper	Function	Preset Condition
S1	Base Address Selection Switches (A07, A06, A05)	
S2	Base Address Selection (A15 to A08)	
JC	Determines address modifier response of the board. Installed jumper indicates response to short nonprivileged I/O access.	
JA, JB	Determines the digital code written to the DAC. JB installed gives two's complement binary coding. JA installed gives offset binary coding.	
JD	Installation of this jumper enabled the program controlled start convert mode as detailed in section "Program Control Update Mode" on page 22.	

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Table 2-1 VMIVME-4116 Factory Preset Configuration (Continued)

Jumper	Function	Preset Condition
JE	Installation of this jumper enables the external start convert mode as detailed in section "External Trigger Update Mode" on page 22. Jumper JD must also be installed to enable this mode.	 NOT INSTALLED

Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming of the DAC board, "Theory of Operation" on page 19 and "Programming" on page 47, been read and applied to system requirements?
2. Review Table 2-1 to verify the factory installed jumpers and board address switches are set to what is desired.
   a. To change DAC board switches (S1 and S2) refer to "Board Address Selection Switches" on page 33.
   b. To change address modifier response jumper (JB) refer to "Address Modifier Response Selection" on page 35.
3. To change the DAC digital code selection refer to "Digital Code Selection" on page 36.
4. To use either the program controlled start convert mode or the external start convert mode refer to "Program Controlled And External Start Convert Mode" on page 37.
5. Has the cable, with proper mating connector, been connected to the analog output connector (P3)? Refer to "Connector Descriptions" on page 38.
6. When optional output isolation hardware is employed on the VMIVME-4116, review "Analog Output Accuracy When Optional Output Isolation Hardware is Used" on page 39 for load impedance requirement.

After the checklist above has been completed, the board can be installed in a VMEbus system. This board can be installed in any slot position, with the exception of slot-one which is usually reserved for the master processing unit.

DAC Board Installation

After steps 1 through 6 have been reviewed the DAC board may be installed in a VMEbus system. (Do not install or remove the board with power ON). The DAC board may generally be installed in any slot position, except slot "one" which is usually reserved for the master processing unit.

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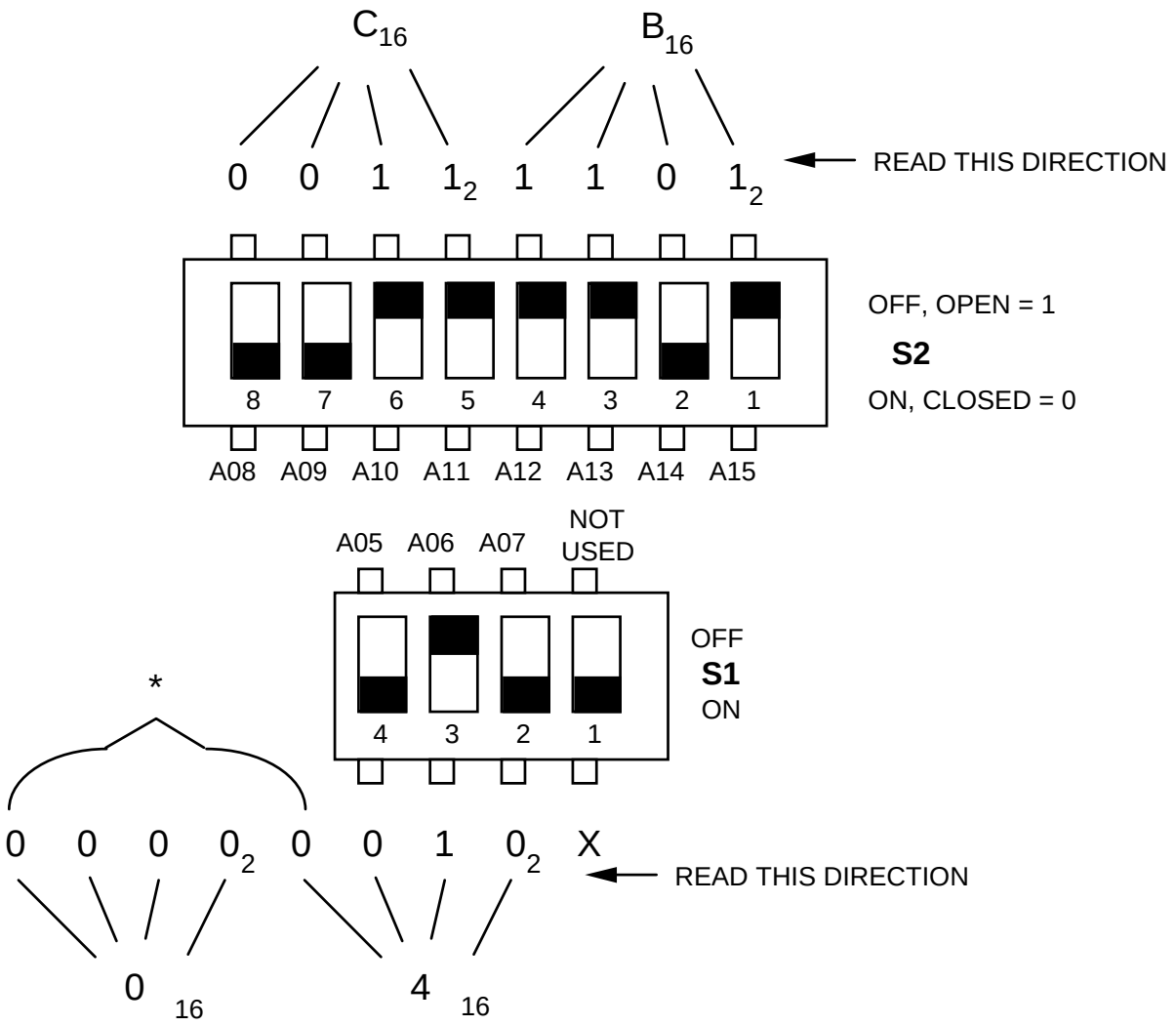
Board Address Selection Switches

There are two address select DIP switches on-board the VMIVME-4116. Each individual switch corresponds to an address bit, or is not used. If the switch is ON the corresponding address bit is compared to a logic "zero". All corresponding address bits must compare with the switch positions during a *Write/Read* of the DAC board. Each switch corresponds to the address bits as shown in Figure 2-1 below. For the board switch locations are shown in Figure 2-2 on page 34.

Example

For the VMIVME-4116 to respond to a base address of (FXFFBC4016) the S1 and S2 switches would be set accordingly.

Figure 2-1 Address Selection Switches

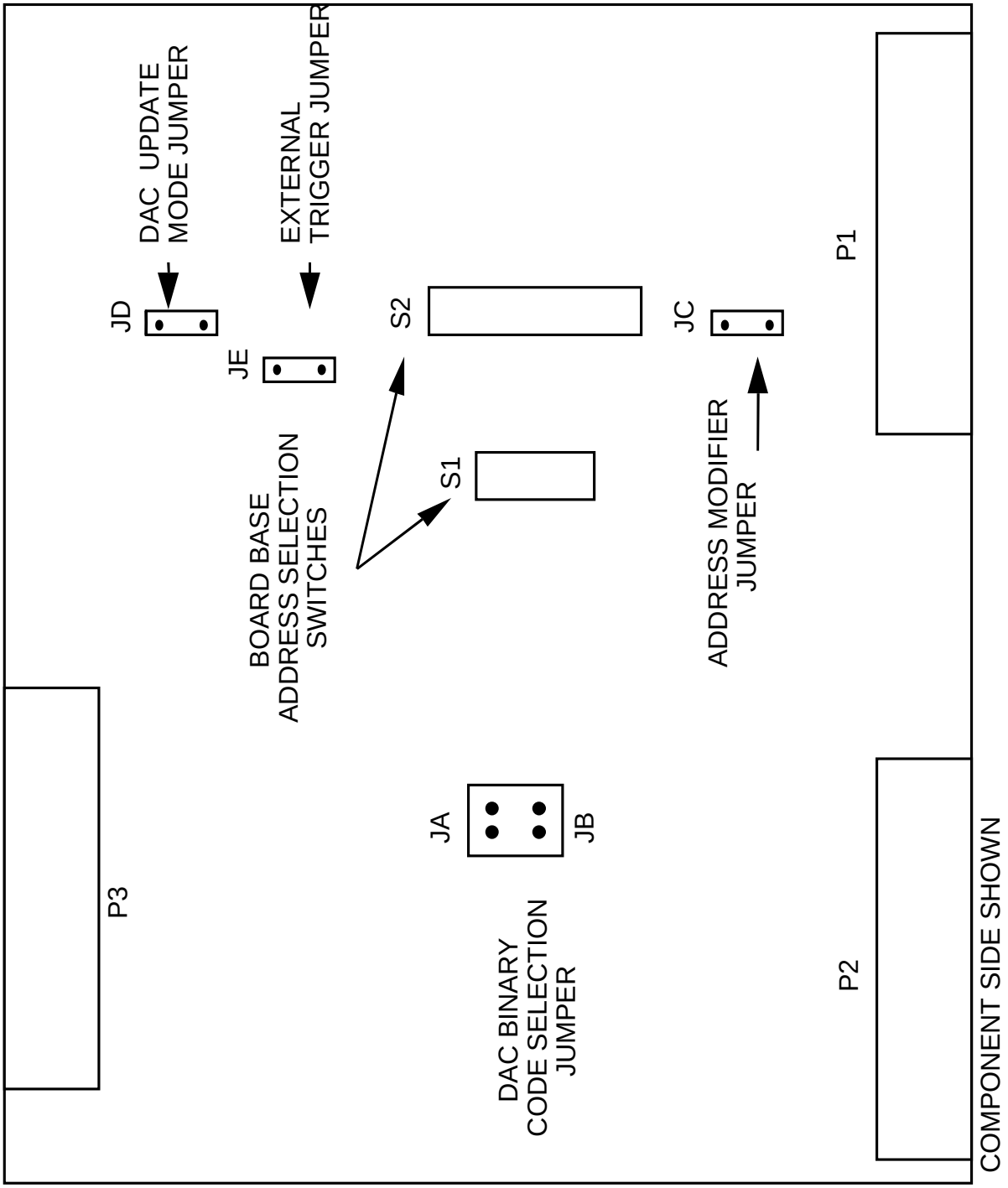


*No switches on-board to represent bits A00 through A04. These bits are understood to be "zeros".

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NOTE: Only bits A05 through A15 have corresponding switches. A16 through A31 are not compared on-board and will vary from CPU to CPU. For example, force uses FBFF while Motorola uses FFFF.

Figure 2-2 Jumper and Switch Locations on the VMIVME-4116



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Address Modifier Response Selection

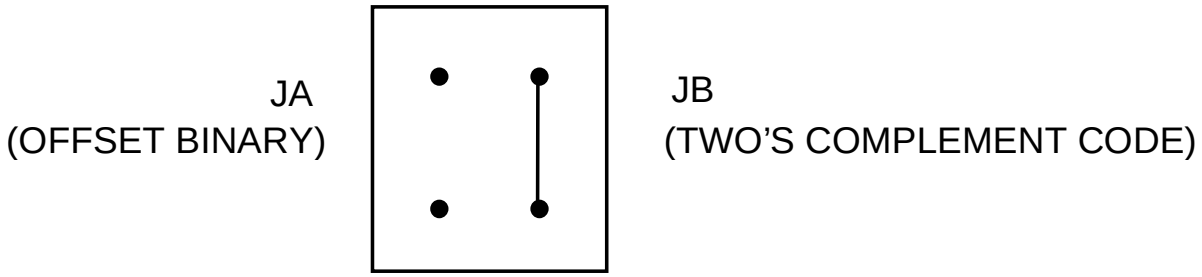
The DAC board is memory mapped in the short I/O address space as described in "Programming" on page 47. The DAC board will respond to either of the two address modifier codes that may be issued to the DAC board by a CPU board during a Write or Read cycle. The DAC board is factory set to respond to supervisory short I/O access. To select short nonprivileged I/O access then install the jumper at jumper location (JC) (refer to Figure 2-2 on page 34).

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Digital Code Selection

The DAC board is factory configured for offset binary coding. To change the DAC input coding to two's complement binary, remove jumper JA and install jumper JB (see Figure 2-3 below).

Figure 2-3 Digital Code Selection



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Program Controlled And External Start Convert Mode

The PROGRAM CONTROLLED START CONVERT MODE is enabled by inserting jumper JD. This mode is detailed in "Program Control Update Mode" on page 22 and "Delayed DAC Update Mode" on page 55. With no jumper installed at JD, the board operates in the IMMEDIATE DAC UPDATE MODE as described in "Immediate DAC Update Mode" on page 21 and "Immediate DAC Update Mode" on page 51.

The EXTERNAL START CONVERT MODE is enabled by installing jumper JE. Jumper JD must also be installed (refer to "External Trigger Update Mode" on page 22). The external trigger is buffered in through the P2 connector pin A25 with an associated digital ground wire at pin A26. The locations of jumpers JD and JE are shown in Figure 2-2 on page 34.

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Connector Descriptions

Two 96-pin DIN type connectors, P1 and P2, connect the DAC board to the VMEbus backplane. The primary connector, P1, contains the address data and control lines and all additional signals necessary to control data transfer and other bus functions. The P2 connector carries the I/O lines necessary to join the DAC board with the optional MUX expander board and the ADC board. The P2 connector connects the DAC board with the analog P2 backplane (AMXbus™). See Figure 2-4 on page 40 and Table 2-2 on page 41 for the P2 connector signal assignments.

If the test bus option is to be used in conjunction with other VMIC analog I/O boards, then the user must use a VMIC printed circuit analog P2 backplane. These backplanes are available in different slot widths to accommodate almost any combination of boards.

The P3 connector is a Panduit 32-pin male connector type, number 120-332-033A. The matching Panduit connector for the input cable is a female connector type, number 120-332-435E. This connector handles the 16 analog outputs, each with an associated analog ground wire. See Figure 2-5 on page 42 and Table 2-3 on page 43 for P3 connector assignment.

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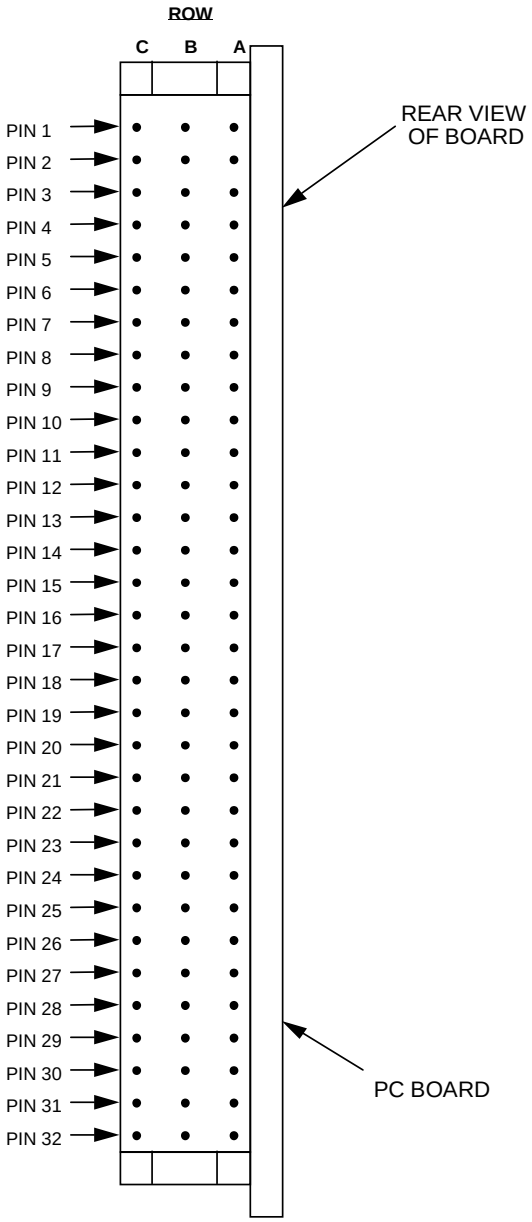
Analog Output Accuracy When Optional Output Isolation Hardware is Used

The VMIVME-4116 is offered to the user in several option configurations to the user. One of which is the use of Built-in-Test functions when used with other VMIVME boards, as discussed in "Delayed DAC Update Mode" on page 22.

The Built-in-Test hardware features analog output isolation switches for all eight channels that can be turned ON / OFF by software commands. These switches are in series with the analog output and the user-connected device at the P3 connector. These switches have an ON resistance of approximately 100Ω (maximum). If the user-connected load does not have a high impedance input then a possible voltage division error is introduced. For example, if R(LOAD) is 10 kΩ then a 1 percent error is introduced. R(LOAD) should be 10 M or greater for an error of 0.001 percent or less.

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Figure 2-4 P2 Connector - Pin Assignments



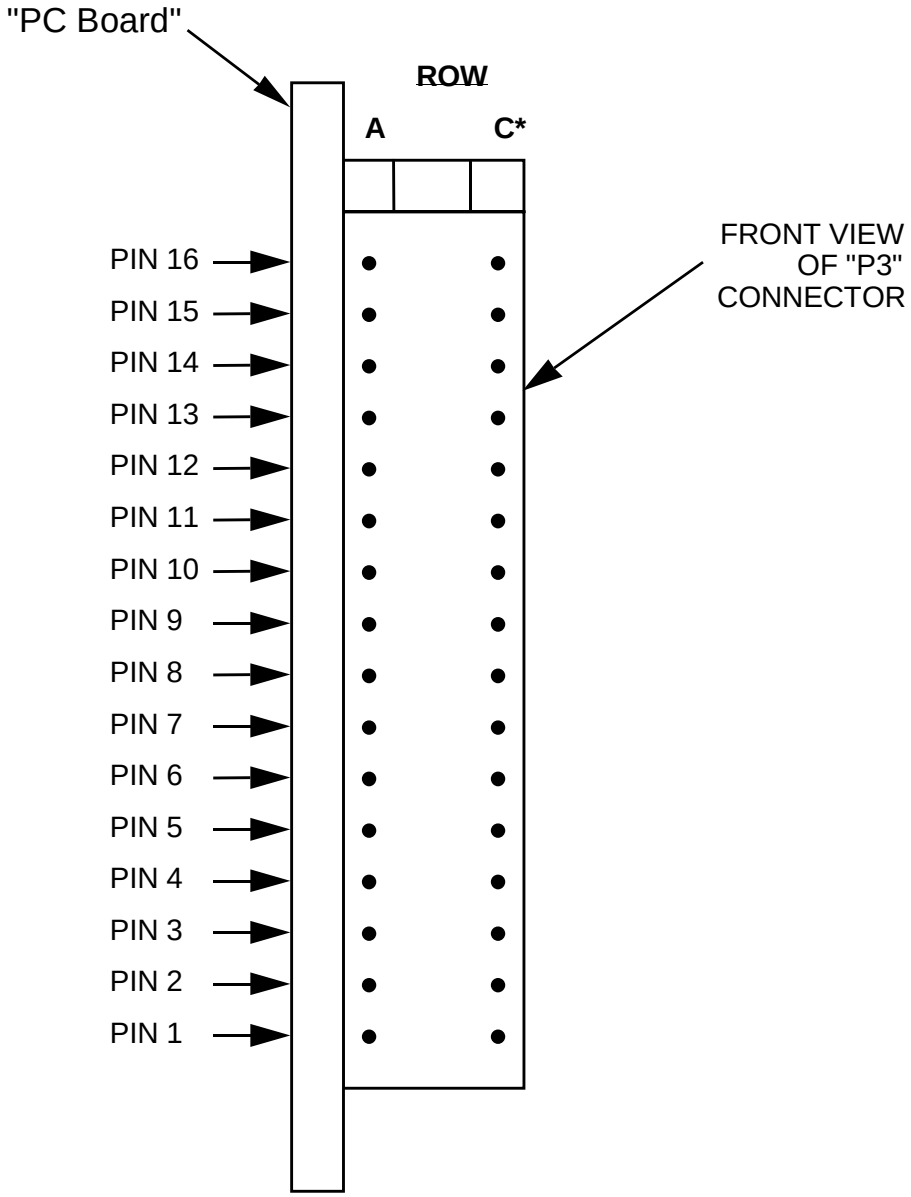
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Table 2-2 P2 Connector

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	ANA COM	+5V	
2	ANA COM	GND	
3	ANA COM		
4	ANA COM		
5	ANA COM		
6	ANA COM		
7	AINTESTBS		
8	ANA COM		
9	AOTESTBS		
10	ANA COM		
11			
12	ANA COM	GND	
13		+5V	
14	ANA COM		
15	GND SEN		
16	ANA COM		
17			
18	ANA COM		
19			
20	ANA COM		
21			
22	ANA COM	GND	
23	ANA COM		
24	ANA COM		
25	EXTSCL		
26	GND		
27			
28			
29			
30			
31		GND	
32		+5V	

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Figure 2-5 P3 Connector - Pin Assignments



*Row C pins are all analog common

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Table 2-3 P3 Connector

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	ANA COM		
2	AN00		ANA COM
3	AN01		ANA COM
4	AN02		ANA COM
5	AN03		ANA COM
6	AN04		ANA COM
7	AN05		ANA COM
8	AN06		ANA COM
9	AN07		ANA COM
10			
11			
12			
13			
14			
15			
16			

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DAC Zero Offset and Gain Calibration

NOTE: This procedure assumes that the offset binary coding jumper (JA) is selected.

1. Remove power from the VMIVME-4116.
2. Remove any cable connected to the P3 connector.
3. Remove the VMIVME-4116 from the chassis assembly and install a VMEbus Extender board in its place.
4. Install the VMIVME-4116 on to the VMEbus Extender board.
5. Apply power to the module and allow 15 minutes for Temperature Stabilization before making any measurements.
6. Using the IMMEDIATE UPDATE MODE write digital code 4100 HEX to the CSR location XXXX0070. This HEX code is the Control Word for output to the VMIVME-4116 P3 connector.
7. Write 8000 HEX to each of the eight DAC channels at addresses XXXX0060 through XXXX006E.
8. Using a 6-digit multimeter, monitor each DAC output at the P3 connector. Connect the negative lead to connector P3 pin C2. Adjust each DAC's offset potentiometer for a voltage of 0.0000 ±60 µV. Refer to Table 2-4 below and Figure 2-6 on page 45 for the Potentiometer Location and P3 connector pin for each channel.

Table 2-4 VMIVME-4116 Calibration Table

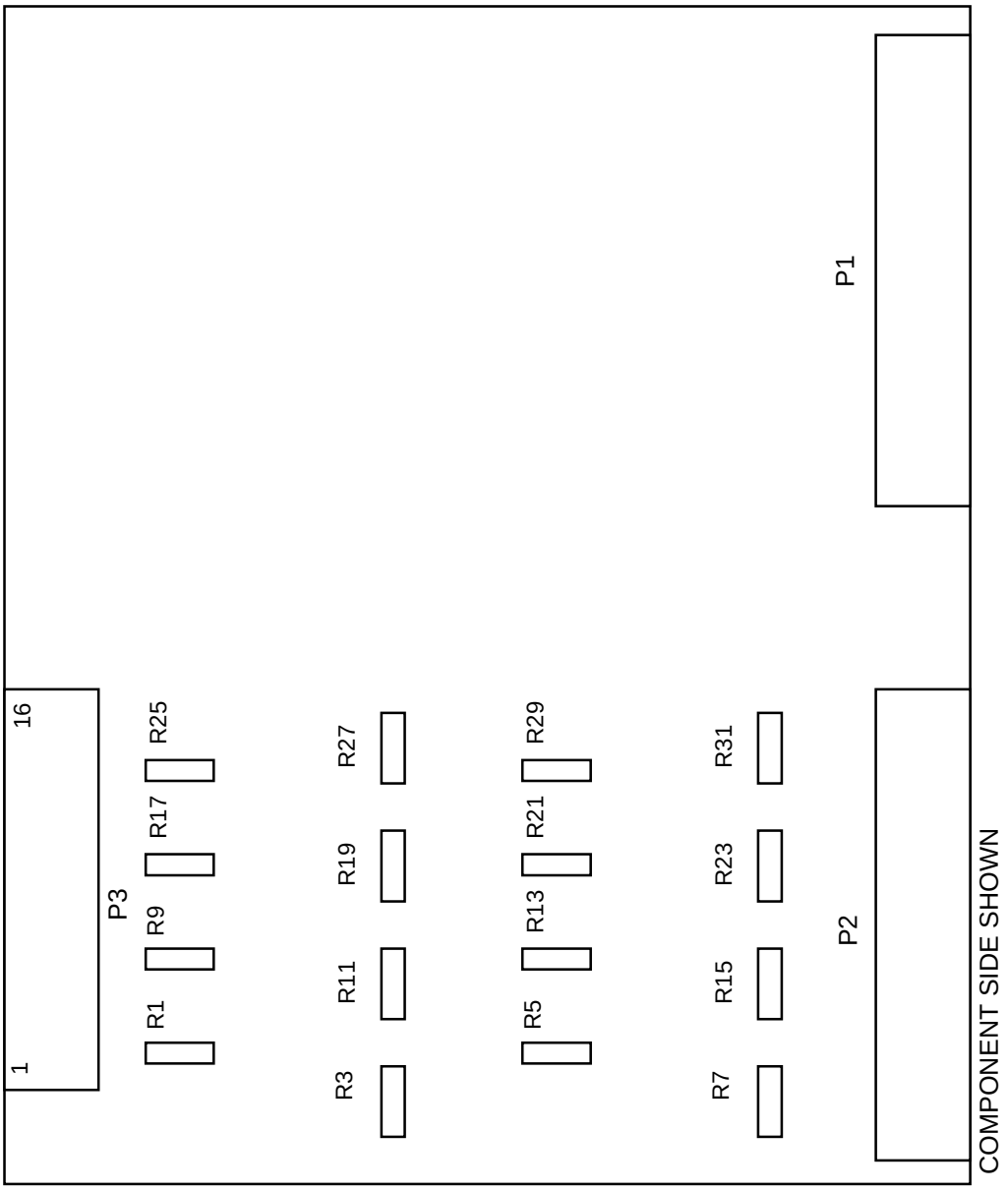
Channel	Offset POT	Gain POT	P3 Connector
1	R23	R21	A2
2	R19	R17	A3
3	R31	R29	A4
4	R27	R25	A5
5	R3	R1	A6
6	R7	R5	A7
7	R15	R13	A8
8	R11	R9	A9

9. Repeat Step 7 using digital code FFFF HEX.

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10. Using the multimeter, monitor each DAC output at the P3 connector. Connect the negative lead to connector P3 pin C2. Adjust each DAC's gain potentiometer for a voltage of 9.99969 ±60 µV. Refer to Table 2-4 on page 44 and Figure 2-6 below for the Potentiometer Location and P3 connector pin for each channel.
11. Remove extender and re-install board into the chassis. Calibration completed.

Figure 2-6 Calibration Adjustment Locations



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CHAPTER 3

Programming

Contents

DAC Board Programming Options 51
Delayed DAC Update Mode 55
Test Mode Programming 56
MC68000 Assembly Language Programming of the VMIVME-4116 DAC Board 57
Program Example (Delayed DAC Update Mode) 58

Introduction

The VMIVME-4116 Digital-to-Analog Converter (DAC) Board is memory mapped in the short I/O address space. The board occupies 16 successive word locations in the VME short I/O address space of 65,535 bytes. Only the first nine word locations are actually used by the board. The short I/O space is located from XXXX0000 HEX to XXXXFFFF HEX. The address bits A31 to A16 are CPU dependent. Each Read cycle may be either a word or byte transfer. The board base address may be selected by DIP switches as shown in "Board Address Selection Switches" on page 33. Table 3-1 and represents the DAC address map assuming the factory set base address of XXXX0060 HEX.

Table 3-1 VMIVME-4116 Control and Status Register (CSR) (Read/Write) Address Map

Address XXXX0070 Control and Status Register (CSR) (Read/Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used	Control and Status Bits						

Address XXXX0070 Control and Status Register (CSR) (Read/Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

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Table 3-2 VMIVME-4116 DAC Channels (0 to 7) (Write) Address Map

Address XXXX0060 DAC Out 0 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX0060 DAC Out 0 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

Address XXXX0062 DAC Out 1 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX0062 DAC Out 1 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

.

Address XXXX0064 DAC Out 2 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX0064 DAC Out 2 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

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Table 3-2 VMIVME-4116 DAC Channels (0 to 7) (Write) Address Map (Continued).

Address XXXX0066 DAC Out 3 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX0066 DAC Out 3 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

.

Address XXXX0068 DAC Out 4 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX0068 DAC Out 4 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

.

Address XXXX006A DAC Out 5 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX006A DAC Out 5 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

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Table 3-2 VMIVME-4116 DAC Channels (0 to 7) (Write) Address Map (Continued).

Address XXXX006C DAC Out 6 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX006C DAC Out 6 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

.

Address XXXX006E DAC Out 7 (Write)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
MSB							

Address XXXX006E DAC Out 7 (Write)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
LSB							

NOTE: Jumper JC determines whether the board operates in short supervisory I/O access or short nonprivileged I/O access. with the jumper installed short nonprivileged I/O access is selected.

Table 3-2 shows addressing information for 16-bit word transfers. Data may be transferred to the DACs in 8-bit format. When using byte format, the low byte is always transferred first then the high byte next. For example, assuming a board base address of XXXX0000 HEX, a low byte transfer (D7 to D0) to Channel 0 is written to address XXXX0001 HEX. The high byte of data (D15 to D8) is then written to address XXXX0000 HEX.

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DAC Board Programming Options

Introduction

There are two types of registers that must be written to for proper operation of the DAC board. One is the CSR, and the other is the DAC. The order in which they are written to may differ depending on the method used to start a conversion.

Immediate DAC Update Mode

The IMMEDIATE DAC UPDATE MODE is described in "Immediate DAC Update Mode" on page 21 and the board is configured for this mode when received from the factory. Once this has been set up, a 16-bit word can be written to any DAC channel where it will begin immediate analog conversion. When byte transfer (8-bit) is used to load the DAC channel, conversion begins immediately upon the loading of the high byte (D15 to D8).

The CSR controls the analog isolation switches(*) between the DAC outputs and the P3 (user) connector. All eight DAC channels can be initiated to a value, as described in the preceding paragraph, before they are connected to the external circuitry. After powering up the board, load the DAC channels with the initial 16-bit word (or two 8-bit bytes) required (positive true offset binary or binary two's complement coding, Table 3-3 below). A control word can then be written to the CSR to enable the DAC outputs to the P3 connector. The CSR bit description for this mode of operation is detailed in Table 3-4 on page 52 and Table 3-5 on page 53.

(*) Analog isolation switches are optional. P3 isolation is dependent upon ordering option support.

Table 3-3 DAC Data Format Analog Output versus Digital Input (±10 V Scale)

Offset Binary Coding					
Digital Input Code				Analog Output Voltage	
(MSB) D15			(LSB) D0		
0000	0000	0000	0000	-10.000V	-Full Scale
0100	0000	0000	0000	-5.000V	-1/2 Scale
1000	0000	0000	0000	0.000V	Zero
1000	0000	0000	0001	300µV	+LSB
1100	0000	0000	0000	+5.000V	+1/2 Scale
1111	1111	1111	1111	9.99969V	+Full Scale

The analog output may be calculated by the input code written by the processor to the selected DAC channel as follows:

Analog Output = -10 V + ([(Digital Input Code in decimal) X 20]/65536)

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Example

The analog output for a digital input of 0A00H would be:

1. 0A00H decimal equivalent is 2560
2. Analog out = -10 V + ((2560) $\frac{20}{65{,}536}$)

$$= 9.21875$$

Table 3-4 Control Register Data Format and Definitions

Control Register							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used					Not Used	Program Control Start Convert	

Control Register							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

Control Register Bit Definitions:

Bit D15 — Not used.

Bit D14 — A low state turns the Fail LED ON. A high state turns the Fail LED OFF. At power-up this control bit is low.

Bit D13 — A high state enables the selected analog output to pass out the P2 connector on test bus 2 (AOTESTBS). At power-up this control bit is low.

Bit D12 — A high state enables the selected analog output to pass out the P2 connector on test bus 1 (AINTESTBS). At power-up this control bit is low.

Bit D11(2) — When written high, it engages one analog output from the DAC to one of two test buses. Used in conjunction with D12 and D13 to determine which test bus is selected. At power-up this control bit is low which disengages the test buses.

Bit D10 — Not Used.

Bit D09 — **Program Control Start Convert** — When set to a "one", it generates a signal that transfers contents of previously loaded DACs to the second rank register and updates the analog output.

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Bit D15 Not used.

Bit D08(1) When written high, it engages DAC outputs to the P3 connector, and disengages DAC outputs from P3 connector when written low. At power-up this control bit is low.

(1) Applies only to boards with output isolation option. Otherwise this bit is a don't care.

(2) Channel selection for muxing one of the outputs to either test bus is achieved by writing the CSR data to the data address + 10H. See "Test Mode Programming" on page 56 for additional information.

Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions

Table 3-5 Analog Output Over TEST BUS 1 (AINTESTBS)

Control and Status Register (CSR)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used	1	0	1	1	Not Used	0 or 1	0

Control and Status Register (CSR)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

Table 3-6 Analog Output Over TEST BUS 2 (AOTESTBS)

Control and Status Register (CSR)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used	1	1	0	1	Not Used	0 or 1	0

Control and Status Register (CSR)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

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Table 3-7 Analog Output Over TEST BUS 2 and Over P3 Connector to Field-connected Device (Used for Real-time Fault Detection of DACs)

Control and Status Register (CSR)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used	1	1	0	1	Not Used	0 or 1	1

Control and Status Register (CSR)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

.

Table 3-8 Analog Output Over P3 Connector Only

Control and Status Register (CSR)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
Not Used	1	0	0	0	Not Used	0 or 1	1

Control and Status Register (CSR)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
Not Used							

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Delayed DAC Update Mode

The DELAYED DAC UPDATE MODE operation is described in "Delayed DAC Update Mode" on page 22. This mode must have previously been enabled by the jumper configuration in "Program Controlled And External Start Convert Mode" on page 37. There are two ways for a DAC channel to be updated after the 16-bit word is loaded into the DAC's first register. The first way is under program control when data bit D9 is written high to the CSR. It should be noted that when setting D9 to initiate the DAC update that control bits D8, and D11 through D14 should be set or reset according to where the user wants the converted output to be routed, (refer to Table 3-4 on page 52 and "Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions" on page 53). Also, a previously loaded DAC may be updated by an external trigger input from another device. A programming example of the DELAYED DAC UPDATE MODE is detailed in "Program Example (Delayed DAC Update Mode)" on page 58.

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Test Mode Programming

As described in "VMIVME-4116 Test Mode Description" on page 23, any of the eight DAC outputs may be selected to pass to an ADC board over test bus 2 to verify the DAC outputs. If a MUX is present in the analog backplane then any DAC output can be selected to go to that board for test purposes over test bus 1. Generally the programming sequence for utilizing one of the two test buses is as follows:

If IMMEDIATE DAC UPDATE MODE is employed, then a Control Word should first be written to the CSR. This Control Word information includes which test bus the DAC output is to be routed to, and whether the output is to be isolated or connected to the P3 connector (refer to Table 3-4 on page 52 and "Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions" on page 53). The DAC to be updated is then loaded with a 16-bit word. The channel is updated and passes out the selected test bus.

An output may also be updated under program control to route to a specified test bus. The board must have previously been jumpered to accommodate the DELAYED DAC UPDATE MODE as shown in "Program Controlled And External Start Convert Mode" on page 37. The programming sequence is as follows:

First, a 16-bit word or two 8-bit bytes are written to the address of the DAC channel that is to be updated. The data is stored in the DAC Register and will be converted by setting the proper bits in a Write cycle to the CSR. The CSR must be written to at the same address as that of the DAC channel that has previously been loaded plus 10 HEX. For example, if the user wanted to convert Channel no. 2 which was written to address XXXX0062 HEX, then the Control Word would be written to address XXXX0072 HEX (XXXX0062 and 10 HEX). Data bit D09 when written as "one" to the CSR initiates the analog conversion of the previously stored 16-bit word.

The test modes can only be used if an ADC board exists in the same VMIC analog (P2) backplane (AMXbus™) as the VMIVME-4116.

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MC68000 Assembly Language Programming of the VMIVME-4116 DAC Board

Just a few assembly language statements is all that is necessary to properly control and utilize the DAC board. It will be assumed that the base address of the board in this example is FF0060. The board address can be determined as described on page 47 and in"Board Address Selection Switches" on page 33.

The first example will be the loading of all the eight Digital-to-Analog Converters (DACs) with a full scale value of FFFFH giving an analog output over the P3 connector of 9.99969 V. The DAC output value will be updated immediately upon being written to. This is the IMMEDIATE DAC UPDATE MODE explained in "Immediate DAC Update Mode" on page 51. The following program is intended as an instructional example only and may not be useful in the user's application. A flowchart of this example is shown in Figure 3-3 on page 61 and the assembly language program is shown in Figure 3-2 on page 60.

In Step 2 in Figure 3-2 on page 60 the Control Register was set to enable the analog outputs over the P3 connector. The outputs could have also been selected to pass out either of the two test buses, or out the AOTESTBS and the P3 connector simultaneously by selecting the proper Control Word as determined from "Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions" on page 53 and as shown below in Table 3-9 on page 60, the HEX value for the different control words.

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Program Example (Delayed DAC Update Mode)

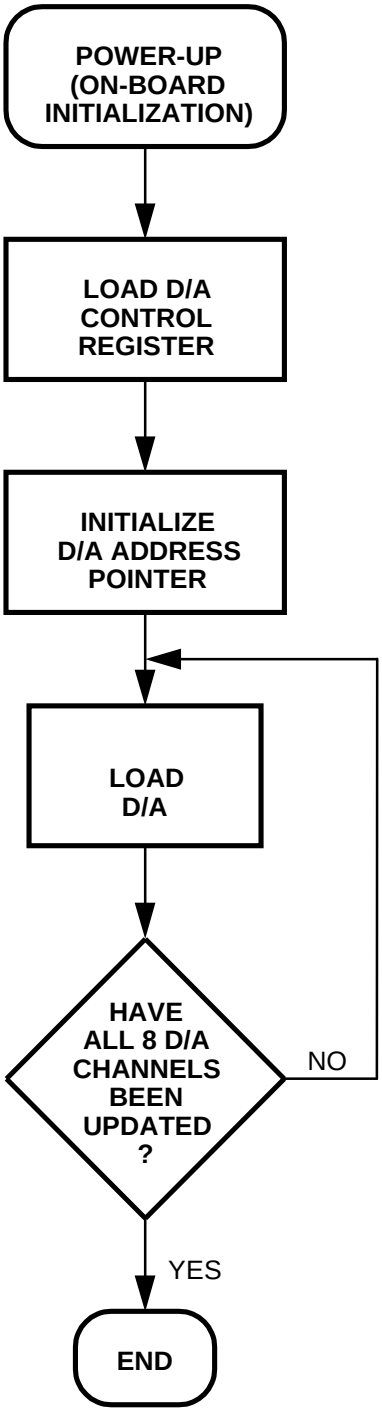
In the programming example in "Test Mode Programming" on page 56 all eight DAC converters were loaded with a full scale value of FFFH in the IMMEDIATE UPDATE MODE. For illustration purposes the same result will be obtained by this programming example by using the DELAYED DAC UPDATE MODE. The DELAYED DAC MODE is jumper-selectable as described in "Program Controlled And External Start Convert Mode" on page 37.

The programming sequence in a flowchart is shown in Figure 3-4 on page 62. Figure 3-4 on page 62 is the example program listing and comments. A base address of FF0060 is assumed.

In the following program example all eight DAC channels are loaded with new data, and then updated under program control. Alternatively, if previously enabled, an external trigger input could have initiated the DAC conversion process.

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Figure 3-1 DAC Programming Sequence (Immediate DAC Start Convert Mode)



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Figure 3-2 Program Example (Immediate DAC Update Mode)

			Comment
Load Next D/A	MOVE.W	#0 D0	1
	MOVE.W	#4100, $FF0070	2
	LEA	$ FF0060, A0	3
	MOVE.W	#$ FFFF, (A0)+	4
	ADD.W	#1, D0	5
	CMP.W	#$ 0008, D0	6
	BNE	LOAD NEXT D/A	7
	STOP		8

Comments

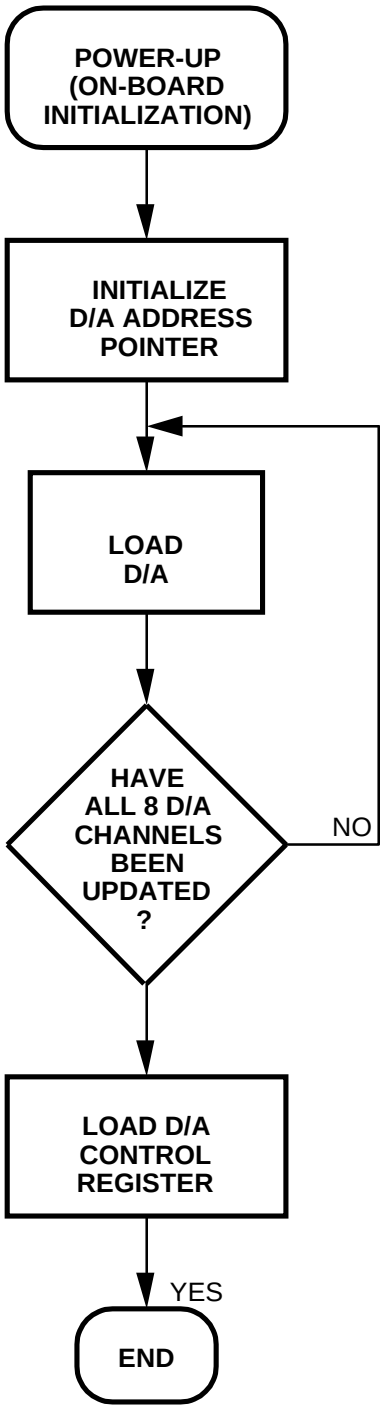
1. Initialize Register D0 (used as a counter) to "zero".
2. Load Control Register to enable DAC outputs to P3 connector.
3. Load address of DAC Channel no. 1 into Address Register A0.
4. Load DAC channel with maximum value. Address pointer is automatically incremented to next DAC channel.
5. Increment counter stored in D0.
6. If all eight DAC channels have not been loaded then (7).
7. Load next DAC channel.
8. Else STOP.

Table 3-9 Analog Output Control in Immediate Update Mode

Analog Out Pathway	Control Word (D15 to D0) Hex Value
P3 Connector	4100
AOTESTBS (TEST BUS 2)	6C00
AINTESTBS (TEST BUS 1)	5C00
AOTESTBS and P3 Connector	6D00

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Figure 3-3 DAC Programming Sequence (Delayed DAC Update Mode)



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Figure 3-4 Program Example (Delayed DAC Update Mode)

			Comment
Load Next D/A	MOVE.W	#$ 0 D0	1
	LEA	$ FF0060, A0	2
	MOVE.W	#$ FFFF, (A0)+	3
	ADD.W	#1, D0	4
	CMP.W	#$ 0008, D0	5
	BNE	LOAD NEXT D/A	6
	MOVE.W	#$4300, $FF0070	7
	STOP		8

Comments

1. Initialize Register D0 (used as a counter) to "zero".
2. Load address of DAC Channel no. 1 into Address Register A0.
3. Load DAC channel with maximum value. Address pointer is automatically incremented to next DAC channel.
4. Increment counter stored in D0.
5. If all eight DAC channels have not been loaded then (6).
6. Load next DAC channel.
7. Load Control Register to start digital-to-analog conversion of all eight DAC channels. Analog outputs routed out P3 connector.
8. STOP.

In step 7 above, the Control Register was set to enable the analog outputs to pass out the P3 connector. The outputs could have been selected to pass out either of the two test buses or out the AOTESTBS (test bus 2) and the P3 connector simultaneously by selecting the proper Control Word as determined from "Programming the Control and Status Register for Different Analog Output Variations - Bit Definitions" on page 53 and shown in Table 3-10 below.

Table 3-10 Analog Output Control in the Delayed DAC Update Mode

Analog Out Pathway	Control Word (D15 to D0) Hex Value
P3 Connector	4300
AOTESTBS (TEST BUS 2)	6E00
AINTESTBS (TEST BUS 1)	5E00
AOTESTBS and P3 Connector	6F00

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Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

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