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VMIVME-4140
32-Channel 12-bit Analog Output Board

Product Manual

A GE Fanuc Company

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Huntsville, Alabama 35803-3308, USA
(256) 880-0444 • (800) 322-3616 • Fax: (256) 882-0859

500-004140-000 Rev. D

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Overview

Introduction

Features

The VMIVME-4140 Analog Output Board has 32 analog output channels with 12-bit resolution, sourcing up to 10 mA at ±10 V. Each output has a dedicated Digital-to-Analog Converter (DAC) assigned to it. The analog outputs can be disconnected from the field wiring for off-line testing. Calibration and self-test are initiated by a VMEbus system reset or by execution of a software command. During calibration, a table of offset and gain coefficients is compiled and stored in RAM. There is an entry for offset and gain corresponding to each of the 32-channels configured in each of the 6 output voltage ranges.

The VMIVME-4140 has the following features:

- 32 Analog output channels
  - 10 mA maximum output current per channel
  - One 12-bit Digital-to-Analog Converter (DAC) per output channel
  - 0.8Ω output impedance (typical)
- Random update (non-scanning) or synchronous update (external or software)
- Automatic calibration initiated by system reset or by software command
- Unipolar (0 to +10 V, 0 to +5 V, or 0 to +2.5 V) or bipolar (±2.5, ±5, or ±10 V) software selectable voltage ranges
- Discrete wire or mass terminated cables
- Self-Test
  - Extensive on-board diagnostic testing capability
  - Outputs can be disconnected from the field
- Front panel status LED
- Front panel analog output connector
- Front panel reference voltage access
- Front panel reference voltage adjustment

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References

VMEbus Specification Rev. C. and the VMEbus Handbook
VMEbus International Trade Assoc. (VITA)
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(602) 951-0720 (FAX)
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Physical Description and Specification

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Safety Symbols Used in This Manual

STOP: informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER 1

Theory of Operation

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Introduction

The VMIVME-4140 provides 32 non-scanning 10 mA analog outputs. This capability is attained by the following principal hardware functions, as shown in Figure 1-1 on page 17:

- VMEbus Interface
- Digital Signal Processor (DSP)
- EPROM
- Control Logic
- Analog Outputs
- Self-Test Network
- Power Converters

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VMEbus Interface

The VMIVME-4140 responds to word (D16) or byte (D08(EO)) data accesses. Nonprivileged, supervisory or both access modes are supported along with short, standard, and extended address modes.

Control and Status Registers (CSRs)

The Control and Status Registers offset address begins at $000. The Board ID Register contains an ID code which indicates the VMIVME-4140, 32- or 16-channel ordering option.

The Configuration Control Register provides control of the front panel LED, output switches, output voltage range, output polarity, output synchronization, and the data format.

The Self-Test Control Register provides failure status of calibration/self-test and provides further control of calibration and the front panel LED.

Self-Test Status Registers 0 and 1 provide status of any channel which has failed calibration/self-test.

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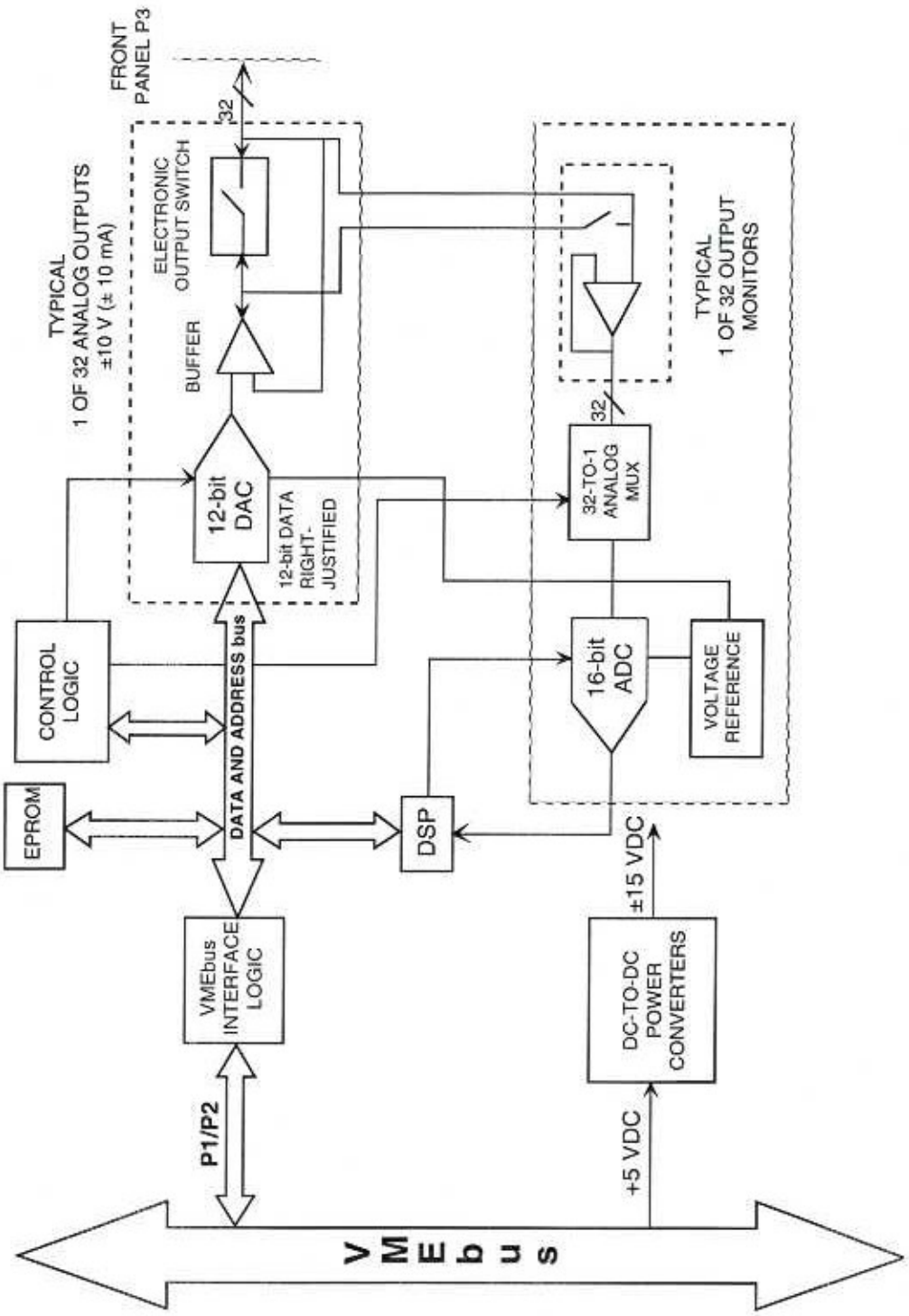


Figure 1-1 VMIVME-4140 Functional Block Diagram

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Output Data Registers

The Output Data Registers offset address begins at $040. The data format for unipolar output ranges is binary, and the bipolar data format is either offset binary or 2's complement as programmed in the Configuration Control Register (CCR). In either data format the data is right justified.

Commands

The user can issue a number of commands to the VMIVME-4140 via the VMEbus. The commands are initiated by VMEbus byte write access at the indicated address.

The Software Reset Command returns the board to its power-up reset state with the outputs off-line, and starts calibration/self-test. During calibration/self-test the VMEbus access should be limited to reading of the Board ID register. The Board ID Register's data appears as $FFFF while calibration/self-test is still active. When calibration/self-test is complete, this register's data appears as $2A00 for 32 channel option or $2A01 for the 16-channel option. During calibration/self-test the board will respond to any valid VMEbus access, however, this should be avoided if possible in order to keep digital traffic on-board to a minimum during the critical calibration period. Any data written to the board during this time will not be stored and any read will result in data of $FFFF.

The Software SYNC Command provides software synchronization of all output channels. The CAL/Test Command starts calibration/self-test but does not return control registers to their power-up state. The outputs are taken off-line during calibration/self-test. Output Data registers are returned to their power-up state (0 V).

The 32 Test Channel Commands provide the user the capability of individually testing any of the 32-outputs. Like with the CAL/Test Command, VMEbus access is limited to Board ID reads until the test is complete, which is indicated by $2A00 or $2A01. Unlike CAL/Test Command, this command does not take the outputs off-line during the test.

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Digital Signal Processor (DSP)

Upon initiation of calibration/self-test, the outputs are taken off-line and control of the Digital-to-Analog Converters (DACs) passes to the DSP. A least mean square estimate of the channel transfer function is found for each of the output channels in each of the output ranges and polarities. A gain and offset correction is calculated from this estimate and stored in RAM. When calibration is complete the DSP writes stimulus test values to the DACs and reads response test values from the Analog-to-Digital Converter (ADC).

If the difference between the response and stimulus test values are outside the specified error tolerance the failing channels are indicated in the Self-Test Status registers. On VMEbus write access to the Output Data Registers, the user data is stored unchanged in the Output Data register. The output data is modified by the appropriate gain and offset values and output to the corresponding DAC.

Upon initiation of a channel test the DSP reads from the ADC and compares the value read to the data in the corresponding Output Data register. If the difference is outside the specified error tolerance the failing channel is indicated in the corresponding Self-Test Status register.

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EPROM

The DSP firmware is stored in the EPROM. New boot pages are loaded into the DSP during power-up, calibration/self-test and channel test.

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Control Logic

The control logic consists of the logic required to load and synchronize the DACs and the logic required to control output range and polarity.

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Analog Outputs

The VMIVME-4140 can provide ±10 mA at output ranges of 0 to 2.5 V, 0 to 5 V, 0 to 10 V, ±2.5 V, ±5 V, and ±10 V.

Digital-to-Analog Converter (DAC)

The output Digital-to-Analog Converters (DACs) have two sets of data registers, this allows the outputs to be updated either when the data is written to the channel or when an external or software trigger occurs. The output ranges and polarities are achieved by controlling the voltage reference to the DACs.

Buffer

The outputs are buffered and protected from a short circuit to ground. The on-line output impedance is 0.8Ω (typical).

Output Switch

The outputs are powered-up in an off-line state and return to this off-line state during calibration. When outputs are taken off-line under software control the output impedance is 10 MΩ

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Self-Test Network

This network allows any channel to be monitored through firmware control during calibration, or software control with the Test Channel commands.

Analog-to-Digital Converter (ADC)

A single 16-bit Analog-to-Digital Converter (ADC) is used to convert the selected channel for calibration and test purposes. The ADC has a fixed precision reference which produces a range of ±10 VDC.

Voltage Reference

The voltage reference is the only part of the VMIVME-4140 which requires user calibration. The isolated BNC connector on the front panel allows access to the internal reference voltage. Access to the corresponding reference voltage adjustment is also provided at the front panel. All calibration and test measurements made by the on-board ADC are based on this reference.

Output Monitor

The output monitor is effectively a 32-channel buffer which provides a test point from each of the 32-output channels.

Analog Multiplexer (MUX)

The 32-channel Analog Mux is used to select one of the analog signals presented by the output monitor.

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Power Converters

Power for the analog outputs is provided by two DC-to-DC Converters which convert the 5 V logic power from the VMEbus into an isolated and regulated ±15 VDC. Only one DC-to-DC Converter is required for the 16-channel option.

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CHAPTER 2

Configuration and Installation

Contents

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Introduction

This chapter describes the installation and configuration of the board. Cable configuration, jumper/switch configuration and board layout are illustrated in this chapter.

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

NOTE: Do not install or remove board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

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Base Address Configuration

There are 29 jumper positions to establish the base address, address mode and access mode. The address mode can be configured for extended, standard or short address space. The base address is determined by the presence (address bit compared to logic zero) or absence (address bit compared to logic one) of a jumper shunt at each appropriate address jumper position. For short, standard and extended address mode configurations, the address jumper positions which must be configured are, respectively, A[7:15], A[7:23] or A[7:31]. The access mode can be configured for supervisory, nonprivileged, or for either supervisory or nonprivileged access.

Jumper functions are illustrated in Figure 2-1 on page 28, Figure 2-2 on page 29 and Figure 2-3 on page 30. Omission of a jumper shorting plug produces a HIGH (logic 1) requirement for the associated control bit; installation of the jumper produces a LOW (logic 0) requirement.

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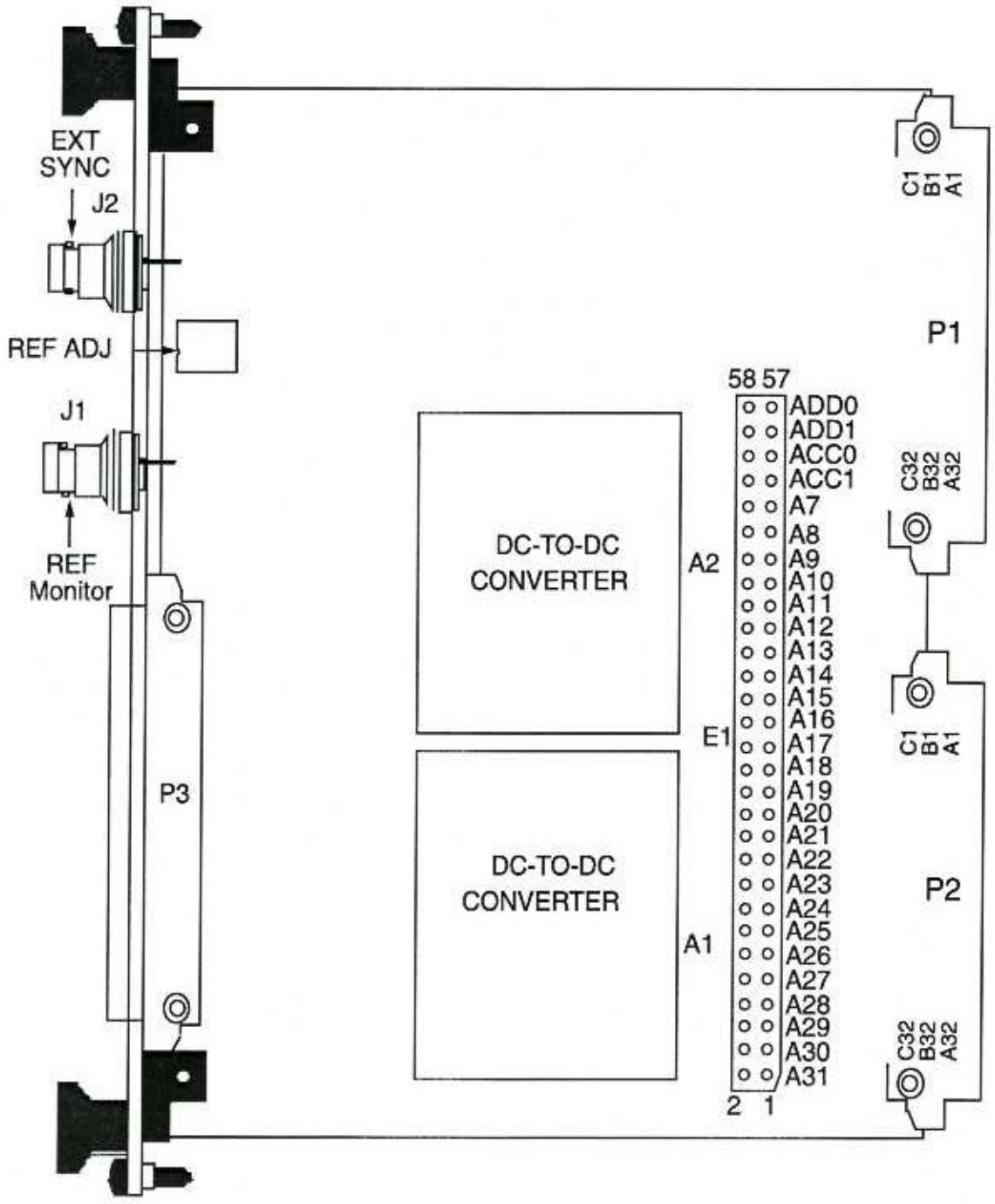


Figure 2-1 Configuration Jumpers and System Connectors

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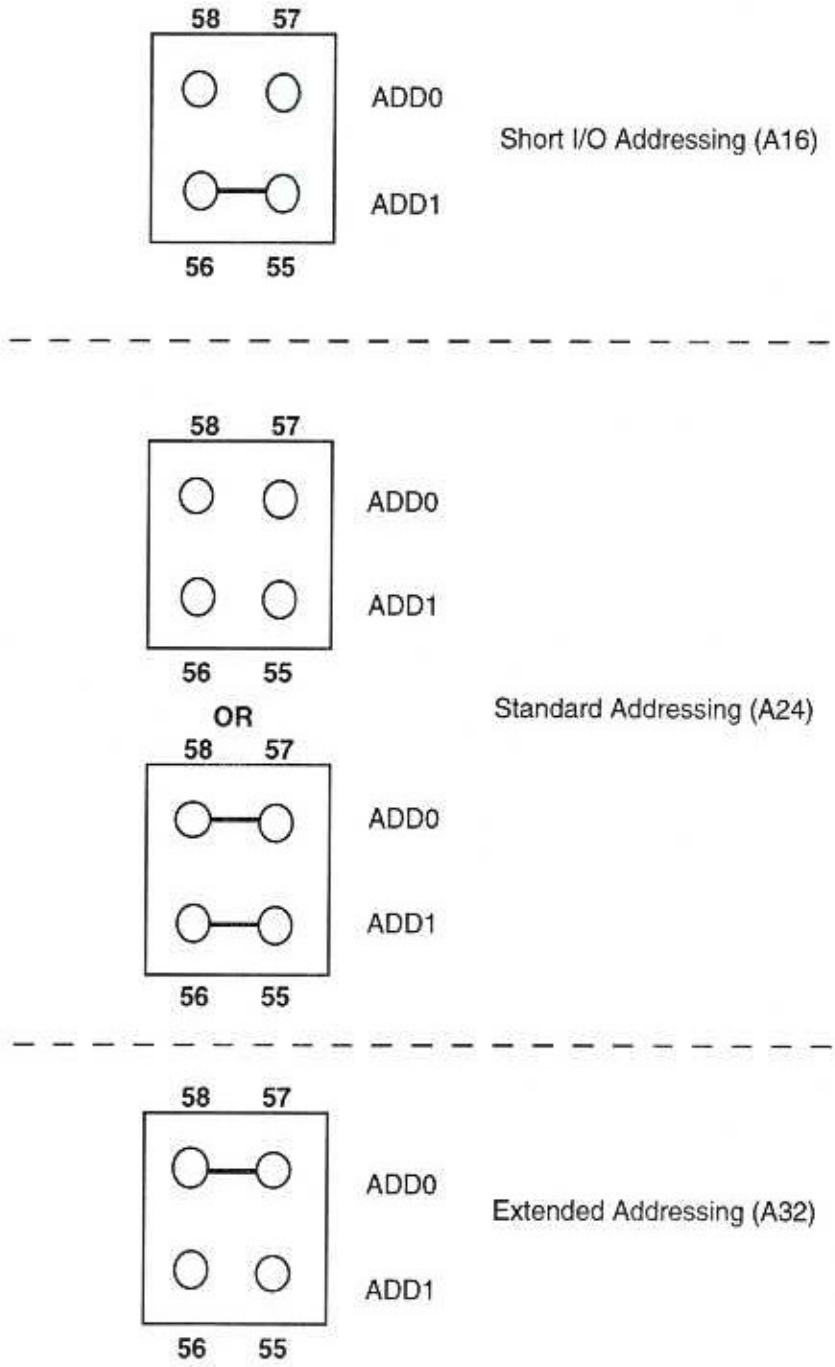


Figure 2-2 Address Mode Configuration

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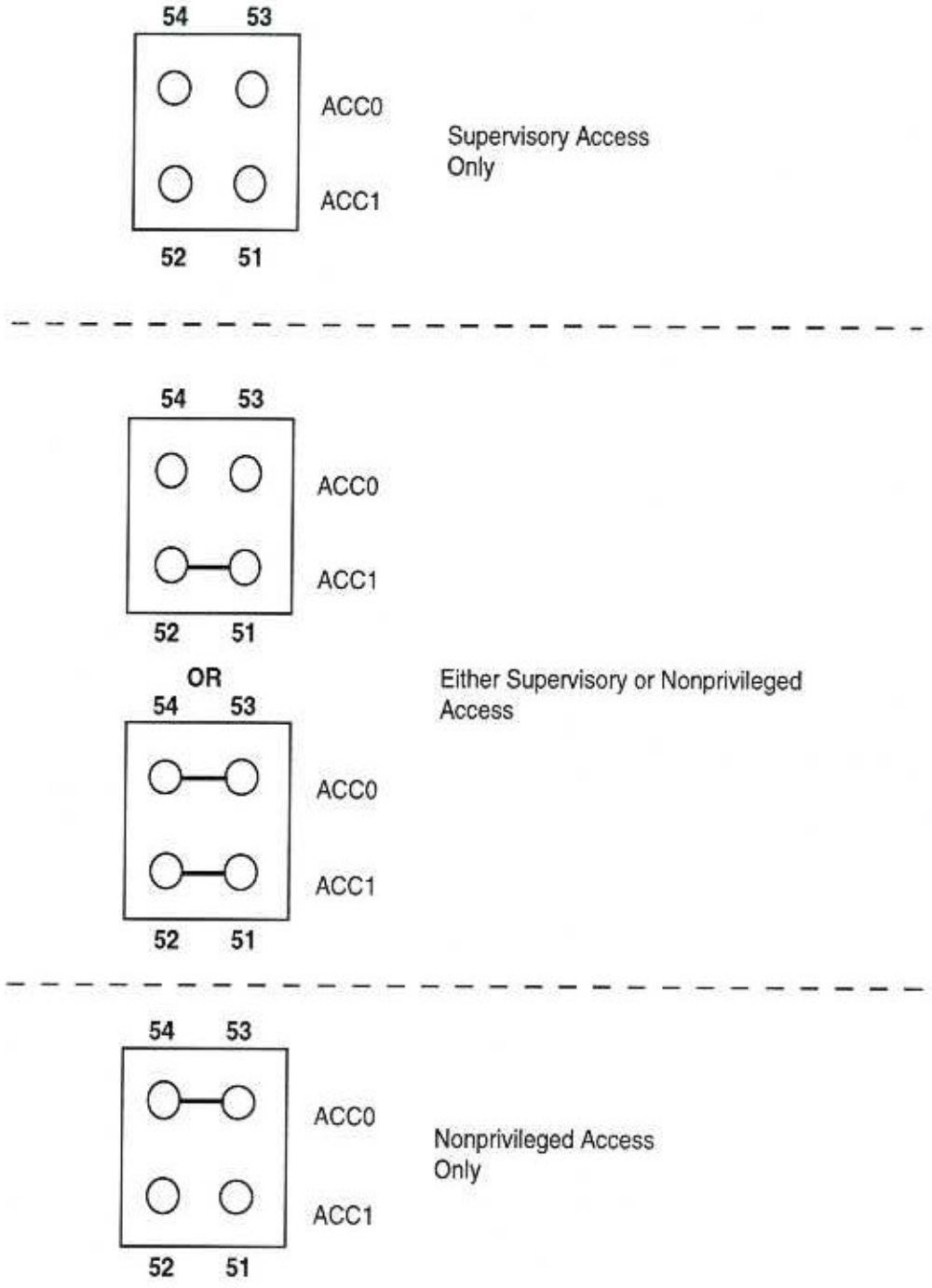


Figure 2-3 Access Mode Configuration

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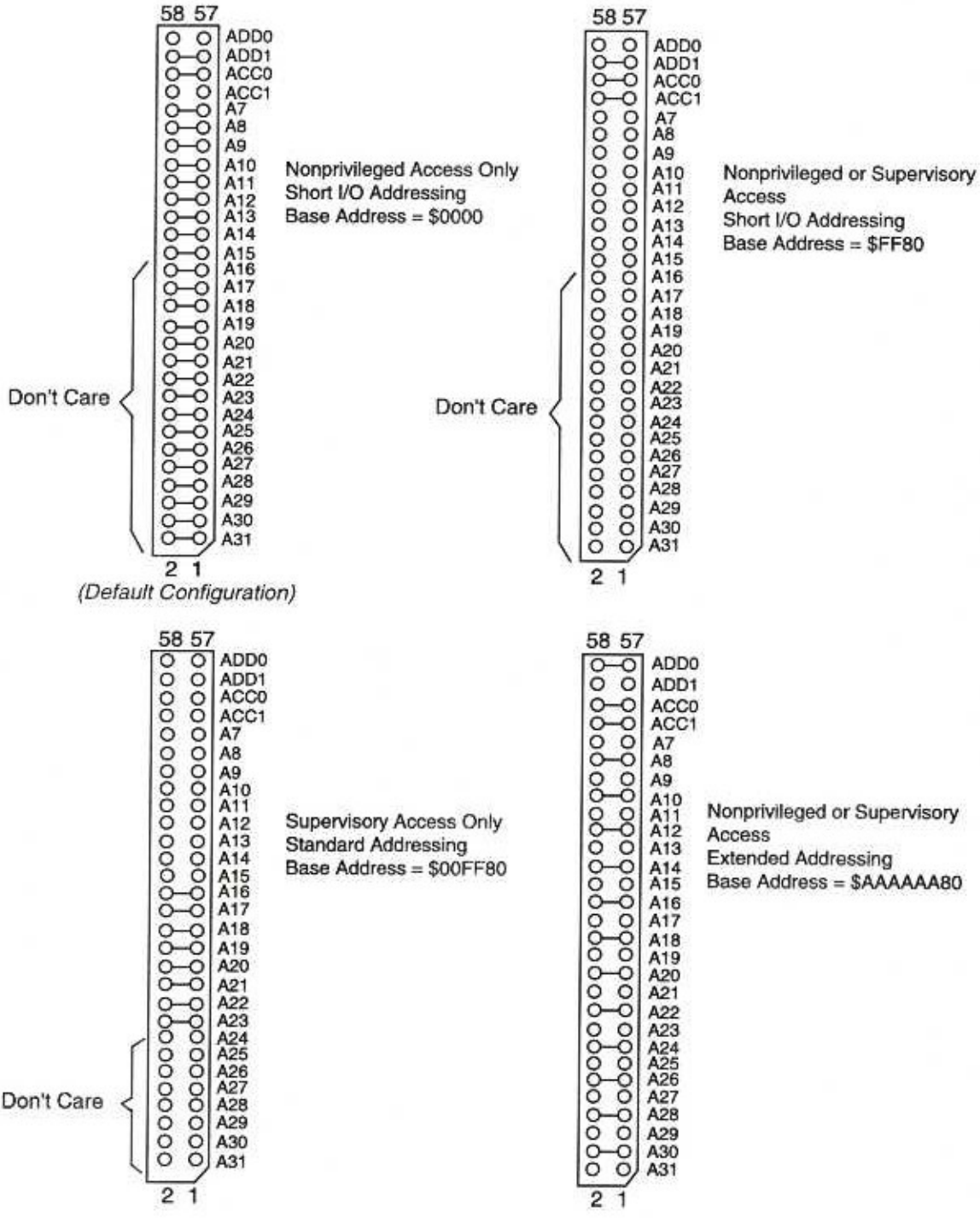


Figure 2-4 Jumper Configuration Examples

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Power Distribution

Power is provided by two DC-to-DC converters. Channels 0 through 15 and the analog logic are powered from one of the two converters, while the remaining output channels (16 through 31) are supplied from the other converter. A 16-channel board will contain only one DC-to-DC converter assembly.

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Front Panel Reference Voltage Access

A front-panel insulated BNC connector is available for monitoring the internal precision reference voltage. The BNC connector (and a pin on P2) is provided for the user to test and calibrate the on-board +10 V reference when the board is in a system. A panel-access potentiometer is provided for calibration adjustments.

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Calibration

The only VMIVME-4140 function which requires manual calibration is the internal precision reference voltage. This voltage can be monitored at the front-panel BNC connector J1, labeled REF Monitor. The adjustment control for the reference voltage is available at the front panel, labeled REF ADJ. After the board has warmed up for 15 minutes, connect a 5 1/2 digit (or better) voltmeter to the REF Monitor connector and adjust the REF ADJ control until the meter indicates +10.000 VDC ±0.001 VDC.

NOTE: To avoid damaging the front panel finish, a plastic-shrouded alignment tool is recommended for adjusting the REF ADJ potentiometer. The board should be removed from the cardcage to reseal the potentiometer.

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Self-Test

After a system reset, the outputs are first placed off-line by the resident controller, and then are calibrated and initialized to 0V. The Self-Test pass/fail status of each channel is reported in two 16-bit Self-Test registers. Self-Test is run automatically after system reset. Self-Test can also be run on a channel-by-channel basis, using the Test Channel Commands, or on all channels under software control. The Self-Test register indicates the results of the self-test.

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System Connections

Table 2-1 on page 37 lists P2 connector pinout, and Table 2-2 on page 38 lists P3 connector pinout. The locations of the system interface connectors are shown in Figure 2-1 on page 28. All 32 analog outputs are available at a single 64-pin DIN front-panel connector (Figure 2-6 on page 38 P3 connector). A return pin is provided for each channel, and all returns are connected internally to a common ground (AGND).

The output drivers are designed to support up to 10 mA loads at all outputs simultaneously, and will tolerate shorts to AGND or ±15 VDC indefinitely. An insulated BNC connector (J1; REF Monitor) provides a front-panel calibration test point, and contains the only adjustable voltage on the board. The use of this connector is described in the section pertaining to calibration.

A second BNC connector on the front panel (J2; EXT SYNC) accepts external TTL-level trigger which can be used to update all DAC outputs simultaneously. The effect of this input is controlled with software. In the external-SYNC operating mode, output values which are written to the data registers are held in intermediate registers until an external trigger occurs. The trigger event causes all intermediate values to appear at their respective outputs simultaneously. The trigger event is software-defined as either a rising edge or a falling edge.

Both the REF Monitor and EXT SYNC connections are duplicated at the P2 connector.

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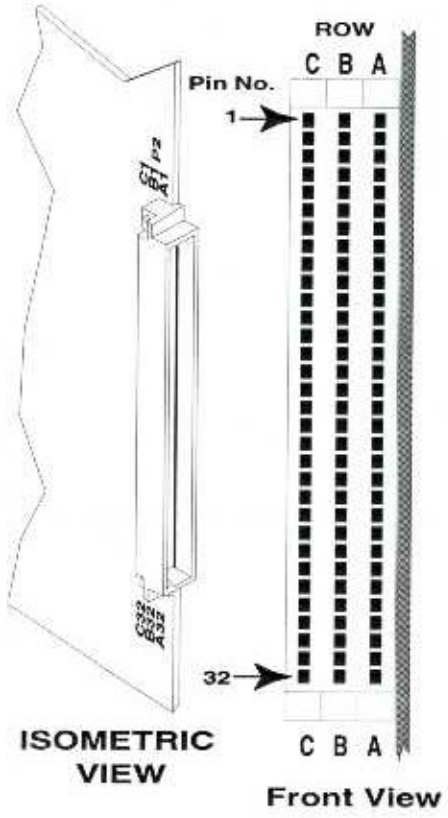
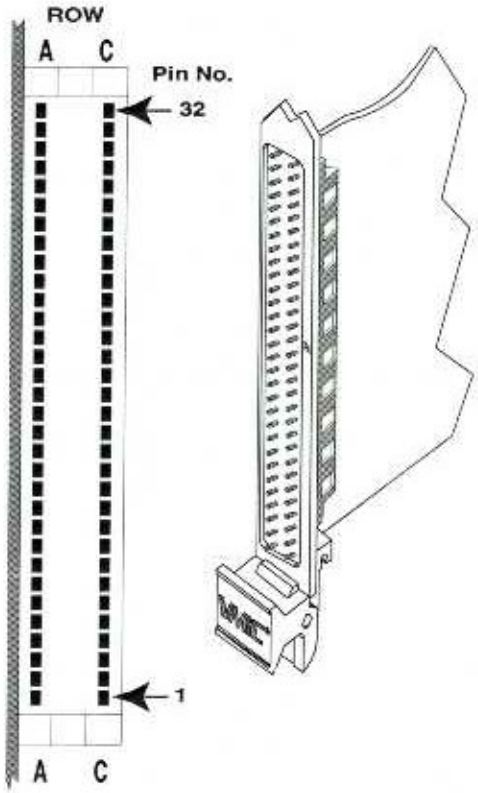


Figure 2-5 P2 Connector

Table 2-1 P2 Pin Layout

Pin#	Row C	Row A
1	REF Monitor, +10.000 VDC	REF Monitor Return
2	N/C	N/C
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16	N/C	N/C
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31	N/C	N/C
32	External SYNC	External SYNC Return
N/C = No Connection		

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Front View

Figure 2-6 P3 Connector

Table 2-2 P3 Pin Layout

Pin#	Row A	Row C
32	Chan 31 Return	Chan 31 Output
31	Chan 30 Return	Chan 30 Output
30	Chan 29 Return	Chan 29 Output
29	Chan 28 Return	Chan 28 Output
28	Chan 27 Return	Chan 27 Output
27	Chan 26 Return	Chan 26 Output
26	Chan 25 Return	Chan 25 Output
25	Chan 24 Return	Chan 24 Output
24	Chan 23 Return	Chan 23 Output
23	Chan 22 Return	Chan 22 Output
22	Chan 21 Return	Chan 21 Output
21	Chan 20 Return	Chan 20 Output
20	Chan 19 Return	Chan 19 Output
19	Chan 18 Return	Chan 18 Output
18	Chan 17 Return	Chan 17 Output
17	Chan 16 Return	Chan 16 Output
16	Chan 15 Return	Chan 15 Output
15	Chan 14 Return	Chan 14 Output
14	Chan 13 Return	Chan 13 Output
13	Chan 12 Return	Chan 12 Output
12	Chan 11 Return	Chan 11 Output
11	Chan 10 Return	Chan 10 Output
10	Chan 09 Return	Chan 09 Output
09	Chan 08 Return	Chan 08 Output
08	Chan 07 Return	Chan 07 Output
07	Chan 06 Return	Chan 06 Output
06	Chan 05 Return	Chan 05 Output
05	Chan 04 Return	Chan 04 Output
04	Chan 03 Return	Chan 03 Output
03	Chan 02 Return	Chan 02 Output
02	Chan 01 Return	Chan 01 Output
01	Chan 00 Return	Chan 00 Output

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CHAPTER 3

Programming

Contents

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Introduction

This section describes the programming operations necessary for controlling the VMIVME-4140 board. The VMEbus slave interface is summarized first and followed by a detailed description of the VMIVME-4140 register set.

A resident controller minimizes VMEbus overhead by performing self-test and autocalibration functions independently, without direct involvement of the VMEbus controller. *Self-Test/Calibration Commands* on page 49 describes the self-test and calibration commands available to the bus.

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VMEbus Slave Interface

Interaction of the board with the VMEbus is directed by a resident controller which is constructed around a Digital Signal Processor (DSP). While performing calibration/ self-test (either power-up, reset or software initiated) or while servicing a test channel command, the DSP is unavailable to the VMEbus.

During this time the Board ID Register (BID) can be polled to detect completion of these tasks, $FFFF will be returned while the DSP is unavailable. When the DSP has completed these tasks, the BID will be read as $2A00 for the 32 channel option or $2A01 for the 16-channel option. At this time all registers and commands are available to the user.

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VMIVME-4140 Registers

Table 3-1 VMIVME-4140 Register Address and Functions

Offset	Function	Access	Size
$000	Board ID Register (BID)	Read*	Byte/Word
$002	Configuration Control Register (CCR)	Read/Write*	Byte/Word
$004	Self-Test Control Register (SCR)	Read/Write*	Byte/Word
$006	Self-Test Status Register 0	Read*	Byte/Word
$008	Self-Test Status Register 1	Read*	Byte/Word
$00A . $01C	Reserved	. . .	- . .
$01D	Software Reset	Write	Byte
$01E	Software SYNC	Write	Byte
$01F	Cal/Test all Channels	Write	Byte
$020	Test Channel 0	Write	Byte
$021	Test Channel 1	Write	Byte
.	.	.	.
$03E	Test Channel 30	Write	Byte
$03F	Test Channel 31	Write	Byte
$040	Output Data Channel 0	Read/Write*	Byte/Word
$042	Output Data Channel 1	Read/Write*	Byte/Word
.	.	.	.
$07C	Output Data Channel 30	Read/Write*	Byte/Word
$07E	Output Data Channel 31	Read/Write*	Byte/Word

NOTE: *While performing a calibration/self-test, the value read from these registers is $FFFF.

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Board ID Register (BID)

The Board ID register is a read-only data register that is not fixed, but changes per *VMEbus Slave Interface* on page 40. The contents of this register identifies the VMIVME-4140.

Table 3-2 Board ID Register Bit Map

Board ID Register (Offset $000) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	0	1	0	1	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	16 CH

Board ID Register Bit Definitions

Bit 00: 16CH - A logical 1 indicates that the board is a VMIVME-4140-100 (16-channel). A logical 0 indicates that the board is a VMIVME-4140-000 (32-channel).

Configuration Control Register (CCR)

The CCR is a read/write register allowing software configuration of the DAC output range and DAC synchronization, and control of the front panel status LED.

Table 3-3 Configuration Control Register Bit Map

Configuration Control Register (Offset $002) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED Off	On Line	REF SEL 1	REF SEL 0	POL SEL	SYNC EN	EXT SYNC	SYNC POL

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Data FMT	0	0	0	0	0	0	EXT SYNC RCVD

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Configuration Control Register Bit Definitions

Bit 15: LED Off - A logical 1 written to this location causes the front panel status LED to be turned off. A logical 0 written to this location causes the front panel status LED to be turned on. If the No Status bit of the SCR is a logical 0, this bit is set to a logical 0 on self-test failure.

Bit 14: On Line - A logical 1 written to this bit location causes the DAC outputs to be connected to the field, i.e. P3 connector. (Default is logical 0).

Bits 13 through 11: REF SEL [1:0], POL SEL - These bits specify the analog output voltage range and polarity, see Table 3-4. (Default for each is logic 0).

Bits 10 through 08: SYNC EN, EXT SYNC, SYNC POL - These bits allow the DACs to be loaded synchronously with either a software driven, or external synchronizing signal as shown in Table 3-5 on page 44. (Default for each is logic 0).

Bit 07: Data FMT - A logical 1 written to this location causes the output data for bipolar ranges to be interpreted as offset binary. When this bit is 0 the output data for bipolar ranges is interpreted as 2's complement. Data for unipolar ranges is unaffected by this bit and is interpreted as binary. (Default is logic 0).

Bit 00: EXT SYNC RCVD - This bit will be set to a logical 1 whenever external trigger is enabled and received. It will be cleared when read.

Table 3-4 Configuration Control Register Bit Definitions (REF SEL and POL SEL)

REF SEL 1	REF SEL 0	POL SEL	Output Voltage range	Data Format
0	0	0	-10 V to + 10 V	2's Complement or Offset Binary
0	0	1	0 V to + 10 V	Binary
0	1	0	-5 V to +5 V	2's Complement or Offset Binary
0	1	1	0 V to +5 V	Binary
1	0	0	-2.5 V to +2.5 V	2's Complement or Offset Binary
1	0	1	0 V to +2.5 V	Binary
1	1	0	0 V	*N/A
1	1	1	0 V	*N/A

*N/A = Not Applicable

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Table 3-5 Configuration Control Register Bit Definitions (SYNC EN, EXT SYNC, SYNC POL)

SYNC EN	EXT SYNC	SYNC POL	Function
0	X	X	DAC is loaded each time output is updated
1	0	X	DAC is loaded by a byte write to offset $01E
1	1	0	DAC is loaded by falling edge on external SYNC input
1	1	1	DAC is loaded by rising edge on external SYNC input
X = Don't Care			

Self-Test Control Register (SCR)

The SCR provides control and status of the self-test and calibration functions, bit definitions are described in Table 3-6.

Table 3-6 Self-Test Control Register Bit Map

Self-Test Control Register (Offset $004) Read/Write, Byte/Word							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CAL RC	Fail	No Status	0	0	0	0	0

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
0	0	0	0	0	0	0	0

Self-Test Control Register Bit Definitions

Bit 15: CAL RC - A logical 1 written to this bit location causes calibration to be run each time the output range is changed. (Default is logic 0).

Bit 14: Fail - A logical 1 in this bit location indicates that on the last execution of calibration/self-test, a failure was detected. Any channels which have failed self-test are indicated by Self-Test Register 1 and Self-Test Register 0.

Bit 13: No Status - A logical 1 written to this location causes the status LED not to be turned on in the event of a calibration/self-test failure. When this bit is a logical 1 the status LED is totally under software control. (Default is logic 0).

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Self-Test Status Registers (SSRs)

The two Self-Test Status Registers (SSRs) provide status from self-test and calibration operations (see Table 3-7 and Table 3-8). Any channels which have failed self-test or have failed to calibrate properly are indicated in these registers.

Table 3-7 Self-Test Status Register 1 Bit Map

Self-Test Status Register 1 (Offset $008) Read, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CHF31	CHF30	CHF29	CHF28	CHF27	CHF26	CHF25	CHF24
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CHF23	CHF22	CHF21	CHF20	CHF19	CHF18	CHF17	CHF16

Table 3-8 Self-Test Status Register 0 Bit Map

Self-Test Status Register 0 (Offset $006) Read, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CHF15	CHF14	CHF13	CHF12	CHF11	CHF10	CHF09	CHF08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CHF07	CHF06	CHF05	CHF04	CHF03	CHF02	CHF01	CHF00

Self-Test Control Register Bit Definitions

Bits 31 through 00: CHF [31:0] - A logical 1 indicates that a failure for that channel has occurred during self-test or that the channel has failed to calibrate properly.

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Output Data Registers

The Output Data registers hold user data representing the desired output voltage. After power-up or reset this data is set to $0000 (0V for 2's complement data format). After calibration/self-test this data is set to $0000 or $0800, whichever represents 0V, depending on the programmed polarity and data format.

Table 3-9 Output Data Registers Format

Offset	Function	Access	Size
$040	Output Data Channel 0	Read/Write	Byte/Word
$042	Output Data Channel 1	Read/Write	Byte/Word
$044	Output Data Channel 2	Read/Write	Byte/Word
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
$07C	Output Data Channel 30	Read/Write	Byte/Word
$07E	Output Data Channel 31	Read/Write	Byte/Word

Table 3-10 Output Data Register Bit Map

Output Data Register Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	D11	D10	D09	D08

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
D07	D06	D05	D04	D03	D02	D01	D00

X = Don't Care

Output Data Registers Bit Definitions

Bits 11 through 00: D[11:0] - Data representing the desired output voltage from negative full-scale to positive full-scale. Table 3-11 on page 47 gives sample output voltages and their respective data representations:

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Data Formats

Bipolar scales encompass both positive and negative output values, and can be expressed in the data registers as either 2's complement or offset binary numbers. Unipolar scales contain only positive output values, and are expressed in the data registers as straight binary numbers. The following sections describe the output data formats.

Bipolar Output Data 2's Complement Format

2's complement data, representing the desired output voltage from negative full-scale to positive full-scale. Table 3-11 gives sample output voltages and their respective data representations:

Table 3-11 Sample Bipolar Output Voltages and DataRepresentations (2's Complement)

Output Voltage	Data Representation
Negative Full-Scale	$X800
Mid-Scale	$X000
Positive Full-Scale	$X7FF

Bipolar Output Data Offset Binary Format

Offset binary data (see Table 3-10 on page 46 for bit map) representing the desired output voltage from negative full-scale to positive full-scale. Table 3-12 gives sample output voltages and their respective data representations:

Table 3-12 Sample Bipolar Output Voltage and Data Representations (Offset Binary)

Output Voltage	Data Representation
Negative Full-Scale	$X000
Mid-Scale	$X800
Positive Full-Scale	$XFFF

Unipolar Output Data Format

Binary data (see Table 3-10 on page 46 for bit map) representing the desired output voltage from 0 to full-scale. Table 3-13 gives sample voltages and their respective data representations.

Table 3-13 Sample Unipolar Output Voltage and Data Representations (Straight Binary)

Output Voltage	Data Representation
Zero Volts (0V)	$X000
Mid-Scale	$X800
Positive Full-Scale	$XFFF

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Software Reset Command

The Software Reset Command allows a board level reset which puts all registers and outputs in their power-up state and the calibration/test is run (see Table 3-14).

Table 3-14 Software Reset Command (Data = Don't Care)

Offset	Function	Access	Size
$01D	Software Reset	Write Only	Byte

Software SYNC Command

The Software SYNC Command allows the update of all DAC outputs to be software synchronized. See CCR description.

Table 3-15 Software SYNC Command (Data = Don't Care)

Offset	Function	Access	Size
$01E	Software SYNC	Write Only	Byte

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Self-Test/Calibration Commands

The following commands allow calibration/self-test to be run on all channels or a limited test to be run on an individual channel. During these tests, a VMEbus read operation to any valid VMIVME-4140 address will yield data of $FFFF. The BID can be polled to indicate completion of the test.

Calibration/Self-Test

Calibration/Self-Test is run automatically on all channels on VMEbus system reset. Calibration/Self-Test can also be run under software control using the CAL/Test command. This test will take all outputs off line, calibrate all ranges and all channels, and run self-test on all channels. The Output Data registers are initialized to 0 V.

Table 3-16 Calibration/Self-Test Bit Map (Data = Don't Care)

Offset	Function	Access	Size
$01F	Cal/Test (All Channels)	Write Only	Byte

Test Channel Commands

The Test Channel Commands can be used to test an individual channel at the currently programmed DAC voltage level. This test may be run with the outputs on or off-line. During this test, the DAC output for the indicated channel is connected to the onboard ADC. The data from the ADC is compared with the contents of the channel's Output Data register. If the difference of these values is outside the specified error tolerance, a failure is indicated in the Self-Test Status registers.

If the DACs are configured to be loaded synchronously, this test should be run only after the output DACs have been loaded and before a new value is written to the channel's output data register, otherwise, an undesired test failure could occur.

If the output voltage range is changed, this test should be run only after the output DAC for the channel under test has been loaded, otherwise, an undesired test failure could occur.

Table 3-17 Test Channel Command Registers (Data = Don't Care)

Offset	Function	Access	Size
$020	Test Channel 0	Write only	Byte
$021	Test Channel 1	Write only	Byte
.	.	.	.
.	.	.	.
.	.	.	.
$03E	Test Channel 30	Write only	Byte
$03F	Test Channel 31	Write only	Byte

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Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com

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Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.

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