VMIVME-9064
INTELLIGENT I/O CONTROLLER

PRODUCT MANUAL

DOCUMENT NO. 500-009064-000 H

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RECORD OF REVISIONS

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G	11/30/95	Entire	95-0682
H	08/19/97	Entire	97-0603

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

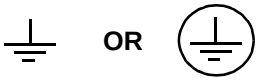
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

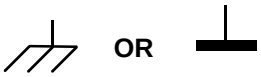
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



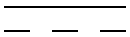
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

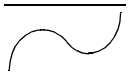


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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1

INTRODUCTION

IN THIS CHAPTER:

SECTION 1 - HOW TO USE THIS MANUAL

This manual provides product specific information concerning the hardware configuration and installation of a VMIVME-9064/32 Intelligent I/O Controller (IIOC). ***Chapter 1 - Introduction*** presents a general overview of IIOC capabilities. ***Chapter 2 - Configuration and Installation*** discusses the default CPU configuration and VMEbus resources used by the IIOC; thus, it should be read by the user prior to installing user-supplied special purpose processors in the VMIVME-9064/32 VMEbus system. The reflective memory jumpering options are also discussed in this chapter. ***Chapter 3 - IIOC Address Maps*** provides a detailed description of the VMEbus addresses and address spaces utilized by the IIOC and those available for use by the user's resources within the IIOC. This chapter should be consulted prior to installing optional user-supplied resources in the IIOC master chassis to ensure compatibility with the IIOC. ***Chapter 4 - Host Communications*** provides a general description of host-to-IIOC communications. This product specific manual complements the ***IIOC Family Instruction Manual***, Document Number 500-009000-000, which provides detailed information and explanations of IIOC operation and functionality.

SECTION 2 - GENERAL OVERVIEW

The VMIVME-9064/32 is an Intelligent I/O Controller (IIOC) implemented on either a Motorola MVME143S-2 or MVME162-202 VMEbus single board computer with VMIC's IIOC firmware. Although the VMIVME-9064/32 IIOC is not installed in a host computer system, VMIC classifies this model as an embedded host IIOC because the host interface is memory-mapped as though the IIOC and host are resident on the same backplane. The external host computer communicates with this IIOC through a reflective memory board (either a VMIVME-5550, VMIVME-5576, or VMIVME-5588).

VMIC's family of IIOCs combine the intelligence to ease integration and simplify maintenance with the power to significantly reduce the impact of real-time I/O on your host computer resources. The IIOCs provide a high-density, high-throughput, low-cost solution to the data acquisition and control problem by off-loading the I/O scanning, scaling computations, and engineering unit conversion tasks from host computational resources.

SECTION 3 - OTHER APPLICABLE DOCUMENTS

Other appropriate documents in reference to the VMIVME-9064/32 are as follows:

IIOC Family Instruction Manual, Document Number 500-009000-000, VME Microsystems International Corporation.

VMIVME-5550 Reflective Memory Board Instruction Manual, Document Number 500-035550-000, VME Microsystems International Corporation.

VMIVME-5576 Reflective Memory Board Instruction Manual, Document Number 500-005576-000, VME Microsystems International Corporation.

VMIVME-5588 Reflective Memory Board Product Manual, Document Number 500-005588-000, VME Microsystems International Corporation.

CHAPTER

2 CONFIGURATION

IN THIS CHAPTER:

SECTION 1 - SYSTEM CONFIGURATION

This chapter describes the capabilities, default configuration, and system configuration options available with the VMIVME-9064/32. Prior to installing the VMIVME-9064/32 in the VMEbus backplane, the user should carefully read this entire chapter to ensure that the reflective memory board is appropriately jumpered for the system configuration required. This chapter discusses all jumpering information required for modifying the factory default configuration.

All of VMIC's IIOCs are based on the industry standard VMEbus. The VMIVME-9064/32 is composed of a single VMEbus CPU board with VMIC's IIOC firmware and a required reflective memory board for host communications. Figure 2-1 on page 2-2 shows a typical VMIVME-9064/32 IIOC VMEbus configuration. Figure 2-2 and Figure 2-3 on page 2-3 show system diagrams of multiple IIOC configurations.

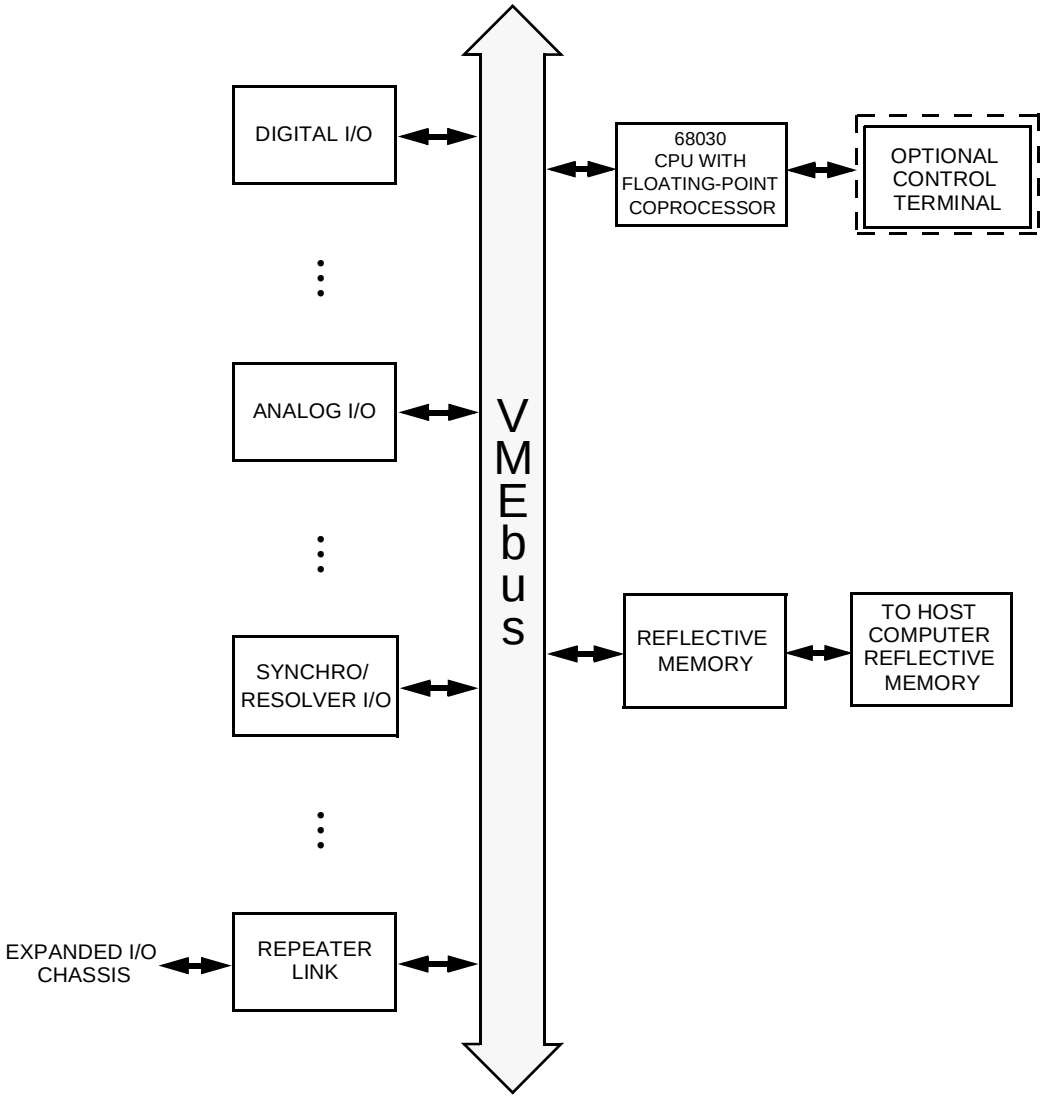

Figure 2-1 VMIVME-9064/32 Reflective Memory Intelligent I/O Controller

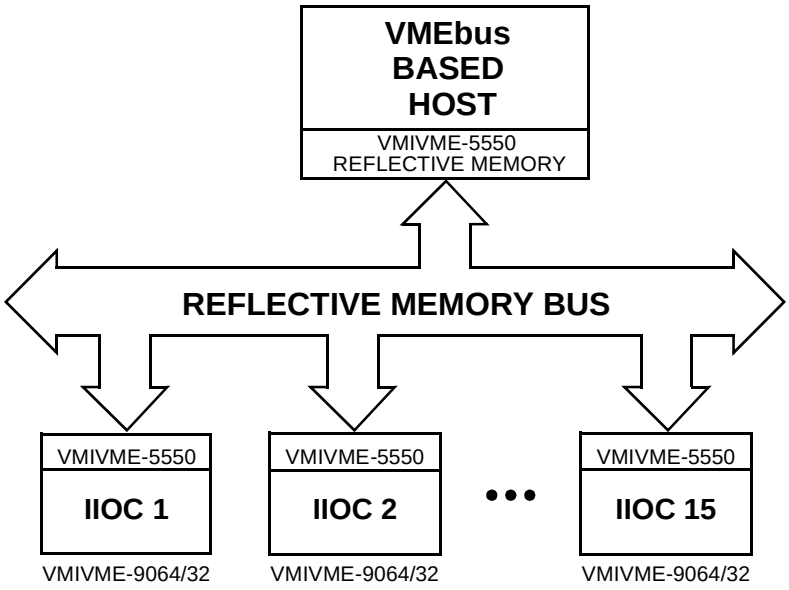

Figure 2-2 VMIVME-9064/32 IIOC Subsystem Block Diagram Using VMIVME-5550 Reflective Memory

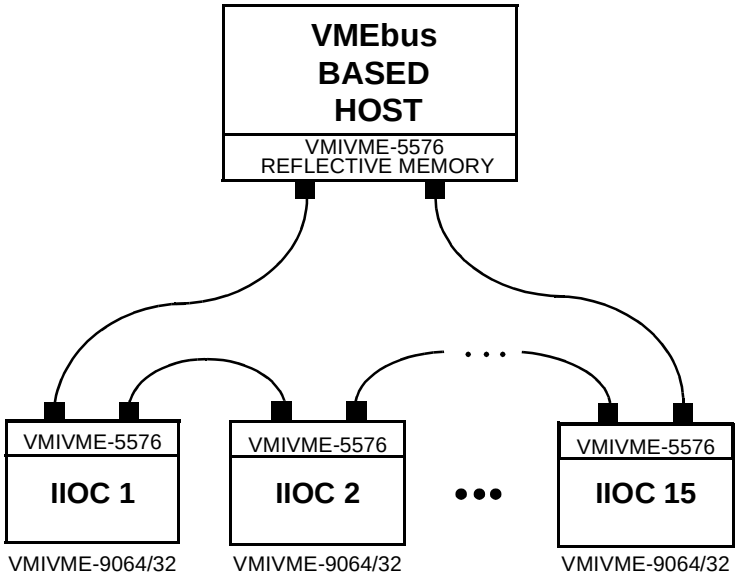

Figure 2-3 VMIVME-9064/32 IIOC Subsystem Block Diagram Using VMIVME-5576 Fiber-Optic Reflective Memory

VMEbus SYSTEM CONTROLLER

The VMIVME-9064/32 IIOC CPU board is installed as system controller in slot 1 of the IIOC VMEbus master chassis (lowest numbered chassis). This board provides a four-level arbiter, a system clock driver, an interrupt acknowledge daisy chain driver, a system reset driver, and a VMEbus clear driver.

The VMIVME-9064/32 comes factory configured as a round-robin arbiter. Round-robin arbitration grants bus masters access to the VMEbus on a rotating priority basis. When the bus is granted to a master on bus request level n, the highest priority for the next arbitration is assigned to bus request n-1. This method of arbitration ensures that all requesting masters are given access to the bus in a timely fashion. This is the preferred VMEbus arbitration method for the VMIVME-9064/32 and should not be modified.

VMIVME-9064/32 REFLECTIVE MEMORY

The host computer system provided by the user must contain a VMEbus for installation of the reflective memory board, such as the VMIVME-5550, VMIVME-5576, or VMIVME-5588. The reflective memory provides the communications path between the host computer system and the VMIVME-9064/32 IIOC. Through the use of memory allocation structures and reflective memory link interrupts, the host computer allocates the IIOC control window and I/O data buffer space. The ***IIOC Family Instruction Manual*** describes the host communications protocol for embedded host IIOCs and the host allocation of memory space for the VMIVME-9064/32 IIOC.

A single host computer may control up to 15 VMIVME-9064/32 IIOCs with a single reflective memory link. Any write access to a reflective memory board (one place only) on one node transmits the data to all other reflective memory on the link without software intervention.

Modifications to the factory default configuration of the reflective memory board may be required during VMIVME-9064/32 integration with the host system. These modifications are discussed in the following sections.

Please refer to the Product Manual of the specific reflective memory board for the locations of the termination resistor SIPs and jumper fields.

REFLECTIVE MEMORY NODE ID

The reflective memory board installed in the IIOC master chassis is factory configured as node 1. The reflective memory installed in the host computer is usually configured as node 0. The node IDs assigned to each reflective memory board must be unique. The following sections discuss specific configuration requirements for VMIVME-5550, VMIVME-5576, and VMIVME-5588 reflective memory boards.

Node 0 is always the reflective memory link arbiter. Due to the hardware implementation of the link arbiter, node 0 always obtains the link every other arbitration cycle. Thus, node 0 should be the node which performs the greatest number of writes to the reflective memory. This is usually true of the host computer.

ADDRESSING OF HOST COMPUTER'S REFLECTIVE MEMORY BOARD

The VMIVME-9064/32 IIOC places no restrictions on the addressing of the reflective memory installed in the host computer. All data passed on the reflective memory link is transmitted to an address offset relative to a reflective memory board base address. Thus, every reflective memory board on the link may be addressed differently to accommodate the system in which it is installed.

INTERRUPT LEVELS AND VECTORS FOR HOST COMPUTER

The reflective memory board installed in the host computer must be initialized by the host if interrupts are to be received from the VMIVME-9064/32. See the Product Manual for the specific reflective memory board installed for interrupt level and vector initialization. The ***IIOC Family Instruction Manual*** discusses the use of interrupts for IIOC communications. No interrupts are sent to the host from the VMIVME-9064/32 unless the IIOC is configured by the host to generate interrupts. The ***IIOC Family Instruction Manual*** describes the host-to-IIOC communications protocol in detail.

VMIVME-9064/32 CPU BOARD

The supported CPU boards are:

- Motorola MVME143S-2
- Motorola MVME162-202

Table 2-1 compares different features of each CPU. In addition to the features in the table, the CPU board contains a full 32-bit master/slave VMEbus interface, VMEbus system controller functions, a serial port for the optional IIOC control terminal, and VMIC IIOC firmware.

Table 2-1 VMIVME-9064/32 CPU Boards

Board	MPU	Speed (MHz)	Local RAM	Dual-Ported RAM	Floating-Point Coprocessor
MOTOROLA MVME143S-2	68030	25	4 MB	YES	YES
MOTOROLA MVME162-202	68040	25	1 MB	YES	NO

The rest of this chapter discusses the factory configuration and all information about the VMIVME-9064/32's CPU and reflective memory boards. The CPUs configured as described in these sections have all system controller functions enabled.

The reflective memory board configuration may need to be altered to adapt to multinode VMIVME-9064/32 system configurations.

CAUTION

SOME OF THE COMPONENTS ON IIOC BOARDS ARE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN A BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

SECTION 2 - MOTOROLA MVME143S-2

MOTOROLA MVME143S-2 FRONT PANEL

Figure 2-4 presents a view of the MVME143S-2 front panel showing the switches, LED indicators, and serial port connector. The functionality of each of these is described in the following sections.

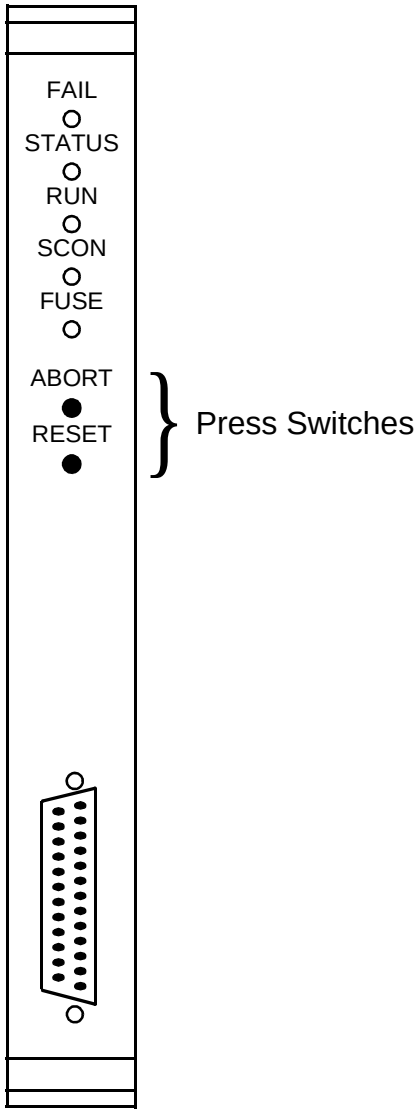

Figure 2-4 MVME143S-2 Front Panel

CONTROL TERMINAL CONNECTION

The IIOC supports an optional control terminal on the RS-232 compatible 25-pin serial port 1 connector at the bottom of the MVME143S-2 front panel. The control terminal provides the user with the capability to monitor and control I/O, initiate IIOC diagnostics, and display IIOC status independent of a host computer. Consult the ***IIOC Family Instruction Manual*** for a detailed description of IIOC control terminal operation.

The control terminal may be any CRT supporting the ANSI-Standard screen commands, such as a Digital Equipment Corporation VT-100 compatible terminal. The following communication setup is required on the control terminal:

- No Parity
- 8 Bits Per Character
- 1 Stop Bit
- 9600 Baud
- Asynchronous Protocol

Table 2-2 shows the RS-232 compatible signals supported by the 25-pin connector on serial port 1. Input and output columns in this table refer to the MVME143S-2 board. The terminal used must not drive signals identified as outputs in the table. All signals in the column labeled "REQUIRED" must be supported by the terminal.

Table 2-2 MVME143S-2 Control Terminal Port Pin Definition

25-pin Connector	Signal	Input	Output	Required	Description
1					Not Used
2	TXD1		X	X	Transmit Data
3	RXD1	X		X	Receive Data
4	RTS1		X		Request to Send
5	CTS1	X			Clear to Send
6	DSR1	X		X	Data Set Ready
7	GND			X	Signal GND
8	DCD1	X			Receive Line Signal Detector
9-19					Not Used
20	DTR1		X	X	Data Terminal Ready
21-25					Not Used

FUNCTION SWITCHES

The MVME143S-2 front panel contains two function switches. These two press switches are labeled ABORT and RESET.

Please exercise each switch prior to installing the CPU in a VMEbus backplane in order to detect mechanical damage to the switches that may have occurred during transport.

The ABORT Function Switch

The ABORT switch is debounced and brought into the PI/T pin H3 which may be programmed to interrupt the MPU on level 7.

The RESET Function Switch

If the front panel RESET switch is enabled (jumper J4), pressing the switch resets all on-board devices including the MPU and asserts SYSRESET if the MVME143S-2 is the system controller.

LED STATUS INDICATORS

The MVME143S-2 front panel LED status indicators give an indication of the state of the MPU and the type of access being performed by the CPU. The following sections give a brief description of these indicators.

FAIL Status LED

FAIL is red when the BRDFAIL control bit is high or when VMEbus SYSFAIL is low while the MVME143S-2 is system controller.

STATUS LED

STATUS is yellow when reset is true or when the MPU STATUS line is low.

RUN Status LED

RUN is green when the MPU address strobe is on.

SCON Status LED

SCON is green when the MVME143S-2 is configured as system controller.

FUSE Status LED

FUSE is red when any of the three fuses are blown (+5 V, +12 V, -12 V).

DEFAULT JUMPER SETTINGS

The following table indicates the factory default jumper settings for the Motorola MVME143S-2 board as installed in the VMIVME-9064/32.

The numbers shown in the Default Configuration column of the Default Jumper Settings tables indicate that a jumper is installed connecting these jumper pins. An absence of pin numbers in this column indicates that no jumpers are installed in that jumper field.

Table 2-3 Default Jumper Settings for VMIVME-9064/32 MVME143S-2

Jumper	Description	Default Configuration
E1-E3	On-chip cache PMMU control select normal	
J1	System controller (yes)	1-2
J2	VMEbus arbiter mode (round robin)	1-2
J3	VMEbus requester mode (fairness off)	
J4	VMEbus request level 3	1-2 5-6 7-8 9-11 10-12
J5	Global timeout select (64 µs)	1-2
J6	VMEbus request level 3	5-6
J7	EPROM size select (64 K x 8)	2-4 5-7 13-15 14-16
J8	EPROM size select (64 K x 8)	2-4 5-7 13-15 14-16
J9	Reset switch (enabled)	1-2
J10	Serial clock select (1.23 MHz)	1-2
J11	Local timeout (2 ms)	1-2
J12	VMEbus interrupt handler (enabled)	1-2 3-4 5-6 7-8 9-10 11-12 13-14
J13	EPROM address map select	1-2

Table 2-3 Default Jumper Settings for VMIVME-9064/32 MVME143S-2 (Continued)

Jumper	Description	Default Configuration
J15	SCC RTXCA source select (crystal)	1-2
J16	SCC RTXCB source select (crystal)	1-2
J17	Serial port 1 configuration (DCE)	1-2 3-4 5-6 7-8 9-10 11-12 13-14
J19	Serial ports 1 and 2 configuration (DCE)	1-2 3-4 5-6 7-8 9-10 11-12 13-14 15-16 17-18 19-20
J20	Serial ports 1 and 2 configuration (DCE)	1-2 3-4 5-6 7-8 9-10 11-12 13-14 15-16 17-18 19-20

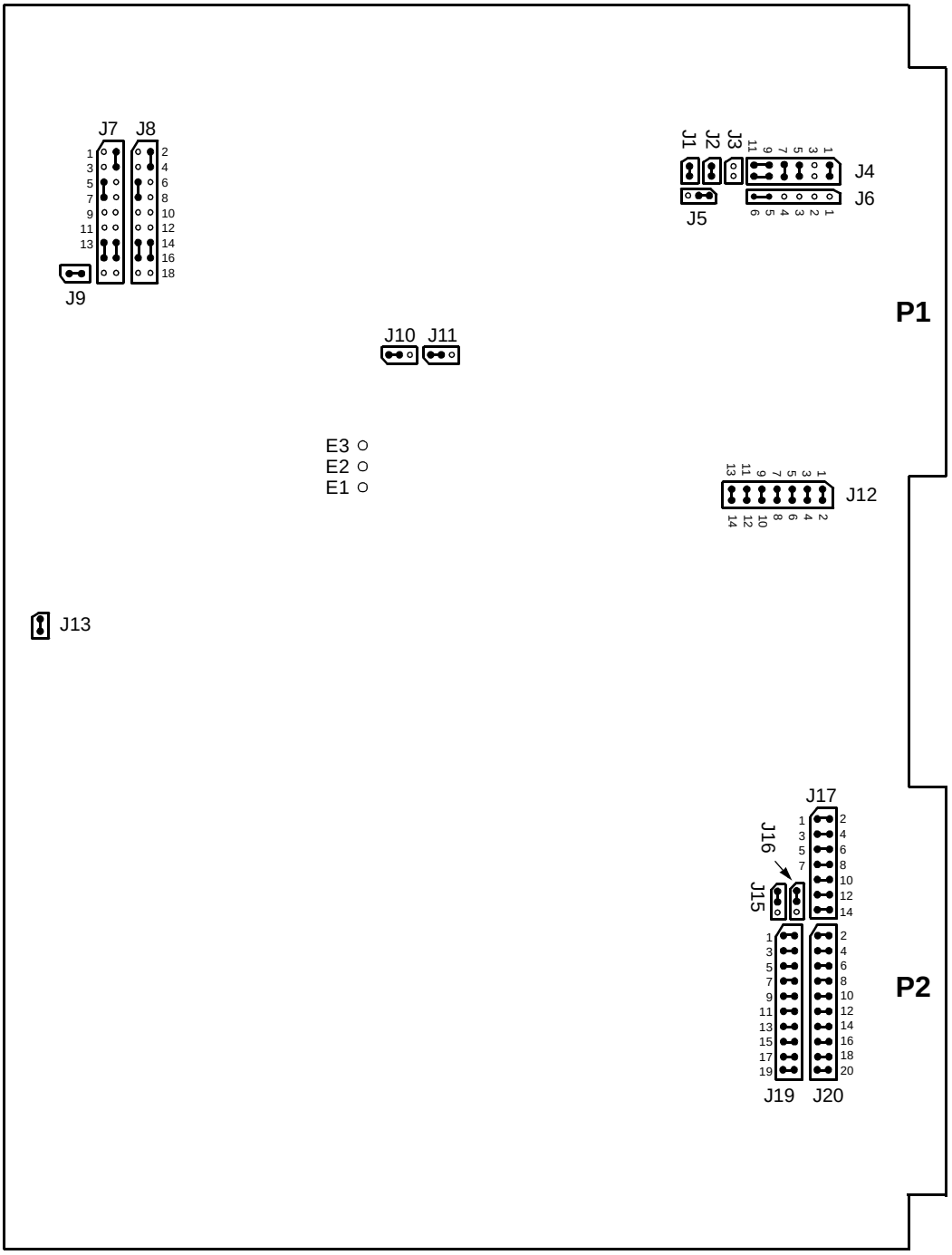

Figure 2-5 MVME143S-2 Jumper Field Locations

REFLECTIVE MEMORY CONFIGURATION FOR MVME143S-2

The reflective memory boards need to be configured differently for each type of CPU board. This section shows the reflective memory configuration to be used with the MVME143S-2.

The numbers shown in the Default Configuration column of the Default Jumper Settings tables indicate that a jumper is installed connecting these jumper pins. An absence of pin numbers in this column indicates that no jumpers are installed in that jumper field.

VMIVME-5550

This section describes the jumper locations for the VMIVME-5550 with a part number of 332-035550-XXX. Refer to the VMIVME-5550 Instruction Manual for location of SIPs and jumper fields.

Table 2-4 Default Jumper Settings for 256 Kbyte VMIVME-5550

Jumper	Description	Default Configuration
J1	On-Board Memory	1-2
J2	On-Board Memory	1-2
J3	On-Board Memory	1-2
J4	On-Board Memory	1-2
J6	VMEbus Standard Base Address (AP20)	1-2
J7	VMEbus Standard Base Address (AP21)	1-2
J8	VMEbus Standard Base Address	1-2 3-4 5-6 7-8 9-10 11-12 13-14 15-16
J9	Number of Nodes	
	Board Node ID Number	9-10 11-12 13-14
J10	Address Modifier (Supervisory Access Only)	
J11	VMEbus Addressing Mode (Standard Addressing)	
J12	Link Transfer Rate (20 Mbyte/second)	1-2

Table 2-4 Default Jumper Settings for 256 Kbyte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J13	Link Transfer Rate (20 Mbyte/second)	1-2
J14	SRAM Decode	1-2
J15	SRAM Decode	1-2
J16	Link Reset (Mode B: Reset Node Only)	1-2
J17	Extended Address Lines A31-A24 (0xFB)	11-12
J18	Memory Selection	
J19	Memory Selection	
J20	Link Reset (Mode B: Reset Node Only)	

Table 2-5 Default Jumper Settings for 512 Kbyte VMIVME-5550

Jumper	Description	Default Configuration
J1	On-Board Memory	1-2
J2	On-Board Memory	1-2
J3	On-Board Memory	
J4	On-Board Memory	1-2
J6	VMEbus Standard Base Address (AP20)	1-2
J7	VMEbus Standard Base Address (AP21)	1-2
J8	VMEbus Standard Base Address	1-2 5-6 7-8 9-10 11-12 13-14
J9	Number of Nodes	
	Board Node ID Number	9-10 11-12 13-14
J10	Address Modifier (Supervisory Access Only)	
J11	VMEbus Addressing Mode (Standard Addressing)	
J12	Link Transfer Rate (20 Mbyte/second)	1-2
J13	Link Transfer Rate (20 Mbyte/second)	1-2
J14	SRAM Decode	1-2
J15	SRAM Decode	1-2
J16	Link Reset (Mode B: Reset Node Only)	1-2
J17	Extended Address Lines A31-A24 (0xFB)	11-12
J18	Memory Selection	

Table 2-5 Default Jumper Settings for 512 Kbyte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J19	Memory Selection	
J20	Link Reset (Mode B: Reset Node Only)	

Table 2-6 Default Jumper Settings for 1 Mbyte VMIVME-5550

Jumper	Description	Default Configuration
J1	On-Board Memory	1-2
J2	On-Board Memory	
J3	On-Board Memory	
J4	On-Board Memory	1-2
J6	VMEbus Standard Base Address (AP20)	1-2
J7	VMEbus Standard Base Address (AP21)	1-2
J8	VMEbus Standard Base Address	3-4 5-6 7-8 9-10 11-12
J9	Number of Nodes	
	Board Node ID Number	9-10 11-12 13-14
J10	Address Modifier (Supervisory Access Only)	
J11	VMEbus Addressing Mode (Standard Addressing)	
J12	Link Transfer Rate (20 Mbyte/second)	1-2
J13	Link Transfer Rate (20 Mbyte/second)	1-2
J14	SRAM Decode	1-2
J15	SRAM Decode	1-2
J16	Link Reset (Mode B: Reset Node Only)	1-2
J17	Extended Address Lines A31-A24 (0xFB)	11-12
J18	Memory Selection	
J19	Memory Selection	
J20	Link Reset (Mode B: Reset Node Only)	

VMIVME-5576

The following tables indicate the factory default jumper settings for the VMIVME-5576 reflective memory board as installed in the VMIVME-9064/32. Three configurations are defined in the following tables. These correspond to the three memory size options of 256 Kbytes, 512 Kbytes, and 1 Mbyte. Refer to the VMIVME-5576 Instruction Manual for location of SIPs and jumper fields.

Table 2-7 Default Jumper Settings for a 256 Kbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	1-2
J2	Address Pass Through Field - Depth 2	1-2
J3	Mask Field (INT0 transfer error interrupt enabled)	1-2
J4	Extended Address Jumper Field A31-A24 (0xFB)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	1-2 3-4 5-6 7-8 9-10 11-12 13-14 15-16
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-8 Default Jumper Settings for a 512 Kbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	1-2
J2	Address Pass Through Field - Depth 2	1-2
J3	Mask Field (INT0 transfer error interrupt enabled)	1-2
J4	Extended Address Jumper Field A31-A24 (0xFB)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	1-2 5-6 7-8 9-10 11-12 13-14
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-9 Default Jumper Settings for a 1 Mbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	
J2	Address Pass Through Field - Depth 2	
J3	Mask Field (INT0 transfer error interrupt enabled)	
J4	Extended Address Jumper Field A31-A24 (0xFB)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	5-6 7-8 9-10 11-12
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-10 Default Jumper Settings for a 256 Kbyte VMIVME-5588 Motorola 143

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:OUT A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:IN A18:IN
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-11 Default Jumper Settings for a 512 Kbyte VMIVME-5588 Motorola 143

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:OUT A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:IN A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-12 Default Jumper Settings for a 1 Mbyte VMIVME-5588 Motorola143

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:OUT A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-13 Default Jumper Settings for a 2 Mbyte VMIVME-5588 Motorola 143

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:OUT A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:OUT A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-14 Default Jumper Settings for a 4 Mbyte VMIVME-5588 Motorola 143

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:OUT A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:OUT A20:OUT A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

SECTION 3 - MOTOROLA MVME162-202

MOTOROLA MVME162-202 FRONT PANEL

Figure 2-6 presents a view of the MVME162-202 front panel showing the switches, LED indicators, and serial port connector. The functionality of each of these is described in the following sections.

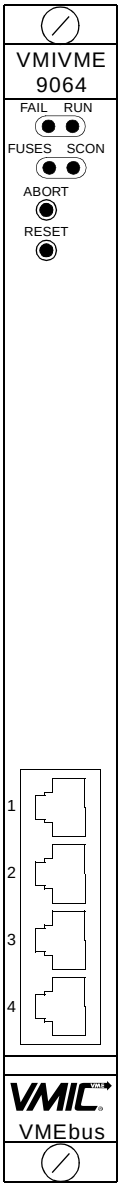

Figure 2-6 MVME162-202 Front Panel

CONTROL TERMINAL CONNECTION

The IIOC supports an optional RJ45 control terminal connected to serial port 1 on the MVME162-202 front panel. The control terminal provides the user with the capability to monitor and control I/O, initiate IIOC diagnostics, and display IIOC status independent of a host computer. Consult the **IIOC Family Instruction Manual** for a detailed description of IIOC control terminal operation.

The control terminal may be any CRT supporting the ANSI-Standard screen commands, such as a Digital Equipment Corporation VT-100 compatible terminal. The following communication setup is required on the control terminal:

- No Parity
- 8 Bits Per Character
- 1 Stop Bit
- 9600 Baud
- Asynchronous Protocol

Table 2-15 shows the RJ45 compatible signals supported by the 8-pin RJ45 adapter for serial port 1.

Table 2-15 MVME162-202 Control Terminal Port Pin Definition

Pin	Signal	Description
1	DCD	Data Carrier Detect
2	RTS	Request to Send
3	SG	Signal Ground
4	TXD	Transmit Data
5	RXD	Receive Data
6	SG	Signal Ground
7	CTS	Clear to Send
8	DTR	Data Terminal Ready

FUNCTION SWITCHES

The MVME162-202 front panel contains two function switches. These two press switches are labeled ABORT and RESET.

Please exercise each switch prior to installing the CPU in a VMEbus backplane in order to detect mechanical damage to the switches that may have occurred during transport.

The ABORT Function Switch

The ABORT switch interrupts normal VMIVME-9064/32 operation, temporarily halts the processor, and performs a register dump to the CRT.

The RESET Function Switch

Pressing the RESET switch resets all on-board devices and asserts SYSRESET if the MVME162-202 is the system controller.

LED STATUS INDICATORS

The MVME162-202 front panel LED status indicators give an indication of the state of the MPU and the type of access being performed by the CPU. The following sections give a brief description of these indicators.

FAIL Status LED

FAIL is red when the BRDFAIL* signal line is active or when the processor is halted.

RUN Status LED

RUN is green (or amber) when the local bus TIP* signal line is low. This indicates one of the local bus masters is executing a local bus cycle.

FUSES Status LED

FUSES is green when +5 Vdc, +12 Vdc, and -12 Vdc power is available to the IP connectors. This LED should always be green.

SCON Status LED

SCON is green when the MVME162-202 is configured as system controller. This LED should always be green.

DEFAULT JUMPER SETTINGS

The following table indicates the factory default jumper settings for the Motorola MVME162-202 board as installed in the VMIVME-9064/32.

Figure 2-7 on page 2-28 is a jumper field location diagram for the MVME162-202.

The numbers shown in the Default Configuration column of the Default Jumper Settings tables indicate that a jumper is installed connecting these jumper pins. An absence of pin numbers in this column indicates that no jumpers are installed in that jumper field.

Table 2-16 Default Jumper Settings for MVME162-202

Jumper	Description	Default Configuration
J1	VMEbus System Controller	1-2
J11	EPROM Memory Map Enabled	1-2 3-4 5-6 9-10 11-12 13-14 15-16
J12	EPROM Configuration	5-6 8-10 9-11
J13	Primary Power Source	1-3 2-4
J14	On-Board SCSI Bus Terminator	1-2

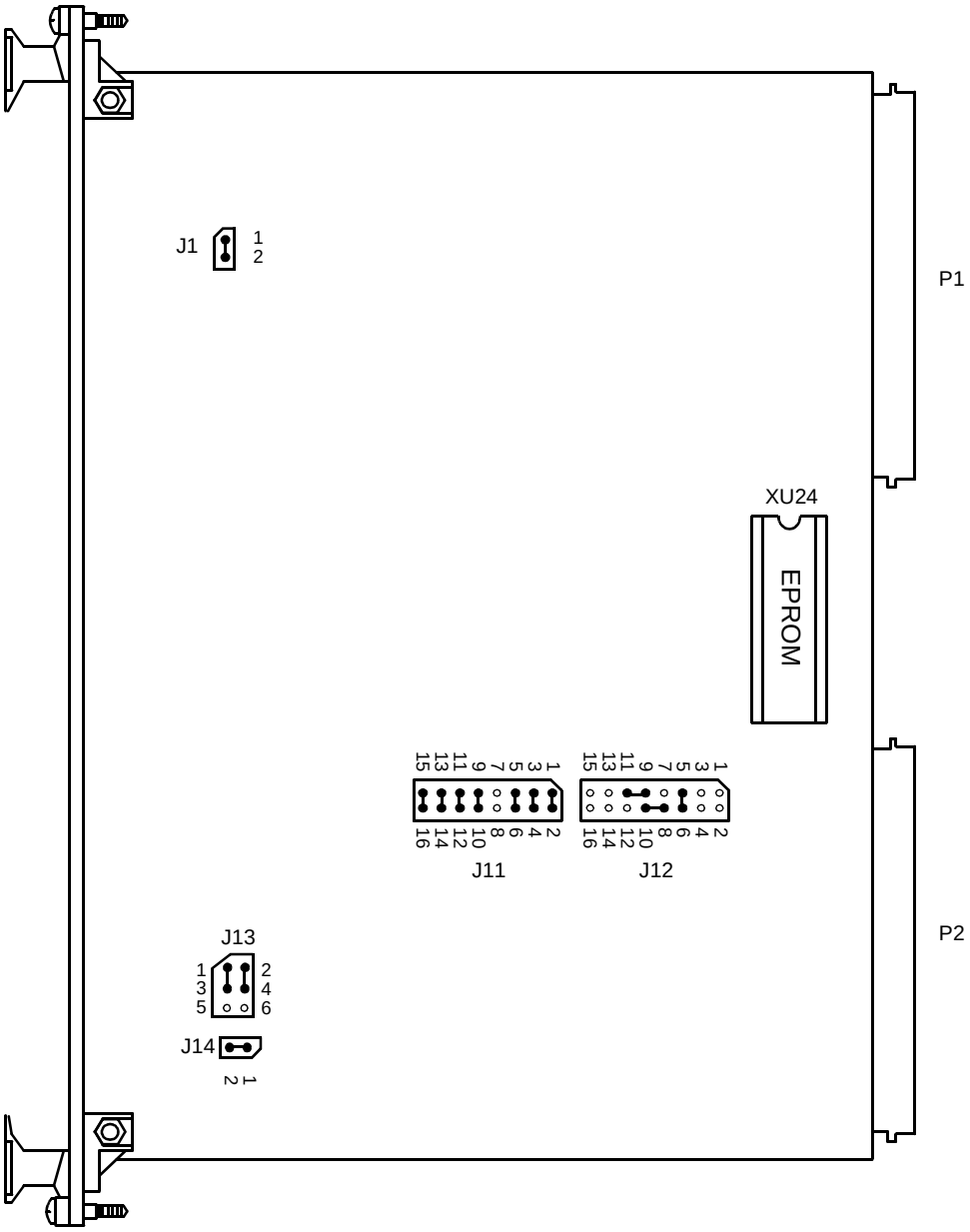

Figure 2-7 MVME162-202 Jumper Field Locations

REFLECTIVE MEMORY CONFIGURATION FOR MVME162-202

The reflective memory boards need to be configured differently for each type of CPU board. This section shows the reflective memory configuration to be used with the MVME162-202.

VMIVME-5550

The VMIVME-5550 reflective memory board with the VMIVME-9064/32 must be configured as shown in Table 2-17.

Table 2-17 Reflective Memory Configuration

Option	Related Jumper Field(s)
Node ID = 1	J9
Maximum Node Number on link = Node ID of last VMIVME-9064/32	J9
Address Modifier = Supervisory	J10
VMEbus Addressing Mode = Extended	J11
Speed Selection = 20 Mbyte/s for cable length less than or equal to 50 ft.	J12, J13
Link Reset Mode = Sender Mode (Mode D)	J20, J16
Extended Address = 7B	J17

Refer to the VMIVME-5550 Instruction Manual for location of jumper fields.

VMIVME-5576

The following tables indicate the factory default jumper settings for the VMIVME-5576 reflective memory board as installed in the VMIVME-9064/32. Three configurations are defined in the following tables. These correspond to the three memory size options of 256 Kbytes, 512 Kbytes, and 1 Mbyte. Refer to the VMIVME-5576 Instruction Manual for location of SIPs and jumper fields.

Table 2-18 Default Jumper Settings for a 256 Kbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	1-2
J2	Address Pass Through Field - Depth 2	1-2
J3	Mask Field (INT0 transfer error interrupt enabled)	1-2
J4	Extended Address Jumper Field A31-A24 (0x7B)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	1-2 3-4 5-6 7-8 9-10 11-12 13-14 15-16
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-19 Default Jumper Settings for a 512 Kbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	1-2
J2	Address Pass Through Field - Depth 2	1-2
J3	Mask Field (INT0 transfer error interrupt enabled)	1-2
J4	Extended Address Jumper Field A31-A24 (0x7B)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	1-2 5-6 7-8 9-10 11-12 13-14
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-20 Default Jumper Settings for a 1 Mbyte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	
J2	Address Pass Through Field - Depth 2	
J3	Mask Field (INT0 transfer error interrupt enabled)	
J4	Extended Address Jumper Field A31-A24 (0x7B)	11-12
J5	Link Speed Selection (6.2 Mbyte)	
J6	Spare	None
J7	Standard Address Jumper Field (000000)	5-6 7-8 9-10 11-12
J8	Address Mode (SUPR)	
J9	Board Node ID Selection (1)	3-4 5-6 7-8 9-10 11-12 13-14 15-16
J10	Standard/Extended Address Selection (Extended)	1-2

Table 2-21 Default Jumper Settings for a 256 Kbyte VMIVME-5588 Motorola 162

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:IN A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:IN A18:IN
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-22 Default Jumper Settings for a 512 Kbyte VMIVME-5588 Motorola 162

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:IN A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:IN A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-23 Default Jumper Settings for a 1 Mbyte VMIVME-5588 Motorola 162

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:IN A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:IN A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-24 Default Jumper Settings for a 2 Mbyte VMIVME-5588 Motorola 162

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:IN A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:IN A20:OUT A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

Table 2-25 Default Jumper Settings for a 4 Mbyte VMIVME-5588 Motorola 162

Jumper	Description	Default Configuration
E1	Extended Address Field	A31:IN A30:OUT A29:OUT A28:OUT A27:OUT A26:IN A25:OUT A24:OUT
E2	Extended Address Jumper	IN
E3	Address Modifier Select	OUT
E4	Standard Address Field	A23:IN A22:IN A21:OUT A20:OUT A19:OUT A18:OUT
E5	Link SYSRESET Enable	OUT
E6	Fast Field	IN
E7	Mask Field	OUT
E8	Optical Relay Bit P2 Disconnect	OUT
E9	Board Node ID Field (Node 1)	ID7:IN ID6:IN ID5:IN ID4:IN ID3:IN ID2:IN ID1:IN ID0:OUT
E10	Loop-Back Enable	IN

CHAPTER

3

IIOC ADDRESS MAPS

IN THIS CHAPTER:

This chapter defines the address spaces utilized by the IIOC. The user must ensure that special purpose resources (user-provided processors or special I/O) installed in IIOC chassis are not configured to respond to the spaces utilized by the IIOC. The host system, including all VMEbus devices, must avoid the use of the address spaces listed in the table below:

Table 3-1 IIOC Address Space

Address Range	VMEbus Address Space	IIOC Utilization
0x0000 - 0xE3FF	Short NP	I/O Boards
0xE400 - 0xEFFF	Short S	Reserved
0x000000 - 0x0FFFFF	Standard S	Reflective Memory (CPU-33)
0x7B000000 - 0x7B0FFFFF	Extended S	Reflective Memory (Motorola 162)
0xF40C0000 - 0xF40FFFFF	Extended S/NP	CPU-33 Shared RAM
0xFB000000 - 0xFB0FFFFF	Extended S	Reflective Memory (Motorola 143)

These spaces are reserved for IIOC operation and host to IIOC communications. In the table, “NP” stands for nonprivileged and “S” stands for supervisory. The following sections describe the IIOC’s use of each of the reserved spaces.

SECTION 1 - SHORT I/O BOARD ADDRESS SPACE

The VMIVME-9064/32 utilizes memory-mapping to determine the I/O board type and location for all IIOC supported I/O boards. This IIOC uses the VMEbus short I/O (A16) nonprivileged space for this purpose. The user must ensure that no user-supplied I/O devices installed in the IIOC respond to the VMEbus nonprivileged short I/O space. The user may utilize the VMEbus short I/O supervisory space, except for the 3072-byte range from 0xE400 through 0xEFFF, for host system or user-supplied I/O devices. Refer to the ***IIOC Family Instruction Manual*** for detailed address information.

SECTION 2 - ADDRESS SPACE FOR FUTURE ENHANCEMENT

A 3072-byte space beginning at location 0xE400 in the VMEbus short supervisory I/O space is reserved for future enhancements of the IIOC.

SECTION 3 - REFLECTIVE MEMORY ADDRESS SPACE

The reflective memory address space is the address space occupied by the reflective memory board installed in the IIOC master chassis. The VMIVME-9064/32 requires a section of this memory space for memory allocation structures initialized by the host computer. The ***IIOC Family Instruction Manual*** describes these structures in detail. The host has complete control of the allocation of the rest of this memory space and may allocate portions of it for use by user-supplied masters installed in the IIOC system.

SECTION 4 - SHARED GLOBAL MEMORY ADDRESS SPACE

The IIOC CPU dual-port memory is accessed at a base address of 0xF4000000 in the VMEbus extended (A32) supervisory or nonprivileged data address space. Table 3-2 shows the IIOC CPU global memory access window for the supported CPUs. Thus, user-supplied resources installed in the IIOC system must have no devices which access or respond to this range of addresses in the specified data space.

Table 3-2 IIOC Global Memory Access Windows

CPU	Window
MVME143S-2	0xC0000 - 0xFFFFF
MVME162-202	0xC0000 - 0xFFFFF

CHAPTER

4

HOST COMMUNICATIONS

IN THIS CHAPTER:

The VMIVME-9064/32 IIOC implements a memory-mapped control window and reflective memory link interrupts for host communications and control. The control window and all commands implemented by the IIOC are described in detail in the ***IIOC Family Instruction Manual***. The host defines the location of the VMIVME-9064/32 control window by initializing node allocation structures on the reflective memory and issuing an interrupt to each IIOC. The host then controls the IIOCs by writing commands and command parameters to the control windows and generating interrupts to the IIOC nodes.

The control window for the VMIVME-9064/32 IIOC is allocated by the host computer in the reflective memory space. The ***IIOC Family Instruction Manual*** provides a definition of the control window parameters and a complete description of host command protocol.

SECTION 1 - ADDRESSES POSTED IN THE CONTROL WINDOW

All addresses posted by the IIOC in the control window are IIOC access addresses. The global memory on the reflective memory is accessed by the IIOC CPU from a base address of 0xFB000000 for the MVME143S-2 and from a base address of 0x7B000000 for the MVME162-202. In order to

access the buffer addresses posted by the IIOC in the control window, the host must mask off the upper eight bits of the 32-bit address and offset the result by the base address of the host local reflective memory.

For example, assume the host local reflective memory is addressed by the host CPU at a base of 0xFF000000 and the IIOC has posted an analog input buffer base address of 0xFB003020. The host would access this buffer at a base address of 0xFF003020.

SECTION 2 - VMEbus ADDRESSES FOR IIOC DATA TRANSFERS

Several commands to the IIOC require the IIOC to perform data transfers to or from the reflective memory board. When the host requires the IIOC to perform data transfers to or from the reflective memory, a full 32-bit absolute address within the IIOC reflective memory space must be provided in the control window.

MAINTENANCE

MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

MAINTENANCE PRINTS

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

APPENDIX

A

VMIVME-9064/32 EPROM PART NUMBERS

EPROMS installed in the VMIVME-9064/32 CPU board are 27512 devices containing 64 Kbytes of program data each. IIOC firmware is contained in two of these devices. The IIOC firmware EPROMS are labeled as shown below:

©VMIC 1990 IIOC U
VMIVME-9064/32-ABC-DEF
Vn.nnx mm/dd/yy

©VMIC 1990 IIOC L
VMIVME-9064/32-ABC-DEF
Vn.nnx mm/dd/yy

The first line on the label is the VMIC copyright and a letter indicating whether the EPROM contains the upper or lower (U or L) bytes of program data.

The second line contains the IIOC model number and the option code. The string "ABC-DEF" is replaced by the numeric code corresponding to the options ordered. See the ordering information in the VMIVME-9064/32 Specification (Document Number 800-009064-000) for the definition of each character in the string.

On the third label line, "n.nnx" is replaced by an alphanumeric string of the form "1.00m" indicating the firmware version number and "mm/dd/yy" indicates the month, day, and year of the firmware version.