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VMIVME-1110

64-BIT HIGH-VOLTAGE DIGITAL INPUT MEGAMODULE™

INSTRUCTION MANUAL

DOCUMENT NO. 500-001110-000 AC

Revised May 12, 1997

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E	02/26/88	Appendix A	88-0011
F	06/29/88	Appendix A	88-0109
G	08/24/88	Appendix A	88-0235
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GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

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Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

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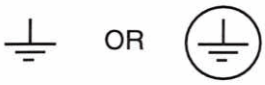
GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



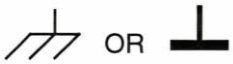
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



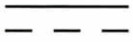
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

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VMIVME-1110
64-BIT HIGH-VOLTAGE DIGITAL INPUT MEGAMODULE™

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A Assembly Drawing, Part List, and Schematic

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIC VMIVME-1110 High Voltage Digital Input Board is designed to read a wide range of high voltages from a variety of devices. These signals may originate from electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, or Opto 22 type signal conditioning modules and numerous other sources. The input signal conditioning options include high voltage current sink or voltage source configurations with a wide variety of input filter options and built-in hysteresis.

The VMIC VMIVME-1110 High Voltage Digital Input Board has several unique features as specified below:

a. Supports 8-, 16- and 32-bit data transfers

b. Contains Built-in-Test logic that allows fault detection in an off-line mode and during real-time operation

c. Built-in-Test supports testing 100 percent of all active components

d. Two sets of address switches are provided such that subsystems may be configured with contiguous I/O addresses to conserve memory

e. Front panel Fail LED for quick fault isolation to the board level

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-1110 is a member of VMIC's Megamodule™ family which is designed with common programming features such that subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these boards (VMIVME-1110, -2130, -2120, and -2510) is designed with two sets of board address switches to provide an efficient memory address map for control and status registers (CSR) and I/O addresses. The CSR address switches may be set such that all CSRs among a variety of boards in a system may be mapped into contiguous memory locations. The MEGAMODULE™ product line is also designed to support 8-, 16-, and 32-bit data transfers. The board also features a front panel Fail LED. It is illuminated at power-up reset and may be extinguished under program control, upon successful completion of board level diagnostics. Specific hardware has been designed into the VMIVME-1110 to support Built-in-Test functions. The VMIVME-1110 supports both off-line and on-line fault detection and isolation.

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1.3 REFERENCE MATERIAL

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Rd.
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products:

TITLE	DOCUMENT
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-001110-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

The VMIVME-1110 High-Voltage Digital Input Board is designed to read a variety of signal inputs such as electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, Opto 22-type signal conditioning modules, and numerous other sources. The two primary types of signal conditioning electronics that may be ordered are voltage source and current sink. Typical input signal conditioning designs are shown in Figure 3.1-1. A block diagram showing the typical connection-to-user hardware is shown in Figure 3.1-2.

The design of the VMIVME-1110 board, as shown in the functional block diagram Figure 3.1-3, consists primarily of four sections:

a. VMEbus Foundation Logic

b. Device Addressing

c. Input Signal Conditioning

d. Built-in-Test Logic

3.2 DEVICE ADDRESSING

The VMIVME-1110 is designed to support data transfers in supervisory or nonprivileged short I/O memory space. A jumper is provided, as shown in Figure 3.2-1 (Address Selection Block Diagram), to allow user selection of either I/O access type. The jumper (JA) is shown in Appendix A on logic diagram 141-001110-000. The VMIVME-1110 is factory configured (jumper JA not installed) to respond to short supervisory I/O access.

The VMIVME-1110 is designed with two sets of board-select switches and decode logic, as shown in Figure 3.2-1, to provide an efficient memory address map for CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into separate contiguous memory locations when configuring subsystems that require more than one board.

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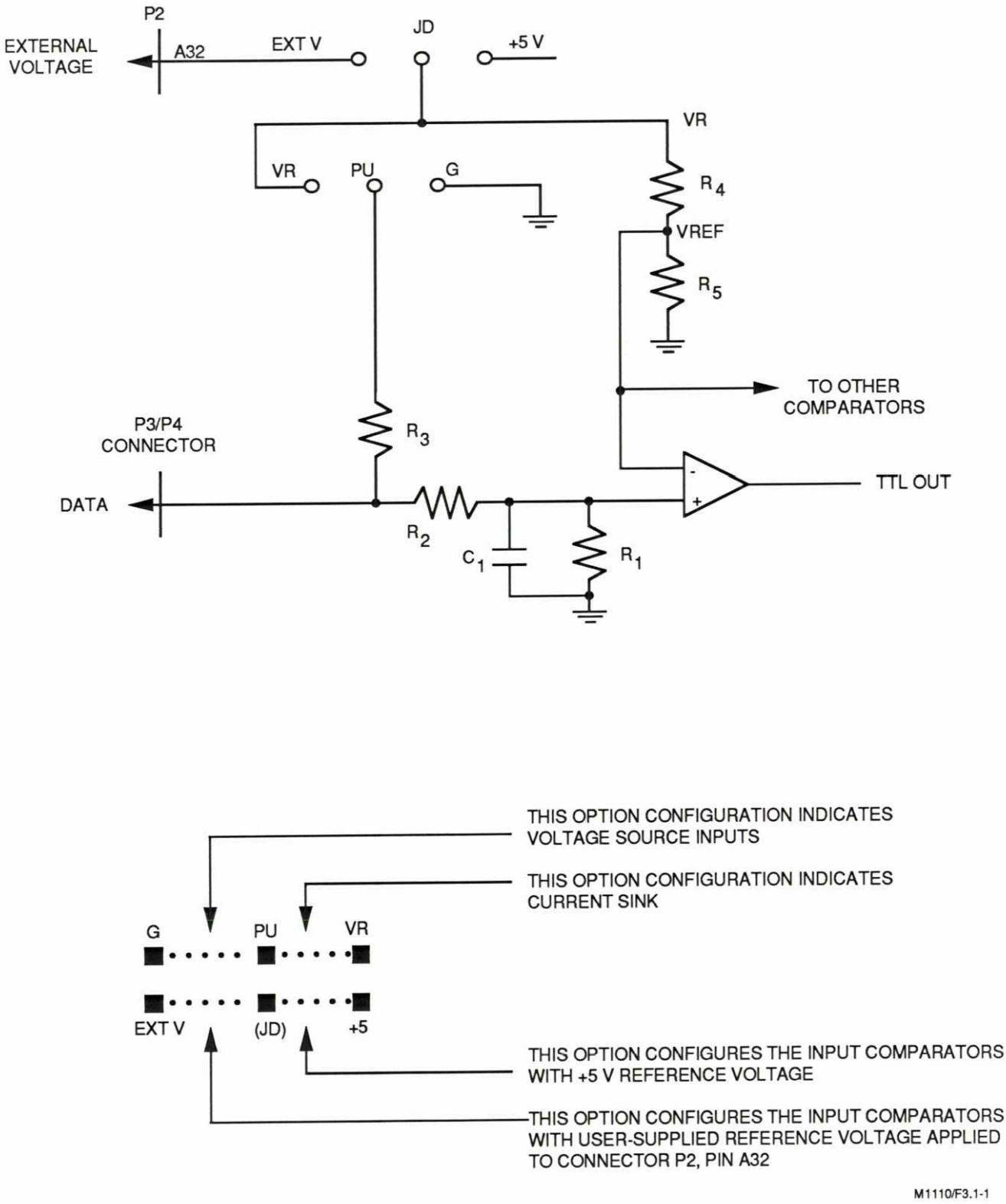


Figure 3.1-1. Signal Conditioning Configuration Selection

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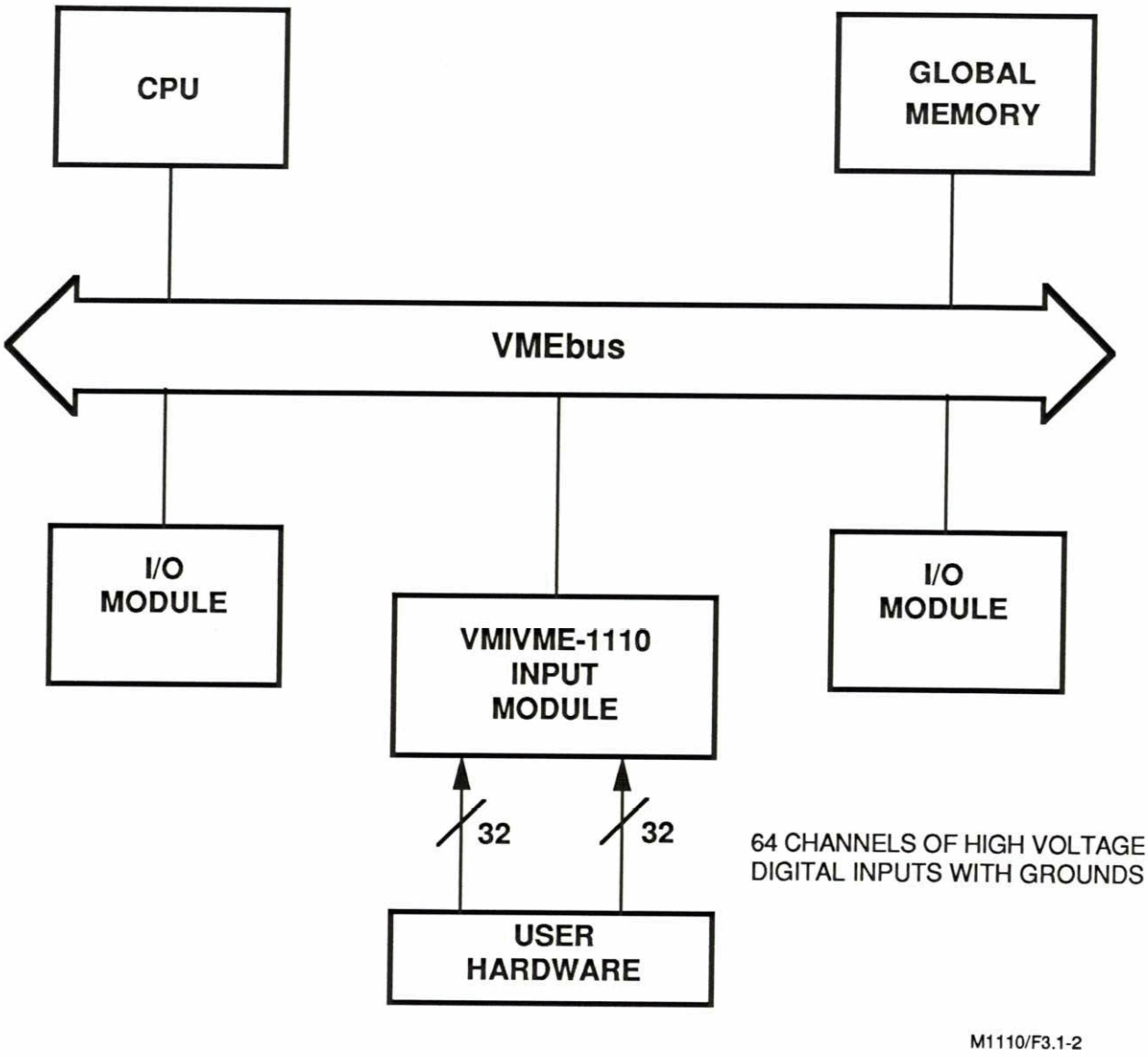


Figure 3.1-2. VMIVME-1110 Connection-to-User Hardware

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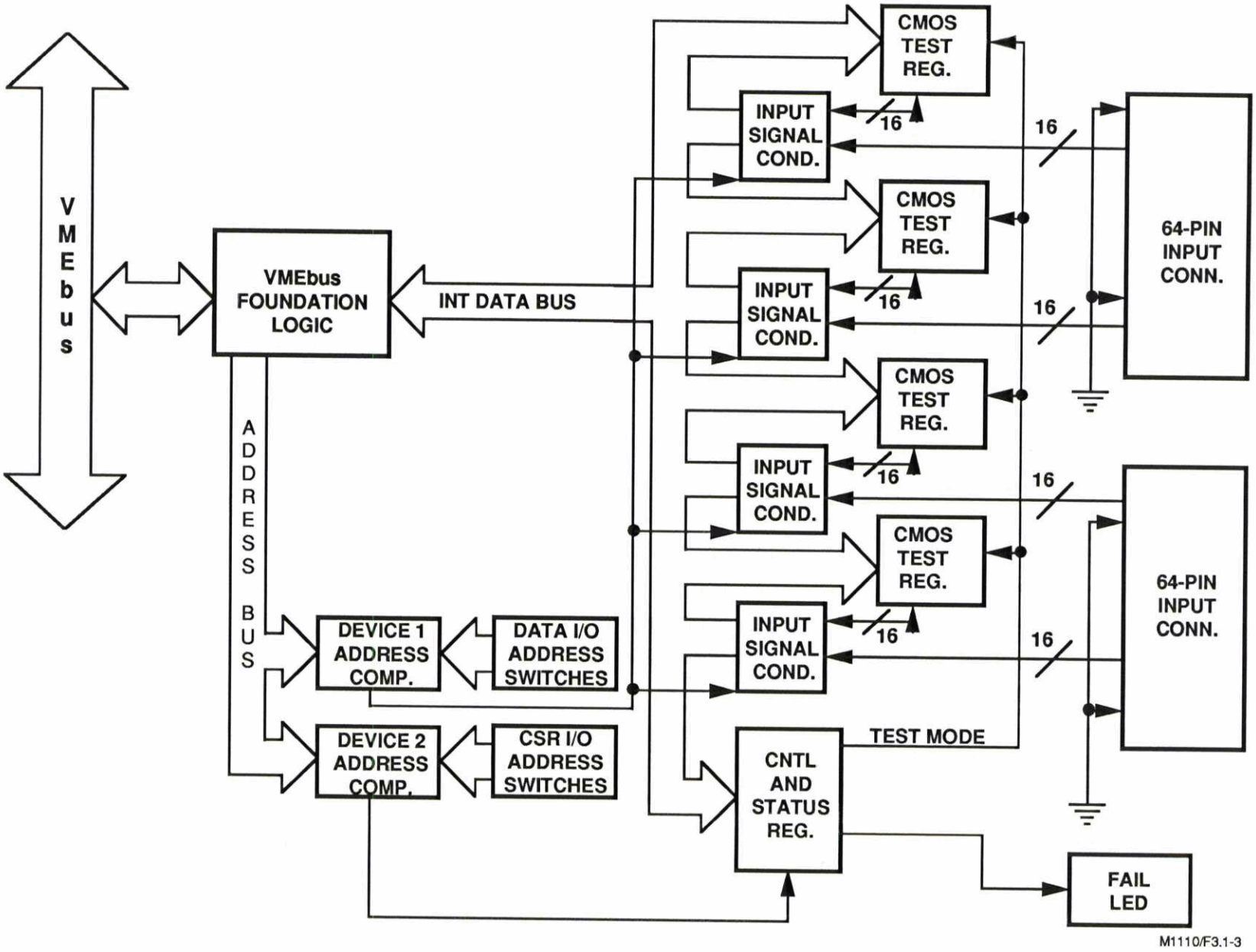


Figure 3.1-3. High Voltage Digital Input MEGAMODULE™

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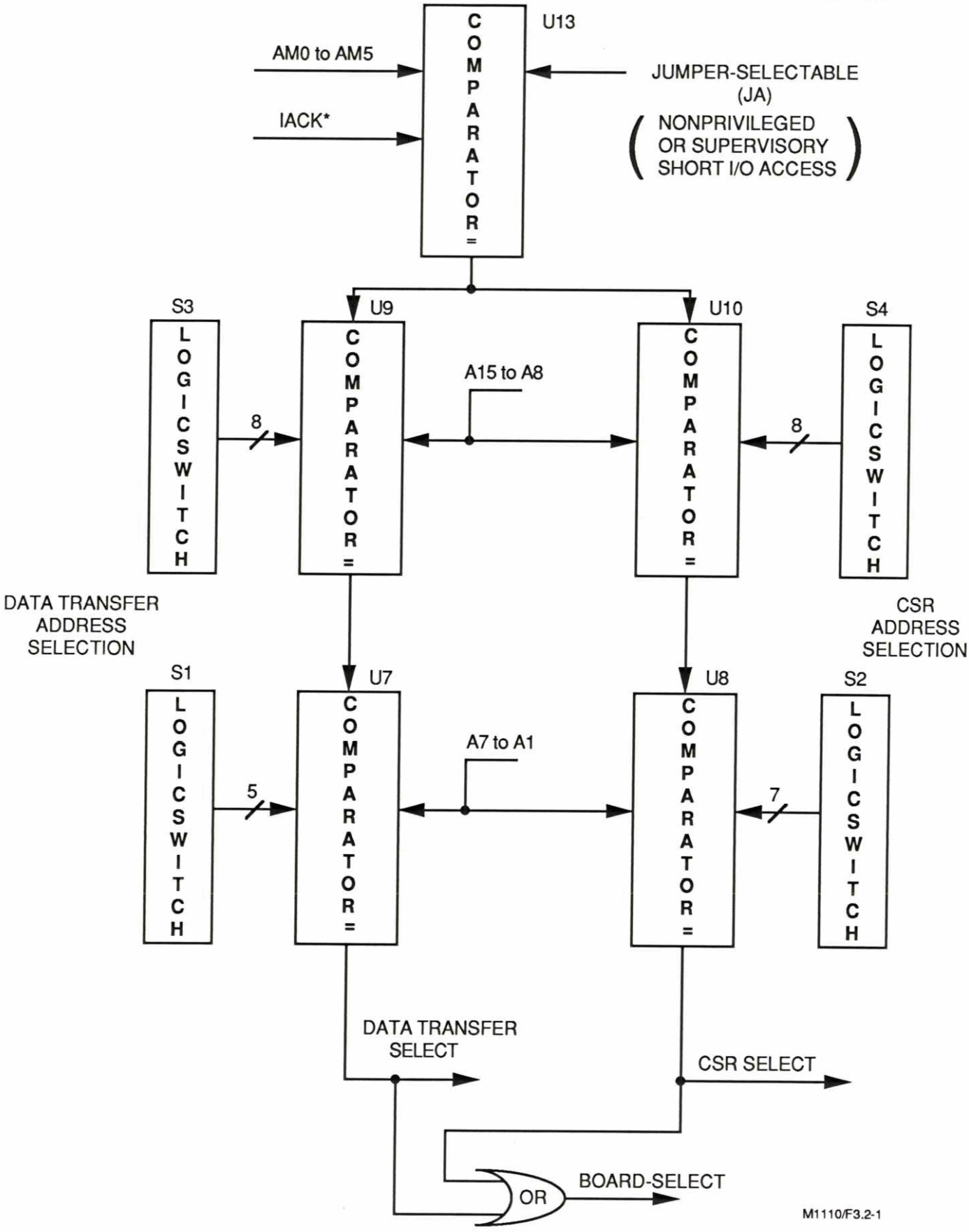


Figure 3.2-1. Device Address Selection Block Diagram

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3.3 VMEbus COMPATIBILITY LOGIC

Typical VMEbus drivers, receivers and control logic are shown in Figures 3.3-1 through 3.3-7. The DTACK generator shown in Figure 3.3-1 is actually designed with a jumper installed at the factory to provide for the maximum rate of data transfer.

3.4 DATA TRANSCEIVERS

Data transfer transceivers are shown in Figure 3.3-3. The VMIVME-1110 may be ordered to support 8- and 16-bit transfers or 8-, 16-, and 32-bit transfers. Integrated circuits U2 and U4 are not installed on units ordered to support 8- and 16-bit transfers only.

3.5 REGISTER CONTROL LOGIC

The VMIVME-1110 Board control logic is designed to support four 16-bit read-only ports with signal conditioning and four 16-bit CMOS test registers to support the Built-in-Test feature. The control logic (shown in Figure 3.3-4) is separated into READ and WRITE control signals and provides the capability to read or write 8, 16, or 32 bits of data.

To perform input data transfers, data is transferred via transceivers, which are selected by address bits A2, A1, and the data strobes. The 64 bits of high voltage inputs are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

3.6 CONTROL AND STATUS REGISTER (CSR)

The CSR is a write only register that controls the Test Mode (TM) bit and the front panel Fail LED, as shown in Figure 3.3-5. The TM bit enables the TRI-STATE outputs of the eight CMOS test registers that are used to perform the Built-in-Test functions. Both bits of the CSR are initialized active upon system reset, such that the test register outputs are enabled and the front panel Fail LED is illuminated.

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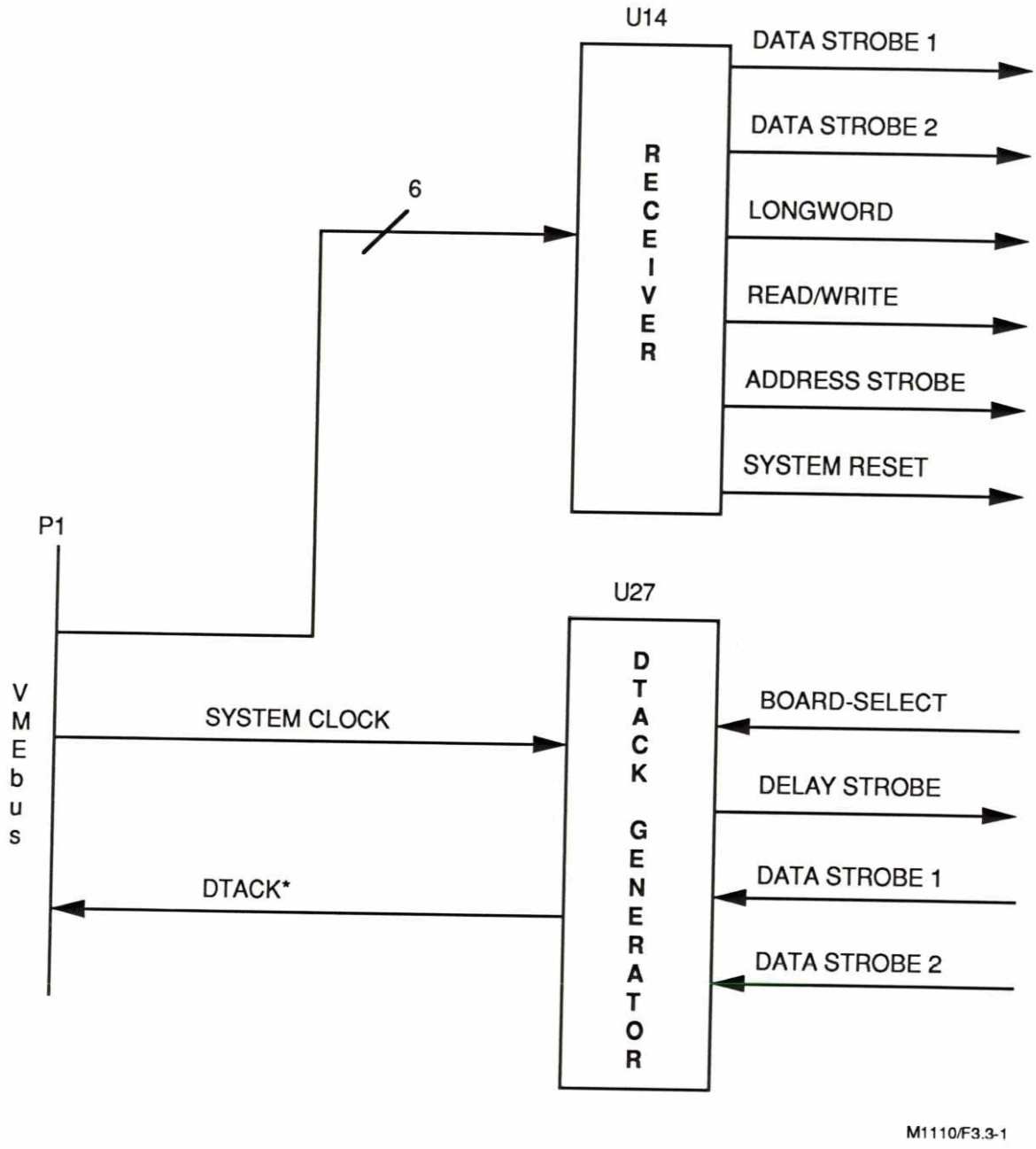


Figure 3.3-1. Control Section Block Diagram

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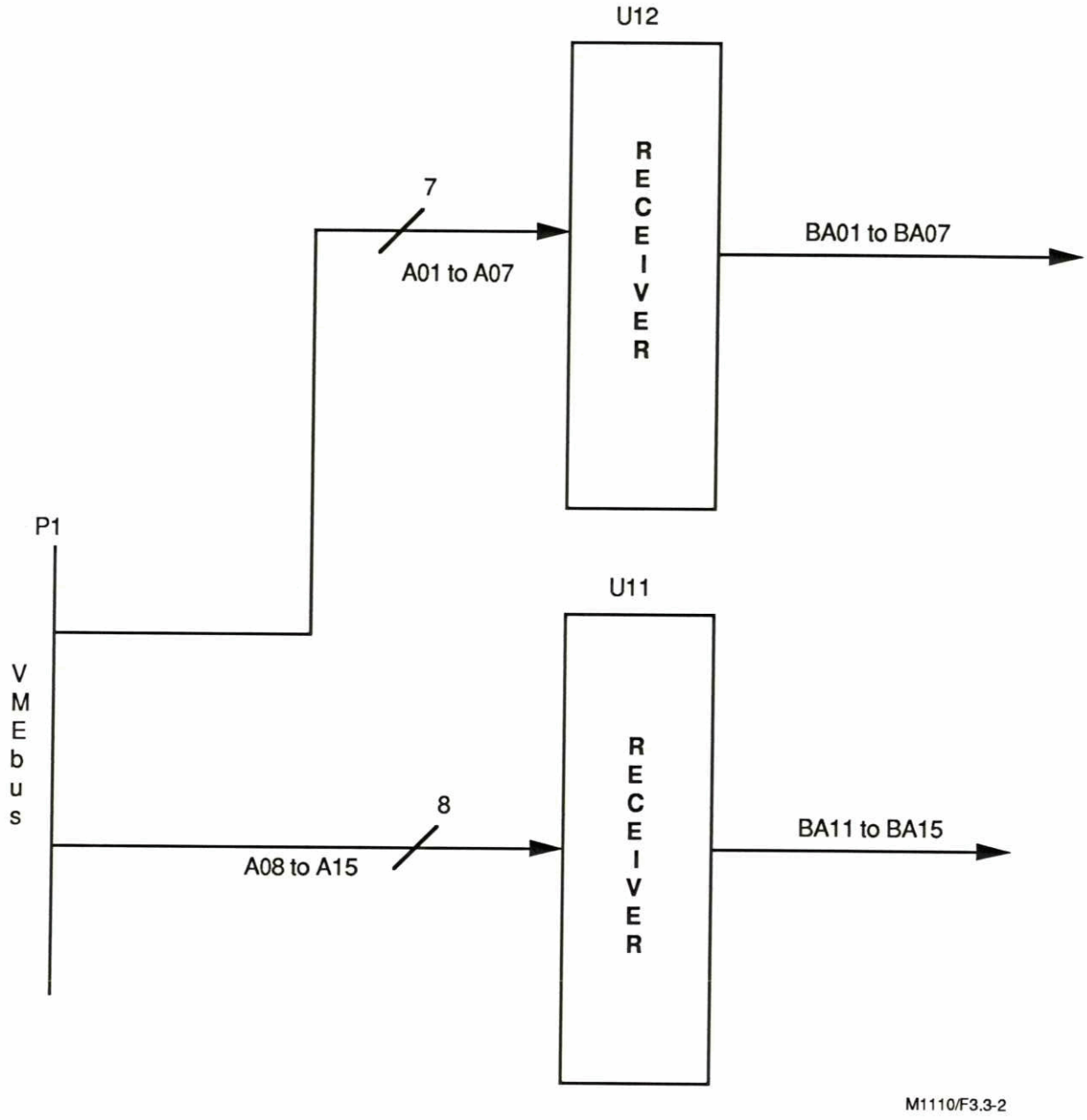


Figure 3.3-2. Address Section Block Diagram

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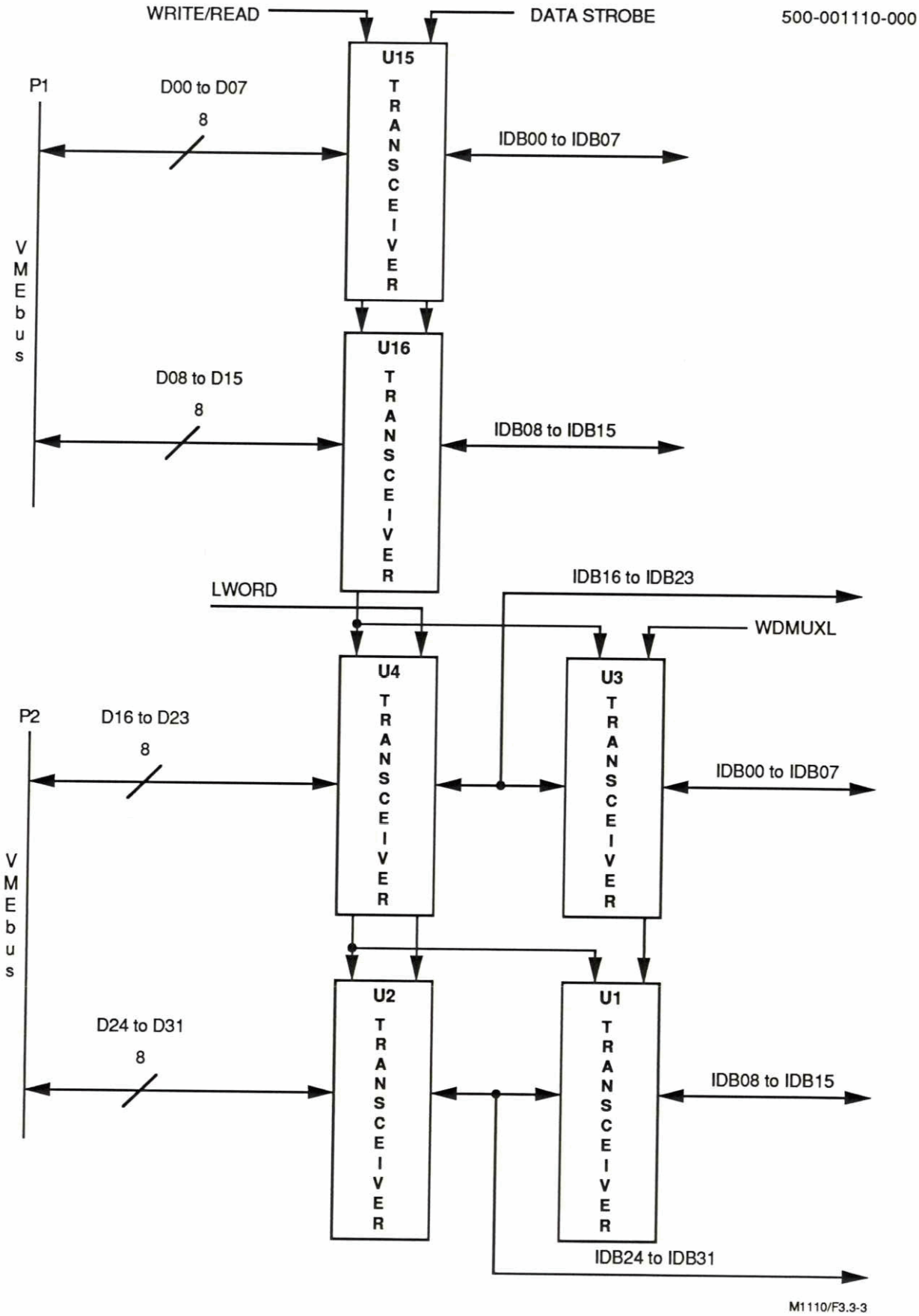


Figure 3.3-3. Data Transfer Block Diagram

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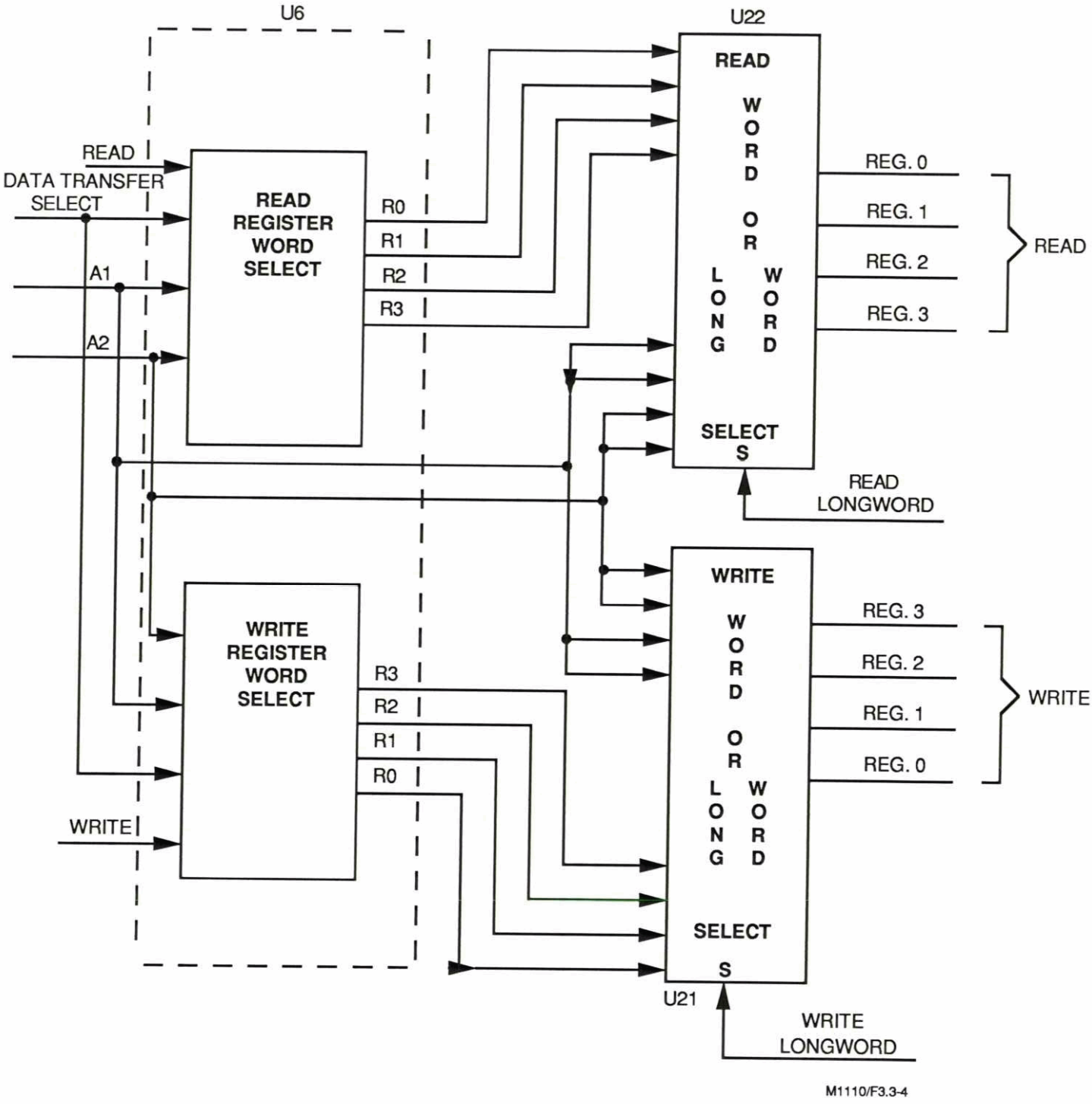


Figure 3.3-4. I/O Register Control Logic Block Diagram

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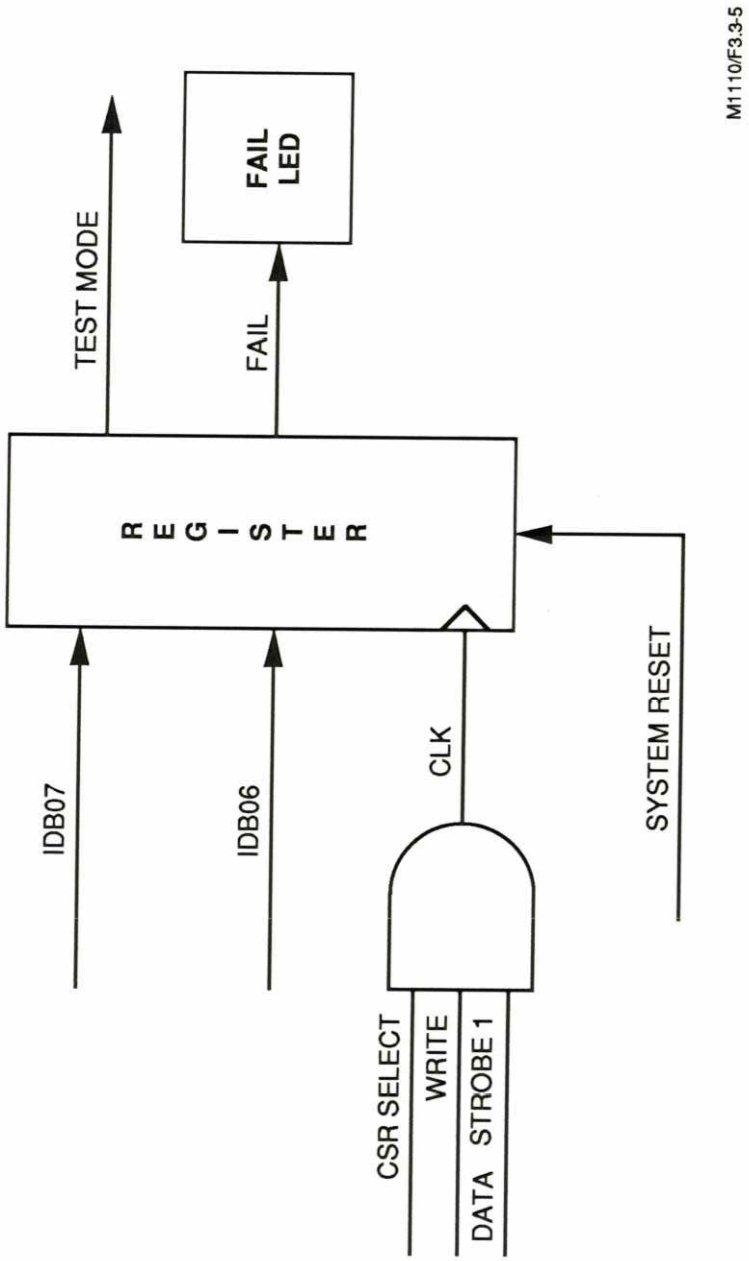


Figure 3.3-5. CSR Control Logic Block Diagram

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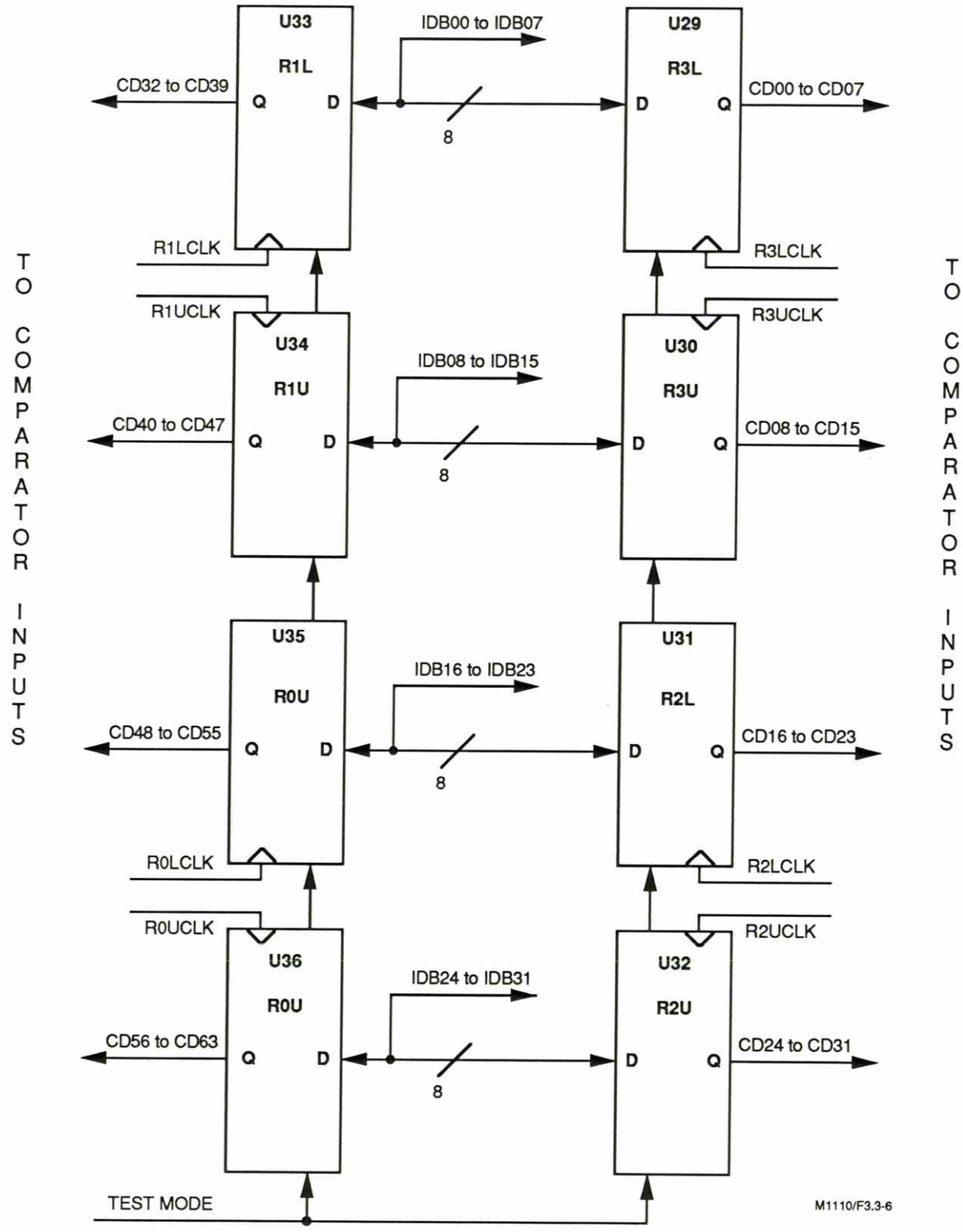
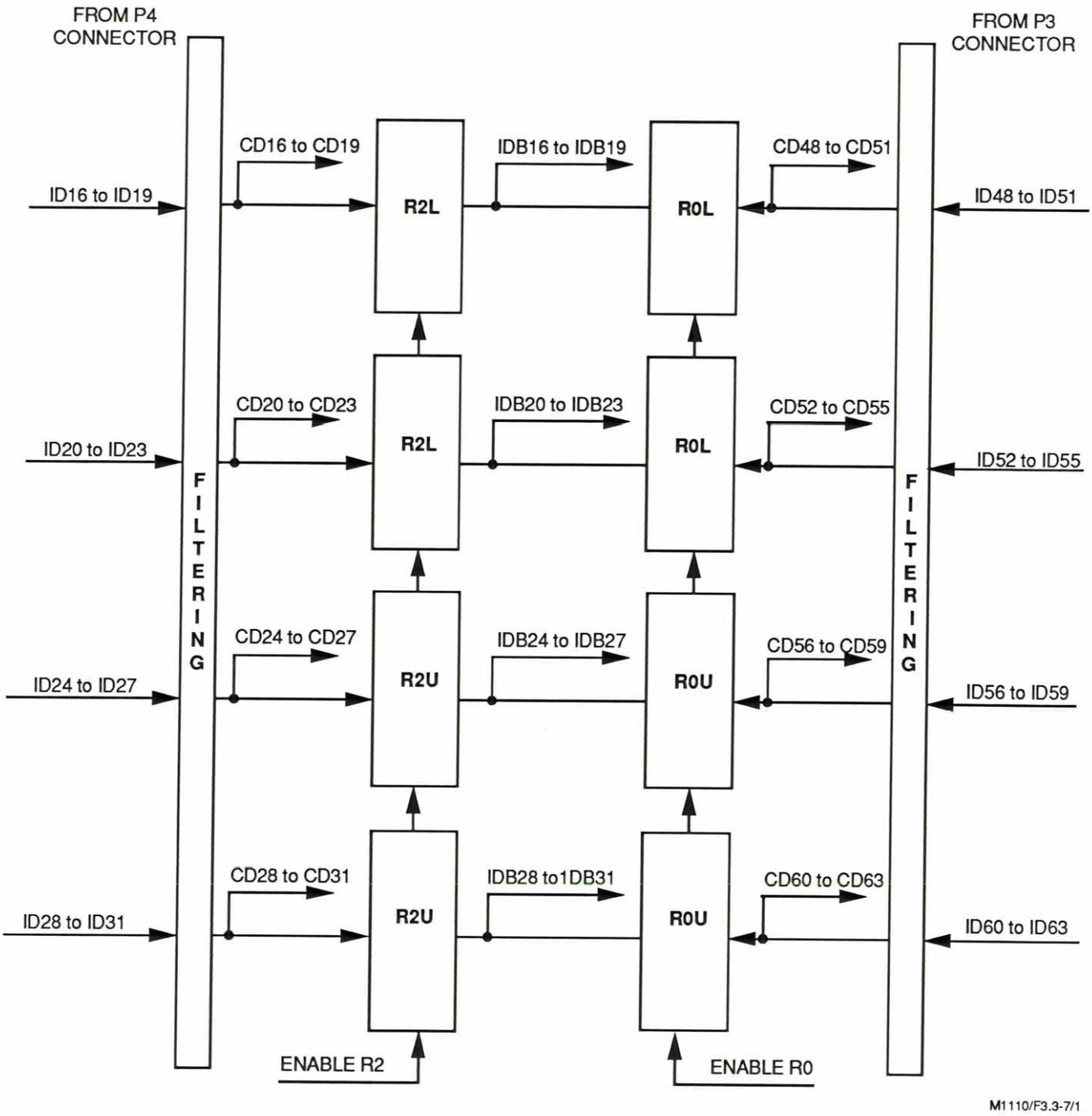


Figure 3.3-6. Self-Test Logic (Test Data Registers) Block Diagram

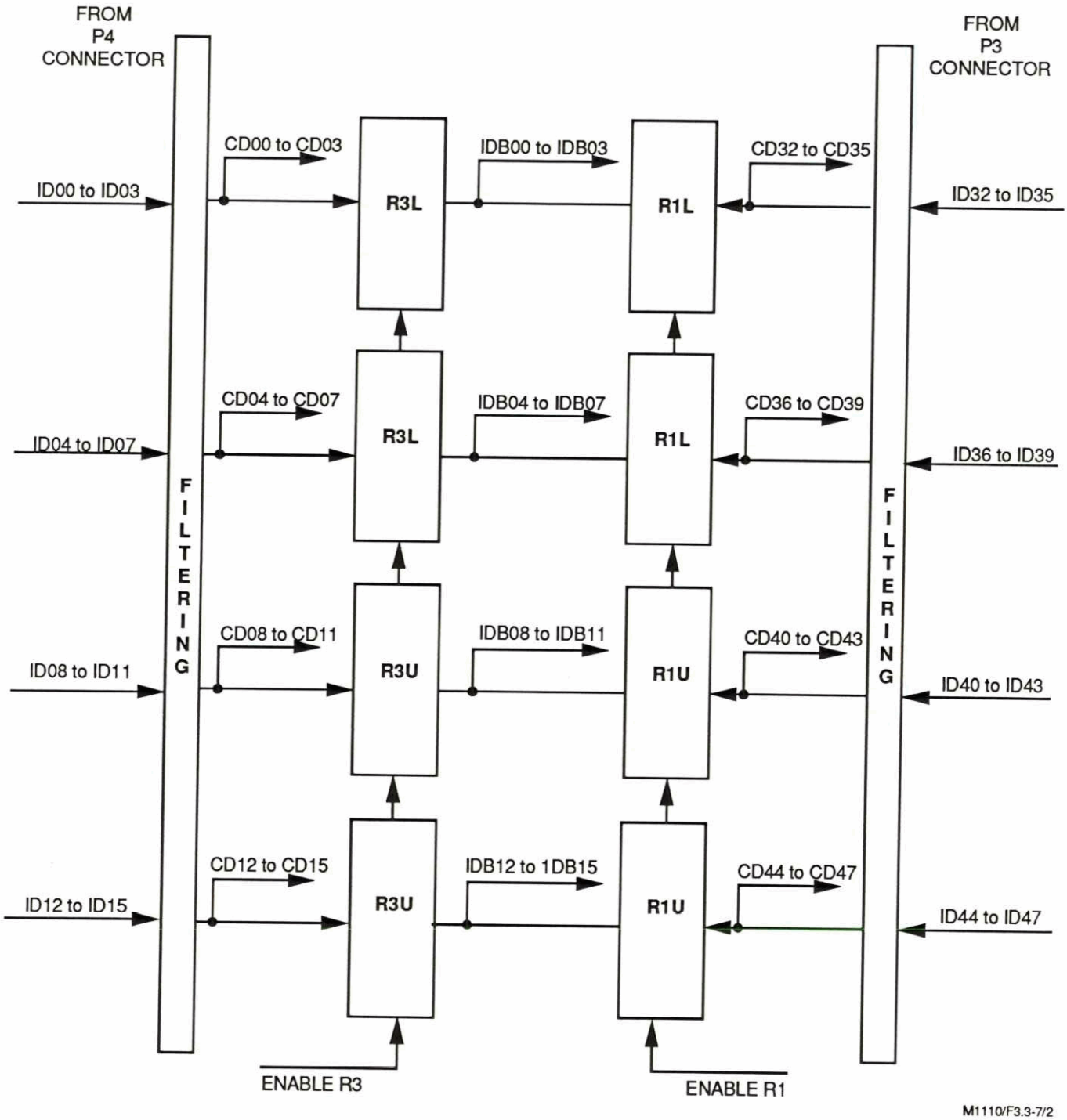
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NOTE: The registers above are Quad Comparators.

Figure 3.3-7. Signal Conditioning Block Diagram (Sheet 1 of 2)

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NOTE: The registers above are Quad Comparators.

Figure 3.3-7. Signal Conditioning Block Diagram Quad Comparators (Sheet 2)

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3.7 TEST REGISTERS

The VMIVME-1110 is designed utilizing eight 8-bit CMOS test registers to support the Built-in-Test features. The outputs of the test registers are connected to the input signal conditioning comparators, as shown in Figure 3.3-7. The reader should refer to the test register functional diagram in Figure 3.3-6. Notice that the signal CDXX coming from the test registers goes to the inputs of the signal conditioning comparators as shown in Figure 3.3-7. This Built-in-Test design concept enables 100 percent testing of all active components on the board.

The Built-in-Test feature of the VMIVME-1110 is enabled by asserting the test mode bit in the control register. While in test mode, test data is written to input register locations and then read back on a read transfer. For example, data is written to the input register being tested, data is read, and a software comparison is performed. The test mode must be disabled to allow normal data input operations.

The test mode bit and the Fail LED bit are enabled after a system reset. Therefore, test mode is activated and the Fail LED is illuminated upon power-up. Once test mode diagnostics have been completed, the Fail LED should be turned off, and the test mode control bit be cleared for normal mode processing of digital inputs.

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The VMIVME-1110 is designed to enable the user to read eight 8-bit input ports and to write to a Control and Status Register that controls the test mode and a front panel LED. The input port registers and the Control and Status Register address maps are shown below. The VMIVME-1110 supports a Built-in-Test function by writing to eight 8-bit CMOS registers whose outputs are connected to the input port signal conditioning logic. The test registers are written to using the same addresses as each input port, as shown below in Table 4.1-1. The data can be accessed as two 32-bit longwords, (if the 32-bit option is ordered), four 16-bit words, or eight 8-bit bytes.

Table 4.1-1. Input Ports

RELATIVE ADDRESS	MNEMONIC	NAME/FUNCTION
$XXX0	DR0	INPUT PORT/TEST REGISTER 0
$XXX1	DR1	INPUT PORT/TEST REGISTER 1
$XXX2	DR2	INPUT PORT/TEST REGISTER 2
$XXX3	DR3	INPUT PORT/TEST REGISTER 3
$XXX4	DR4	INPUT PORT/TEST REGISTER 4
$XXX5	DR5	INPUT PORT/TEST REGISTER 5
$XXX6	DR6	INPUT PORT/TEST REGISTER 6
$XXX7	DR7	INPUT PORT/TEST REGISTER 7

Note: XXX of the address is determined by the input port address select switches S3 and S1. See Section 5.5.

CSR

RELATIVE ADDRESS	MNEMONIC	NAME/FUNCTION
$YYY1	CSRL	CSR LOWER BYTE

Note: YYY of the address is determined by the CSR address select switches S4 and S2. See Section 5.5

The CSR is a write-only register.

M1110/T4.1-1

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4.2 REGISTER BIT DEFINITIONS

$XXX0 DR0

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
INPUT DATA REGISTERS							
IDB63	IDB62	IDB61	IDB60	IDB59	IDB58	IDB57	IDB56

$XXX1 DR1

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
INPUT DATA REGISTERS							
IDB55	IDB54	IDB53	IDB52	IDB51	IDB50	IDB49	IDB48

$XXX2 DR2

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT 9	BIT 8
INPUT DATA REGISTERS							
IDB47	IDB46	IDB45	IDB44	IDB43	IDB42	IDB41	IDB40

$XXX3 DR3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA REGISTERS							
IDB39	IDB38	IDB37	IDB36	IDB35	IDB34	IDB33	IDB32

M1110/F4.2-1/1

Figure 4.2-1. Input Data Register Definitions

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$XXX4 DR4

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
INPUT DATA REGISTERS							
IDB31	IDB30	IDB29	IDB28	IDB27	IDB26	IDB25	IDB24

$XXX5 DR5

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
INPUT DATA REGISTERS							
IDB23	IDB22	IDB21	IDB20	IDB19	IDB18	IDB17	IDB16

$XXX6 DR6

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT 9	BIT 8
INPUT DATA REGISTERS							
IDB15	IDB14	IDB13	IDB12	IDB11	IDB10	IDB9	IDB8

$XXX7 DR7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA REGISTERS							
IDB7	IDB6	IDB5	IDB4	IDB3	IDB2	IDB1	IDB0

M1110/F4.2-1/2

Figure 4.2-1. Input Data Register Definitions (Concluded)

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4.3 REGISTER BIT DEFINITIONS (CSR)

CSR bits 15 through 8 and 5 through 0 are not used as shown in Figure 4.3-1.

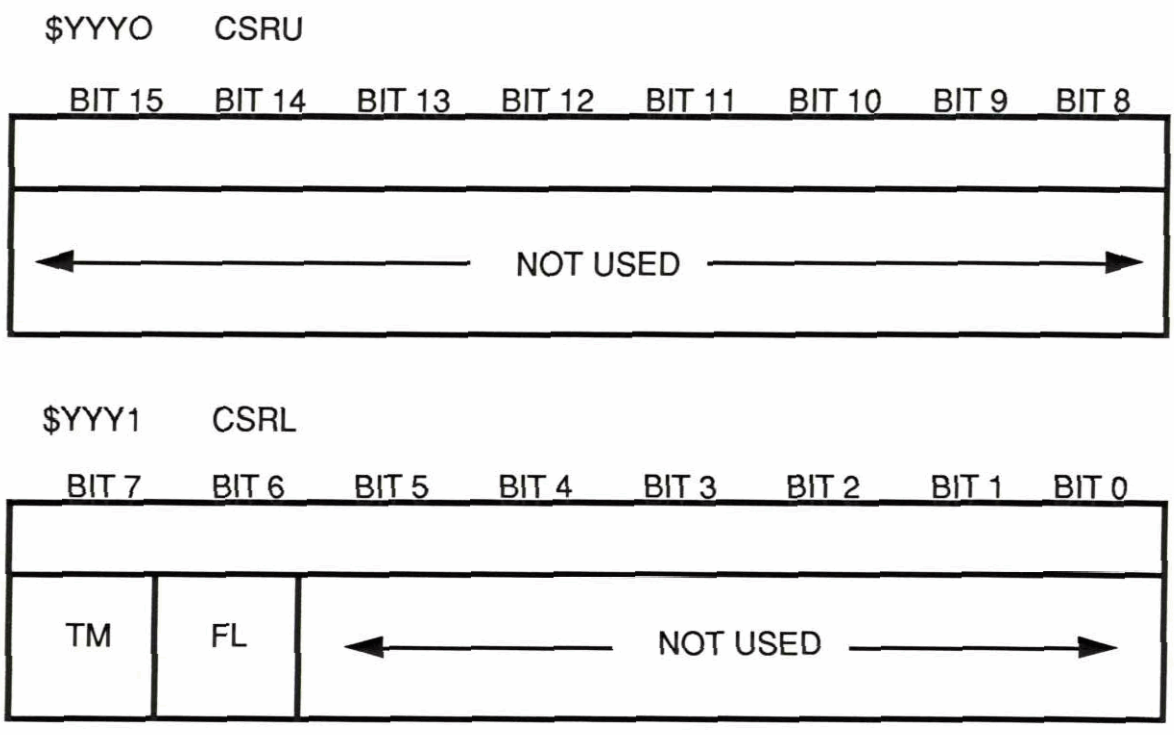


Figure 4.3-1. CSR Bit Definitions

BIT 7 - Test Mode (TM)

When bit 7 is set to a "one", test mode is entered. The CMOS test register outputs are activated, and the user can execute loopback diagnostics on each port. The test mode bit is activated by a system reset and/or at power-up. Bit 7 must be cleared before normal operation can begin.

BIT 6 - Fail LED (FL)

This bit controls the state of the front panel LED. Bit 6 is set to a Logic "one" during a system reset and/or at power-up. It must be cleared to turn off the front panel LED.

When a negative true board is ordered, the data lines driving this resister invert the incoming data. Therefore, the program must take into account this inversion when it asserts the conditions controlled by the CSR.

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4.4 DETAILED DATA ACCESS

4.4.1 Input Data Access

As seen in the register map, DR0 through DR7 corresponds to input channels 63 to 0. Therefore, to access input data, the corresponding input port is read, provided that the test mode bit in the CSR is disabled. The programming sequence for normal operation is shown in Figure 4.4.1-1.

4.4.2 Built-in-Test

The Built-in-Test feature is characterized by being able to test the input comparator stage of the board while the inputs are connected to the field. Loop-back testing can be performed at any time, because the input comparator is isolated from the field by a series resistor. However, when the CMOS registers are in use, the input byte will not read the field data.

The Built-in-Test feature is activated by setting the TM bit in the CSR to the appropriate state for the polarity option of the board (for positive true boards, TM = "one", for negative true boards, TM = "zero"). Test data is then written to the selected test register and may be read back on a read transfer from the same port address. The programming sequence for test mode operation is shown in Figure 4.4.2-1. If the board has optional filtering, allow two or three times the selected filter time constant before reading the inputs during Built-in-Test and immediately after the Built-in-Test program is completed. This is because the discharge time of the filter caps is longer when the CMOS test registers are used.

4.4.3. Power-Up/System Reset

Upon power-up or when a system reset is performed, both bits in the CSR will be set to the appropriate state for the polarity option of the board (for positive true boards, TM = "one", for negative true boards, TM = "zero"); therefore, test mode is enabled and the Fail LED is ON.

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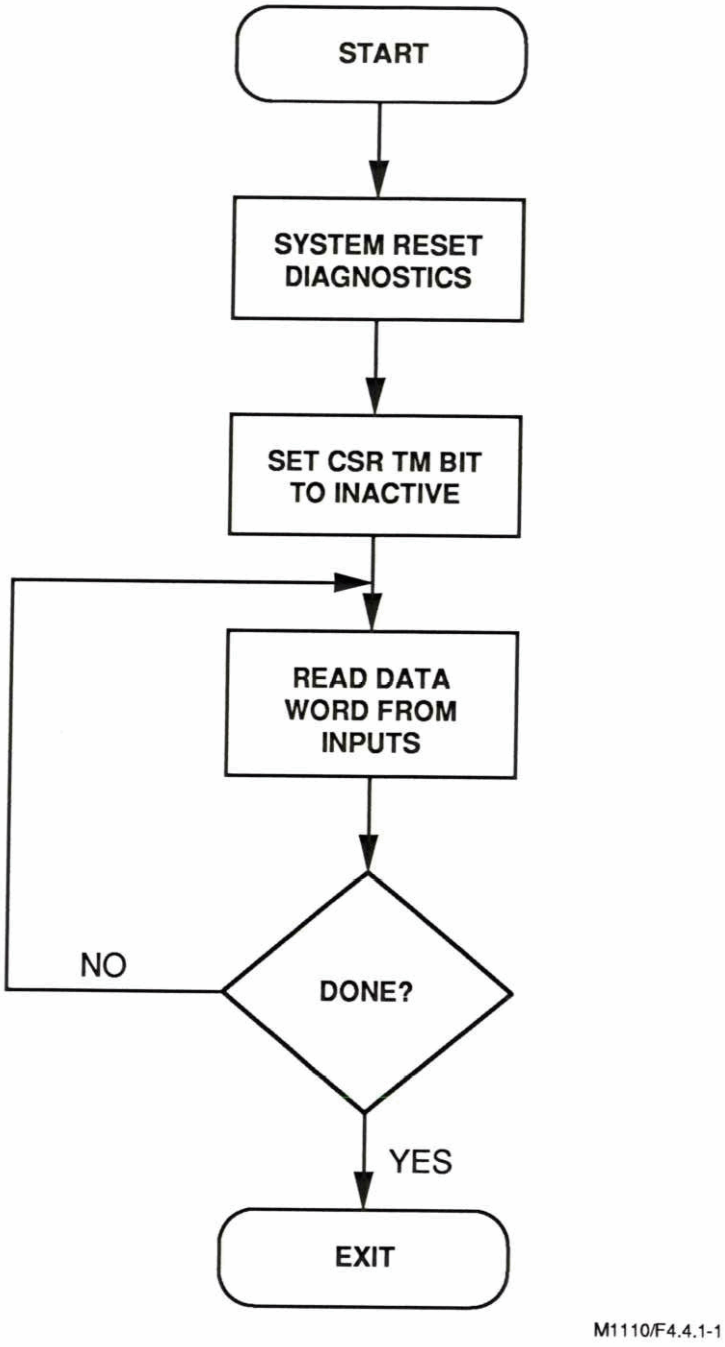


Figure 4.4.1-1. Normal Programming Flowchart

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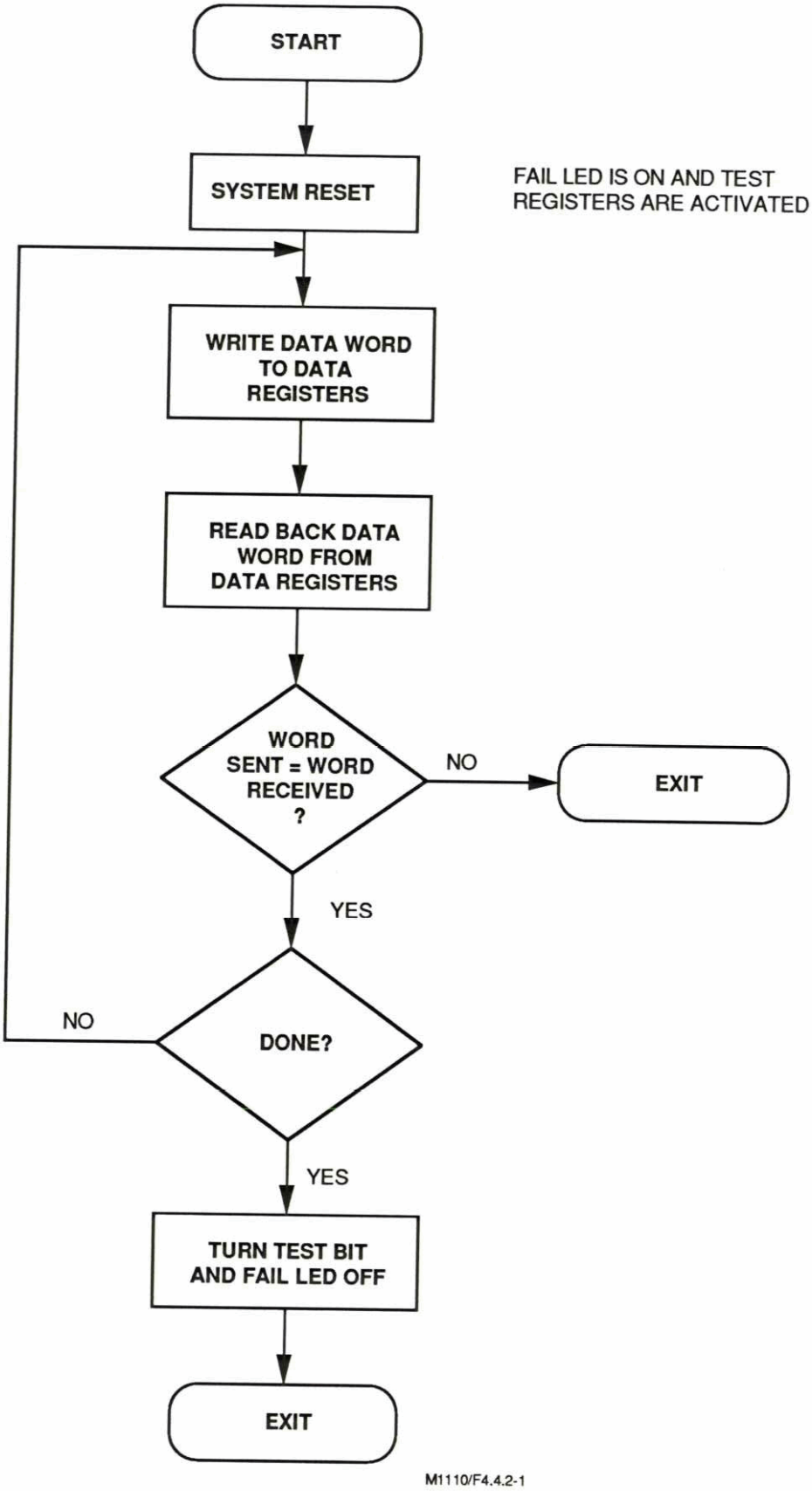


Figure 4.4.2-1. Test Programming Flowchart

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BAGS AS SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

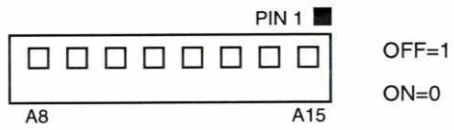
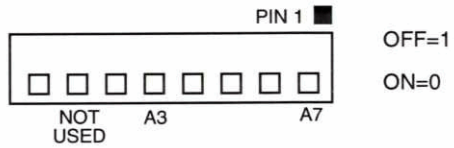
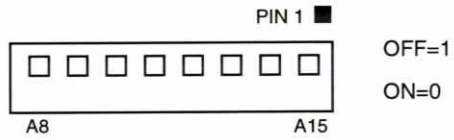
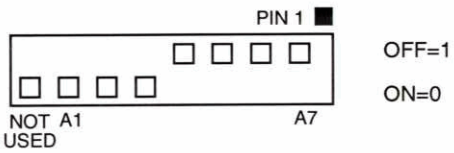
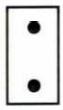
De-energize the equipment and insert the board into an appropriate slot of the chassis. While insuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.2.1 Installation

This section describes the VMIVME-1110 Board setup procedure and board jumper configuration. The jumper and switch factory configurations are shown in Table 5.2.1-1. The physical location of these jumpers and switches are shown in Figure 5.2.1-1.

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Table 5.2.1-1. Factory Set Jumpers and Address Switch Configurations

SWITCH/ JUMPER	FUNCTION	PRE-SET CONDITION
S3	S1 AND S3 DETERMINE THE BASE ADDRESS OF THE EIGHT INPUT PORTS AND TEST RESISTERS.	
S1	THE PRE-SET BASE ADDRESS IS FF00 HEX.	
S4	S2 AND S4 DETERMINE THE ADDRESS OF THE CONTROL/STATUS REGISTER (CSR).	
S2	THE PRE-SET BASE ADDRESS IS FFF0 HEX.	
JA	THIS JUMPER DETERMINES THE BOARD'S RESPONSE TO THE ADDRESS MODIFIER CODES. IF THE JUMPER IS NOT INSTALLED, THE BOARD RESPONDS TO SHORT SUPERVISORY I/O ACCESS. IF THE JUMPER IS INSTALLED, THE BOARD RESPONDS TO SHORT NONPRIVILEGED I/O ACCESS.	 NOT INSTALLED AT THE FACTORY
PU	WHEN THIS JUMPER GOES TO "G", THE BOARD INPUTS ARE VOLTAGE SOURCING. WHEN THE JUMPER GOES TO "VR", THE BOARD INPUTS ARE CURRENT SINKING.	THIS JUMPER IS CONFIGURED BY OPTION ORDERING INFORMATION.
JD	THIS JUMPER CONFIGURES THE INPUT COMPARATORS WITH THE PROPER REFERENCE VOLTAGE.	THIS JUMPER IS CONFIGURED BY OPTION ORDERING INFORMATION.
JB	THIS JUMPER SELECTS THE DTACK TIME DELAY	CONFIGURED AT THE FACTORY

M1110/T5.2.1-1

NOTE: On boards equipped with rocker type switches, depress the switch on the off side for an OFF condition.

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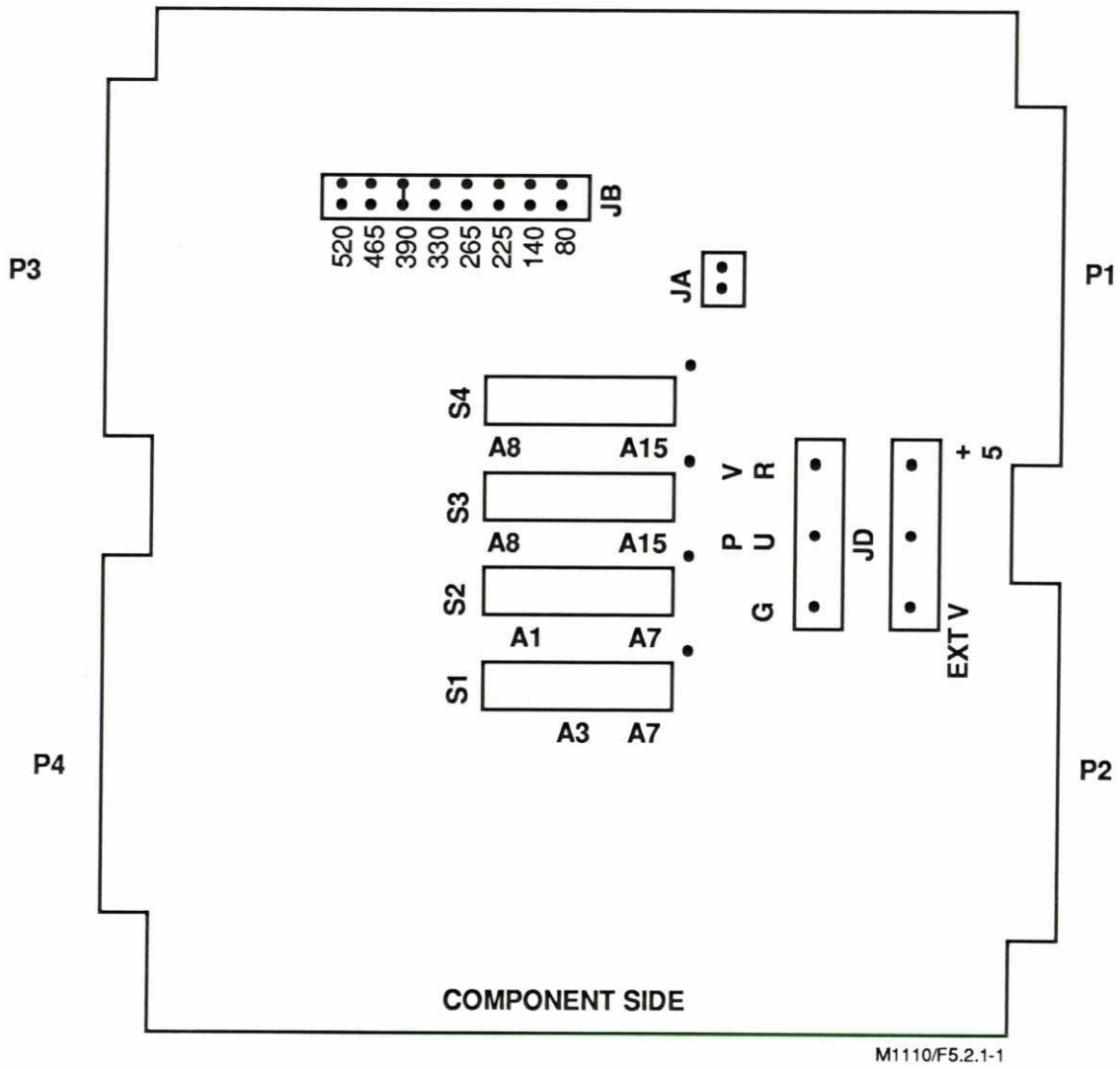


Figure 5.2.1-1. Switch and Jumper Locations

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5.2.2 Before Applying Power: Checklist

Before installing the board in a VMEbus system, perform the following checklist to verify that the board is ready for the intended operation:

a. Have Sections 3 and 4 on Theory and Programming of the VMIVME-1110 been read and applied to system requirements?

_____

b. Review Table 5.2.1-1 to verify factory installation of the jumpers and board address switch positions.

_____

(1.) To change the address switches, refer to Section 5.3.
(2.) To change the address modifier response, refer to Section 5.4.
(3.) To change the current sink/voltage source option, refer to Section 5.5.
(4.) To change the comparator voltage reference, refer to Section 5.6.

c. Have the cables, with proper mating connectors, been connected to the input connectors? Refer to Section 5.7.

_____

After steps 1 through 3 have been reviewed, then the VMIVME-1110 Board may be installed. (Do not install or remove the board with power on.) Generally, the VMIVME-1110 may be installed in any slot position, except slot one, which is usually reserved for the system controller processing unit.

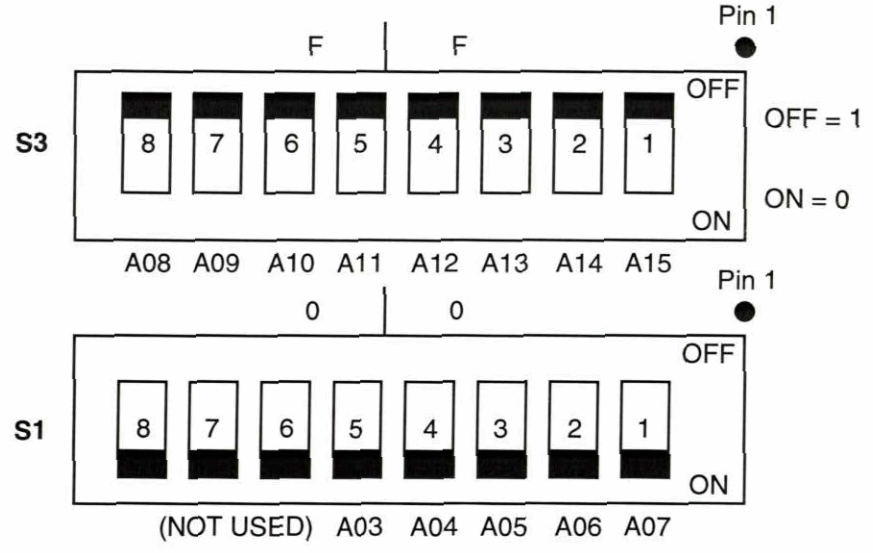
5.3 ADDRESS SELECTION SWITCHES

DIP switches are provided to select the base address of the input data ports and the CSR. Figure 5.3-1 shows an example for setting the data port's base address to FF00 HEX. Figure 5.3-2 shows an example setting the CSR's address to FF10 HEX.

5.4 ADDRESS MODIFIERS

The VMIVME-1110 is configured at the factory to respond to short supervisory I/O access. Installing jumper JA enables the board to respond to short nonprivileged I/O access.

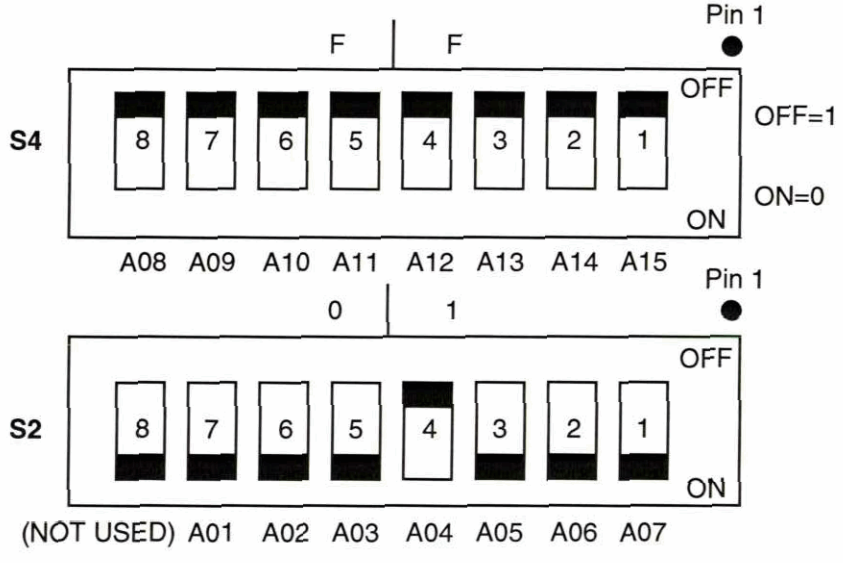
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The example shown is for base address of FF00 HEX.

M1110/F5.3-1

Figure 5.3-1. Input Port Address Select Switches



The example shown is for a base address of FF10 HEX.

M1110/F5.3-2

Note: For Rocker-Type Switches: OFF Pressed In = 1
ON Pressed In = 0

Figure 5.3-2. CSR Select Switches

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5.5 CURRENT SINK, VOLTAGE SOURCE SELECTION

For the specified voltage ranges for each board option, jumper PU is installed at the factory to select between a current sink configuration, or a voltage source configuration. The board is configured for current sink with jumper PU installed going to VR, or for voltage source with jumper PU installed going to G as shown in Figures 5.5-1 and 5.5-2.

5.6 EXTERNAL PULL-UP VOLTAGE

External voltage, if required, is connected to the VMIVME-1110 Board via the P2 connector on pin A32. The user can select the external voltage or the on-board +5 V voltage source to supply the input comparator with the proper reference voltage. Jumper JD selects between the +5 V or the external voltage at jumper positions +5 and EXT V, as shown in Figures 5.5-1 and 5.5-2. Refer to Section 2.2 (Specifications) for the different input voltage requirements for the +5 V, +12 V, +24 V, and +48 V reference options.

5.7 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION

The input connectors (P3 and P4) on the VMIVME-1110 are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Document No. 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning input connections are shown in Figure 5.7-1. Figure 5.7-1 has conductor no. 1 shown at the bottom of the connector as it plugs into the header, due to pin no. 1 of P3 and P4 being mounted as shown. Input connector pin configurations for P3 and P4 are shown in Figure 5.7-2. Details concerning connector P2 user I/O pins and the use of the external voltage input is shown in Table 5.7-1 and Figure 5.7-3.

The VMIVME-1110 Board is designed with a high quality ground plane that is connected to the VMEbus ground and to alternate input pins on connectors P3 and P4 to provide enhanced noise immunity and more reliable operation. Details concerning input pin connector assignments are shown in Tables 5.7-2 and 5.7-3. A compatible flat-ribbon cable connector for the VMIVME-1110 is Panduit No. 120-964-435E, and a strain relief is Panduit No. 100-000-032.

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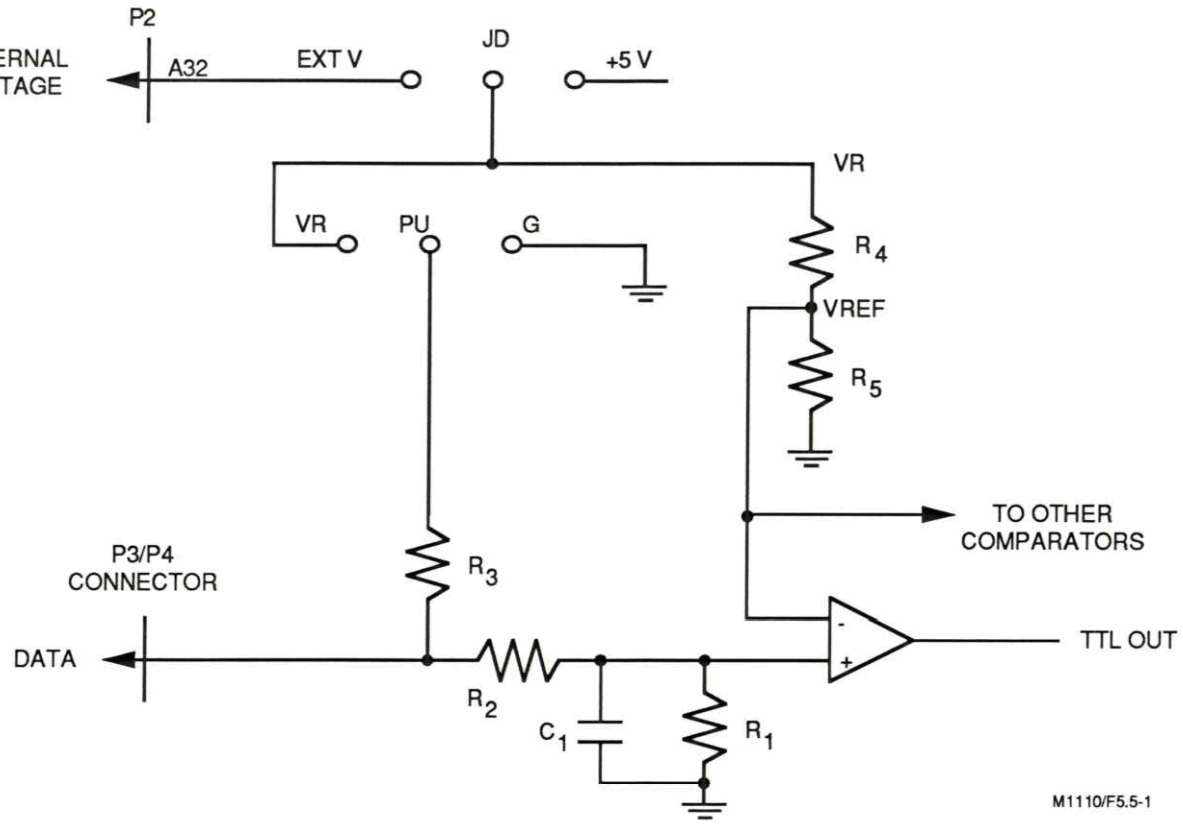


Figure 5.5-1. Signal Conditioning Configuration Selection

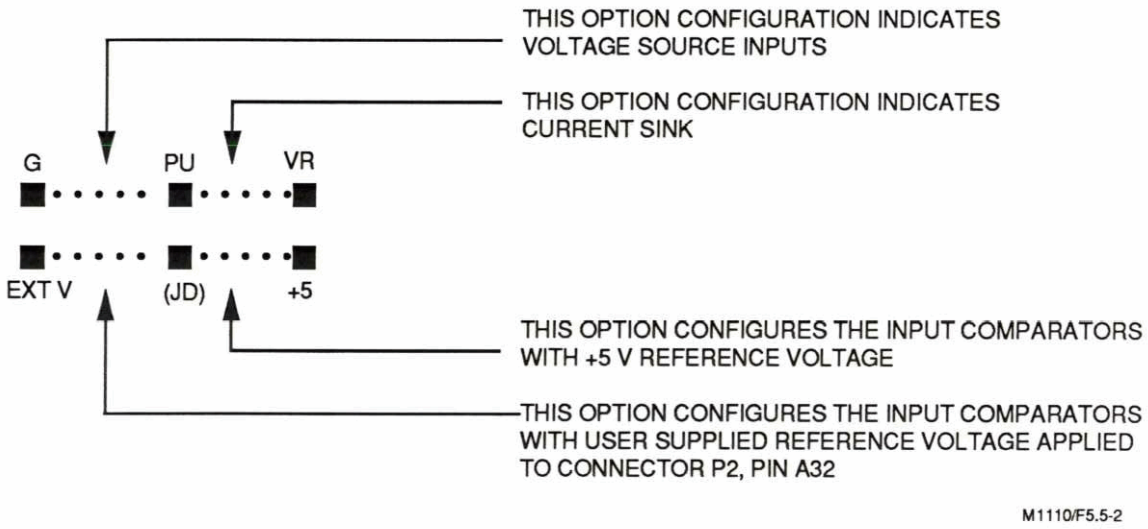


Figure 5.5-2. Jumper Configuration for Pull-up Voltage and Voltage Source/Current Sink Options

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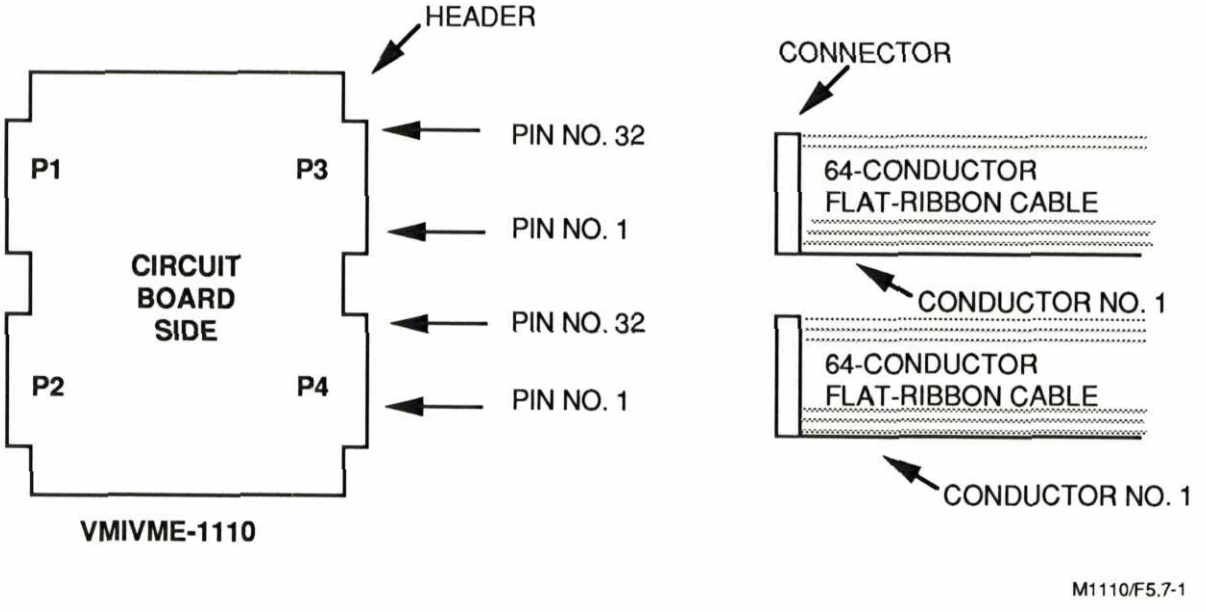


Figure 5.7-1. Cable Connector Configuration

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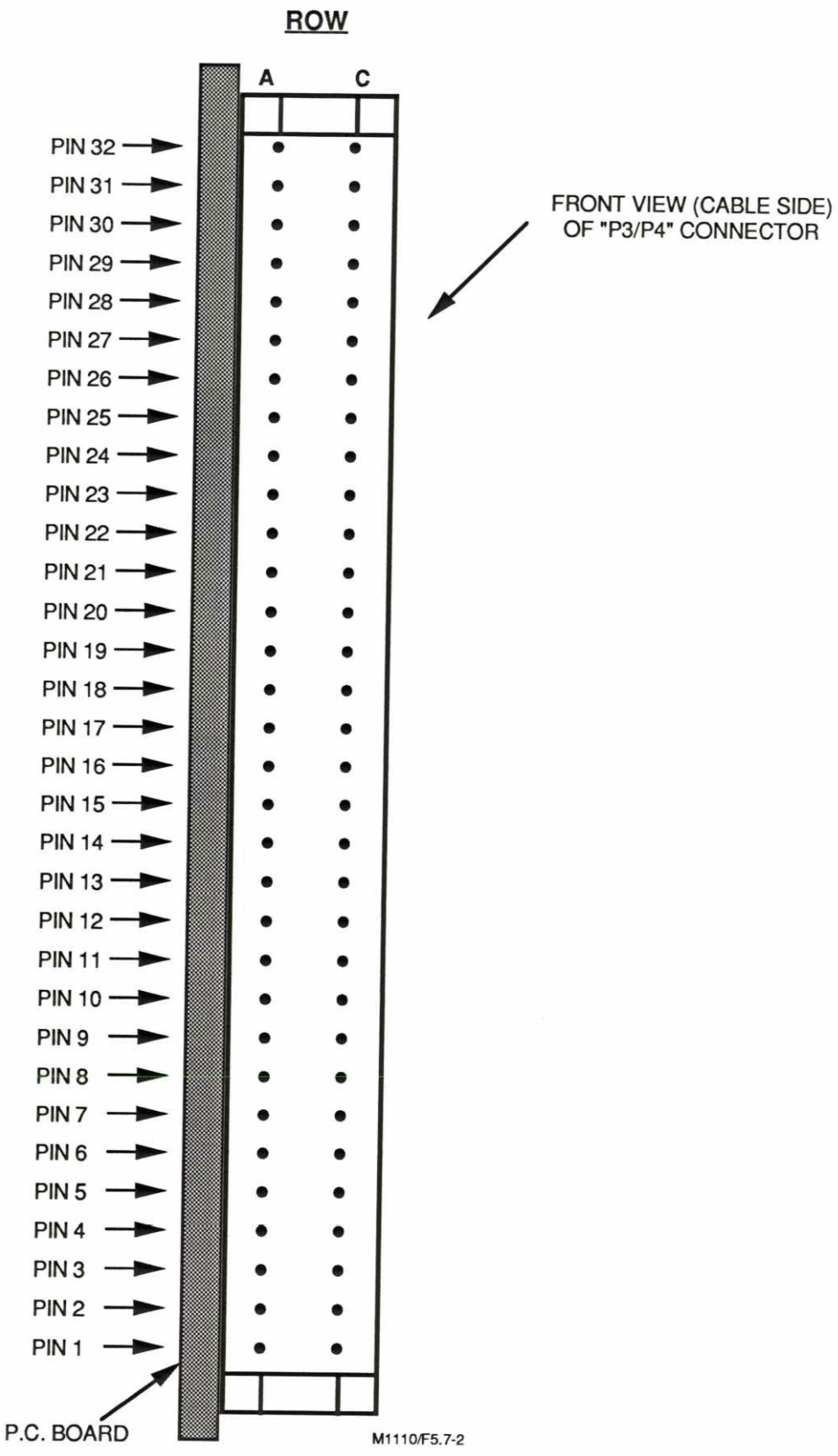


Figure 5.7-2. P3/P4 Connector Pin Layout

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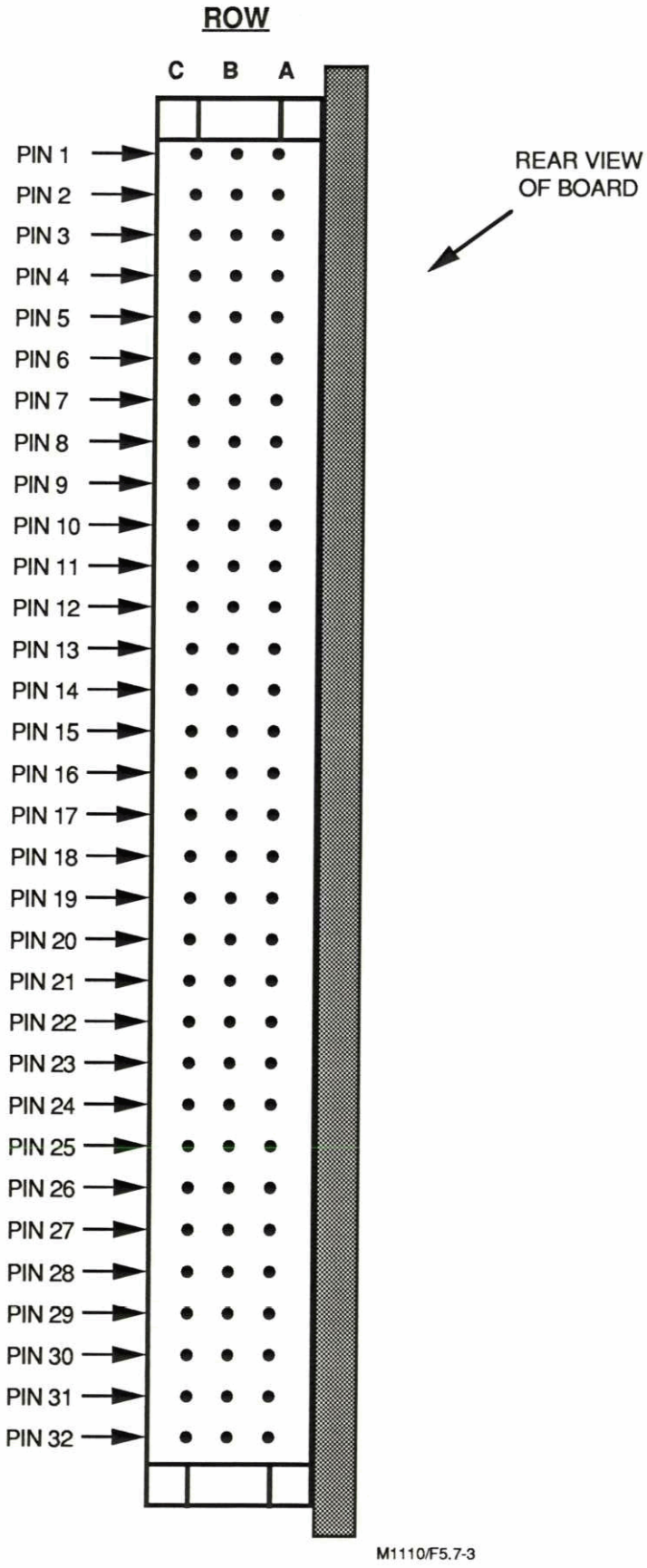


Figure 5.7-3. P1/P2 Connector Pin Layout

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Table 5.7-1. P2 Connector Pin Assignments

PIN NO.	ROW A[1]	ROW B	ROW C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30			
31		GND	
32	Ext V	+5 V	

M1110/T5.7-1

NOTES: 1. External Reference Voltage is supplied by the user.

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Table 5.7-2. P3 Connector Pin Assignments

ROW A PIN	CHANNEL NO.	ROW A PIN	CHANNEL NO.
32	63	16	47
31	62	15	46
30	61	14	45
29	60	13	44
28	59	12	43
27	58	11	42
26	57	10	41
25	56	09	40
24	55	08	39
23	54	07	38
22	53	06	37
21	52	05	36
20	51	04	35
19	50	03	34
18	49	02	33
17	48	01	32

M1110/T5.7-2

NOTE: Row C pins are GND returns for the corresponding input on Row A

Table 5.7-3. P4 Connector Pin Assignments

ROW A PIN	CHANNEL NO.	ROW A PIN	CHANNEL NO.
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00

M1110/T5.7-3

NOTE: Row C pins are GND returns for the corresponding input on Row A

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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