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VMIVME-1128
128-bit Digital Input Board with Built-In-Test (BIT)

Product Manual

A GE Fanuc Company

12090 South Memorial Parkway
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500-001128-000 Rev. N

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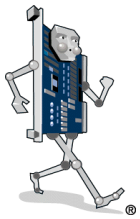
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Overview

Introduction

Features

The VMIVME-1128 Digital Input Board is designed to read a voltage from a variety of devices. The signals may originate from electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, Opto 22 type signal conditioning modules, or numerous other sources. The inputs can be configured to receive current sinking or voltage sourcing signals.

The VMIVME-1128 Digital Input Board has several unique features as specified below:

- 128 bits of voltage sourcing or current sinking digital inputs
- Each group of 8 inputs are jumper-selectable to monitor, voltage source, or current sinking signals
- On-board Built-in-Test logic for fault detection and isolation
- Front panel with Fail LED
- User-selectable input voltage thresholds (0.61 to 34.3 V)
- VMEbus compatible
- 8-, 16-, 32-bit data transfers
- Double Eurocard form factor

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Functional Description

The VMIVME-1128 Board has input circuitry that permits the user to select and configure the basic input functions. The input functions and threshold levels are built into the circuitry. The configuration of the board by the user sets up these functions. This allows the user to set some of the inputs for one function and the rest to another.

The basic function of this board is to sample the external inputs (when the board is accessed by the host) and place this data on the appropriate data lines of the VMEbus. In other words, this board takes a snapshot of the external data and guides it to the host via the VMEbus.

This board supports built-in-testing of its active components. Test registers are mapped into the same addresses as the input registers they are to test. In this way the host simply writes data to an address then reads the same address and compares the data *read* with the data sent to determine the health of the board. Testing can be done with the board off-line or on-line. A Control and Status Register (CSR) is used to control the operating state of the board.

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Reference Material

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
The VMEbus International Trade Association
P O Box 19658
Fountain Hills AZ 85269 USA
Telephone: (480) 837-7486
Email: info@vita.com
www.vita.com

Physical Description and Specifications, refer to *Product Specification, 800-001128-000* available from:
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CHAPTER 1

Theory of Operation

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Introduction

The VMIVME-1128 Digital Input Board is designed to read voltage sourcing or current sinking inputs. The input voltage levels and threshold trip levels are set up by the user.

The VMIVME-1128 is a snapshot type board. When the VMEbus address decoded by this board matches its address, the inputs are stored in an associated input register. The data is then steered to the proper data lines on the backplane for the host to use.

The VMIVME-1128 has Built-in-Test registers (BIT). The BIT registers are used to check the board. The host simply writes data to the register or registers to be checked. Then by reading these registers and comparing the data read to the data written, the user can determine if the board is working. This can be done whenever the user wishes to check the board. The written data will overwrite the external input level.

Figure 1-1 on page 16 is a block diagram of the basic functions of the VMIVME-1128 Board as stated above. These blocks will be discussed in more detail in the following sections.

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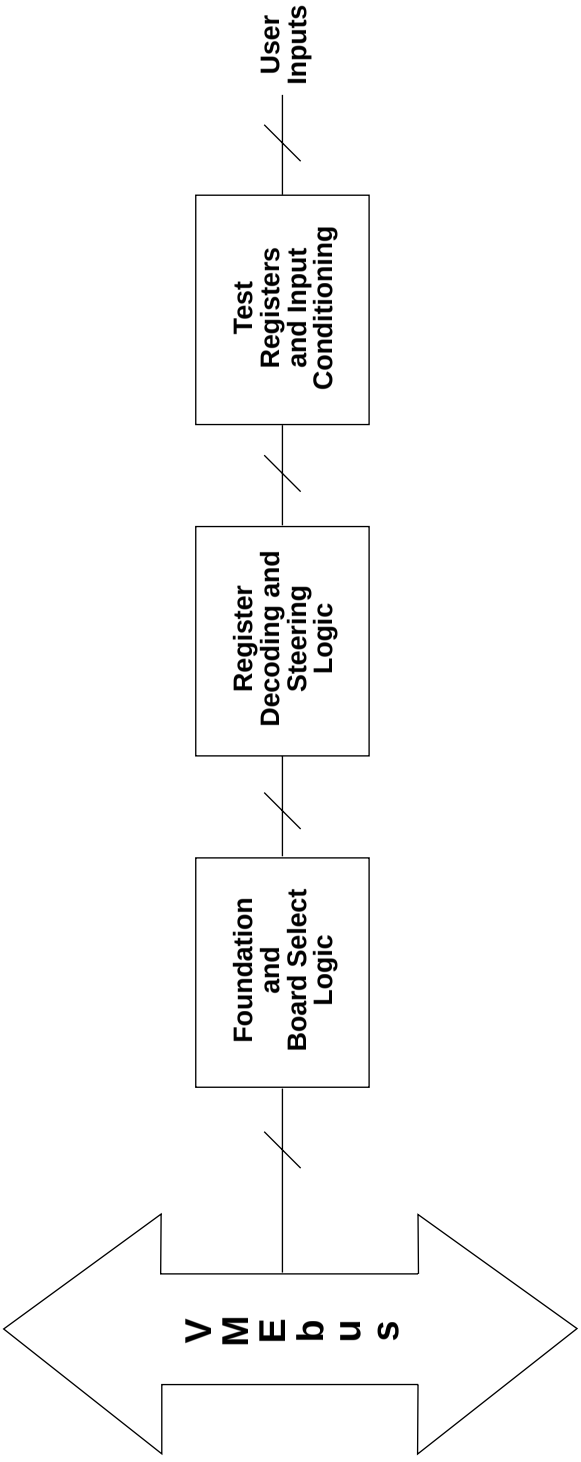


Figure 1-1 Block Diagram of the VMIVME-1128

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Test Registers

The test registers are used to check the "health" of the board. The user writes data into these registers. If their outputs are enabled (TEST MODE active) the data in these registers will overwrite the external inputs. This way the active components can be checked without disconnecting the external inputs. The test registers are mapped into the same address as their corresponding input registers. This way the user simply writes to and then reads from the port to be checked. If the data written is different from the data read, there is a problem. Figure 1-2 below is a block diagram of the Test and Input Data Registers of the VMIVME-1128 Board.

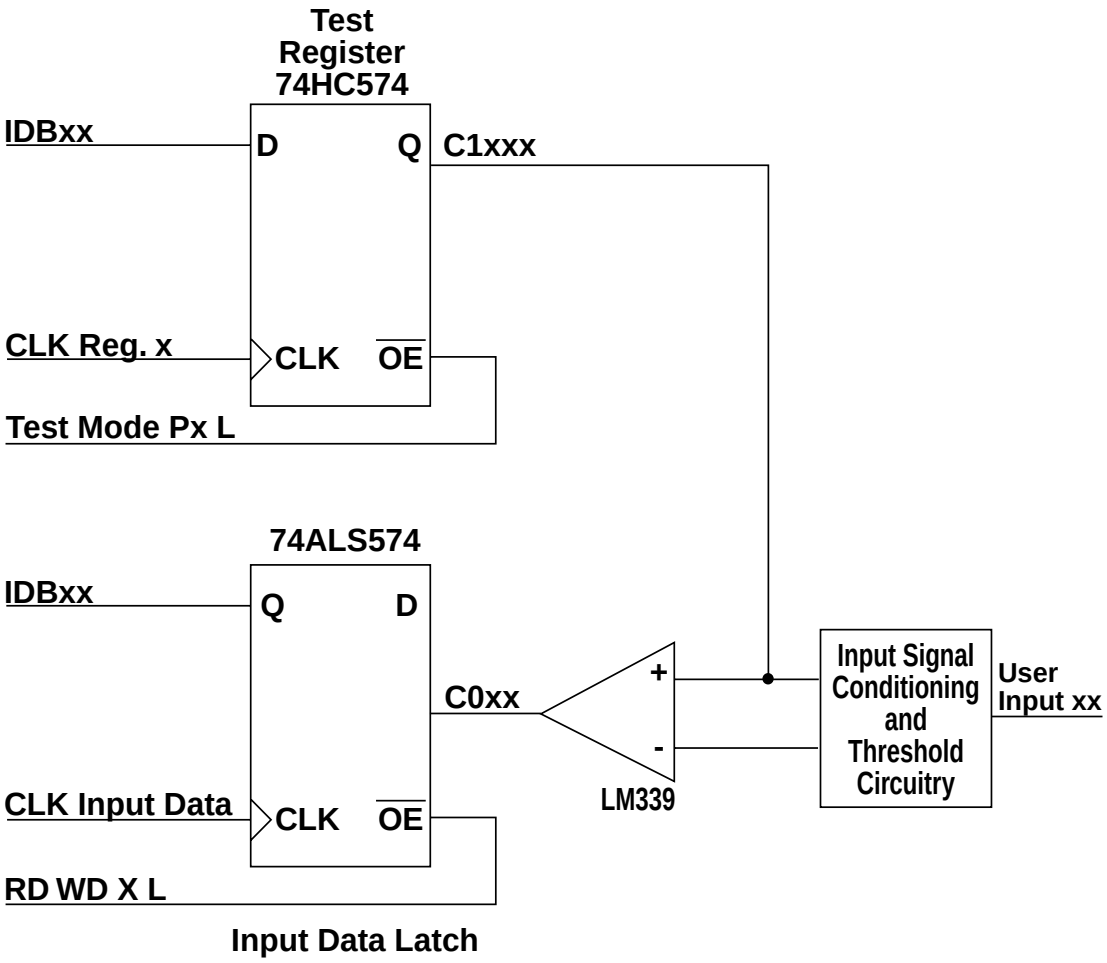


Figure 1-2 VMIVME-1128 Test and Input Data Registers

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Input Circuitry

Figure 1-3 below shows the basic topology for each input. The BIT (Built-in-Test) Register is shown with only one of its eight lines (each register controls eight input circuits). The comparator output goes to an Input Data Register (IDR). When the board is selected these registers are clocked. This is the snapshot effect. The incoming data is then held in these registers while the board guides the data to the appropriate VMEbus data lines.

The input circuit of Figure 1-3 below uses RPA, RPD, and associated header to set the threshold (or trip) level for the comparator. The threshold is approximately 51 percent of the maximum input voltage. Table 2-1 on page 21 is a detailed listing of the thresholds for some common input levels. The threshold equation is also provided. The user can use this to calculate the trip voltage for the specific input voltage range he is using.

Input Types

The inputs can be configured in one of two types; either as voltage sourcing or current sinking. In the voltage sourcing input setup RPA's jumper is grounded. The input must be a voltage across RPA. RPD has its jumper going to a voltage the user chooses. The voltage chosen will establish the threshold level for the input voltage. Please refer to Table 2-1 on page 21 for the actual value of the trip voltage.

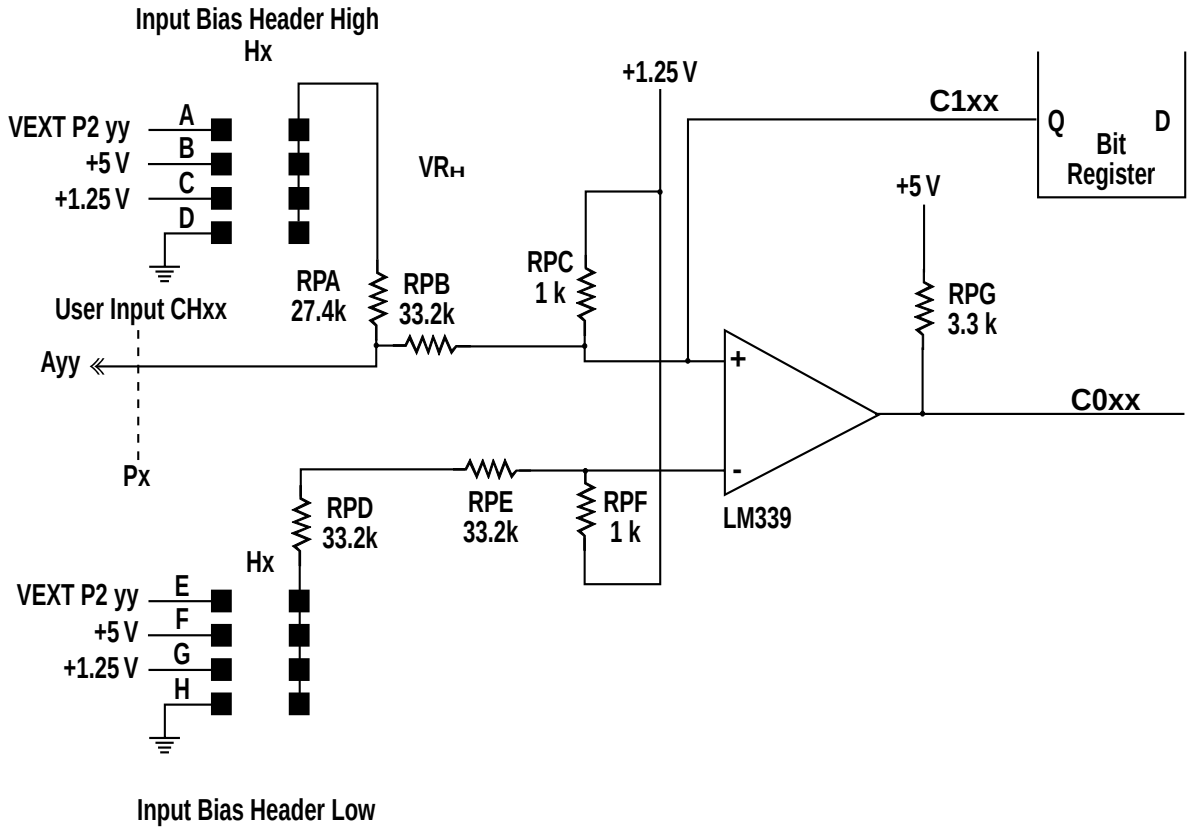


Figure 1-3 Basic Input Circuit Topology

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CHAPTER 2

Configuration and Installation

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning the disposition of the damaged item(s).

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Board Configuration

The VMIVME-1128 circuitry permits the user to configure the inputs based on the application. The following sections of the manual are intended to instruct the user in the implementation of these input configurations. The user must first decide which input topology to use: the inputs can receive either current sinking or voltage sourcing signals. Next, the user must select a threshold level; the threshold can be set as shown in Table 2-1 below. The input channels are configured in groups of 8 so the channels can be set-up on a byte-by-byte basis.

Table 2-1 Threshold Voltages

$Vt = 0.51\ VR_L + 0.61$	
VR_L	**Vt**
0 V	0.61 V
1.25 V	1.25 V
5 V	3.2 V
12 V	6.7 V
24 V	12.9 V
28 V	14.8 V
48 V	25.1 V
66 V	34.3 V

Input Topology

The input topology is configured by placing jumpers in certain positions of a header field. Figure 2-1 on page 22 shows the circuit topology for a current sink input. Figure 2-2 on page 23 shows a voltage source input. Jumper J1 selects the pull-up voltage applied to input resistor RPA and J2 selects the reference voltage applied to the threshold resistor RPD. Jumpers J1 and J2 in these figures represent the jumpers used to control a group of 8 input channels. The physical location of these jumpers is shown in Figure 2-4 on page 25.

If J1 is in the ground position, the input circuit is voltage sourcing (see Figure 2-2 on page 23). In any other position, the input is current sinking. In the circuit shown in Figure 2-1 on page 22, the pull-up voltage VR_H is 5 V. If the voltage you are using is greater than 5 V, then you should use V_{EXT} for J1. Table 2-2 on page 26 shows the location of V_{EXT} for each group of channels.

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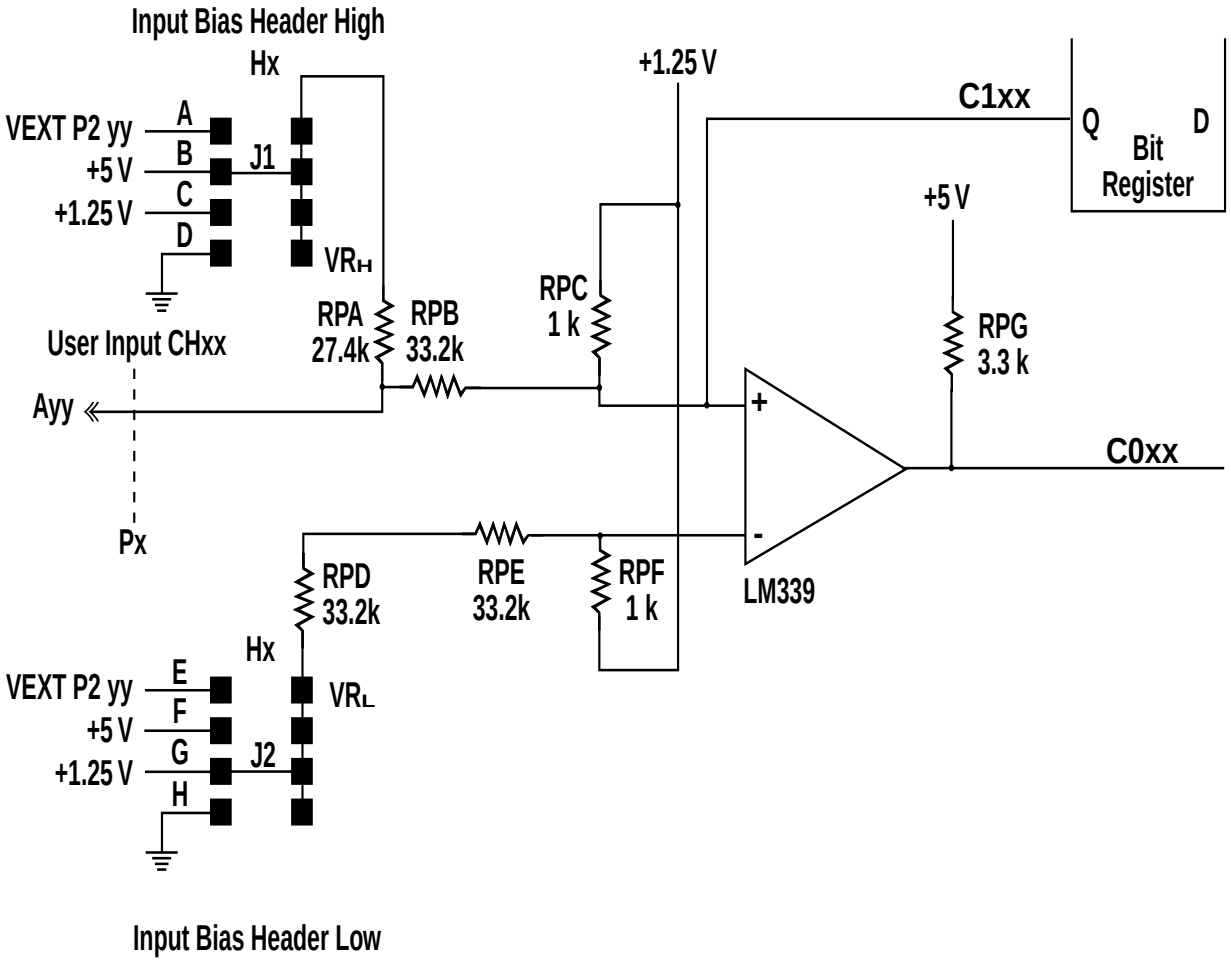


Figure 2-1 Basic Current Sinking Input

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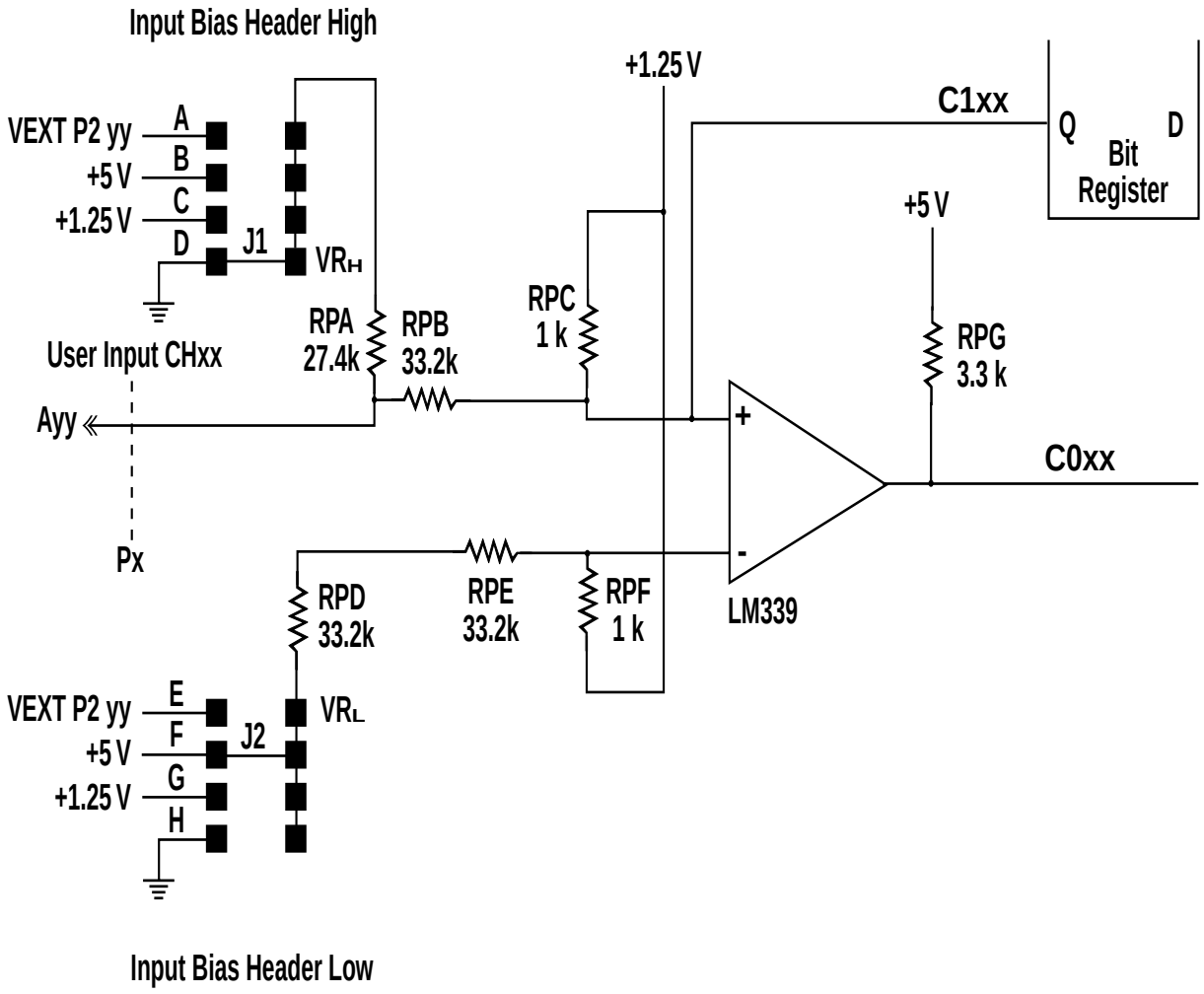
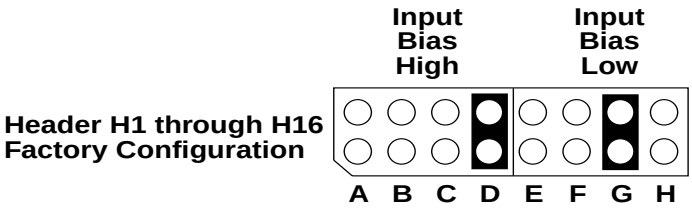


Figure 2-2 Basic Voltage Sourcing Input

Jumper J2 chooses the reference voltage (VR_L) for the threshold level (V_t). Table 2-1 on page 21 lists several threshold values as a function of reference voltage. An equation for the threshold voltage is given if the value you require is not listed. Figure 2-2 describes the possible jumper configurations.

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		A	B	C	D
Input Bias Low Jumper Location	E	T = CS Vp = V_{EXT} V_{OC} = Eq 2 V_T = Eq 1	T = CS Vp = +5 V V_{OC} = +3.35 V V_T = Eq 1	T = CS Vp = +1.25 V V_{OC} = +1.25 V V_T = Eq 1	T = VS V_T = Eq 1
	F	T = CS Vp = V_{EXT} V_{OC} = Eq 2 V_T = +3.2 V	T = CS Vp = +5 V V_{OC} = +3.35 V V_T = +3.2 V	**Not Used**	T = VS V_T = +3.2 V
	G	T = CS Vp = V_{EXT} V_{OC} = Eq 2 V_T = +1.25 V	T = CS Vp = +5 V V_{OC} = +3.35 V V_T = +1.25 V	**Not Used**	**Factory Configuration** T = VS V_T = +1.25 V
	H	T = CS Vp = V_{EXT} V_{OC} = Eq 2 V_T = +0.61 V	T = CS Vp = +5 V V_{OC} = +3.35 V V_T = +0.61 V	**Not Used**	T = VS V_T = +0.61 V

T = Input Circuit Topology
VS = Voltage Sourcing Input
CS = Current Sinking Input
V_T = Threshold Voltage
V_P = Pull-Up Voltage (applied to 27 k_ pull-up resistor)
V_{OC} = Open Circuit Input Voltage
Eq 1 = 0.51 VR_L + 0.61
Eq 2 = 0.56 VR_H + 0.55

Figure 2-3 Input Circuitry Jumper Configuration

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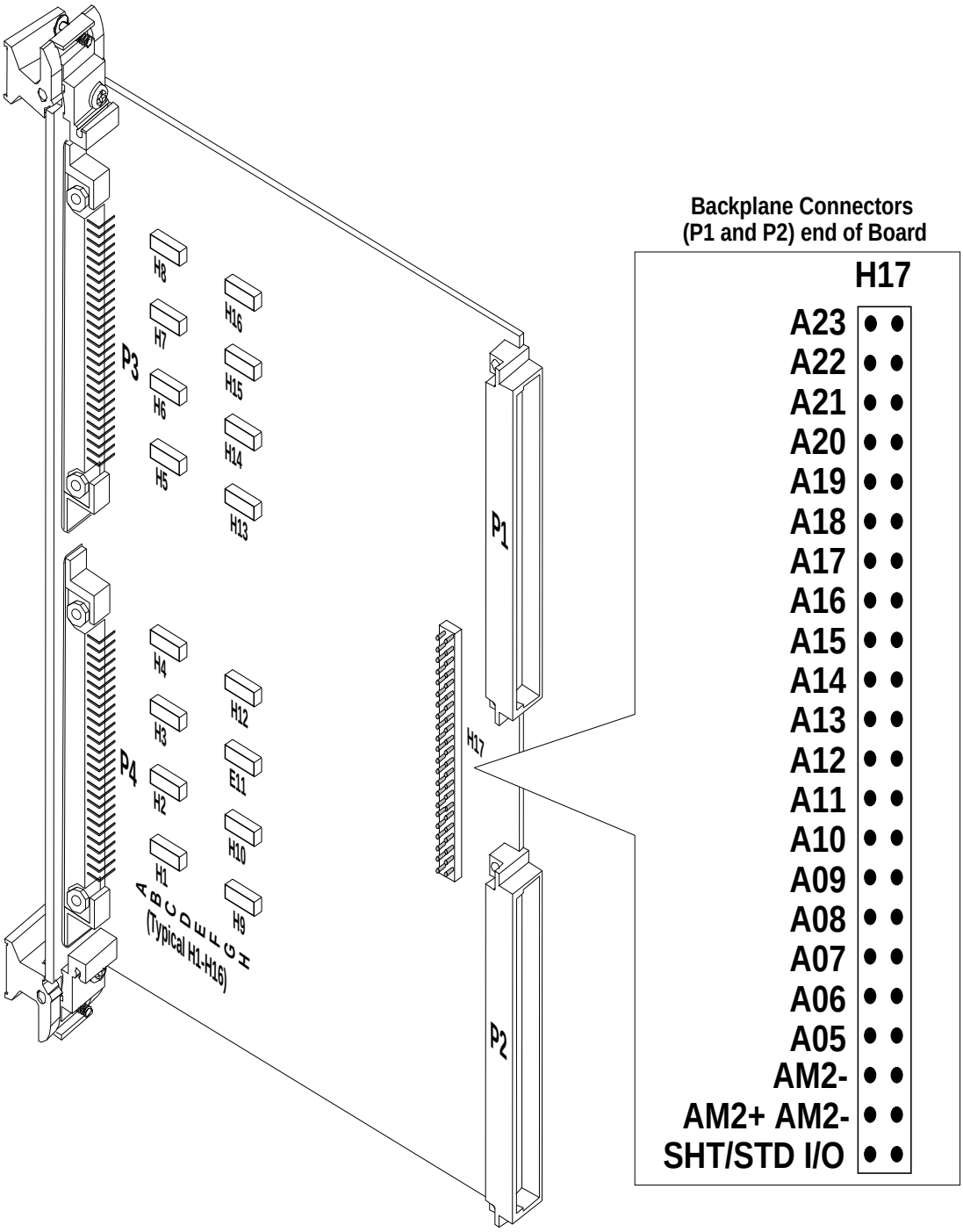


Figure 2-4 Physical Location of Jumpers

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Table 2-2 Header Assignments

Header Ref. Des.	Associated Channels	Location of V_{EXT}
H1	CH07 - CH00	P2-C32
H2	CH15 - CH08	P2-C30
H3	CH23 - CH16	P2-C28
H4	CH31 - CH24	P2-C26
H5	CH64 - CH71	P2-C16
H6	CH72 - CH79	P2-C14
H7	CH80 - CH87	P2-C12
H8	CH88 - CH95	P2-C10
H9	CH32 - CH39	P2-C24
H10	CH40 - CH47	P2-C22
H11	CH48 - CH55	P2-C20
H12	CH56 - CH63	P2-C18
H13	CH103 - CH96	P2-C8
H14	CH111 - CH104	P2-C6
H15	CH119 - CH112	P2-C4
H16	CH127 - CH120	P2-C2

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Before Applying Power: Checklist

Before installing the board in a VMEbus system, perform the following checklist to verify the board is ready for the intended operation:

1. Have Sections 1 and 3 on Theory and Programming of the VMIVME-1128 been read and applied to system requirements?
2. Review this chapter to verify factory installation of the jumpers. See Figure Figure 2-4 on page 25 for factory configuration.
   - To change the address jumpers, refer to Figure 2-11 on page 31.
   - To change the address modifier response, refer to Figure 2-5 through Figure 2-10.
3. The VMIVME-1128 is designed to accommodate either current sink or voltage source inputs. See Figure 2-1 and Figure 2-2, respectively, for the correct configuration of the desired input.
4. Have the cables, with proper mating connectors, been connected to the input connectors? Refer to *I/O Cable and Front Panel Connector Configuration* on page 32.

After completing the checklist, the VMIVME-1128 Board may be installed. Generally the VMIVME-1128 may be installed in any slot position except slot one which is usually reserved for the system controller processing unit.

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Address Modifiers

The VMIVME-1128 is configured at the factory, as shown in Figure 2-5, to respond to short supervisory I/O access. This configuration can be changed by installing jumpers at the appropriate locations in header H17 as shown in the corresponding figures.

I/O Access	Corresponding Figure
Short Supervisory	Figure 2-5 below
Standard Supervisory	Figure 2-6 on page 29
Short Nonprivileged	Figure 2-7 on page 29
Standard Nonprivileged	Figure 2-8 on page 29
Short (responds to either supervisory or nonprivileged)	Figure 2-9 on page 30 (factory configuration)
Standard (responds to either supervisory or nonprivileged)	Figure 2-10 on page 30

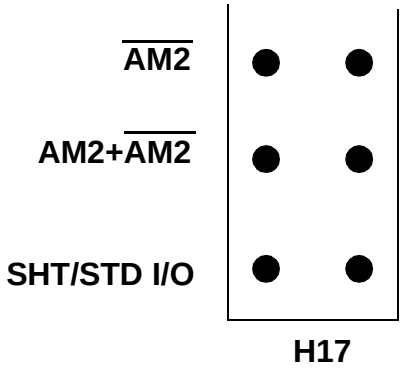


Figure 2-5 Jumper Configuration for Short Supervisory Access

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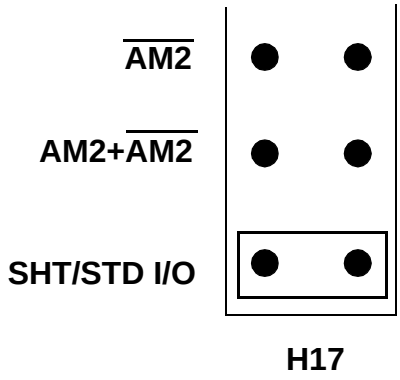


Figure 2-6 Jumper Configuration for Standard Supervisory Access

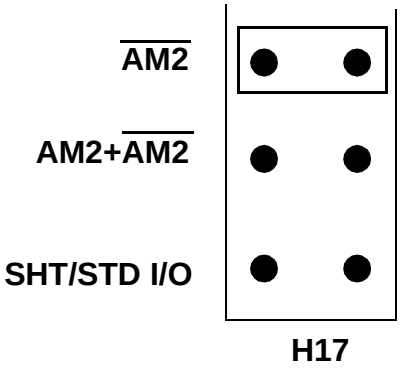


Figure 2-7 Jumper Configuration for Short Nonprivileged Access

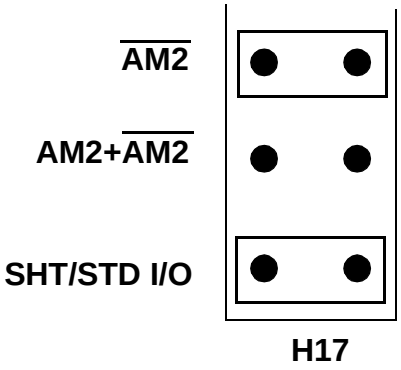


Figure 2-8 Jumper Configuration for Standard Nonprivileged Access

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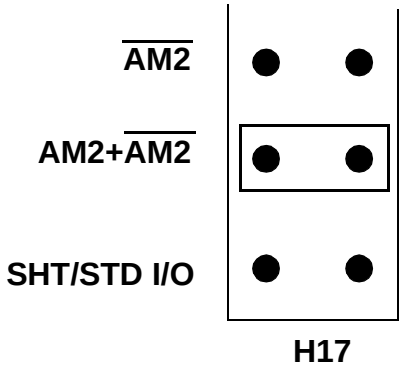


Figure 2-9 Jumper Configuration for Short Addressing and Supervisory or Nonprivileged Access

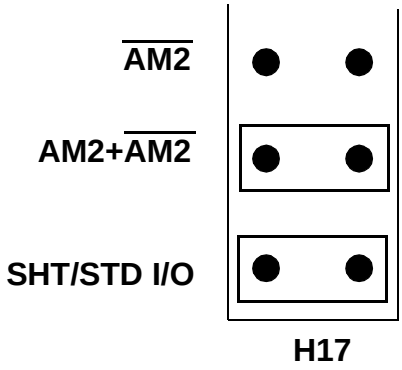


Figure 2-10 Jumper Configuration for Standard Addressing and Supervisory or Nonprivileged Access

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Address Selection Jumpers

The VMIVME-1128 is designed with a bank of address select jumpers that specify the beginning board address for data transfers. An installed jumper equals zero; a removed jumper equals one. The address selection jumpers are shown in Figure 2-11 below. The VMIVME-1128 is factory configured to respond to 0000 HEX.

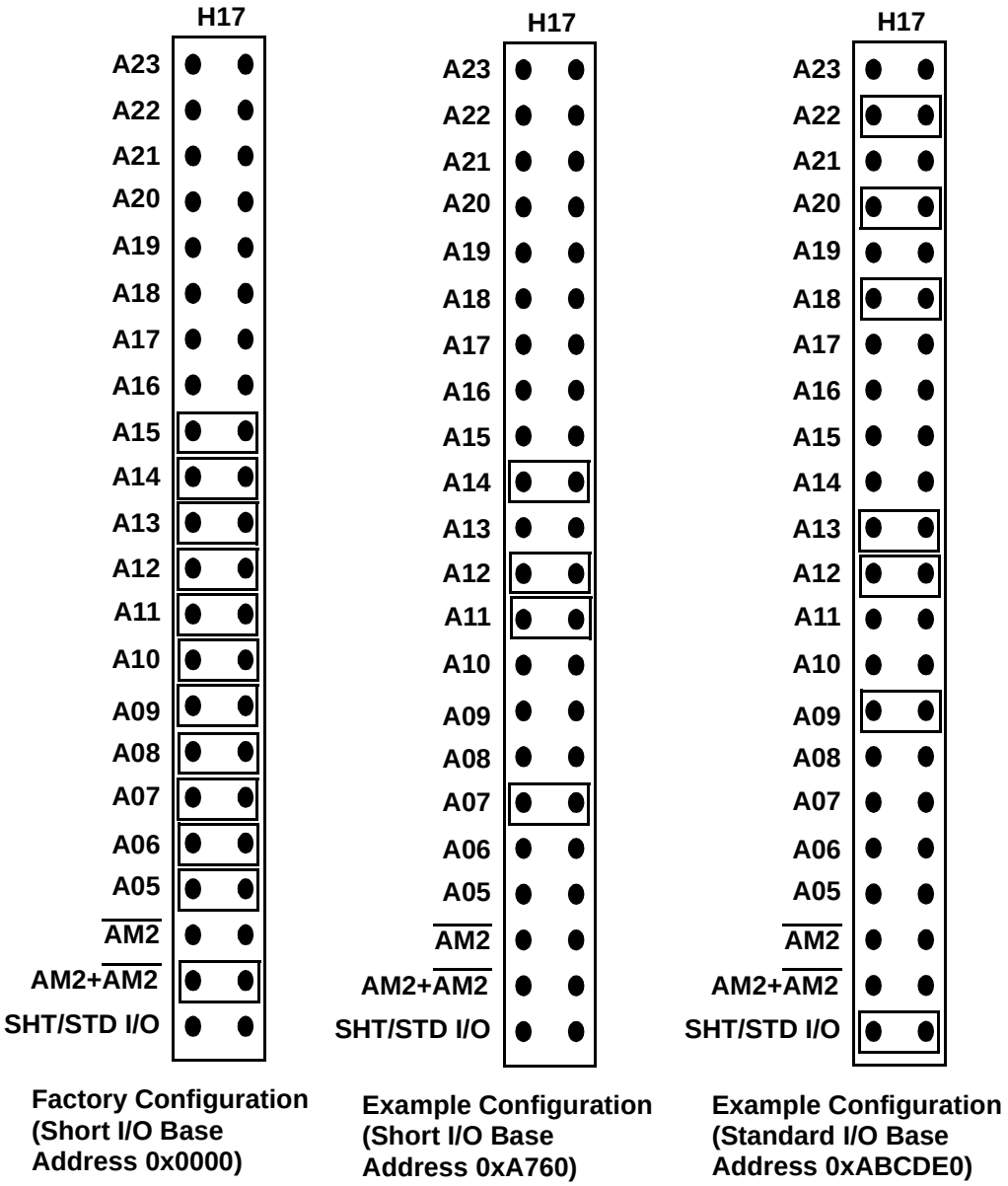


Figure 2-11 Base Address Select Jumpers

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I/O Cable and Front Panel Connector Configuration

The input connectors (P3 and P4) on the VMIVME-1128 are 96-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Document No. 825-000000-006) for additional information concerning the variety of possible cable and connector types available.

Figure 2-12 below shows the pin layout of the P3 and P4 connectors. Table 2-3 on page 33 and Table 2-4 on page 34 detail the connector pin assignments. The P2 connector pin layout is shown in Figure 2-13 on page 35, while the pin assignments are listed in Table 2-5 on page 36.

We recommend ERNI female connectors part no. 913.031. Because of the density involved, 33 MIL flat cable should be used for mass termination connectors.

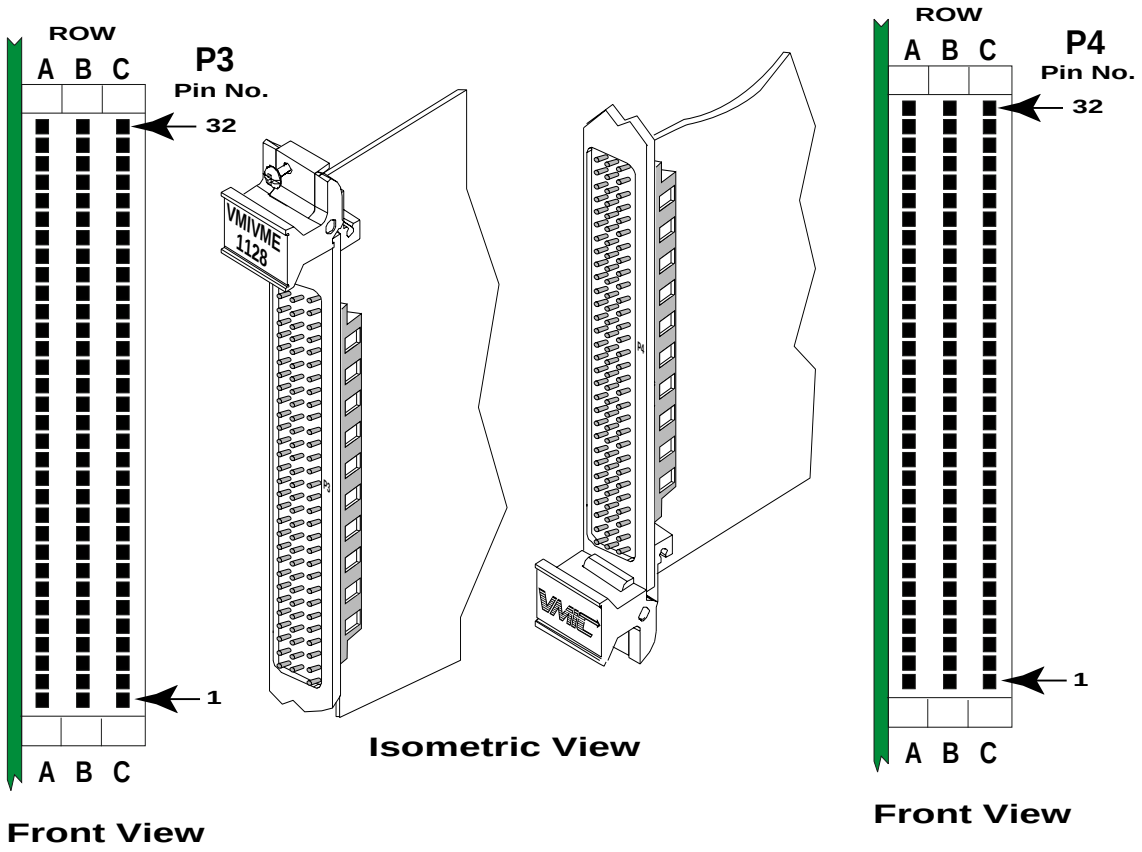


Figure 2-12 P3/P4 Connector Pin Layout

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Table 2-3 P3 Pin - Channel Assignments

P3		P3	
ROW C PIN	**CHANNEL No.**	**ROW C PIN**	**CHANNEL No.**
32	127	16	111
31	126	15	110
30	125	14	109
29	124	13	108
28	123	12	107
27	122	11	106
26	121	10	105
25	120	09	104
24	119	08	103
23	118	07	102
22	117	06	101
21	116	05	100
20	115	04	99
19	114	03	98
18	113	02	97
17	112	01	96
All Pins in Row B are Grounded.			

P3		P3	
ROW A PIN	**CHANNEL No.**	**ROW A PIN**	**CHANNEL No.**
32	95	16	79
31	94	15	78
30	93	14	77
29	92	13	76
28	91	12	75
27	90	11	74
26	89	10	73
25	88	09	72
24	87	08	71
23	86	07	70
22	85	06	69
21	84	05	68
20	83	04	67
19	82	03	66
18	81	02	65
17	80	01	64
All pins in Row B are Grounded.			

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Table 2-4 P4 Pin - Channel Assignments

P4		P4	
ROW C PIN	**CHANNEL No.**	**ROW C PIN**	**CHANNEL No.**
32	63	16	47
31	62	15	46
30	61	14	45
29	60	13	44
28	59	12	43
27	58	11	42
26	57	10	41
25	56	09	40
24	55	08	39
23	54	07	38
22	53	06	37
21	52	05	36
20	51	04	35
19	50	03	34
18	49	02	33
17	48	01	32
All pins in Row B are Grounded.			

P4		P4	
ROW A PIN	**CHANNEL No.**	**ROW A PIN**	**CHANNEL No.**
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00
All pins in Row B are Grounded.			

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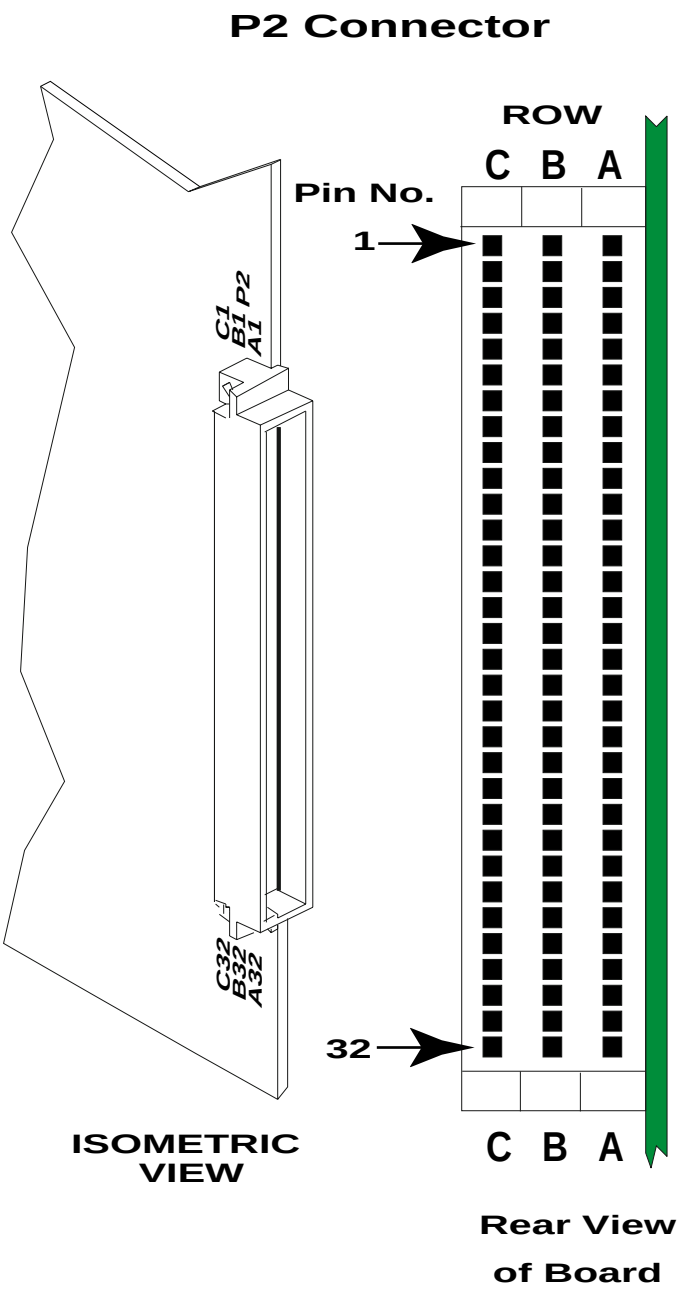


Figure 2-13 P2 Connector Pin Layout

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Table 2-5 P2 Connector Pin Assignments

PIN NO.	ROW A	ROW B	ROW C
1	GND	+5 VOLTS	GND
2	GND	GND	VEXT CH 120_127
3	GND	N / C	GND
4	GND	N / C	VEXT CH 112_119
5	GND	N / C	GND
6	GND	N / C	VEXT CH 104_111
7	GND	N / C	GND
8	GND	N / C	VEXT CH 96_103
9	GND	N / C	GND
10	GND	N / C	VEXT CH 88_95
11	GND	N / C	GND
12	GND	GND	VEXT CH 80_87
13	GND	+5 VOLTS	GND
14	GND	D16	VEXT CH 72_79
15	GND	D17	GND
16	GND	D18	VEXT CH 64_71
17	GND	D19	GND
18	GND	D20	VEXT CH 56_63
19	GND	D21	GND
20	GND	D22	VEXT CH 48_55
21	GND	D23	GND
22	GND	GND	VEXT CH 40_47
23	GND	D24	GND
24	GND	D25	VEXT CH 32_39
25	GND	D26	GND
26	GND	D27	VEXT CH 24_31
27	GND	D28	GND
28	GND	D29	VEXT CH 16_23
29	GND	D30	GND
30	GND	D31	VEXT CH 8_15
31	GND	GND	GND
32	GND	+5 VOLTS	VEXT CH 0_7

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Test Mode Selection

At power up both test mode bits are active which places all channels on the P3 and P4 connectors in their test mode. While in test mode, data written to the test registers can be read back through the input circuitry thereby verifying its readiness. To return to normal operation, bits 14 and 13 of the CSR must be set to a "one".

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CHAPTER

3

Programming

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Introduction

The VMIVME-1128 is a snapshot board. The user simply performs a read or write operation within the board's address space and the appropriate transfer is performed. The only setup involved with this board deals with the Control and Status Register. Once this register is programmed, the user performs data transfers to or from this board.

Table 3-1 on page 40 lists the address map for the VMIVME-1128. Xs in the address are determined by the address select header H17. This header's function is discussed in more detail in *Configuration and Installation* section on page 19 of this manual. This board responds to nonprivileged, supervisory, or both accesses depending on how the AM2 and X TO (AM2) jumpers are positioned.

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Table 3-1 Address Map

Relative Address*	Mnemonic	Name/Function
XXX0 0000	IDU	Board ID Register Upper Byte
XXX0 0001	IDL	Board ID Register Lower Byte
XXX0 0010	CSRU	Control and Status Register (CSR) Upper Byte
XXX0 0011	CSRL	Control and Status Register (CSR) Lower Byte
XXX0 0100 through XXX0 1111 Not Used**		
XXX1 0000	DR0U	Test Register 0 Upper Byte
XXX1 0001	DR0L	Test Register 0 Lower Byte
XXX1 0010	DR1U	Test Register 1 Upper Byte
XXX1 0011	DR1L	Test Register 1 Lower Byte
XXX1 0100	DR2U	Test Register 2 Upper Byte
XXX1 0101	DR2L	Test Register 2 Lower Byte
XXX1 0110	DR3U	Test Register 3 Upper Byte
XXX1 0111	DR3L	Test Register 3 Lower Byte
XXX1 1000	DR4U	Test Register 4 Upper Byte
XXX1 1001	DR4L	Test Register 4 Lower Byte
XXX1 1010	DR5U	Test Register 5 Upper Byte
XXX1 1011	DR5L	Test Register 5 Lower Byte
XXX1 1100	DR6U	Test Register 6 Upper Byte
XXX1 1101	DR6L	Test Register 6 Lower Byte
XXX1 1110	DR7U	Test Register 7 Upper Byte
XXX1 1111	DR7L	Test Register 7 Lower Byte

* The relative address is defined by A4-A0. All other address lines help to define the base address.
** A read or write access to these addresses will not result in a bus error; however, any data written to these addresses will not be stored. Any data read from these addresses will not be meaningful.

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Board ID Register (BD ID)

The BD ID Register is a read-only register. Its data is fixed at $1C00. You can write to this address; however, the data you write will be lost and there will be no effect on the board. If you choose to write to this location, the board will DTACK to prevent any bus errors. The BD ID can be read as a word or as two bytes. Table 3-2 below shows the bit values for this register.

Table 3-2 BD ID Register Bit Map

XXX0 0000			Board ID Upper Byte				(Read Only)
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
0	0	0	1	1	1	0	0

XXX0 0001			Board ID Lower Byte				(Read Only)
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
0	0	0	0	0	0	0	0

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CSR Bit Definitions

The CSR is a 16-bit register that is used to control the board's Fail LED and the test registers' outputs. Table 3-3 below shows the bits used to perform these functions. Bit 15 controls the LED. Bit 14 controls the test registers for P4 and P3 Row A (Channels 0 through 31 and Channels 64 through 95) while Bit 13 controls the test registers for P4 and P3 Row C (Channels 32 through 64 and Channels 96 through 127). P3 and P4 channel assignments are shown in Table 2-3 on page 33 and Table 2-4 on page 34. The BIT map for each channel is shown in Table 3-4 on page 43.

Bits 15, 14 and 13 are active low (0 = ON, 1 = OFF). All other bits are read only and will read as a low. When the board is powered up or after a system reset, these signals are activated. Writing a logic high into each bit location will deactivate them. Writing a logic low in these locations will subsequently activate the function. Each of the functions are independent of the others. Thus, the LED can be turned on and off as you wish.

Table 3-3 CSR Bit Map

XXX0 0010		CSR Upper Byte			(Bits 12 through 08 are Read-Only)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fail_L	Test_ Mode_ P3/P4 Row A-L	Test_ Mode_ P3/P4 Row C-L	L	L	L	L	L

XXX0 0011		CSR Lower Byte			(Read-Only)		
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
L	L	L	L	L	L	L	L

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Input Registers Bit Definitions

Table 3-4 below lists the input channels and their associated register bit locations. The internal data bit can be used as a guide to locate an input channel when you are doing a longword transfer. When doing word or byte transfers the even address bytes will go to bits 15 through 8 on the VMEbus data bus while the odd address bytes go to bits 7 through 0.

Table 3-4 Input Data Registers Bit Map

XXX1 0000	Data Register 0 Upper Byte						(Read/Write)
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120

XXX1 0001	Data Register 0 Lower Byte						(Read/Write)
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	CH 112

XXX1 0010	Data Register 1 Upper Byte						(Read/Write)
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104

XXX1 0011	Data Register 1 Lower Byte						(Read/Write)
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 103	CH 102	CH 101	CH 100	CH 099	CH 098	CH 097	CH 096

XXX1 0100	Data Register 2 Upper Byte						(Read/Write)
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH 095	CH 094	CH 093	CH 092	CH 091	CH 090	CH 089	CH 088

XXX1 0101	Data Register 2 Lower Byte						(Read/Write)
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH 087	CH 086	CH 085	CH 084	CH 083	CH 082	CH 081	CH 080

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Table 3-4 Input Data Registers Bit Map (Continuation)

XXX1 0110	Data Register 3 Upper Byte					(Read/Write)	
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 079	CH 078	CH 077	CH 076	CH 075	CH 074	CH 073	CH 072

XXX1 0111	Data Register 3 Lower Byte					(Read/Write)	
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 071	CH 070	CH 069	CH 068	CH 067	CH 066	CH 065	CH 064

XXX1 1000	Data Register 4 Upper Byte					(Read/Write)	
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH 063	CH 062	CH 061	CH 060	CH 059	CH 058	CH 057	CH 056

XXX1 1001	Data Register 4 Lower Byte					(Read/Write)	
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH 055	CH 054	CH 053	CH 052	CH 051	CH 050	CH 049	CH 048

XXX1 1010	Data Register 5 Upper Byte					(Read/Write)	
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 047	CH 046	CH 045	CH 044	CH 043	CH 042	CH 041	CH 040

XXX1 1011	Data Register 5 Lower Byte					(Read/Write)	
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 039	CH 038	CH 037	CH 036	CH 035	CH 034	CH 033	CH 032

XXX1 1100	Data Register 6 Upper Byte					(Read/Write)	
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH 031	CH 030	CH 029	CH 028	CH 027	CH 026	CH 025	CH 024

XXX1 1101	Data Register 6 Lower Byte					(Read/Write)	
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH 023	CH 022	CH 021	CH 020	CH 019	CH 018	CH 017	CH 016

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Table 3-4 Input Data Registers Bit Map (Concluded)

XXX1 1110	Data Register 7 Upper Byte				(Read/Write)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 015	CH 014	CH 013	CH 012	CH 011	CH 010	CH 009	CH 008

XXX1 1111	Data Register 7 Lower Byte				(Read/Write)		
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 007	CH 006	CH 005	CH 004	CH 003	CH 002	CH 001	CH 000

Please note that input channels CH00 through CH63 come from input connector P4 while inputs CH64 through CH127 come via P3.

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Built-In-Test (BIT) Programming

Built-in-Test is activated when either or both test mode bits in the CSR are set low. With test mode active, data patterns written to the tested data registers will overwrite any external input data, and these patterns will be read back. If there is a difference, then the board has a problem. When you are through testing the board, the test mode bits **MUST** be set to a "one" in the CSR; otherwise, the board will not be able to monitor the external inputs.

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Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com

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Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.

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