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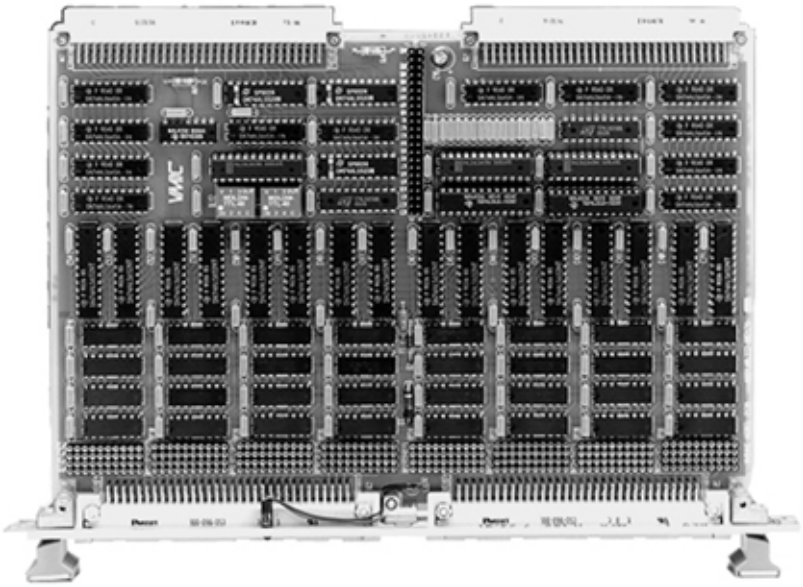
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GE Fanuc Automation



VMIVME-2128

128-bit High-Voltage Digital Output Board

PRODUCT MANUAL
500-002128-000 REV. K

Embedded Systems

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Table of Contents

Overview 11

Reference Material List 12
Safety Summary 13
Ground the System 13
Do Not Operate in an Explosive Atmosphere 13
Keep Away from Live Circuits 13
Do Not Service or Adjust Alone 13
Do Not Substitute Parts or Modify System 13
Dangerous Procedure Warnings 13
Safety Symbols Used in This Manual 14

Chapter 1 - Theory of Operation 15

Operational Overview 17
Device Addressing 17
VME Foundation Logic 17
Data Transfers 17
Register Control Logic 18
Built-In-Test (BIT) 19
Output Drivers 19
P2 User Ground Option 19

Chapter 2 - Configuration and Installation 21

Unpacking Procedures 22
Jumper and Switch Locations 23
Address Modifiers 23
Address Selection Jumpers 25
I/O Cable and Front Panel Connector Configuration 25
Optional USER Grounds 33

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Warming Resistors 33

Chapter 3 - Programming 35

Register Map 36
CSR and ID Register Map 37
Output Data Register 38
Detailed Programming 40
Output Data Transfers 40
Built-in-Test 40

Maintenance 43

Maintenance Prints 44

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List of Figures

Figure 1-1 VMIVME-2128 Functional Block Diagram 16
Figure 1-2 Address Selection Block Diagram 17
Figure 1-3 Data Transfer Block Diagram 18
Figure 1-4 Output Driver Circuitry 20
Figure 2-1 Jumper Locations 24
Figure 2-2 Jumper Configuration for Short Supervisory Access 26
Figure 2-3 Jumper Configuration for Standard Supervisory Access 26
Figure 2-4 Jumper Configuration for Short Nonprivileged Access 26
Figure 2-5 Jumper Configuration for Standard Nonprivileged Access 27
Figure 2-6 Jumper Configuration for Short Addressing and Supervisory or Nonprivileged Access . . 27
Figure 2-7 Jumper Configuration for Standard Addressing and Supervisory or Nonprivileged Access 27
Figure 2-8 Base Address Select Jumpers 28
Figure 2-9 P2 Connector - Pin Layout 29
Figure 2-10 P3 Connector - Pin Layout 30
Figure 2-11 P4 Connector - Pin Layout 31
Figure 2-12 Cable Connector Configuration 32
Figure 3-1 Programming Flowchart (Built-in-Test Active) 41
Figure 3-2 Programming Flowchart (Built-in-Test Not Active) 42

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List of Tables

Table 2-1	P2 Connector Pin Assignments	29
Table 2-2	P3 Pin - Channel Assignments	30
Table 2-3	P4 Pin - Channel Assignments	31
Table 3-1	Data Register Address Map	36
Table 3-2	CSR and ID Register Bit Map	37
Table 3-3	Output Data Register Bit Map	38
Table 3-3	Output Data Register Bit Map (Continued)	39

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Overview

Introduction

The VMIVME-2128 is capable of delivering 128 channels of high voltage and/or high current sink outputs. The VMIVME-2128 open collector output drivers are capable of supporting output voltages from 5 to 48VDC. A unique feature of the VMIVME-2128 Board is the Built-in-Test (BIT) logic, which allows the user, under software control, to verify the operation of each channel.

A brief overview of the VMIVME-2128's features include the following:

- 128 channels of high voltage digital outputs (5 to 48VDC)
- 8-, 16- or 32-bit VME data transfers
- High current open collector drivers (600mA sink) with built-in suppressor diodes
- Outputs may be paralleled for higher drive capability
- Open collector pull-up resistors (optional)
- Fault protection for the outputs (outputs shutdown when current exceeds 1.0A)
- Built-in-Test logic
- Front panel software controlled Fail LED (for Built-in-Test)
- User configurable address jumpers allow for contiguous addressing when more than one board is used in a VME system

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Reference Material List

For a detailed explanation of the VME and its characteristics, refer to "The VMEbus Specification" available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(480) 951-8866
FAX: (480) 951-0720
www.vita.com

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

GE Fanuc Embedded Systems assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc Embedded Systems for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual

STOP: This symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: This sign denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: This sign denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, practice, or condition which is essential to highlight.

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CHAPTER

1

Theory of Operation

Contents

Operational Overview 17

Introduction

The VMIVME-2128 is designed for a variety of applications such as:

- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepper motor drivers
- LED drivers
- High-current, high-voltage drivers
- Fiber-optic LED drivers

The VMIVME-2128 also supports a variety of output voltages. Please contact Sales for ordering options.

The design of the VMIVME-2128 Board as shown in the functional block diagram in Figure 1-1 on page 16 consists primarily of four sections:

- VME Foundation Logic
- Device Addressing
- Output Drivers
- Built-in-Test Logic

The VMIVME-2128 Board supports eight 16-bit bi-directional registers, a Control and Status Register (CSR), high performance output drivers, typical VME foundation logic and a device address jumper bank. The jumper bank provides the user with the capability to select the VMIVME-2128 base address.

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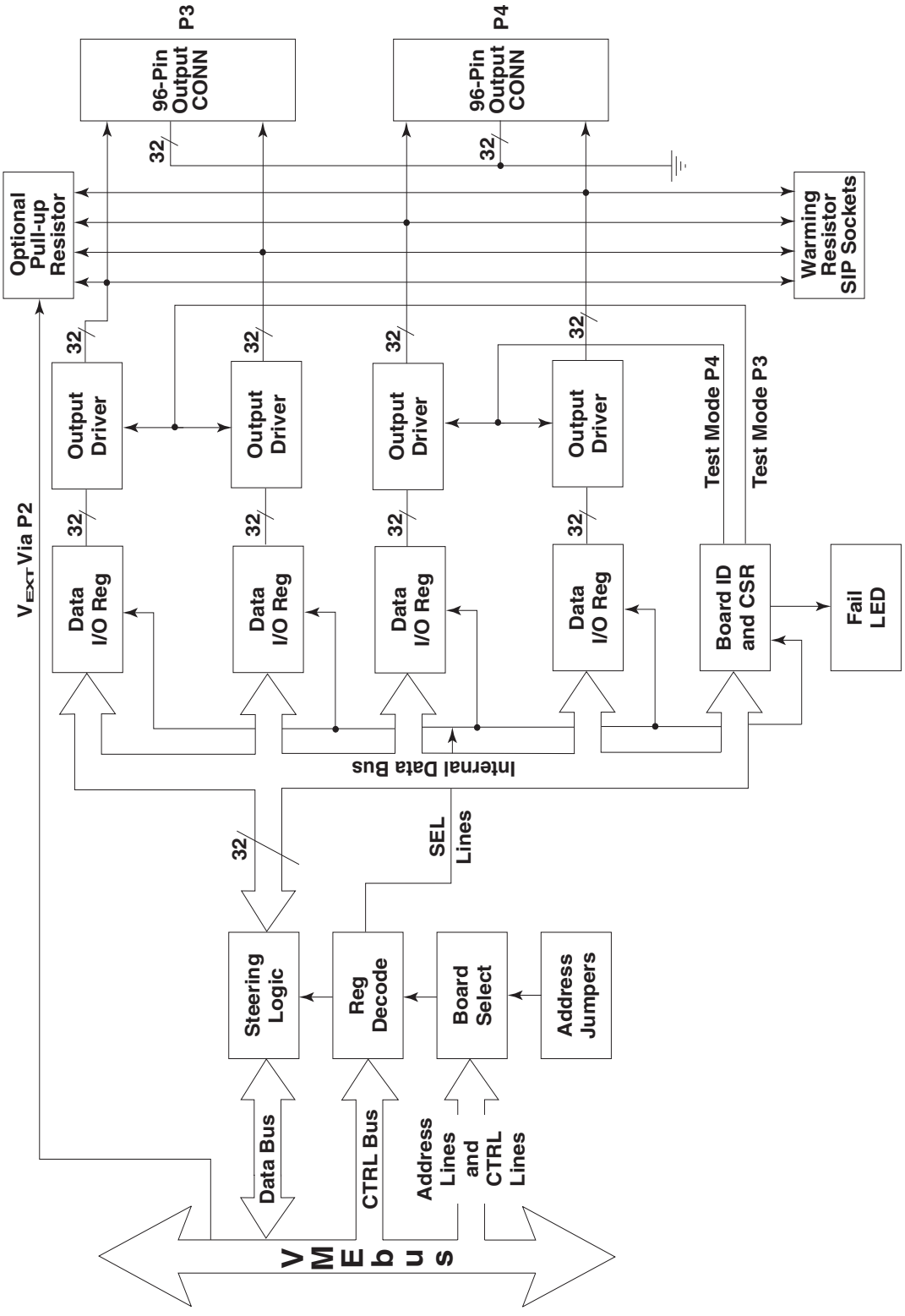


Figure 1-1 VMIVME-2128 Functional Block Diagram

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Operational Overview

Device Addressing

The VMIVME-2128 supports data transfers in short or standard I/O memory space with supervisory and/or nonprivileged data access. Jumpers are provided as shown in Figure 1-2 below, allowing user selection of either I/O access type. The VMIVME-2128 is factory configured to respond to short supervisory I/O access.

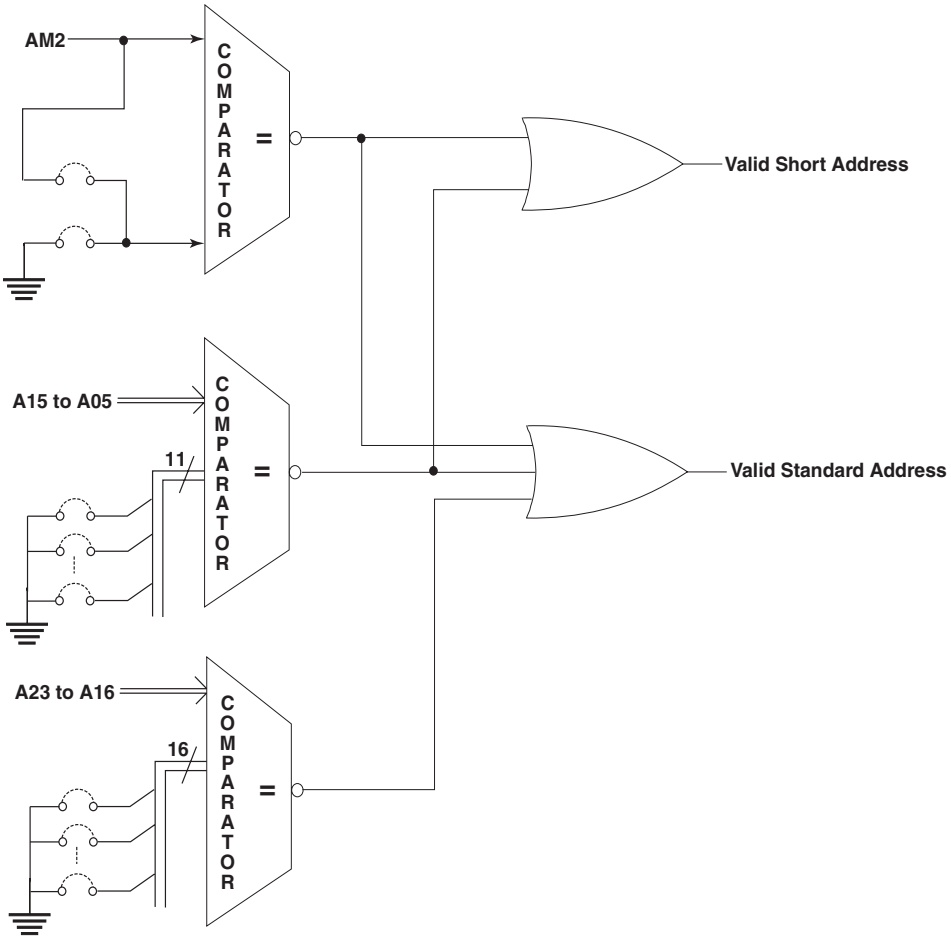


Figure 1-2 Address Selection Block Diagram

VME Foundation Logic

The typical VME foundation logic is comprised of drivers, receivers and control logic. The DTACK generator is designed to provide high data transfer rates.

Data Transfers

Data transfer transceivers are shown in Figure 1-3 on page 18. The data transceivers are designed to support write and read operations on 8-, 16- and 32-bit boundaries.

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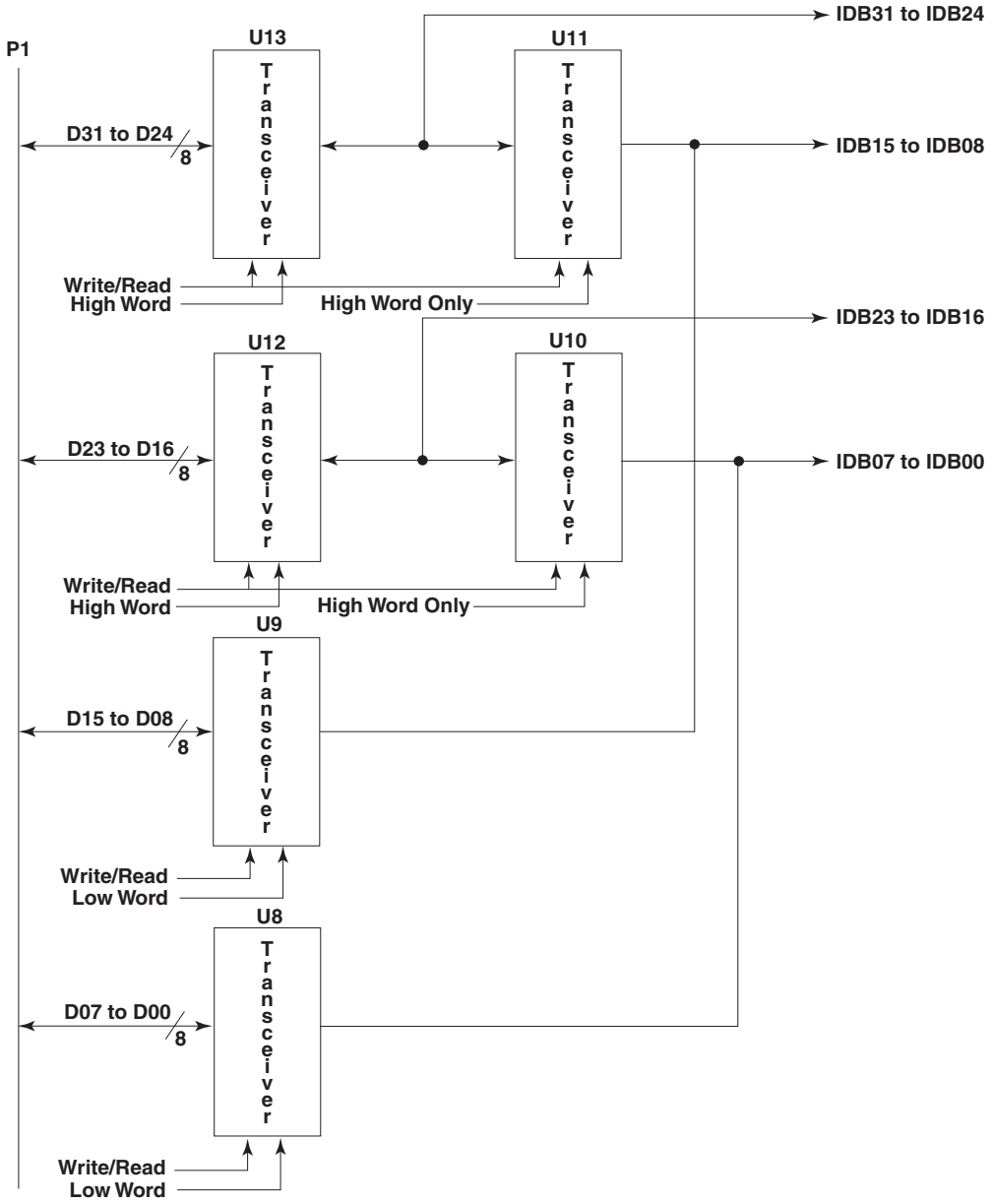


Figure 1-3 Data Transfer Block Diagram

Register Control Logic

The VMIVME-2128 Board register control logic is designed to support *write* and *read* operations to and from eight 16-bit bi-directional dual port latches and from a CSR register that controls the test mode and front panel LED.

To perform output data transfers, data is transferred via transceivers, which are selected by address bits A4, A3, A2, A1 and the data strobes. The 128 bits of high voltage outputs are addressable as four 32-bit longwords, eight 16-bit words or as sixteen 8-bit bytes.

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Built-In-Test (BIT)

The Built-in-Test feature of the VMIVME-2128 is enabled by asserting the test mode bits in the CSR. While in test mode, test data may be written to any Output Data Register (ODR), and read back on a *read* operation. While in test mode, all drivers are off (tri-state). The ODRs may be read at any time independent of the test mode bits.

The Built-in-Test features of this product provide the user with the capability of performing real-time loopback testing with the output drivers connected and off-line diagnostic testing with the output drivers disconnected from the field devices.

A front panel Fail LED is provided for quick fault isolation to the board level. The Fail LED is illuminated at power-up or system reset, and may be extinguished by the user upon successful diagnostic execution.

Output Drivers

Figure 1-4 on page 20 is an illustration of the Output Drivers, providing the user with thermal and inrush current shutdown protection. The inrush current protection will allow up to 990mA of surge current before shutting down the driver. This current is determined by the type and number of loads used. For example, if the load per channel is two 48mA, 28V parallel lamps, they may have as much as 960mA ((40mA x 2) x 12 = 960mA) of cold filament inrush current per channel. If the inrush current of the external circuitry per channel will exceed the 990mA limit, then warming resistors should be used. These resistors should draw approximately 10 percent of the rated (warm) lamp load current. For the example above, this current would be 8mA ((40mA x 2) x 0.1 = 8mA). SIP resistor sockets are provided on the board for these warming resistors. These resistors must be the bussed type with pin 1 being common. The sockets have pin 1 grounded. The wattage rating of these SIP resistors should be sufficient to handle the dissipation required.

The output driver user load return currents must be provided the lowest resistance return path possible to the user voltage supply. These return currents must not be allowed to flow through the VME backplane digital ground return. They must flow back through the front panel connectors P3 and P4 B-row pins to the user supply or through the P2 connector pins A1 through A26 if the P2 user ground option is ordered. If the user ground is of insufficient quality that the user load return currents flow onto the backplane digital ground, the fuse F1 will blow and render the board inoperative. The function of this fuse is to protect the backplane digital ground pins, since they are not rated for the magnitude of user load currents this board is capable of handling. Blown fuses usually indicate poor user ground quality. The fuse circuit is necessary for digital input ground returns for control signals to the output driver.

P2 User Ground Option

The User Grounds are connected to all B row pins of front panel connectors P3 and P4. If the P2 USER GROUND option is ordered, then these grounds are also routed to the backplane P2 connector's A1 through A26 pins by installing shorting bars SB1 through SB4 (RP33 through 36). The external supply's ground (user ground) can now be accessed from the P2 backplane connector of the VME chassis. All 26 wires are needed to provide a low resistance return path for the user load currents. For a typical 300mA/channel load, the currents can be as much as 1.48A/Wire (128 channels x 300mA/channel/26 wires = 1.48A/wire). Each wire not used means that its current must be shared by the remaining wires. For example, from the calculation each wire will carry 1.48A and a 28 AWG solid wire can carry 2.2A with a 10°C temperature rise. Thus, 28 AWG wire or larger should be used.

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CAUTION: Care must be taken not to exceed the maximum current rating of the connector pins.

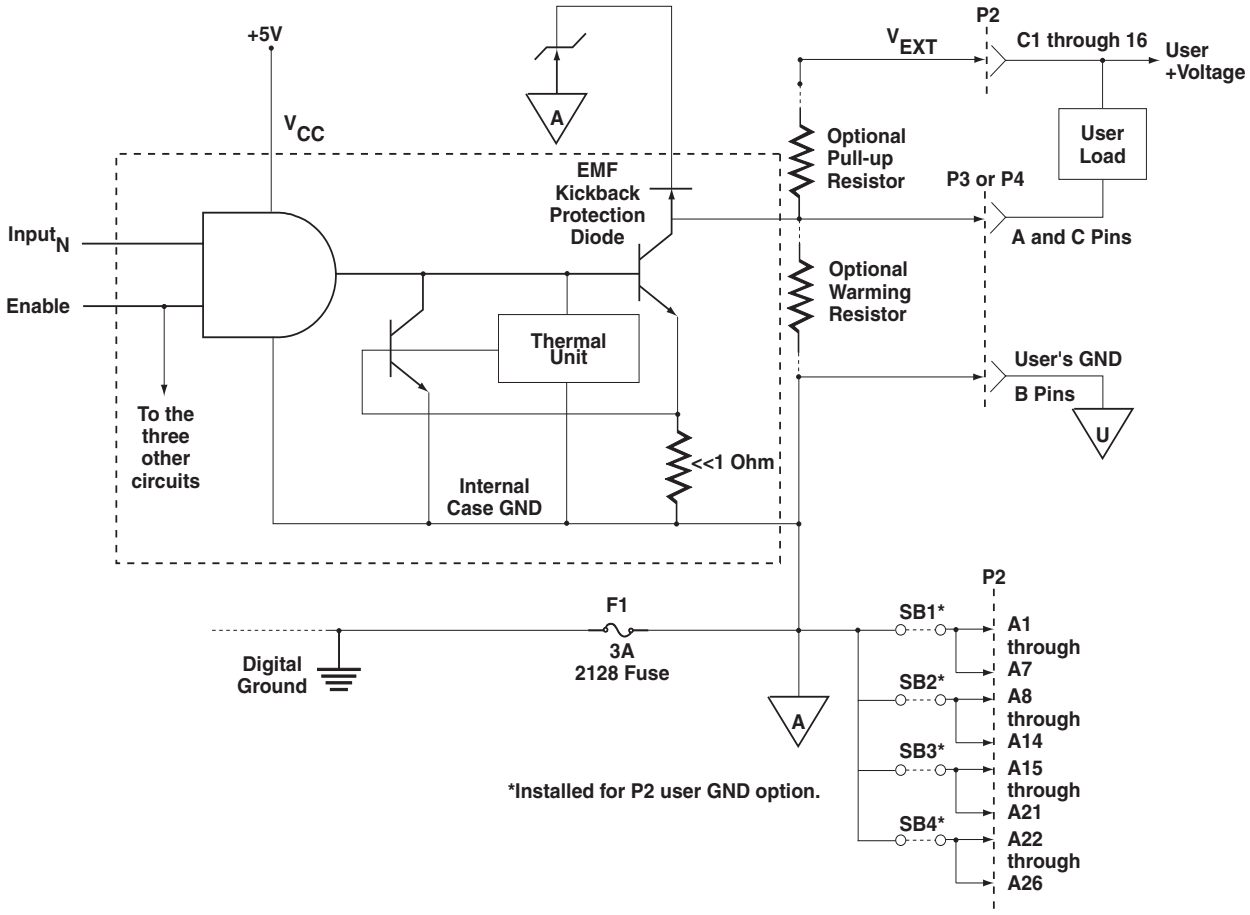


Figure 1-4 Output Driver Circuitry

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CHAPTER 2

Configuration and Installation

Contents

Unpacking Procedures 22
Jumper and Switch Locations 23

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMIVME-2128.

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Unpacking Procedures

CAUTION: Some of the components assembled on GE Fanuc Embedded Systems' products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc Embedded Systems, together with a request for advice concerning the disposition of the damaged item(s).

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Jumper and Switch Locations

The physical locations of the jumpers described in this section are shown in Figure 2-1 on page 24.

Address Modifiers

The VMIVME-2128 is configured at the factory, as shown in Figure 2-2 on page 26, to respond to short supervisory I/O access. This configuration can be changed by installing jumpers at the appropriate locations in header H1 as shown in the corresponding figures.

I/O Access	Corresponding Figure
Short Supervisory	Figure 2-2 on page 26
Standard Supervisory	Figure 2-3 on page 26
Short Nonprivileged	Figure 2-4 on page 26
Standard Nonprivileged	Figure 2-5 on page 27
Short (Responds to either Supervisory or Nonprivileged)	Figure 2-6 on page 27
Standard (Responds to either Supervisory or Nonprivileged)	Figure 2-7 on page 27

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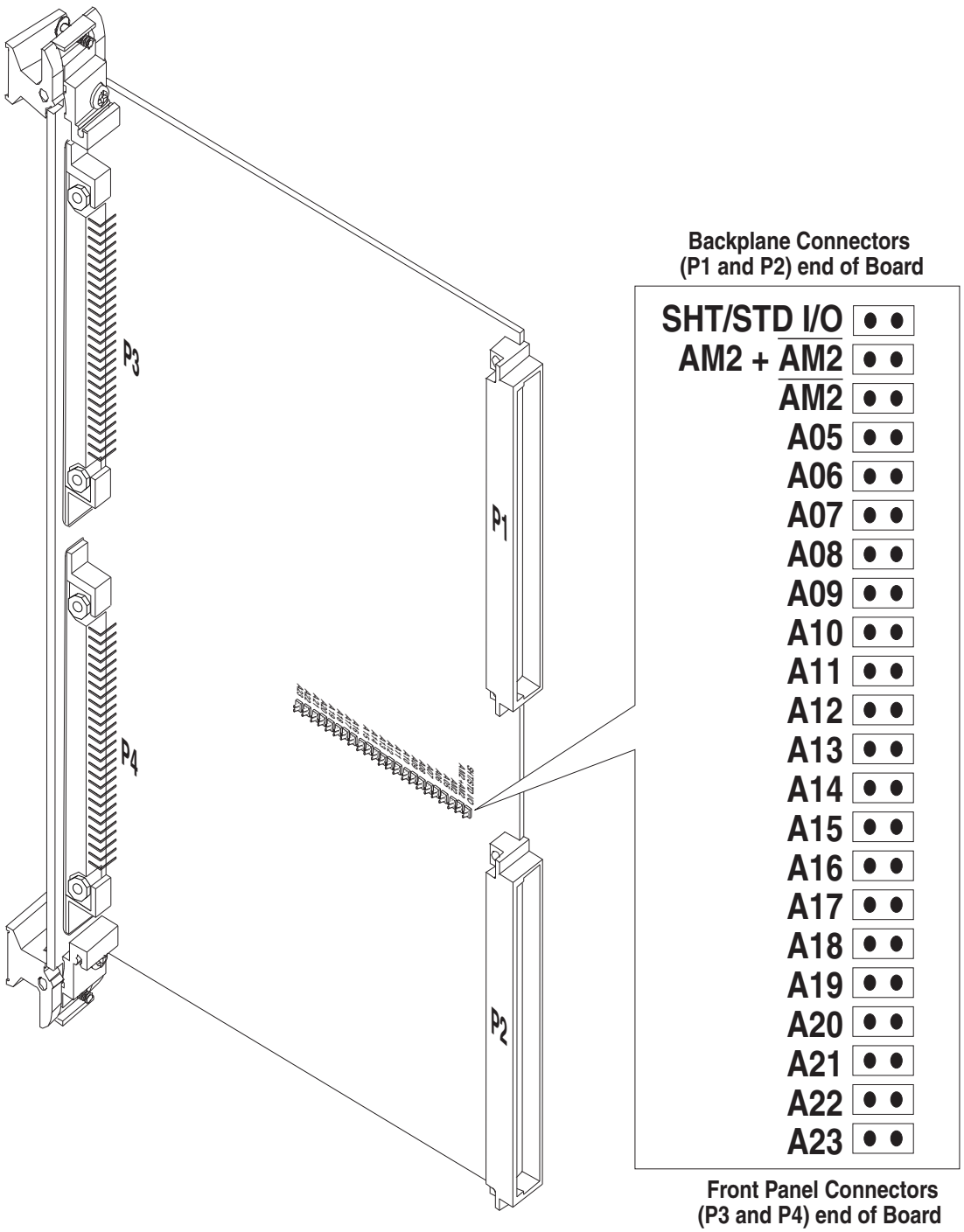


Figure 2-1 Jumper Locations

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Address Selection Jumpers

The VMIVME-2128 is designed with a bank of address select jumpers that specify the beginning board address for data transfers. The address selection jumpers are shown in Figure 2-8 on page 28. An installed jumper equals zero; an omitted jumper equals one. The VMIVME-2128 is factory configured to respond to 0000 HEX in short supervisory space.

I/O Cable and Front Panel Connector Configuration

The output connectors (P3 and P4) on the VMIVME-2128 are 96-pin DIN standard and were selected by GE Fanuc Embedded Systems because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to GE Fanuc Embedded Systems' Connector and I/O Cable Application Guide (GE Fanuc Embedded Systems Document No. 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning connector P2 user I/O pins and the use of the external voltage input are shown in Figure 2-9 on page 29 and Table 2-1 on page 29. Output connector pin configurations for P3 and P4 are shown in Figure 2-10 on page 30.

The VMIVME-2128 board is designed with a high-quality ground plane that is connected to VME ground through fuse F1 and to row B pins on connectors P3 and P4 to provide enhanced noise immunity and more reliable operation. Figure 2-12 on page 32 has Conductor No.1 shown at the bottom of the cable as it plugs into the header. Connector pin assignments for the 64 output channels are shown in Table 2-2 on page 30 and Table 2-3 on page 31.

CAUTION: It is important that the grounded conductors are connected to the power supply (GND return) associated with these signal loads. A ground connection should be implemented so as to prevent excessive currents (DC or noise) from flowing through the VME backplane. The externally applied USER voltage should not be applied to the VMIVME-2128 without the VME backplane +5VDC being on. If these voltages cannot be applied and removed together, then the preferred sequence is: **USER voltage ON last, OFF first.**

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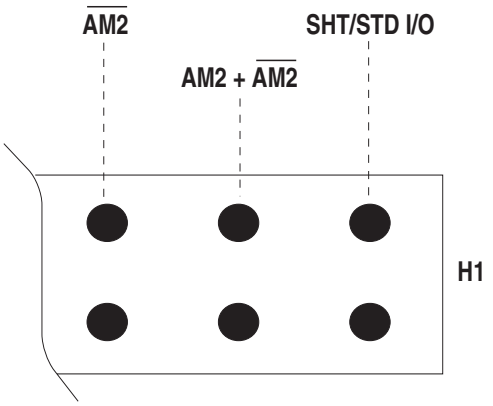


Figure 2-2 Jumper Configuration for Short Supervisory Access

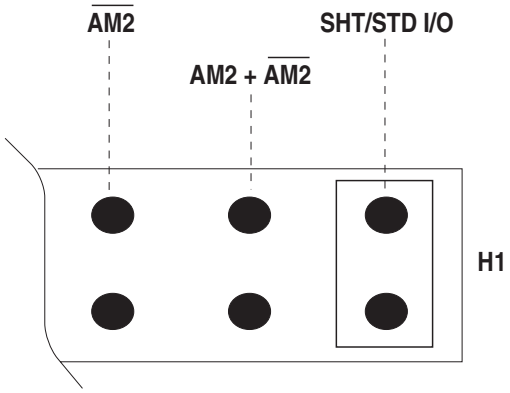


Figure 2-3 Jumper Configuration for Standard Supervisory Access

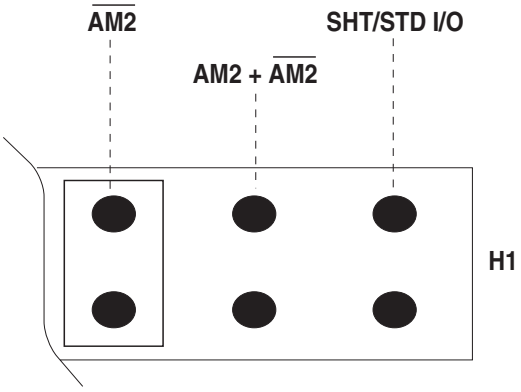


Figure 2-4 Jumper Configuration for Short Nonprivileged Access

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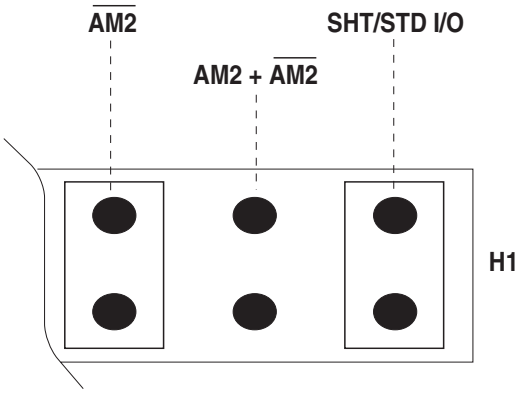


Figure 2-5 Jumper Configuration for Standard Nonprivileged Access

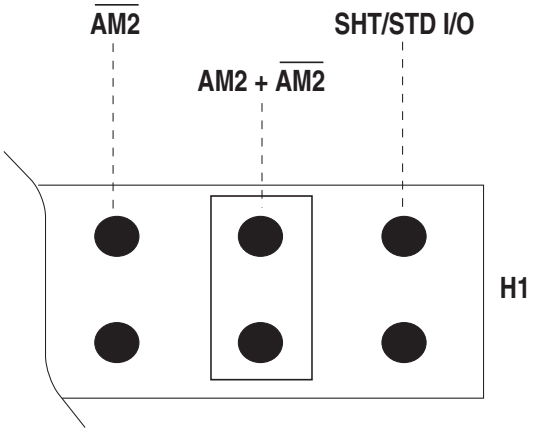


Figure 2-6 Jumper Configuration for Short Addressing and Supervisory or Nonprivileged Access

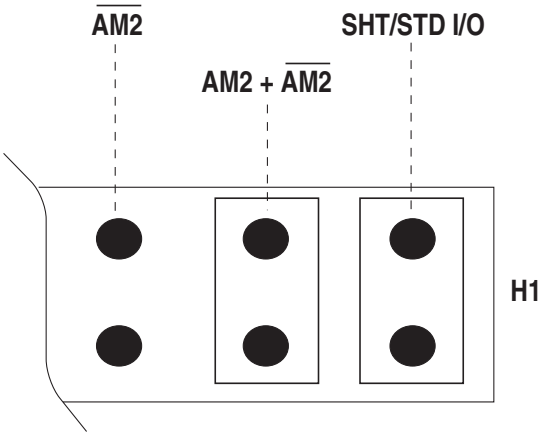
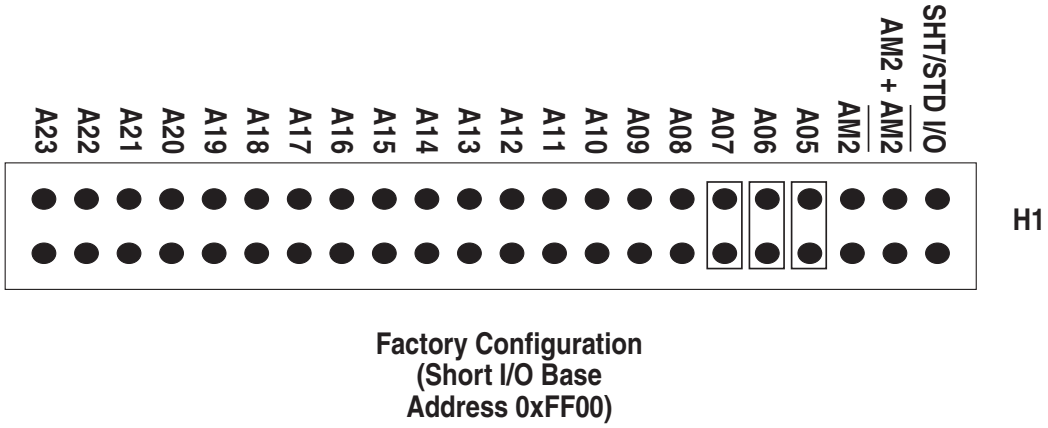
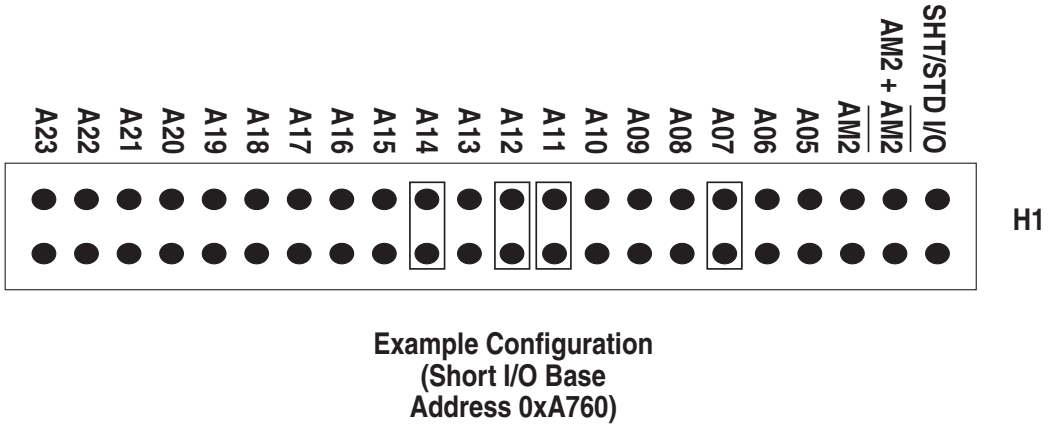


Figure 2-7 Jumper Configuration for Standard Addressing and Supervisory or Nonprivileged Access

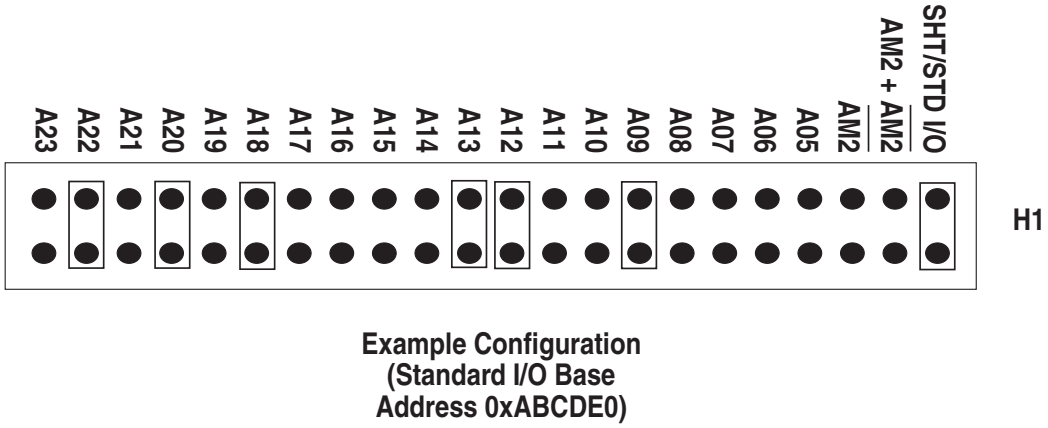
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Factory Configuration (Short I/O Base Address 0xFF00)



Example Configuration (Short I/O Base Address 0xA760)



Example Configuration (Standard I/O Base Address 0xABCDE0)

Figure 2-8 Base Address Select Jumpers

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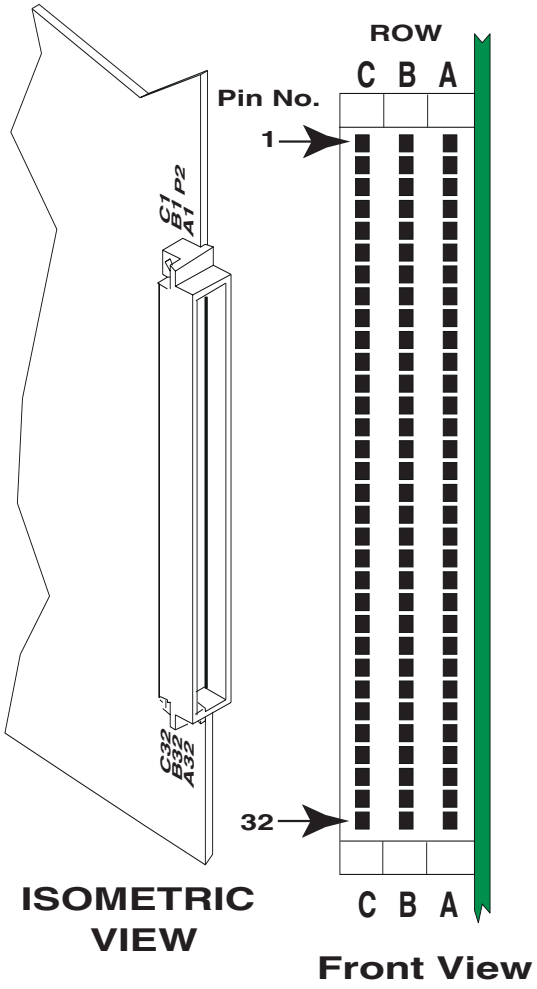


Figure 2-9 P2 Connector - Pin Layout

Table 2-1 P2 Connector Pin Assignments

Pin #	ROW C	ROW B	ROW A
1	VEXT P0	+5 V	OPT USR GND
2	VEXT P1	GND	OPT USR GND
3	VEXT P2	Reserved	OPT USR GND
4	VEXT P3	A24	OPT USR GND
5	VEXT P4	A25	OPT USR GND
6	VEXT P5	A26	OPT USR GND
7	VEXT P6	A27	OPT USR GND
8	VEXT P7	A28	OPT USR GND
9	VEXT P8	A29	OPT USR GND
10	VEXT P9	A30	OPT USR GND
11	VEXT P10	A31	OPT USR GND
12	VEXT P11	GND	OPT USR GND
13	VEXT P12	+5V	OPT USR GND
14	VEXT P13	D16	OPT USR GND
15	VEXT P14	D17	OPT USR GND
16	VEXT P15	D18	OPT USR GND
17	N/C	D19	OPT USR GND
18	N/C	D20	OPT USR GND
19	N/C	D21	OPT USR GND
20	N/C	D22	OPT USR GND
21	N/C	D23	OPT USR GND
22	N/C	GND	OPT USR GND
23	N/C	D24	OPT USR GND
24	N/C	D25	OPT USR GND
25	N/C	D26	OPT USR GND
26	N/C	D27	OPT USR GND
27	N/C	D28	N/C
28	N/C	D29	N/C
29	N/C	D30	N/C
30	N/C	D31	N/C
31	N/C	GND	N/C
32	N/C	+5 V	N/C

NOTE: External reference voltage is supplied by the user.

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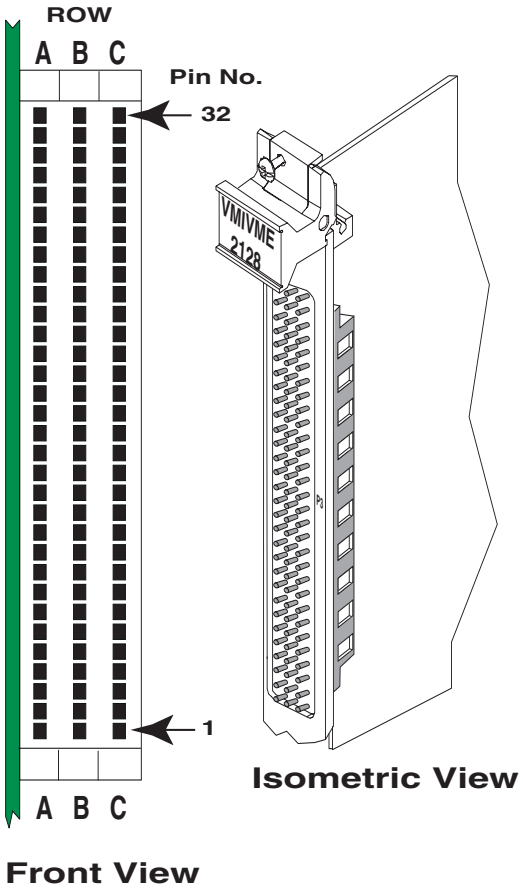


Figure 2-10 P3 Connector - Pin Layout

Table 2-2 P3 Pin - Channel Assignments

P3		P3	
Row A Pin#	**Channel No.**	**Row C Pin#**	**Channel No.**
32	95	32	127
31	94	31	126
30	93	30	125
29	92	29	124
28	91	28	123
27	90	27	122
26	89	26	121
25	88	25	120
24	87	24	119
23	86	23	118
22	85	22	117
21	84	21	116
20	83	20	115
19	82	19	114
18	81	18	113
17	80	17	112
16	79	16	111
15	78	15	110
14	77	14	109
13	76	13	108
12	75	12	107
11	74	11	106
10	73	10	105
09	72	09	104
08	71	08	103
07	70	07	102
06	69	06	101
05	68	05	100
04	67	04	99
03	66	03	98
02	65	02	97
01	64	01	96

NOTE: All pins in row B are user grounded.

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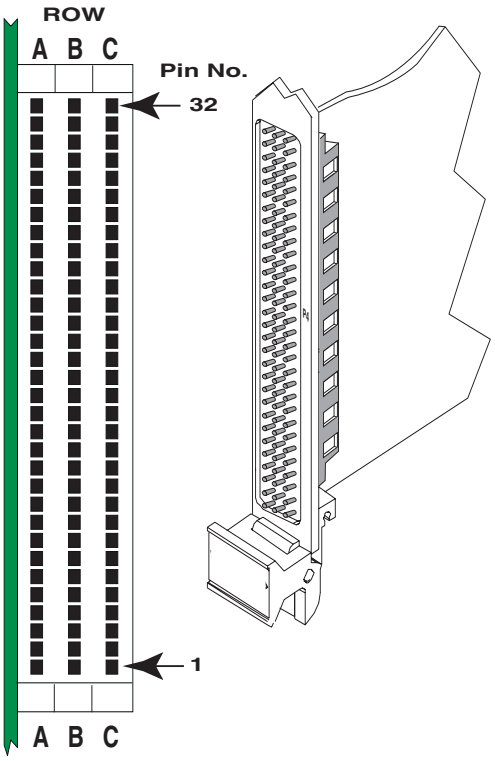


Figure 2-11 P4 Connector - Pin Layout

Table 2-3 P4 Pin - Channel Assignments

P4		P4	
Row A Pin#	**Channel No.**	**Row C Pin#**	**Channel No.**
32	31	32	63
31	30	31	62
30	29	30	61
29	28	29	60
28	27	28	59
27	26	27	58
26	25	26	57
25	24	25	56
24	23	24	55
23	22	23	54
22	21	22	53
21	20	21	52
20	19	20	51
19	18	19	50
18	17	18	49
17	16	17	48
16	15	16	47
15	14	15	46
14	13	14	45
13	12	13	44
12	11	12	43
11	10	11	42
10	09	10	41
09	08	09	40
08	07	08	39
07	06	07	38
06	05	06	37
05	04	05	36
04	03	04	35
03	02	03	34
02	01	02	33
01	00	01	32

NOTE: All pins in row B are user grounded.

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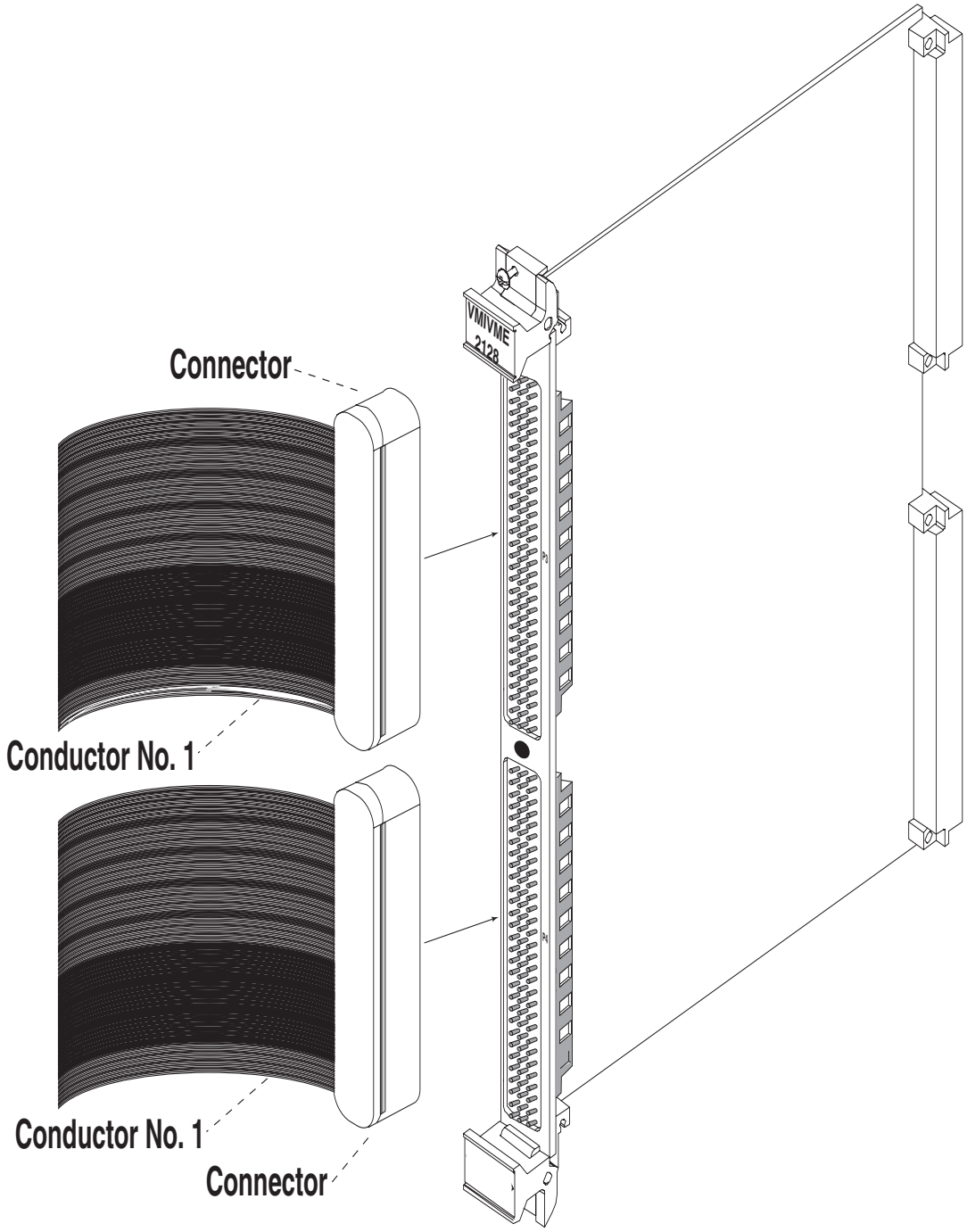


Figure 2-12 Cable Connector Configuration

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Optional USER Grounds

If the USER GROUND option is ordered, the output returns are routed to P2's A1 through A26 pins via the installation of shorting bars SB1 through SB4. This circuit permits the external supply's ground to be accessed from the P2 backplane of the VME chassis. An area of concern is keeping this ground path lower resistance than the VME ground path. If the VME ground is sensed lower, then the external supply current will flow through the VME and can damage it. When this option is ordered, use as many of the wires as possible to bring out these grounds. The currents in these wires can be high (for example: (128 channels x 300mA/channel)/26 wires = 1.48A/wire). Thus, 28 AWG or larger wire should be used with these pins. This will permit the large currents in the output circuits to be diverted from the VME backplane ground.

CAUTION: Care must be taken not to exceed the maximum current rating of the connector pins.

Warming Resistors

When an incandescent lamp is initially turned on, the cold lamp filament is at minimum resistance and would normally allow a 10 x to 12 x inrush current. Inrush current of 1A or more will force the output driver into foldback current limiting. To avoid this problem, a warming or current limiting resistor should be used in the lamp circuitry. The warming resistor should draw approximately 10 percent of the rated (warm) current of the bulb or bulbs.

Ten-pin SIP sockets are provided on the board for warming resistors. These resistors must be the bussed type with pin 1 being common. The sockets have pin 1 grounded. The location of the warming resistor sockets are RP2, RP4, RP6, RP8, RP10, RP12, RP14, RP16, RP18, RP20, RP22, RP24, RP26, RP28, RP30 and RP32. The wattage rating of these SIP resistors should be sufficient to handle the dissipation required.

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CHAPTER

3

Programming

Contents

Register Map 36
Detailed Programming 40

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Register Map

The VMIVME-2128 contains a 16-bit Board ID Register, a 16-bit CSR and eight 16-bit ODRs. Register address maps are shown in Table 3-1. The ODR allows control of 128 high voltage, digital output channels and are addressable as four 32-bit longwords, eight 16-bit words or as sixteen 8-bit bytes. The ODR can be read under program control for data validation or diagnostic testing. The CSR and Board ID are each addressable as a 16-bit word or as two 8-bit bytes. The ID and CSR bit maps are shown in Table 3-2 on page 37. The ODR bit map is shown in Table 3-3 on page 38. The board uses 32 bytes of address space.

Table 3-1 Data Register Address Map

Relative Address*	Mnemonic	Name/Function
XXX0 0000	IDU	Board ID Upper Byte
XXX0 0001	IDL	Board ID Lower Byte
XXX0 0010	CSRU	CSR Upper Byte
XXX0 0011	CSRL	CSR Lower Byte
XXX0 0100 Through XXX0 1111	Not Used**	
XXX1 0000	DR0U	Data Register 0 Upper Byte
XXX1 0001	DR0L	Data Register 0 Lower Byte
XXX1 0010	DR1U	Data Register 1 Upper Byte
XXX1 0011	DR1L	Data Register 1 Lower Byte
XXX1 0100	DR2U	Data Register 2 Upper Byte
XXX1 0101	DR2L	Data Register 2 Lower Byte
XXX1 0110	DR3U	Data Register 3 Upper Byte
XXX1 0111	DR3L	Data Register 3 Lower Byte
XXX1 1000	DR4U	Data Register 4 Upper Byte
XXX1 1001	DR4L	Data Register 4 Lower Byte
XXX1 1010	DR5U	Data Register 5 Upper Byte
XXX1 1011	DR5L	Data Register 5 Lower Byte
XXX1 1100	DR6U	Data Register 6 Upper Byte
XXX1 1101	DR6L	Data Register 6 Lower Byte
XXX1 1110	DR7U	Data Register 7 Upper Byte
XXX1 1111	DR7L	Data Register 7 Lower Byte

NOTE: * The relative address is defined by A4 through A0. All other address lines help to define the base address.

NOTE: **A read or write access to these addresses will not result in a bus error, however, any data written to these addresses will not be stored. Any data read from these addresses will not be meaningful.

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CSR and ID Register Map

Table 3-2 CSR and ID Register Bit Map

Board ID Upper Byte: XXX0 0000, Read-Only							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
0	0	0	1	0	1	0	0

Board ID Lower Byte: XXX0 0001, Read-Only							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
0	0	0	0	0	0	0	0

CSR Upper Byte: XXX0 0010, (Bit 12 through Bit 08 are Read-Only)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fail*	Test_ Mode_ P4_L*	Test_ Mode_ P3_L*	Fuse_ Blown**	0	0	0	0

CSR Lower Byte: XXX0 0011, Read-Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	0

NOTE: *Zero (0) = ON, One (1) = OFF

NOTE: **The Fuse Blown is an active high signal. Reading a one (1) in this location means the fuse has opened.

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Output Data Register

Table 3-3 Output Data Register Bit Map

Data Register 0 Upper Byte: XXX1 0000, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD127	OD126	OD125	OD124	OD123	OD122	OD121	OD120

Data Register 0 Lower Byte: XXX1 0001, Read/Write							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD119	OD118	OD117	OD116	OD115	OD114	OD113	OD112

Data Register 1 Upper Byte: XXX1 0010, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD111	OD110	OD109	OD108	OD107	OD106	OD105	OD104

Data Register 1 Lower Byte: XXX1 0011, Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD103	OD102	OD101	OD100	OD099	OD098	OD097	OD096

Data Register 2 Upper Byte: XXX1 0100, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD095	OD094	OD093	OD092	OD091	OD090	OD089	OD088

Data Register 2 Lower Byte: XXX1 0101, Read/Write							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD087	OD086	OD085	OD084	OD083	OD082	OD081	OD080

Data Register 3 Upper Byte: XXX1 0110, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD079	OD078	OD077	OD076	OD075	OD074	OD073	OD072

Data Register 3 Lower Byte: XXX1 0111, Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD071	OD070	OD069	OD068	OD067	OD066	OD065	OD064

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Table 3-3 Output Data Register Bit Map (Continued)

Data Register 4 Upper Byte: XXX1 1000, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD063	OD062	OD061	OD060	OD059	OD058	OD057	OD056

Data Register 4 Lower Byte: XXX1 1001, Read/Write							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD055	OD054	OD053	OD052	OD051	OD050	OD049	OD048

Data Register 5 Upper Byte: XXX1 1010, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD047	OD046	OD045	OD044	OD043	OD042	OD041	OD040

Data Register 5 Lower Byte: XXX1 1011, Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD039	OD038	OD037	OD036	OD035	OD034	OD033	OD032

Data Register 6 Upper Byte: XXX1 1100, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD031	OD030	OD029	OD028	OD027	OD026	OD025	OD024

Data Register 6 Lower Byte: XXX1 1101, Read/Write							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD023	OD022	OD021	OD020	OD019	OD018	OD017	OD016

Data Register 7 Upper Byte: XXX1 1110, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD015	OD014	OD013	OD012	OD011	OD010	OD009	OD008

Data Register 7 Lower Byte: XXX1 1111, Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD007	OD006	OD005	OD004	OD003	OD002	OD001	OD000

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Detailed Programming

Output Data Transfers

The Data Register Address Map (Table 3-1 on page 36) shows the correspondence between the ODRs (DR0 to DR7) and the output data channels 127 to 0.

Built-in-Test

The Built-in-Test features of the VMIVME-2128 provide the user with the capability of real-time loopback data verification and off-line diagnostic execution. The off-line Built-in-Test feature is initiated by setting the Test Mode (TM) bit in the CSR to a logic "zero". When the TM bit is set, all of the output drivers are tristated, and test data can be written to the selected data register and read back on a *read* transfer without affecting the user's equipment. Data can also be read back when the Test Mode is OFF. This permits on-line testing of the board.

The test mode bit and the Fail LED control bit are initialized ACTIVE at power-up or upon system reset. Thus, the Fail LED is ON and the output drivers are DISABLED. Simplified programming flowcharts are shown in Figure 3-1 on page 41 and Figure 3-2 on page 42.

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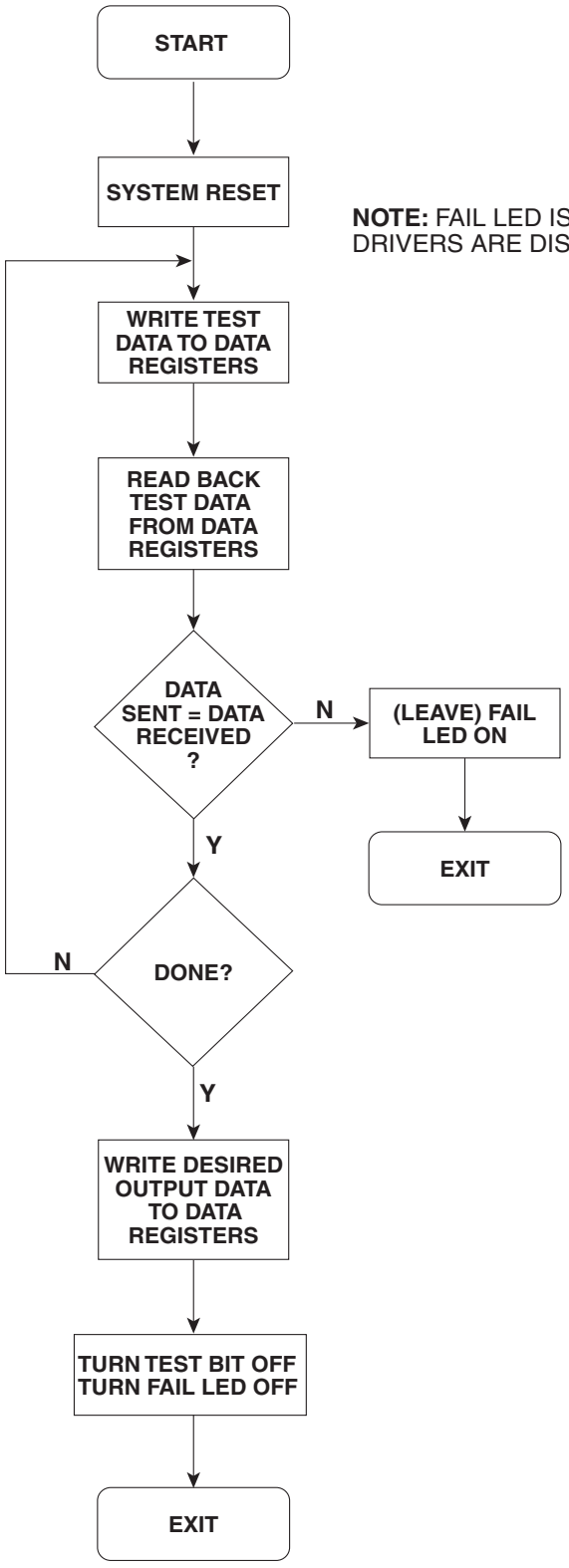
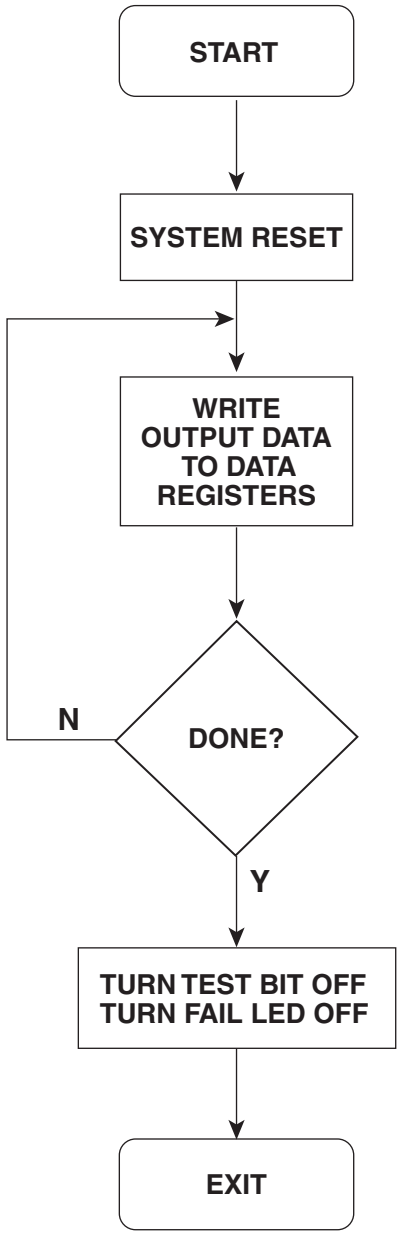


Figure 3-1 Programming Flowchart (Built-in-Test Active)

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NOTE: AT SYSTEM RESET, OUTPUT DRIVERS ARE DISCONNECTED AND THE FAIL LED IS ILLUMINATED.

Figure 3-2 Programming Flowchart (Built-in-Test Not Active)

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Maintenance

If a GE Fanuc Embedded Systems' product malfunctions, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE Fanuc Embbeded Systems for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**. RMAs are available at: rma@gefanuc.com

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GE Fanuc Embedded Systems Customer Care is available at: 1-800-GEFANUC (or 1-800-433-2682), or 1-780-401-7700. Or E-mail us at support.embeddedsystems@gefanuc.com

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Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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Additional Resources

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