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VMIVME-2511
Programmable I/O Board

Product Manual

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

500-022511-000 Rev. K

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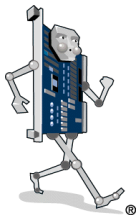
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(I/O man figure)



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VMIC Safety Summary

NOTE: The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product. VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

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Dangerous Procedure Warnings

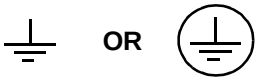
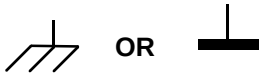
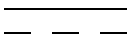
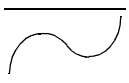
Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Safety Symbols

General definitions of safety symbols used in this manual:

Symbol	Description
	Product manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the product manual in order to protect against damage to the system.
	Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).
	Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.
	Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.
	Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.
	Alternating current (power line).
	Direct current (power line).
	Alternating or direct current (power line).

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Symbol	Description
WARNING:	**WARNING** denotes a hazard. It calls attention to an operating procedure, a practice, a condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.
CAUTION:	**CAUTION** denotes a hazard. It calls attention to an operating procedure, a practice, a condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.
NOTE:	**NOTE** denotes important information. It calls attention to an operating procedure, a practice, a condition or the like, which is essential to highlight.

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Introduction to the VMIVME-2511

The VMIVME-2511 is a VMEbus-compatible, programmable I/O board. It utilizes two Motorola MC68230 Parallel Interface/Timer I.C.s and one Motorola MC68153 Bus Interrupter Module. The board also has the following features:

- 48 bits of I/O, unidirectional 8-bit and 16-bit, or bidirectional 8-bit and 16-bit
- Interrupt generation logic allowing four interrupt sources (one timer interrupt and one port interrupt per MC68230)
- Optional high current drivers with 64 mA sink capability
- Two 24-bit programmable timers
- Software programmable timer modes
- Selectable handshake timer provides an interface flexible enough for connection to a wide variety of low, medium or high-speed peripherals or other computer systems

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Functional Description

The VMIVME-2511 Programmable I/O Board consists of VMEbus foundation logic, interrupt control logic and I/O control logic associated with the parallel interface/timer modules. The VMEbus foundation logic contains address decoding logic and data transfer control logic allowing the VMEbus to write and read 8-bit data transfers. The interrupt control logic utilizes the Motorola MC68153 BIM which allows port and timer interrupts from each parallel interface/timer. The interrupt requests to the CPU are issued by the MC68153 when requested to do so by a Parallel Interface/Timer (MC68230). The parallel I/O ports are programmable to allow unidirectional 8-bit or 16-bit ports and bidirectional 8-bit or 16-bit ports. A high current driver option is also available. When the high current option is employed, ports A and B are programmable as outputs only.

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General Description

The VMIVME-2511 is designed utilizing two Motorola MC68230 Parallel Interface / Timers (PI / Ts) and one MC68153 Bus Interrupter Module (BIM) to support all board functions as shown in Figure 1.

The VMIVME-2511 is capable of handling four interrupt requests. Each PI / T module is capable of two requests, a port interrupt request and a timer interrupt request. The four interrupt request signals (two from PI / T No. 1 and two from PI / T No. 2) are connected to the BIM, giving full interrupt support for both PI / T modules. Each PI / T module has two on-board interrupt vector registers programmable by the user. Table 1 on page 17 provides a summary of operational modes for the PI / T.

The MC68230 Parallel Interface / Timer provides a versatile, double-buffered, parallel interface, and an operating system oriented timer to VMEbus systems. The parallel interfaces operate in unidirectional or bi-directional modes, either 8 or 16 bits wide. In the unidirectional mode, an associated data direction register determines whether the port pins are inputs or outputs. In the bi-directional mode, the data direction registers are ignored, and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium or high-speed peripherals or the other computer systems. The PI / T ports allow use of vectored or auto vectored interrupts, and can generate periodic interrupts, a square wave or a single interrupt after a programmed time period. Also, the PI / T ports can be used for elapsed time measurement, or as a device watchdog. MC68230 I / O pins available to the user are shown in Figure 1.

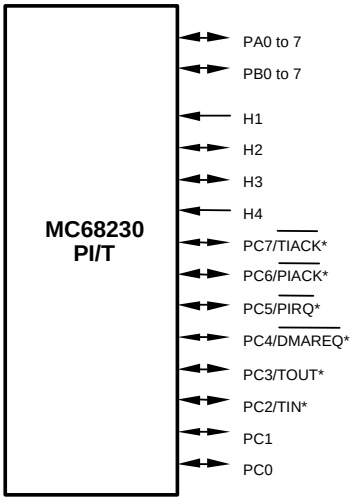


Figure 1 PI/T Pin Assignments

NOTE: (*) in the previous figure designates an individually programmable dual function pin.

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PA0 to PA7 and PB0 to PB7 (Port A and Port B)

Ports A and B are 8-bit ports that may be linked to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1 to H4. For stabilization during system power-up, Ports A and B have internal pull-up resistors to VCC. All port pins are active high.

H1 to H4 (Handshake Pins (I/O depending on the mode and submode))

Handshake pins H1 to H4 are multi-purpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers) or simple I/O pins. For stabilization during system power-up, H2 and H4 have internal pull-up resistors to VCC. Their sense (active high or low) may be programmed in the port general control register bits 3 to 0. The instantaneous level of the handshake pins can be read from the port status register independent of the mode.

Port C (PC0 to PC7/Alternate Function)

This port can be used as eight general-purpose I/O pins (PC0 to PC7), or any combination of six special function pins and two general-purpose I/O pins (PC0 to PC1). (Each dual function pin can be standard I/O or a special function independent of the other Port C pins.). The dual function pins are defined in the following paragraphs. When used as Port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the Port C data direction register.

The alternate functions (TIN, TOUT and TIACK) are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high, and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general purpose square-wave output, initially high. TIACK is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request (PIRQ) and interrupt acknowledge (PIACK) pins.

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Port Control Structure

The primary focus of most applications will be on Ports A and B, the handshake pins and the port interrupt pins. They are controlled using the port general control register, which contains a 2-bit field that specifies a set of four operation modes. These modes govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and the behavior of two of the handshake pins. This structure is summarized in Table 1 below and Table 2 on page 18.

Table 1 PI/T I/O Channel Definitions

Pin(s)	Description
(PA0 to PA7)	All eight bits, input or output depending on jumper configuration chosen
(PB0 to PB7)	All eight bits, input or output depending on jumper configuration chosen
(PC4 to PC7)	All four bits, input or output depending on jumper configuration chosen
H1	Input only
H2	Configured as input or output
H3	Input only
H4	Configured as input or output
PC0	Configured as input or output
PC1	Configured as input or output
PC2/TIN	Input only
PC3/TOUT	Output only

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Table 2 Port Mode Control Summary

Mode 0 (Unidirectional 8-bit Mode)			
Port A	Submode	00	Double-buffered input
		H1	Latches input data
		H2	Status / interrupt generating input, general-purpose output or operation with H1 in the interlocked or pulsed input handshake protocols
	Submode	01	Double-buffered output
		H1	Indicates data received by peripheral
		H2	Status / interrupt generating input, general-purpose output or operation with H1 in the interlocked or pulsed output handshake protocols
	Submode	1X	Bit I / O *
		H1	Status / interrupt generating input
		H2	Status / interrupt generating input or general purpose output
Port B		H3 and H4	Identical to Port A, H1 and H2

Mode 1 (Unidirectional 16-bit Mode)			
Port A Doubled-buffered data (Most significant)	Submode	XX	(Not used)
		H1	Status / interrupt generating input
		H2	Status / interrupt generating input or general-purpose output
Port B Double-buffered data (Least significant)		X0	Unidirectional 16-bit input
		H3	Indicated data received by peripheral
		H4	Status / interrupt generating input, general-purpose output or operation with H3 in the interlocked or pulsed output handshake protocol

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Table 2 Port Mode Control Summary (Continued)

Mode 2 (Bi-directional 8-bit Mode)			
Port A Bit I/O (With no handshaking pins)	Submode	XX	Not used
Port B Bi-directional 8-bit data (double- buffered)	Submode	XX	(Not used)
		H1	Indicates output data received by peripheral
		H2	Operation with H1 in the interlocked or pulsed output handshake protocols
		H3	Latches input data
		H4	Operation with H3 in interlocked or pulsed input handshake protocols

Mode 3 (Bi-directional 16-bit Mode)			
Port A Double-buffered data (Most significant)	Submode	XX	(Not used)
Port B Double-buffered data (Least significant)	Submode	XX	(Not used)
		H1	Indicates output data received by peripheral
		H2	Operation with H1 in the interlocked or pulsed output handshake protocols
		H3	Latches input data
		H4	Operation with H3 in the interlocked or pulsed input handshake protocols

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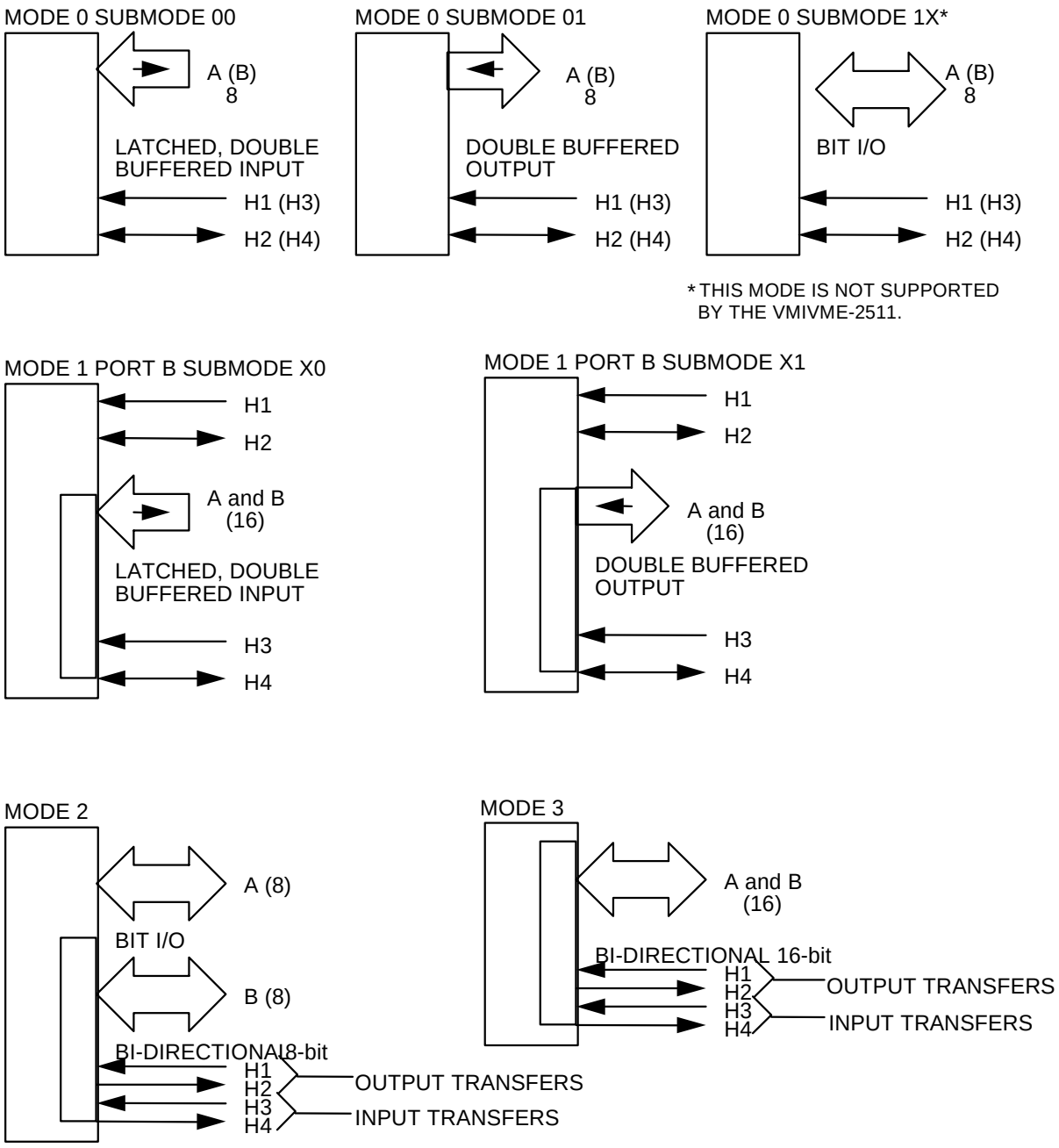


Figure 2 Port Mode Layout

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Reference Material List

Refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification and implementation of systems based on VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Low Level Analog I/O Configuration Guide	825-000000-001
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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Description and Specifications

The following are sources for description and specification information.

The 48-bit Digital Parallel Input / Output Board specification (Document number 800-022511-000) is available from:

VMIC
12090 South Memorial Parkway
Huntsville, AL 35803-3308
PH: 256-880-0444
1-800-240-7782
FX: 256-650-7245
Email: customer.service@vmic.com
Internet: www.vmic.com
PDF for the VMIVME-2511: www.analog.digital.vmic.com / pdf / 800-022511-000.pdf

The TS68230CP8 HCMOS Parallel Interface / Timer specification is available from:

STMicroelectronics
1000 East Bell Road
Phoenix, AZ 85022
PH: 602-485-6100
FX: 602-485-6102
Internet: www.us.st.com
PDF for the TS68230CP8: www.us.st.com / stonline / books / pdf / docs / 2353.pdf

The Epic Ei68C153 Bus Interrupter Module (VME) specification is available from:

Epic Semiconductor, Inc.
4801 S. Lakeshore Dr.
Suite 203
Tempe, AZ 85282
PH: 480-730-1000
FX: 480-838-4740
Internet: www.epicsemi.com
PDF for the Ei68C153: www.epicsemi.com / 153.pdf

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Motorola MC68153 BIM and MC68230 PI/T

The VMIVME-2511 was originally manufactured using the Motorola MC68153 BIM and MC68230 PI/T, both of which are now out of production. The Epic Ei68C153 BIM and STMicroelectronics TS68230CP8 PI/T are being used as replacements on all newly-manufactured VMIVME-2511 boards. Any references to the Ei68C153 and TS68230CP8 in this document are also applicable to the MC68153 and MC68230.

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CHAPTER

1

Theory of Operation

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Introduction

The VMIVME-2511 consists of eight major subsystems as illustrated in Figure 1-1 on page 26. Each subsystem is further broken down into more detailed block diagrams as shown in Figure 1-2 on page 27 through Figure 1-4 on page 29.

Figure 1-2 shows the address decoding scheme and the address modifier jumper (J1), which is used to select the short I/O space to be used. A block diagram of the connections for the PI/T is shown in Figure 1-3 on page 28, while Figure 1-4 shows the basic configuration of the BIM.

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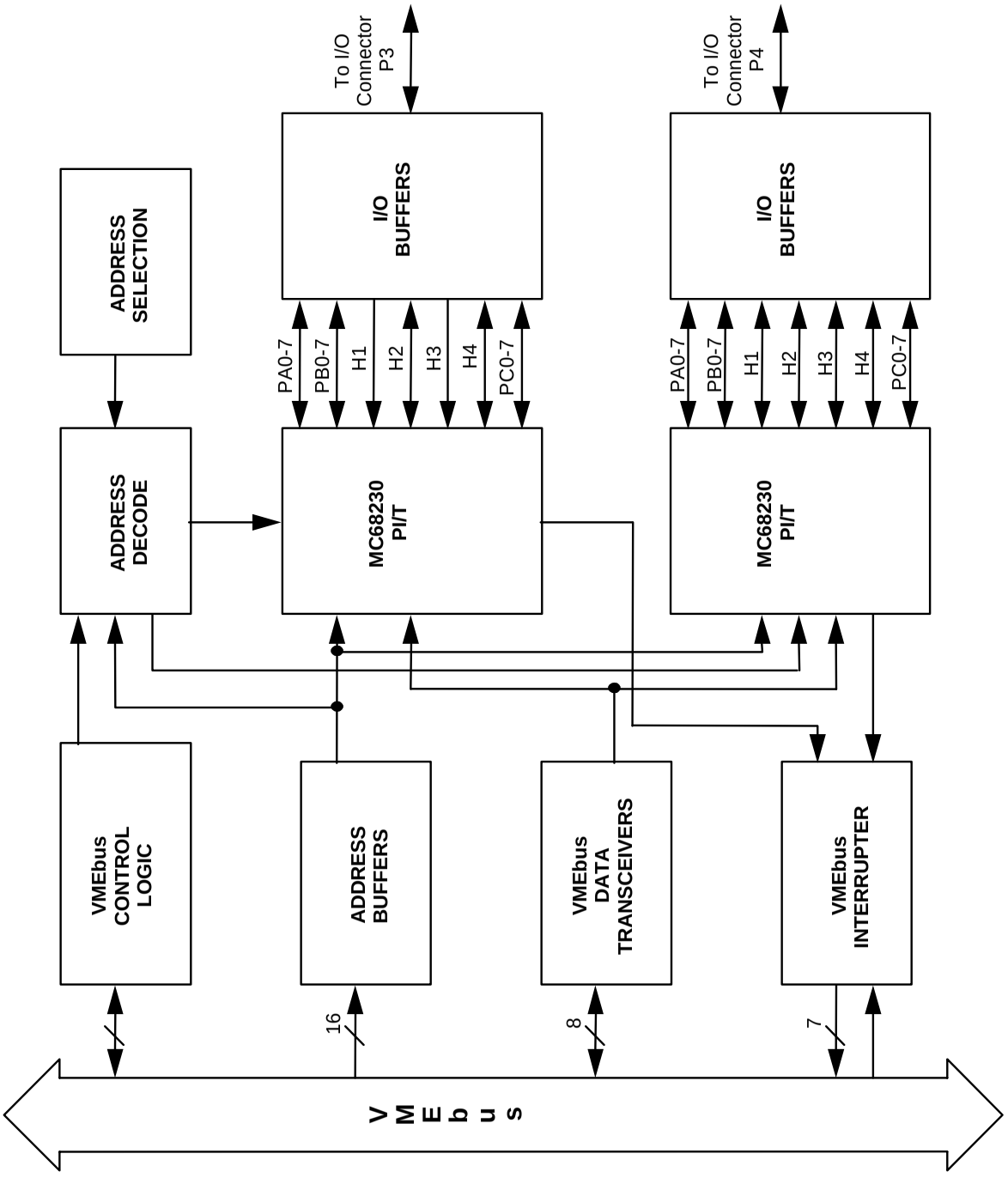


Figure 1-1 Functional Block Diagram

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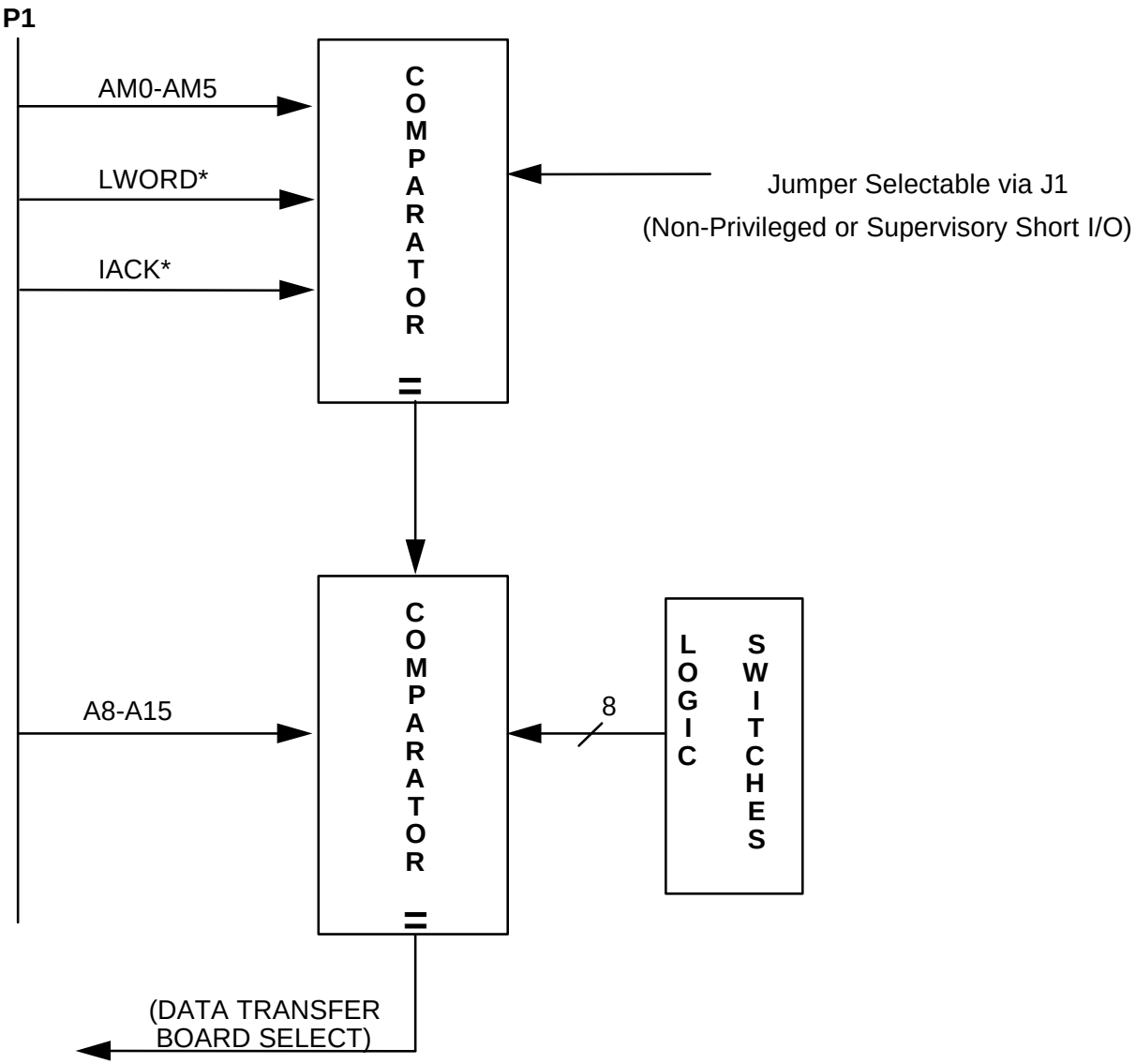


Figure 1-2 VMIVME-2511 Address Decode Subsystem Block Diagram

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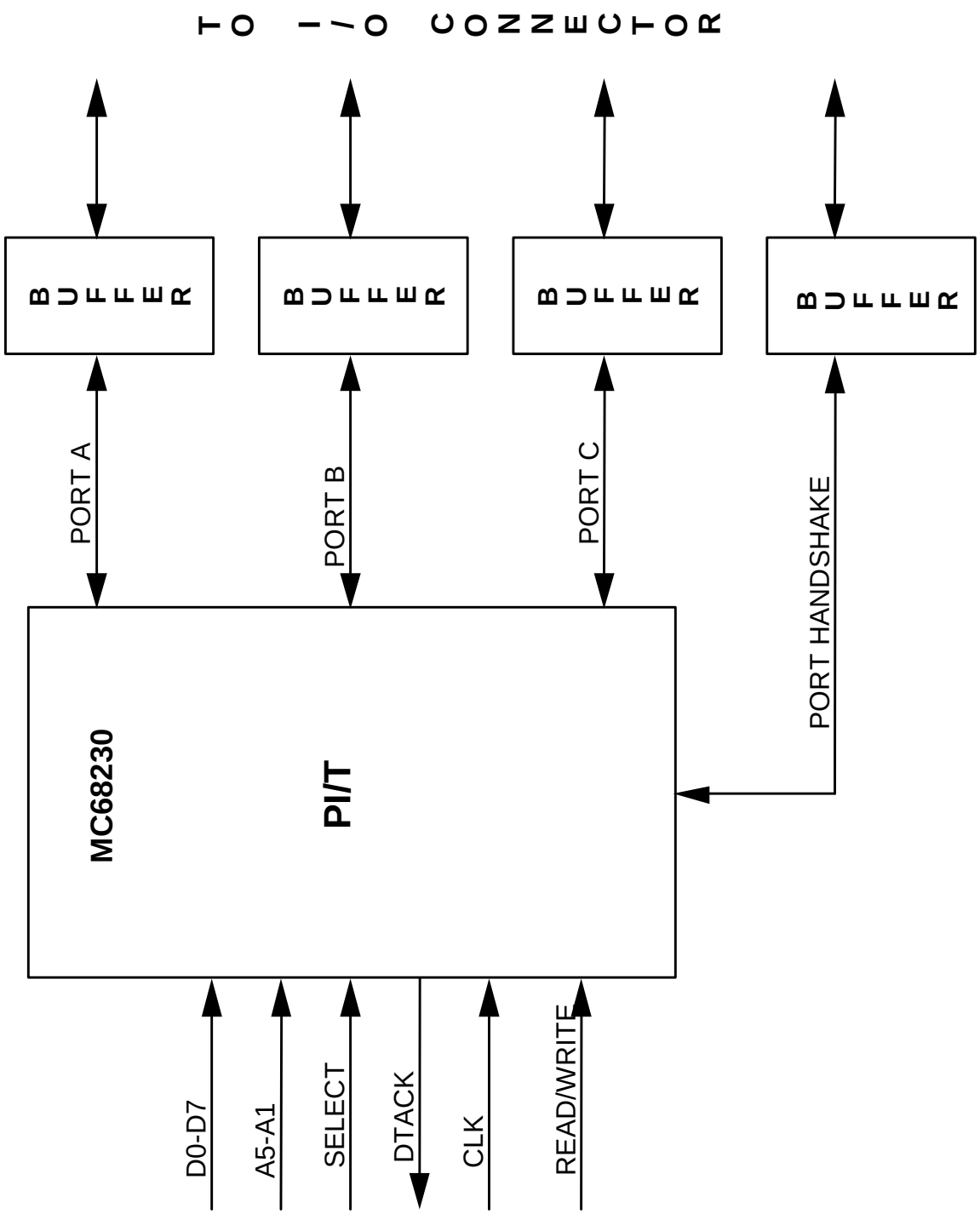


Figure 1-3 Block Diagram of Parallel Interface/Timer and I/O Port Control Logic

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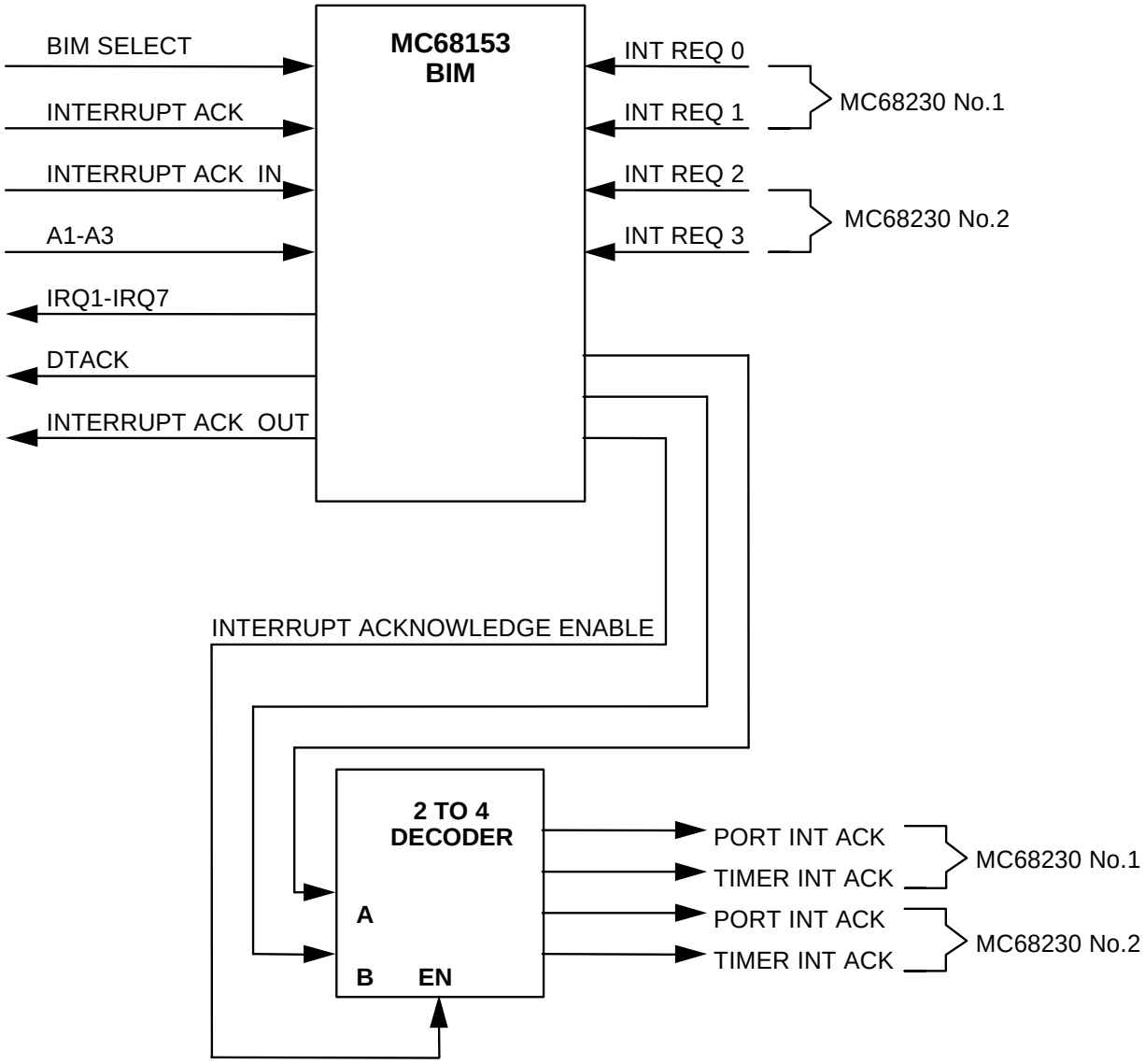


Figure 1-4 VMIVME-2511 VMEbus Interrupter System

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Operational Overview

As noted in the functional block diagram in Figure 1-1 on page 26, the VMIVME-2511 utilizes two MC68230 modules. Each MC68230 Parallel Interface/Timer module (PI/T) has three I/O ports and some additional handshake interface. The handshake signals and the I/O ports of each module are in turn mapped into a single I/O connector. The module that is associated with the P3 connector will be referred to in the discussion which follows as PI/T No. 1. The module associated with the P4 connector will be referred to as PI/T No. 2. Although the discussions may be about PI/T No. 1, they are equally applicable to PI/T No. 2.

To perform I/O data transfers with the VMIVME-2511, prepare the appropriate PI/T for the type of transfer to be made and then process the data. The PI/T to be used will depend upon the input channel of interest. The type of transfer will have to be programmed in the control registers of the PI/T. See "Description and Specifications" on page 22, and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining a specification containing a detailed description of the set-up and use of the MC68230.

To achieve interrupt processing with the VMIVME-2511, the chosen PI/T module is programmed for port or timer interrupts. Then, if the proper channel of the MC68153 Bus Interrupter Module (BIM) is enabled, the particular interrupt source of interest will be acknowledged by the system processor. Some jumper selection is required, because the port channels of the PI/T modules can serve as I/O channels, interrupt requests or acknowledge signals.

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I/O Data Transfer Description

The VMIVME-2511 performs I/O transfers via connectors P3 and P4, which are accessible from the front panel of the board. The I/O transfers are done through the port registers in the desired PI/T module. While reading this section, please refer to logic diagram 141-022511-000 and the MC68230 specification. The VMIVME-2511 supports all of the data I/O modes in the PI/T modules, while providing a data buffer to the external host equipment if the high current option is not ordered.

To perform bi-directional operations, the two general purpose I/O pins of Port C (PC0 and PC1) are used. They must be programmed for output only operations. They are used to control the direction of the Ports A and B data buffers. PC0 controls Port A and PC1 controls Port B. To perform a data transfer set the level of the appropriate Port C line and then process the data. A low level on one of these Port C lines will place the associated data buffer in the output mode. A high level on the Port C line will put the data buffer in the input mode.

These operations require jumpering. Please refer to Figure 3-3 on page 61 and Figure 3-4 on page 62, as well as Table 3-1 on page 63, while reading this paragraph. The jumpers involved are J22, J23, J26, J27, J30, J31 and J34 through J43. If the Port C lines of PI/T No. 1 are to control its data buffers, then jumpers J40 and J41 are installed while J22, J23, J30, J31, J36 and J37 are NOT installed. These last jumpers are used when the Port C lines are used as general purpose I/O lines. The remaining jumpers are used with PI/T No. 2. Thus, PI/T No. 1 can be configured differently from PI/T No. 2.

For uni-directional operations, the buffers can be preset for input or output by installing or not installing jumpers J36 through J39. If these jumpers are installed, the associated port pins are outputs only. If these jumpers AND jumpers J40 through J43 are NOT installed, the associated port pins are inputs only. In either of these modes, the Port C pins "zero" and "one" are available for the types of tasks stated in the MC68230 specification.

Regardless of the type of operation stated above, the rest of the Port C pins can be used as stated in the MC68230's specification. However, these lines have jumper options that must be observed. These options are defined in Chapter 3, "Configuration and Installation".

NOTE: See "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining the MC68230 specification.

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Interrupt Capability

The VMIVME-2511 is capable of handling four interrupt requests. Each PI/T module is capable of two requests (a port interrupt request and a timer interrupt request). The four interrupt request signals (two from PI/T No. 1 and two from PI/T No. 2) are connected to the MC68153 BIM, giving full interrupt support for both PI/T modules. Each PI/T module has two on-board interrupt vector registers programmable by the user. Programming information concerning the BIM and PI/T modules will be found in the programming section that follows, and in the MC68153 specification.

NOTE: See "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining the MC68153 specification.

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The MC68230 Parallel Interface/Timer

The MC68230 PI/T provides a versatile parallel I/O interface to a wide variety of peripheral and computer systems. Each 8-bit port is double buffered and each port (Ports A and B) has two handshake lines to provide for orderly transfer of data to and from the MC68230. See the MC68230 specification for the port control structure, handshaking definition and I/O interface timing diagrams. Port C of each MC68230 may be used as six general purpose I/O lines (C0, C1, C4-C7) with C2 and C3 used as the timer clock input and timer clock output, respectively. Alternatively, Port C (C4-C7) may be programmed to support the MC68230's interrupt structure. C2 and C3 remain the timer input/output pins, and C0 and C1 stay as general purpose I/O pins.

The MC68230 may indicate a need for service in one of two ways. The processor may poll the Port Status Register (PSR) to check the state of the handshake pins or the MC68230 may be programmed for interrupts. These interrupts may occur on the assertion of any of the handshake pins, H1 and H2 for port A or H3 and H4 for Port B or at the end of a timer count. This is further explained in the MC68230 specification.

NOTE: See "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining the MC68230 specification.

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CHAPTER 2

Programming

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Detailed Programming. 47

Introduction

The operation of the Parallel Interface/Timer (PI/T) module can be limited due to the buffers being used to drive port data to the P3 and P4 connectors. This limitation restricts the use of some port pins in some port modes, such as bi-directional data transfer. Before reading the next section the reader should have an understanding of the Programmers Model section of the MC68230 data specifications. Read "Theory of Operation" on page 25 and"Physical Installation" on page 55 so that the programming will be consistent with the jumper configuration of the I/O ports. For programming concerning interrupts, the reader should have an understanding of the BIM, which is described in the BIM and PI/T specifications (see "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for more information), to supplement the description which follows.

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BIM and PI/T Register Map

The Bus Interface Module, (BIM) MC68153 contains eight 8-bit registers, while each of the PI/T modules contain 32 eight-bit registers of which only 23 are used. All of the registers are addressed on odd-byte locations only. Of the 15 address bits A1-A15, only eight (A15-A8) are decoded for board select with the BIM mapped first RI/T1 second and PI/T2 last. The BIM register map is shown in Table 2-2 on page 37. The PI/T No. 1 register map is shown in Table 2-3 on page 38. The PI/T No. 2 register map is shown in Table 2-4 on page 42. The bit definitions of each register in the MC68153 BIM and the MC68230 PI/T will be found in the specifications for these parts. See "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for more information.

Table 2-1 PI/T No. 1 (P3 Connector Byte Address Locations)

Binary Address		
A15 A8	A7 A0	
X X X X X X X X	0 1 0 0 0 0 0 1	Port General Control Register
Base Switch	Individual Register	
Switch Selectable	Addresses	
X X X X X X X X	0 1 1 1 1 1 1 1	Timer Status Register
Hex Address		
$XX41 through $XX47 for PI/T No. 1		

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Table 2-2 BIM Register Map

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
Y . . . . Y	0	0	X	X	0	0	0	1	**Control Register 0**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									F	FAC	X / $\overline{IN}$	IRE	IRAC	L2	L1	L0
Y . . . . Y	0	0	X	X	0	0	1	1	**Control Register 1**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									F	FAC	X / $\overline{IN}$	IRE	IRAC	L2	L1	L0
Y . . . . Y	0	0	X	X	0	1	0	1	**Control Register 2**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									F	FAC	X / $\overline{IN}$	IRE	IRAC	L2	L1	L0
Y . . . . Y	0	0	X	X	0	1	1	1	**Control Register 3**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									F	FAC	X / $\overline{IN}$	IRE	IRAC	L2	L1	L0
Y . . . . Y	0	0	X	X	1	0	0	1	**Vector Register 0**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									V7	V6	V5	V4	V3	V2	V1	V0
Y . . . . Y	0	0	X	X	1	0	1	1	**Vector Register 1**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									V7	V6	V5	V4	V3	V2	V1	V0
Y . . . . Y	0	0	X	X	1	1	0	1	**Vector Register 2**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									V7	V6	V5	V4	V3	V2	V1	V0
Y . . . . Y	0	0	X	X	1	1	1	1	**Vector Register 3**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									V7	V6	V5	V4	V3	V2	V1	V0

Y - Represents user switch selectable positions. See DIP switch selection for address selection.

F - Flag Bit

FAC - Flag Auto Clear

X / $\overline{IN}$ - External / $\overline{Internal}$ (Vector Source)

IRE - Interrupt Enable

IRAC - Interrupt Auto-Clear

L2, L1 and L0 - Interrupt Level

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Table 2-3 PI/T No.1 Register Map

Binary Address																	
A15 - A8	A7	A6	A5	A4	A3	A2	A1	A0									
X X	0	1	0	0	0	0	0	1	**Port General Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	
X X	0	1	0	0	0	0	1	1	**Port Service Request Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control			
X X	0	1	0	0	0	1	0	1	**Port A Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	0	1	0	0	0	1	1	1	**Port B Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	0	1	0	0	1	0	0	1	**Port C Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	0	1	0	0	1	0	1	1	**Port Interrupt Vector Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Interrupt Vector Number						*	*	
X X	0	1	0	0	1	1	0	1	**Port A Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port A Submode		H2 Control			H2 INT. Enable	H1 SVCRQ	H1 STCTL	
X X	0	1	0	0	1	1	1	1	**Port B Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port B Submode		H4 Control			H4 INT. Enable	H3 SVCRQ	H3 STCTL	

*Unused, read zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selection.

NOTE: See MC68230 Specifications for port control register information.

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Table 2-3 PI/T No.1 Register Map (Continued)

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
X X	0	1	0	1	0	0	0	1	**Port A Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	0	1	0	0	1	1	**Port B Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	0	1	0	1	0	1	**Port A Alternate Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	0	1	0	1	1	1	**Port B Alternate Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	0	1	1	0	0	1	**Port C Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	0	1	1	0	1	1	**Port Status Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S
X X	0	1	0	1	1	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	0	0	1	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**

XX - Represents user selectable positions. See DIP switch selection for address selection.

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Table 2-3 PI/T No.1 Register Map (Continued)

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
X X	0	1	1	0	0	0	0	1	**Timer Control Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									TOUT/TIACK Control			ZD CTRL	*	Clock Control		Timer Enable
X X	0	1	1	0	0	0	1	1	**Timer Interrupt Vector Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	0	1	1	0	0	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	0	0	1	1	1	**Counter Preload Register (HI)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
X X	0	1	1	0	1	0	0	1	**Counter Preload Register (MID)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
X X	0	1	1	0	1	0	1	1	**Counter Preload Register (LOW)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 0
X X	0	1	1	0	1	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	0	1	1	1	1	**Counter Register (High)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16

*Unused, read as zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selections.

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Table 2-3 PI/T No.1 Register Map (Concluded)

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
X X	0	1	1	1	0	0	0	1	**Counter Register (MID)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
X X	0	1	1	1	0	0	1	1	**Counter Register (Low)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 0
X X	0	1	1	1	0	1	0	1	**Timer Status Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									*	*	*	*	*	*	*	ZDS
X X	0	1	1	1	0	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	1	1	0	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	1	1	0	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	1	1	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	0	1	1	1	1	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**

*Unused, read as zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selections.

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Table 2-4 PI/T No.2 Register Map

Binary Address																	
A15 - A8	A7	A6	A5	A4	A3	A2	A1	A0									
X X	1	0	0	0	0	0	0	1	**Port General Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	
X X	1	0	0	0	0	0	1	1	**Port Service Request Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control			
X X	1	0	0	0	0	1	0	1	**Port A Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	1	0	0	0	0	1	1	1	**Port B Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	1	0	0	0	1	0	0	1	**Port C Data Direction Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	1	0	0	0	1	0	1	1	**Port Interrupt Vector Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Interrupt Vector Number						*	*	
X X	1	0	0	0	1	1	0	1	**Port A Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port A Submode		H2 Control			H2 INT. Enable	H1 SVCRQ	H1 STCTL	
X X	1	0	0	0	1	1	1	1	**Port B Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Port B Submode		H4 Control			H4 INT. Enable	H3 SVCRQ	H3 STCTL	

*Unused, read zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selection.

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Table 2-4 PI/T No.2 Register Map (Continued)

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
X X	1	0	0	1	0	0	0	1	**Port A Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	1	0	0	1	0	0	1	1	**Port B Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	1	0	0	1	0	1	0	1	**Port A Alternate Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	1	0	0	1	0	1	1	1	**Port B Alternate Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	1	0	0	1	1	0	0	1	**Port C Data Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X X	1	0	0	1	1	0	1	1	**Port Status Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S
X X	1	0	0	1	1	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	1	0	0	0	1	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**

XX - Represents user selectable positions. See DIP switch selection for address selection.

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Table 2-4 PI/T No.2 Register Map (Continued)

Binary Address																	
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**									
X X	1	0	1	0	0	0	0	1	**Timer Control Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									TOUT/TIACK Control			ZD CTRL	*	Clock Control		Timer Enable	
X X	1	0	1	0	0	0	1	1	**Timer Interrupt Vector Register**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X X	1	0	1	0	0	1	0	1	**Not Used**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
X X	1	0	1	0	0	1	1	1	**Counter Preload Register (HI)**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
X X	1	0	1	0	1	0	0	1	**Counter Preload Register (MID)**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08	
X X	1	0	1	0	1	0	1	1	**Counter Preload Register (LOW)**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 0	
X X	1	0	1	0	1	1	0	1	**Not Used**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
X X	1	0	1	0	1	1	1	1	**Counter Register (High)**								
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**	
									Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	

*Unused, read as zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selections.

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Table 2-4 PI/T No.2 Register Map (Concluded)

Binary Address																
A15 - A8	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**								
X X	1	0	1	1	0	0	0	1	**Counter Register (MID)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
X X	1	0	1	1	0	0	1	1	**Counter Register (Low)**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 0
X X	1	0	1	1	0	1	0	1	**Timer Status Register**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
									*	*	*	*	*	*	*	ZDS
X X	1	0	1	1	0	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	1	0	1	1	1	0	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	1	0	1	1	1	0	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	1	0	1	1	1	1	0	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**
X X	1	0	1	1	1	1	1	1	**Not Used**							
									IDB 07	**IDB 06**	**IDB 05**	**IDB 04**	**IDB 03**	**IDB 02**	**IDB 01**	**IDB 00**

*Unused, read as zero (0).

XX - Represents user selectable positions. See DIP switch selection for address selections.

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Table 2-5 PI/T No. 1 (P3 Connector Byte Address Locations)

Binary Address		
A15 A8	A7 A0	
X X X X X X X X	1 0 0 0 0 0 0 1	Port General Control Register
Base Switch	Individual Register	
Switch Selectable	Addresses	
X X X X X X X X	1 0 1 1 1 1 1 1	Timer Status Register
Hex Address		
$XX81 through $XXBF for PI/T No. 2		
Total Address Space of VMIVME-2511		
Hex address $XX01 through $XXBF		

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Detailed Programming

Programming the MC68153 BIM

The vector registers on-board the BIM are not used since the PI/T modules supply their own interrupt vector. These vectors are supplied by the Port Interrupt Vector Register (PIVR) and/or by the Timer Interrupt Vector Register (TIVR) on board the PI/T module, depending on which interrupt source is being acknowledged. Therefore, the BIM must be programmed for external vectors. In addition, the interrupt auto-clear bit corresponding to each interrupt source must be set (a high level), along with its associated interrupt enable bit. This will require the interrupt service routine to set the interrupt enable bit each time an interrupt is processed.

The control registers on-board the BIM associated with the PI/T interrupt channels are shown in Table 2-6 below. All control registers in the BIM are initialized to zero (0) upon a system reset.

Table 2-6 BIM Control Registers and Interrupt Source

Interrupt Channel	Control Register	Interrupt Source
0	0	PI/T No. 1 Port Interrupts
1	1	PI/T No. 1 Timer Interrupts
2	2	PI/T No. 2 Port Interrupts
3	3	PI/T No. 2 Timer Interrupts

NOTE: PI/T No. 1 = P3 connector and PI/T No. 2 = P4 connector.

Programming the MC68230 PI/T

The port section of the MC68230 PI/T consists of three 8-bit ports and four associated handshake signals. The PI/T module permits each bit in each port along with two of the handshake lines to be either input or output. However, certain restrictions must be observed when certain options are ordered.

The high current option (which is applicable to only Ports A and B) of the VMIVME-2511 permits only output operations for Ports A and B while Port C is unrestricted in its operations. The bi-directional operations of the 2511 use standard current devices and bits 0 and 1 of Port C may be used as outputs only to control the direction of the Port A and B buffers as explained in "I/O Data Transfer Description" on page 31.

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The programming of the PI/Ts in the VMIVME-2511 must be consistent with the jumper configuration of the board and the options ordered. Refer to Figure 3-3 on page 61 and Figure 3-4 on page 62 for a jumper diagram, and refer to Figure 3-1 on page 63 for the jumper definitions. The PI/T I/O channel definitions are shown in Table 2-7.

Table 2-7 PI/T I/O Channel Definitions

PI/T I/O Channel Definition	
PA0-PA7	All eight bits are output, if the high current option is chosen
PB0-PB7	All eight bits are output, if the high current option is chosen
PC4-PC7	All four bits input or output, depending on jumper configuration chosen
H1	Input only
H2	Configured as input or output
H3	Input only
H4	Configured as input or output
PC0	Configured as input or output, can be used to control the direction of Port A
PC1	Configured as input or output, can be used to control the direction of Port B
PC2/TIN	Input only
PC3/TOUT	Output only

Timer Programming

All timer modes available on the PI/T module can be utilized with the VMIVME-2511. Port C pins PC2/TIN and PC3/TOUT are specifically buffered for use as timer input and timer output pins respectively. Refer to the MC68230 specification for more information. See "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining the MC68230 specification.

Interrupt Programming

All interrupt programming modes available on the PI/T module can be utilized with the VMIVME-2511, provided that those port pins associated with interrupts are configured as such (see "Physical Installation" on page 55). Interrupts from the two PI/T modules on-board the VMIVME-2511 are generated by the MC68153 BIM. The programming of the BIM and PI/T modules concerning interrupts should follow the

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flowchart shown in Figure 2-1 on page 49. The port interrupt service routine should follow the sequence in Figure 2-2 on page 50. To program the timers for interrupts, see the flowchart in Figure 2-3 on page 51. Refer to "Description and Specifications" on page 22 and "Motorola MC68153 BIM and MC68230 PI/T" on page 23 for information on obtaining the specifications.

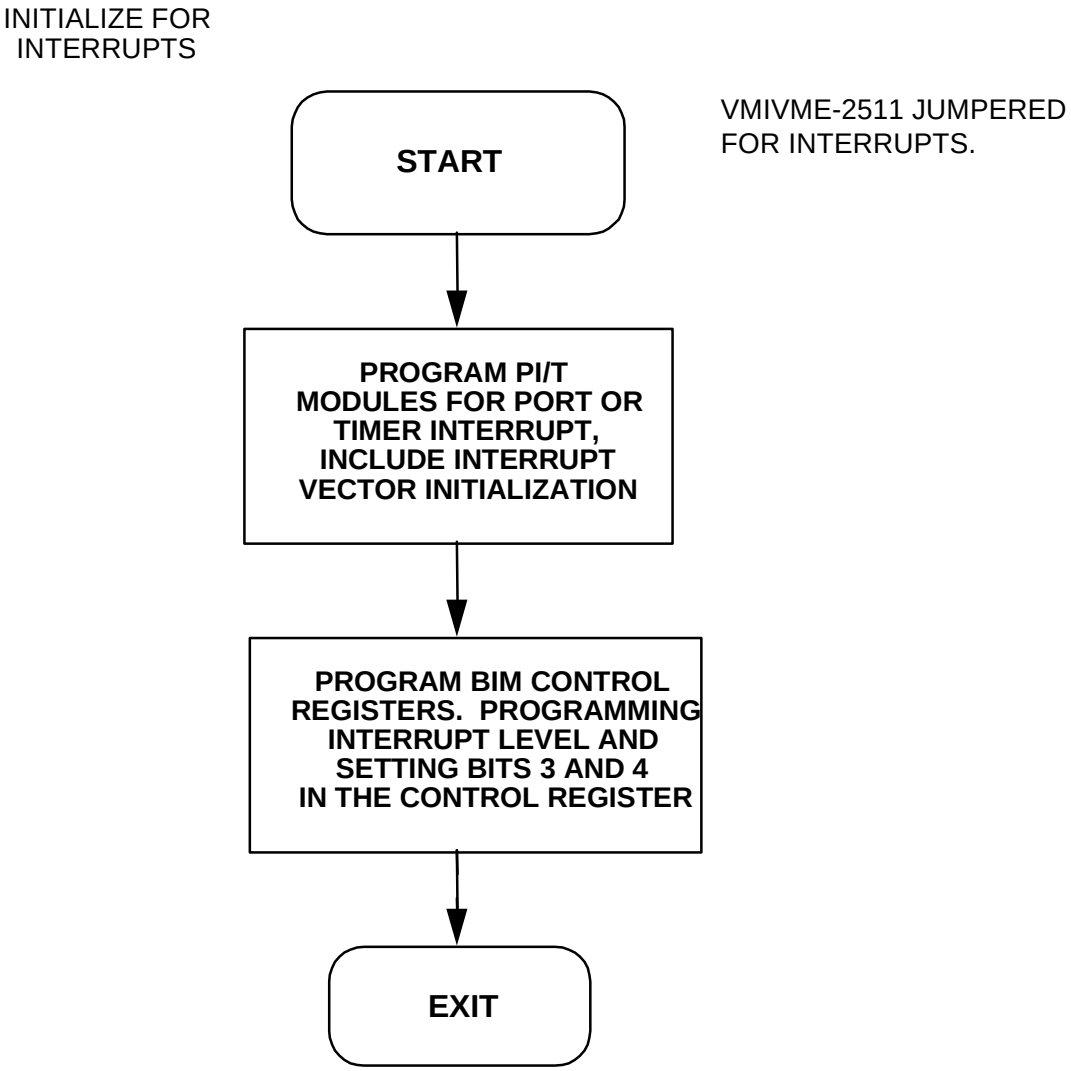


Figure 2-1 Interrupt Programming Sequence

NOTE: For interrupts in Figure 2-1, see "Physical Installation" on page 55.

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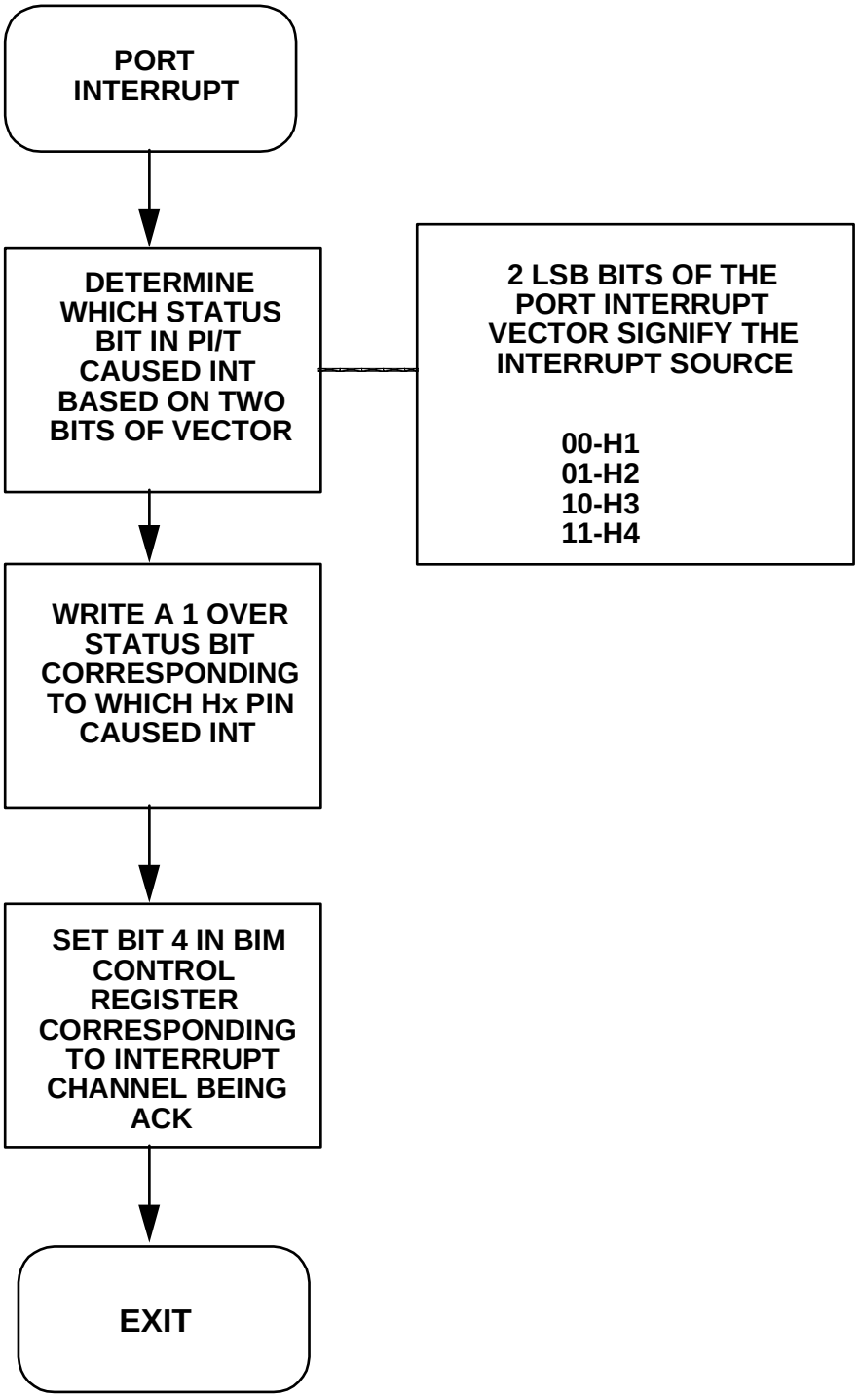


Figure 2-2 Port Interrupt Routine

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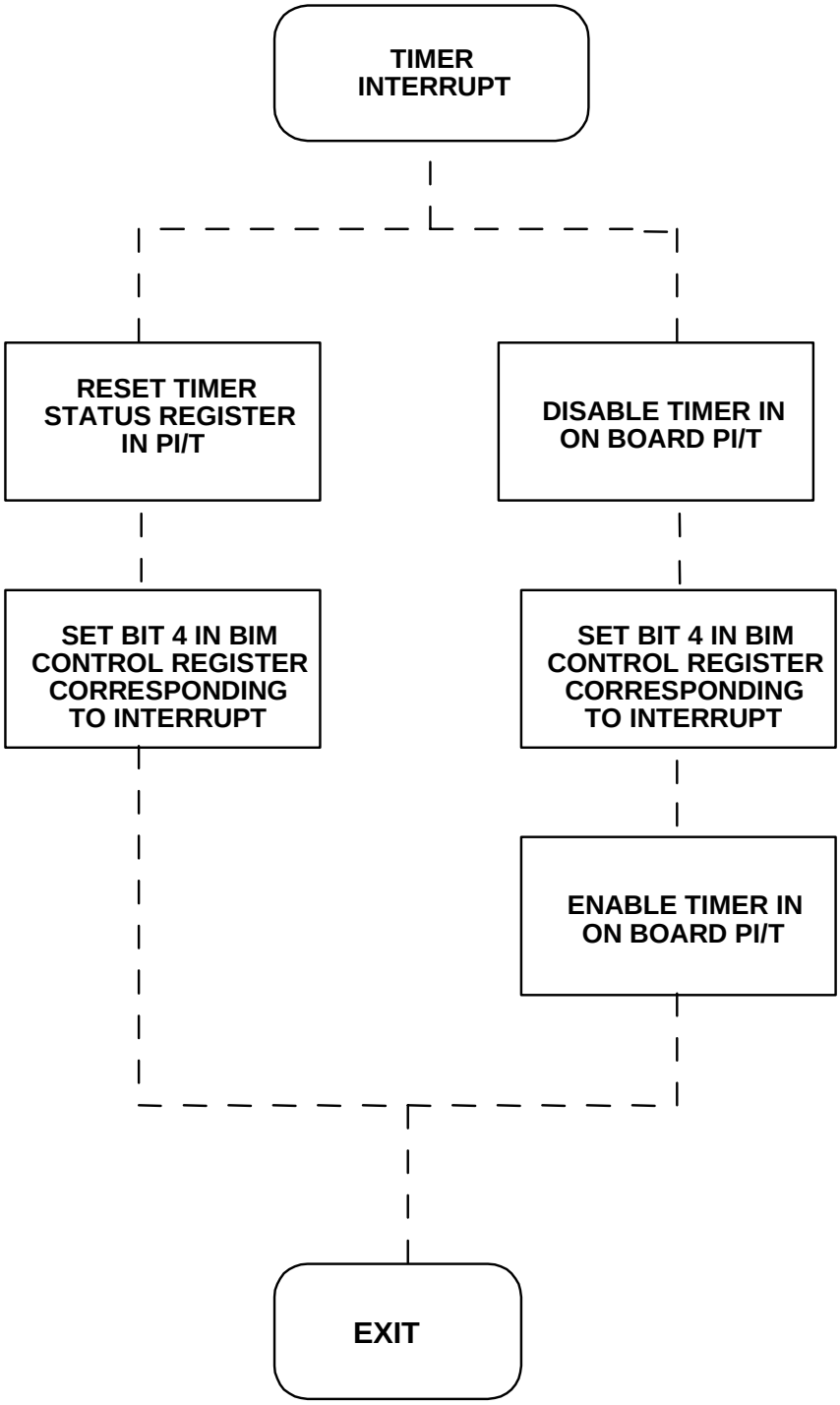


Figure 2-3 Timer Interrupt Sequence

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CHAPTER 3

Configuration and Installation

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC'S products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes in which they were shipped. When the board is to be laid on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

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Physical Installation

CAUTION: Do not install or remove boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

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Switch and Jumper Locations

Refer to Figure 3-1 for the locations of the switches and jumpers described in this section.

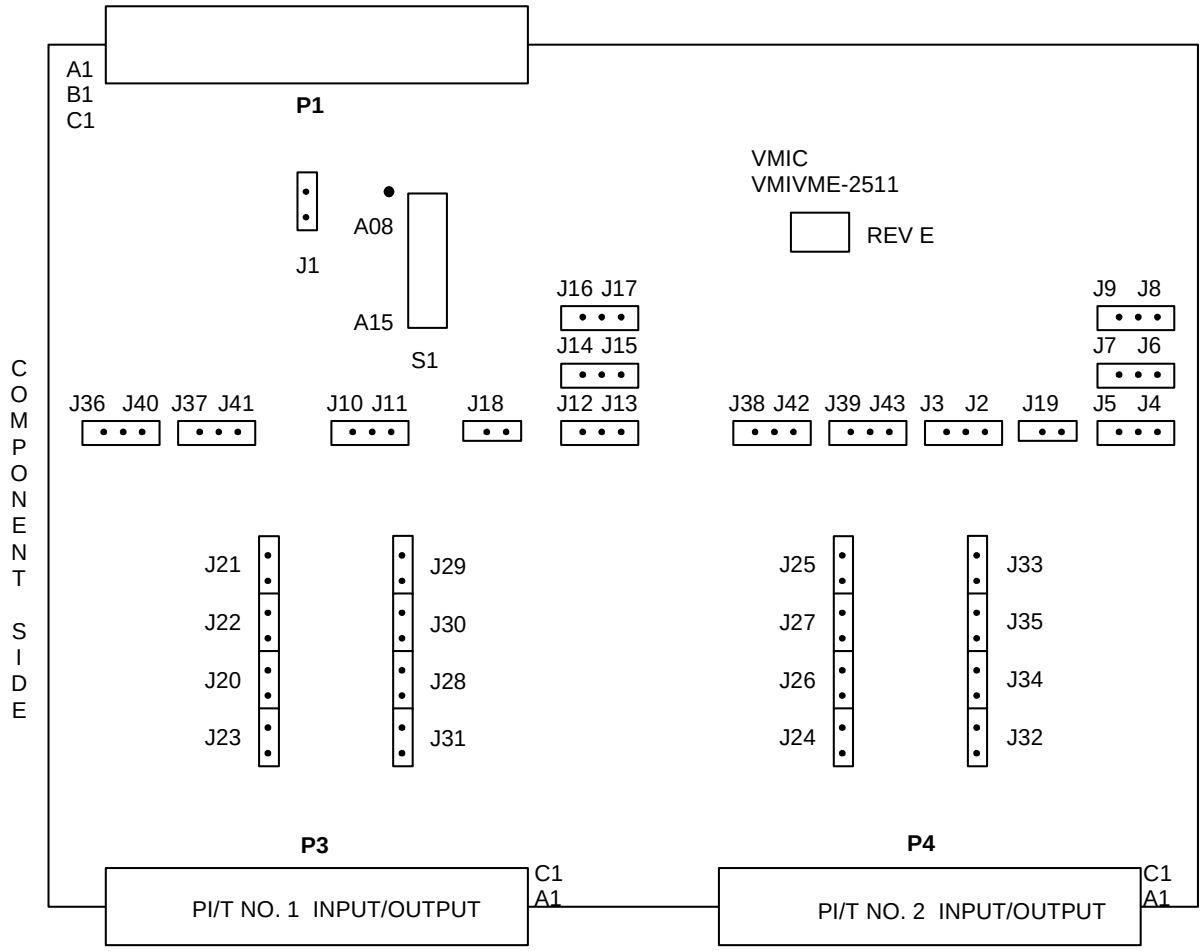


Figure 3-1 Switch and Jumper Locations

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Address Modifiers

The VMIVME-2511 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper J1 to enable the board to respond to short nonprivileged I/O access.

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Jumper and I/O Configuration

The block diagrams of Figure 3-3 on page 61 and Figure 3-4 on page 62 show the detailed jumpering options available on the VMIVME-2511. Table 3-1 on page 63 explains in detail the function of all the jumpers on the board. Not all of the jumpers used on the board are shown in Figure 3-3 and Figure 3-4. Refer to Figure 3-1 on page 56 for locations of all jumpers used on the board.

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Address Selection Switches

The VMIVME-2511 occupies 256 words in the short I/O space. The base address is selected by a single DIP switch. Figure 3-2 shows the switch and its use in the addressing scheme. The example shown below selects a base address of FF00 hexadecimal.

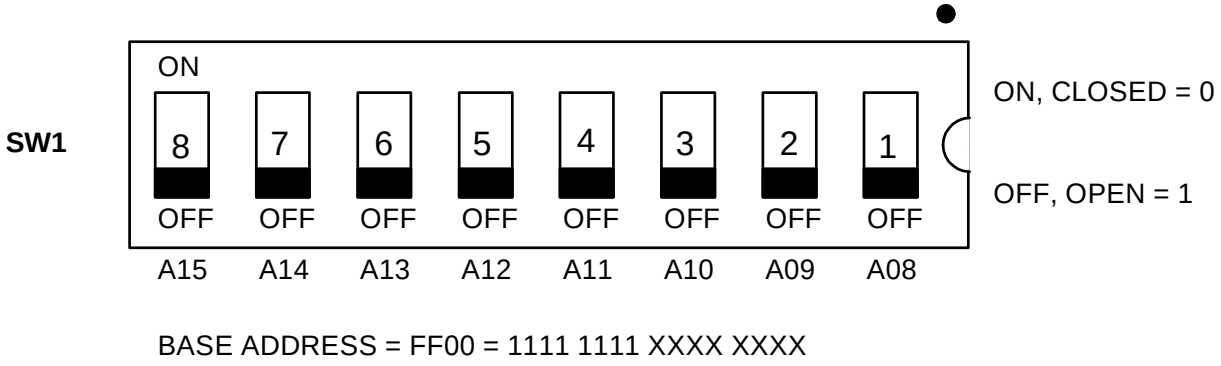


Figure 3-2 Address Select Switch, SW1

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I/O Cable and Card-Edge Connector Configuration

The I/O connectors (P3 and P4) are 64-pin DIN standard and were selected by VMIC because of their high quality. Details concerning the I/O connections are shown in Figure 3-5 on page 65. Conductor No. 1 is shown at the bottom of the connector as it plugs into the header, due to Pin No. 1 of the headers P3 and P4 being mounted as shown. Table 3-2 on page 65 and Table 3-3 on page 66 show the P3 and P4 connector pin assignments for the 64 channels of the VMIVME-2511. A compatible cable connector for the board is Panduit No. 120-964-435E. A compatible strain relief is Panduit No. 100-000-032. A compatible header soldered to the P.C. board is Panduit No. 120-964-033A.

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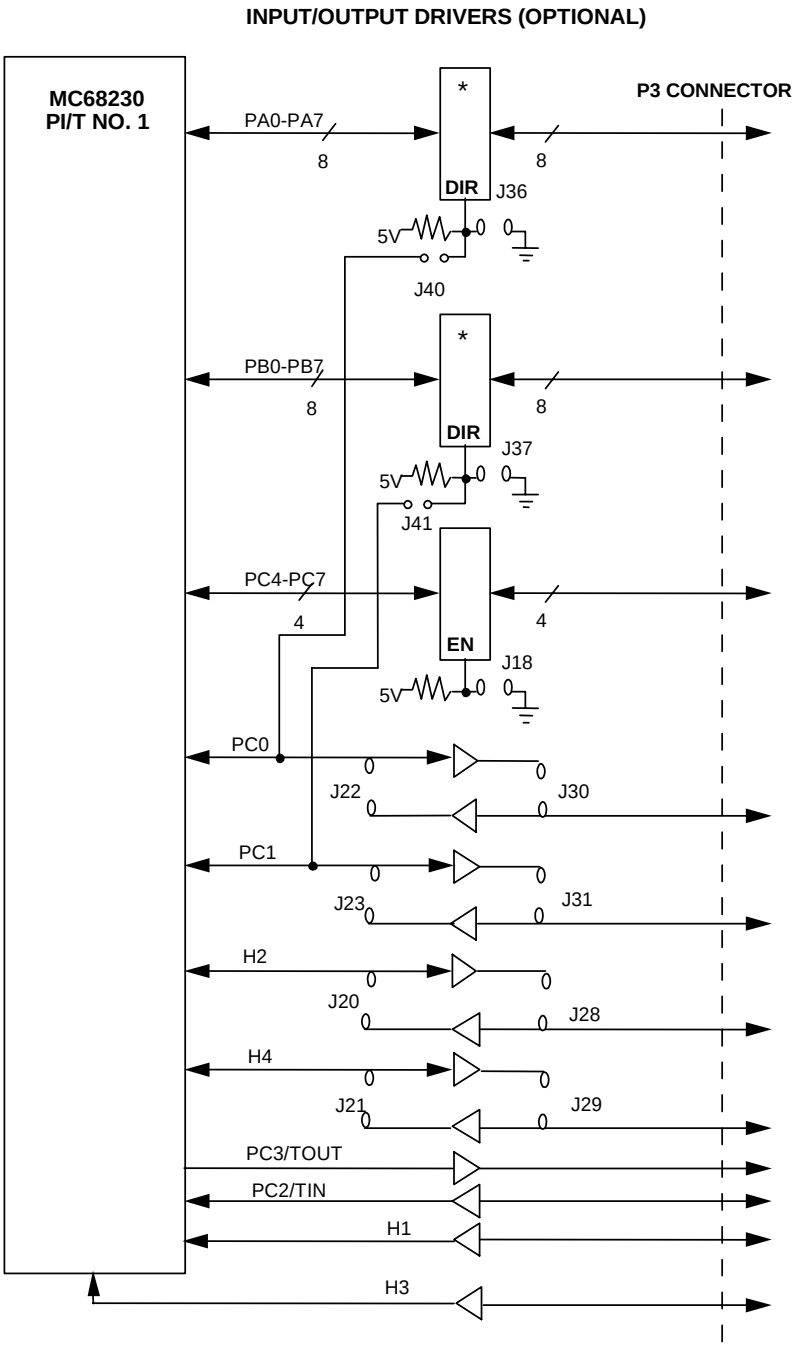


Figure 3-3 I/O and Jumper Block Diagram for PI/T No. 1

NOTE: (*) in Figure 3-3 designates optional I/O buffers.

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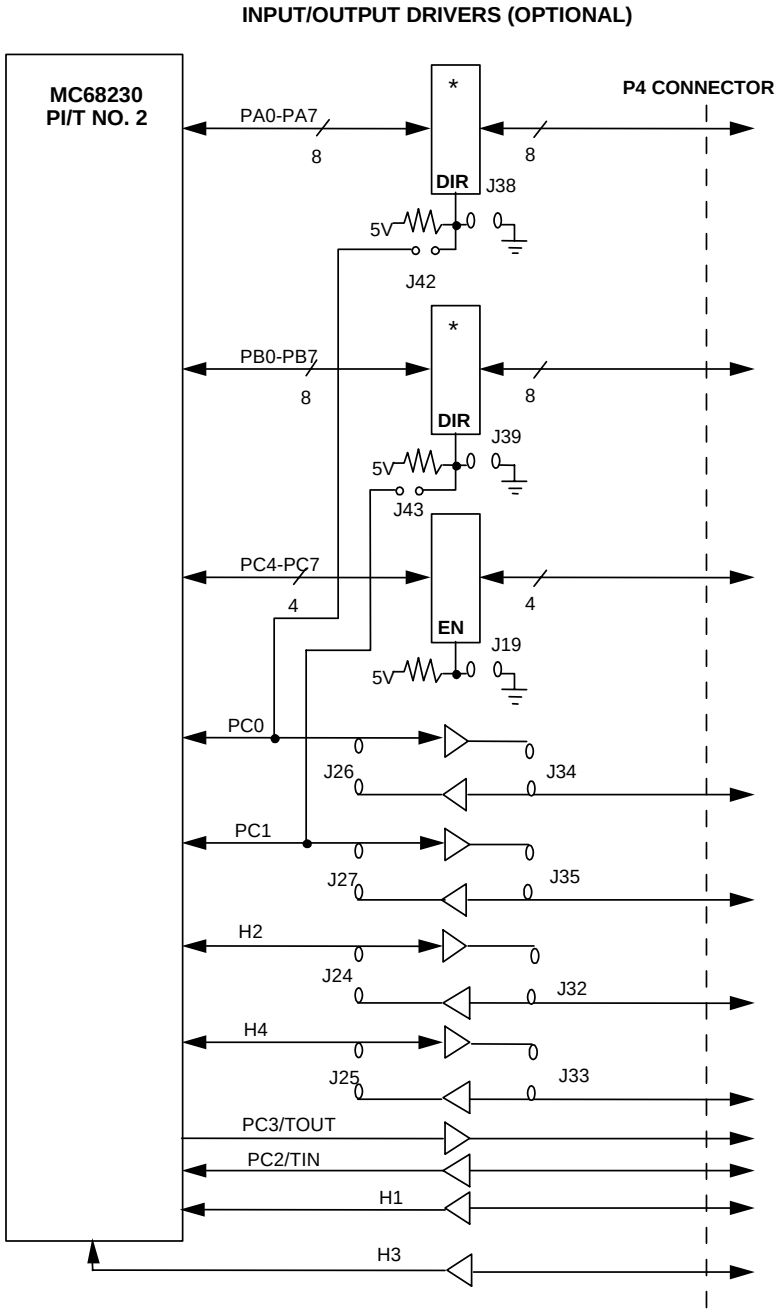


Figure 3-4 I/O and Jumper Block Diagram for PI/T No. 2

NOTE: (*) in Figure 3-4 designates optional I/O buffers.

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.

Table 3-1 Jumper Definition Table

Jumper	Definition
J1	Install for Short Non-Privileged I/O Access; otherwise, the board responds to Short Supervisory I/O Access.
J2 **	Install to connect PI/T No. 2-PC3 to the P4 Connector.
J3	Install to configure PI/T No. 2-PC3 for Timer Interrupt Request.
J4 **	Install to connect PI/T No. 2-PC5 to the P4 Connector.
J5	Install to configure PI/T No. 2-PC5 for Port Interrupt Request.
J6 **	Install to connect PI/T No. 2-PC6 to the P4 Connector.
J7	Install to configure PI/T No. 2-PC6 for Port Interrupt Acknowledge.
J8 **	Install to connect PI/T No. 2-PC7 to the P4 Connector.
J9	Install to configure PI/T No. 2-PC7 for Timer Interrupt Acknowledge.
J10 **	Install to configure PI/T No.1-PC3 for Timer Interrupt Request.
J11	Install to connect PI/T No. 1-PC3 to the P3 Connector.
J12 **	Install to configure PI/T No. 1-PC5 for Port Interrupt Requests.
J13	Install to connect PI/T No. 1-PC5 to the P3 Connector.
J14 **	Install to configure PI/T No. 1-PC6 for Port Interrupt Acknowledge.
J15	Install to connect PI/T No. 1-PC6 to the P3 Connector.
J16 **	Install to configure PI/T No. 1-PC7 for Timer Interrupt Acknowledge.
J17	Install to connect PI/T No. 1-PC7 to the P3 Connector.
J38 **	Install to configure port pins PA0-PA7 of PI/T No. 2 as an output port. Otherwise, it is an input port.
J42	Install to configure port pins PA0-PA7 of PI/T No. 2 as programmable I/O. Otherwise, it is an input port.
J39 **	Install to configure port pins PB0-PB7 of PI/T No. 2 as an output port. Otherwise, it is an input port.
J43	Install to configure port pins PB0-PB7 of PI/T No. 2 as programmable I/O. Otherwise, it is an input port.
J19	Install to configure port pins PC4-PA7 of PI/T No. 2 as an output port. Otherwise, it is an input port.
J36 **	Install to configure port pins PA0-PA7 of PI/T No. 1 as an output port. Otherwise, it is an input port.
J40	Install to configure port pins PA0-PA7 of PI/T No. 1 as programmable I/O. Otherwise, it is an input port.

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Table 3-1 Jumper Definition Table (Continued)

Jumper	Definition
J37 **	Install to configure port pins PB0-PB7 of PI/T No. 1 as an output port. Otherwise, it is an input port.
J41	Install to configure port pins PB0-PB7 of PI/T No. 1 as programmable I/O. Otherwise, it is an input port.
J18	Install to configure port pins PC4-PC7 of PI/T No. 1 as an output port. Otherwise, it is an input port.
J20 **	Install to configure H2 of PI/T No. 1 as an input.
J28	Install to configure H2 of PI/T No. 1 as an output.
J21 **	Install to configure H4 of PI/T No. 1 as an input.
J29	Install to configure H4 of PI/T No. 1 as an output.
J22 **	Install to configure PC0 of PI/T No. 1 as an input.
J30	Install to configure PC0 of PI/T No. 1 as an output.
J23 **	Install to configure PC1 of PI/T No. 1 as an input.
J31	Install to configure PC1 of PI/T No. 1 as an output.
J32 **	Install to configure H2 of PI/T No. 2 as an output.
J24	Install to configure H2 of PI/T No. 2 as an input.
J33 **	Install to configure H4 of PI/T No. 2 as an output.
J25	Install to configure H4 of PI/T No. 2 as an input.
J34 **	Install to configure PC0 of PI/T No. 2 as an output.
J26	Install to configure PC0 of PI/T No. 2 as an input.
J35 **	Install to configure PC1 of PI/T No. 2 as an output.
J27	Install to configure PC1 of PI/T No. 2 as an input.

CAUTION: Paired jumpers in Table 3-1 (designated by **) are mutually exclusive. If one of the jumper pairs is installed, the other jumper in the pair must *not* be installed or damage may result to the VMIVME-2511 or field electronics connected to the VMIVME-2511.

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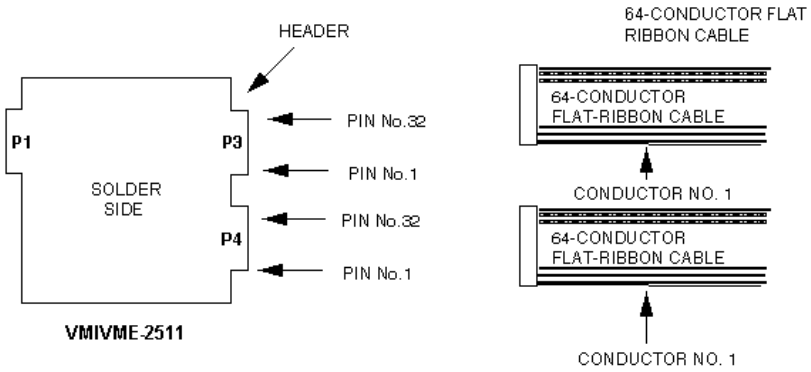


Figure 3-5 Cable Connector Configuration

Table 3-2 P3-PI/T No. 1 Pin and Function Assignments

Pin	Function	Pin	Function
A32	PA0	A16	PB6
A31	PA1	A15	PB7
A30	PA2	A14	H3
A29	PA3	A13	H4
A28	PA4	A12	PC0
A27	PA5	A11	PC1
A26	PA6	A10	PC2
A25	PA7	A09	PC3
A24	H1	A08	PC4
A23	H2	A07	PC5
A22	PB0	A06	PC6
A21	PB1	A05	PC7
A20	PB2	A04	N.C.
A19	PB3	A03	N.C.
A18	PB4	A02	N.C.
A17	PB5	A01	N.C.

NOTE: All row C pins of P3 are grounded.

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Table 3-3 P4-PI/T No. 2 Pin and Function Assignments

Pin	Function	Pin	Function
A32	PA0	A16	PB6
A31	PA1	A15	PB7
A30	PA2	A14	H3
A29	PA3	A13	H4
A28	PA4	A12	PC0
A27	PA5	A11	PC1
A26	PA6	A10	PC2
A25	PA7	A09	PC3
A24	H1	A08	PC4
A23	H2	A07	PC5
A22	PB0	A06	PC6
A21	PB1	A05	PC7
A20	PB2	A04	N.C.
A19	PB3	A03	N.C.
A18	PB4	A02	N.C.
A17	PB5	A01	N.C.

NOTE: All row C pins of P4 are grounded.

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Maintenance

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Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

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Maintenance Prints

User-level repairs are not recommended. Logic diagram 141-022511-000 contains drawings and diagrams for reference purposes only.

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