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# VMIVME-2510B
# 64-Bit TTL I/O Megamodule

## Product Manual

A GE Fanuc Company

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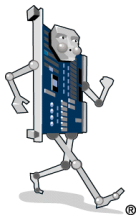
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(IOWorks man figure)













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# Overview

## Introduction

### Features

The VMIVME-2510B is a VMEbus compatible 64-Bit TTL Input/Output Board. Its features include:

- The direction of each 8-bit port is individually programmable
- 64 mA sink capability (15 mA source)
- Separate board address decoding for control and data registers
- Built-in-test logic for fault detection and isolation
- Fail LED
- Compatible with VMIVME-9016 intelligent I/O controller
- High reliability DIN type I/O connectors
- 8-, 16-, 32-bit transfers
- Optional open collector outputs



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# Functional Description

The VMIVME-2510B is a member of VMIC's Megamodule™ family, which is designed with common programming features. Subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these products (VMIVME-1110, VMIVME-2120, VMIVME-2130, and VMIVME-2510B) are designed with two sets of board address switches to provide an efficient memory address map for CSR and I/O addresses. CSR address switches may be set such that all CSR's among a variety of boards in a system may be mapped into contiguous memory locations.

The Megamodule™ product is also designed to support 8-, 16-, and 32-bit data transfers. Specific hardware has been designed into the VMIVME-2510B to support built-in-test functions. The VMIVME-2510B supports both off-line and on-line fault detection and isolation. A front panel Fail LED is used to indicate when a fault exists on this board. Upon power-up or reset, the LED is illuminated. After successfully completing board-level diagnostics, the LED can be extinguished.



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# Reference Material List

The reader should refer to "The VMEbus Specification" ANSI/IEEE STD1014-1987 IEC 821 and 297 for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

### *VMEbus Specification Rev. C. and the VMEbus Handbook*

VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

### *Physical Description and Specification*

Refer to Specification 800-000103-000 available from:
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12090 South Memorial Pkwy.
Huntsville, AL 35803-3308, USA
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(800) 322-3616
FAX: (256) 882-0859
www.vmic.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

| Title | Document No. |
|---|---|
| Digital Input Board Application Guide | 825-000000-000 |
| Change-of-State Application Guide | 825-000000-002 |
| Digital I/O (with Built-in-Test) Product Line Description | 825-000000-003 |
| Connector and I/O Cable Application Guide | 825-000000-006 |



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# Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

## Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

## Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

## Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

## Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

## Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

## Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**WARNING:** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.



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## Warnings, Cautions and Notes

**STOP** informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

**WARNING** denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION** denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE** denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.



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CHAPTER 1

# Theory of Operation

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## Operational Overview

As shown in the functional block diagram in Figure 1-1 on page 18, the VMIVME-2510B provides for the control/monitoring of 64 output/input lines via eight 8-bit data registers. These 64 bits of I/O are addressable as two 32-bit long words, four 16-bit words, or as eight 8-bit bytes. These eight registers are selected by address bits A2, A1, DS0 and DS1.

Direction control of I/O is on a byte basis. Eight direction control bits in the CSR select whether an octal port is to be input or output. In addition, the CSR contains a Fail LED bit, two test mode bits, and five storage bits that can be used for message passing between VMEbus masters.

## Built-in-Test

The built-in-test feature of the VMIVME-2510B is enabled by asserting the Test Mode (TM) bits in the CSR. Test Mode P3 controls the transceivers for connector P3, while Test Mode P4 controls the P4 transceivers. While in the Test Mode, the I/O transceivers are disabled, allowing data to be looped back through the I/O Data Registers for test purposes without disturbing the device being controlled. A port



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must be configured for output before loopback testing can be done. This requires a logic "one" to be written to the appropriate control bit of the CSR. The Test Mode and the Fail LED (FL) bits are initialized active (logic "zero") by system reset. The design of the Built-in-Test hardware supports off-line and on-line fault detection and isolation and on-line fault isolation.

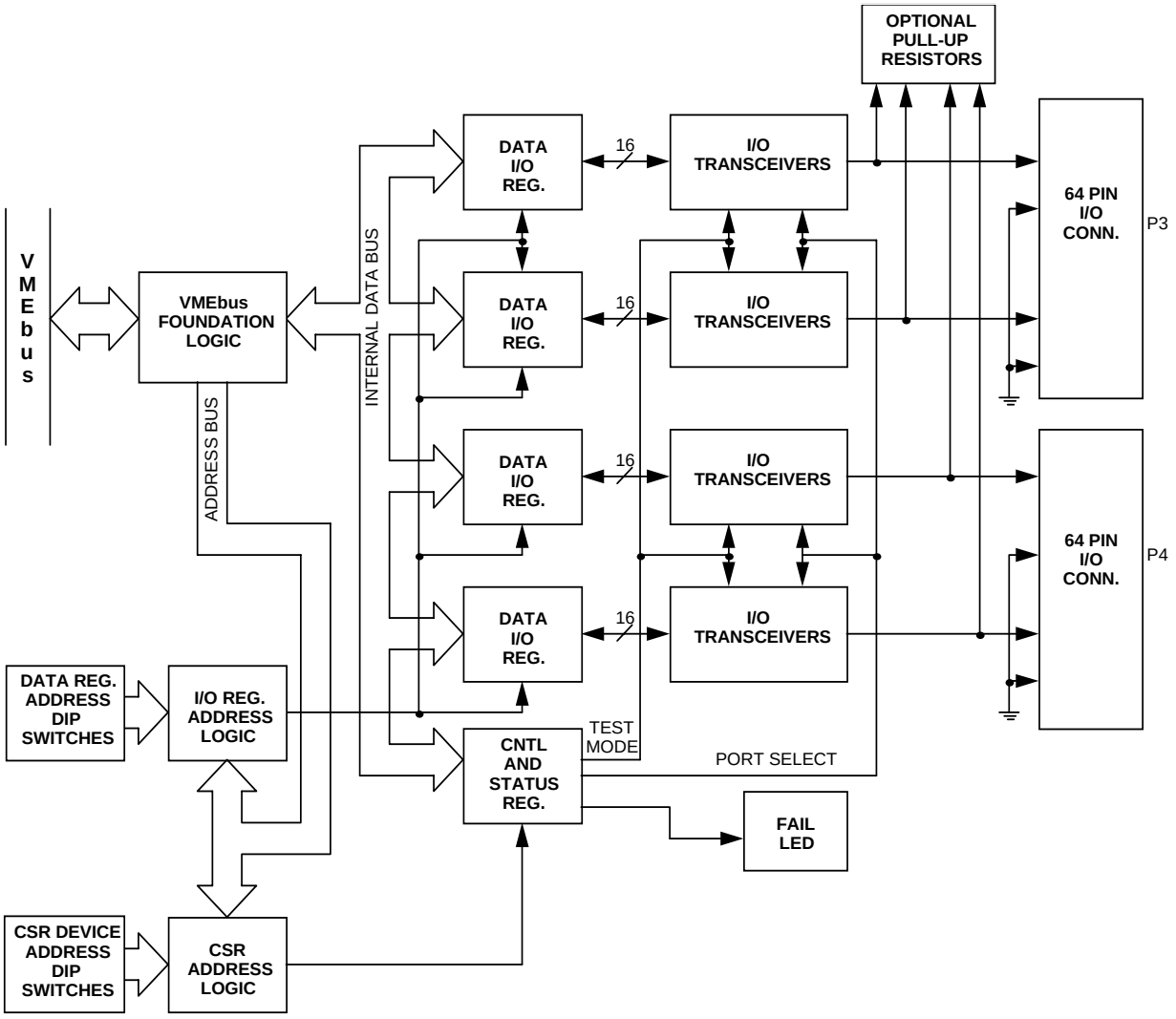



**Figure 1-1** Functional Block Diagram



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# Board Addressing

The VMIVME-2510B is designed to support data transfers in supervisory or non-privileged short I/O memory space. A jumper is provided as shown in Figure 1-2 on page 20 (Address Decoder Block Diagram) to allow user selection of either I/O access type. The jumper (J1) is shown on the logic diagram Figure 1-7 on page 26. The VMIVME-2510B is factory configured (Jumper J1 is not installed) to respond to short-supervisory I/O access.

The VMIVME-2510B is designed with two sets of board select switches and decode logic, as shown in Figure 1-2 on page 20, to provide an efficient memory address map for CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into contiguous memory locations when configuring subsystems that require more than one board.



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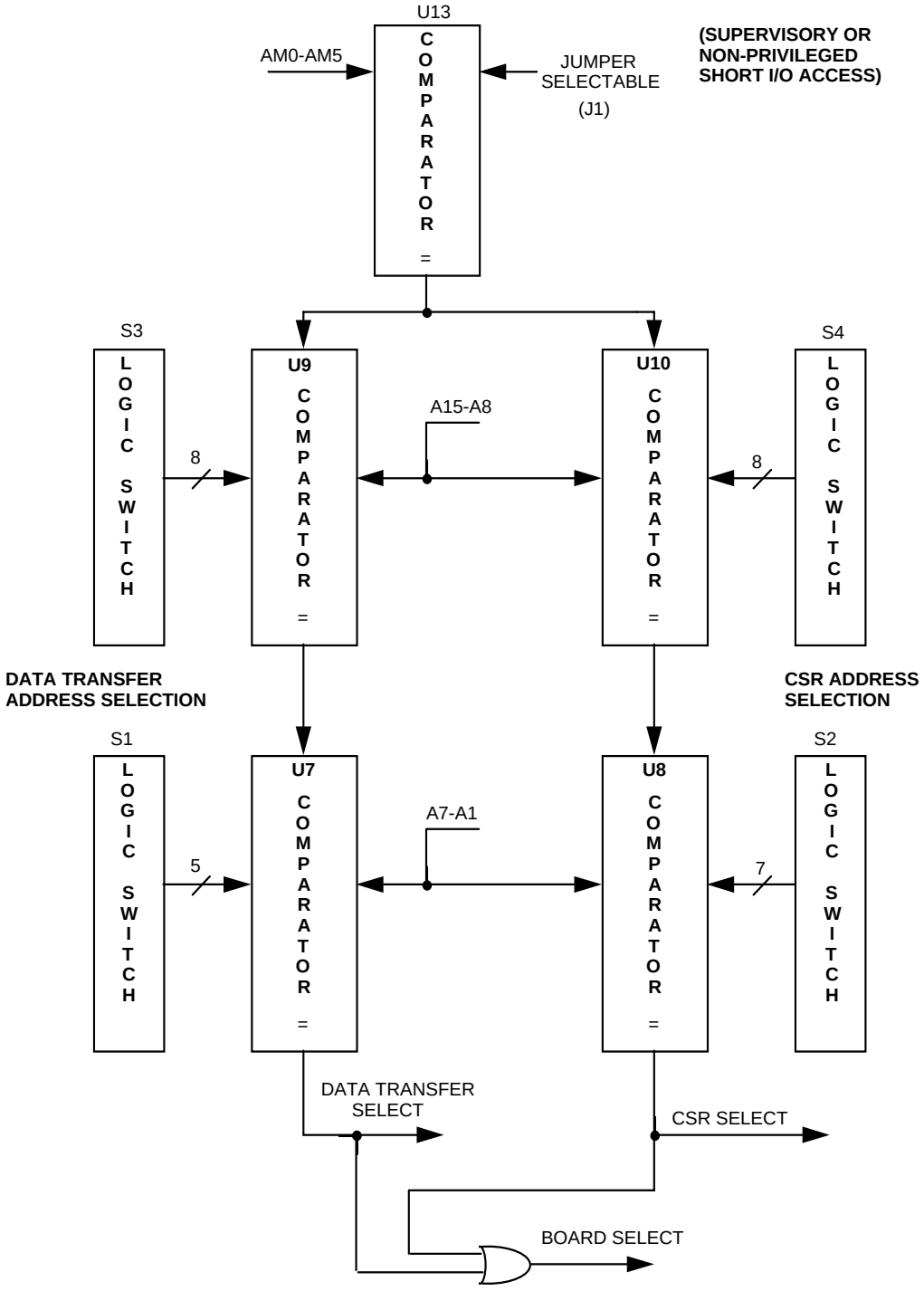



**Figure 1-2** Address Decoder Block Diagram



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## VMEbus Compatibility Logic

Typical VMEbus drivers, receivers and control logic are shown in Figure 1-3, Figure 1-4 on page 22 and Figure 1-5 on page 23.

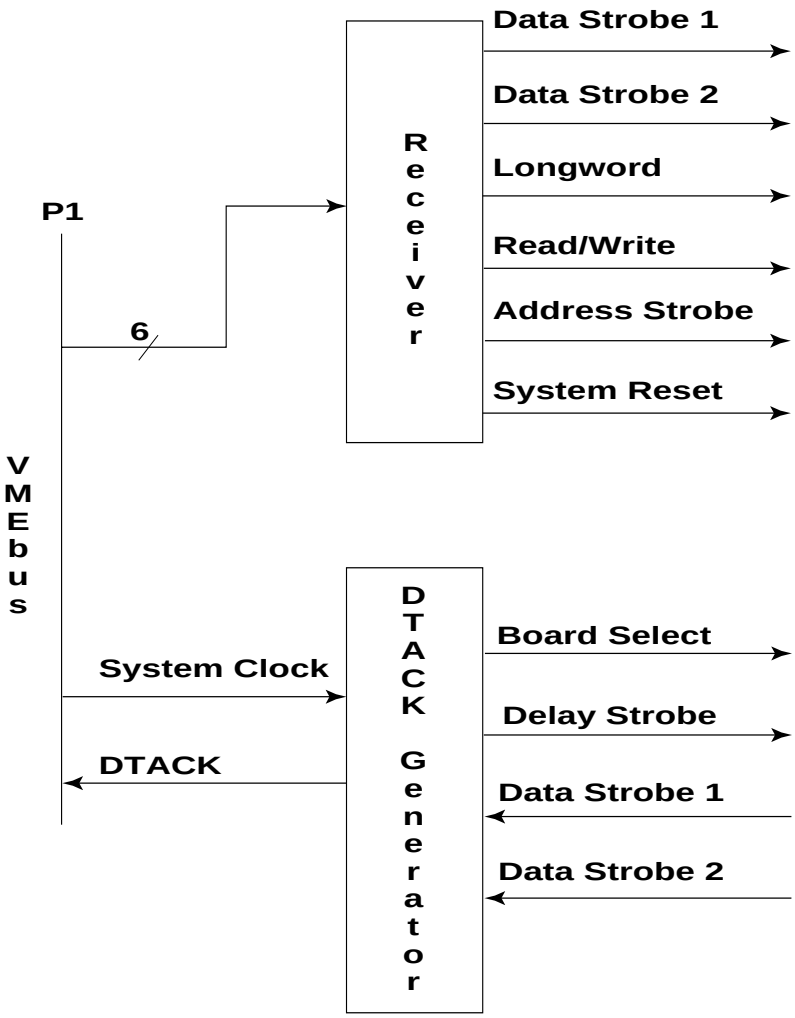



**Figure 1-3** Control Section Diagram



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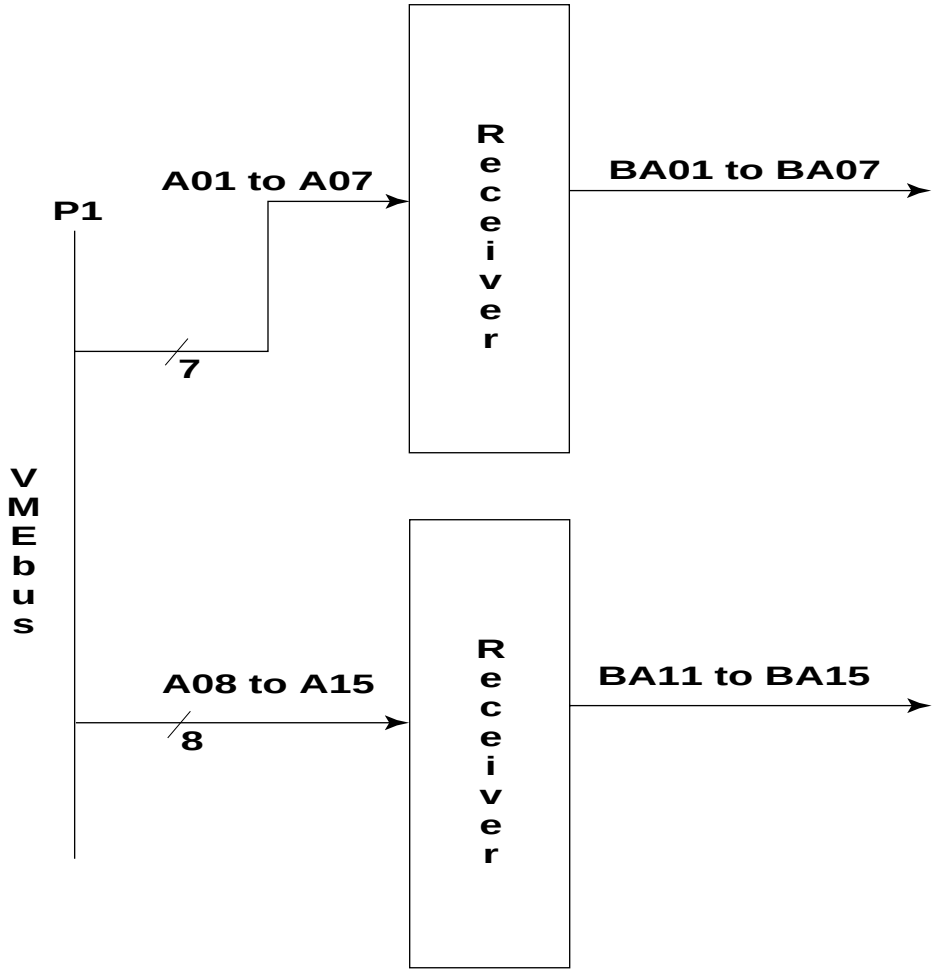



**Figure 1-4** Address Receiver Block Diagram



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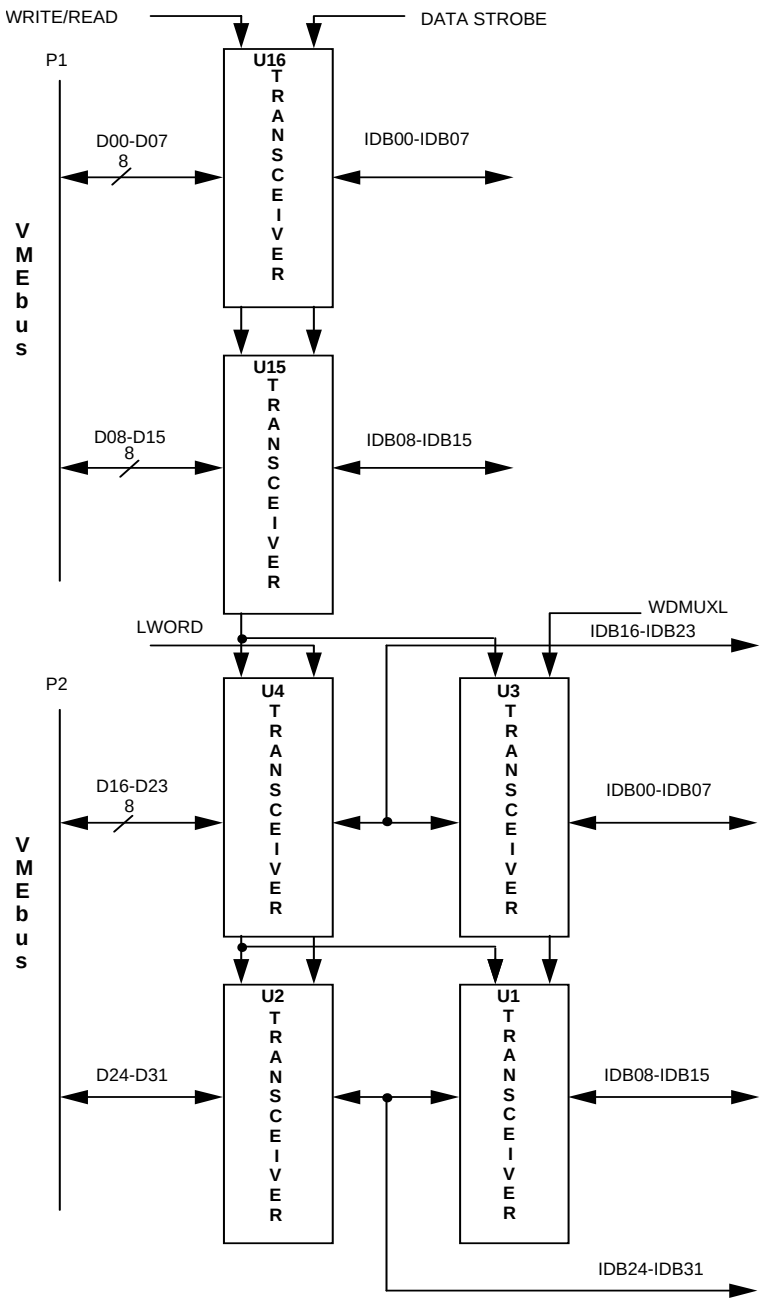



**Figure 1-5** Data Transfer Block Diagram



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## Data Transfers

Data transfer transceivers are shown in Figure 1-5 on page 23. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries.



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## I/O Registers Control Logic

The VMIVME-2510B is designed utilizing the AMD2952 dual-rank octal bi-directional bus latch. The control logic shown in Figure 1-6 is designed to support I/O transfers to eight 8-bit registers. To simplify the control logic design, the read and write control logic is separated to take advantage of the 2952's control lines. As shown in Figure 1-6 below, U6 separates the control signals into write and read register strobes, and U22 provides additional control logic to allow 8-, 16-, and 32-bit data transfers.

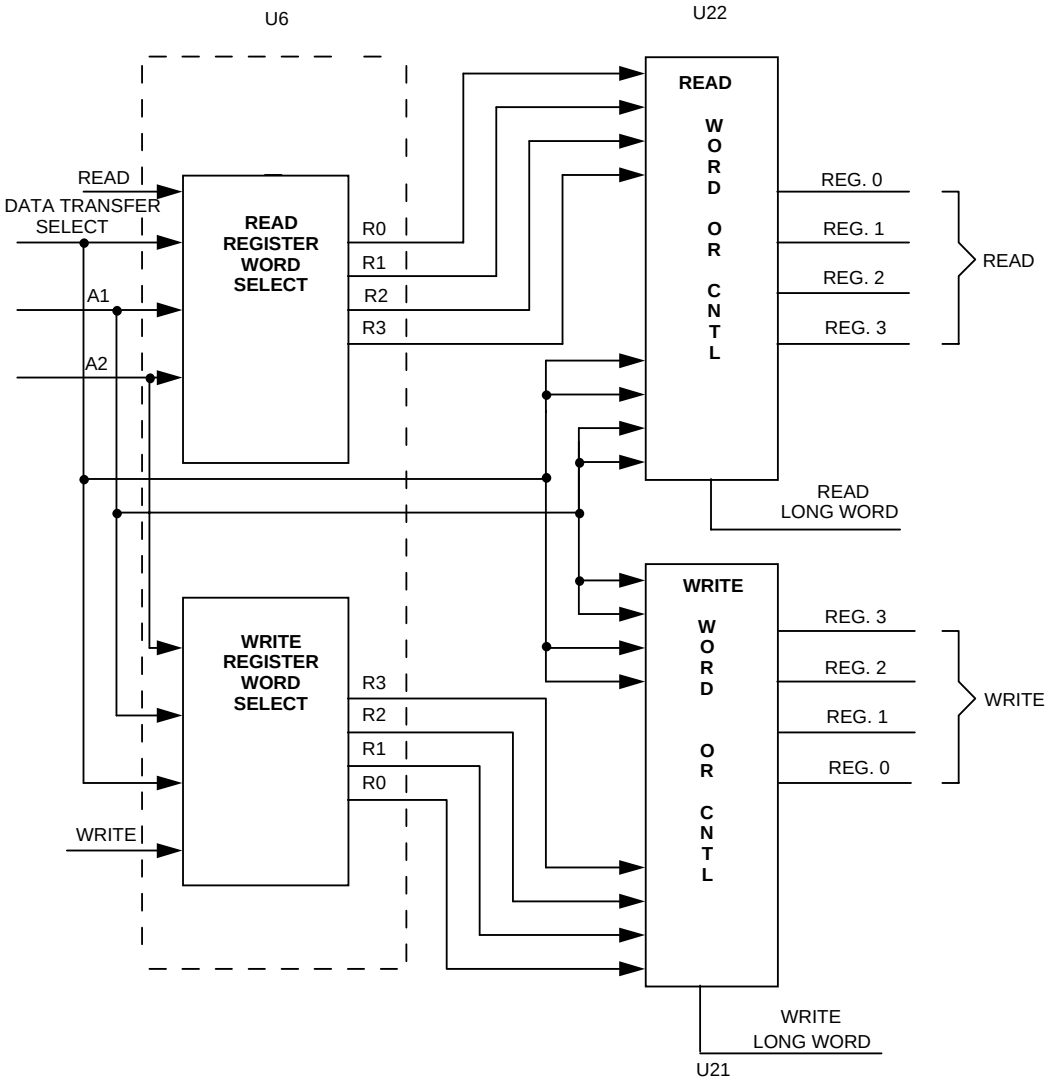



**Figure 1-6** I/O Register Control Logic Block Diagram



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## Control and Status Register (CSR)

The CSR is a 16-bit read / write data register that is independently selectable as described in *Board Addressing* on page 19. The CSR controls the direction of data transfers on each 8-bit I / O port, the Built-in-Test operations, and the front panel Fail LED. Bits 0 through 4 are not used for on-board operations; therefore, the user may program these bits as system resource flags, or semaphores, if required. The CSR is initialized active (outputs are logic "zeros") by a system reset. This enables both Test Mode bits, which places the transceivers in the TRI-STATE mode, and lights the front panel Fail LED. CSR control logic is shown in Figure 1-7 below.

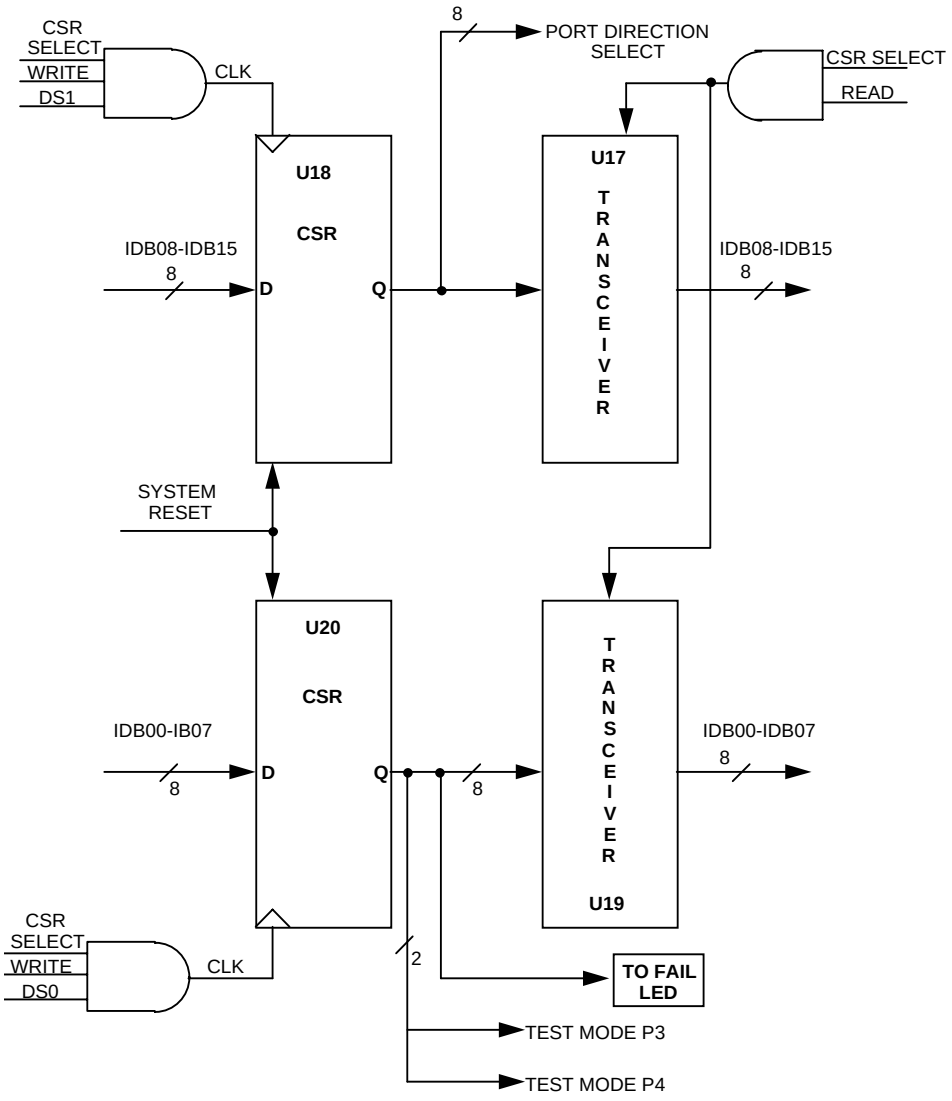



**Figure 1-7** CSR Control Logic Block Diagram



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## I/O Data Registers and Transceivers

The VMIVME-2510B is designed utilizing eight octal bi-directional registers (AMD 2952), as shown in Figure 1-8 on page 28 through Figure 1-11 on page 31. The I/O data port of each register is connected to an I/O transceiver as shown in Figure 1-9 on page 29 and Figure 1-11 on page 31. These transceivers provide the I/O buffering for the data received from, or transmitted to, the user device connected to the P3 and P4 front panel connectors. The VMIVME-2510B may be ordered with open collector outputs and optional pull-up resistors as shown in Figure 1-9 on page 29 and Figure 1-11 on page 31; however, this option is available as 64 output bits only.



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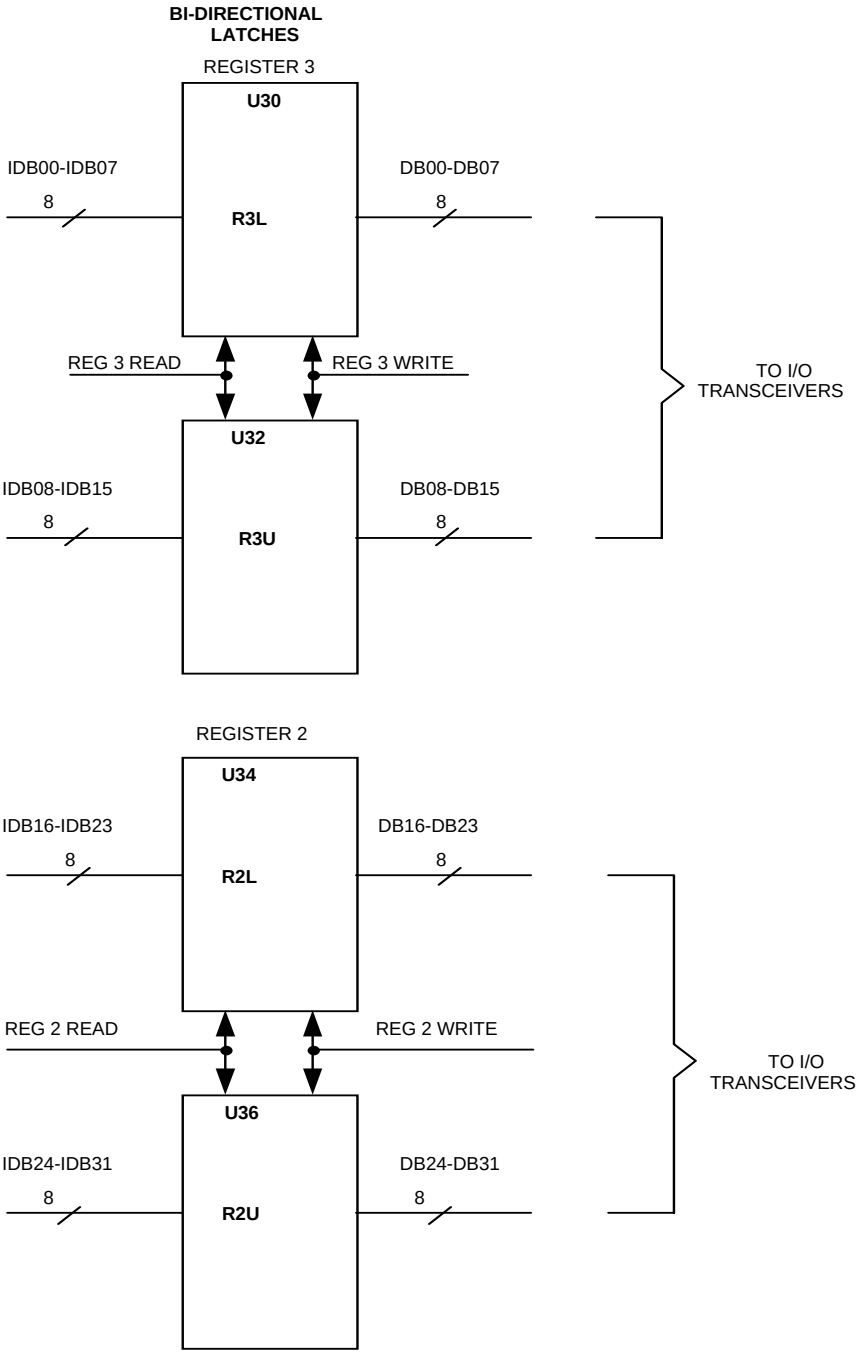



**Figure 1-8** I/O Registers Bank A Block Diagram



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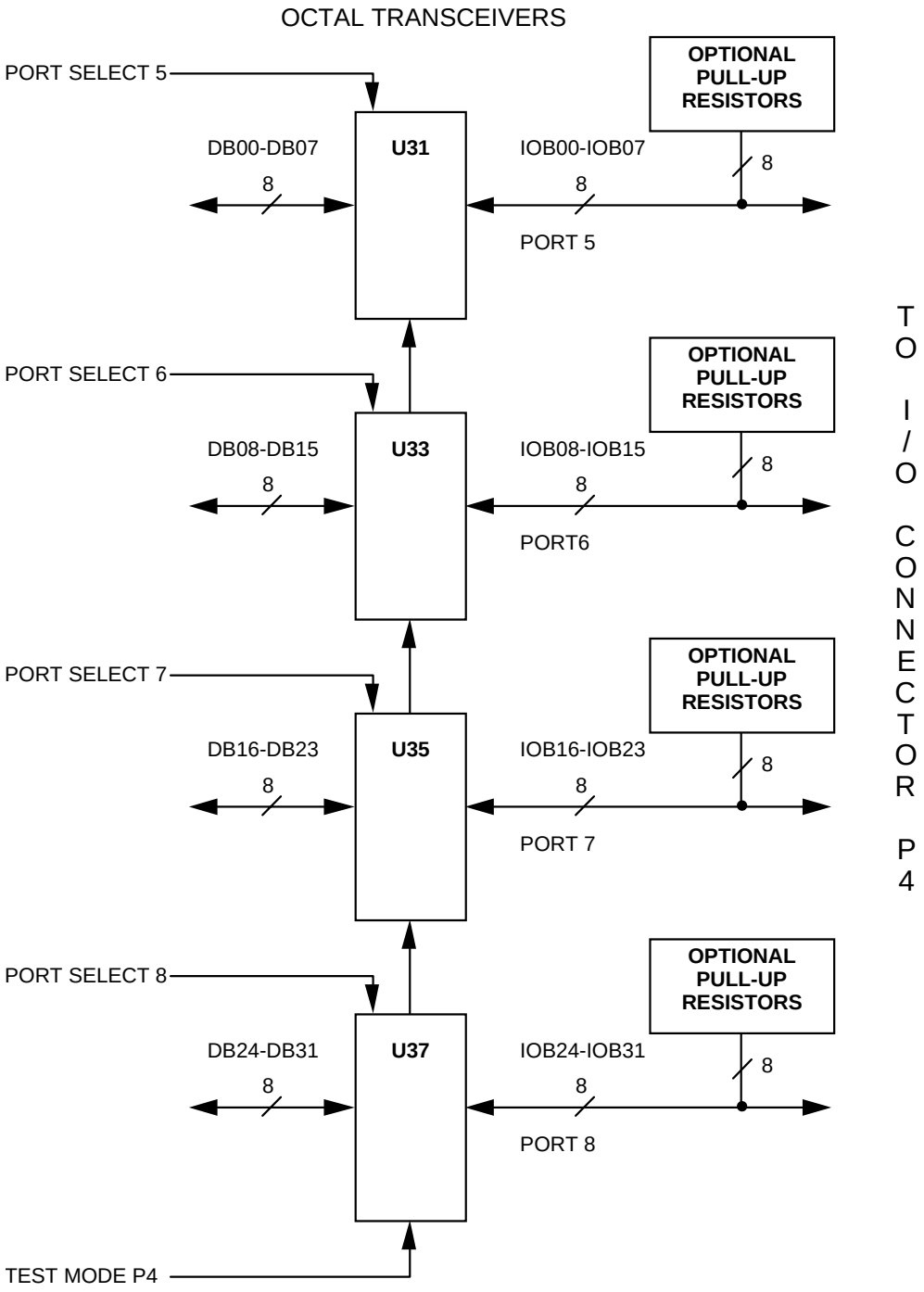



**Figure 1-9** I/O Ports Bank A Block Diagram



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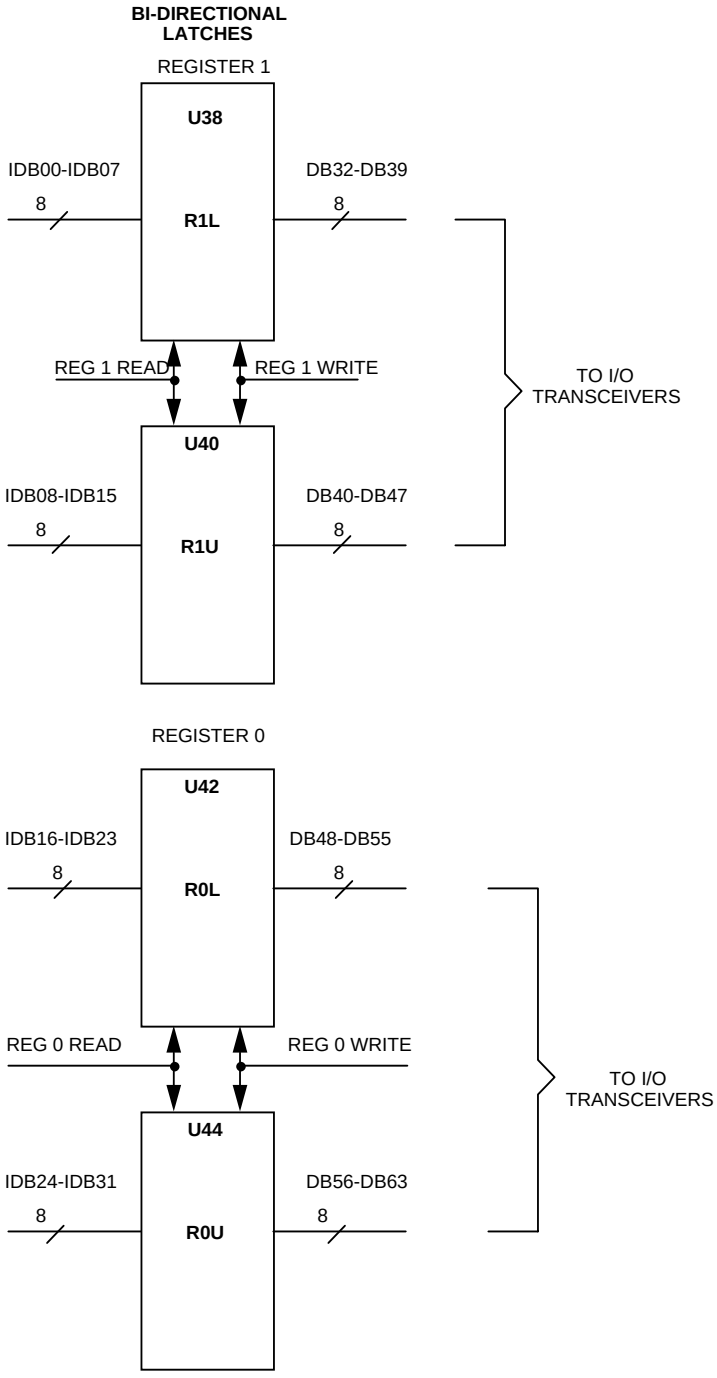



**Figure 1-10** I/O Registers Bank B Block Diagram



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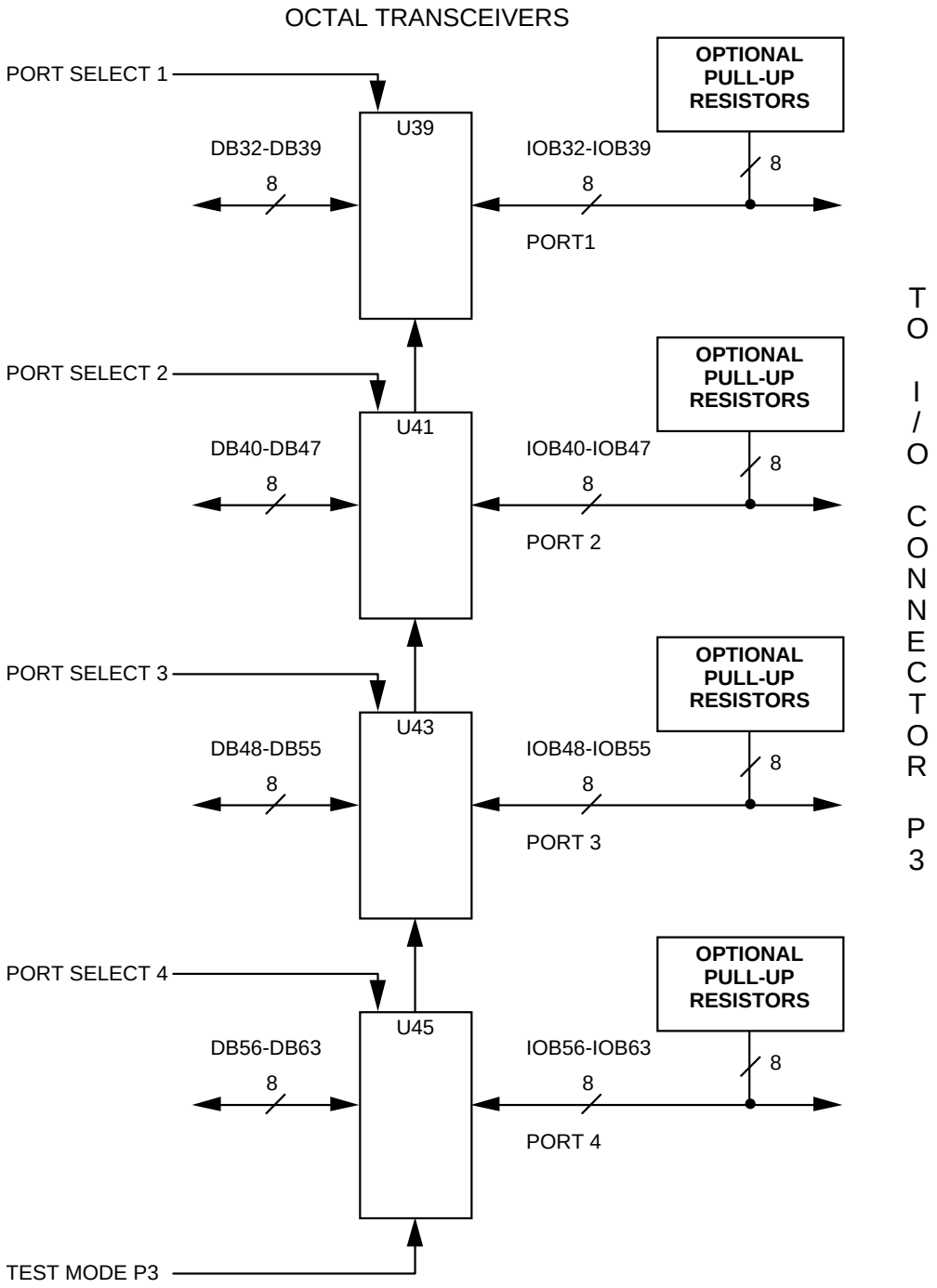



**Figure 1-11** I/O Ports Bank B Block Diagram



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CHAPTER
2

# Configuration and Installation

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## Introduction

This Chapter explains the proper unpacking and installation procedures for the VMIVME-2510B 64-bit TTL I/O Megamodule. Address and node configurations are also discussed.



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# Unpacking Procedures

**CAUTION:** Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

## Physical Installation

**CAUTION:** Do not install or remove the board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.



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## Jumper and Switch Locations

The physical positions of the jumpers and switches described in this section are shown in Figure 2-1.

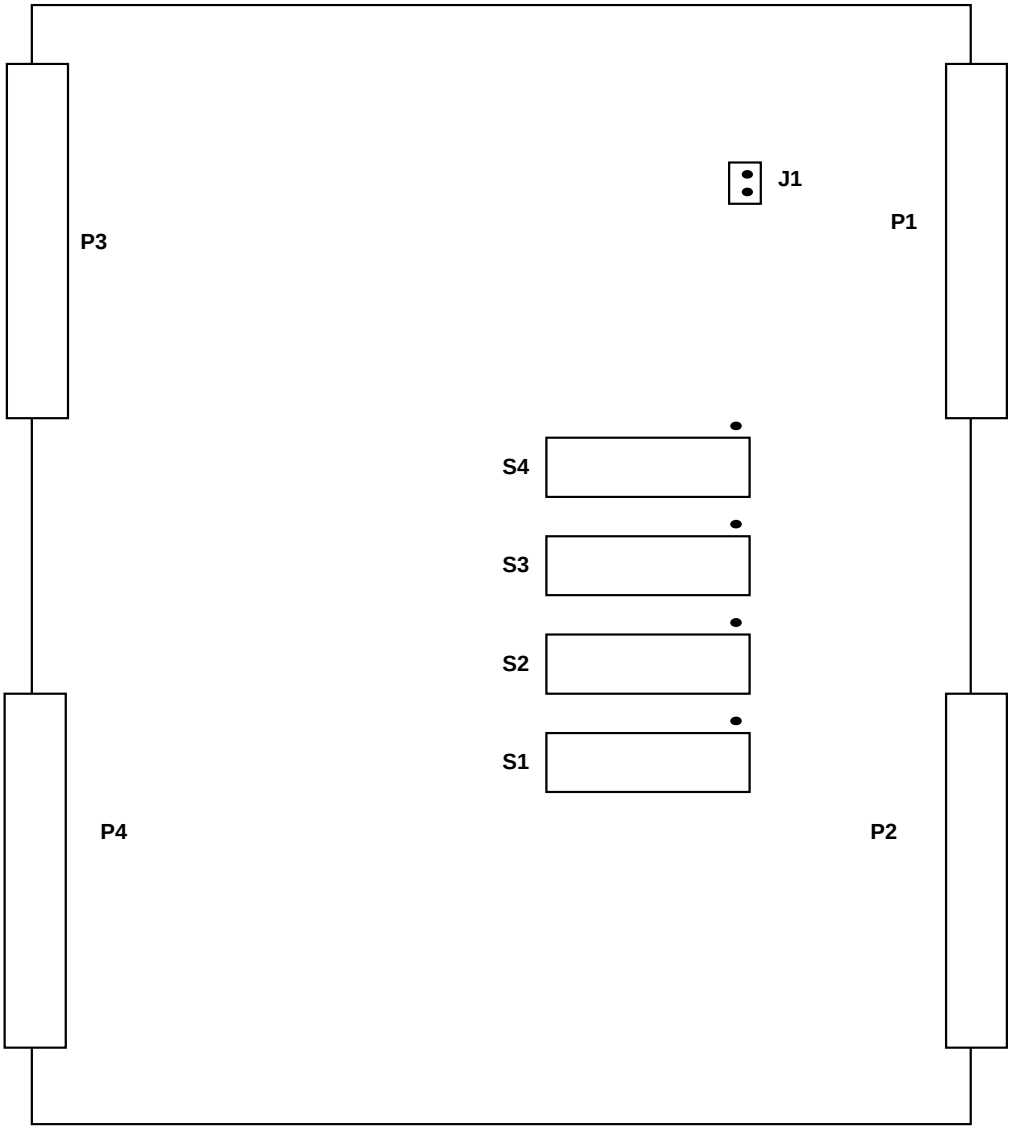



**Figure 2-1** Switch and Jumper Locations



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## Address Modifiers

The VMIVME-2510B is configured at the factory to respond to short supervisory I/O access. This configuration can be changed to short non-privileged by installing jumper J1.



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## Address Selection Switches

Two sets of board select switches are provided. The switches shown in Figure 2-2 select the base address of the Data Registers, and the switches shown in Figure 2-3 select the CSR base address. The figures also show the switches used in the addressing scheme.

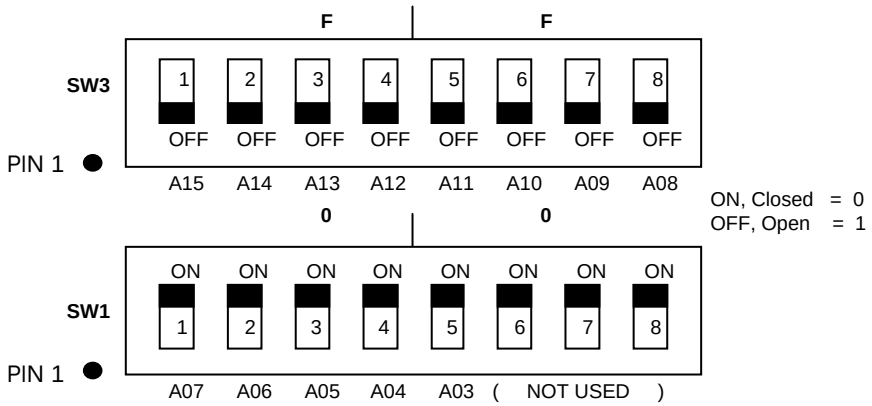



**Figure 2-2** Data Register Base Address Select Switches, SW3 and SW1

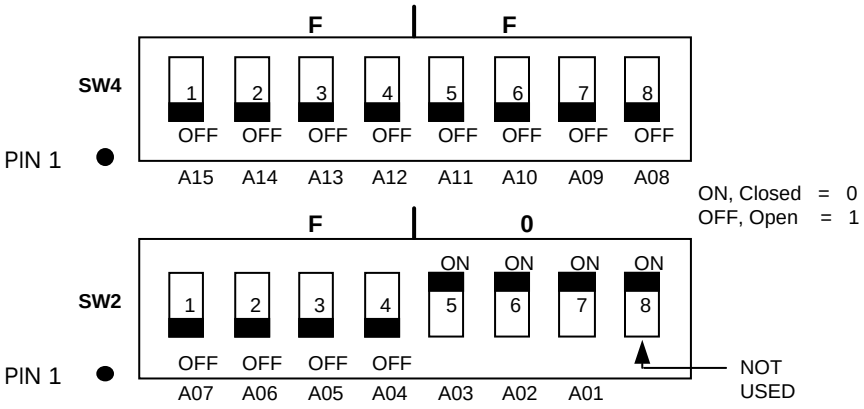



**Figure 2-3** CSR Base Address Select Switches, SW4 and SW2



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## I/O Cable and Card-Edge Connector Configuration

The I/O connectors (P3 and P4) on the VMIVME-2510B are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Applications Guide (VMIC Publication 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning I/O connections are shown in Figure 2-4 below. This figure has conductor no. 1 shown at the bottom of the connector as it plugs into the header, due to pin no. 1 of P3 and P4 being mounted as shown. Table 2-1 on page 39 and Table 2-2 on page 39 depict the P3 and P4 connector pin assignments for the 64 I/O channels of the VMIVME-2510B. A compatible flat-ribbon cable connector for the VMIVME-2510B is Panduit No. 120-964-435E and strain relief, Panduit No.100-000-032.

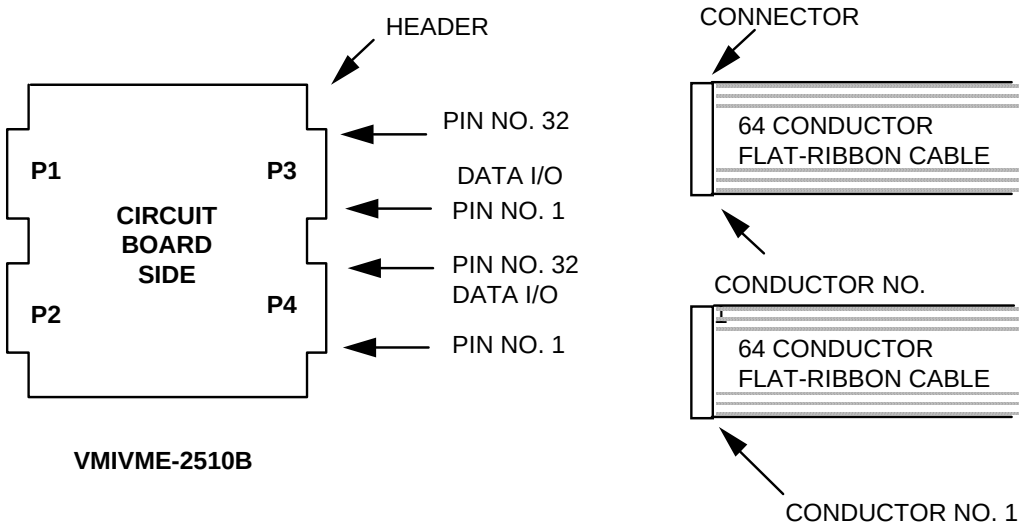



**Figure 2-4** Cable Connector Configuration



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**Table 2-1** P3 Pin and Channel Assignment

| P3* | | P3* | |
|---|---|---|---|
| **Row A Pin#** | **Channel No.** | **Row A Pin#** | **Channel No.** |
| 32 | 63 | 16 | 47 |
| 31 | 62 | 15 | 46 |
| 30 | 61 | 14 | 45 |
| 29 | 60 | 13 | 44 |
| 28 | 59 | 12 | 43 |
| 27 | 58 | 11 | 42 |
| 26 | 57 | 10 | 41 |
| 25 | 56 | 09 | 40 |
| 24 | 55 | 08 | 39 |
| 23 | 54 | 07 | 38 |
| 22 | 53 | 06 | 37 |
| 21 | 52 | 05 | 36 |
| 20 | 51 | 04 | 35 |
| 19 | 50 | 03 | 34 |
| 18 | 49 | 02 | 33 |
| 17 | 48 | 01 | 32 |

*All P3 Row C pins are connected to ground.

**Table 2-2** P4 Pin and Channel Assignment

| P4* | | P4* | |
|---|---|---|---|
| **Row A Pin#** | **Channel No.** | **Row A Pin#** | **Channel No.** |
| 32 | 31 | 16 | 15 |
| 31 | 30 | 15 | 14 |
| 30 | 29 | 14 | 13 |
| 29 | 28 | 13 | 12 |
| 28 | 27 | 12 | 11 |
| 27 | 26 | 11 | 10 |
| 26 | 25 | 10 | 09 |
| 25 | 24 | 09 | 08 |
| 24 | 23 | 08 | 07 |
| 23 | 22 | 07 | 06 |
| 22 | 21 | 06 | 05 |
| 21 | 20 | 05 | 04 |
| 20 | 19 | 04 | 03 |
| 19 | 18 | 03 | 02 |
| 18 | 17 | 02 | 01 |
| 17 | 16 | 01 | 00 |

*All P4 Row C pins are connected to ground.



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CHAPTER

3

# Programming

## Contents


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## Introduction

### Register Map

The VMIVME-2510B contains eight 8-bit I/O Data Registers and a 16-bit CSR. The I/O Data Registers allow access of 64 I/O channels and are addressable as two 32-bit long words, four 16-bit words, or as eight 8-bit bytes (see Table 3-1 on page 44). The CSR is addressable as a 16-bit word or as two 8-bit bytes (see Table 3-2 on page 46).

The register numbering is based on the hexadecimal address of each register; whereas, the input/output channel numbers are based on the CPU bit numbering and location of the least significant byte in a long word. For example, if a long word is written to address XXX4, the least significant byte will be placed in data register DR7, with bit 0 of DR7 being the least significant bit of the long word. Figure 3-1 on page 42 shows a basic VMIVME-2510B programming flow chart.

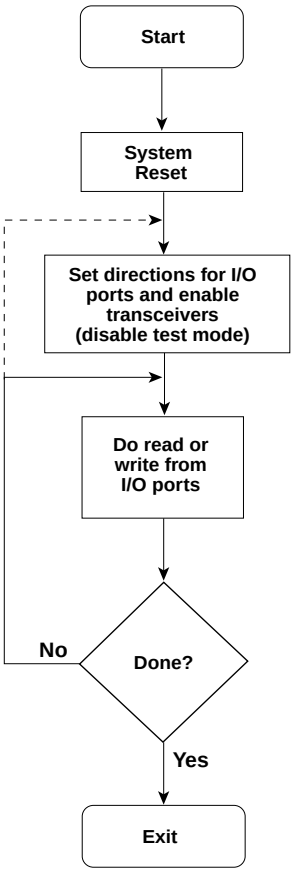


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## Built-in-Test

The Built-in-Test feature of this board lends itself to two basic modes of testing, off-line and on-line. The first, off-line, is characterized by the I/O ports being disabled from the field electronics such that on-board testing will not affect any external equipment. This off-line mode of test is initiated by setting CSRU to all ones and setting both Test Mode bits in CSRL to zero. The VMIVME-2510B has a separate test mode bit for each I/O connector. Setting a test mode bit to "0" allows for Data Register loopback testing whereby the programmer can write to a Data Register and read back the data for comparison. While a Test Mode (TM) bit is active, for an I/O connector, all testing will be transparent to the user equipment associated with that connector. A Test Programming Flowchart is shown in Figure 3-2 on page 43.

A second mode of test can be performed while the VMIVME-2510B is on-line, (TM=1). All ports that are output ports can be tested by performing a read from the corresponding Data Register. This "loopback" mode of test can be useful when the programmer requires an on-line "health test" of the board. Data loopback can only be performed on a register initialized as an output (i.e., the corresponding port direction bit is a one).

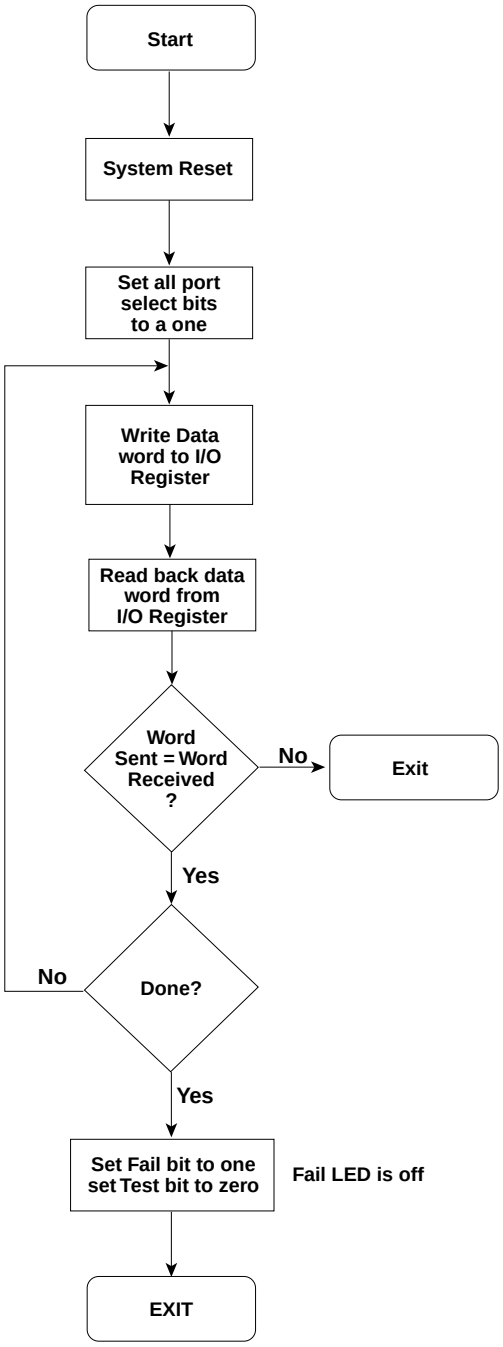



**NOTE:** At system reset, I/O transceivers are "TRI Stated" and the Fail LED is illuminated.

**Figure 3-1** Programming Flowchart (Built-in-Test)



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**NOTE:** At system reset, I/O transceivers are "TRI Stated" and the Fail LED is illuminated.

**Figure 3-2** Programming Flowchart (Built-in-Test Active)



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## I/O Data Registers

**Table 3-1** Data Register Address Map

| Relative Address* | Mnemonic | Name/Function | Port |
|---|---|---|---|
| $XXX0 | DR0 | Data Register 0 | 4 |
| $XXX1 | DR1 | Data Register 1 | 3 |
| $XXX2 | DR2 | Data Register 2 | 2 |
| $XXX3 | DR3 | Data Register 3 | 1 |
| $XXX4 | DR4 | Data Register 4 | 8 |
| $XXX5 | DR5 | Data Register 5 | 7 |
| $XXX6 | DR6 | Data Register 6 | 6 |
| $XXX7 | DR7 | Data Register 7 | 5 |

**NOTE:** * XXX of the address is determined by Data Register address select switches S3 and S1. See Figure 2-2 on page 37.

| $XXX0 DR0, Port 4 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 31** | **Bit 30** | **Bit 29** | **Bit 28** | **Bit 27** | **Bit 26** | **Bit 25** | **Bit 24** |
| I/O63 | I/O62 | I/O61 | I/O60 | I/O59 | I/O58 | I/O57 | I/O56 |

| $XXX1 DR1, Port 3 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 23** | **Bit 22** | **Bit 21** | **Bit 20** | **Bit 19** | **Bit 18** | **Bit 17** | **Bit 16** |
| I/O55 | I/O54 | I/O53 | I/O52 | I/O51 | I/O50 | I/O49 | I/O48 |

| $XXX2 DR2, Port 2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| I/O47 | I/O46 | I/O45 | I/O44 | I/O43 | I/O42 | I/O41 | I/O40 |

| $XXX3 DR3, Port 1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| I/O39 | I/O38 | I/O37 | I/O36 | I/O35 | I/O34 | I/O33 | I/O32 |

| $XXX4 DR4, Port 8 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 31** | **Bit 30** | **Bit 29** | **Bit 28** | **Bit 27** | **Bit 26** | **Bit 25** | **Bit 24** |
| I/O31 | I/O30 | I/O29 | I/O28 | I/O27 | I/O26 | I/O25 | I/O24 |



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## I/O Data Registers (Continued)

| $XXX5 DR5, Port 7 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 23** | **Bit 22** | **Bit 21** | **Bit 20** | **Bit 19** | **Bit 18** | **Bit 17** | **Bit 16** |
| I/O23 | I/O22 | I/O21 | I/O20 | I/O19 | I/O18 | I/O17 | I/O16 |

| $XXX6 DR6, Port 6 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| I/O15 | I/O14 | I/O13 | I/O12 | I/O11 | I/O10 | I/O09 | I/O08 |

| $XXX7 DR7, Port 5 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| I/O07 | I/O06 | I/O05 | I/O04 | I/O03 | I/O02 | I/O01 | I/O00 |



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## CSR Bit Definitions

**Table 3-2** CSR Address Map

| Relative Address* | Mnemonic | Name/Function |
|---|---|---|
| $YYY0 | CSRU | CSR Upper Byte |
| $YYY1 | CSRL | CSR Lower Byte |
| **NOTE:** * YYY of the CSR address is determined by CSR address select switches S4 and S2. See Figure 2-3 on page 37 | | |

| $YYY0 CSRU (Port Direction Control for Register DR0 Through DR7)*, Read/Write | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| Port 1 (DR3) | Port 2 (DR2) | Port 3 (DR1) | Port 1 (DR0) | Port (DR7) | Port (DR6) | Port (DR5) | Port (DR4) |
| **NOTE:** * If the port direction bit = 1, then the port is an output port. If the port direction bit = 0, then the port is an input port. | | | | | | | |

| $YYY1 CSRL (Test Mode and Fail LED Control) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| Test Mode P3 0 = Test Mode 1 = Normal | Fail LED 1 = Off 0 = On | Test Mode P4 0 = Test Mode 1 = Normal | User-Defined Storage | | | | |



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## Power-Up/System Reset

Upon power-up or when a system reset is performed, all bits will be cleared to zero in the CSR. Thus the VMIVME-2510B is in the test mode with the front panel LED illuminated and the output drivers are Tri-stated.



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# *Maintenance*

## Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com



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# Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.



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