ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Abaco Systems / VMIC VMIVME-2511-200* at our website: ***Click HERE***

VMIVME-2511

PROGRAMMABLE I/O BOARD

INSTRUCTION MANUAL

March 1990

DOCUMENT NO. 500-002511-000

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12021-N SOUTH MEMORIAL PARKWAY
HUNTSVILLE, AL 35803
(205) 880-0444

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, VMIC assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

VMIC reserves the right to make any changes, without notice, to this or any of VMIC's products to improve reliability, performance, function, or design.

VMIC does not assume any liability arising out of the application or use of any product or circuit described herein; nor does VMIC convey any license under its patent rights or the rights of others.

VME Microsystems International Corporation

All Rights Reserved

This document shall not be duplicated, nor its contents used for any purpose, unless granted express written permission from VMIC.

Copyright © January 1986 by
VME Microsystems International Corporation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIC

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	04/20/89	Release Manual and Appendix A	88-0313
B	03/22/90	Appendix A	90-0029

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THIS OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THE PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SAFETY SYMBOLS

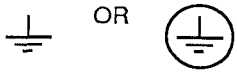
GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



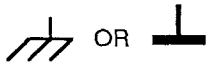
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



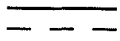
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-2511
PROGRAMMABLE I/O BOARD

TABLE OF CONTENTS

SECTION 1. INTRODUCTION PAGE

1.1 Introduction 1-1
1.2 Reference Material List 1-1

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

2.1 Physical Description 2-1
2.2 Functional Characteristics 2-1
2.3 Electrical Specifications 2-2
2.4 Physical Specifications 2-2
2.5 Ordering Information 2-3

SECTION 3. THEORY OF OPERATION

3.1 Block Diagrams 3-1
3.2 Operational Overview 3-1
3.3 I/O Data Transfer Description 3-1
3.4 Interrupt Capability 3-6
3.5 The 68230 Parallel Interface/Timer 3-6
3.6 Centronics Interface 3-6

SECTION 4. PROGRAMMING

4.1 Introduction 4-1
4.2 BIM and PI/T Register Map 4-1
4.3 Detailed Programming 4-11
4.3.1 Programming the MC68153 BIM 4-11
4.3.2 Programming the MC68230 PI/T. 4-12
4.3.3 Timer Programming 4-13
4.3.4 Interrupt Programming 4-13
4.3.5 Sample Programs 4-17

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 Unpacking Procedures 5-1
5.1.1 Switch and Jumper Locations 5-1
5.2 Physical Installation 5-1
5.3 Address Modifiers 5-1
5.4 Jumper Configuration and Detailed I/O Configuration 5-1
5.5 Address Selection Switches 5-7
5.6 I/O Cable and Card-Edge Connector Configuration 5-7

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 6. MAINTENANCE AND WARRANTY PAGE

6.1 Maintenance 6-1
6.2 Maintenance Prints 6-1
6.3 Warranty 6-1
6.4 Out-of-Warranty Repair Policy 6-2
6.4.1 Repair Category 6-3
6.4.2 Repair Pricing 6-3
6.4.3 Payment 6-3
6.4.4 Shipping Charges 6-3
6.4.5 Shipping Instructions. 6-3
6.4.6 Warranty on Repairs. 6-4
6.4.7 Exclusions 6-4

LIST OF FIGURES

FIGURE NO.

3-1 Functional Block Diagram 3-2
3-2 Address Decode Subsystem Detailed Block Diagram 3-3
3-3 Detailed Block Diagram of Parallel Interface/Time and I/O Port Control Logic 68230 #2 When Logic Is Identical. 3-4
3-4 VMEbus Interrupter Subsystem 3-5
4-1 Interrupt Programming Sequence 4-14
4-2 Port Interrupt Routine 4-15
4-3 Timer Interrupt Sequence 4-16
5-1 Switch and Jumper Locations 5-2
5-2 Detailed I/O Block Diagram 5-3
5-3 Address Select Switch, SW1 5-7
5-4 Cable Connector Configuration 5-8

LIST OF TABLES

TABLE NO.

4-1 BIM Register Map 4-2
4-2 PI/T #1 Register Map 4-3
4-3 PI/T #2 Register Map 4-7
4-4 PI/T I/O Channel Definition 4-13
5-1 Jumper Definition Table 5-4
5-2 P3-PI/T #1 Pin-Function Assignment 5-9
5-3 P4-P1/T #1 Pin-Function Assignment 5-10

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDICES

A	Parallel Interface/Timer (PI/T) MC68230 Specifications
B	Bus Interrupter Module (BIM) MC68153 Specifications
C	Parts List and Maintenance Drawings
D	Sample Program Listings
D1	Data Transfer Test
D2	BIM Test
D3	Loop Test
E	Centronics Parallel Interface
F	MC68230 Parallel Interface/Timer Provides an Effective Printer Interface

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 1
INTRODUCTION

1.1 INTRODUCTION

The VMIVME-2511 is a VMEbus compatible programmable I/O board. It utilizes two Motorola MC68230 Parallel Interface/Timer I.C.'s and one Motorola MC68153 Bus Interrupter Module and has the following features:

- 48 Bits of I/O (bit I/O, unidirectional 8-bit and 16-bit, bidirectional 8-bit and 16-bit)
- Interrupt generation logic allowing four interrupt sources. One timer interrupt and one port interrupt per MC68230
- Optional high current drivers with 64mA sink capability (optional)
- Two 24-bit programmable timers
- Software programmable timer modes
- Selectable handshake timer provides an interface flexible enough for connection to a wide variety of low, medium or high speed peripherals or other computer systems
- Centronics Parallel Interface

1.2 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

PRINTEX
Suite 228
P.O. Box #C-4200
Scottsdale, AZ 85261
(602) 998-0172

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The following application and configuration guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Analog I/O Products (with Built-In-Test) Configuration Guide	825-000000-005
Synchro/Resolver (Built-In-Test) Configuration Guide	825-000000-004
Change-of-State Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006
Low Level Analog I/O Configuration Guide	825-000000-001
Digital I/O (with Built-In-Test) Product Line Description	825-000000-003

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 2
PHYSICAL DESCRIPTION AND SPECIFICATIONS

2.1 PHYSICAL DESCRIPTION

The VMIVME-2511 Programmable I/O Board consists of VMEbus compatibility logic, interrupt control logic, and I/O control logic associated with the parallel interface/timer modules.

The VMEbus compatibility logic contains address decoding logic and data transfer control logic allowing VMEbus write and read data transfers.

Interrupt control logic which utilizes the Motorola MC68153 BIM allows port and timer interrupts from each parallel interface/timer. The interrupt requests to the CPU are issued by the MC68153 when requested to do so by the parallel interface/timer (68230).

The parallel I/O ports are programmable to allow unidirectional 8-bit ports, bidirectional 8-bit ports and bit I/O (each bits direction in a 8-bit port is programmable. A high current driver option is available. When the high current option is employed, the 8-bit ports are programmable for unidirectional only, either outputs or inputs.

2.2 FUNCTIONAL CHARACTERISTICS:

Compatibility:	VMEbus Specification Compatible Double-Height Form Factor
I/O Connector Type:	64-pin connector-DIN 41612
I/O Organization:	The 2511 board utilizes two Motorola MC68230 Parallel Interface/Timers that provide a wide variety of programmable I/O features including bit I/O, unidirectional 8-bit and 16-bit I/O, bi-directional 8-bit and 16-bit I/O, selectable handshaking options and a 24-bit programmable timer. The 2511 may be ordered with a buffered I/O option that provides up to 64mA sink capability; however, the bi-directional modes are not supported with this option. In addition, if the bit I/O mode is chosen, all Port A data bits must be programmed in the same direction.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Addressing Scheme: One eight position DIP switch provides the board address. The 2511 is configured at the factory to respond to short supervisory I/O access; however, the user may change the jumper to enable short non-privileged I/O access.

Data Polarity: Order as high-true or low-true

2.3 ELECTRICAL SPECIFICATIONS

A. Without I/O Buffers
Output High Voltage (VOH=2.4min.)

ILOAD = -150µA, VCC=min	H2, H4, PBØ-PB7, PRØ-PA7
ILOAD = -100µA, VCC=min	PCØ-PC7

Output Low Voltage (VOL = 0.5max)

ILOAD = 8.8mA, VCC=min	PC3/Tout, PC5/PIRQ
ILOAD = 2.4mA, VCC=min	PAØ-PA7, PBØ-PB7, H2, H4 PCØ-PC2, PC4, PC6, PC7

B. With I/O Buffers (5.25V ≤ VCC ≥ 4.75V)

VIH = 2Vmin
VIL = Ø.8V mux
IOH = -15mA
IOL = 64mA

2.4 PHYSICAL SPECIFICATIONS

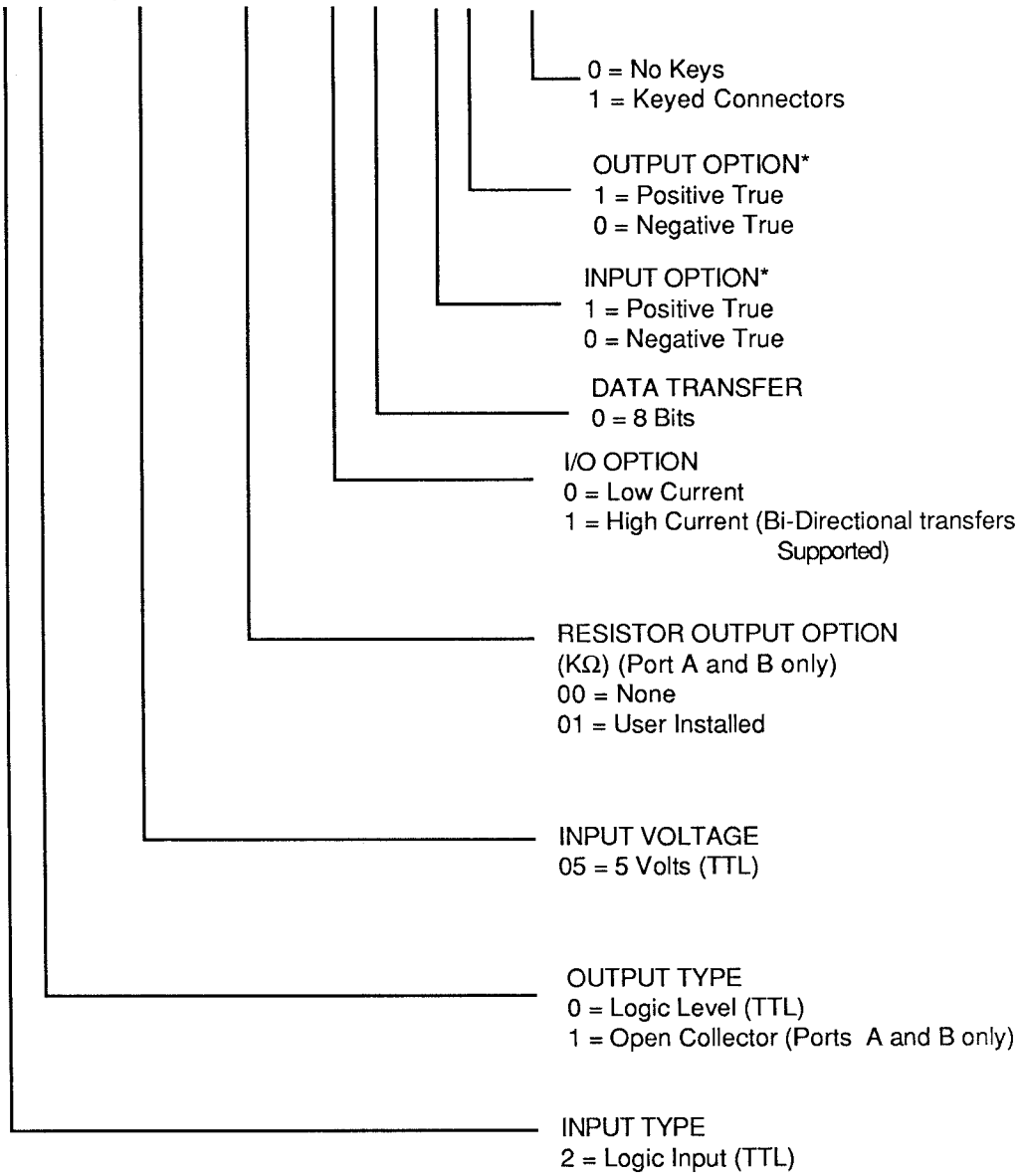
Environmental:

Temperature Range:	0° to 55°C, Operating -20° to 85°C, Storage
Relative Humidity Range:	20% to 80%, non-condensing
Cooling:	Convection
Power Requirements:	+5V at 2.5 Amps (max)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.3 ORDERING INFORMATION

VMIVME-2511 - A B - C D - E F - G H - I J - K



*Input and Output polarity options must be the same

CONNECTOR DATA

COMPATIBLE CONNECTOR	PANDUIT No. 120-964-455E
STRAIN RELIEF	PANDUIT No. 100-000-032
P.C. BOARD CONNECTOR	PANDUIT No. 120-964-053A

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 3
THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

The VMIVME-2511 consists of 10 major subsystems as illustrated in Figure 3-1. Each subsystem is further broken down into detailed block diagrams as shown in Figures 3-2 through 3-4.

3.2 OPERATIONAL OVERVIEW

As noted in the functional block diagram in Figure 3-1, the VMIVME-2511 utilizes two MC68230 modules. Each MC68230 Parallel Interface/Timer module (PI/T) has 3 I/O ports and some additional handshake interface. The handshake signals and the I/O ports of each module are in turn mapped into a single I/O connector. The module which is associated with the P3 connector will be referred to in the discussion which follows as PI/T #1. The module which is associated with the P4 connector will be referred to as PI/T #2.

To perform I/O data transfers with the VMIVME-2511, registers on board the two PI/T modules are selected for either input or output data transfers depending on which connector, P3 or P4, is to be accessed.

To achieve interrupt processing with the VMIVME-2511, the chosen PI/T module is programmed for port or timer interrupts. Then the proper channel in the 68153 Bus Interrupter Module (BIM) is enabled allowing the particular interrupt source of interest to be acknowledged by the system processor. Some jumper selection is required due to the port channels of the PI/T modules which can serve as I/O channels or interrupt request or acknowledge signals when the buffer option signal direction is also jumpered.

3.3 I/O DATA TRANSFER DESCRIPTION

The VMIVME-2511 performs I/O transfers via connectors P3 and P4 which are accessible from the front of the card. The I/O transfers are achieved through port registers on board the desired PI/T module. With the optional buffers, the I/O operation of the VMIVME-2511 is a subset of that of the PI/T module when optional output buffers are used. This is the case due to the octal transceivers used for buffering data to and from each of the I/O ports of the PI/T. Although this scheme limits the PI/T in I/O programmability, it greatly enhances the PI/T operation with greater drive capability than would be the case if buffering were not used. Limitations on programming the PI/T module are discussed in the programming section.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

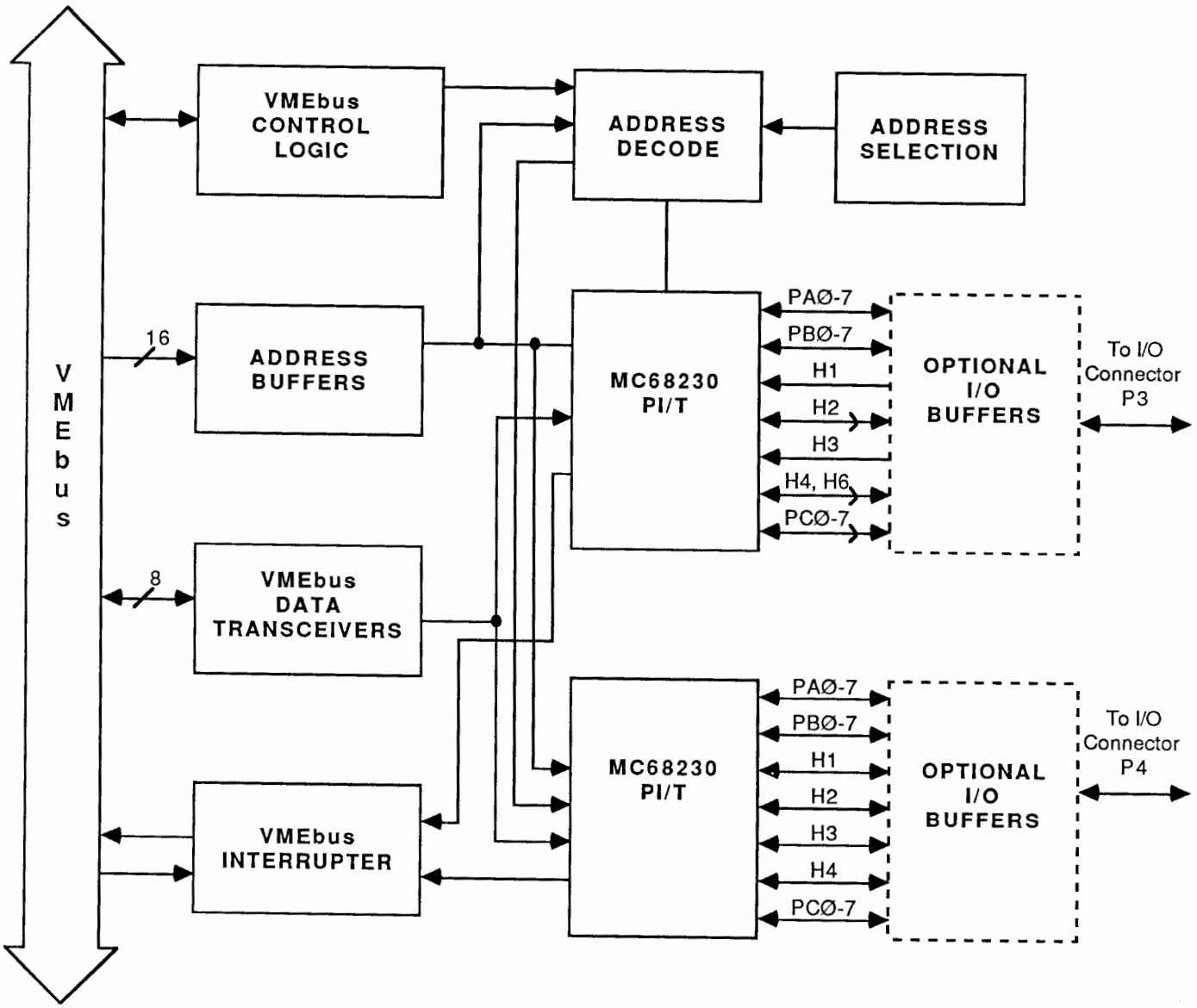


FIGURE 3-1. FUNCTIONAL BLOCK DIAGRAM

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

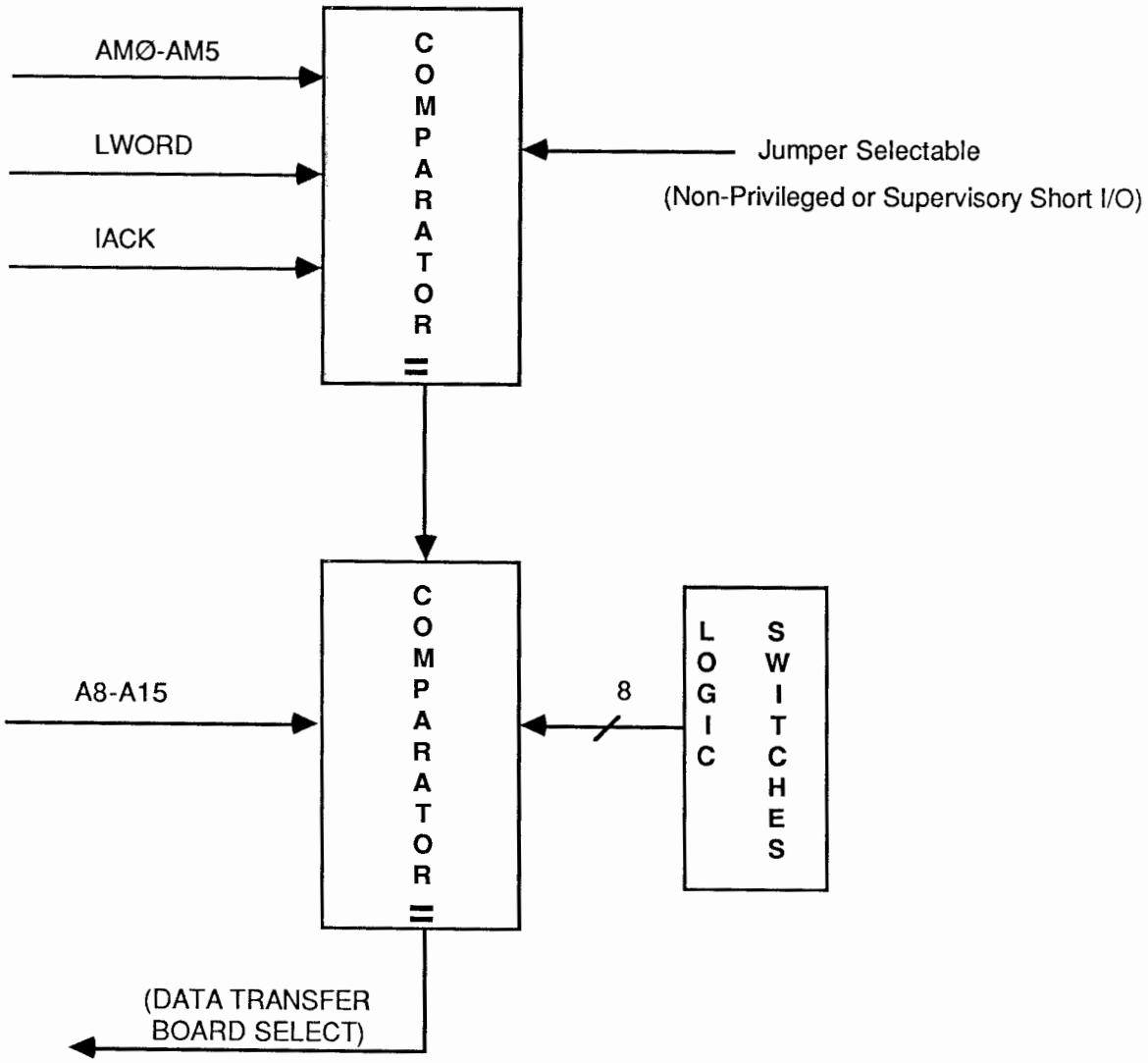


FIGURE 3-2. VMIVME-2511 ADDRESS DECODE SUBSYSTEM
DETAILED BLOCK DIAGRAM

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

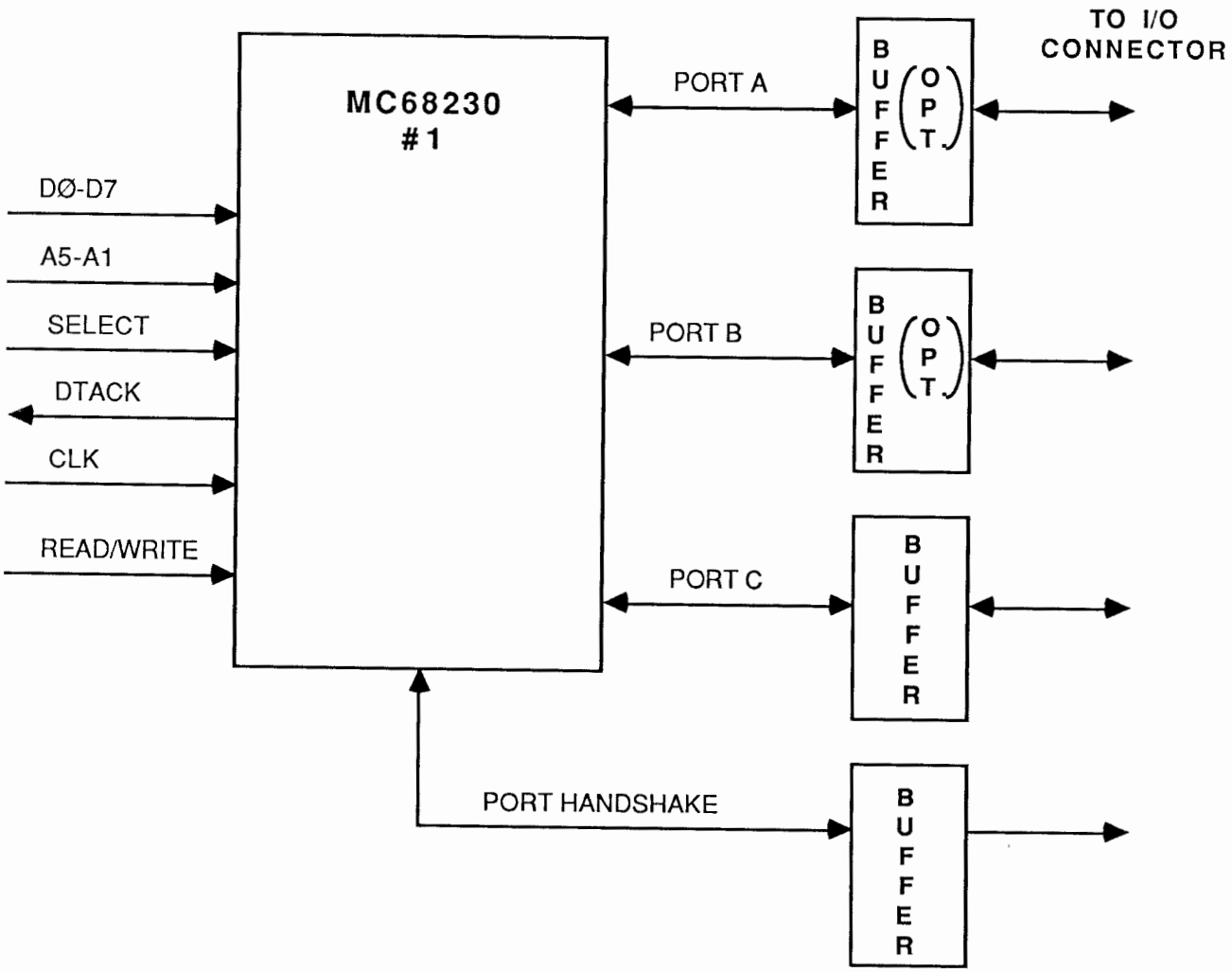


FIGURE 3-3. DETAILED BLOCK DIAGRAM OF PARALLEL INTERFACE/TIME AND I/O PORT CONTROL LOGIC 68230 #2 WHEN LOGIC IS IDENTICAL

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

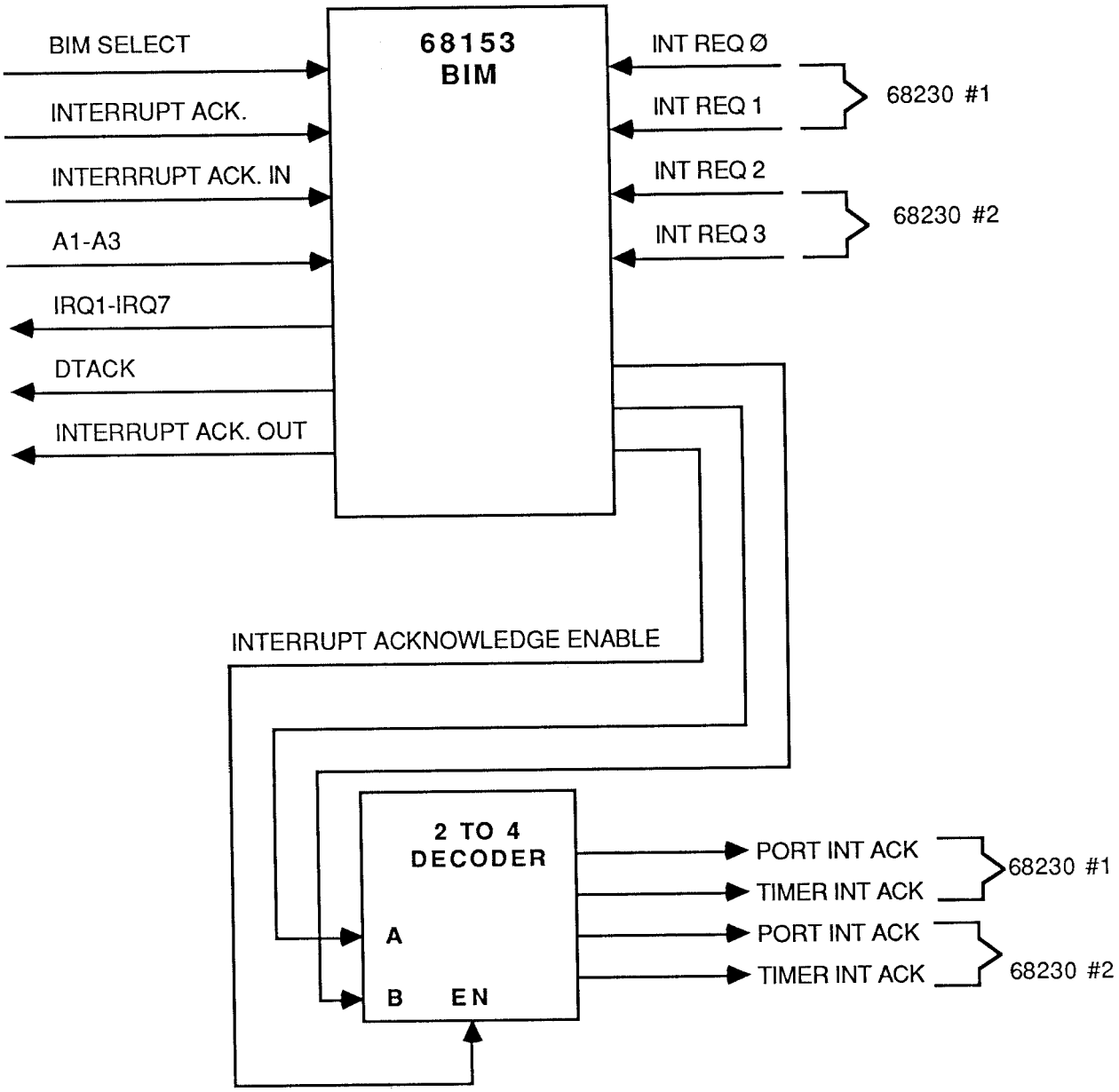


FIGURE 3-4. VMIVME-2511 VMEBUS INTERRUPTER SUBSYSTEM

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.4 INTERRUPT CAPABILITY

The VMIVME-2511 is capable of handling four interrupt requests. Each PI/T module is capable of two requests, a port interrupt request and a timer interrupt request. The four interrupt request signals (two from PI/T #1, and two from PI/T #2) are connected to the 68153 BIM, giving full interrupt support for both PI/T modules. Each PI/T module has two on-board interrupt vector registers programmable by the user. Programming concerning interrupts for the BIM and PI/T module are found in the programming section that follows.

3.5 THE 68230 PARALLEL INTERFACE/TIMER

The 68230 Parallel Interface and Timer provides for a versatile parallel I/O interface to a wide variety of peripheral and computer systems. Each 8-bit port is double buffered and each port (Port A and B) has two handshake lines to provide for orderly transfer of data to and from the 68230. See Appendix A, pages 12, 13, and 14 for the port control structure, handshaking definition and I/O interface timing diagrams. Port C of each 68230 may be used as six general purpose I/O lines (CØ, C1, C4-C7) with C2 and C3 used as the timer clock input and timer output, respectively. Alternatively, port C (C4-C7) may be programmed to support the 68230's interrupt structure. C2 and C3 remain the timer input/output pins, and CØ and C1 are general purpose I/O.

The 68230 may indicate a need for service in two ways. The processor may poll the Port Status Register to indicate the state of the handshake pins. The 68230 may be programmed for interrupts. The interrupts may occur on a transition of any of the two handshake pins, H1 and H2 for port A, H3 and H4 for Port B. This is further explained on page 15 of Appendix A.

3.6 CENTRONICS INTERFACE

A simple example of a centronic interface is provided in Appendix E. An interconnection scheme is shown with a detailed timing diagram.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 4
PROGRAMMING

4.1 INTRODUCTION

As stated in Section 3.2, the operation of the PI/T module can be limited due to octal buffers being used to drive port data to the P3 and P4 connectors. This limitation restricts the use of some port modes, such as bi-directional data transfer. Before reading the next section the reader should have an understanding of the Programmers Model section of the MC68230 data specifications in the appendices of this manual. The user will also want to read Section 5.2 such that the programming is consistent with the jumper configuration of the I/O ports before powering the VMIVME-2511. For programming concerning interrupts, the reader should have an understanding of the BIM which is referenced in the appendices to supplement the BIM programming description which follows.

4.2 BIM AND PI/T REGISTER MAP

The MC68153 BIM contains eight 8-bit registers while the PI/T modules each contain 32 eight-bit registers of which only 25 are used. All registers are addressed on odd-byte locations. The BIM register map is shown in Table 4-1.

The VMIVME-2511 is factory configured to respond to Short Supervisory I/O Access, but can be configured to respond to Short Non-Privileged I/O Access by installing a jumper, see Section 5.1. Of the 15 address bits A1-A15, only eight (A15-A8) are decoded for board select. See Section 5.3 for address selection switches. The PI/T #1 register map is shown in Table 4-2 (4 pages). The PI/T #2 register map is shown in Table 4-3 (4 pages).

The eight 8-bit registers on board the MC68153 BIM are accessed as odd byte locations. The bit definition of each register can be found in the MC68153 BIM specifications in the appendices.

The 32 eight-bit registers on board each MC68230 PI/T modules are accessed as odd-byte locations. The bit definition of each register can be found in the MC68230 PI/T specifications in the appendices.

PI/T #1 (P3 CONNECTOR) BYTE ADDRESS LOCATIONS

Binary Address

A15 A8	A7 AØ	
X X X X X X X X	0 1 0 0 0 0 0 1	Port General Control Register
Base Switch Switch Selectable	Individual Register Addresses	↕
X X X X X X X X	0 1 1 1 1 1 1 1	Timer Status Register

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-1. BIM REGISTER MAP

HEX ADDRESS		BINARY ADDRESS														
A15	A8	A7	A6	A5	A4	A3	A2	A1	AØ							
										CONTROL REGISTER Ø						
X	X	Ø	Ø	X	X	Ø	Ø	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	LØ
										CONTROL REGISTER 1						
X	X	Ø	Ø	X	X	Ø	Ø	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	LØ
										CONTROL REGISTER 2						
X	X	Ø	Ø	X	X	Ø	1	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	LØ
										CONTROL REGISTER 3						
X	X	Ø	Ø	X	X	Ø	1	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	LØ
										VECTOR REGISTER Ø						
X	X	Ø	Ø	X	X	1	Ø	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										V7	V6	V5	V4	V3	V2	V1	VØ
										VECTOR REGISTER 1						
X	X	Ø	Ø	X	X	1	Ø	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										V7	V6	V5	V4	V3	V2	V1	VØ
										VECTOR REGISTER 2						
X	X	Ø	Ø	X	X	1	1	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										V7	V6	V5	V4	V3	V2	V1	VØ
										VECTOR REGISTER 3						
X	X	Ø	Ø	X	X	1	1	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										V7	V6	V5	V4	V3	V2	V1	VØ

X Represents user switch selectable positions. See DIP Switch Selection Switches for address selection.

F - Flag Bit

FAC- Flag Auto Clear

X/$\overline{IN}$ - External/$\overline{Internal}$ (Vector Source)

IRE - Interrupt Enable

IRAC - Interrupt Auto-Clear

L2, L1, LØ - Interrupt Level

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-2. PI/T #1 REGISTER MAP

HEX ADDRESS		BINARY ADDRESS															
A15	A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X	X	Ø	1	Ø	Ø	Ø	Ø	Ø	1	PORT GENERAL CONTROL REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										PORT MODE CONTROL		H34 ENABLE	H12 ENABLE	H 4 ENABLE	H 3 ENABLE	H2 ENABLE	H1 ENABLE
X	X	Ø	1	Ø	Ø	Ø	Ø	1	1	PORT SERVICE REQUEST REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										*	SVCRQ SELECT		INTERRUPT PFS		PORT INTERRUPT PRIORITY CONTROL		
X	X	Ø	1	Ø	Ø	Ø	1	Ø	1	PORT A DATA DIRECTION REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X	X	Ø	1	Ø	Ø	Ø	1	1	1	PORT B DATA DIRECTION REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X	X	Ø	1	Ø	Ø	1	Ø	Ø	1	PORT C DATA DIRECTION REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X	X	Ø	1	Ø	Ø	1	Ø	1	1	PORT INTERRUPT VECTOR REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										INTERRUPT VECTOR NUMBER						*	*
X	X	Ø	1	Ø	Ø	1	1	Ø	1	PORT A CONTROL REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										PORT A SUBMODE		H2 CONTROL			H2 INT. ENABLE	H1 SVCRQ	H1 STCTL
X	X	Ø	1	Ø	Ø	1	1	1	1	PORT B CONTROL REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										PORT B SUBMODE		H4 CONTROL			H4 INT. ENABLE	H3 SVCRQ	H3 STCTL

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

NOTE: See MC68230 Specifications for Port Control Register Information.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-2 (CONT'D). PI/T #1 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
									PORT A DATA REGISTER							
X X	Ø	1	Ø	1	Ø	Ø	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
									PORT B DATA REGISTER							
X X	Ø	1	Ø	1	Ø	Ø	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
									PORT A ALTERNATE REGISTER							
X X	Ø	1	Ø	1	Ø	1	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
									PORT B ALTERNATE REGISTER							
X X	Ø	1	Ø	1	Ø	1	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
									PORT C DATA REGISTER							
X X	Ø	1	Ø	1	1	Ø	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
									PORT STATUS REGISTER							
X X	Ø	1	Ø	1	1	Ø	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									H4 LEVEL	H3 LEVEL	H2 LEVEL	H1 LEVEL	H4S	H3S	H2S	H1S
									NOT USED							
X X	Ø	1	Ø	1	1	1	Ø	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									NOT USED							
X X	Ø	1	Ø	1	1	1	1	1	IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-2 (CONT'D). PI/T #1 REGISTER MAP

HEX ADDRESS		BINARY ADDRESS															
A15	A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X	X	Ø	1	1	Ø	Ø	Ø	Ø	1	TIMER CONTROL REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										TOUT/TIACK CONTROL			ZD CTRL	*	CLOCK CONTROL		TIMER ENABLE
X	X	Ø	1	1	Ø	Ø	Ø	1	1	TIMER INTERRUPT VECTOR REGISTER							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X	X	Ø	1	1	Ø	Ø	1	Ø	1	NOT USED							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X	X	Ø	1	1	Ø	Ø	1	1	1	COUNTER PRELOAD REGISTER (HI)							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 23	BIT 22	BIT 21	BIT 2Ø	BIT 19	BIT 18	BIT 17	BIT 16
X	X	Ø	1	1	Ø	1	Ø	Ø	1	COUNTER PRELOAD REGISTER (MID)							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 1Ø	BIT Ø9	BIT Ø8
X	X	Ø	1	1	Ø	1	Ø	1	1	COUNTER PRELOAD REGISTER (LOW)							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT Ø7	BIT Ø6	BIT Ø5	BIT Ø4	BIT Ø3	BIT Ø2	BIT Ø1	BIT Ø
X	X	Ø	1	1	Ø	1	1	Ø	1	NOT USED							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X	X	Ø	1	1	Ø	1	1	1	1	COUNTER REGISTER (HIGH)							
										IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
										BIT 23	BIT 22	BIT 21	BIT 2Ø	BIT 19	BIT 18	BIT 17	BIT 16

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-2 (CONT'D). PI/T #1 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X X	Ø	1	1	1	Ø	Ø	Ø	1	COUNTER REGISTER (MID)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 1Ø	BIT Ø9	BIT Ø8
X X	Ø	1	1	1	Ø	Ø	1	1	COUNTER REGISTER (LOW)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT Ø7	BIT Ø6	BIT Ø5	BIT Ø4	BIT Ø3	BIT Ø2	BIT Ø1	BIT Ø
X X	Ø	1	1	1	Ø	1	Ø	1	TIMER STATUS REGISTER							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									*	*	*	*	*	*	*	ZDS
X X	Ø	1	1	1	Ø	1	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	Ø	1	1	1	1	Ø	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	Ø	1	1	1	1	Ø	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	Ø	1	1	1	1	1	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	Ø	1	1	1	1	1	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-3. PI/T #2 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X X	1	Ø	Ø	Ø	Ø	Ø	Ø	1	**PORT GENERAL CONTROL REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									PORT MODE CONTROL		H34 ENABLE	H12 ENABLE	H 4 ENABLE	H 3 ENABLE	H2 ENABLE	H1 ENABLE
X X	1	Ø	Ø	Ø	Ø	Ø	1	1	**PORT SERVICE REQEST REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									*	SVCRQ SELECT		INTERRUPT PFS		PORT INTERRUPT PRIORITY CONTROL		
X X	1	Ø	Ø	Ø	Ø	1	Ø	1	**PORT A DATA DIRECTION REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	Ø	Ø	1	1	1	**PORT B DATA DIRECTION REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	Ø	1	Ø	Ø	1	**PORT C DATA DIRECTION REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	Ø	1	Ø	1	1	**PORT INTERRUPT VECTOR REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									INTERRUPT VECTOR NUMBER						*	*
X X	1	Ø	Ø	Ø	1	1	Ø	1	**PORT A CONTROL REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									PORT A SUBMODE		H2 CONTROL			H2 INT. ENABLE	H1 SVCRQ	H1 STCTL
X X	1	Ø	Ø	Ø	1	1	1	1	**PORT B CONTROL REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									PORT B SUBMODE		H4 CONTROL			H4 INT. ENABLE	H3 SVCRQ	H3 STCTL

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-3 (CONT'D). PI/T #2 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X X	1	Ø	Ø	1	Ø	Ø	Ø	1	**PORT A DATA REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	1	Ø	Ø	1	1	**PORT B DATA REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	1	Ø	1	Ø	1	**PORT A ALTERNATE REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	1	Ø	1	1	1	**PORT B ALTERNATE REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	1	1	Ø	Ø	1	**PORT C DATA REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	Ø	1	1	Ø	1	1	**PORT STATUS REGISTER**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									H4 LEVEL	H3 LEVEL	H2 LEVEL	H1 LEVEL	H4S	H3S	H2S	H1S
X X	1	Ø	Ø	1	1	1	Ø	1	**NOT USED**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	Ø	1	1	1	1	1	**NOT USED**							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-3 (CONT'D). PI/T #2 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X X	1	Ø	1	Ø	Ø	Ø	Ø	1	TIMER CONTROL REGISTER							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									TOUT/TIACK CONTROL			ZD CTRL	*	CLOCK CONTROL		TIMER ENABLE
X X	1	Ø	1	Ø	Ø	Ø	1	1	TIMER INTERRUPT VECTOR REGISTER							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
X X	1	Ø	1	Ø	Ø	1	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	Ø	Ø	1	1	1	COUNTER PRELOAD REGISTER (HI)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 23	BIT 22	BIT 21	BIT 2Ø	BIT 19	BIT 18	BIT 17	BIT 16
X X	1	Ø	1	Ø	1	Ø	Ø	1	COUNTER PRELOAD REGISTER (MID)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 1Ø	BIT Ø9	BIT Ø8
X X	1	Ø	1	Ø	1	Ø	1	1	COUNTER PRELOAD REGISTER (LOW)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT Ø7	BIT Ø6	BIT Ø5	BIT Ø4	BIT Ø3	BIT Ø2	BIT Ø1	BIT Ø
X X	1	Ø	1	Ø	1	1	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	Ø	1	1	1	1	COUNTER REGISTER (HIGH)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 23	BIT 22	BIT 21	BIT 2Ø	BIT 19	BIT 18	BIT 17	BIT 16

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-3 (CONT'D). PI/T #2 REGISTER MAP

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	AØ								
X X	1	Ø	1	1	Ø	Ø	Ø	1	COUNTER REGISTER (MID)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 1Ø	BIT Ø9	BIT Ø8
X X	1	Ø	1	1	Ø	Ø	1	1	COUNTER REGISTER (LOW)							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									BIT Ø7	BIT Ø6	BIT Ø5	BIT Ø4	BIT Ø3	BIT Ø2	BIT Ø1	BIT Ø
X X	1	Ø	1	1	Ø	1	Ø	1	TIMER STATUS REGISTER							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
									*	*	*	*	*	*	*	ZDS
X X	1	Ø	1	1	Ø	1	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	1	1	Ø	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	1	1	Ø	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	1	1	1	Ø	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø
X X	1	Ø	1	1	1	1	1	1	NOT USED							
									IDB Ø7	IDB Ø6	IDB Ø5	IDB Ø4	IDB Ø3	IDB Ø2	IDB Ø1	IDB Ø

* Unused, read as zero.

XX Represents user selectable positions. See DIP Switch Selection Switches for address selection.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

HEX ADDRESS

$XX41 through $XX7F for PI/T #1

PI/T #2 (P4 CONNECTOR) BYTE ADDRESS LOCATIONS

Binary Address

A15 A8	A7 A0	
X X X X X X X X	1 0 0 0 0 0 0 1	Port General Contrd Register
Base Address Switch Selectable	Individual Register Address	
X X X X X X X X	1 0 1 1 1 1 1 1	Timer Status Register

HEX ADDRESS

$XX81 through $XXBF for PI/T #2

Total Address Space of VMIVME-2511

Hex address $XX01 through $XXBF

4.3 DETAILED PROGRAMMING

4.3.1 PROGRAMMING THE MC68153 BIM

The vector registers on-board the BIM are not used since the PI/T modules supply their own interrupt vector. Therefore, the BIM must be programmed for external vectors. In addition, the interrupt auto-clear bit corresponding to each interrupt source must be set (high level), along with its associated interrupt enable bit. This will require the interrupt service routine to be used to set the interrupt enable bit each time an interrupt is processed.

The interrupt vector is supplied by the interrupting PI/T module during an interrupt acknowledge cycle. These vectors are supplied by the Port Interrupt Vector Register and by the Timer Interrupt Vector Register on board the PI/T module, depending on which interrupt source is being acknowledged.

The control registers on-board the BIM are associated with the PI/T interrupt channels as shown below.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

INTERRUPT CHANNEL	CONTROL REGISTER	INTERRUPT SOURCE
Ø	Ø	PI/T #1 PORT INTERRUPTS
1	1	PI/T #1 TIMER INTERRUPTS
2	2	PI/T #2 PORT INTERRUPTS
3	3	PI/T #2 TIMER INTERRUPTS

PI/T #1 (P3 CONNECTOR)
PI/T #2 (P4 CONNECTOR)

All control registers on the BIM are initialized upon a system reset from the system processor.

4.3.2 PROGRAMMING THE MC68230 PI/T

The port section of the MC68230 PI/T consists of three 8-bit ports and four associated handshake signals. The PI/T modules allow each bit in each 8-bit port to be either input or output, along with two of the handshake lines. The buffered VMIVME-2511 option allows only one direction within each 8-bit port, with the exception of the port designated as Port C. Therefore, the 8-bit and 16-bit bi-directional modes cannot be programmed on the buffered PI/T modules. In addition, if the bit I/O mode is chosen on the buffered PI/T, all Port A data direction register bits must be programmed for the same direction, as well as those for the Port B data direction register. Bit I/O mode and bi-direction mode may be used on the unbuffered option. The following table and block diagram will clarify these statements as well as define programming for the handshake lines and port C. The programming of the buffered PI/T has to be consistent with the diagram and jumper selection of the VMIVME-2511, otherwise damage to the VMIVME-2511 may result. See Section 5.2. The PI/T I/O channel definition is shown in Table 4-4.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 4-4. PI/T I/O CHANNEL DEFINITION

PI/T I/O CHANNEL DEFINITION (with I/O Buffer Option)	
(PAØ-PA7)	All eight bits input or output, depending on jumper configuration chosen.
(PBØ-PB7)	All eight bits input or output, depending on jumper configuration chosen.
(PC4-PC7)	All four bits input or output, depending on jumper configuration chosen.
H1	Input only
H2	Configured as input or output
H3	Input only
H4	Configured as input or output
PCØ	Configured as input or output
PC1	Configured as input or output
PC2/TIN	Input only
PC3/TOUT	Output only

4.3.3 TIMER PROGRAMMING

All timer modes available on the PI/T module can be utilized with the VMIVME-2511. Port C pins PC1/TIN and PC2/TOUT are specifically buffered as input and output, respectively, for use as timer input and timer output pins.

4.3.4 INTERRUPT PROGRAMMING

All interrupt programming modes available on the PI/T module can be utilized with the VMIVME-2511, provided that those port pins associated with interrupts are configured as such. See Section 5.2. Interrupts from the two PI/T modules on-board the VMIVME-2511 are generated by the MC68153 BIM. The programming of the BIM and PI/T modules concerning interrupts should follow the flowchart shown in Figure 4-1. The port interrupt service routine should follow the sequence in Figure 4-2. To program the timers for interrupts, see the flowchart in Figure 4-3.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

INITIALIZE FOR INTERRUPTS

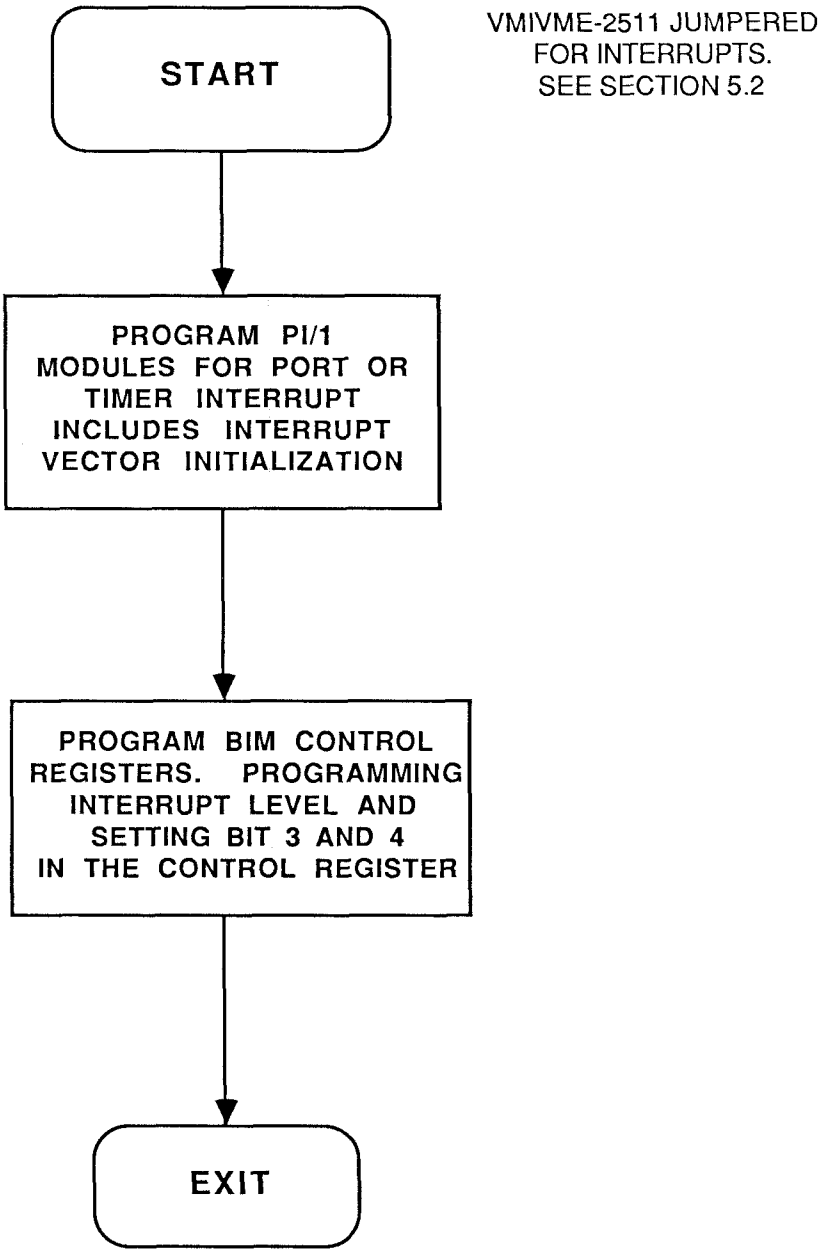


FIGURE 4-1. INTERRUPT PROGRAMMING SEQUENCE

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

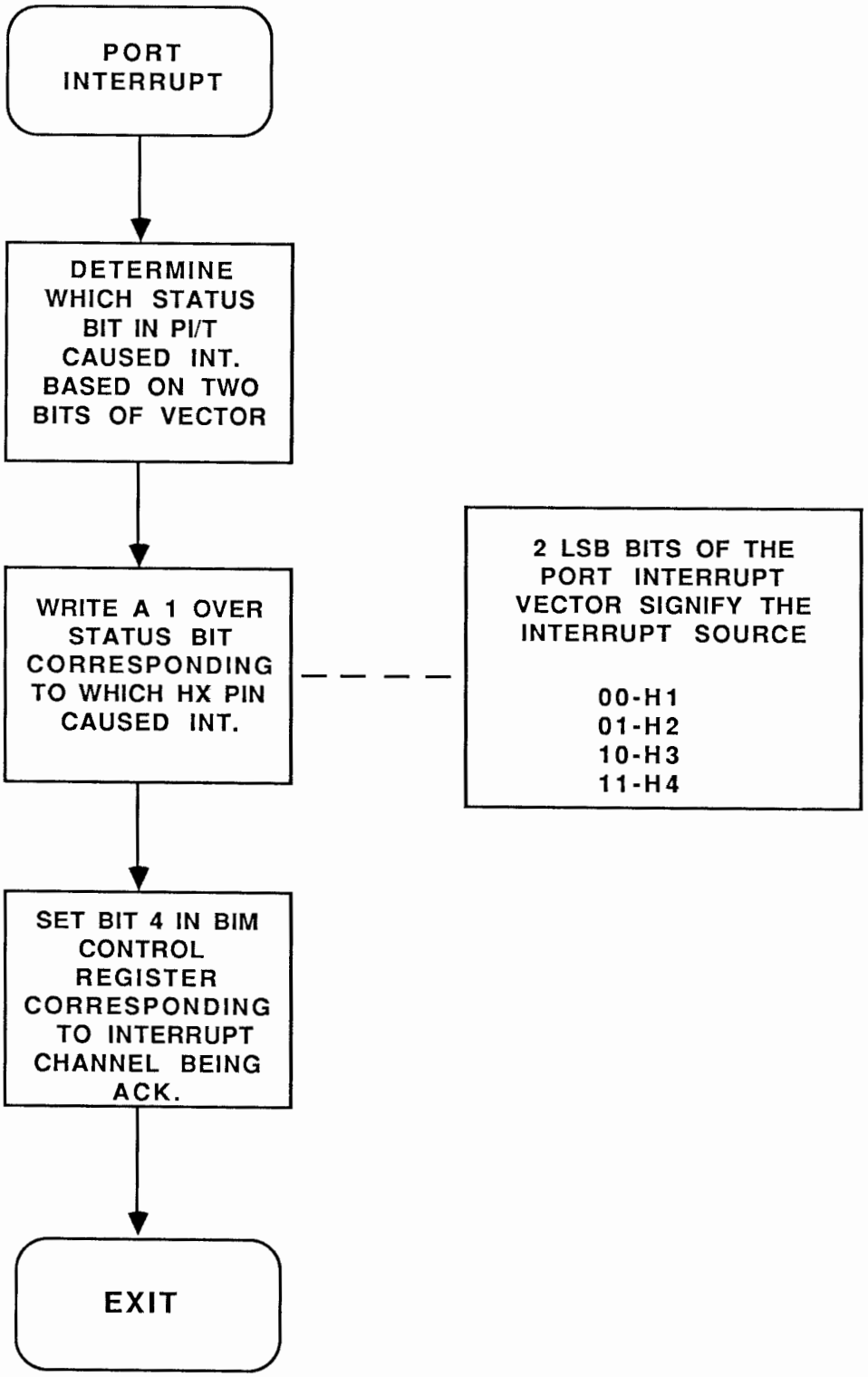


FIGURE 4-2. PORT INTERRUPT ROUTINE

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

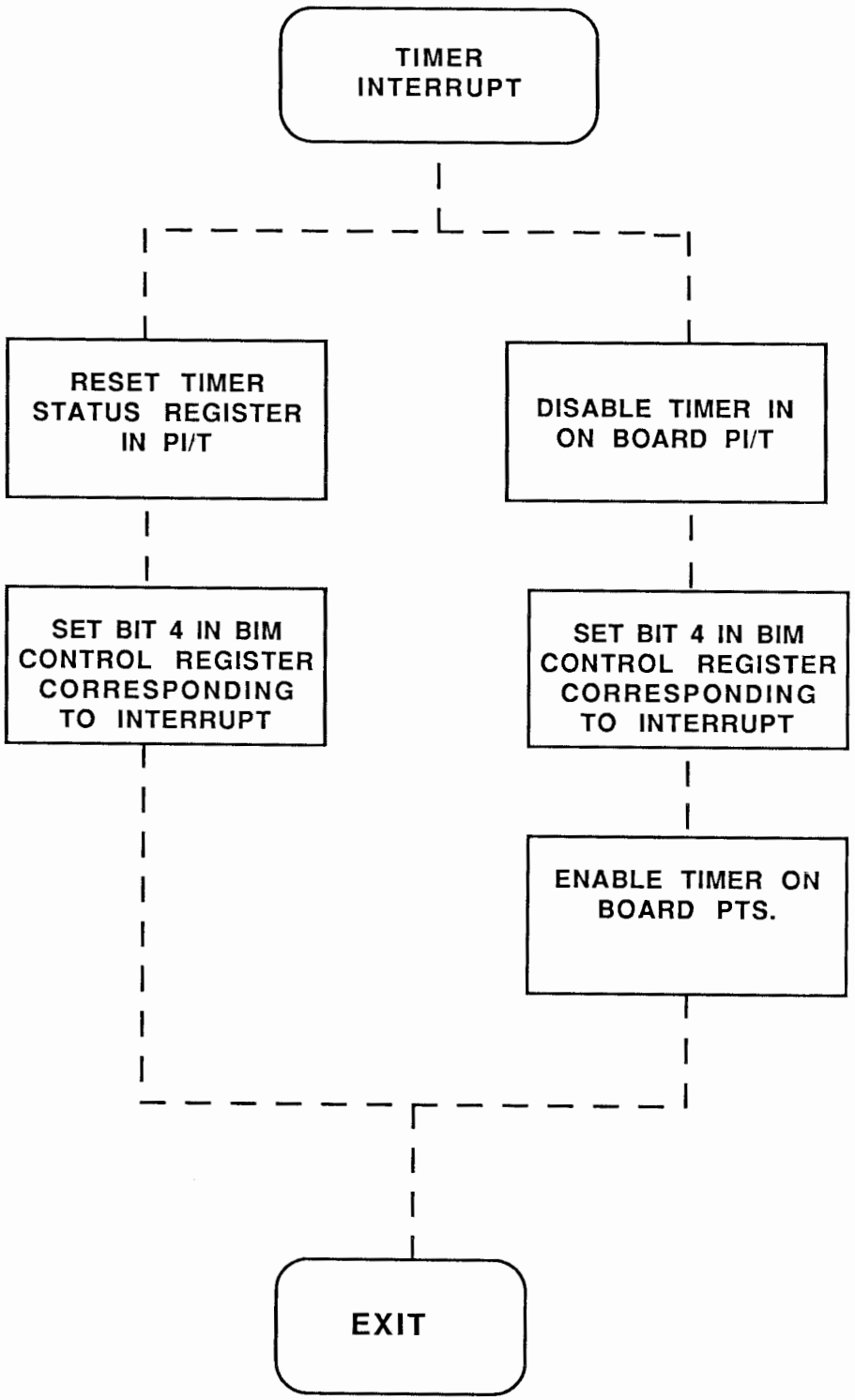


FIGURE 4-3. TIMER INTERRUPT SEQUENCE

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.3.5 SAMPLE PROGRAMS

Detailed sample program listings are provided in Appendix D to assist the user in programming this product. Appendix D1 provides a detailed listing of a test that transfers data from the P3 to P4 connector using the interlocked handshake mode. Appendix D2 provides a detailed listing of a test that verifies all interrupt levels of the 68153 BIM integrated circuit. Appendix D3 provides a detailed listing of a test that writes data to port A (P3 connector), interrupts on the H1 status handshake line, reads data in on Port A (P4) and stores data in memory.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 5
CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes as shipped. When the board is to be laid on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.1.1 SWITCH AND JUMPER LOCATIONS

Refer to Figure 5-1 for the locations of the switches and jumpers described in this section.

5.2 PHYSICAL INSTALLATION

CAUTION: Do not install or remove boards while power is applied.

Deenergize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated.

5.3 ADDRESS MODIFIERS

The VMIVME-2511 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper J9 to enable the board to respond to short non-privileged I/O access.

5.4 JUMPER CONFIGURATION AND DETAILED I/O CONFIGURATION

The following block diagrams show the detailed jumpering options available on the VMIVME-2511. The block diagrams reference P1/T #1. Jumper Definition Table 5-1 explains the function of each jumper in detail, in addition to defining some jumpers not shown in Figure 5-2.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

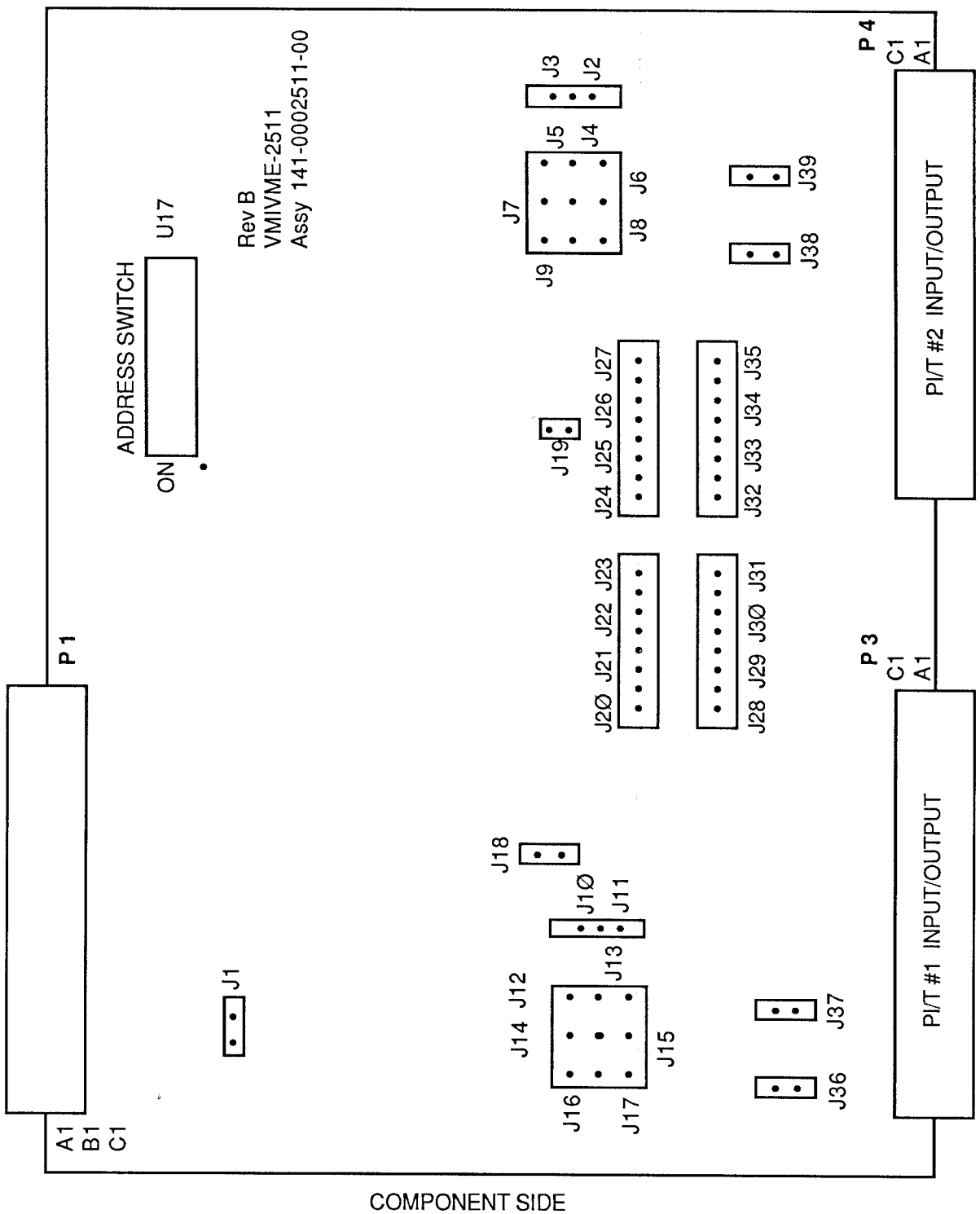


FIGURE 5-1. SWITCH AND JUMPER LOCATIONS

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

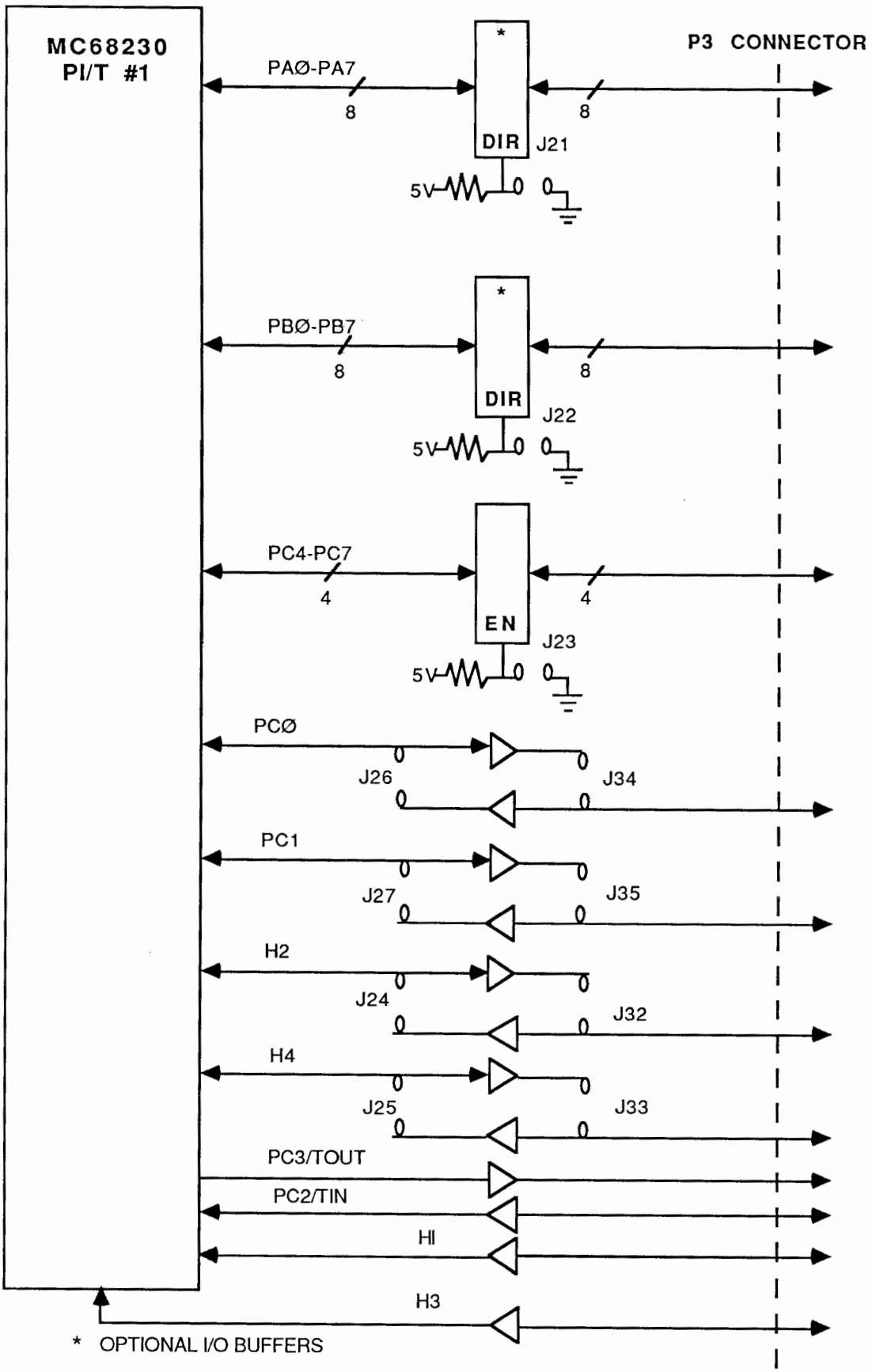


FIGURE 5-2. DETAILED I/O BLOCK DIAGRAM

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 5-1. JUMPER DEFINITION TABLE

JUMPER NUMBER		DEFINITION
J1		Install for Short Non-Privileged I/O Access; otherwise, VMIVME-2511 responds to Short Supervisory I/O Access.
J2	**	Install to Conn. PI/T #2 PC3 to the P4 Conn.
J3		Install to configure PI/T #2 PC3 pin for Timer Interrupt Request
J4	**	Install to connect PI/T #2 PC5 to P4 Conn.
J5		Install to configure PI/T #2 PC5 pin for Port Interrupt Requests
J6	**	Install to connect PI/T #2 PC6 to P4 Conn.
J7		Install to configure PI/T #2 PC6 for Port Interrupt Acknowledge
J8	**	Install to conn. PI/T #2 PC7 to P4 Conn.
J9		Install to configure PI/T #2 PC7 for timer Interrupt Acknowledge
J10	**	Install to configure PI/T #1 PC3 for Timer Interrupt Request
J11		Install to Conn. PI/T #1 PC3 to P3 Conn.
J12	**	Install to configure PI/T #1 PC5 for Port Interrupt. Requests
J13		Install to Conn. PI/T #1 PC5 to P3 Conn.
J14	**	Install to configure PI/T #1 PC6 for Port Interrupt Acknowledge
J15		Install to connect PI/T #1 PC6 to P3 Conn.
J16	**	Install to configure PI/T #1 PC7 for Timer Interrupt Acknowledge
J17		Install to conn. PI/T #1 PC7 to P3 Conn.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 5-1 (CONT'D). JUMPER DEFINIITON TABLE

JUMPER NUMBER		DEFINITION
J38*		Install to configure port pins PAØ-PA7 of PI/T #2 as an output port; otherwise, the port is an input port.
J39*		Install to configure port pins PBØ-PB7 of PI/T #2 as an output port; otherwise, it is input port.
J19		Install to configure port pins PC4-PC7 of PI/T #2 as an output port; otherwise, it is an input port
J36*		Install to configure port PAØ-PA7 of PI/T #1 as an output port; otherwise, the port is an input port.
J37*		Install to configure port PBØ-PB7 of PI/T #1 as an output port; otherwise, it is an input port.
J18		Install to configure port pin PC4-PC7 of PI/T #1 as an output port; otherwise, it is an input port
J20	**	Install to configure PI/T #1 H2 as an input.
J28		Install to configure PI/T #1 H2 as an output*.
J21	**	Install to configure H4 of PI/T #1 as an input.
J29		Install to configure H4 of PI/T #1 as an output.
J22	**	Install to configure PCØ of PI/T #1 as an input.
J30		Install to configure PCØ of PI/T #1 as an output.
J23	**	Install to configure PC1 of PI/T #1 as an input.
J31		Install to configure PC1 of PI/T #1 as an output.
J32	**	Install to configure PI/T #2 H2 as an output.
J24		Install to configure H2 of PI/T #2 as an input.
J33	**	Install to configure H4 of PI/T #2 as an output.
J25		Install to configure H4 of PI/T #2 as an input.
J34	**	Install to configure PCØ of PI/T #2 as an output.
J26		Install to configure PCØ of PI/T #2 as an input.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 5-1 (CONT'D) JUMPER DEFINITION TABLE

JUMPER NUMBER	DEFINITION
J35 **	Install to configure PC1 of PI/T #2 as an output.
J27 **	Install to configure PC1 of PI/T #2 as an input.

* NOTE 1: These four jumpers are used only on the buffered I/O Option.

** NOTE 2: Jumpers paired with brackets are mutually exclusive. If one of the jumper pairs is installed, the other jumper in the pair must not be installed or damage may result to the VMIVME-2511 or to field electronics connected to the VMIVME-2511.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

5.5 ADDRESS SELECTION SWITCHES

The VMIVME-2511 occupies 256 words of short I/O address space. The base address is selected by a single DIP switch, as shown in Figure 5-3.

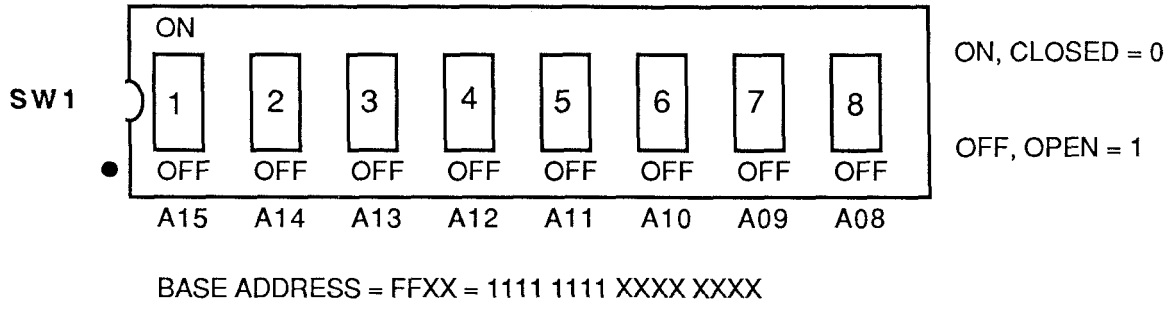


FIGURE 5-3. ADDRESS SELECT SWITCH, SW1

The example shown selects a base address of FFXX hexadecimal.

5.6 I/O CABLE AND CARD-EDGE CONNECTOR CONFIGURATION

The VMIVME-2511 is designed to receive contact inputs via two flat ribbon cables connected to connectors P3 and P4 as shown in Figure 5-4. Conductor #1 is shown at the bottom of the connector as it plugs into the header, due to pin #1 of P3 and P4 being mounted as shown.

Using a flat ribbon connector that has Row C as the end circuit, all of the odd numbered conductors of the cable are grounded due to Row C of P3 and P4 being connected to VMEbus ground. Therefore, all even numbered conductors of the cable are contact input signals coming into the VMIVME-2511. If a cable connector were used that has Row A as the end circuit, all odd numbered conductors would be signal conductors, while the even numbered conductors would be ground.

Tables 5-2 and 5-3 shows the P3 and P4 connector pin assignment for the 64 input channels of the VMIVME-2511. Cable conductor/signal assignment will depend on the type of cable connector chosen (Row A or Row C as end circuit).

A compatible cable connector for the VMIVME-2511 is Panduit #120-964-455E. Strain relief is Panduit #100-000-032. Header connector 15, Panduit #120-964-053A, is soldered to the P.C. Board.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

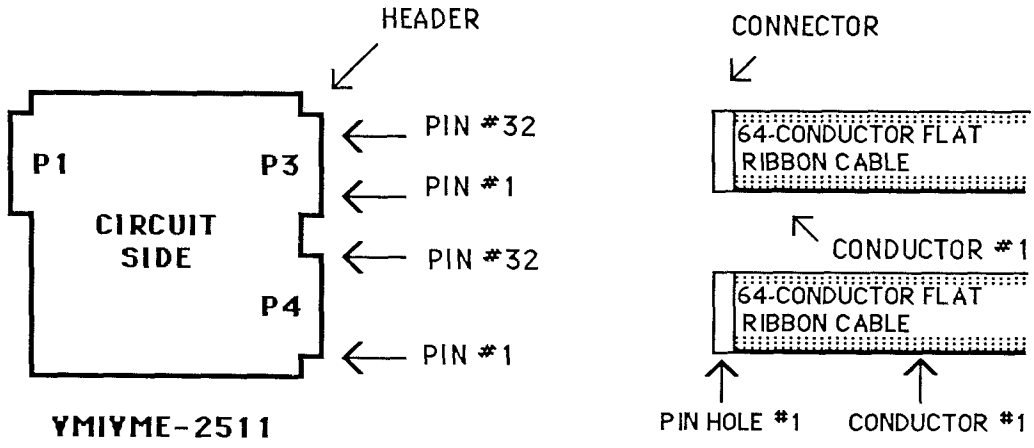


FIGURE 5-4. CABLE CONNECTOR CONFIGURATION

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 5-2. P3-PI/T#1 PIN-FUNCTION ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
32	PAO	16	PB6
31	PA1	15	PB7
30	PA2	14	H3
29	PA3	13	H4
28	PA4	12	PCØ
27	PA5	11	PC1
26	PA6	10	PC2
25	PA7	09	PC3
24	H1	08	PC4
23	H2	07	PC5
22	PBØ	06	PC6
21	PB1	05	PC7
20	PB2	04	N.C.
19	PB3	03	N.C.
18	PB4	02	N.C.
17	PB5	01	N.C.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE 5-3. P4-PI/T#1 PIN-FUNCTION ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
32	PAO	16	PB6
31	PA1	15	PB7
30	PA2	14	H3
29	PA3	13	H4
28	PA4	12	PCØ
27	PA5	11	PC1
26	PA6	10	PC2
25	PA7	09	PC3
24	H1	08	PC4
23	H2	07	PC5
22	PBØ	06	PC6
21	PB1	05	PC7
20	PB2	04	N.C.
19	PB3	03	N.C.
18	PB4	02	N.C.
17	PB5	01	N.C.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact factory for a Return Authorization Number.

6.2 MAINTENANCE PRINTS

Appendix A contains drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within one week after the customer's discovery of such defect.

In order to return the defective product or part at VMIC's expense, the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. After a Call Ticket Number has been obtained, the product or part

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

claimed to be defective may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product or part will be shipped back to the customer at the expense of VMIC.

The customer should be aware that the above process can sometimes take up to eight days for the shipment to reach VMIC. The customer has the option to ship the defective product or part at his own expense if he cannot afford this possible delay.

There shall be no warranty or liability for any VMIC products or parts which have been subject to accident, negligence, misuse by the customer, or modification by the customer without VMIC approval.

There shall also be no warranty or liability for any VMIC product or part damaged from customer's misapplication of electrical power, the insertion or removal of boards from backplanes and/or I/O connectors with power applied or board damage resulting from loss of electrical power.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in handling and shipping the returned product or part.

The warranty period of the replacement or repaired product or part shall terminate with the termination of the warranty period with respect to the original product or part for all replacement parts supplied or repairs made during the original warranty period.

Notwithstanding anything herein to the contrary, VMIC reserves the right to discharge its applicable warranty by refunding the purchase price and taking back the item or items sold to buyer hereunder.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY ITEM FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Board Exchange
b. Fixed Price Repair

Category 1 (board exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt if VMIC has the product in stock. Customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to boards returned to VMIC for repair and subsequent return to the customer.

6.4.2 Repair Pricing

Board exchange is 50% of the current list price. Fixed price repairs are performed at 25% of the current list price.

(Repair prices are subject to change without notice).

6.4.3 Payment Net 30 days.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's return authorization number assigned by VMIC's Quality Assurance Department.

6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repair, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the board depends on whether the board is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the board(s), using the same precautions listed in the "unpacking procedures" paragraph (Section 5, paragraph 5.1). The user should utilize the same (or equivalent) protective packaging container for reshipment as was provided by VMIC.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all boards that were repaired out of warranty. See standard condition of sale for boards repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to boards which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for board repair or replacement. The customer may then, at his option, choose to have the board repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX A

PARALLEL INTERFACE/TIMER (PI/T)
MC68230
SPECIFICATIONS

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD AUSTIN TEXAS 78721

MC68230L8
MC68230L10

Advance Information

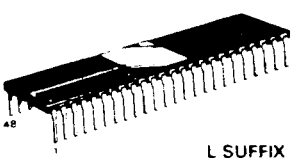
HMOS
(HIGH-DENSITY N-CHANNEL SILICON-GATE)

PARALLEL INTERFACE/TIMER

MC68230 PARALLEL INTERFACE/TIMER

The MC68230 Parallel Interface/Timer provides versatile double buffered parallel interfaces and an operating system oriented timer to MC68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA Request pin for connection to the MC68450 Direct Memory Access Controller or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also it can be used for elapsed time measurement or as a device watchdog.

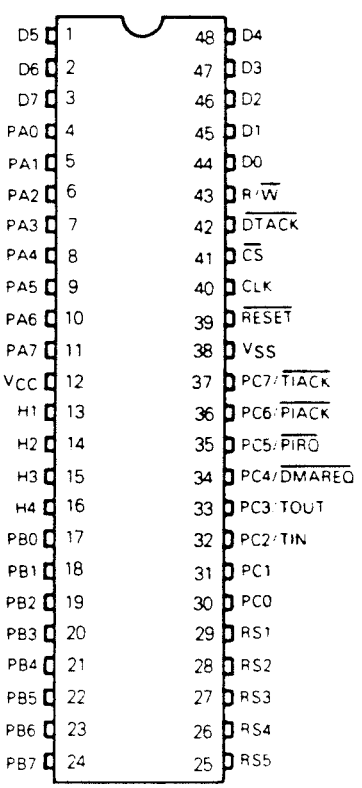
- MC68000 Bus Compatible
- Port Modes Include:
  - Bit I/O
  - Unidirectonal 8-Bit and 16-Bit
  - Bidirectional 8-Bit and 16-Bit
- Selectable Handshaking Options
- 24-Bit Programmable Timer
- Software Programmable Timer Modes
- Contains Interrupt Vector Generation Logic
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility



L SUFFIX
CERAMIC PACKAGE
CASE 740

P SUFFIX
PLASTIC PACKAGE
AVAILABLE 2Q82

PIN ASSIGNMENT



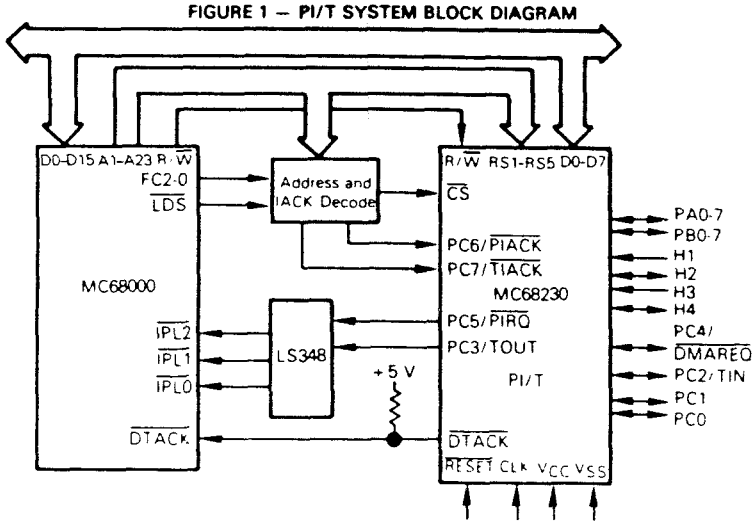
This document contains information on a new product. Specifications and information herein are subject to change without notice.

©MOTOROLA INC., 1981

ADI-860

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 1 — PI/T SYSTEM BLOCK DIAGRAM



POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K - (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance Ceramic	θ_{JA}	50	°C/W

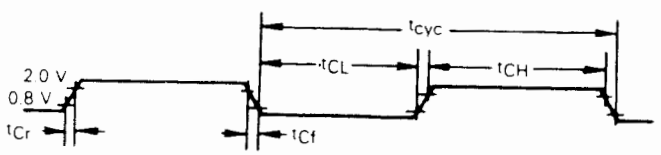
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, T_A = 0 to 70°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS} + 2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$	I_{in}	–	10.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{DTACK}$, PC0-PC7, D0-D7 H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	– −0.1	20 −1.0	μA mA
Output High Voltage (I_{Load} = −400 μA, V_{CC} = min) (I_{Load} = −150 μA, V_{CC} = min) (I_{Load} = −100 μA, V_{CC} = min)	$\overline{DTACK}$, D0-D7 H2, H4, PB0-PB7, PA0-PA7 PC0-PC7	V_{OH}	V_{SS} + 2.4	–	V
Output Low Voltage (I_{Load} = 8.8 mA, V_{CC} = min) (I_{Load} = 5.3 mA, V_{CC} = min) (I_{Load} = 2.4 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$ D0-D7, $\overline{DTACK}$ PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	–	0.5	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	500	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	–	15	pF

CLOCK TIMING (See Figure 2)

Characteristic	Symbol	8 MHz MC68230L8		10 MHz MC68230L10		Unit
		Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	ns
Clock Pulse Width	t_{CL} t_{CH}	55 55	250 250	45 45	250 250	ns
Clock Rise and Fall Times	t_{Cr} t_{Cf}	– –	10 10	– –	10 10	ns

FIGURE 2 — INPUT CLOCK WAVEFORM



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_S = 0 Vdc, T_A = 0°C to 70°C)

Number	Characteristic	8 MHz MC68230L8		10 MHz MC68230L10		Unit
		Min	Max	Min	Max	
1	R/$\overline{W}$, RS1-RS5 Valid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	ns
2(10)	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	–	65	–	ns
3(11)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	–	20	–	ns
4(2)	$\overline{CS}$ Low to data Out Valid (Delay)	–	75	–	60	ns
5	RS1-RS5 Valid to Data Out Valid (Delay)	–	140	–	100	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle) (Delay)	0	70	0	60	ns
7(3)	DTACK Low to $\overline{CS}$ High (Hold Time)	0	–	0	–	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	–	0	–	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High-Impedance (Delay)	–	50	–	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to DTACK High (Delay)	–	50	–	30	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance (Delay)	–	100	–	55	ns
12	Data Invalid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	ns
13	$\overline{CS}$ Low to Data In INvalid (Hold Time)	100	–	65	–	ns
14	Input Data Valid to H1(H3) Asserted (Setup Time)	100	–	60	–	ns
15	H1(H3) Asserted to Input Data Invalid (Hold Time)	20	–	20	–	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	–	40	–	ns
17	Handshake Input (H1-H4) Pulse Width Negated	40	–	40	–	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay)	–	150	–	120	ns
19	CLK Low to H2(H4) Asserted (Delay)	–	100	–	100	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	–	0	–	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay)	–	125	–	125	ns
22(9, 11)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted (See Figures 13 and 14)	2.5	3.5	2.5	3.5	CLK Per
23	CLK Low $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	3	3	3	3	CLK Per
24	CLK Low to Output Data Valid (Delay) (Modes 0, 1)	–	150	–	120	ns
25(9, 11)	Synchronized H1(H3) to Output Data Invalid (Modes 0, 1)	1.5	2.5	1.5	2.5	CLK Per
26	H1 Negated to Output Data Valid (Modes 2, 3)	–	70	–	50	ns
27	H1 Asserted to Output Data High Impedance (Modes 2, 3)	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	–	0	–	ns
29	CLK Low to Data Output Valid (Interrupt Acknowledge Cycle)	–	120	–	100	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	–	40	–	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	–	40	–	ns
32(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ is Asserted (See Figures 13 and 14)	3	3	3	3	CLK Per
33(9, 11)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	CLK Per
34	CLK Low to $\overline{DTACK}$ Low (Interrupt Acknowledge Cycle (Delay)	–	75	–	60	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay)	0	120	0	100	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay)	0	120	0	100	ns
–	CLK Low to $\overline{PIRQ}$ Low or High Impedance	–	200	–	150	ns
– (8)	TIN Frequency (External Clock) – Prescaler Used	0	1	0	1	Fclk(Hz)/(6)
–	TIN Frequency (External Clock) – Prescaler Not used	0	1/32	0	1/32	Fclk(Hz)/(6)
–	TIN Pulse Width High or Low (External Clock)	55	–	45	–	ns
–	TIN Pulse Width Low (Run/Halt Control)	1	–	1	–	CLK
–	CLK Low to TOUT High, Low, or High Impedance	0	200	0	150	ns
–	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	–	30	–	ns

NOTES

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three CLKs after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

2. Assuming the RS1-RS5 to Data Valid time has also expired.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3 This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

4 This specification assures recognition of the asserted edge of H1(H3).

5 This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

6 CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

7 If the setup time on the rising edge of the clock is violated, H1(H3) may not be recognized until the next rising of the clock.

8 This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

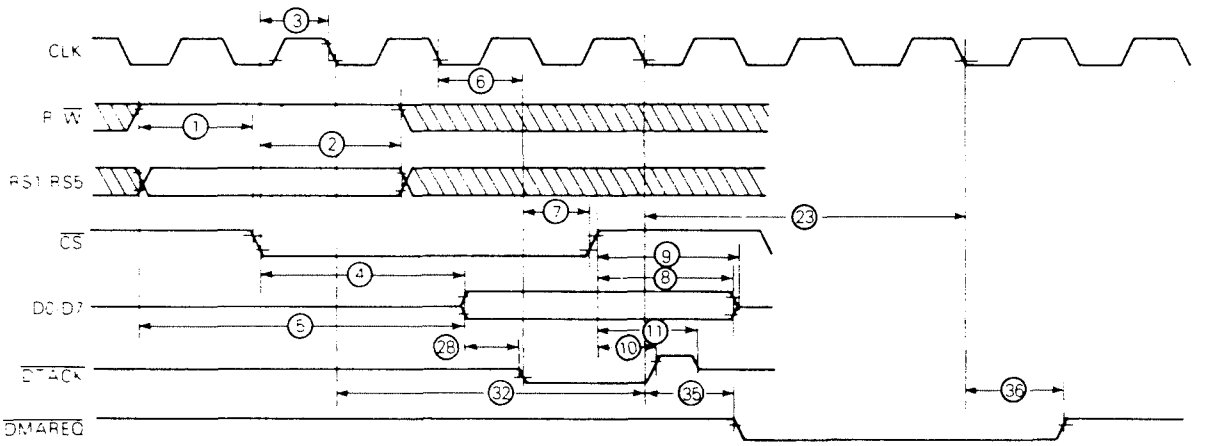
If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an 'AND' function of the clock and a control signal.

9 The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.

10 See BUS INTERFACE CONNECTION section for exception.

11 Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the BUS INTERFACE CONNECTION section for the exception concerning $\overline{CS}$.)

FIGURE 3 — BUS READ CYCLE TIMING



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 4 — BUS WRITE CYCLE TIMING

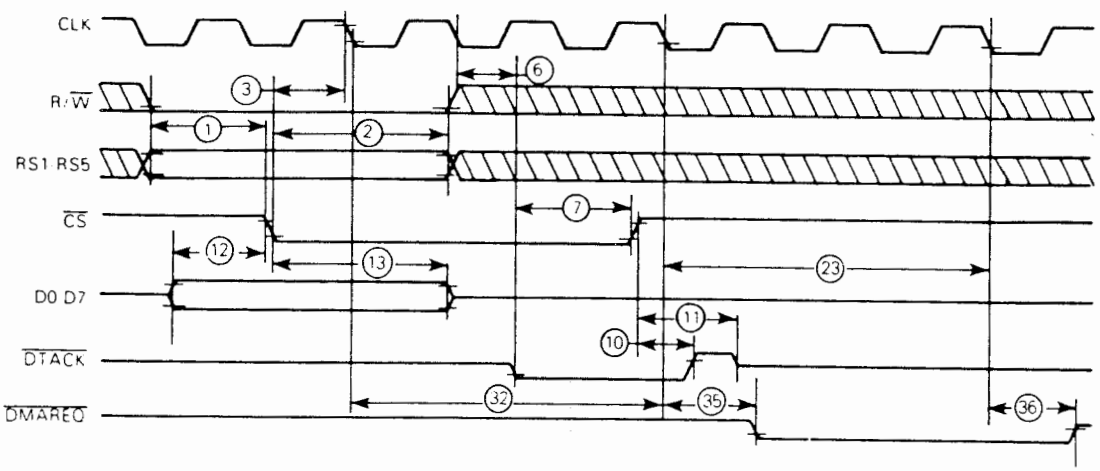
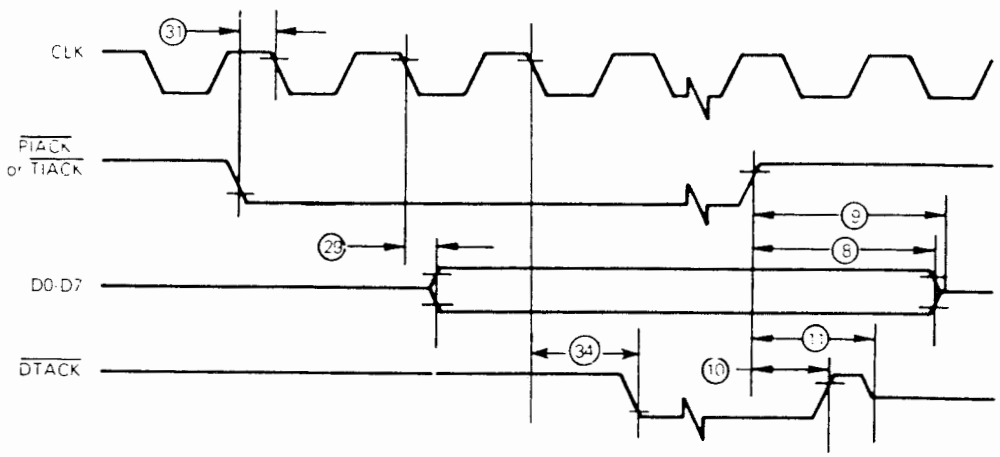


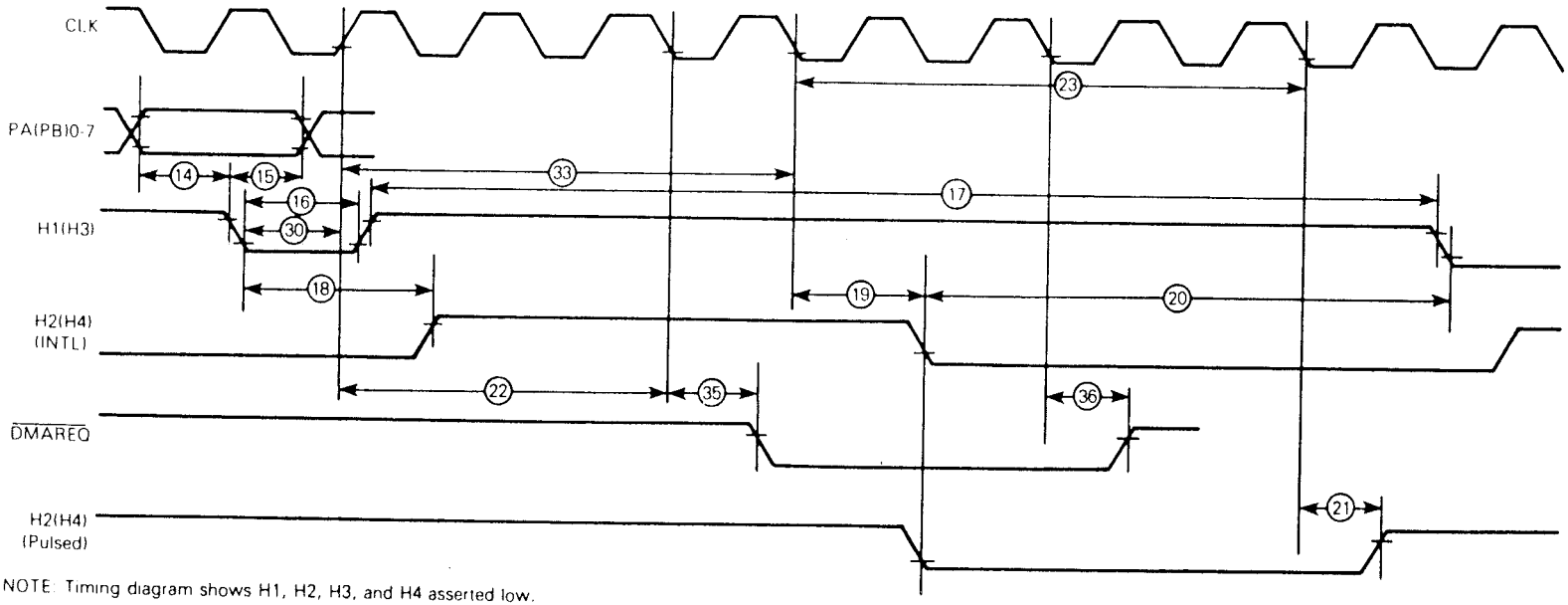
FIGURE 5 — INTERRUPT ACKNOWLEDGE
FUNCTIONAL TIMING DIAGRAM



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

FIGURE 6 — PERIPHERAL INTERFACE INPUT TIMING



NOTE: Timing diagram shows H1, H2, H3, and H4 asserted low.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP