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VMIVME-2536

OPTICALLY-COUPLED DIGITAL I/O BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-002536-000 C

Revised May 10, 1995

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	01/05/93	Release per ECO	92-0499
B	04/27/93	Cover, pages ii, and 3-2	93-0418
C	05/10/95	Cover, pages i, ii, v, vi, vii, 3-3, 5-2, and Section 6	95-0301

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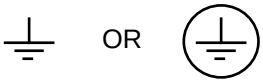
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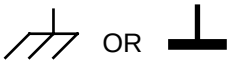
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



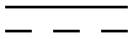
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



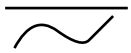
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

```
**************
*  CAUTION   *
**************
```

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

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VMIVME-2536
OPTICALLY COUPLED DIGITAL I/O BOARD

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A Assembly Drawing, Parts List, and Schematics

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SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-2536 Optically Coupled Digital I/O Board is designed to provide isolation between the field and VME chassis. There are 32 optically coupled inputs and 32 optically coupled outputs. Both inputs and outputs provide a sustained 1 kV of system isolation to the VME backplane. The inputs have a software selectable debounce timer to prevent false readings of mechanical switches or relays.

The VMIVME-2536 optically coupled digital I/O board has several features as specified below.

a. 32 bits of optically coupled voltage sourcing or current sinking outputs
b. 32 bits of optically coupled voltage or contact sensing inputs
c. On-board sockets for user-installed pull-up resistors to reconfigure the I/O
d. External voltage or internal VMEbus +5 V may be jumper-selected on byte boundaries to supply power for contact sensing mode.
e. On-board Built-in-Test logic for fault detection and isolation
f. Front panel with Fail LED
g. Input ranges of 5 to 125 V
h. Output ranges to a maximum of 30 V/300 mA
i. 8-, 16-, 32-bit data transfers
j. Double Eurocard form factor

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-2536 Board has input circuitry that permits the user to select and configure the basic input functions. This allows the user to set some of the inputs for one function and the rest for another on byte boundaries. The threshold levels for the inputs are set during manufacturing according to the selected option.

The output circuitry of the VMIVME-2536 also has user selectable configurations. The optically coupled open-collector outputs may be configured with a user-installed pull-up resistor to select between voltage sourcing and current sinking. These output functions may be selected on byte boundaries.

This board supports built-in-test of most of the active components. Test registers are mapped into the same addresses as the I/O registers they are to test. These registers allow the host to write data to an address, read it back, and compare the two to determine the health of the board. After the health of the board has been determined, the board may be changed from off-line to on-line mode.

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A Control and Status Register (CSR) is used to control the state of the board. This register allows independent control of the on-line/off-line state of the inputs and outputs. It also allows the user to select one of eight possible input debounce times and provides control for the front panel Fail LED.

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-002536-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

The VMIVME-2536 Optically Coupled Digital Input/Output Board is designed to provide isolation between the system hardware and the VMEbus. The input threshold trip level is set during manufacturing according to the option ordered. The output voltage level is determined by the system hardware to which it is connected.

When the VMEbus address matches the board address for the input data ports, the corresponding field data is latched in the Input Data Registers. The data is then steered to the proper data lines on the backplane for the host to use. If no debounce delay has been selected, successive reads of the input data ports will result in new data being latched from the field on every read cycle. If one of the debounce delays has been selected, successive reads of the input data ports will present the same data that was latched from the previous read until the debounce timer expires. Only after expiration of the timer will new data be stored in the input data latches on a read cycle.

When the VMEbus address matches the board address for the output data ports, the data is steered from the backplane and stored in the Output Data Registers. The data stored in these registers is used to drive the open-collector outputs to the field.

The VMIVME-2536 has built-in-test registers. They are used to check the health of the board. The host simply writes data to the register to be checked. Then by reading the register and comparing the data read to the data written, the user can determine if the board is functioning correctly. In order to maintain isolation between the field and the VMEbus, the built-in-test registers can only verify the circuitry associated with the VME side of the board.

Figure 3.1-1 is a block diagram of the basic functions of the VMIVME-2536. These blocks will be discussed in more detail in the following sections.

3.1.1 Data Polarity

The VMIVME-2536 has positive true I/O data polarity. This means that when the external input applied causes the optocoupler to be active (turned on) it will result in a one being seen at the VMEbus. When a "one" on the VMEbus is written to an output, the open-collector output transistor will be active (turned on).

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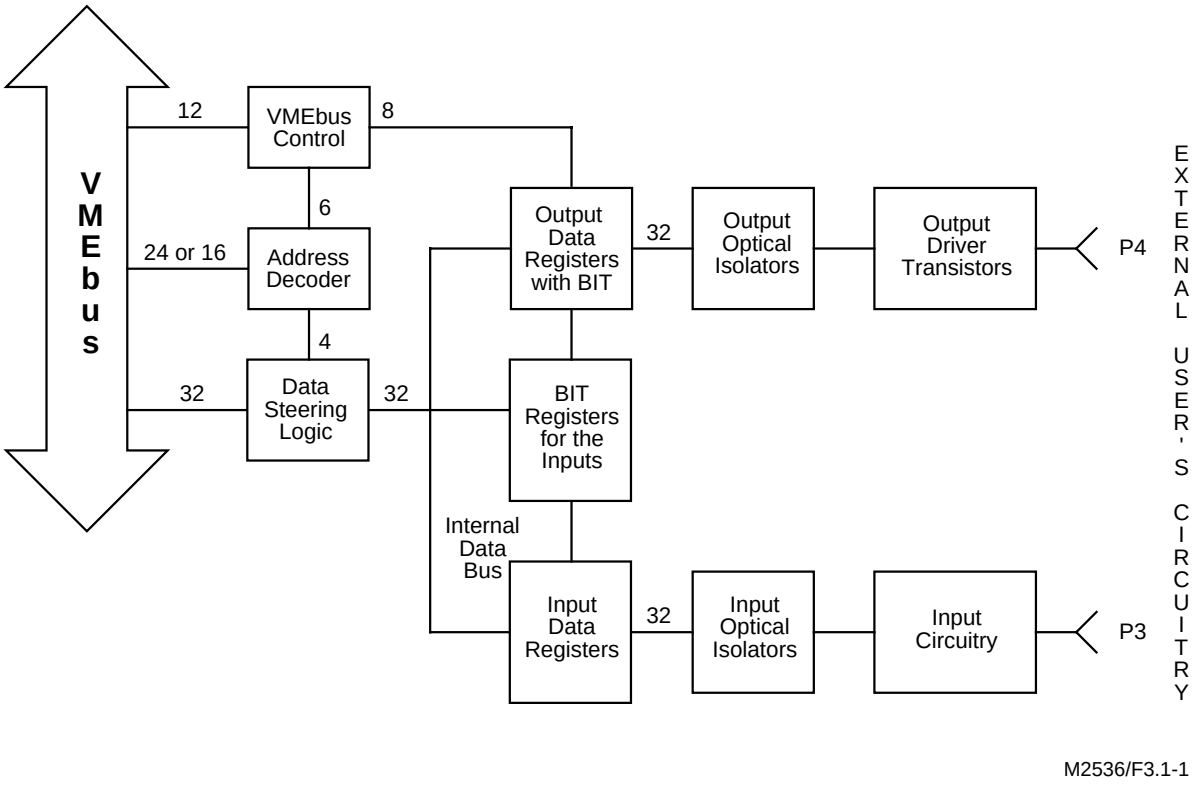


Figure 3.1-1. VMIVME-2536 Functional Block Diagram

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3.2 TEST REGISTERS

The test registers are used to check for proper functioning of the board. If the test mode bits are set Low (TEST MODE active), half of the test registers are allowed to drive the inputs of the input data latches, the other half of the test registers monitor the data present at the Output Data Registers. The test registers are mapped into the same address as their corresponding Input or Output Registers. This allows the user to simply write to and then read from the port to be checked. Data written to the INPUT TEST Register will overwrite the data in the INPUT DATA Register on the next read cycle. Data stored in the OUTPUT DATA Register will be latched in the OUTPUT TEST Register on the next read cycle. Figure 3.2-1 is a block diagram of the Test and Data Registers of the VMIVME-2536.

3.3 INPUT CIRCUITRY

Figure 3.3-1 shows the basic topology for each input. The open-collector output of the optoisolator goes to an Input Data Register (IDR). When a VMEbus read is performed on the input port, the Input Data Register latches the data present at the output of the optoisolator. The data is held in these registers while the on-board control logic steers the data to the appropriate VMEbus data lines.

Resistor Rvs is an option dependent current limiting resistor. The value of this resistor is selected during manufacturing to provide the typical threshold specified for the option ordered.

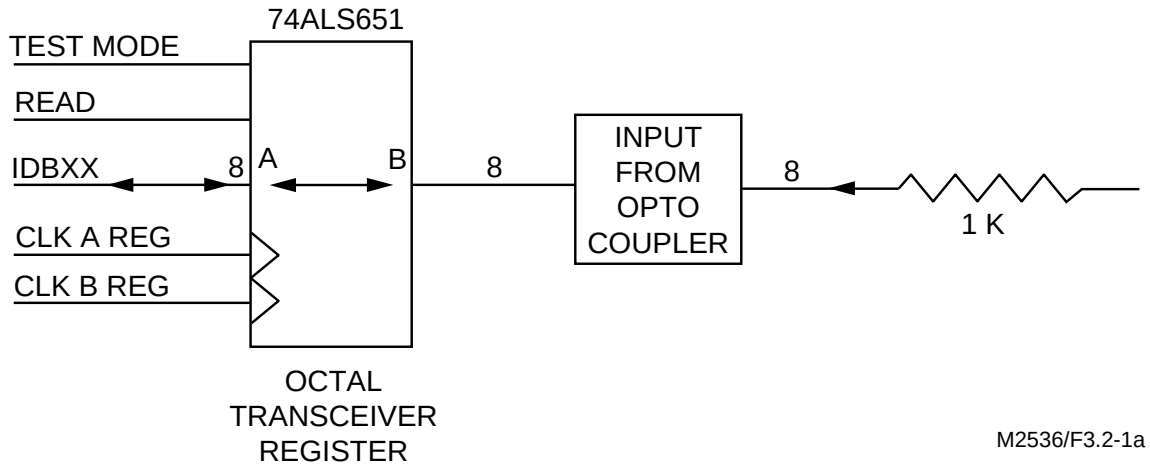
3.3.1 Input Types

The inputs can be configured for one of two types, either as voltage sensing or contact sensing. Voltage sensing is the input type shipped from the factory. Sockets have been provided on-board for installation of user-supplied pull-up resistors to configure the inputs for contact sensing. These pull-up resistors may be jumpered to the on board +5 V or an external voltage supplied by the user (see Figures 5.2.1-1 and 5.2.2-2). The typical threshold current through the on-board input circuit is approximately 0.9 mA. A table listing user-supplied pull-up resistor values resulting in a current draw of approximately 0.9 mA is shown in Table 3.3.1-1.

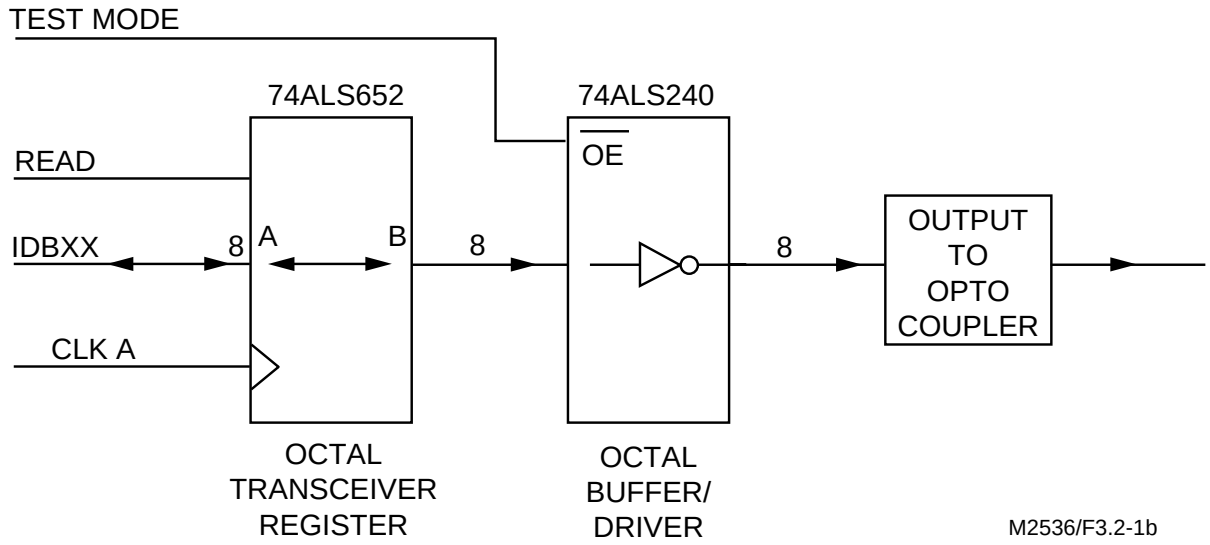
3.4 OUTPUT CIRCUITRY

Figure 3.4-1 shows the basic topology of each output. The information stored in the Output Data Register (ODR) from a VMEbus write is gated to the LED of the optocoupler. The output of the optocoupler biases the output transistors ON or OFF.

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a. Input Built-in-Test



b. Output Built-in-Test

Figure 3.2-1. Test and Data Register Block Diagram

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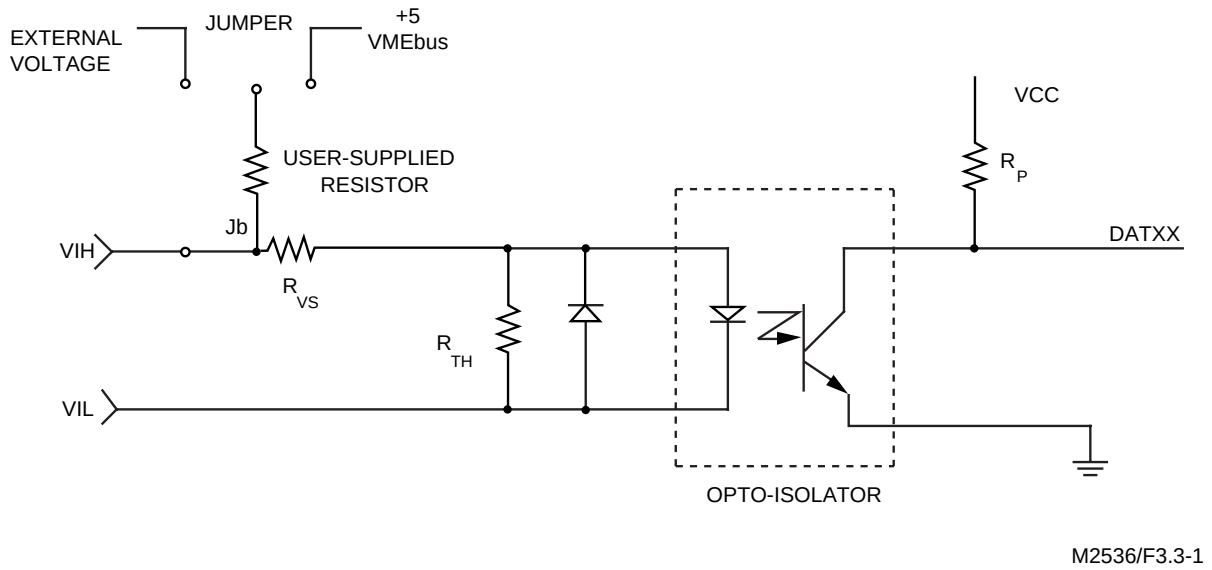


Figure 3.3-1. Typical Input Configuration

Table 3.3.3-1. User-Supplied Contact Sense Resistors

INPUT VOLTAGE OPTION	R VALUE FOR APPROXIMATELY 0.9 mA CURRENT DRAW
5 V	2.7 kΩ
12 V	6.8 kΩ
28 V	18 kΩ
48 V	22 kΩ
125 V	*

M2536/T3.3.3-1

* Cannot support contact sense on the 125 V option. The maximum power of a SIP resistor pack is 0.125 W.

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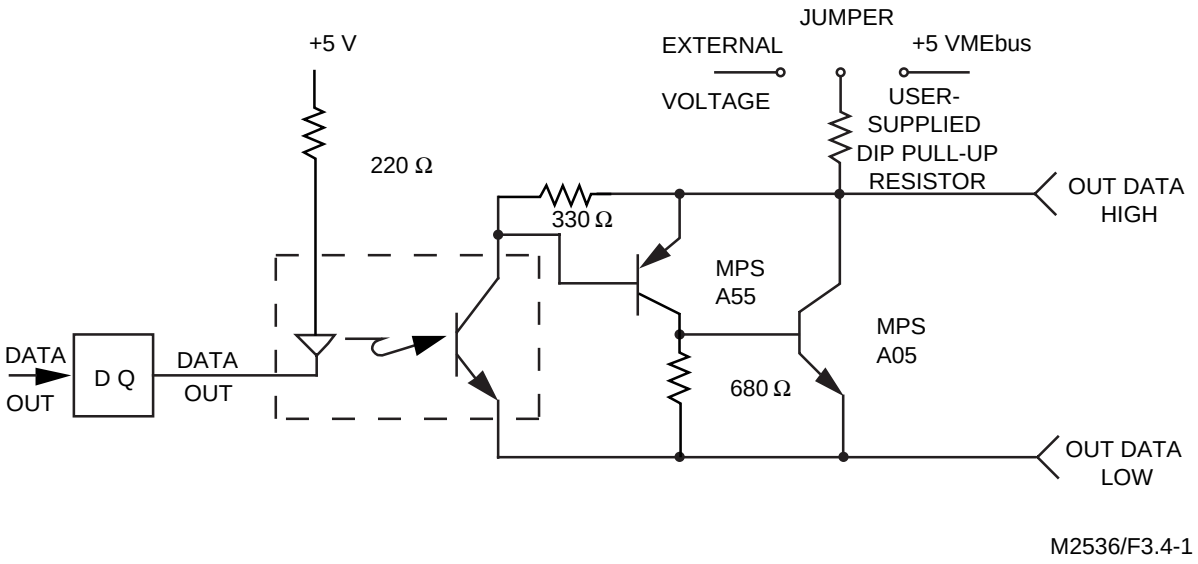


Figure 3.4-1. Typical Output Configuration

3.4.1 Output Types

The open-collector outputs can be configured for one of two types, either voltage sourcing or current sinking. Current sinking is the type shipped from the factory. Sockets have been provided on-board for installation of user-supplied pull-up resistors to configure the outputs for voltage sourcing. These pull-up resistors may be jumpered to either the on-board + 5 Volts or an external voltage supplied by the user.

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The VMIVME-2536 requires very little software. After performing any initialization or off-line testing, the user exits test mode by writing the Control and Status Register (CSR). The user may then perform a read or write operation to the appropriate I/O port to exchange data with the field.

Table 4.1-1 lists the address map for the VMIVME-2536. All addresses are shown relative to the board's base address.

Table 4.1-1. Address Map

Relative Address	Register Name
$00	BD ID (Board ID)
$02	CSR (Control and Status Register)
$04	Input Data Register 0
$05	Input Data Register 1
$06	Input Data Register 2
$07	Input Data Register 3
$08	Output Data Register 0
$09	Output Data Register 1
$0A	Output Data Register 2
$0B	Output Data Register 3
$0C	Reserved
$0D	Reserved
$0E	Reserved
$0F	Reserved

M2536/T4.1-1

4.2 BOARD ID REGISTER (BD ID)

The BD ID Register is a read only register. Its data is fixed at $2000. The board will respond to a write to this register; however, the data will be lost and will have no effect on the board. Table 4.2-1 shows the bit values for this register.

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Table 4.2-1. BD ID Register Bit Map

RELATIVE ADDRESS $00 BOARD ID UPPER BYTE (Read Only)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
L	L	H	L	L	L	L	L

RELATIVE ADDRESS $01 BOARD ID LOWER BYTE (Read Only)							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
L	L	L	L	L	L	L	L

M2536/T4.2-1

4.3 CONTROL AND STATUS REGISTER (CSR)

The CSR is a 16-bit register that is used to control the boards Fail LED, Test Registers, and Debounce timer. Table 4.3-1 shows the position of the bits used to perform these functions.

Table 4.3-1. CSR Bit Map

RELATIVE ADDRESS $02 CSR UPPER BYTE (Read/Write)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
FAIL_L	TEST MODE P4_L	TEST MODE P3_L	RESER-VED	RESER-VED	DELAY SELECT 2	DELAY SELECT 1	DELAY SELECT 0

RELATIVE ADDRESS $03 CSR LOWER BYTE (Read Only)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
L	L	L	L	L	L	L	L

M2536/T4.3-1

Bit 15 controls the Fail LED. Writing this bit low will turn the Fail LED ON.

Bit 14 controls the test mode for the P4 optically coupled outputs. Writing this bit low prevents the open-collector outputs from being biased on by the data stored in the Output Data Registers. Data stored in the Output Data Registers can always be read back through the Output Test Registers regardless of the state of the P4 test mode bit. This bit must be set high to allow the outputs to drive the field.

Bit 13 controls the test mode for the P3 optically coupled inputs. Writing this bit low disables the field data from being latched in the Input Data Registers and allows the Input Test Registers' outputs to be latched in the Input Data Registers. Data written to the Input Test Registers can only be read back when this bit is low. This bit must be set high to allow the board to read field data.

Bits 12 and 11 are Reserved. Data written to these locations can be read back; however, it has no effect on the board.

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Bits 10 through 8 are used to select one of the eight possible debounce delays for the opticoupled inputs. Table 4.3-2 lists the delays selected by the different bit combinations.

Table 4.3-2. Debounce Delay

CSR BITS 10	09	08	Debounce Time Selected
0	0	0	0.0
0	0	1	256 µ
0	1	0	512 µ
0	1	1	1.024 m
1	0	0	2.048 m
1	0	1	4.09 m
1	1	0	8.19 m
1	1	1	16.384 m

M2536/T4.3-2

Bits 7 through 0 are unused and will always read back as low. Data written to these locations will be lost and has no effect on the board.

All eight of the upper control bits (15 through 8) will be low on power-up or after a VMEbus reset. This ensures that the test mode is active and prevents the board from interacting with the field until commanded by the host. This will also cause the Fail LED to illuminate and selects a debounce time of zero.

4.4 INPUT REGISTER BIT DEFINITIONS

Table 4.4-1 lists the input channels and their associated register bit locations. The Input Data Register can be read as a Byte, Word, or Longword.

4.5 OUTPUT REGISTER BIT DEFINITIONS

Table 4.5-1 lists the output channels and their associated register bit locations. The Output Data Register can be written as a Byte, Word, or Longword.

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Table 4.4-1. Input Data Register Bit Map

RELATIVE ADDRESS $04 INPUT DATA REGISTER 0 (Read/Write)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24

RELATIVE ADDRESS $05 INPUT DATA REGISTER 1 (Read/Write)							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16

RELATIVE ADDRESS $06 INPUT DATA REGISTER 2 (Read/Write)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08

RELATIVE ADDRESS $07 INPUT DATA REGISTER 3 (Read/Write)							
Bit 07	Bit 08	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

M2536/T4.4-1

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Table 4.5-1. Output Data Register Bit Map

RELATIVE ADDRESS $08 OUTPUT DATA REGISTER 0 (Read/Write)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24

RELATIVE ADDRESS $09 OUTPUT DATA REGISTER 1 (Read/Write)							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16

RELATIVE ADDRESS $0A OUTPUT DATA REGISTER 2 (Read/Write)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08

RELATIVE ADDRESS $0B OUTPUT DATA REGISTER 3 (Read/Write)							
Bit 07	Bit 08	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

****
* CAUTION *
****

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 BOARD CONFIGURATION

The VMIVME-2536 is factory configured for current sinking outputs and voltage sensing inputs. Sockets have been provided on board to allow the user to install pull-up resistors for both inputs and outputs. This allows the outputs to be configured for voltage sourcing and the inputs to be configured for contact sensing. The inputs and outputs are configured in groups of 8 so the channels can be set on a byte-to-byte basis.

5.2.1 Input Topology

Figure 5.2.1-1 shows the circuit topology for contact sensing inputs. Figure 5.2.1-2 shows the circuit topology for the voltage sensing configuration.

5.2.2 Output Topology

Figure 5.2.2-1 shows the circuit topology for voltage sourcing outputs. Figure 5.2.2-2 shows the circuit topology for the current sinking configuration.

5.2.3 External Voltage

Figure 5.2.3-1 shows the location of the pull up voltage selection jumpers. Jumper fields E1, E6 - E8 are used for the four output bytes and E2 - E5 are

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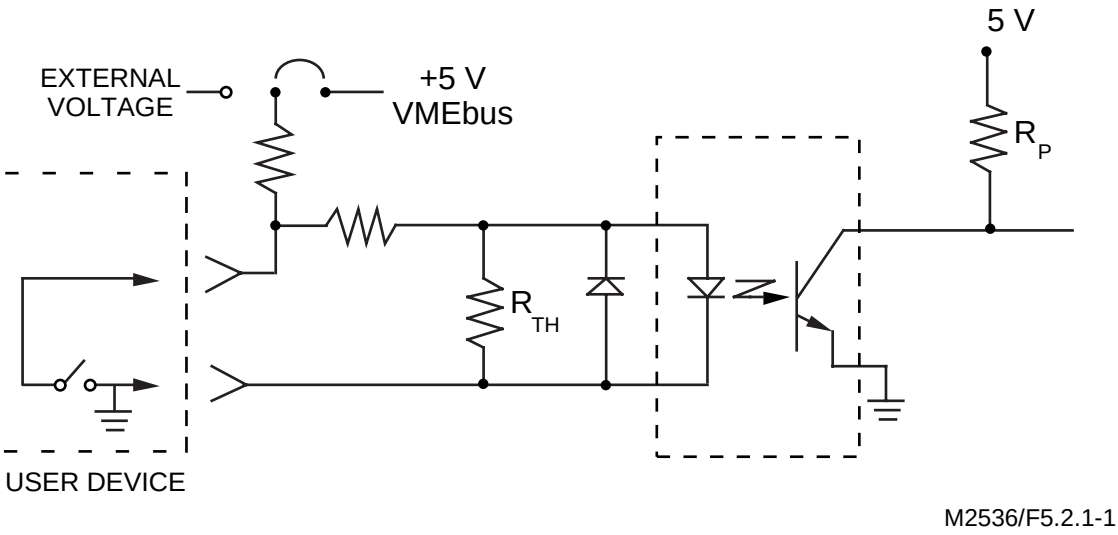


Figure 5.2.1-1. Typical Contact Sense Opto Input

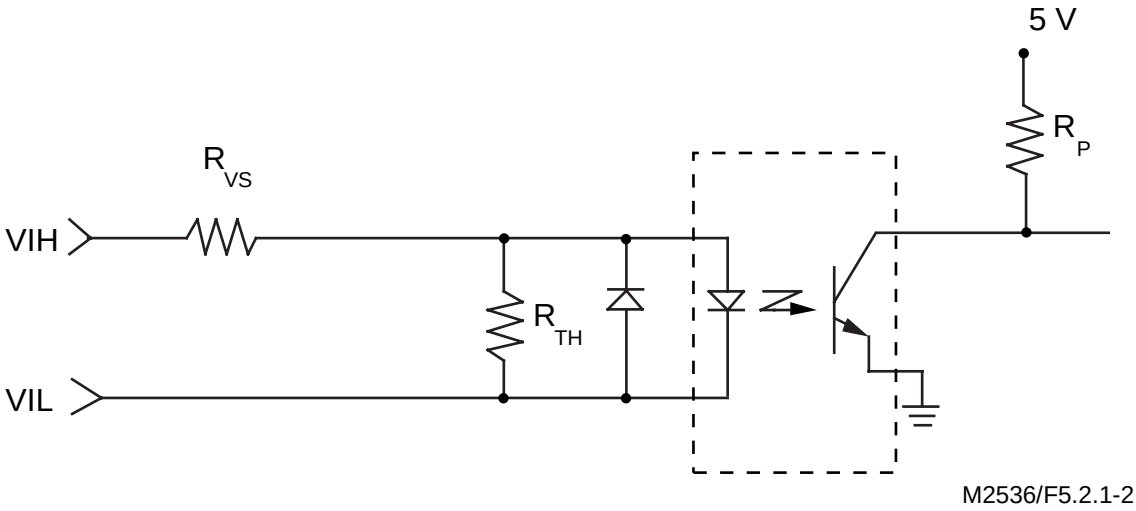


Figure 5.2.1-2. Typical Voltage Sense Opto Input

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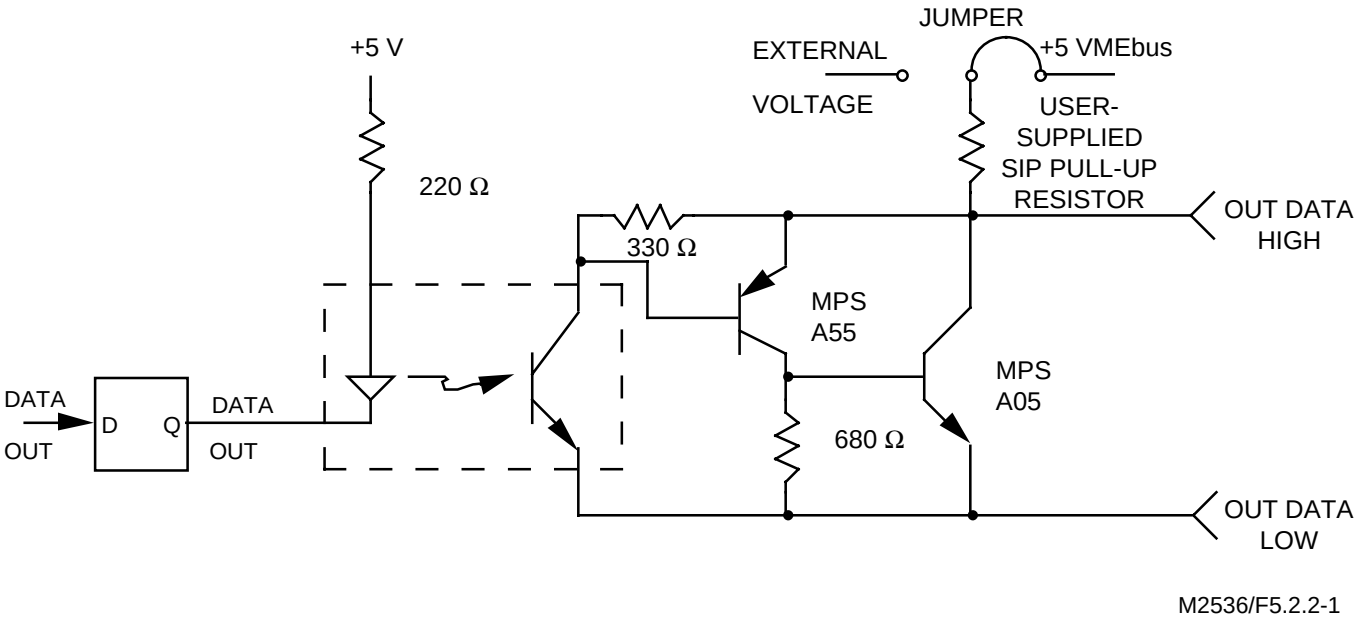


Figure 5.2.2-1. Typical Voltage Sourcing Output Configuration

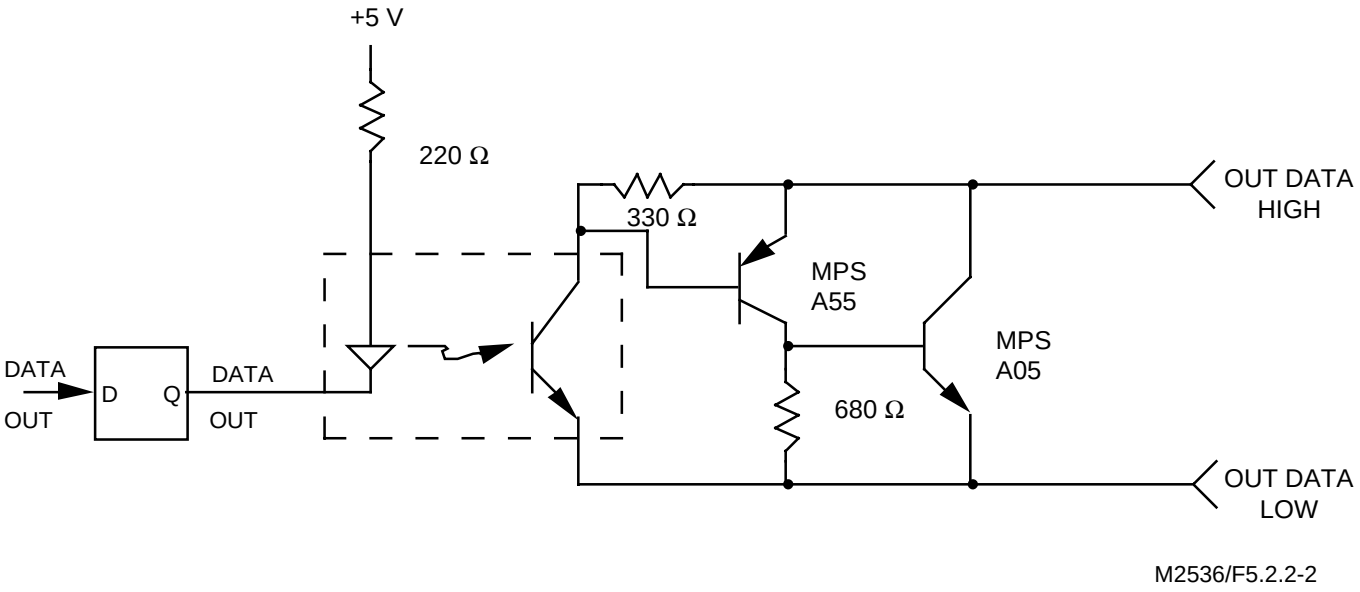


Figure 5.2.2-2. Typical Current Sinking Output Configuration

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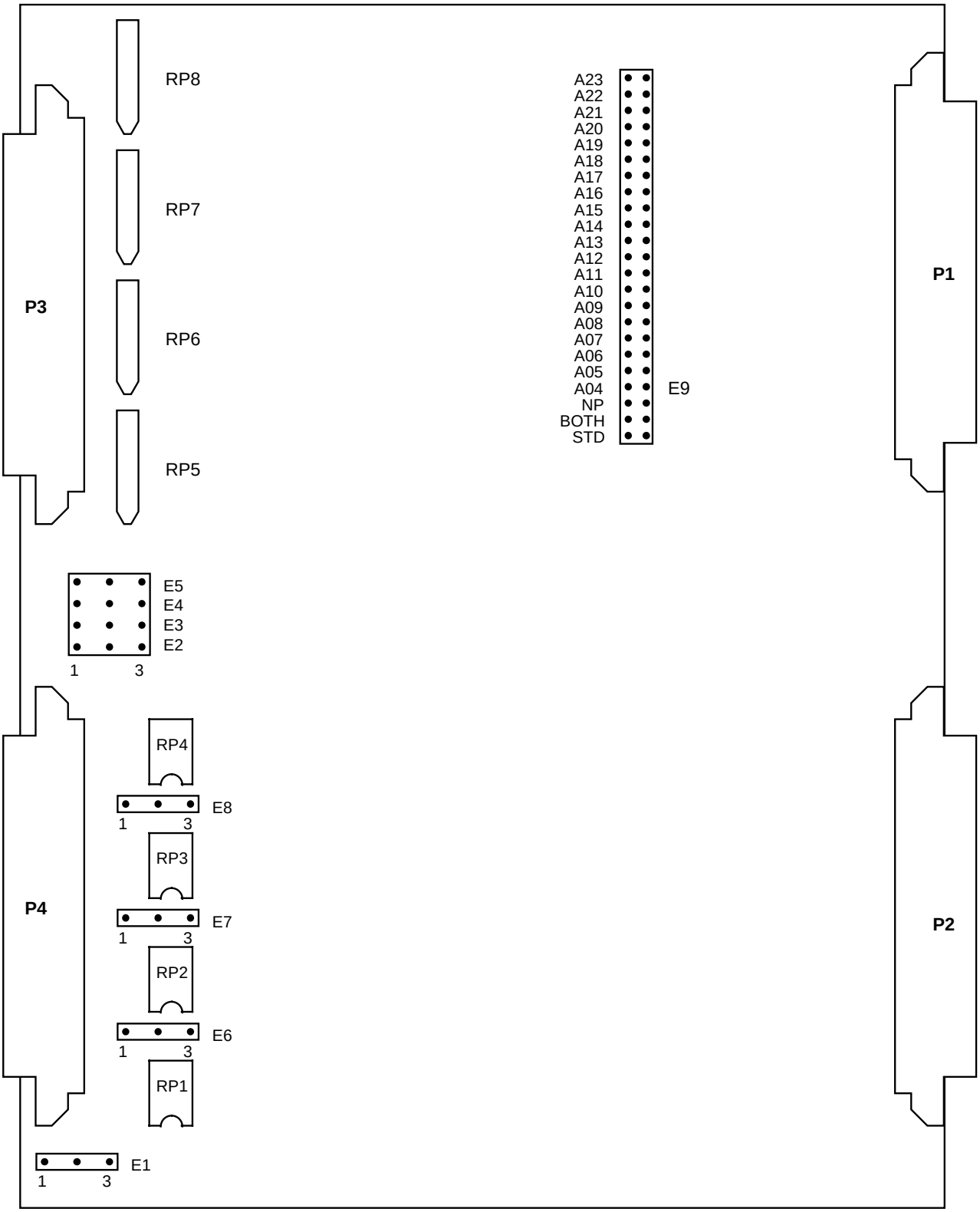


Figure 5.2.3-1. VMIVME-2536 Jumper Locations

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used for the four input bytes. Table 5.2.3-1 shows the data bits associated with each jumper. A jumper placed across pins 1 and 2 connects the on board + 5 Volts to the pull up. A jumper placed across pins 2 and 3 connects the user supplied external voltage to the pull up. The factory configuration has no jumpers installed.

Table 5.2.3-1. Pull-Up Voltage Selection Jumpers

PULL UP	JUMPER POSITION	DATA BITS
RP1	E1	Output Data Bits 7 through 0
RP2	E6	Output Data Bits 15 through 8
RP3	E7	Output Data Bits 23 through 16
RP4	E8	Output Data Bits 31 through 24
RP5	E5	Input Data Bits 7 through 0
RP6	E4	Input Data Bits 15 through 8
RP7	E3	Input Data Bits 23 through 16
RP8	E2	Input Data Bits 31 through 24

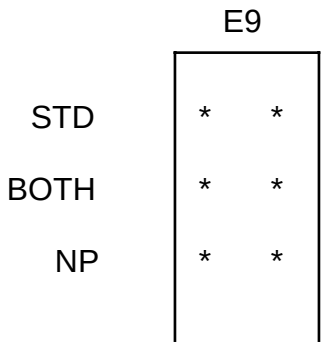
M2536/T5.2.3-1

5.3 ADDRESS MODIFIERS

The VMIVME-2536 is factory configured to respond to either short supervisory or short nonprivliged access. Figure 5.3-5 shows the factory configuration of the address modifier jumpers. This configuration can be changed by installing jumpers at the appropriate locations in the header as shown in the corresponding figures.

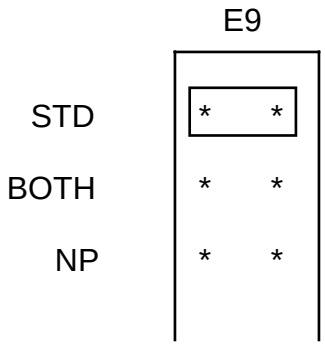
I/O ACCESS	CORRESPONDING FIGURE
Short supervisory	Figure 5.3-1
Standard Supervisory	Figure 5.3-2
Short Nonprivileged	Figure 5.3-3
Standard Nonprivileged	Figure 5.3-4
Short Supervisory or Short Nonprivileged	Figure 5.3-5 (factory configuration)
Standard Supervisory or Standard Nonprivileged	Figure 5.3-6

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M2536/F5.3-1

Figure 5.3-1. Jumper Configuration for Short Supervisory Access



M2536/F5.3-2

Figure 5.3-2. Jumper Configuration for Standard Supervisory Access

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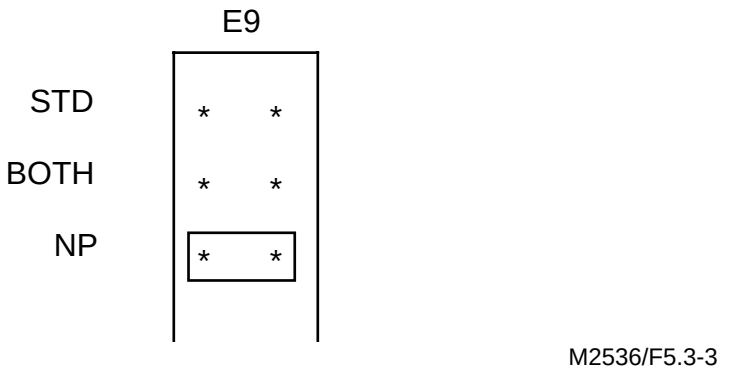


Figure 5.3-3. Jumper Configuration for Short Nonprivileged Access

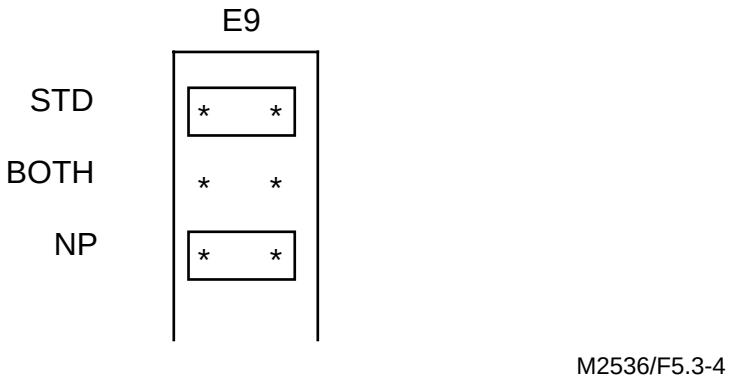
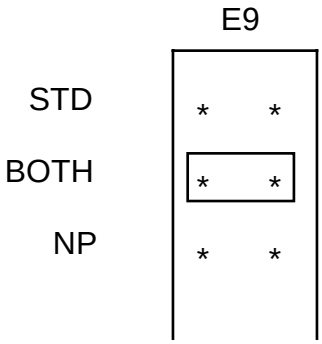


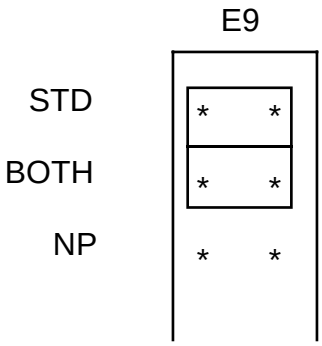
Figure 5.3-4. Jumper Configuration for Standard Nonprivileged Access

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M2536/F5.3-5

Figure 5.3-5. Jumper Configuration for Short Addressing with Supervisory or Nonprivileged Access



M2536/F5.3-6

Figure 5.3-6. Jumper Configuration for Standard Addressing with Supervisory or Nonprivileged Access

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5.4 ADDRESS SELECTION

The VMIVME-2536 is designed with a bank of address select jumpers that specifies the base address of the board. The address selection jumpers are shown in Figure 5.4-1. The VMIVME-2536 is factory configured to respond to 0000 HEX. An installed jumper causes the board to compare to a low address line, an omitted jumper causes the board to compare to a high address line.

5.5 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

a. Verify that the sections pertaining to theory and programming, Sections 3 and 4, have been reviewed and applied to system requirements.

b. Review Section 5.4 to verify that all factory installed jumpers are in place. To modify the board configuration, refer to Section 5.4.

c. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to Section 5.6 for connector descriptions.

After the checklist above has been completed, the board can be installed in a VMEbus system. DO NOT install or remove the board with power applied. This board may be installed in any slot position, except Slot 1 which is reserved for the system controller.

```
*****************
*    CAUTION    *
*****************
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DO NOT INSTALL OR REMOVE THE BOARDS WHILE POWER IS APPLIED.

5.6 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION

The front panel I/O connectors (P3 and P4) on the VMIVME-2536 are 64-pin DIN standard with the A and C rows installed and the B row empty. Table 5.6-1 contains compatible connector part numbers. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Document No. 825-000000-006) for additional information concerning the variety of possible cable and connector types available.

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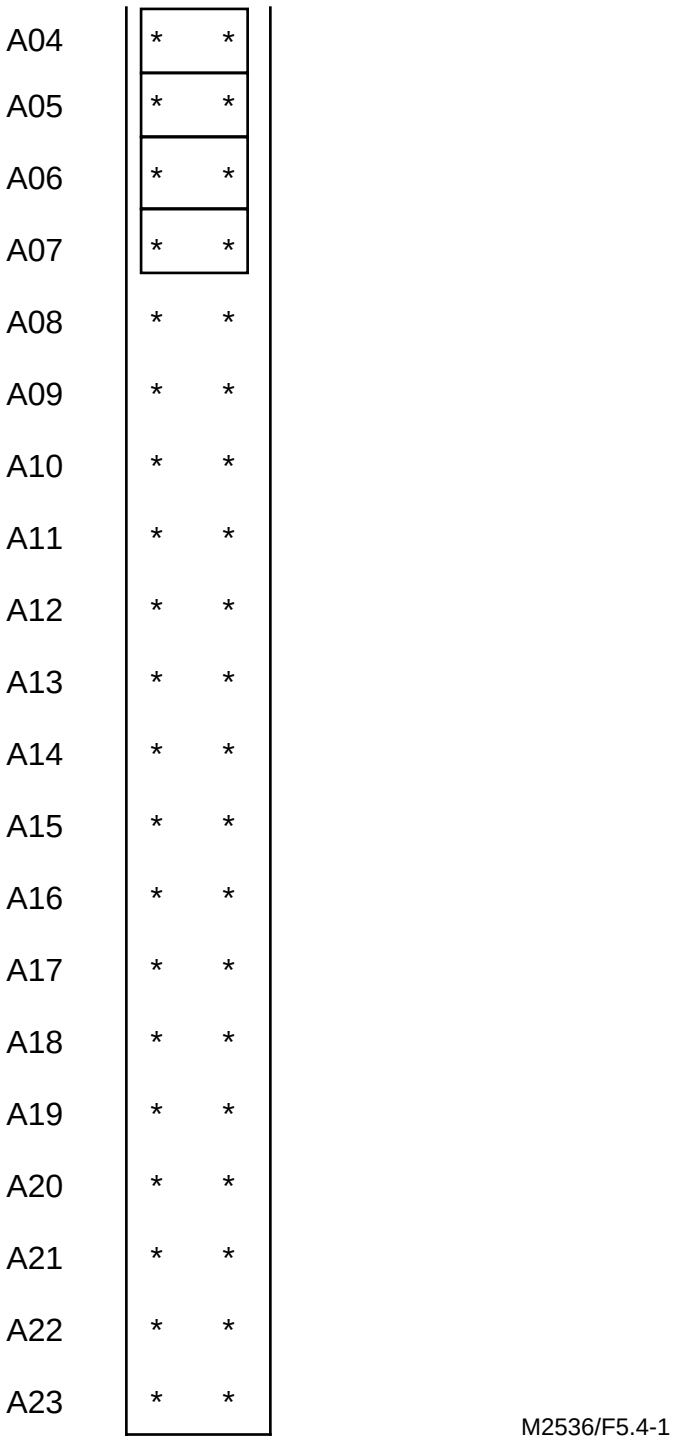


Figure 5.4-1. Base Address Select Jumpers

The example shown is for a short I/O base address of FF00 Hexadecimal (FFFF00 for Standard I/O Access)

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Table 5.6-1. Connector Information

COMPATIBLE CABLE CONNECTOR	PANDUIT NO. 120-964-435E
STRAIN RELIEF	PANDUIT NO. 100-000-032
PC BOARD HEADER CONNECTOR	PANDUIT NO. 120-000-032

M2536/T5.6-1

Figure 5.6-1 shows the pin layout of the P3 and P4 connectors. Tables 5.6-2 and 5.6-3 detail the connector pin assignments.

The P2 connector pin layout is shown in Figure 5.6-2 and the P2 pin assignments are listed in Table 5.6-4

5.7 TEST MODE SELECTION

At power-up both test mode bits are active which places all the I/O channels on the P3 and P4 connectors in their noninteractive mode. While in the test mode, data written to the Input Test Register can be read back through the input circuitry thereby verifying its readiness. Data written to the Output Data Register can be read back through the Output Test Register. To enable normal operation bits 14 and 13 of the CSR must be set to a "one".

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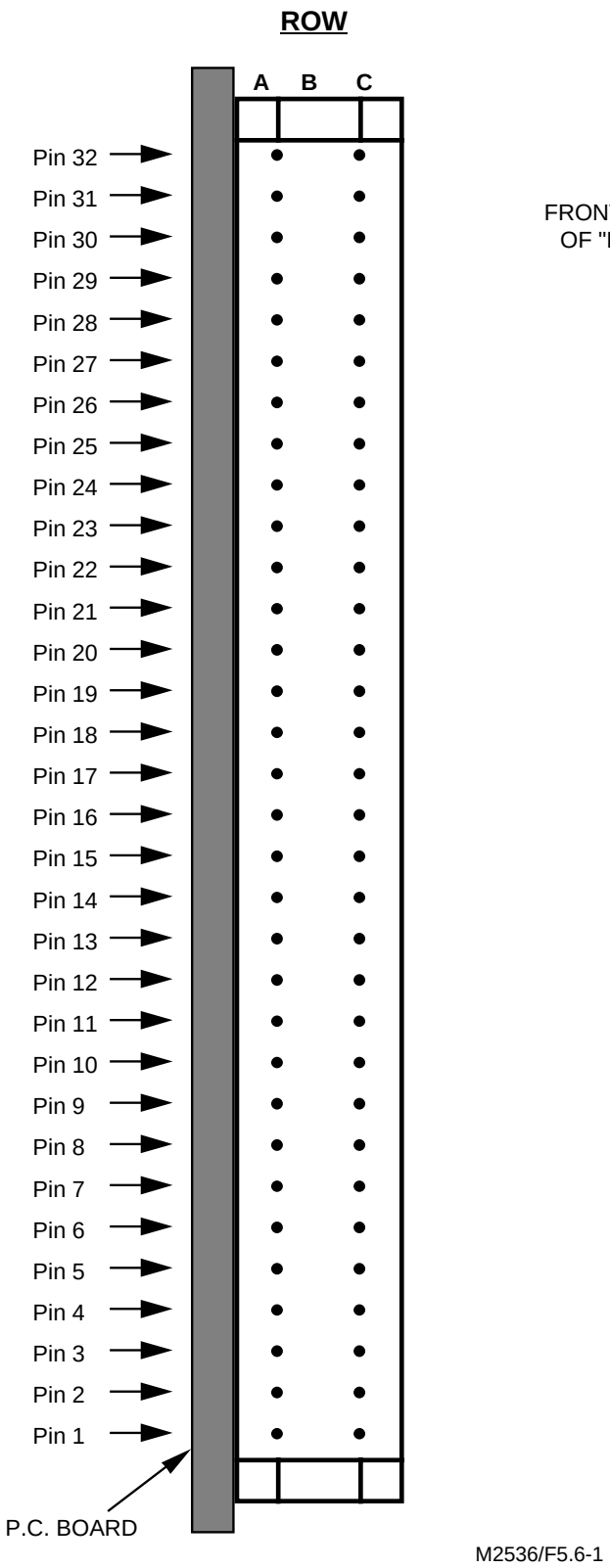


Figure 5.6-1. P3/P4 Connector Pin Layout

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Table 5.6-2. P3 PIN Assignments

ROW A	DATA BIT	ROW C	DATA BIT
1	HIGH IN 0	1	LOW IN 0
2	HIGH IN 1	2	LOW IN 1
3	HIGH IN 2	3	LOW IN 2
4	HIGH IN 3	4	LOW IN 3
5	HIGH IN 4	5	LOW IN 4
6	HIGH IN 5	6	LOW IN 5
7	HIGH IN 6	7	LOW IN 6
8	HIGH IN 7	8	LOW IN 7
9	HIGH IN 8	9	LOW IN 8
10	HIGH IN 9	10	LOW IN 9
11	HIGH IN 10	11	LOW IN 10
12	HIGH IN 11	12	LOW IN 11
13	HIGH IN 12	13	LOW IN 12
14	HIGH IN 13	14	LOW IN 13
15	HIGH IN 14	15	LOW IN 14
16	HIGH IN 15	16	LOW IN 15
17	HIGH IN 16	17	LOW IN 16
18	HIGH IN 17	18	LOW IN 17
19	HIGH IN 18	19	LOW IN 18
20	HIGH IN 19	20	LOW IN 19
21	HIGH IN 20	21	LOW IN 20
22	HIGH IN 21	22	LOW IN 21
23	HIGH IN 22	23	LOW IN 22
24	HIGH IN 23	24	LOW IN 23
25	HIGH IN 24	25	LOW IN 24
26	HIGH IN 25	26	LOW IN 25
27	HIGH IN 26	27	LOW IN 26
28	HIGH IN 27	28	LOW IN 27
29	HIGH IN 28	29	LOW IN 28
30	HIGH IN 29	30	LOW IN 29
31	HIGH IN 30	31	LOW IN 30
32	HIGH IN 31	32	LOW IN 31

M2536/T5.6-2

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Table 5.6-3. P4 PIN Assignments

ROW A	DATA BIT	ROW C	DATA BIT
1	HIGH OUT 0	1	LOW OUT 0
2	HIGH OUT 1	2	LOW OUT 1
3	HIGH OUT 2	3	LOW OUT 2
4	HIGH OUT 3	4	LOW OUT 3
5	HIGH OUT 4	5	LOW OUT 4
6	HIGH OUT 5	6	LOW OUT 5
7	HIGH OUT 6	7	LOW OUT 6
8	HIGH OUT 7	8	LOW OUT 7
9	HIGH OUT 8	9	LOW OUT 8
10	HIGH OUT 9	10	LOW OUT 9
11	HIGH OUT 10	11	LOW OUT 10
12	HIGH OUT 11	12	LOW OUT 11
13	HIGH OUT 12	13	LOW OUT 12
14	HIGH OUT 13	14	LOW OUT 13
15	HIGH OUT 14	15	LOW OUT 14
16	HIGH OUT 15	16	LOW OUT 15
17	HIGH OUT 16	17	LOW OUT 16
18	HIGH OUT 17	18	LOW OUT 17
19	HIGH OUT 18	19	LOW OUT 18
20	HIGH OUT 19	20	LOW OUT 19
21	HIGH OUT 20	21	LOW OUT 20
22	HIGH OUT 21	22	LOW OUT 21
23	HIGH OUT 22	23	LOW OUT 22
24	HIGH OUT 23	24	LOW OUT 23
25	HIGH OUT 24	25	LOW OUT 24
26	HIGH OUT 25	26	LOW OUT 25
27	HIGH OUT 26	27	LOW OUT 26
28	HIGH OUT 27	28	LOW OUT 27
29	HIGH OUT 28	29	LOW OUT 28
30	HIGH OUT 29	30	LOW OUT 29
31	HIGH OUT 30	31	LOW OUT 30
32	HIGH OUT 31	32	LOW OUT 31

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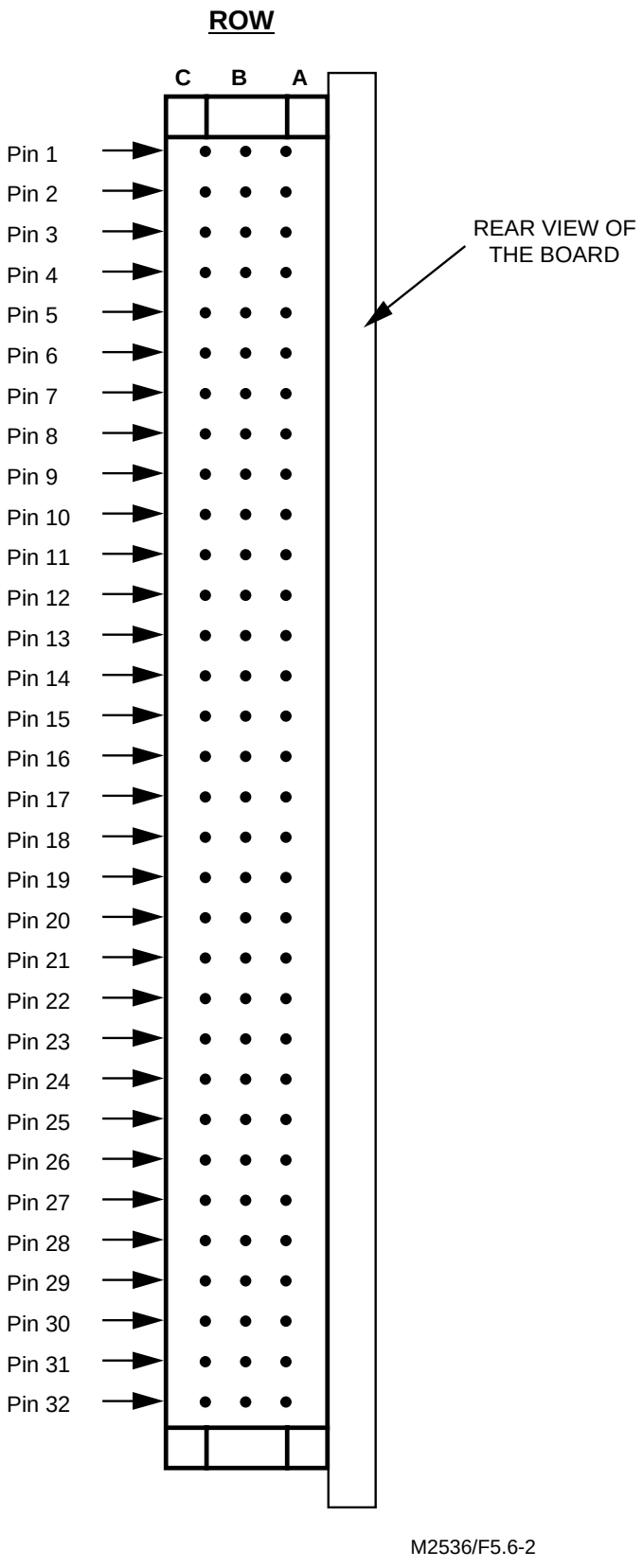


Figure 5.6-2. P2 Connector Pin Layout

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Table 5.6-4. P2 Connector Pin Assignments

PIN NO.	ROW A	ROW B	ROW C
1	GND	+5 V	GND
2	GND	GND	VEXT 1
3	GND	N/C	GND
4	GND	N/C	VEXT 2
5	GND	N/C	GND
6	GND	N/C	VEXT 3
7	GND	N/C	GND
8	GND	N/C	VEXT 4
9	GND	N/C	GND
10	GND	N/C	VEXT 5
11	GND	N/C	GND
12	GND	GND	VEXT 6
13	GND	+5 V	GND
14	GND	D16	VEXT 7
15	GND	D17	GND
16	GND	D18	VEXT 8
17	GND	D19	GND
18	GND	D20	N/C
19	GND	D21	GND
20	GND	D22	N/C
21	GND	D23	GND
22	GND	GND	N/C
23	GND	D24	GND
24	GND	D25	N/C
25	GND	D26	GND
26	GND	D27	N/C
27	GND	D28	GND
28	GND	D29	N/C
29	GND	D30	GND
30	GND	D31	N/C
31	GND	GND	GND
32	GND	+5 V	N/C

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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