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Find the *Abaco Systems / VMIC VMIVME-2540-300* at our website: ***Click HERE***

VMIVME-2540
24-Channel Intelligent Counter/Controller

- Event counting - up to 4 giga events
- Frequency measurement —1.16 x 10^{-3} Hz to 2.5 MHz
- Period/pulse-width measurement—400 ns to 8.5899 x 10^{6} s (32-bit floating point), 400 ns to 858 s (32-bit unsigned integer)
- Square wave/pulse train generation - 0.0076 Hz to 2.5 MHz
- Timer/periodic VMEbus interrupter - 0.0076 to 1,000 Hz
- Quadrature position measurement - sin/cos up to 1 MHz, 32-bit counters, limit/modulo checking
- Integer period/pulse-width measurement 16- and 32-bit, discrete or continuous; low data transport lags
- Programmed output - up to 24 discrete outputs
- Pulse sequence mode - train of N pulses with programmable duty cycle
- Quadrature position control outputs - ±1/4 wave control resolution; up to 1.25 MHz step rate and ±32767 steps per command
- Integer QPM group acquisition - captures two integer QPM measurements simultaneously
- Event-triggered timer delay - generates VMEbus interrupt up to 131.1 seconds after event edge input; retriggerable
- 24 control/measurement interfaces: 24 clocks, 24 gates, 24 outputs
- RS-422 differential interface with support for single-ended TTL inputs
- Options allow configurations of 4, 8, 16, and 24 interfaces
- On-board 15 MHz 68HC000 CPU
- A32/A24/D32/D16/D8 (EO) VME slave interface, 64 Kbyte VMEbus memory window
- Data exchange interface: ANSI/IEEE standard 754-1985 for 32-bit floating-point arithmetic
- Continuous measurement modes
- VMEbus compatible ANSI/IEEE 1014-1987 IEC 821 and 297

APPLICATIONS

- Rotational shaft instrumentation: angular position, velocity, acceleration
- Automotive industry testing: brakes, transmissions, tachometer
- Robotics
- Telescope/observatory
- Medical/laboratory instruments
- Linear position measurement: distance, velocity, acceleration
- Elevators
- Overhead cranes
- X-Y tables
- Machine tools
- Automatic storage retrieval

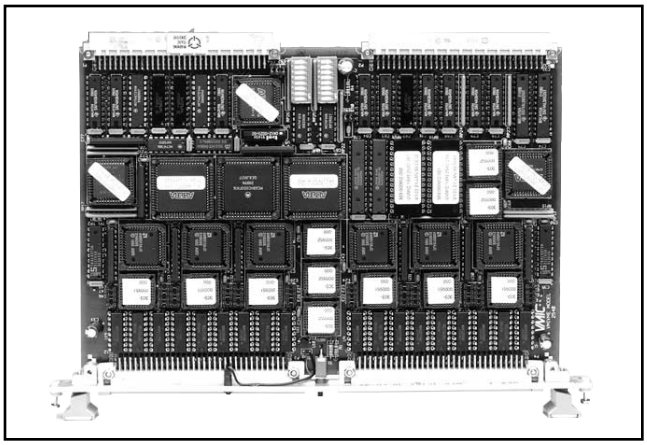
PRODUCT OVERVIEW — The VMIVME-2540 Intelligent Counter/Controller (ICC) is a VMEbus slave I/O module designed to provide high-precision digital measurement and function generation capability for VMEbus systems with a simple, consistent memory-mapped user interface. The following functions are supported by the VMIVME-2540:

Measurement Functions

Event counting
Frequency measurement
Period/pulse-width measurement
Quadrature position measurement

Generation Functions

Pulse train/square wave generation
Timer/periodic interrupt generation
Frequency division
Quadrature position control



Once programmed by the VMEbus host, the VMIVME-2540 ICC performs these functions automatically. The on-board CPU maintains data structures in shared local memory for buffering measurements and queueing control commands. Measurement functions are also supported by a Continuous Measurement Mode in which measurements are made repeatedly without host CPU involvement. I/O connections are routed through high-density connectors located on the front panel with support for differential and single-ended signal levels. The user data exchange interface for measurement and generation modes complies with ANSI/IEEE Standard 754-1985 for 32-bit floating-point arithmetic. Integer modes operate with two's complement signed arithmetic and with unsigned arithmetic.

TECHNICAL DESCRIPTION — The VMIVME-2540 ICC is comprised of three sections: the VMEbus slave DTB interface which arbitrates for the local CPU resources, the CPU with firmware and support logic, and the circuitry which implements the measurement and control functions. The block diagram of the VMIVME-2540 ICC is shown in Figure 1.

Ordering Options								
January 24, 1999 800-002540-000 J	A	B	C	–	D	E	F	
VMIVME-2540	–		0	0	–			

A = Interface Options
0 = 4 Channels
1 = 8 Channels
2 = 16 Channels
3 = 24 Channels
BC = 00 (Options reserved for future use)

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com
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The ICC counter circuitry consists of six programmable System Timing Controllers (STCs). Each STC provides the ICC with four high-speed counter/waveform synthesis interfaces, giving the VMIVME-2540 twenty-four channels of digital measurement and control. The STC counters may be configured individually or in groups of up to four to implement the various measurement and control functions. The on-board 68HC000 CPU configures and manages each STC interface directly, allowing the VMEbus host interface to be elevated above the hardware level. Ordering options allow the VMIVME-2540 to be factory configured with 1, 2, 4, or 6 System Timing Controllers. The inputs and outputs of the System Timing Controllers are buffered at the front panel connectors with RS-422 line receivers and line drivers. TTL input signal compatibility is supported by connecting the inverting input of the RS-422 line receiver to an on-board 1.4 V reference through the front panel, and the TTL signal to the noninverting input.

The user interface of the Intelligent Counter/Controller is implemented by a 15 MHz 68HC000 CPU supported by 64 Kbyte of EPROM firmware, 128 Kbyte of zero-wait-state static RAM, and highly-integrated control and interrupt logic. The VMEbus host programs the ICC by queueing function control blocks in local memory and issuing commands. The CPU responds to the commands by interpreting the function control blocks, configuring the system timing controllers, and then acknowledging the host command. Once configured, the CPU maintains data structures of measurement data in local memory and interrupts the VMEbus host when a measurement or control process is complete.

The slave VMEbus interface of the VMIVME-2540 locates the 64 Kbyte VMEbus local memory window in A32 or A24 address space with DIP switches, with nonprivileged and/or Supervisory access. The VMEbus host must arbitrate with the 68HC000 CPU for local bus access since the RAM is shared. The data accesses may be D32, D24, D16, and D08, and unaligned transfers are supported. Because the local CPU executes its code from RAM, the arbiter relinquishes control of the local resources after a single VMEbus data transfer.

The Intelligent Counter/Controller supports two VMEbus interrupter modules which may assert any of two IRQ levels simultaneously. When serviced, the interrupter modules respond with an 8-bit interrupt vector and automatically clear the pending IRQ. The CPU maintains a queue of pending interrupt events in memory, writing a new IRQ to the interrupter modules when the previous event is cleared.

FUNCTIONAL SPECIFICATIONS

System Time Base: 5 MHz

Accuracy/Stability: ±0.005 percent

EVENT COUNTING

Input Frequency Range: Up to 2.5 MHz

Count Range Returned: Up to 2^{16} (word mode) Up to 2^{32} (long mode)

PERIOD/PULSE-WIDTH MEASUREMENT

Input Period Range/Accuracy

16-bit Counter: 131.07 s to 400 ns

131 s to 13.1 ms Accuracy: 0.015 percent maximum

13.1 ms to 200 ns Accuracy: Percent Error = 100*(200 ns/Period)

16-bit Enhanced-Resolution Counter: 858.9 s to 800 ns

Requires two 16-bit counters

32-bit Integer Operations: Requires two 16-bit counters for pulse-width operation

Requires three 16-bit counters for period measurement operation

16-bit Prescaler Range: ÷2-65536 with 400 ns resolution

FREQUENCY MEASUREMENT

Input Frequency Range/Accuracy

16-bit Counter: 0.0076 Hz to 2.5 MHz

0.007 to 76 Hz Accuracy: 0.015 percent maximum

76 Hz to 2.5 MHz Accuracy: Percent Error = 100* (Frequency/5 MHz)

16-bit Enhanced-Resolution Counter: 0.001 Hz to 1.25 MHz

Requires two 16-bit counters

16-bit Prescaler Range: ÷2-65536 with 2.5 MHz maximum clock rate

PERIOD/PULSE TRAIN GENERATION

Pulse Repetition Rate: 0.0038 Hz to 2.5 MHz

Period Range: 262.1 s to 400 ns

Pulse-Width Range: 131 s to 200 ns

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Pulse-Width Resolution (for Nonsquare Wave):

131 s to 13.1 ms: 0.015 percent maximum

13.1 ms to 200 ns: Percent Error = 100* (200 ns/Pulse Width)

PERIODIC VMEbus INTERRUPT GENERATION

VMEbus IRQ Levels/Vectors: IRQ1 to IRQ7, 8-bit vector

IRQ Repetition Rate: 0.0076 to 1,000 Hz

QUADRATURE POSITION MEASUREMENT

Sin/Cos Input Range: DC to 1 MHz

Accuracy: ±1/4 wave/5 MHz sample rate
Requires two channels per Encoder

PHYSICAL SPECIFICATIONS

Power Requirements: +5 V ± 5/-2.5 percent
4.25 A typical
5 A maximum

INPUT BUFFER SPECIFICATIONS

Common-Mode Voltage Limit: ±25 V

Differential Mode Voltage Limit: ±5 V
The differential voltage range is limited to ±5 V due to a 1/4 W, 120 Ω termination resistor

V_{IH}/V_{IL} Differential Mode: RS-422-compliant differential input

V_{IH}: Occurs whenever the primary (positive) input voltage is 100 mV greater than the differential (negative) input voltage within the common-mode voltage range of ±25 V.

V_{IL}: Occurs whenever the primary (positive) input voltage is 100 mV less than the differential (negative) input voltage within the common-mode voltage range of ±25 V.

V_{IH}/V_{IL} Unipolar (Single-Ended) Mode (Differential Input Connected to V_{TTL}):

$V_{IH} = V_{TTL} + 100$ mV

$V_{IL} = V_{TTL} - 100$ mV

Input Hysteresis: 50 mV

Input Rise Time Recommendations:
Minimum rise time - 5 ns
Propagation delay - 25 ns typical
Maximum rise time - 1 ms

The AM26LS33A differential receivers used on the VMIVME-2540 are capable of accepting inputs that vary greatly on voltage and time domain. Care must be taken to ensure that the input voltages are stable around V_{TTL} when in single-ended mode or spurious data will be produced. Similarly, when using differential inputs, care must be taken to ensure that the inputs, are not allowed to float with voltage values within 100 mV of each other or data transitions may be generated.

OUTPUT BUFFER SPECIFICATIONS

AM26LS31

Short Circuit Current: I_{SC} = -60 mA typical

Differential Output Voltage: $|V_t| = 2$ V minimum

TEMPERATURE

Operating: 0 to 65 ˚C

Nonoperating: -40 to 85 ˚C

Humidity: 5 to 95 percent RH noncondensing
ANSI/IEEE 1014-1987 IEC 821 and 297

VMEbus COMPLIANCE

A32/D32 DTB Slave
Base address selectable on 64 Kbyte boundaries
Supervisory/Nonprivileged Address Modifier Codes
Dual Interrupter Modules assert any of IRQ1 to IRQ7
Board size 160 x 233.4 mm

INTERFACE: DISCRETE WIRE CONNECTORS AND TERMINAL BLOCKS — The VMIVME-2540 has a large amount of front panel I/O which must be broken out by cabling and possibly rack-mounted terminal blocks. If the user wishes to use discrete wire connectors and cables, the suggested manufacturer is Harting Elektronik, Inc., 2155 Stonington Ave., Suite 212, P.O. Box 95710, Hoffman Estates, Illinois 60195-0710, (312) 519-7700. The recommended connector components for cabling to P3 and P4 are given in the table below.

Recommended Discrete Wire Connectors and Accessories

Component	Harting Catalog No.
96-pin Discrete Wire Connector	0903-096-3214
Female Crimp Contacts	0902-000-8484
Connector Shell Housing	0903-096-0501
Left Locking Lever	0902-000-9902
Right Locking Lever	0902-000--9903

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The RS-422 differential signals should be connected by twisted pair insulated wires, 24 AWG solid or stranded-copper conductors (R < 30 Ω/ 1,000 ft for other conductors), with a maximum cable length of 4,000 feet. Care should be taken to ensure that each signal group is properly grounded for reliable operation.

TTL signals may be connected by flat 96-conductor ribbon cable, 30 AWG insulated copper-stranded conductor. The corresponding female 96-pin DIN connector for flat-ribbon cable is ERNI 913.031 or similar. It is recommended that the total cable length be 50 feet or less for the TTL application with attention given to maximum signal transition rate and signal degradation over distance. RS-422 differential interface is clearly superior for longer cable lengths.

If the user wishes the I/O signals from the VMIVME-2540 front panel to be broken out at terminal blocks, the VMIACC-BT04 Dual 96-pin Transition Panel is suggested. The VMIACC-BT04 is a 19-inch rack-mountable panel which breaks all 192 signals out from two DIN 96-pin connectors to standard terminal blocks. Connection between the VMIACC-BT04 and the VMIVME-2540 front panel is made by 96-conductor ribbon cables, three foot length recommended.

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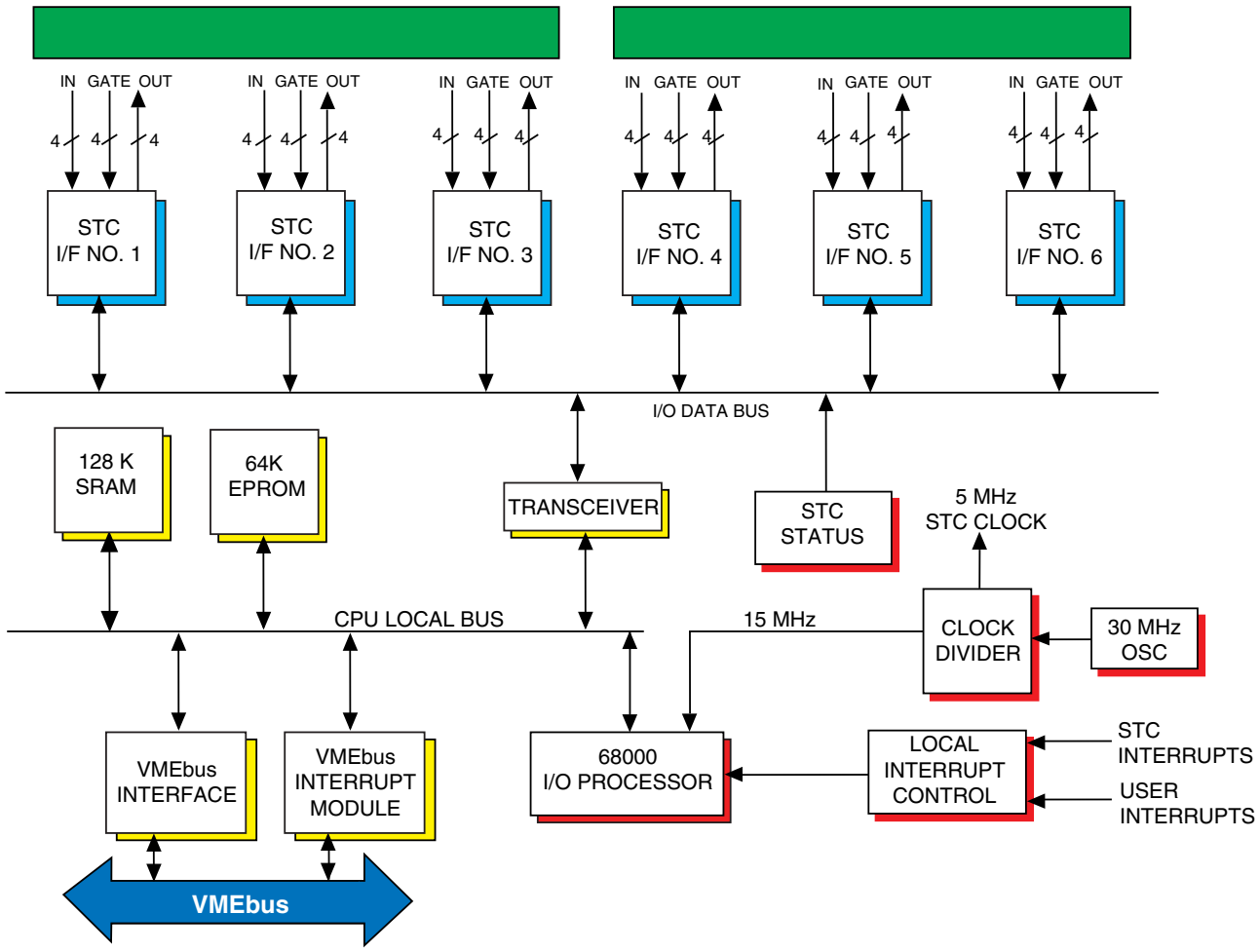


Figure 1. Intelligent Counter/Controller Block Diagram

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