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VMIVME-3100

16-CHANNEL 12-bit ANALOG-TO-DIGITAL CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-003100-000 U

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Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

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The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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VMIVME-3100
16-CHANNEL 12-bit ANALOG-TO-DIGITAL CONVERTER BOARD

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-3100 12-bit Analog-to-Digital Converter (ADC) Board is a medium performance 12-bit ADC board that is designed to support 16 single-ended or 8 differential front-panel analog inputs and a variety of multiplexer expansion boards. The multiplexer expansion boards utilize an AMXbus™ for routing analog signals from the multiplexer inputs to the VMIVME-3100 ADC Board. The VMIVME-3100 ADC Board also features Built-in-Test functions, and a front panel Fail LED provides the user with the capability of fault detection and isolation. A photograph of the VMIVME-3100 ADC Board is shown in Figure 1.1-1.

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-3100 ADC Board features the following:

a. On-board Built-in-Test logic for fault detection and isolation.
b. Front panel Fail LED.
c. 12-bit resolution.
d. On-board precision voltage sources (on-board self-test support).
e. User selectable for one ADC per slot, or one ADC and slaved MUX board.
f. 9 µsec maximum conversion time.
g. 9 µsec acquisition time*.
h. 16-channel single-ended multiplexer.
i. 8-channel differential input option.
j. Dedicated multiplexer input for testing VMIC's analog output boards.
k. Dedicated multiplexer input for economical expansion of analog inputs.
l. Overvoltage protected inputs.
m. Individually coded/keyed VME connectors.
n. Double Eurocard form factor.
o. Fail-Safe with power OFF.

*Acquisition time is selectable as a function of full-scale input voltage (refer to page 3-2, Table 3.1.2-1 for details).

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M3100/F1.1-1

Figure 1.1-1. VMIVME-3100 ADC Board

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The unique features of the VMIVME-3100 ADC Board are the Built-in-Test logic and the AMXbus™ support, which is a VMIC analog bus that enables different types of analog I/O boards to functionally interconnect. A functional block diagram of the interconnect scheme is shown in Figure 1.2-1. The primary purpose is to allow high density, low cost analog input expansion by connecting up to 16 of VMIC's wide variety of multiplexer boards to one ADC board.

The AMXbus™ also supports testing of a subset of VMIC's analog output boards. Analog outputs may be switched via program control to the AMXbus™ to route the signal to the VMIVME-3100 ADC to be digitized and compared with the original data that was converted by the analog output board. Utilizing this technique, a subset of VMIC's products support real-time and off-line fault detection and isolation.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based in VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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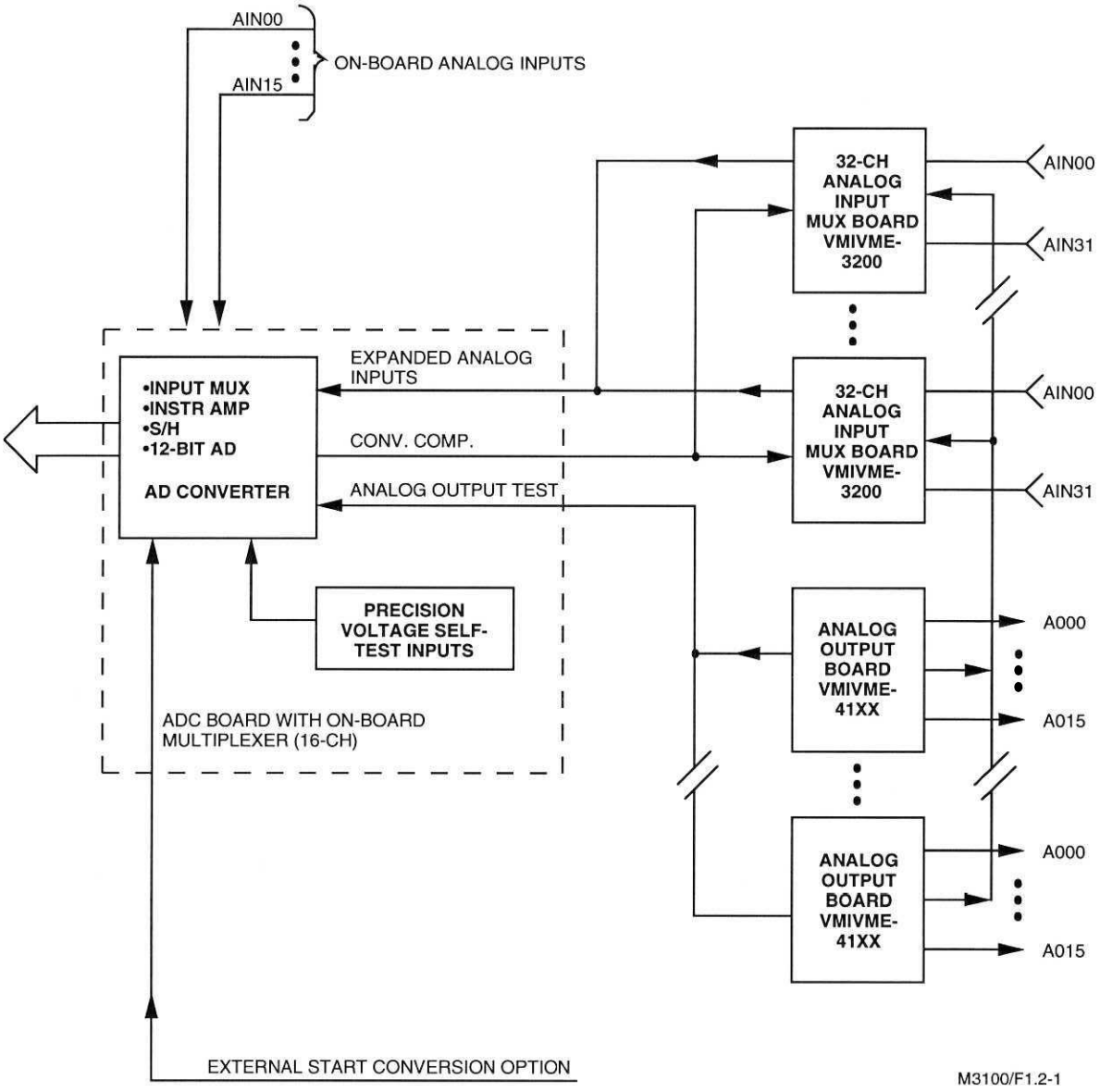


Figure 1.2-1. Functional Block Diagram of the AMXbus™ Interconnect Scheme

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The reader should refer to the following VMIC documents for a thorough understanding of the Built-in-Test capabilities and subsystem configurations:

(VMIVME-) MODEL NO.	TITLE	VMIC DOCUMENT NO.
3200	32-Channel Analog Input Multiplexer Board	500-003200-000
3210	64-Channel Analog Input Multiplexer Board	500-003210-000
4500	16-Channel Analog I/O 12-Bit Digital-to-Analog (DA) (S/H) Outputs (16 Channels) Input Multiplexer(16 Channels)	500-004500-000
4100	16-Channel 12-Bit Digital-to-Analog Converter Board (DAC)	500-004100-000
4116	8-Channel 16-Bit Digital-to-Analog Converter Board (DAC)	500-004116-000
4105	8-Channel 12-Bit Multiplying Digital-to-Analog Converter Board (DAC)	500-004105-000

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003100-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3100 Analog-to-Digital Converter (ADC) Board is designed to support single-ended and differential inputs. The VMIVME-3100 also offers a low cost data acquisition system with superior performance and reliability. The VMIVME-3100 ADC converter board may be manufactured with a variety of options, as shown by the ordering information guide. Acquisition and conversion time combined without the expansion multiplexers is approximately 20 µsec maximum, giving a maximum throughput rate of approximately 50 kHz (for high-level inputs). Output coding is straight binary, offset binary, or two's complement.

The successive approximation ADC board circuitry includes a built-in multiplexer, a programmable gain instrumentation amplifier, and a sample-and-hold circuit. The instrumentation amplifier is programmed with a single resistor for gains of 1 to 1,000. This key feature is useful in low-level signal applications involving bridge amplifiers, transducers, strain gage, and thermocouple interfaces.

3.1.1 Protection

The 16 front panel analog inputs are overvoltage protected. Protection is assured to 20 V beyond the ±15 V supply voltages. With the +15 V power ON, the maximum input voltage range is ±35 V. If the power supply is OFF, the maximum input voltage is ±20 V.

3.1.2 Analog-to-Digital (A/D) Throughput

The throughput time for operation with front panel inputs is the sum of the amplifier settling time (acquisition time) and the A/D conversion time. The A/D conversion time is 9 µsec. The amplifier settling time is a function of the input voltage range and the gain setting. When the gain exceeds 10, the amplifier needs more than the allotted 9 µsec for settling to within 12-bit accuracy. Even though the signal inputs may change slowly, the amplifier must have enough time to settle fully in response to the abrupt change before a conversion takes place.

Table 3.1.2-1 provides a matrix of throughput as a function of input voltage ranges and gain settings.

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Table 3.1.2-1. Input Range Parameters (Typical)

INPUT RANGE	GAIN	RGAIN (Ω)	AMPLIFIER SETTLING TIME	RDELAY (Ω)	THROUGHPUT	SYSTEM ACCURACY
±10 V	1	NONE	9 µsec	NONE	55.5 kHz	0.009%
±5 V	2	20.0 K	9 µsec	NONE	55.5 kHz	0.009%
±2.5 V	4	6.667 K	9 µsec	NONE	55.5 kHz	0.009%
±1 V	10	2.222 K	9 µsec	NONE	55.5 kHz	0.009%
±200 mV	50	408.2	16 µsec	7 K	40.0 kHz	0.010%
±100 mV	100	202.0	30 µsec	21 K	25.6 kHz	0.011%
±50 mV	200	100.5	60 µsec	51 K	14.5 kHz	0.016%
±20 mV	500	40.08	144 µsec	135 K	6.5 kHz	0.035%
±10 mV	1000	20.02	288 µsec	279 K	3.3 kHz	0.069%

M3100/T3.1.2-1

3.1.3 System Throughput

The VMIVME-3100 supports a wide variety of multiplexer expansion boards that affect the total system throughput. The total system throughput may be calculated from the information given in Table 3.1.3-1 using the formula as shown below:

$$F_S = \frac{1}{N\,(T_1 + T_2 + T_3)}$$ Samples per second, where

N is the number of channels
T_1 is the remote multiplexer acquisition time
T_2 is the VMIVME-3100 amplifier settling time
T_3 is the VMIVME-3100 ADC conversion time

A wide variety of multiplexer expansion boards are supported by the VMIVME-3100 ADC Board. An analog expansion bus (AMXbus™) is available as a standard product to support the low-cost expansion concept. A list of multiplexer expansion products is provided in Table 3.1.3-2.

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Table 3.1.3-1. System Throughput with Expansion Multiplexers

GAIN	T_1	T_2	T_3
1	X	9 µs	9 µs
2	X	9 µs	9 µs
4	X	9 µs	9 µs
10	X	9 µs	9 µs
50	X	16 µs	9 µs
100	X	30 µs	9 µs
200	X	60 µs	9 µs
500	X	144 µs	9 µs
1000	X	288 µs	9 µs

M3100/T3.1.3-1

T_1 is a variable available on each multiplexer expansion board data sheet.

Table 3.1.3-2. Multiplexer Expansion Products

MODEL NO. (VMIVME-)	DESCRIPTION	AVAILABILITY
3200	32S/16D MUX with Built-in-Test	Now
3210	64S/32D MUX with Current Sense Option	Now
3220	8-Channel Thermocouple MUX	Now
3230	8-Channel RTD/Strain Gage MUX	Now
4500	16 Single-Ended MUX with 16 Analog Outputs	Now
A05	5-Slot P2 Analog Backplane	Now
A09	9-Slot P2 Analog Backplane	Now
A19	19-Slot P2 Analog Backplane	Now

M3100/T3.1.3-2

3.1.4 Built-in-Test

The VMIVME-3100 Board supports a wide variety of VMIC's analog I/O products that are designed to support fault-detection and isolation to the board level. The VMIVME-3100 employs an internal voltage divider to support testing the VMIVME-3100 as a stand-alone board. The VMIVME-3100 also contains a dedicated input test multiplexer that supports loop-back testing of a variety of VMIC's analog output boards. A summary of analog output products that support this loopback concept is shown in Table 3.1.4-1.

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Table 3.1.4-1. Analog Output Products with Built-in-Test

MODEL NO. (VMIVME-)	DESCRIPTION
4100	16-Channel, 12-Bit DAC
4105	8-Channel, 12-Bit Multiplying
4116	8-Channel, 16-Bit DAC
4500	16-Channel, 12-Bit DAC, Dual Port Memory, 16 S/H Outputs and 16 Single-Ended Analog Input Multiplexers Channels

M3100/T3.1.4-1

3.2 NORMAL MODE OPERATION

In the normal operating mode, the analog signal may be received by either the front panel P3 connector or via the AMXbus™ (P2 connector). The AMXbus™ supports a wide variety of multiplexer expansion boards.

3.2.1 Front Panel Inputs (P3 Connector)

The VMIVME-3100 ADC supports eight differential or 16 single-ended analog inputs via the front panel. Differential inputs require an optional ADC module (HDAS-8) that must be installed at the factory and specified by the ordering code as shown in Section 2. In the single-ended mode, each of the 16 inputs are designed with an associated ground signal to support reliable operation in noisy environments by utilizing twisted pairs for incoming signals. A wide variety of low-pass filter options are available as shown in Figure 3.2.1-1. Low pass filters are available to support 3dB attenuation at 6, 9, or 32 Hz.

3.2.2 AMXbus™ Operation

The AMXbus™ and compatible AIO boards are designed to support up to 16 analog input multiplexers connected to one ADC as shown in Figure 3.2.2-1. AMXbus™ backplanes are available from VMIC in a wide variety of configurations. The VMIC AMXbus™ also supports Built-in-Test functions associated with VMIC's Analog I/O BITMODULES™.

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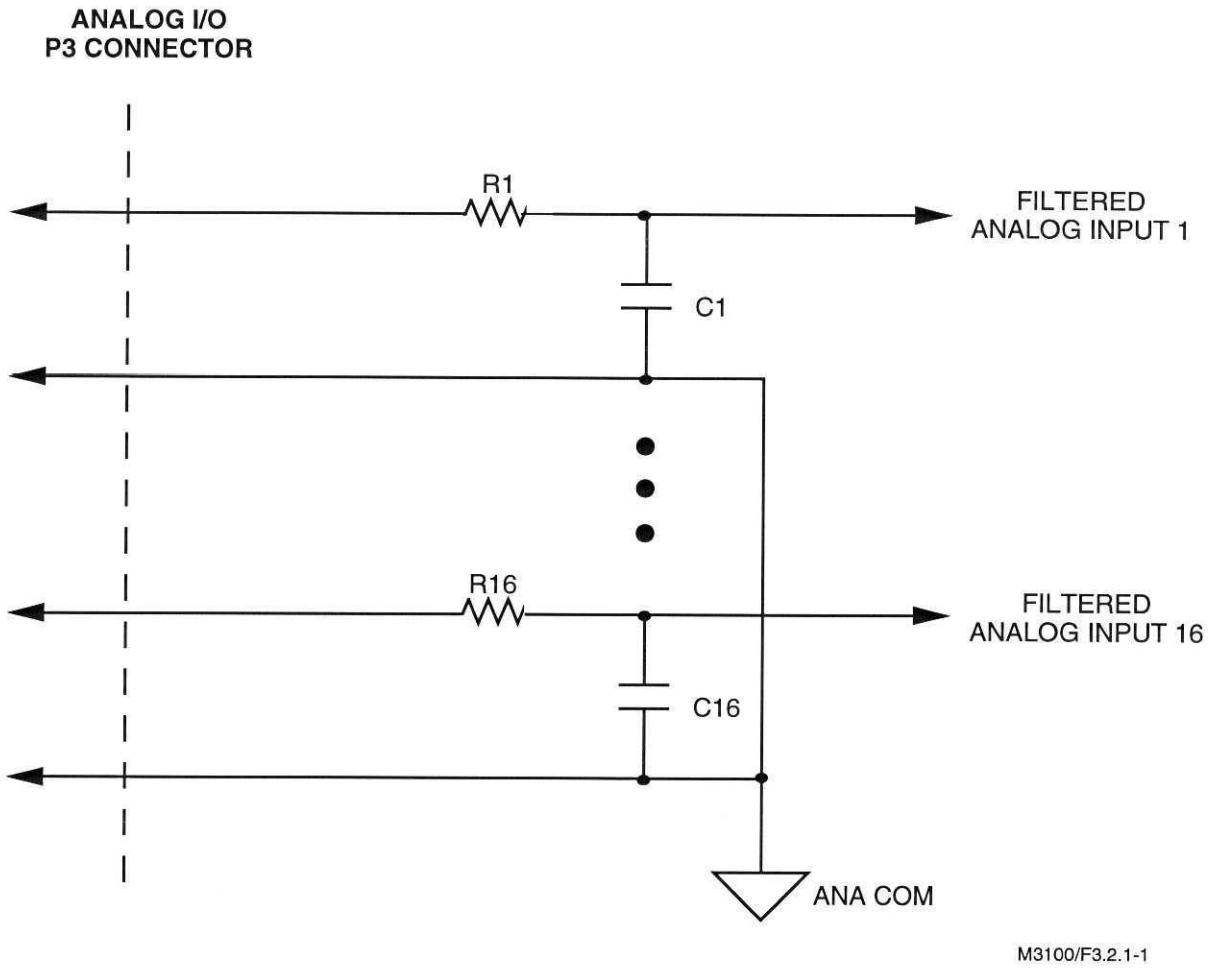


Figure 3.2.1-1. 16-Channel Single-Ended Filtered Analog Inputs

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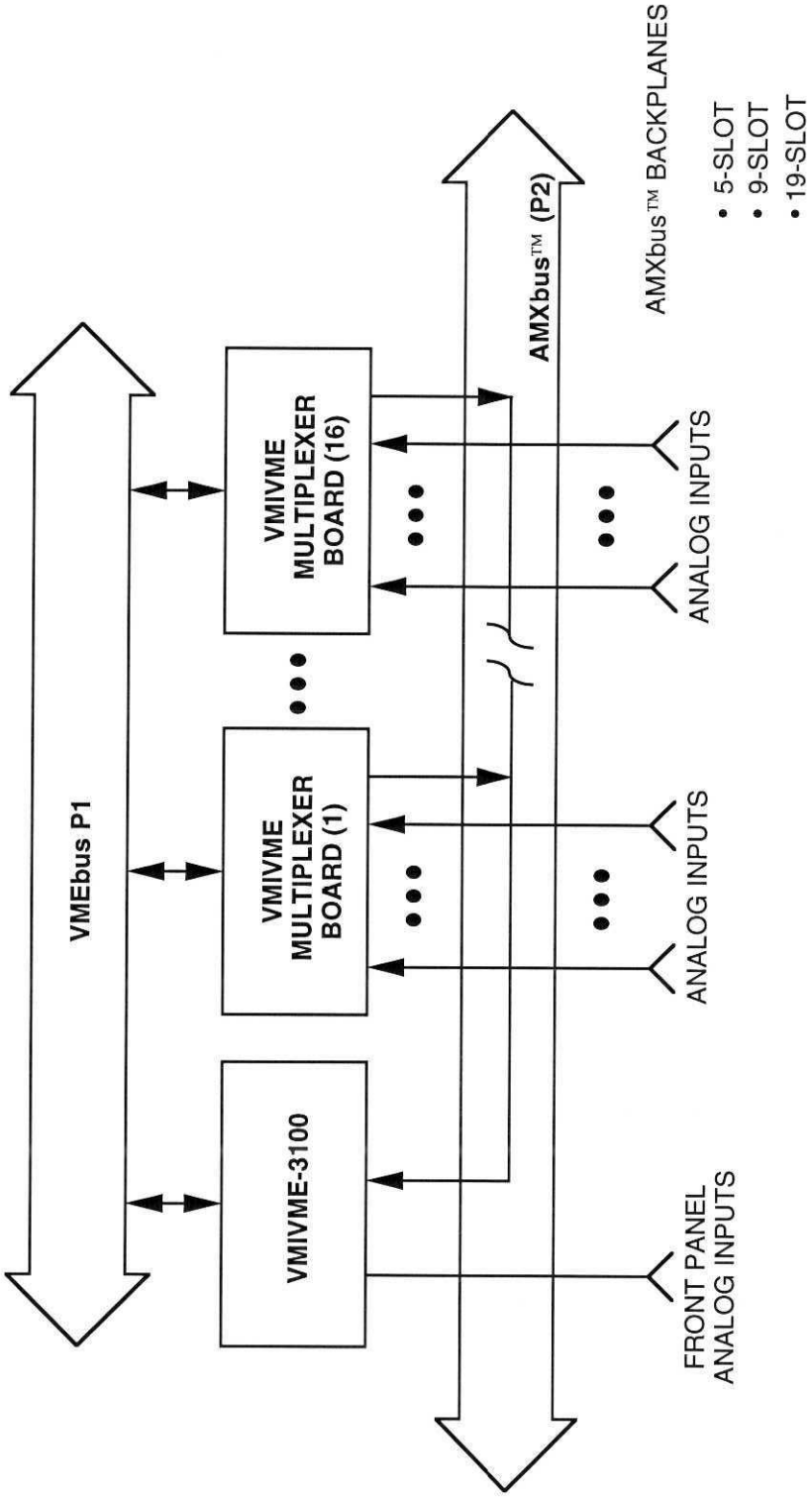


Figure 3.2.2-1. VMIVME-3100 Typical Configuration with Multiplexer Expansion

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Figure 3.2.2-2 shows the three dedicated analog bus lines that interconnect a multiplexer board with the ADC board. Signal EXMUXHIBUS (Expansion MUX High Bus) and GND SEN (Ground Sense) support single-ended analog inputs. The GND SEN line senses the analog ground at the multiplexer board to reduce common-mode errors due to different ground potentials. Signals EXMUXHIBUS and EXMUXLOBUS (Expansion MUX Low Bus) support differential inputs from a wide variety of multiplexer boards.

Figure 3.2.2-3 depicts a configuration that supports 512 single-ended inputs via 16 VMIVME-3200 multiplexer boards. The ADC board supports these boards via the expansion capability of the AMXbus™. The P3 connector at the ADC board can receive 16 additional analog inputs, providing a system total of 528 inputs maximum per one ADC board. The VMIVME-3210 64-Channel Multiplexer Board can effectively double the input capacity to 1,040 single-ended or 512 differential analog inputs. The VMIVME-3200 supports self-testing of all 32 channels via a dedicated test output from a VMIVME-41XX Digital-to-Analog Converter (DAC) board that is connected on the same AMXbus™. VMIC has developed other multiplexer boards that are compatible with the ADC board and the AMXbus™, including low-level input multiplexers, RTD/STRAIN gage, and thermocouple input multiplexers.

The general sequence to control the system, as shown in Figure 3.2.2-3, is as follows: first, the CPU board selects a single channel on one of the multiplexer boards. The selected analog signal is then routed to the P2 connector to the expansion bus lines of the AMXbus™.

The CPU board writes a control word to the ADC board to begin conversion. When conversion is completed, the end-of-conversion signal from the ADC board removes the signal from the AMXbus™ and the sequence may be continued.

3.2.3 External Trigger Input

An external TTL compatible signal may be used to initiate an ADC conversion. The external trigger conversion circuitry is enabled by setting a bit in the control word that enables the receipt of a (200 nsec/minute, active low) pulse which will initiate the ADC conversion. The AMXbus™ backplane has a wirewrap pin to which the trigger may be connected.

3.3 BUILT-IN-TEST MODES

The VMIVME-3100 ADC Board contains special Built-in-Test logic that may be used for off-line or on-line fault detection and isolation. The VMIVME-3100 ADC supports fault detection and isolation (via the AMXbus™) of a wide variety of VMIC Analog Input/Output (AIO) boards.

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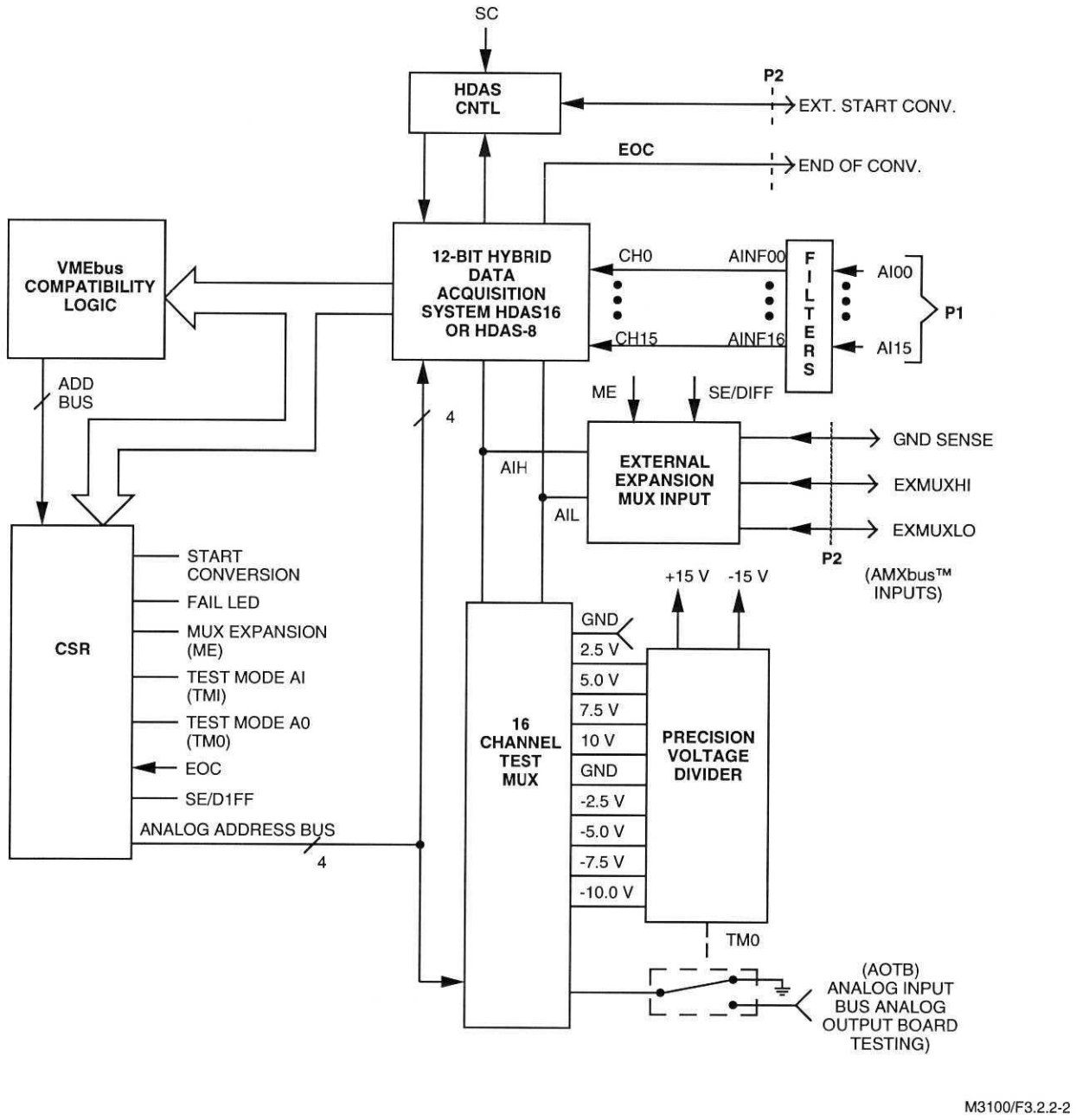


Figure 3.2.2-2. VMIVME-3100 Functional Block Diagram

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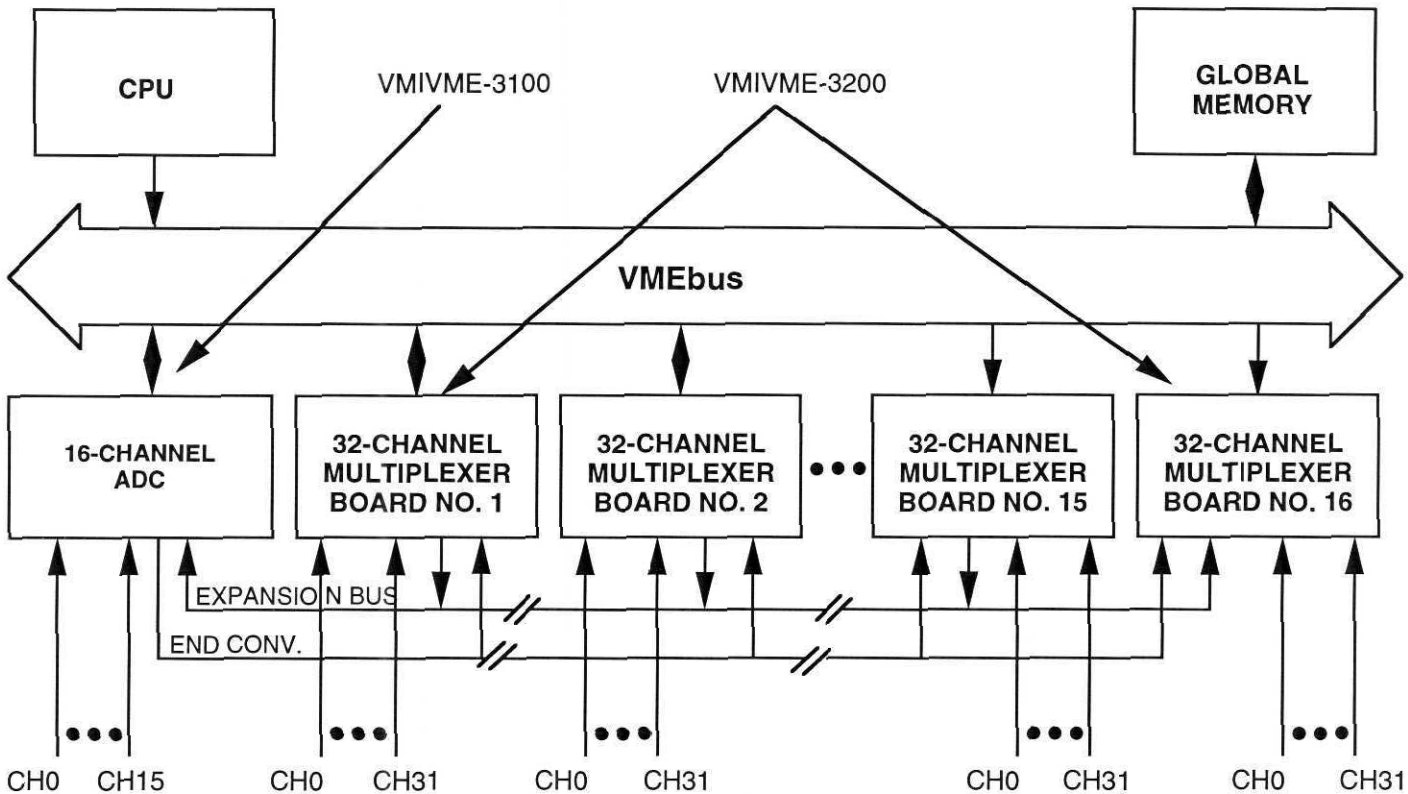


Figure 3.2.2-3. VMIC High Performance Analog Input Configuration

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3.3.1 ADC Board Built-in-Test

The ADC board contains a Control and Status Register (CSR) that is utilized to select certain operation modes. The CSR is a *write/read* register. The user may verify the functional operation of D0 - D14 of the VMIVME-3100 VMEbus logic by utilizing the write/read capability of the CSR, utilizing D15 to select the CSR and using bits D0 - D14 for verification.

The VMIVME-3100 Board contains nine precision voltage sources (-10.000 V, -7.500 V, -5.000 V, -2.500 V, 0.000 V, +2.500 V, +5.000 V, +7.500 V, +10.000 V) that may be selected by user test subroutines to verify correct board operation and accuracy. These precision voltages may also be used to calibrate the VMIVME-3100, if necessary.

3.3.2 Using the VMIVME-3100 to Verify Operation of the VMIVME-41XX and VMIVME-32XX Boards

The AMXbus™ allows interconnection of these three board types to perform analog output (VMIVME-41XX) to analog input (VMIVME-32XX and VMIVME-3100) wrapback testing. The basic test premise is that a digital word is written to a DAC channel (analog output) of the VMIVME-41XX, which is multiplexed on the AMXbus™ to the VMIVME-32XX Multiplexer Board (this is Test Bus 1 shown on Figure 3.3.2-1) or directly to the ADC board (this is Test Bus 2 shown in Figure 3.3.2-1). Test Bus 1 is used to test the input channels of the Multiplexer Board. Test Bus 2 is used to test the analog outputs of the VMIVME-41XX Board. Test Bus 2 is routed directly to the ADC board where, under program control, the analog signal is converted back to a 12-bit word, read by the CPU, and compared to the original 12-bit word written to the VMIVME-41XX. Test Bus 1 is routed through a selected MUX channel to the ADC board via the AMXbus™ for conversion (Figure 3.2.2-3).

3.3.3 Fault Detection and Isolation Using the VMIVME-3100 and VMIVME-4500

A typical system configuration using these products is shown in Figure 3.3.3-1. The VMIVME-4500 is a low-cost, 16-channel, analog output board with 16 channels of single-ended analog multiplexer inputs that require a VMIVME-31XX Series ADC and VMIC's AMXbus™ for processing. The VMIVME-4500 Board is designed to support real-time and off-line fault detection and isolation. The analog outputs may be disconnected from the user device via program control to support worst-case off-line board level testing. Each analog output may be multiplexed under program control via the AMXbus™ to a VMIVME-31XX Series ADC to be digitized.

3.4 VMEbus INTERFACE DESCRIPTION

The VMEbus interface (Figure 3.4-1) contains the necessary logic to interface a slave board (VMIVME-3100) to the VMEbus. The VMIVME-3100 is memory mapped in the VMEbus short I/O address space. During a *write* cycle to

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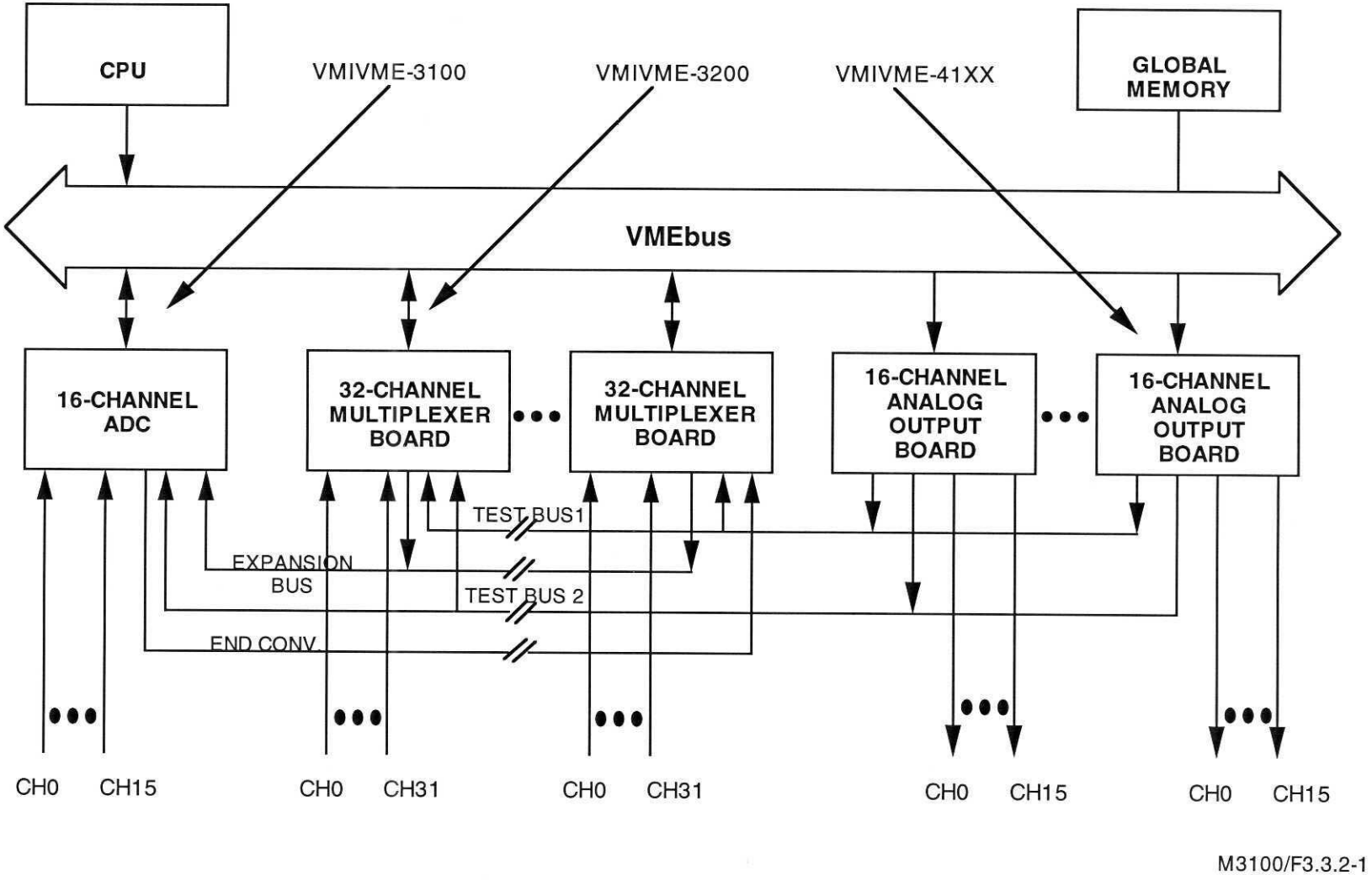


Figure 3.3.2-1. VMIC High Performance Analog Input/Output Configuration

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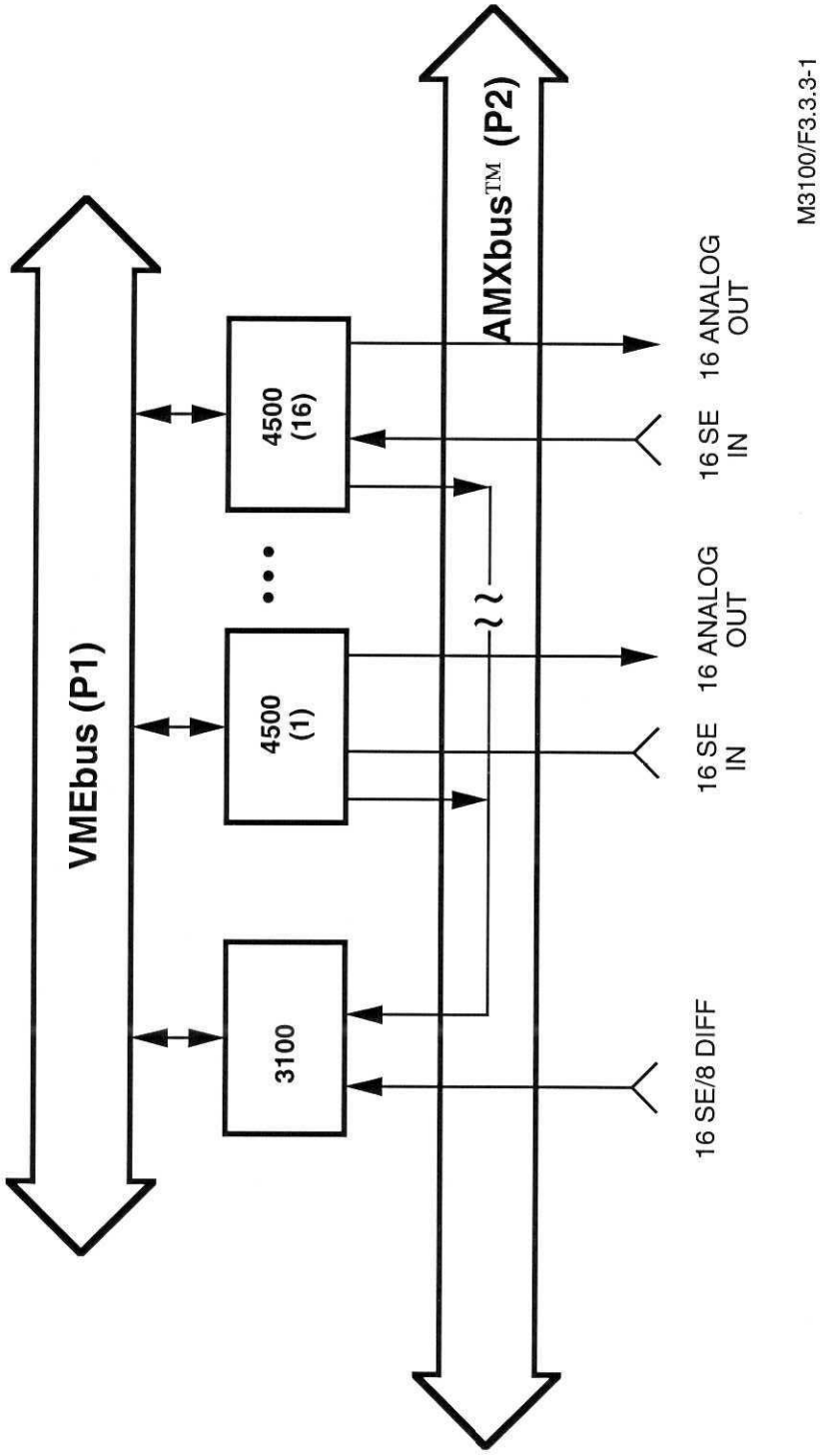


Figure 3.3.3-1. Typical Low Cost AIO Subsystem with Built-in-Test

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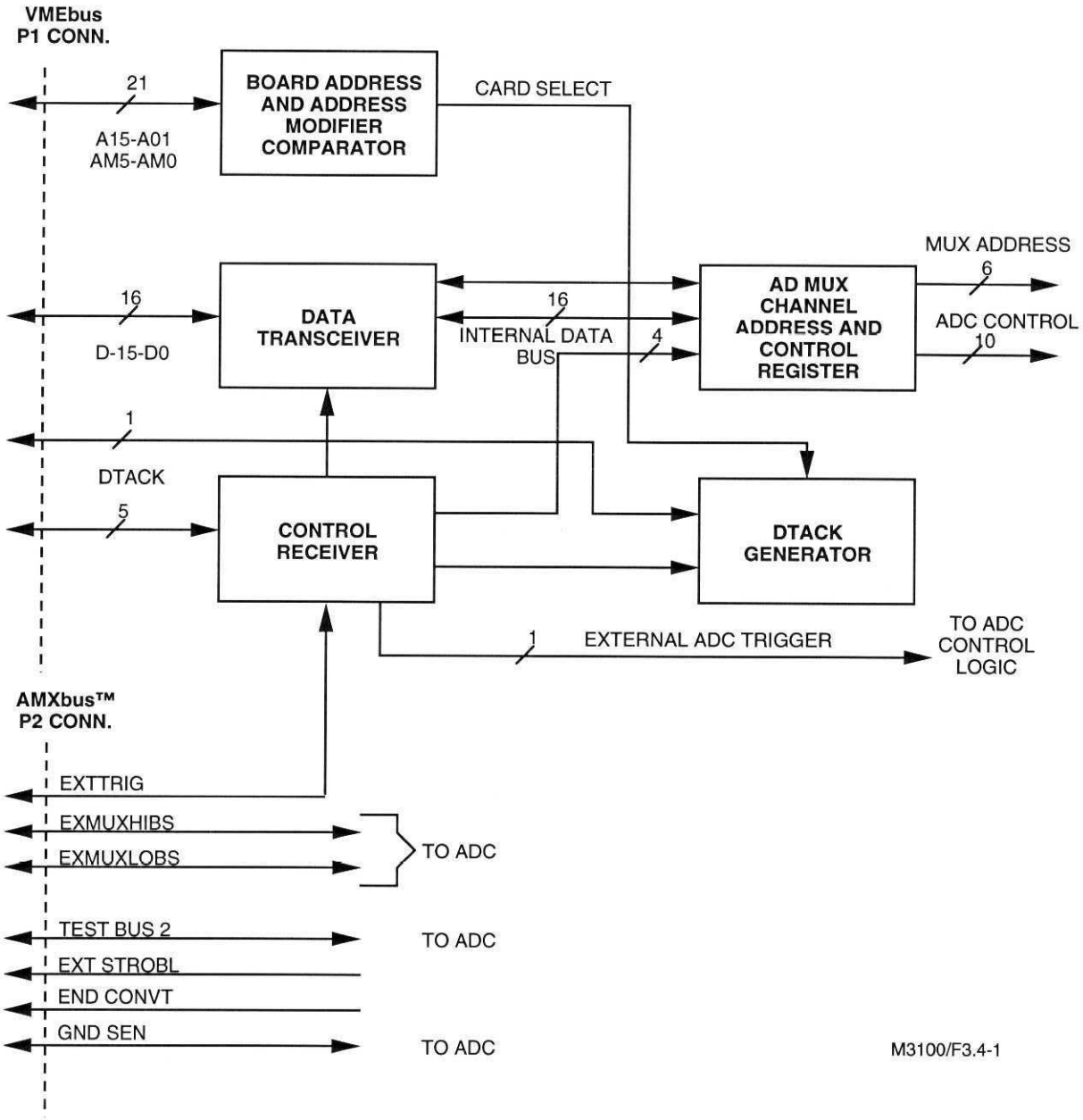


Figure 3.4-1. VMEbus Interface Logic and Interface Signals

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the board address, bits A01 through A15 are compared with the previously selected board address. The board address is selected by DIP switches. If the address compares, then a board select signal is generated. This signal, along with the control signals received at the board, gates the data (D0 to D15) to the CSR on the VMIVME-3100.

The VMIVME-3100 circuitry requires +5 V, +15 V, and -15 V. The +5 V is supplied to the board via the P1 and P2 connectors. An on-board DC-to-DC converter (Figure 3.4-2) generates the +15 V and -15 V for the analog circuitry.

3.5 P2 CONNECTOR I/O SIGNAL DEFINITION (AMXbus™) SIGNALS

a. AOTESTBS (Test Bus 2) - P2 Connector, Pin A19. An analog test bus from the VMIVME-41XX board, used in conjunction with the VMIVME-3100 ADC Board to verify the analog outputs of the DAC boards.

b. EXMUXHIBS - P2 Connector, Pin A13. The high signal of a pseudo-differential or differential input to the ADC board from an external multiplexer board.

c. EXMUXLOBS - P2 Connector, Pin A11. The low signal of a differential input to the ADC board from an external multiplexer board.

d. GNDSEN - P2 Connector, Pin A15. The low signal of a pseudo-differential input to the ADC board from an external multiplexer board.

e. EXTTRIG - P2 Connector, Pin A27. External trigger input, when received active low from an external device, intiates an ADC conversion. The signal must be TTL compatible and be valid low for a minimum of 200 ns before returning to a TTL high state.

f. EXTSTROBL - P2 Connector, Pin A31. When the ADC board control word is loaded to enable external trigger mode, a 100 ns active low pulse is output on this pin to indicate that the external trigger input is enabled. This signal does not have to be monitored by the user.

g. ENDCONVT - P2 Connector, Pin A29. This signal is generated by the ADC board to indicate an ADC end-of-conversion. Any multiplexer board on the AMXbus™ backplane will remove its analog output from the AMXbus™ backplane upon receipt of this signal.

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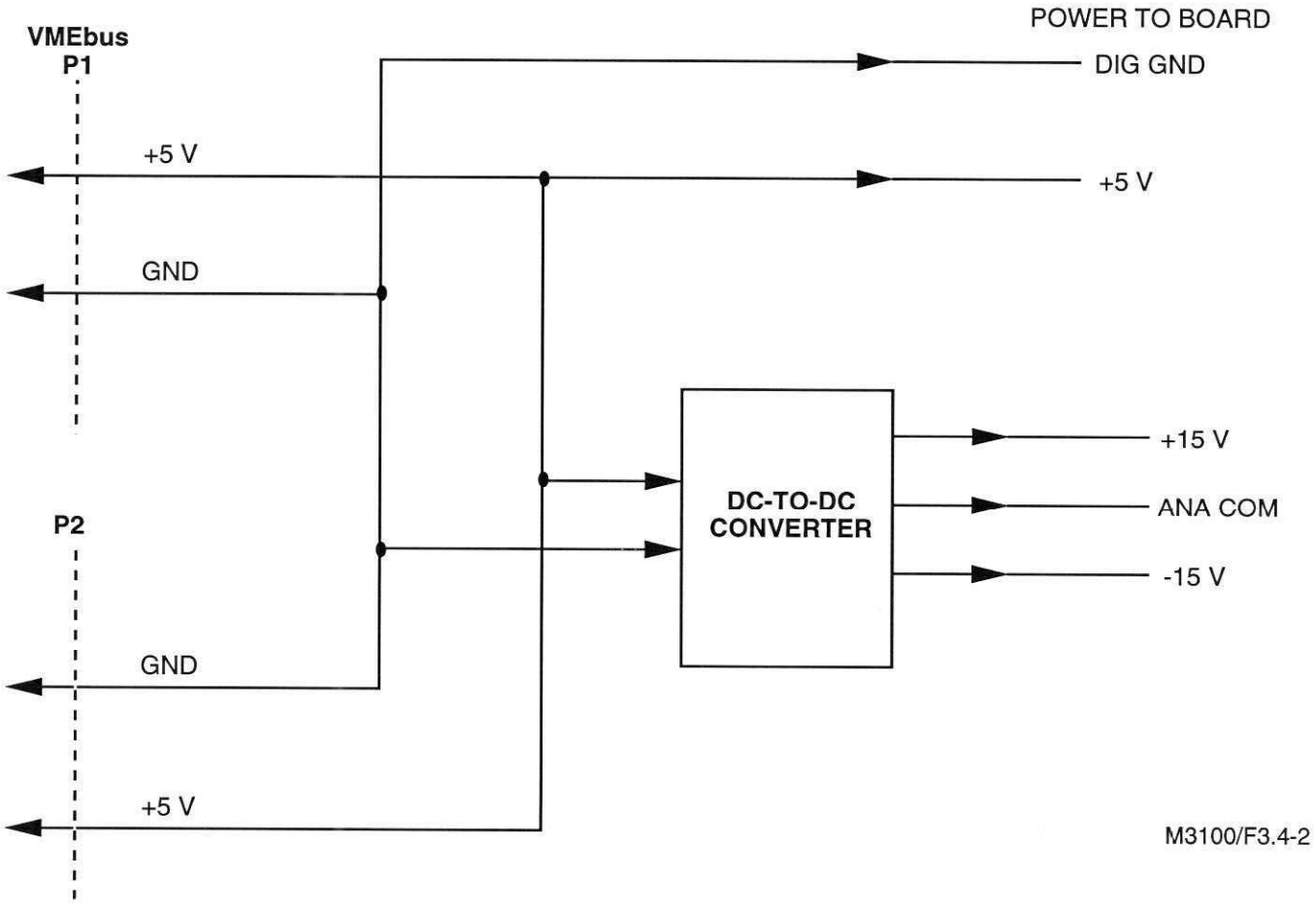


Figure 3.4-2. ADC Board Power

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The Analog-to-Digital (ADC) board is memory mapped in the VME short I/O address space and occupies only one word location within the VME short I/O address space of 65,535 bytes. The board address is selected by DIP switches, as shown in Section 5.5. The short I/O space is mapped from FF0000 (HEX) to FFFFFF (HEX). The ADC data register, which contains the 12 bits of converted digital data is a *read only* register. The Control Status Register (CSR) is a read/write register and is used for board control. The CSR access and the ADC end-of-conversion register access is selected by data bit D15 because both of these registers use the same address.

4.2 CONTROL STATUS REGISTER DESCRIPTION

The programming of the Control Status Register (CSR) selects the operational mode of the board. The CSR is a 16-bit *read/write* register. To initiate an AD conversion, data bit D6 in the CSR is set, data bits D0 through D5 and D8 through D14 must be programmed according to the desired operating mode (refer to Figure 4.2-1). Because the ADC board uses only one word in the address space, data bit D15 must be programmed in the CSR to differentiate between the two possible read cycles. D15 must have previously been reset to "zero" in the CSR to enable a *read* access of the converted digital data from the ADC data register. Data bit D15 must have previously been set to a "one" in the CSR to enable a *read* access of the CSR.

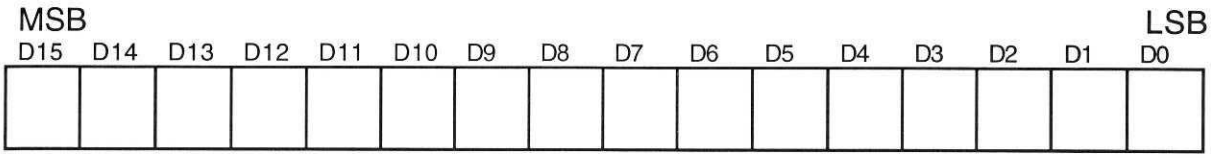
4.2.1 Programming the CSR for Normal Mode Operations

In the normal operating mode, analog inputs are received by either the front panel (P3 connector) or via the AMXbus™ (P2 connector). The AMXbus™ supports a variety of analog input multiplexer boards for processing a wide range of analog input signals. The proper data bits must be programmed in the CSR to select the type of analog input and to start conversion on the selected input. The hexadecimal value of control words that select the different analog inputs are given in Table 4.2.1-1.

4.2.2 Programming the CSR for Test Mode Operations

The CSR controls the selection of the precision voltage source for testing the ADC. Any one of nine precision voltages may be selected for conversion. The

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The following description describes the functions of data bits D15 to D0 that are written to the CSR. All CSR bits are initialized to logic "zero" at power-up and after a VMEbus reset.

- D3, D2, D1, D0 Selects one of 16 channels on either P3 connector MUX or TEST MUX, depending on D4 and D5.

- D5, D4 D5, when high, enables the TEST MUX. D4, when high, enables the P3 connector MUX.

- D6 D6, when high, enables a start conversion.

- D7 Not used.

- D9, D8 D9 and D8 select which one of the four modes from which the ADC board can access analog information.

  Mode 1 The ADC board can access up to 16 single analog inputs via the P3 connector using the on board MUX.

  D9 = 0, D8 = 0

  Mode 2 The ADC board can access external single-end analog inputs from an external VMIC MUX board over the EXPANSION-MUX-Hibus and the GND-SEN-bus.

  D9 = 0, D8 = 1

  Mode 3 The ADC board can access up to 8 differential analog inputs via the P3 connector using the on-board MUX.

  D9 = 1, D8 = 0

  Mode 4 The ADC board can access external differential inputs from an external VMIC multiplexer board via the VMIC AMXbus™.

  D9 = 1, D8 = 1

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Figure 4.2-1. Control Register Write and Read Data Format (Page 1 of 2)

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- D10 — D10 in combination with D6 allows for conversions to be started under software control upon receipt of an external trigger. To start a conversion under software control write a "one" to D6 and "zero" to D10 simultaneously whereas, to start a conversion upon receipt of an external trigger write a "one" to D6 and a "one" to D10 simultaneously.

- D11, D12, — Not used.

- D13 — When high, this control bit enables the test Bus 2 (AOTESTBS) input from the AMXbus™ backplane to the ADC multiplexer input.

- D14 — When low, this bit turns on the Fail LED indicating the board did not pass a diagnostic test. When high, this bit turns the LED off.

- D15 — Write only control bit. This bit controls the on-board select for routing information to the processor data bus. A Write access with this bit asserted (High) enables Read access of the CSR (bits D0-D14). A Write access with this bit de-asserted (Low) enables Read access of the converted data register (D0-D11) and the conversion complete status bit (D15).

NOTICE

THE DATA FORMAT FOR A CONTROL REGISTER READ IS THE SAME AS REGISTER DATA BITS D0 THROUGH D14, AS DESCRIBED ABOVE FOR A CONTROL REGISTER WRITE CYCLE. HOWEVER, TO DISTINGUISH BETWEEN A READ OF THE AD CONVERTED DATA OR THE CONTROL REGISTER, DATA BIT D15 MUST HAVE PREVIOUSLY BEEN WRITTEN HIGH TO THE CONTROL REGISTER.

M3100/F4.2-1

Figure 4.2-1. Control Register Write and Read Data Format (Page 2 of 2)

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Table 4.2.1-1. Analog Input Control Words for Normal Operation Modes (HEX Value)

SELECT ANALOG INPUT TO BE CONVERTED		IMMEDIATE A/D CONVERSION		ENABLE EXTERNAL TRIGGER CONVERSION	
SINGLE-ENDED	DIFFERENTIAL	Analog Input via P3 Connector (Single-Ended)	Analog Input via P3 Connector (Differential)	Analog Input via P3 Connector (Single-Ended)	Analog Input via P3 Connector (Differential)
CH 1	CH 1, HI & LO	5050H	5250H	5410H	5610H
CH 2	CH 2, HI & LO	5051H	5251H	5411H	5611H
CH 3	CH 3, HI & LO	5052H	5252H	5412H	5612H
CH 4	CH 4, HI & LO	5053H	5253H	5413H	5613H
CH 5	CH 5, HI & LO	5054H	5254H	5414H	5614H
CH 6	CH 6, HI & LO	5055H	5255H	5415H	5615H
CH 7	CH 7, HI & LO	5056H	5256H	5416H	5616H
CH 8	CH 8, HI & LO	5057H	5257H	5417H	5617H
CH 9		5058H		5418H	
CH 10		5059H		5419H	
CH 11		505AH		541AH	
CH 12		505BH		541BH	
CH 13		505CH		541CH	
CH 14		505DH		541DH	
CH 15		505EH		541EH	
CH 16		505FH		541FH	

SELECT ANALOG INPUT TO BE CONVERTED	IMMEDIATE A/D CONVERSION		ENABLE EXTERNAL TRIGGER CONVERSION	
	Single-Ended	Differential	Single-Ended	Differential
Analog Input via AMXbus™	5140H	5340H	5500H	5700H

M3100/T4.2.1-1

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CSR enables the conversion of Test Bus 2 via the AMXbus™, as described in Section 3.3.2. Table 4.2.2-1 gives the hexadecimal value of control words that select the test inputs.

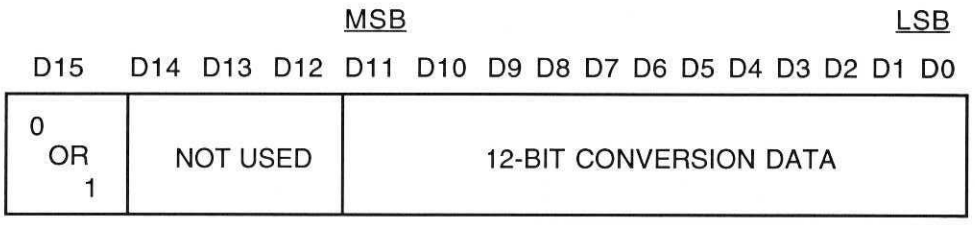
Table 4.2.2-1. Analog Input Control Words for Test Modes (HEX Value)

SELECT ANALOG INPUT TO BE CONVERTED	IMMEDIATE A/D CONVERSION
ON-BOARD PRECISION TEST VOLTAGES	
+10.000	5060H
+7.500	5061H
+5.000	5062H
+2.500	5063H
0.000	5064H
-2.500	5065H
-5.000	5066H
-7.500	5067H
-10.000	5068H
ANALOG OUTPUT LOOPBACK TESTING	
SELECT TEST BUS 2	606FH

M3100/T4.2.2-1

4.3 ADC BOARD READ DATA FORMAT

To read the 12 bits of converted data, data bit D15 must have previously been written low to the CSR. The data is not valid until data bit D15 is read as a logic "zero". The valid data is contained in data bits D0 through D11 (refer to Figure 4.3-1). Throughput is a function of conversion time (9 µsec) and amplifier setting time, which is specified in Table 3.1.3-1.



D15 = 0, DATA VALID
D15 = 1, DATA INVALID

M3100/F4.3-1

Figure 4.3-1. ADC Data Format

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The representation of the different digital output codings for different full-scale range analog inputs is shown in Table 4.3-1. The analog input ranges are resistor selectable, as described in Section 5.8.1. A two's complement option for each output coding shown is available by inserting a jumper, as described in Section 5.7. Two's complement inverts the most significant bit (D11) of the output coding.

Table 4.3-1. ADC Board Output Coding

OUTPUT CODING					
UNIPOLAR			**STRAIGHT BINARY**		
	0 to +10 V	0 to +5 V	D11		D0
+FS-1 LSB	+9.9976	+4.9988	1111	1111	1111
+1/2 FS	+5.0000	+2.5000	1000	0000	0000
+1 LSB	+0.0024	+0.0012	0000	0000	0000
BIPOLAR			**OFFSET BINARY**		
	±10 V	±5 V	D11		D0
+FS-1 LSB	+9.9951	+4.9976	1111	1111	1111
+1/2 FS	+5.0000	+2.5000	1100	0000	0000
+1 LSB	+0.0049	+0.0024	1000	0000	0001
ZERO	0.0000	0.0000	1000	0000	0000
-FS +1 LSB	-9.9951	-4.9976	0000	0000	0001
-FS	-10.000	-5.0000	0000	0000	0000

M3100/T4.3-1

4.3.1 Determining Analog Input Value from Analog-to-Digital Conversion Data

The analog input may be calculated from the output code.

a. For Offset Binary:

$$\text{Analog Input} = (\text{-Full-Scale Voltage}) + (\text{Digital Output Code in Decimal}) \times \frac{\text{Full-Scale Range}}{4096}$$

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Example: For ±10 V input range

(1) -10 V = (-Full-Scale Voltage)
(2) 20 V = Full-Scale Range
(3) If the HEX value of the output code is A00H, then the decimal equivalent is 2560
(4) Analog Input = $-10 + \frac{(2560)\ 20}{4096} = 2.5$ V

b. For Straight Binary:

Analog Input = (Digital Output Code in Decimal) x $\frac{\text{Full-Scale Range}}{4096}$

Example: For 0 to +10 V range

(1) Full-Scale Range = 10 V
(2) If the HEX value of the output code is A00H, then the decimal equivalent is 2560
(3) Analog Input = $\frac{(2560)\ 10}{4096} = 6.25$ V

4.4 MC68000 ASSEMBLY LANGUAGE PROGRAMMING OF THE VMIVME-3100 ADC BOARD

The following example program provides the user with a basic assembly language listing that utilizes a base address of FF0000H (HEX). To select a different board address, the user should refer to Sections 4.1 and 5.2.

The VMIVME-3100 may receive analog information from the front-panel P3 connector or via the multiplexer expansion lines of the AMXbus™ (P2 connector). The following example will digitize the 16 single-ended analog inputs received at the P3 connector. The program is intended as an instructional example only and may not be useful in the user's application. A flow chart of this example is shown in Figure 4.4-1, and the assembly language program is shown in Figure 4.4-2.

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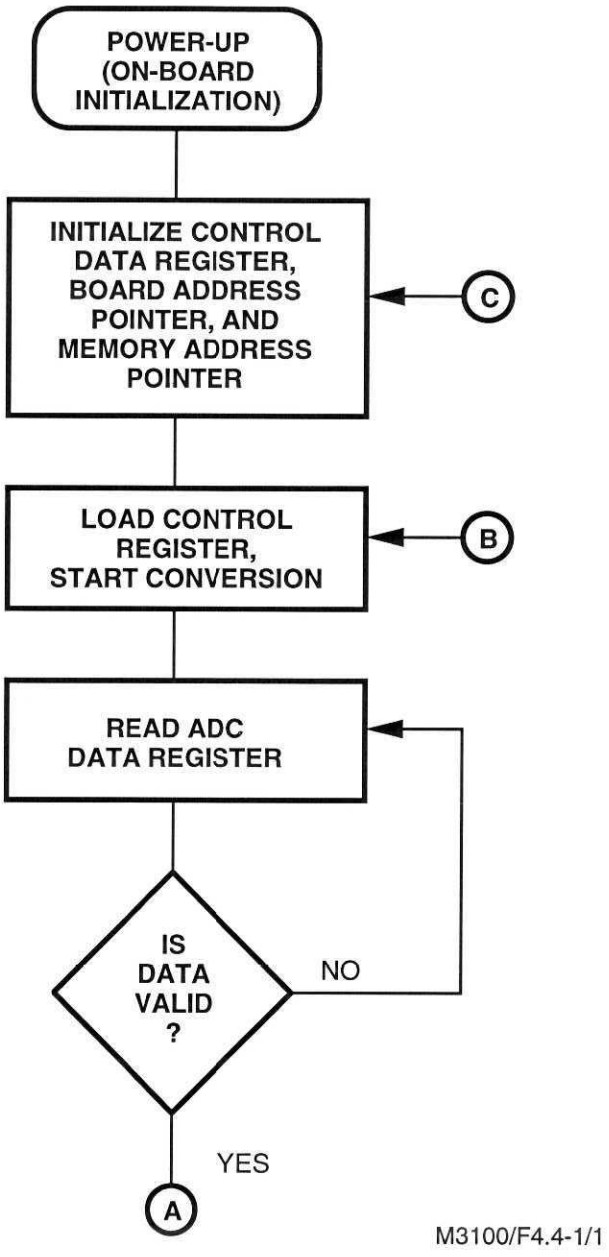
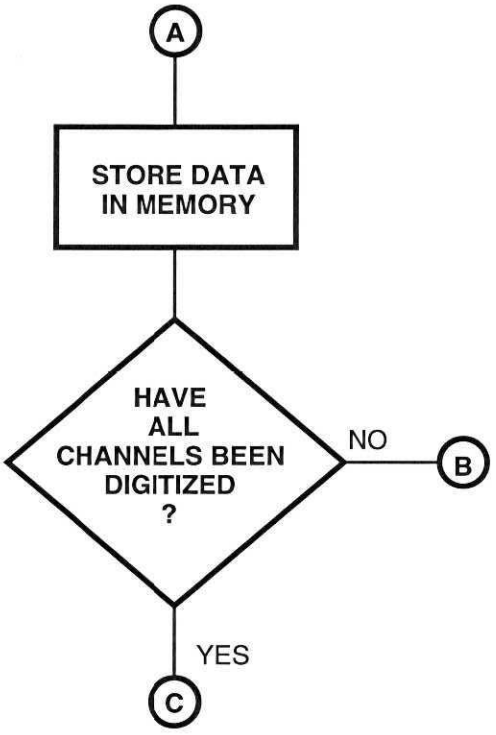


Figure 4.4-1. ADC Programming Sequence Flow Chart (ADC Conversion of 16 Inputs at P3 Connector) (Page 1 of 2)

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M3100/F4.4-1/2

Figure 4.4-1. ADC Programming Sequence Flow Chart (ADC Conversion of 16 Inputs at P3 Connector) (Page 2 of 2)

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```
                                                        COMMENT
INITIALIZE      MOVE.W      #$ MEMORY POINTER, A0       1
                MOVE.W      #$ 5050,D0                  2
                LEA         $FF0000, A1                 3
START AD        MOVE.W      D0, $FF0000                 4
READ AD         MOVE.W      (A1), D1                    5
BTST            #15, D1                                 6
BNE             READ AD                                 7
MOVE.W          D1, (A0)+                               8
ADD.W           #1, D0                                  9
CMP.W           #$ 5060, D0                             10
BNE             START A/D                               11
BRA             INITIALIZE                              12
```

COMMENTS

1. Initialize memory pointer (register A0).
2. Initialize control register contents in register D0.
3. Load board address into address register A1.
4. Load control register - start conversion.
5. Read EOC register data.

6., 7. If bit 15 is a "one," conversion is not complete, keep polling.

8. Store valid data in memory.
9. Increment control register to select next analog input channel (P3 connector).

10., 11., 12. If all 16 channels have been digitized, then start over or else continue to digitize next channel.

M3100/F4.4-2

Figure 4.4-2. Program Example - ADC Conversion of the P3 Connector Inputs

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4.4.1 Program Example - Using the AMXbus™ Expansion Capabilities

The VMIVME-3100, via VMIC's AMXbus™ (connects to the P2 connector), can access a large number of analog input channels from VMIC's 32XX series of analog input multiplexer boards. The ADC board can process a wide variety of analog input signals that are multiplexed under program control via VMIC's AMXbus™.

The following example program selects an analog input from the VMIVME-3200 Multiplexer Board (channel 0) and multiplexes the signal to the ADC board via the AMXbus™ backplane. The signal is then digitized and stored in memory. A flow chart of the example is shown in Figure 4.4.1-1, and the assembly language program is shown in Figure 4.4.1-2. The board address of the VMIVME-3200 is FF0002 (HEX).

The ADC board also will accept and digitize differential signals from the VMIVME-3200 Multiplexer Board. To select differential inputs, a change in the control register programming is required. The multiplexer Board Control Register (BCR) requires a control word of 180 (HEX) and the ADC BCR requires a control word of 5340 (HEX).

4.4.2 Test Programming of the VMIVME-3100 ADC Board

The VMIVME-3100 has self-test capabilities which can be used to support off-line or on-line fault detection and isolation. A diagnostic may be performed after power-up before processing of user analog inputs. Data can be written to the CSR and read back by the processor. This *write/read* test verifies the basic VME interface logic. An on-board precision reference source is provided for verification of the ADC and its associated control circuitry. The following program example depicts an assembly language program that converts the eight precision references and compares the digitized value with the theoretical correct value. A flowchart of the example is shown in Figure 4.4.2-1, and the assembly language program listing is shown in Figure 4.4.2-2. The test voltages and their equivalent digital value is shown in Table 4.4.2-1.

4.4.3 Using the ADC Board to Test the Analog Outputs of the VMIVME-4100 DAC Board

A dedicated test bus (Test Bus 2) on the AMXbus™ is designed to connect the VMIVME-41XX multiplexed analog outputs to the ADC board. The ADC board can verify each of the DAC channel outputs by converting the multiplexed outputs via Test Bus 2, then comparing the digitized value (12 bits) with the original value written to the DAC board(s).

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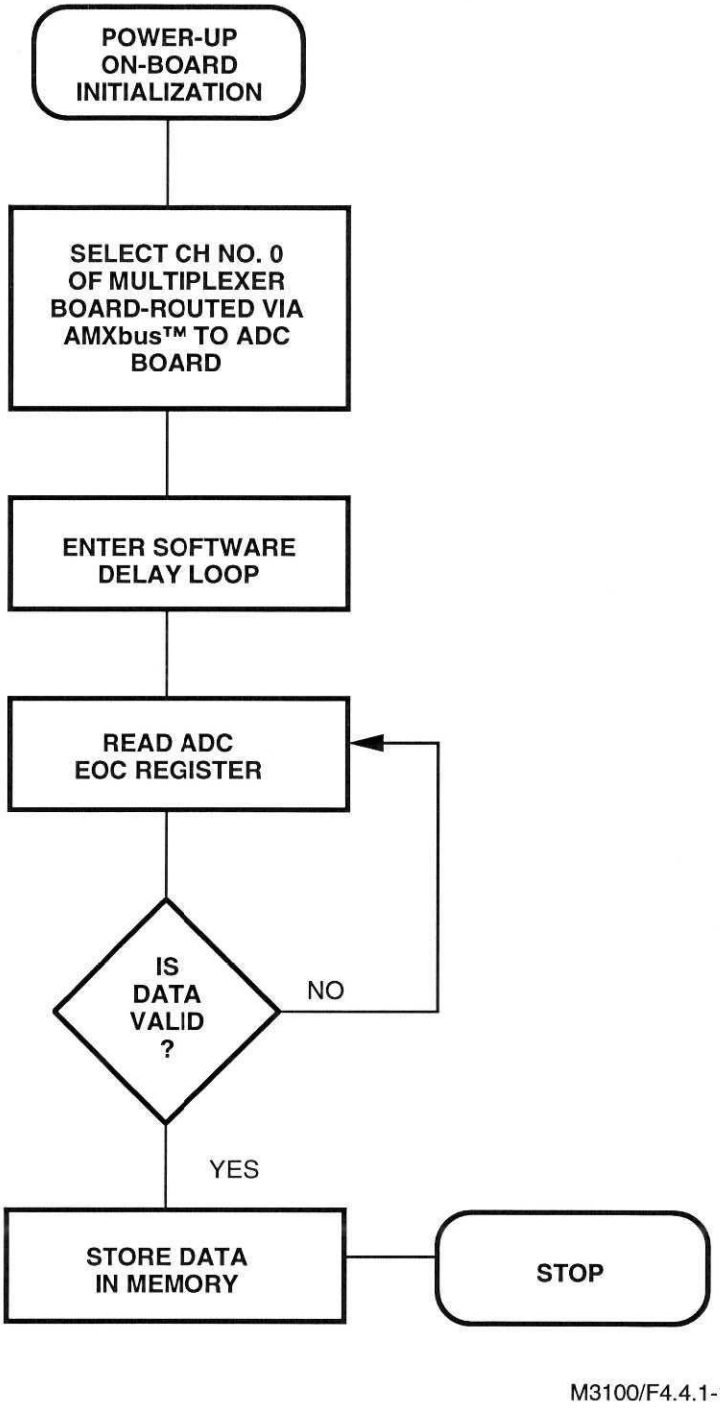


Figure 4.4.1-1. ADC Programming Sequence Flow Chart (Using External Multiplexer Board)

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```
                                                        COMMENT
        LEA         $FF0000, A0                           1
        MOVE.W      #$01A0, FF0002                        2
        MOVE.W      #$ 3F, D0                             3
DELAY   SUB.W       #$1, D0                               4
        BNE         $ DELAY                               5
        MOVE.W      #$ 5140, $FF0000                      6
READ A/D MOVE.W     (A0), D1                              7
        BTST        #15, D1                               8
        BNE         READ A/D                              9
        MOVE.W      D1, MEMORY                            10
```

COMMENTS

1. Load board address into address register A0.
2. Select channel No. 0 of multiplexer board.
3. Initialize delay loop.
4., 5. Delay approximately 10 µs for signal to settle at ADC board input.
6. Load control register - start conversion.
7. Read EOC register data.
8., 9. If bit 15 is a "one", conversion is not complete; keep polling.
10. Store valid data in memory.

M3100/F4.4.1-2

Figure 4.4.1-2. Program Example - ADC Conversion of a Multiplexed Single-Ended Analog Signal (Channel) from the VMIVME-3200 Board

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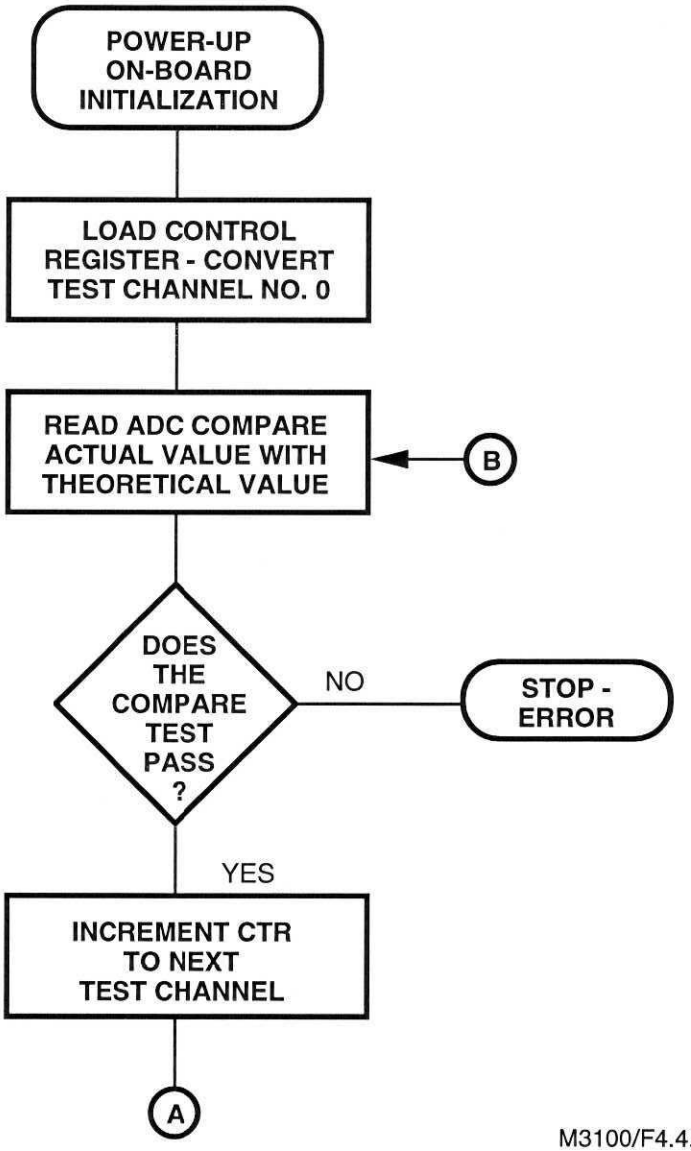


Figure 4.4.2-1. ADC Programming Sequence Flow Chart (Using On-Board Precision Reference Voltage for Self-Test) (Page 1 of 2)

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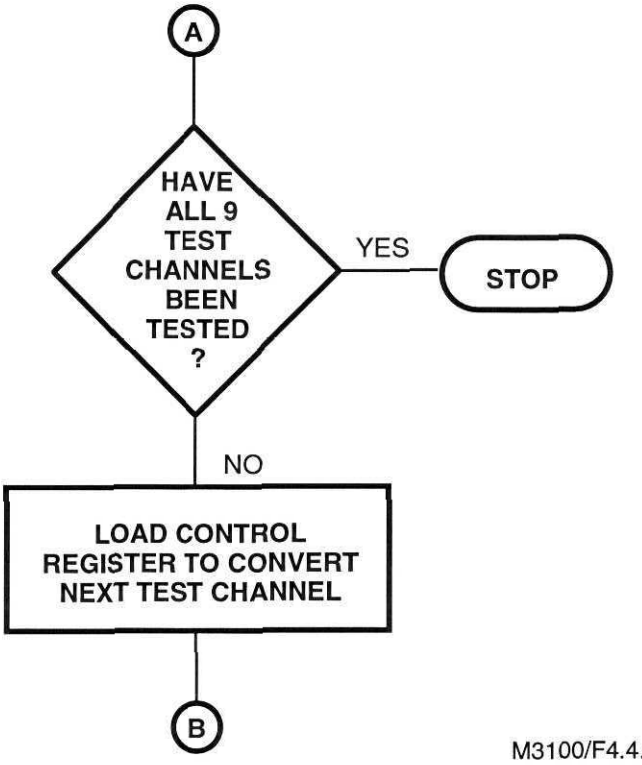


Figure 4.4.2-1. ADC Programming Sequence Flow Chart (Using On-Board Precision Reference Voltage for Self-Test) (Page 2 of 2)

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			COMMENT
START	LEA	$FF0000, A0	1
	MOVE.W	#$ 5060, D0	2
	MOVE.W	D0, $FF0000	3
	MOVE.W	#$ FFF, D1	4
	JSR	READ A/D	5
	MOVE.W	#$ E00, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ C00, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ A00, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ 800, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ 400, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ 200, D1	6
	JSR	READ A/D	6
	MOVE.W	#$ 000, D1	6
	JSR	READ A/D	6
	BRA	END	7
READ A/D	MOVE.W	(A0), D2	8
	BTST	#15, D2	9
	BNE	READ A/D	10
	SUB.W	D1, D2	11
	BPL	POS	12
	NEG.W	D2	13
POS	SUB.W	#3, D2	14
	BGT	ERROR	15
	ADD.W	#1, D0	16
	CMP.W	#$ 5069, D0	17
	BEQ	CONT	18
	MOVE.W	D0, $FF0000	19
CONT	RTS		20

M3100/F4.4.2-2

Figure 4.4.2-2. Program Example - Built-In Self-Test Using On-Board Precision References (Page 1 of 2)

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COMMENTS

1. Load ADC board address into register A0.

2. Load control word into register D0.

3. Load control register - start conversion.

4. Store theoretical results for conversion of test channel No. 0 into register D1.

5. Jump to subroutine that will read ADC converted value and compare with theoretical results previously stored in register D0.

6. Continue like steps 4 and 5 for all nine test values (refer to Table 4.4.2-1).

7. When all test channels have been successfully tested, then STOP.

8. Read end-of-conversion register data.

9., 10. If bit 15 is a "one," conversion is not complete; keep polling.

11., 12., 13. Subtract the ADC converted value from the current test value. Check to see if the result is positive; if not, negate D2 to make it a positive value.

14., 15. Subtract error allowance from D2. If the result is positive, then the test has failed.

16., 17., 18., 19., 20. Increment to next test channel and start conversion. Return from subroutine.

M3100/F4.4.2-2

Figure 4.4.2-2. Program Example - Built-In Self-Test Using On-Board Precision References (Page 2 of 2)

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Table 4.4.2-1. Precision Reference Voltages

TEST CHANNEL NO.	REFERENCE VOLTAGE (±1 mV)	CONVERTED DIGITAL VALUE (HEX)
0	+10.000	FFFH
1	+7.500	E00H
2	+5.000	C00H
3	+2.500	A00H
4	0.000	800H
5	-2.500	600H
6	-5.000	400H
7	-7.500	200H
8	-10.000	000H

M3100/T4.4.2-1

The reader should refer to the programming requirements of the selected VMIVME-41XX Analog Output Board for a thorough understanding of programming requirements. This example utilizes the VMIVME-4100 Board whose base board address was selected at FF0060 (HEX). The program example ramps the analog output from its minimum value (000H) to its maximum value (FFFH) by incrementing one LSB each time through the test loop. Channels 0 through 15 are multiplexed, one at a time, to the ADC board via the AMXbus™. The analog value is digitized and compared to the original value written to the analog output channel. A flowchart of the programming sequence is shown in Figure 4.4.3-1, and the assembly language listing is shown in Figure 4.4.3-2.

4.4.4 Using the ADC Board in Conjunction with the VMIVME-4100 DAC Board to Verify the VMIVME-3200 Multiplexer Board

A dedicated test bus (Test Bus 1) on the AMXbus™ supports multiplexed analog outputs from the VMIVME-4100 to the VMIVME-3200. This analog output can be routed through all 32 channels of the multiplexing logic on the VMIVME-3200 Board. This signal is then multiplexed via the AMXbus™ to the ADC board for conversion. This design concept uses any channel of any VMIVME-4100 Board as a dynamic source for testing VMIVME-3200 Multiplexer Boards. Prior to testing the VMIVME-3200, the user executes diagnostics on the VMIVME-3100 ADC for verification, followed by diagnostics on VMIVME-4100 Boards. Upon successful completion of diagnostics on these boards, the user executes diagnostics on all VMIVME-3200 Boards in the system. The following program, shown in Figure 4.4.4-2, uses only channel 0 of the VMIVME-4100 and increments from -10 to +10 V signals (or 000 to FFF HEX), one count at a time, through each multiplexer channel. The programming sequence is shown in Figure 4.4.4-1.

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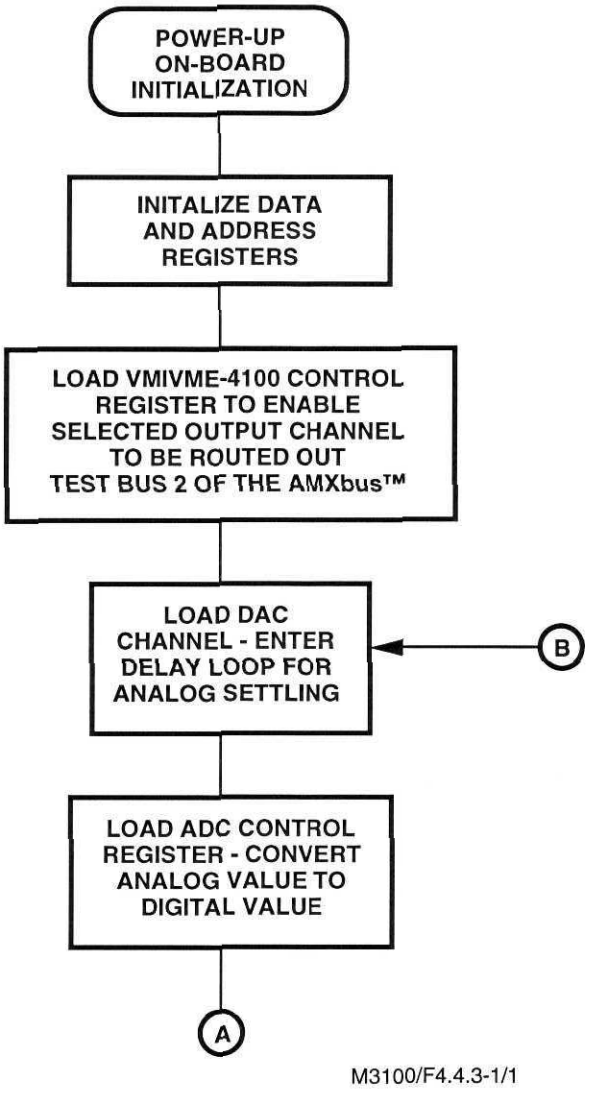


Figure 4.4.3-1. ADC Programming Sequence Flow Chart (Using the ADC Board to Verify the Analog Output Channels of the VMIVME-4100 DAC Board) (Page 1 of 2)

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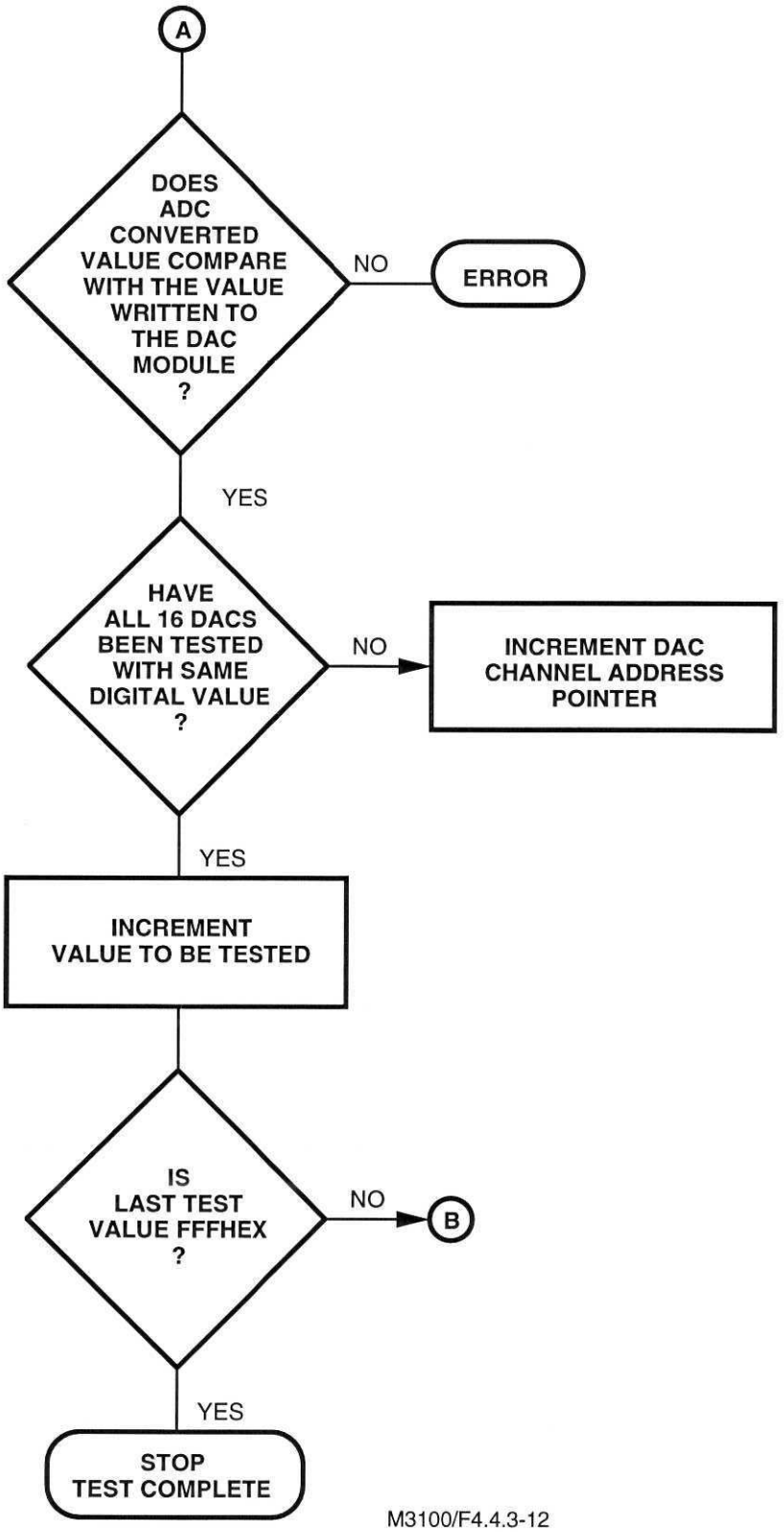


Figure 4.4.3-1. ADC Programming Sequence Flow Chart (Using the ADC Board to Verify the Analog Output Channels of the VMIVME-4100 DAC Board)(Page 2 of 2)

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```
                                                    COMMENTS
START       MOVE.W      #O, D0                      1
            MOVE.W      #0 D1                       2
            LEA         $FF0060,  A0                3
            MOVE.W      #$ EC00, $ FF0060           4
LOAD DACS   MOVE.W      D0, (A0)+                   5
            ADD.W       #1, D1                      6
            MOVE.W      #$1F, D2                    7
DELAY       SUB.W       #1, D2                      8
            BNE         DELAY                       9
            LEA         $FF0000, A1                 10
            MOVE.W      #$ 606F, $FF0000            11
READ        MOVE.W      (A1), D3                    12
            BTST        #15, D3                     13
            BNE         READ                        14
            SUB.W       D0, D3                      15
            BPL         POS                         16
            NEG.W       D3                          17
POS         SUB.W       #3, D3                      18
            BGT         ERROR                       19
            CMP.W       #$ 1 0, D1                  20
            BNE         LOAD DAC                    21
            ADD.W       #1, D0                      22
            CMP.W       #$ 1000, D0                 23
            BEQ         END                         24
            MOVE.W      #0, D1                      25
            LEA         $FF0060, A0                 26
            BRA         LOAD DACS                   27
```

1. Initialize test value counter to 000H.

2. Initialize channel counter to 00H.

3. Load DAC board address into register A0.

4. Load DAC board control word to enable multiplexed outputs to AMXbus™.

M3100/F4.4.3-2

Figure 4.4.3-2. Program Example - Using the VMIVME-3100 ADC Board to Verify the Analog Output Channels of the VMIVME-4100 DAC Board (Page 1 of 2)

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COMMENTS

5. Load current DAC channel (A0) with current test value (D0). This instruction automatically increments A0 to point to next DAC channel to be tested.

6. Increment channel counter by "one".

7., 8., 9. Delay routine to allow for analog output settling before conversion by ADC board.

10. Load ADC board address into register A1.

11. Load ADC board control register - start conversion.

12., 13., 14. Read ADC board and test bit 15. When bit 15 goes low, then data on D11 through D0 is the valid conversion data.

15., 16., 17. Subtract the ADC converted value from the current test value. Check to see if the result is positive; if not, negate D3 to make it a positive value.

18., 19. Subtract error allowance from D3. If the result is positive, then the test has failed.

20., 21. If all 16 DAC channels have not been loaded with current test value, then continue until they have been.

22. If all 16 DACs have been tested with current test value, then increment test value (D0).

23., 24. If FFF HEX was the last test value converted, then test is complete.

25., 26., 27. Otherwise, re-initialize channel counter to "zero". Re-load DAC Board starting address into A0 and continue test until all 16 channels have been tested from 000 HEX to FFF HEX.

M3100/F4.4.3-2

Figure 4.4.3-2. Program Example - Using the VMIVME-3100 ADC Board to Verify the Analog Output Channels of the VMIVME-4100 DAC Board (Page 2 of 2)

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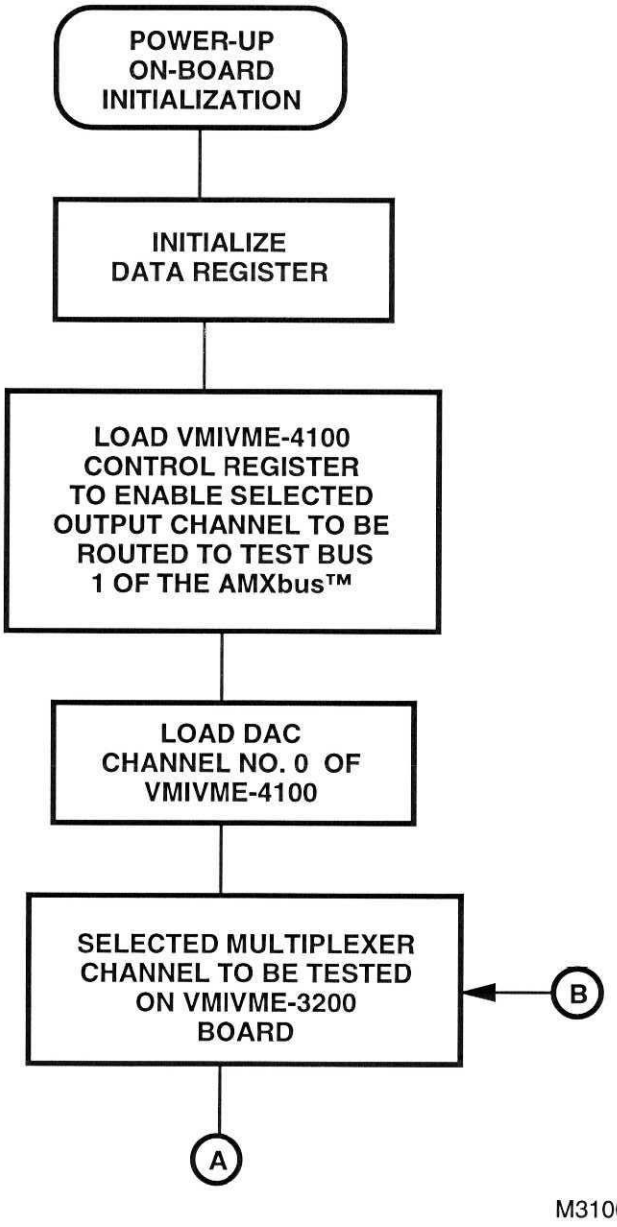


Figure 4.4.4-1. Programming Sequence Flow Chart (Using the ADC Board and the VMIVME-4100 Board to Verify the VMIVME-3200 Board) (Page 1 of 3)

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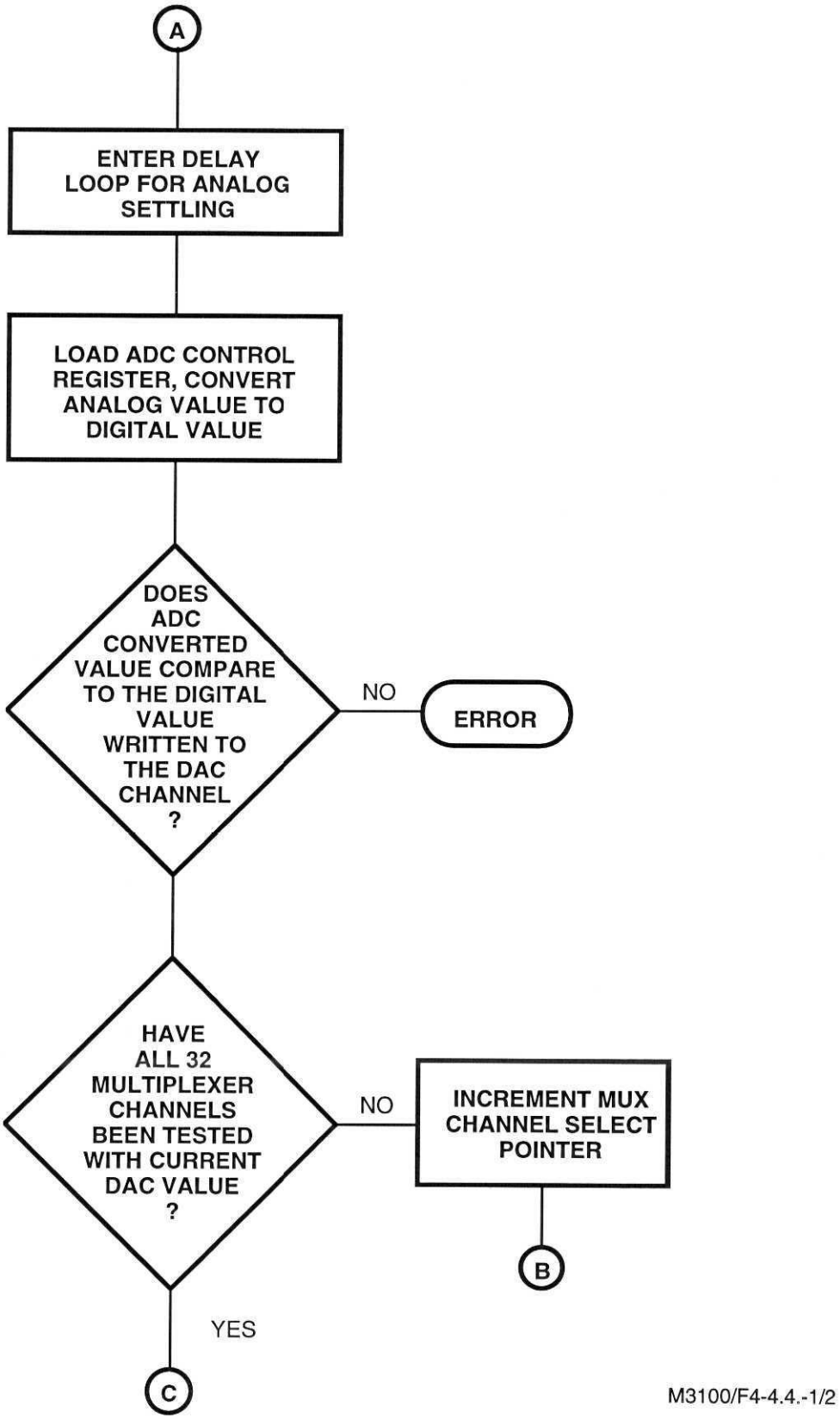


Figure 4.4.4-1. Programming Sequence Flow Chart (Using the ADC Board and the VMIVME-4100 Board to Verify the VMIVME-3200 Board) (Page 2 of 3)

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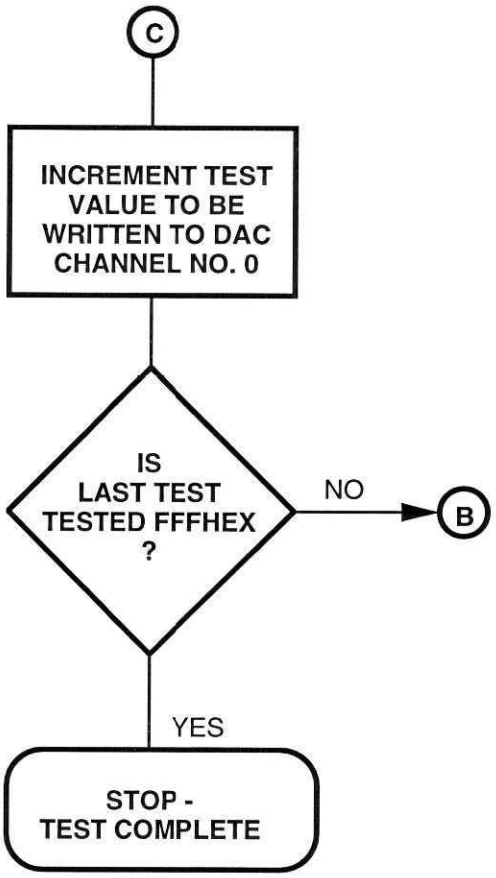


Figure 4.4.4-1. Programming Sequence Flow Chart (Using the ADC Board and the VMIVME-4100 Board to Verify the VMIVME-3200 Board) (Page 3 of 3)

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```
                                                        COMMENTS
          MOVE.W      #$, D1                            1
START     MOVE.W      #$ 0160, D0                       2
LOAD DAC  MOVE.W      #$ DC00, $FF0060                  3
          MOVE.W      D1, $FF0060                       4
          MOVE.W      D0, $FF0002                       5
          MOVE.W      #$ 2F, D2                         6
DELAY     SUB.W       #$ 1, D2                          7
          BNE         DELAY                             8
          LEA         $FF0000, A0                       9
          MOVE.W      #$ 5140, $FF0000                  10
READ      MOVE.W      (A0), D3                          11
          BTST        #15, D3                           12
          BNE         READ                              13
          SUB.W       D1, D3                            14
          BPL         POS                               15
          NEG.W       D3                                16
POS       SUB.W       #3, D3                            17
          BGT         ERROR                             18
          ADD.W       #$1, D0                           19
          CMP.W       #$ 0180, D0                       20
          BNE         LOAD DAC                          21
          ADD.W       #$ 1, D1                          22
          CMP.W       #$ 1000, D1                       23
          BEQ         STOP                              24
          BRA         START                             25
```

1. Initialize Test Value counter to 000 HEX.

2. Initialize Multiplexer Control Register (MCR) to select test mode on VMIVME-3200 and select channel 0.

3. Load DAC board control word to enable multiplexed outputs to Test Bus 1 of the AMXbus™.

4. Load DAC channel 0 with current test value.

M3100/F4.4.4-2

Figure 4.4.4-2. Program Example - Using the ADC Board and the VMIVME-4100 to Verify the VMIVME-3200 Board (Page 1 of 2)

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COMMENTS

5. Enable multiplexer channel to be tested.

6., 7., 8. Delay routine to allow for analog output settling before conversion by ADC board.

9. Load ADC board address into address register A0.

10. Load ADC board control register - start conversion.

11., 12., 13. Read ADC board and test bit 15. When bit 15 goes low, then data on D11 through D0 is the valid conversion data.

14., 15., 16. Subtract the ADC converted value from the current test value. Check to see if the result is positive; if not, negate D3 to make it a positive value.

17., 18. Subtract error allowance from D3. If the result is positive, then the test has failed.

19., 20., 21. Increment the CSR value, which selects the next multiplexer channel to be tested. If all 32 channels have not been tested, then continue until they have been.

22., 23., 24., 25. Increment test value to be written to the DAC channel No. 0. If last value tested was FFF HEX, then test is complete; otherwise, continue testing.

M3100/F4.4.4-2

Figure 4.4.4-2. Program Example - Using the ADC Board and the VMIVME-4100 to Verify the VMIVME-3200 Board (Page 2 of 2)

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
*****************
*    CAUTION    *
*****************
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
*****************
*    CAUTION    *
*****************
```

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

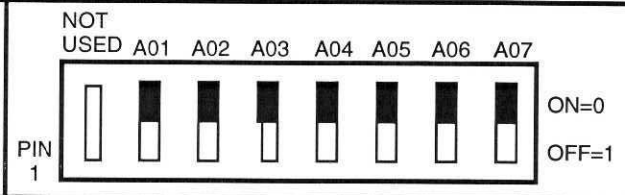
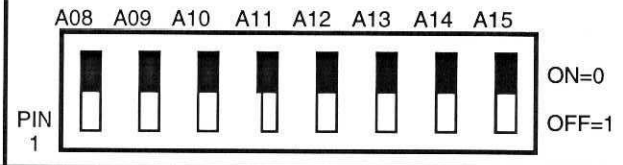
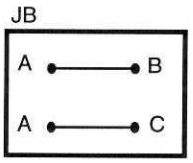
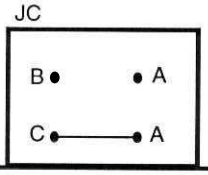
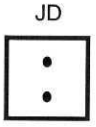
De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated.

5.3 INSTALLATION

This section describes the VMIVME-3100 Analog-to-Digital Converter (ADC) Board set-up procedure and the different board configurations. The board select address and optional configurations are factory preset as shown in Table 5.3-1. The board address switches (S1, S2) are all shown in the ON position. This selects a base address at FF0000H (HEX) for the board.

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Table 5.3-1. VMIVME-3100 Factory Set Jumpers and Address Switch Configurations

JUMPER	FUNCTION	PRE-SET CONDITION
S1	BOARD ADDRESS SELECTION SWITCH (A07 TO A01)	
S2	BOARD ADDRESS SELECTION SWITCH (A15 TO A08)	
JB	IN BIPOLAR OPERATION, SELECTS IF AD OUTPUT CODING IS OFFSET BINARY OR TWO'S COMPLEMENT. PIN A CONNECTED TO PIN C IS OFFSET BINARY. PIN A CONNECTED TO PIN B IS TWO'S COMPLEMENT.	
JC	JC SELECTS THE INPUT RANGE TO THE ADC. PIN A TO PIN C IS FOR BIPOLAR RANGES. PIN A TO PIN B IS FOR UNIPOLAR INPUTS.	 PRE-SET PIN A TO PIN C FOR ±10 INPUTS UNLESS ORDERED OTHERWISE
JD	SELECTS ADDRESS MODIFIER RESPONSE OF THE BOARD. FACTORY INSTALLED JUMPER INDICATES RESPONSE TO SHORT NON-PRIVELEGED I/O ACCESS. WITH JUMPER REMOVED, THE BOARD RESPONDS TO SUPERVISORY I/O ACCESS.	 JUMPER NOT INSTALLED AT FACTORY

M3100/T5.3-1

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5.4 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, go through the following checklist to verify the board is ready for the intended operation.

1. Have the sections on Theory and Programming, Sections 3 and 4, of the Digital-to-Analog Converter (DAC) Board been read and applied to system requirements?

   ____√____

2. Review Table 5.3-1 to verify that factory installed jumpers and board address switches are set to what is desired. _____

   a. To change DAC board address switches (S1 and S2), refer to Section 5.5.
   b. To change address modifier response jumper (JD), refer to Section 5.6.
   c. To change ADC output coding (Jumper JB), refer to Section 5.7.
   d. To change from bipolar to unipolar analog inputs, refer to Section 5.8.

3. If ±2.5 V, ±5 V, 0 to +2.5 V, 0 to +5 V full-scale input range is desired, refer to Section 5.8.1. _____

4. If an increase in acquisition time is required (time for the multiplexer, instrumentation amplifier, and sample-hold to settle out before conversion), refer to Section 5.9. _____

5. Has the cable, with proper mating connector, been connected to the analog input connector (P3)? Refer to Section 5.10. _____

6. Calibration is performed at the factory. If re-calibration is required, refer to Section 5.11. _____

After steps 1 through 6 have been reviewed in Section 5.4, then the ADC board may be installed in a VMEbus system. The ADC board may generally be installed in any slot position, except slot one, which is usually reserved for the master processing unit.

```
*****************
*    CAUTION    *
*****************
```

DO NOT INSTALL OR REMOVE THE BOARD WITH THE POWER ON UNLESS THIS BOARD WAS MANUFACTURED WITH THE EXTENDED GROUND PIN OPTION.

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5.5 BOARD ADDRESS SELECTION SWITCHES

There are two address DIP switches on the VMIVME-3100. Each individual switch corresponds to an address bit or is not used. If the switch is ON, the corresponding address bit is compared to a logic "zero." All corresponding address bits must compare with the switch positions during a *write/read* of the DAC boards. Address switch details are shown in Figure 5.5-1. The physical locations of the switches are shown in Figure 5.5-2.

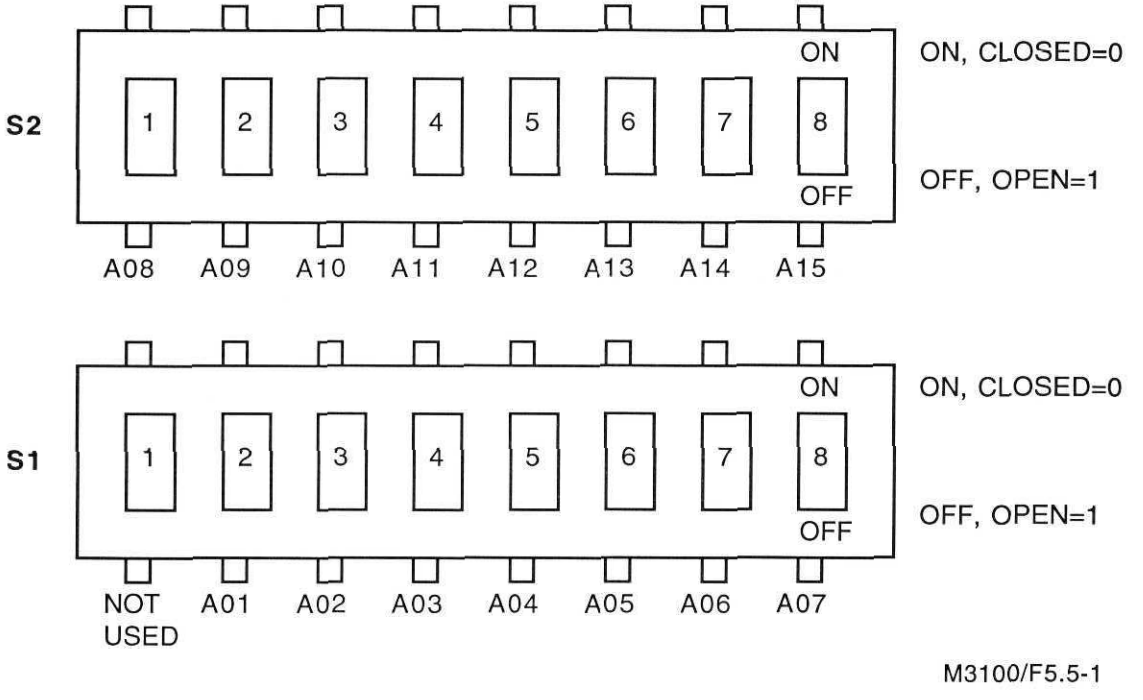


Figure 5.5-1. Address Select Switches, S1 and S2

Example: For the VMIVME-3100 to respond to a base address of $(FFFFOO)_{16}$, the S1 and S2 switches are set as shown below:

	1	2	3	4	5	6	7	8
S2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S1	X	ON	ON	ON	ON	ON	ON	ON

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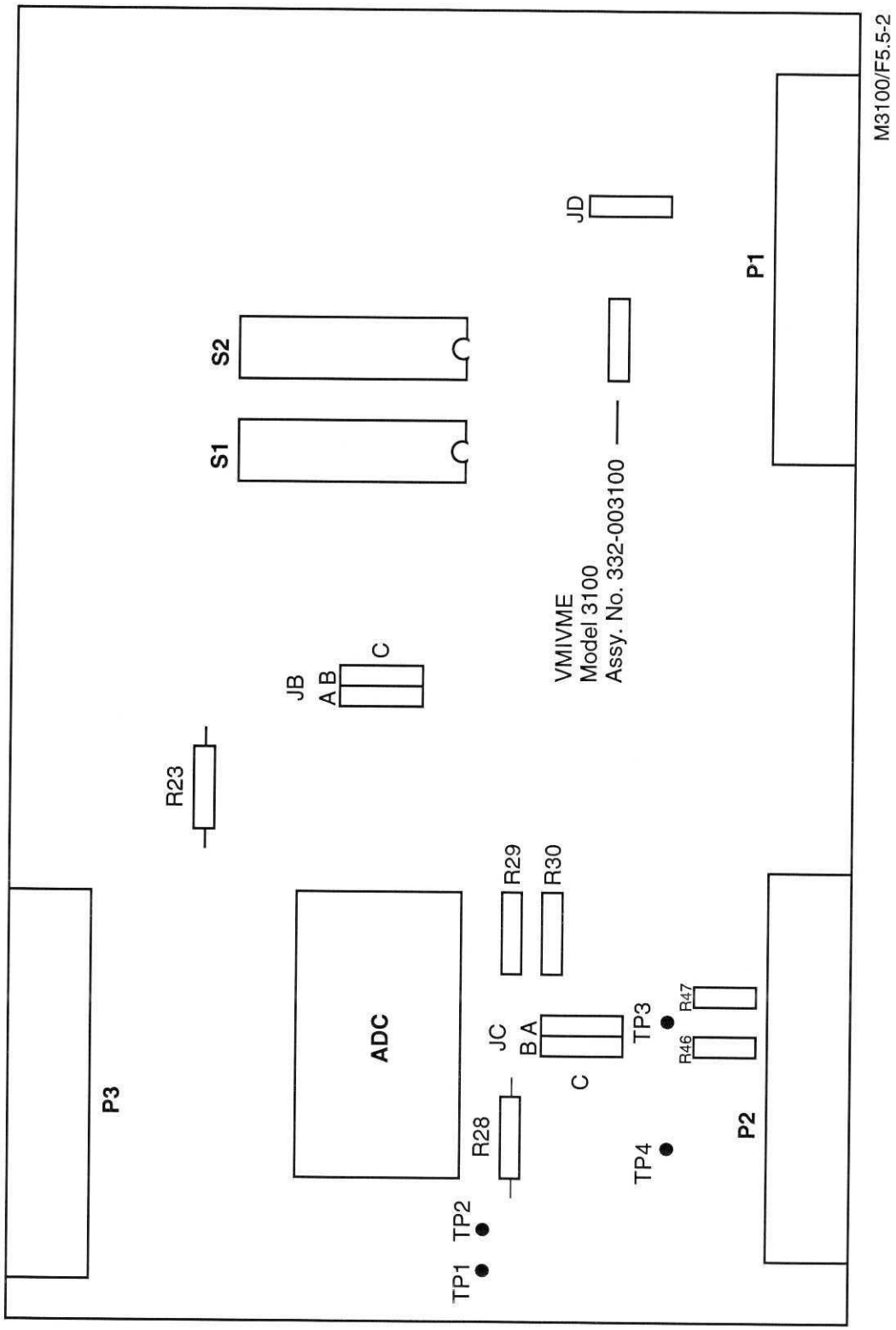


Figure 5.5-2. Jumper and Switch Locations on VMIVME-3100 (Component Side)

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5.6 ADDRESS MODIFIER RESPONSE SELECTION

The DAC board is memory mapped in the short I/O address space, as described previously in Section 4. The DAC board will respond to either of the two address modifier codes that may be issued to the ADC board by a CPU board during a *write* or *read* cycle. The ADC board is factory set to respond to supervisory short I/O access. To select non-privileged short I/O access, then install the jumper at jumper location (JD). The physical location of this jumper is shown in Figure 5.5-2.

5.7 ADC OUTPUT CODING SELECTION

The ADC board is shipped factory-configured for straight binary digital coding for unipolar inputs and offset binary for bipolar inputs, as shown in Table 4.3-1. To change the output coding to two's complement (invert the MSB), connect jumper JB, pin A to pin B, as shown in Figure 5.7-1. Jumper location (JB) is shown in Figure 5.7-2.

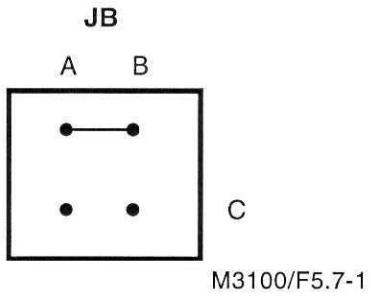


Figure 5.7-1. Two's Complement Jumper Selection

5.8 ANALOG INPUT FULL SCALE RANGE SELECTION

Jumper (JC) selects unipolar or bipolar ADC converter operation. This jumper, with the associated gain resistor (R28), selects the full-scale range to be digitized by the ADC. The unipolar ranges are 0 to ±2.5 V, ±5 V, and ±10 V. This jumper connection is wirewrapped. Refer to Figure 5.8-1 for the jumper connection details. The physical location of jumper (JC) is shown in Figure 5.5-2.

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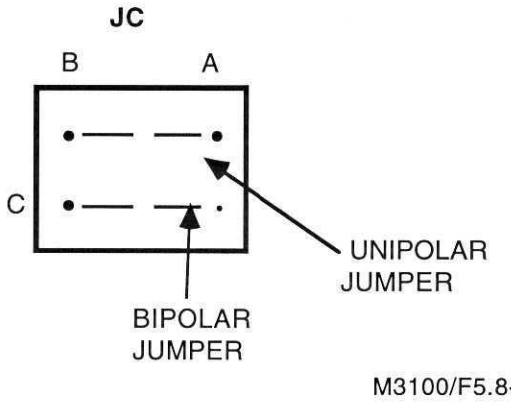


Figure 5.8-1. Jumper Configuration (JC)

5.8.1 Installing the Gain Resistor (R28) for Different Input Ranges

Gain resistor (R28) is installed at the factory according to the ordering code, as shown in Section 2.3. For full-scale ranges of 0 to ±10 V and -10 to +10 V, no gain resistor is required. For 0 to +5 V and ±5 V, a 20.0 kΩ resistor with 0.01 percent tolerance is required. For 0 to +2.5 V and ±2.5 V, a 6.667 kΩ resistor with 0.01 percent tolerance is required.

5.9 RDELAY (OPTIONAL) SELECTION

The board is factory configured with no RDELAY resistor. This selects an acquisition settling time of 9 µsec and is the time for the on-board multiplexer, instrumentation amplifier, and sample-and-hold to settle out before conversion of a high-level analog input signal. The required acquisition time is shown as a function of full-scale analog input ranges in Table 3.1.2-1 (page 3-2). If the VMIVME-3100 ADC Board is used to convert analog signals multiplexed via the AMXbus™ from external multiplexers, additional settling time may be programmed by the user. Note that any delay added in the acquisition time would increase the throughput time and decrease the conversion rate of the system.

a. Throughput time = Acquisition time
+ AD Conversion Time (9 µsec)

b. Maximum Conversion Rate = $\frac{1}{\text{Throughput time}}$

Table 5.9-1 provides RDELAY for various acquisition times. The RDELAY (R23) physical location is shown in Figure 5.5-2.

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Table 5.9-1. RDELAY versus Acquisition Time

RDELAY (Ω)	ACQUISITION TIME
NONE	9 µsec (factory configuration)
7 K	16 µsec
21 K	30 µsec
51 K	60 µsec

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5.10 CONNECTOR DESCRIPTIONS

Two connectors, P1 and P2, connect the VMIVME-3100 Board to the VMEbus backplane. The connectors are 96-pin DIN type. The primary connector, P1, contains the address data and control lines and all additional signals necessary to control data transfer and other bus functions. The P2 user I/O pins are used by the AMXbus™ for controlling external multiplexer expansion boards and for testing VMIC's analog output boards. The P2 connector pin and signal assignments are shown in Figure 5.10-1 and Table 5.10-1.

The AMXbus™ backplane is used when the user requires an off-board multiplexer expansion unit (VMIC VMIVME-32XX Series) or when Built-in-Test is desired using the VMIVME-41XX Series Analog Output Board(s). The AMXbus™ is a low-noise backplane, available in 5, 9, or 19 slots.

The P3 connector is a Panduit 32-pin male connector, type 120-332-033A. The matching Panduit connector for the input cable is a female connector, type 120-332-435E. This connector supports the 16 single-ended or eight differential analog inputs, each with an associated analog ground pin. For P3 connector pin and signal assignments, refer to Figure 5.10-2 and Table 5.10-2.

Using a flat-ribbon connector that has Row "C" as the end circuit, all of the odd-numbered conductors of the cable are grounded due to Row "C" of P3 being connected to ground. Therefore, all even-numbered conductors of the cable are input signals for the VMIVME-3100. Cable connectors that use Row "A" as the end circuit are available. Utilizing Row "A" as the end circuit provides the user with the capability of using all odd-numbered conductors for signal and the even-numbered conductors for ground. Normally, connectors with an end circuit of Row "C" would be used. However, end circuit Row "A" connectors would allow connections to field devices with DIN connectors that used Row "C" as the signal output and Row "A" as the ANA COM. The VMIVME-3100 P3 connector input requires the signal inputs to Row "A" and the ANA COM signal to Row "C". The P3

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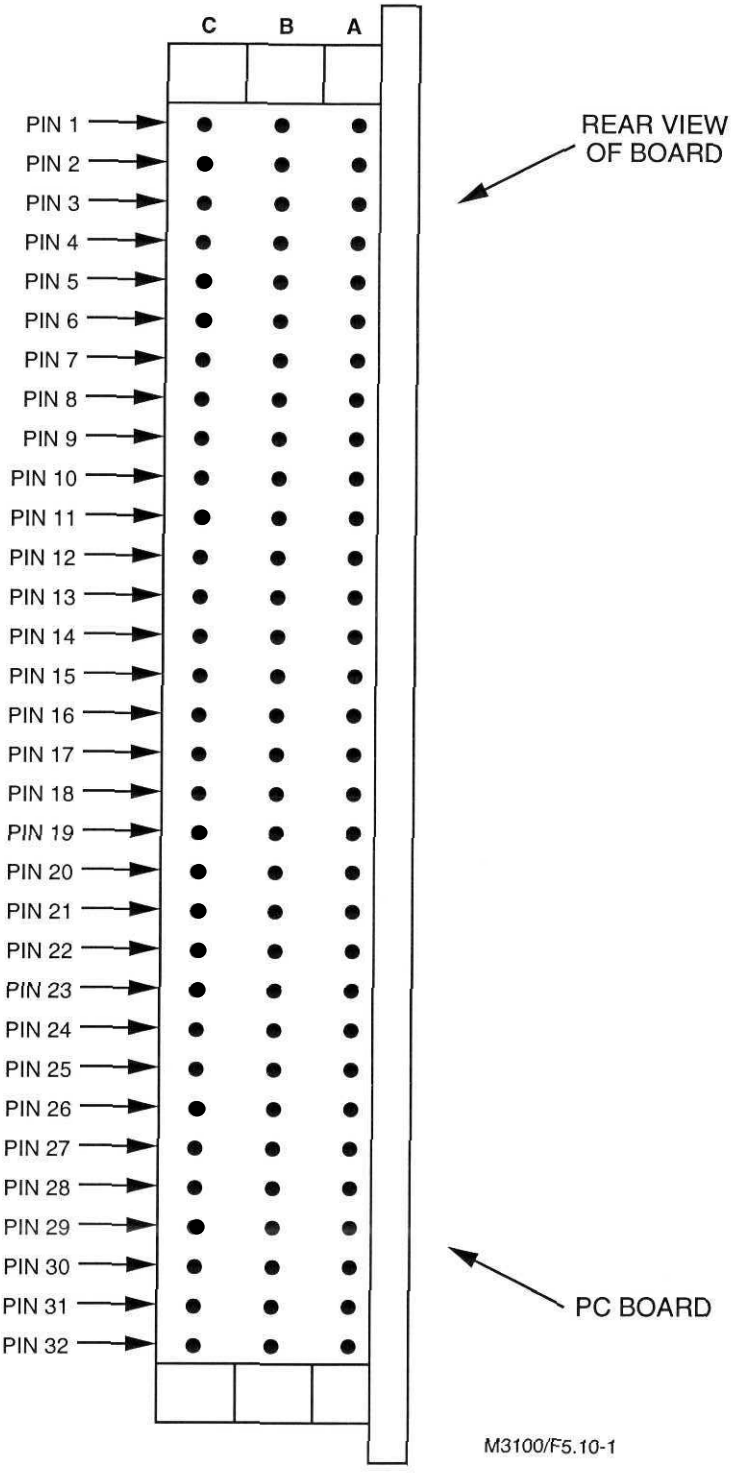


Figure 5.10-1. P2 Connector-Pin Assignments

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Table 5.10-1. P2 Connector Signal Assignment

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	ANA COM	+5 V	
2	ANA COM	GND	
3	ANA COM		
4	ANA COM		
5	ANA COM		
6	ANA COM		
7			
8	ANA COM		
9	AOTESTBS		
10	ANA COM		
11	EXMUXLOBS		
12	ANA COM	GND	
13	EXMUXHIBS	+5 V	
14	ANA COM		
15	GND SEN		
16	ANA COM		
17			
18	ANA COM		
19			
20	ANA COM		
21			
22	ANA COM	GND	
23	ANA COM		
24	ANA COM		
25			
26	GND		
27	EXTTRIGL		
28	GND		
29	ENDCONVTL		
30	GND		
31	EXTSTROBL	GND	
32	GND	+5 V	

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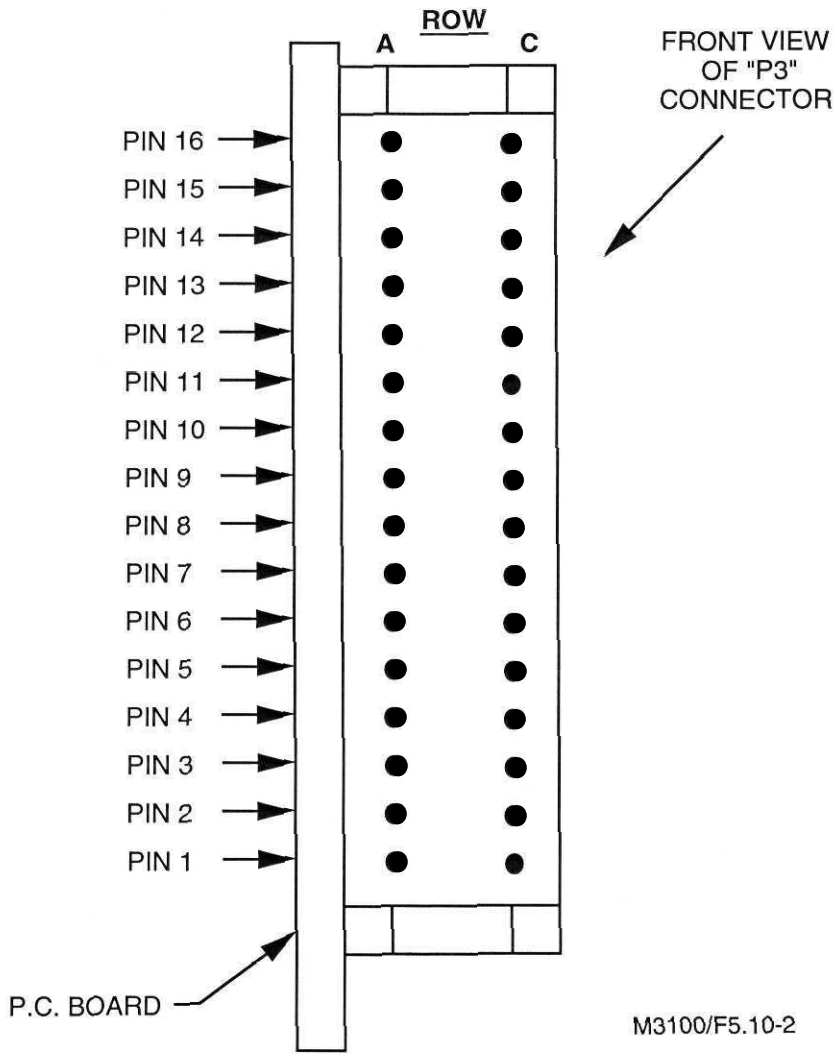


Figure 5.10-2. P3 Connector - Pin Assignments

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Table 5.10-2. Single-Ended Inputs P3 Connector Signal Assignment

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	CH0	ANA COM
2	CH1	ANA COM
3	CH2	ANA COM
4	CH3	ANA COM
5	CH4	ANA COM
6	CH5	ANA COM
7	CH6	ANA COM
8	CH7	ANA COM
9	CH8	ANA COM
10	CH9	ANA COM
11	CH10	ANA COM
12	CH11	ANA COM
13	CH12	ANA COM
14	CH13	ANA COM
15	CH14	ANA COM
16	CH15	ANA COM

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connector assignment for single-ended inputs is shown in Table 5.10-2 and the connector assignment for differential inputs is shown in Table 5.10-3.

A Connector and I/O Cable Application Guide (VMIC Document No. 825-00000-006) is available from VMIC. This application guide provides the user with additional information concerning field connections, the use of round cables, and a thorough explanation of compatible connectors and cabling techniques.

5.11 VMIVME-3100 CALIBRATION

There are four potentiometer adjustments on the VMIVME-3100. They have been properly adjusted at the factory and lock-tight has been applied to the potentiometer adjustment in shipping and handling. However, the adjustment screw is easily broken away for user adjustment if necessary. Two potentiometers adjust the +10 and -10 V precision references that are applied to a precision resistance network that generates the test voltages. The other two potentiometers are used in calibrating the offset and gain adjustments on the ADC. When recalibration is desired, first calibrate the on-board precision references. These references can then be used to recalibrate the ADCs. The procedure is as follows:

a. Remove any cable connected to the P3 connector.
b. Apply power to the board and allow 10 minutes for warm-up.
c. Using a 4-1/2 digit voltmeter, connect the negative lead to the P3 connector, pin C-1 (ANA COM).
d. Attach the positive lead to Test Point 3 (TP3). Refer to Figure 5.5-2 for TP3 board location.
e. Adjust potentiometer R46 until the voltmeter reads 9.9951 ±1 mV.
f. Attach the positive lead to Test Point 4 (TP4) and adjust potentiometer R47 to -10.000 V ±1 mV.
g. Perform an ADC conversion on Test Channel number seven, as discussed in Section 4.2.2. Adjust the offset potentiometer (R30) until the converted value alternates between 000 HEX and 001 HEX. This may require several iterations of conversions and adjustments until the desired results are reached.
h. Perform an ADC conversion on Test Channel number zero, as discussed in Section 4.2.2. Adjust the gain potentiometer (R29) until the converted value alternates between FFE HEX and FFF HEX.

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Table 5.10-3. Differential Inputs P3 Connector Signal Assignment

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	CH0 HI	ANA COM
2	CH1 HI	ANA COM
3	CH2 HI	ANA COM
4	CH3 HI	ANA COM
5	CH4 HI	ANA COM
6	CH5 HI	ANA COM
7	CH6 HI	ANA COM
8	CH7 HI	ANA COM
9	CH0 LO	ANA COM
10	CH1 LO	ANA COM
11	CH2 LO	ANA COM
12	CH3 LO	ANA COM
13	CH4 LO	ANA COM
14	CH5 LO	ANA COM
15	CH6 LO	ANA COM
16	CH7 LO	ANA COM

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SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of ninety (90) days from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

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In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

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6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

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6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

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APPENDIX A
ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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