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VMIVME-3111

48 ANALOG-TO-DIGITAL INPUTS
2-CHANNEL DIGITAL-TO-ANALOG OUTPUT BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-003111-000 T

Revised June 19, 1995

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VMIVME-3111
48 ANALOG-TO-DIGITAL INPUTS
2-CHANNEL DIGITAL-TO-ANALOG OUTPUT BOARD

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GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-3111 Analog-to-Digital Converter (ADC) Board provides both the stimulus and the response functions encountered in VME closed-loop analog systems. Self-contained, with a resident 12-bit ADC and Digital-to-Analog Converters (DACs), the VMIVME-3111 board represents a single board solution to the analog input/output requirements of such VME applications as process control, simulators, trainers, and supervisory control.

Because it does not rely upon additional supporting analog boards for A/D or D/A conversion, the VMIVME-3111 simplifies the task of designing any VME system which requires both analog inputs and outputs. The following brief overview of the principal features illustrates the flexibility and performance that is available with the VMIVME-3111 Board:

a. Thirty-two single-ended or 16 differential P2 analog inputs
b. Sixteen single-ended front panel analog input channels (cable compatible with the 3V and 5V series signal conditioners)
c. Two analog output channels with 10 mA drive capability
d. Program-controlled off-line operation of analog outputs
e. Resident 12-bit ADCs and DACs
f. Input and output ranges selectable as 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V
g. Optional low pass filters available for analog input noise elimination
h. ADC data coding program-selectable as either binary, offset binary, or two's complement format
i. Automatic ADC timing simplifies programming
j. Stable on-board precision voltage references
k. Program-controlled autocalibration of gain and zero
l. 19 µs A/D conversion time (sample plus conversion)
m. 8 to 120 µs input acquisition time (gains of x1 to x500)
n. On-board smart controller permits interleaved (pipelined) operation for maximum A/D conversion throughput
o. All inputs and outputs protected against line transients and short circuits
p. Front panel FAIL indicator
q. Double Eurocard form factor
r. Individually coded/keyed VME connectors

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1.2 FUNCTIONAL DESCRIPTION

The VMIVME-3111 ADC Board is a self-contained, 12-bit board. The analog inputs can be configured either as 48 single-ended channels, or as 16 differential plus an additional 16 single-ended inputs. In addition to user-selectable ranges, the VMIVME-3111 offers real-time programmable input gains of x1, x10, x100, and x500. Autocalibration features permit program-controlled calibration of zero offsets and input gain. A block diagram of the VMIVME-3111 is shown in Figure 1.2-1.

All inputs are available with low pass filters for noise elimination. Thirty-two of the input channels are available at the rear panel P2 connector; the front panel P3 connector contains 16 input channels which are cable compatible with the VMIC 3V/5V Series of signal conditioners. A resident smart controller permits "pipelined" ADC operation, and automatically inserts all necessary settling delays. These features reduce program control of the ADC to a simple handshake sequence, and provide the highest possible throughput or sample rate, without degrading accuracy.

Two wideband analog outputs can supply 10 mA of drive current over the full output range of ±10 V, and can be operated off-line for self-test. Built-in-Test (BIT) features permit off-line verification of all active components by routing the analog outputs through the analog input multiplexers.

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from the following:

VITA
VFEA International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	**DOCUMENT NO.**
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) System Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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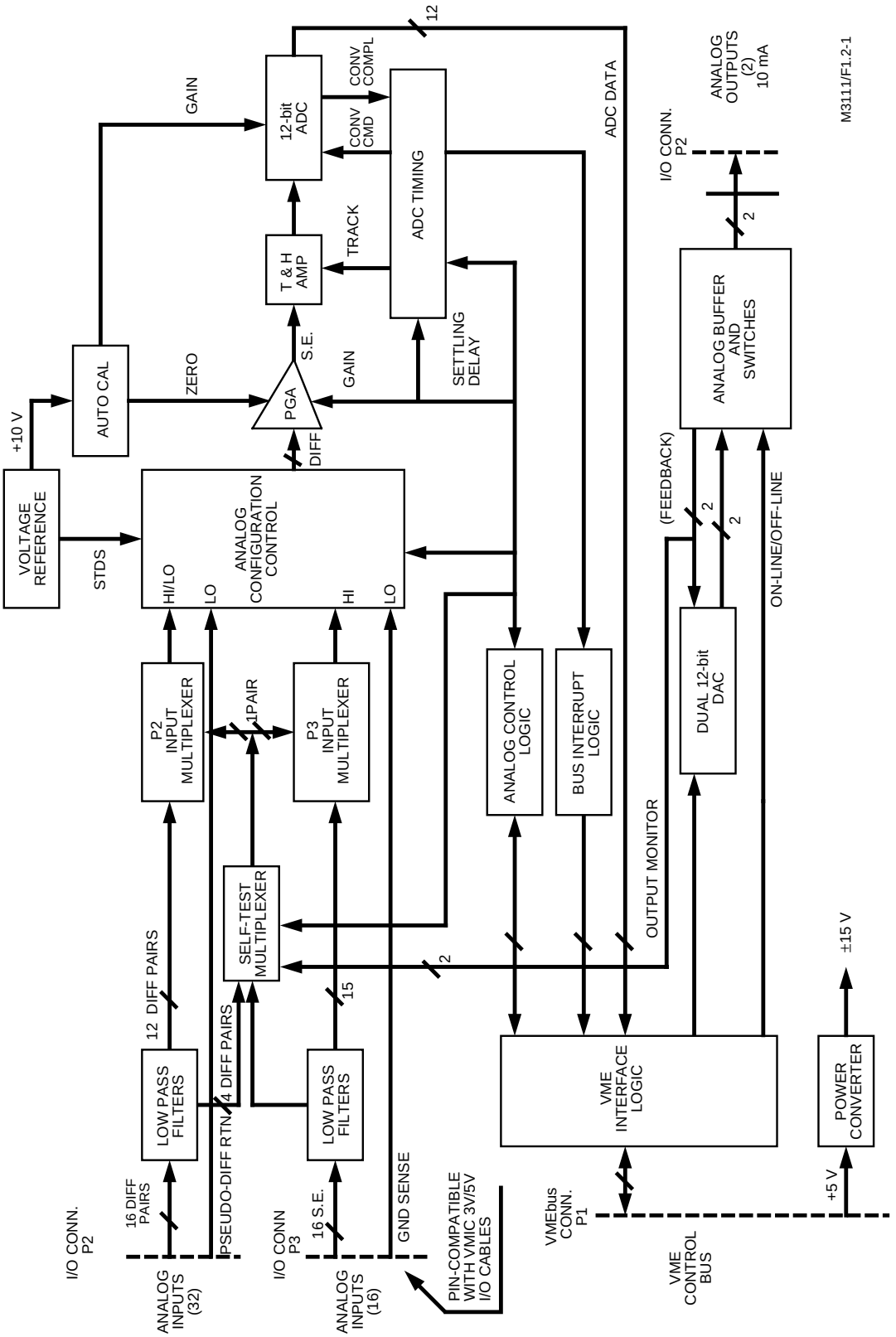


Figure 1.2-1. VMIVME-3111 Functional Block Diagram

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003111-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3111 Board is a 12-bit, programmable gain, Analog-to-Digital Converter (ADC) board which is designed to operate on the standard VMEbus. With a resident 12-bit ADC, a Digital-to-Analog Converter (DAC), and loopback self-test features, the board is self-contained and does not require additional boards to provide high-quality analog input and output functions. The VMIVME-3111 is a flexible system I/O element which offers Built-in-Test and off-line operational features not found in many other products.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-3111 is divided into the following functional categories which are illustrated in the functional block diagram shown in Figure 1.2-1. All VMIVME-3111 functions are discussed in detail in subsequent sections of this manual.

a. VMEbus Interface
b. Bus Interrupter
c. Analog Input Filters and Multiplexers
d. Analog Configuration Networks
e. Programmable Gain Amplifier
f. ADC Channel
g. Self-Test Multiplexer
h. DACs
i. Analog Output Buffers and Switches
j. Autocalibration
k. Power Converter

3.3 VMEbus CONTROL INTERFACE

The VMIVME-3111 communication registers are memory mapped as 16 (decimal), 16-bit words. The registers are contiguous and may be user-located on any 32-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged bus communications.

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3.3.1 Read/Write Operations

During each READ/WRITE operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers shown in Figure 3.3.1-1 and the address and address modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted ON (LOW). Subsequent removal of the CPU READ/WRITE command causes the board-generated DTACK signal to return to the OFF (HIGH) state.

After board selection has occurred, three groups of VMEbus signals control READ/WRITE communications with the board:

a. Data Bus lines D00 to D15
b. Address lines A01, A02, A03, A04
c. Bus Control Signals:

    1. WRITE*
    2. DS0*, DS1*
    3. SYS CLK
    4. SYS RESET* ("*" = Asserted LOW)

Data bus lines are bidirectional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A04 map the 16 communication registers onto a 32-byte boundary within the VME address space (Section 4). The control signals determine whether data is to be moved to the board (WRITE) or from the board (READ). The control signals also provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all timers and flags.

Static controls are latched into the Control Register, and are used primarily to establish the operational mode of the boards. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC, are read through the Status Register. The Control and Status Registers (CSRs) are referred to collectively as the Control and Status Register (CSR). Most of the Control Register outputs can be monitored directly through the Status Register.

Each of the two analog output channels are controlled by writing 12-bit right-justified data into a dedicated 16-bit READ/WRITE register. The lower 12 bits (D00 to D11) of each Analog Output Register are loaded directly into the DAC for the output, while the upper four bits (D12 to D15) are ignored.

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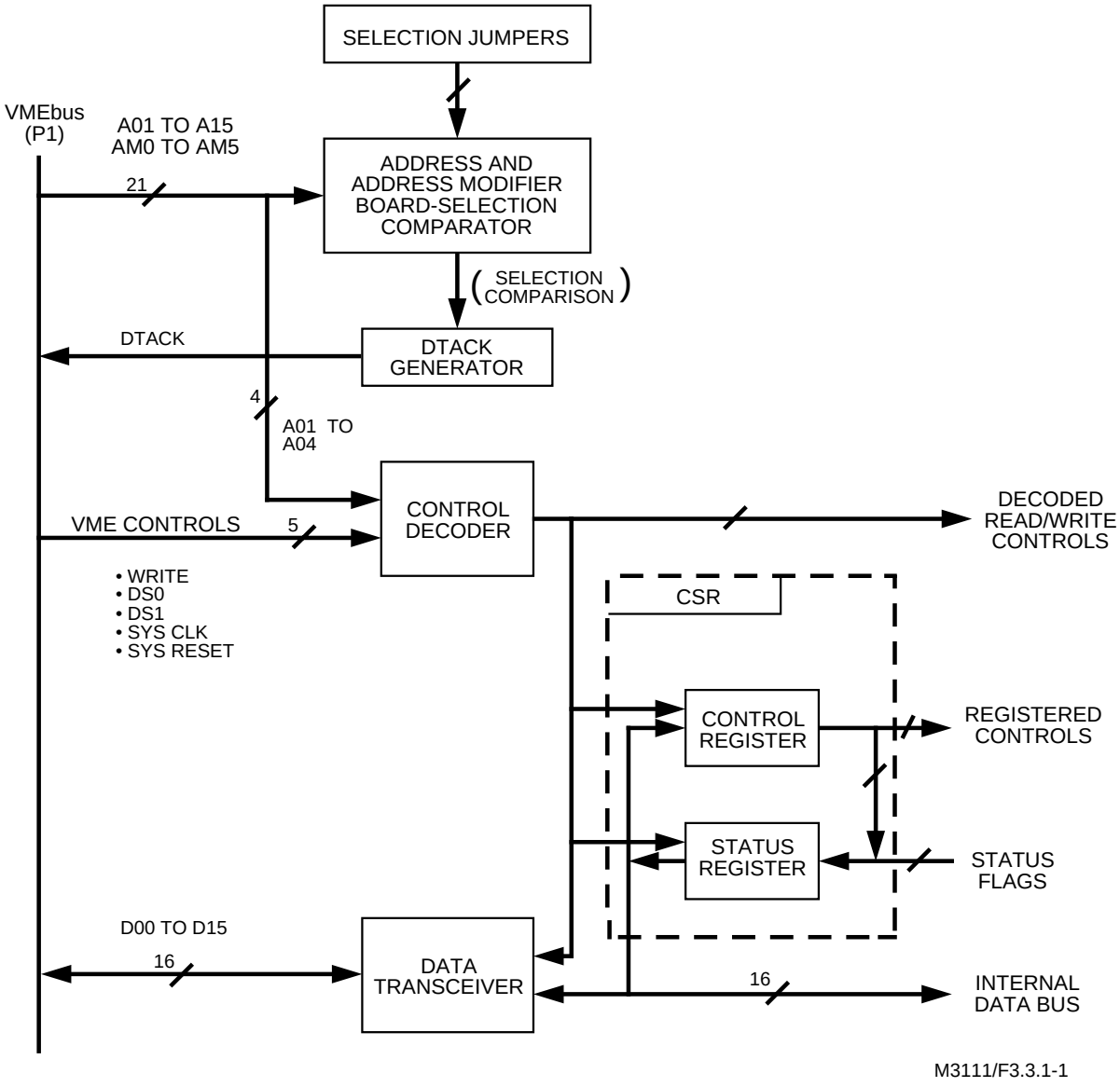


Figure 3.3.1-1. VMEbus Control Signals and Interface Logic

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3.3.2 Bus Interrupter

To eliminate the processing overhead usually associated with ADC polling, the VMIVME-3111 provides access to the VME interrupt structure through the Bus Interrupter Module (BIM) shown in Figure 3.3.2-1. Control Registers for the interrupter are located at relative addresses 10 and 18 (HEX) in the VMIVME-3111 assigned address space. These control registers are for INT0. Once the BIM has been programmed and an A/D conversion has been started, the bus signals IACK, IACKIN, and IRQ1 to IRQ7 control communication of the final NEW DATA RDY flag to the VME controller. Details of interrupt control requirements are described in Section 4.

3.4 ADC CONTROL AND TIMING

Control commands and status flags associated with controlling the ADC are illustrated in Figure 3.4-1, and are described both in the following sections and in Section 4.

3.4.1 Converter Controls and Status Flags

A conversion sequence is initiated by writing a "1" to the START SETTLING and EN START CONV controls bits, and is composed of the following consecutive time intervals:

a. Settling Delay
b. Tracking Interval
c. Analog-to-Digital Conversion

All ADC timing intervals discussed in this section are performed automatically by the on-board smart controller. Program control of the converter consists of basic handshake sequences.

The settling delay occurs directly after a state change has occurred in the analog networks (such as selecting a new input channel), and represents the settling time of the networks. After the settling delay has been completed, the track-and-hold (T&H) amplifier (see Figure 1.2-1) enters the tracking mode and the tracking interval begins.

During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage. The SETTLING BUSY flag is set HIGH at the beginning of the settling delay, and is cleared LOW at the end of the tracking interval. The CONV BUSY flag is set HIGH by the EN START CONV control bit, and remains HIGH until the conversion sequence has been completed.

At the end of the tracking interval, the T&H amplifier enters the HOLD MODE, in which the output of the amplifier is held at a constant level, and a CONV CMD from the timing decoder causes the A/D conversion to begin. The A/D

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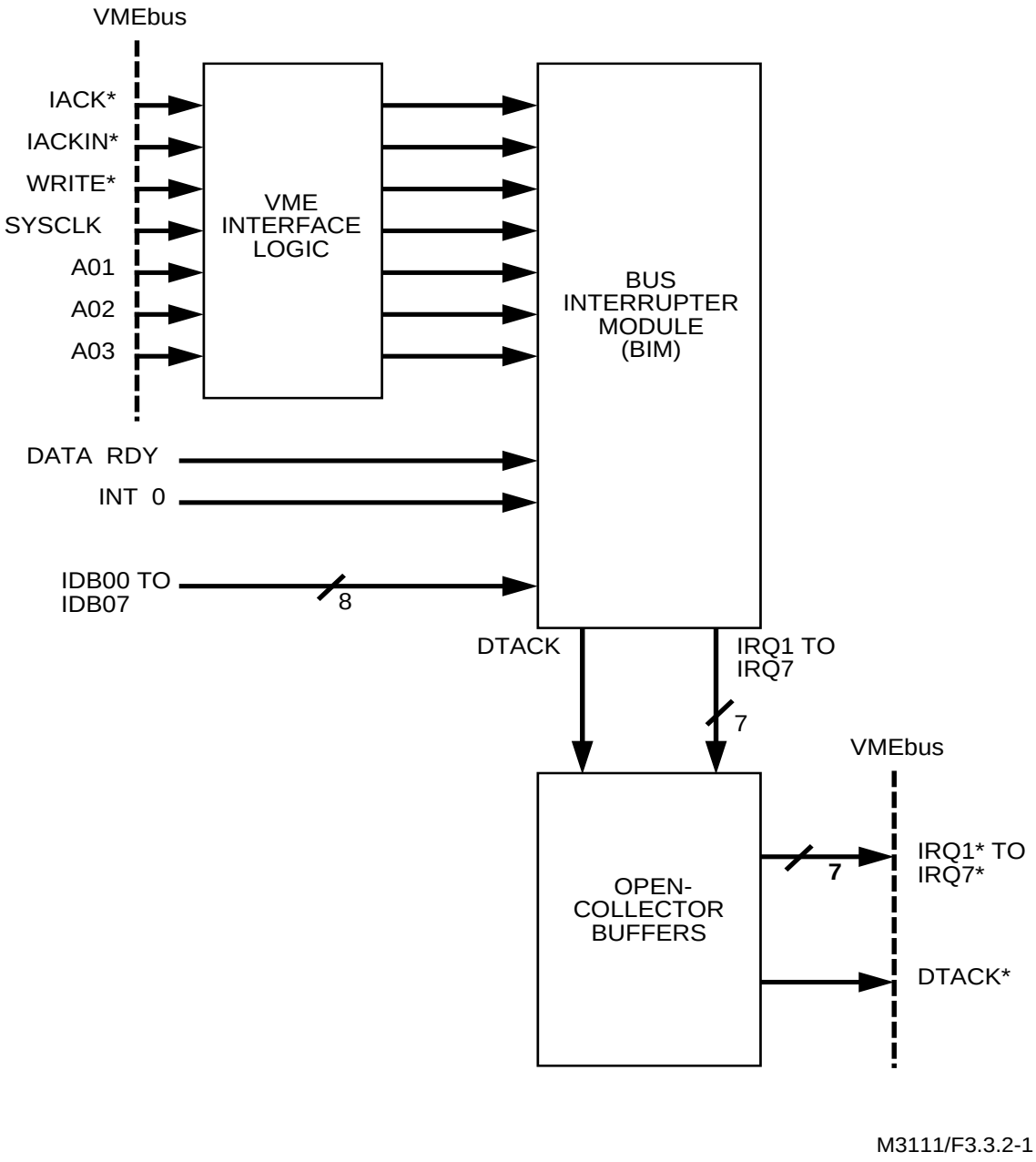


Figure 3.3.2-1. Bus Interrupt Logic

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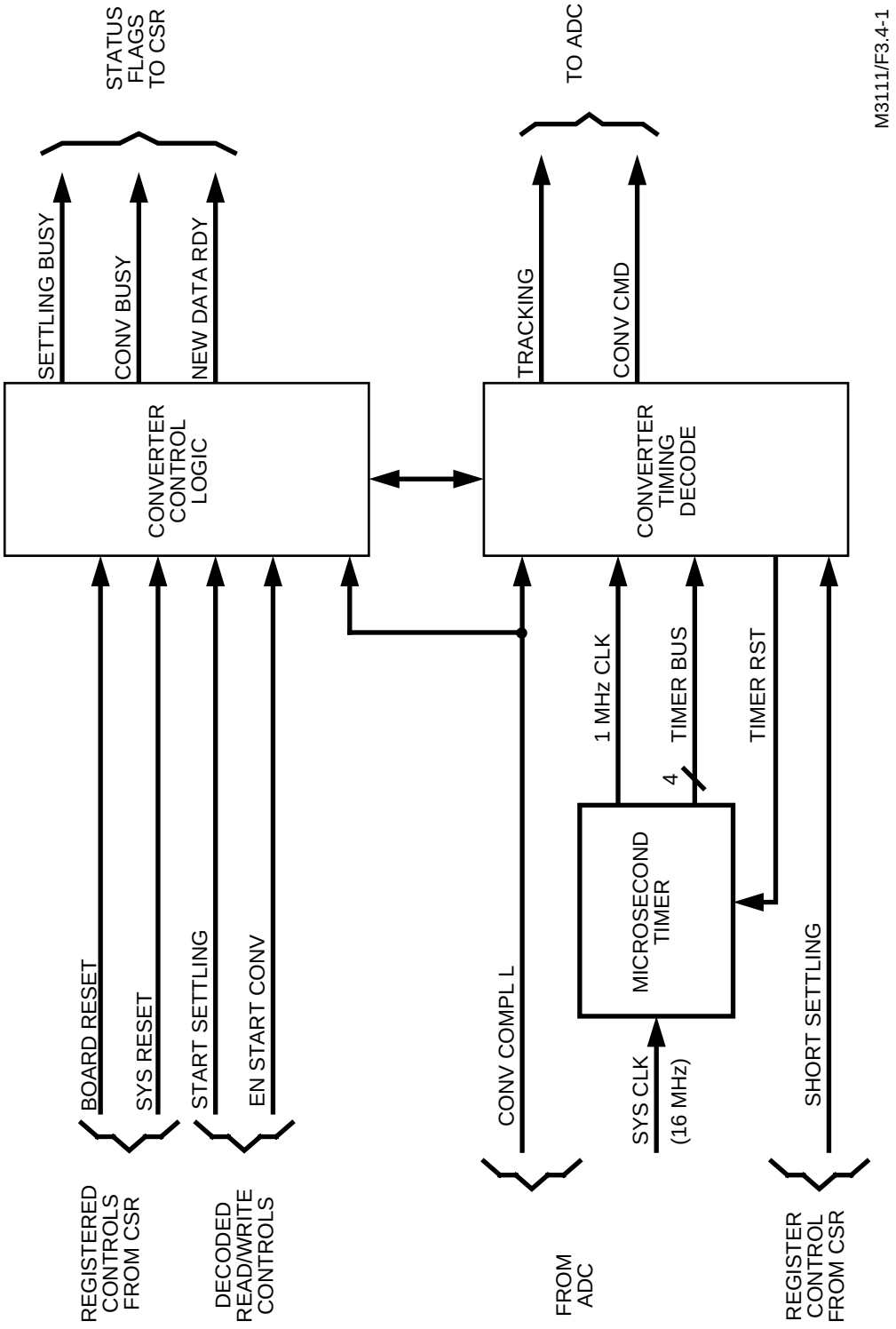


Figure 3.4-1. ADC Timing Logic and Control Signals

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conversion digitizes the output of the T&H amplifier into a 12-bit data word, and then terminates the conversion sequence. The CONV COMPL L flag from the ADC is HIGH during the conversion, and is LOW otherwise.

Completion of the A/D conversion causes the NEW DATA RDY flag to be set HIGH, indicating that valid data is present in the Converter Data Register (Section 4). The action of reading the Converter Data Register resets the NEW DATA RDY and CONV BUSY flags to the LOW ("0") state. ADC output coding can be program-selected as either binary or two's complement.

3.4.2 Throughput (Sample Rate) Factors

Total system throughput (sample rate) F_T can be expressed generally as:

$$F_T = 1/ [n X (T1 + T2 + T3)],$$

Where:
F_T = Throughput (samples per second, per channel)
N = Number of channels
T1 = 3111 settling delay . . . . . .8-120 µs (Gain x1 to x500)
T2 = 3111 A/D conversion time . . 19 µs
T3 = CPU (controlling processor) time invested per channel

If CPU time is negligible relative to the conversion sequence, then T3 is zero, and the expression for maximum throughput (N=1) is:

$$F_T \text{ (maximum)} = 1 / (T1 + T2)$$

Maximum throughput for a gain of "x1" then, 37,037 samples per second for a single input channel.

3.4.3 Interleaved (Pipelined) Operation

By allowing a new channel to settle before conversion of the previously selected channel has been completed, T_1 will be eliminated from F_T (maximum). The VMIVME-3111 control logic permits this to take place if the board is operated in the interleaved (pipelined) mode. Operating requirements for the interleaved mode are discussed in Section 4. By eliminating T_1, maximum throughput in this mode is:

$$F_T \text{ (maximum)} = 53 \text{ kHz.}$$

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3.4.4 Programmable Gain Amplifier

Voltage gain of the ADC channel is program-selectable as x1, x10, x100, and x500. The gain may be changed between channel selections by controlling
the two least significant bits (LSBs) (D00, D01) in the Gain Control Register located at relative address 0E (HEX). When changing the gain, refer to Section 4.5.3 "Gain and Channel Selection Precedence" for proper software sequence.

3.5 FRONT PANEL (P3) ANALOG INPUTS

Sixteen single-ended, high-level, analog input channels are available at the front panel through the P3 connector. By connecting the analog return in the remote device to the INPUT GROUND SENSE input (Figure 3.5-1) in the P3 connector, the single-ended lines can be operated as pseudo-differential inputs.

3.5.1 P3 Low Pass Filters and Input Multiplexer

The 16 front panel analog inputs are available with low pass filters. The outputs from the filters are then multiplexed into the analog configuration network
for selection into the ADC channel. To achieve maximum system accuracy with ***filtered analog inputs***, the sample rate should be limited to 300 Hz or less per channel (4.8 kHz for 16 channels). Higher sample rates will produce reflected "pumpback" currents at the inputs which can induce error voltages across the filter input resistors.

Each of the P3 analog inputs is selected by the four LSBs (D00 to D03) from the Control Register, these are shown as MUX A0 H through MUX A3 H in Figure 3.5-1. When set HIGH, CSR bit D07 selects the P3 multiplexer. Channel "00" is routed through the self-test multiplexer before appearing at the P3 multiplexer.

Signal pin assignments in the P3 connector are arranged for cable-compatibility with the 3V and 5V series signal conditioner assemblies.

3.5.2 Current Loop Receiving Mode

P3 analog inputs may be used as current loop receivers by replacing the filter capacitors with loop termination resistors. The resistance of the terminators should be selected to produce a total termination power dissipation

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not exceeding
5 W.

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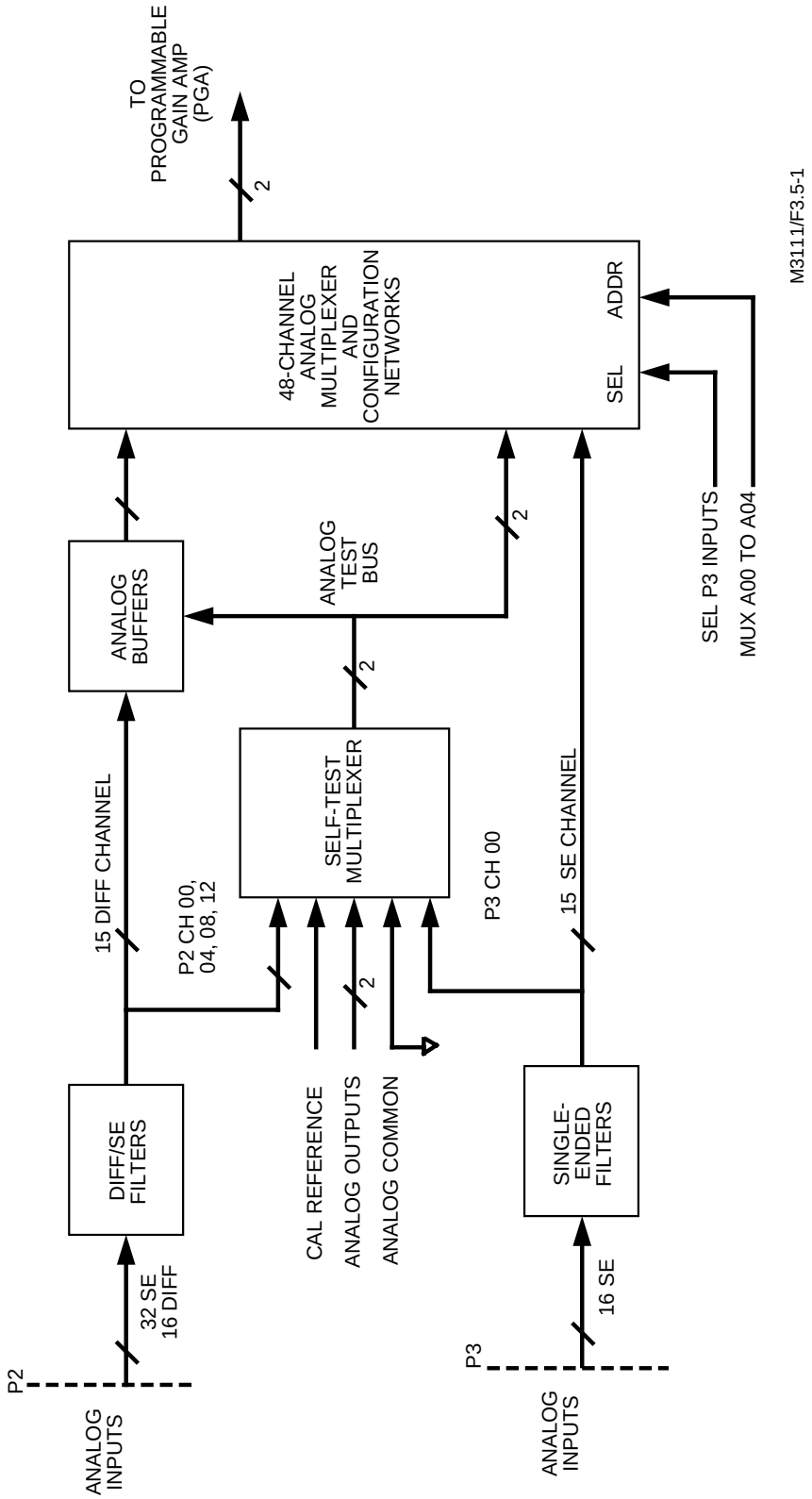


Figure 3.5-1. Analog Inputs and Signal Routing

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3.6 REAR PANEL (P2) ANALOG INPUTS

Analog inputs at the rear panel I/O connector P2 are configurable as 32 single-ended channels, 16 differential channels, or as a combination of both types. An external P2 GND SENSE line permits single-ended inputs to be operated as pseudo-differential inputs to eliminate the effect of potential differences between signal returns in different subassemblies within a VME system.

P2 input channels are selected with CSR bits D00 through D04, shown in Figure 3.5-1 as MUX A0 H through MUX A04 H. In order to test the four input multiplexers dedicated to P2 inputs, channels 00, 04, 08, and 12 are routed
through the self-test multiplexer. The P2 multiplexers are selected when the CSR D07 control bit is cleared LOW.

Buffered low pass filters, shown in Figure 3.6-1, are available options for all P2 analog inputs. Since the filters are buffered before the multiplexer, the throughput is not restricted by reflected multiplexer currents. Application programs, therefore, can realize the maximum sample rates permitted by the ADC timing controller.

3.7 ANALOG INPUTS SIGNAL ROUTING

After passing through the input multiplexers, the analog input signals are routed to analog configuration networks for final switching into the ADC channel.
To test the input multiplexers, four of the analog channels (one for each multiplexer device) are first switched through the self-test multiplexer shown in Figure 3.7-1.

3.7.1 Self-Test Multiplexer

For board-level self-testing, the self-test multiplexer (Figure 3.7-1) can switch five categories of signals to the analog input multiplexer.

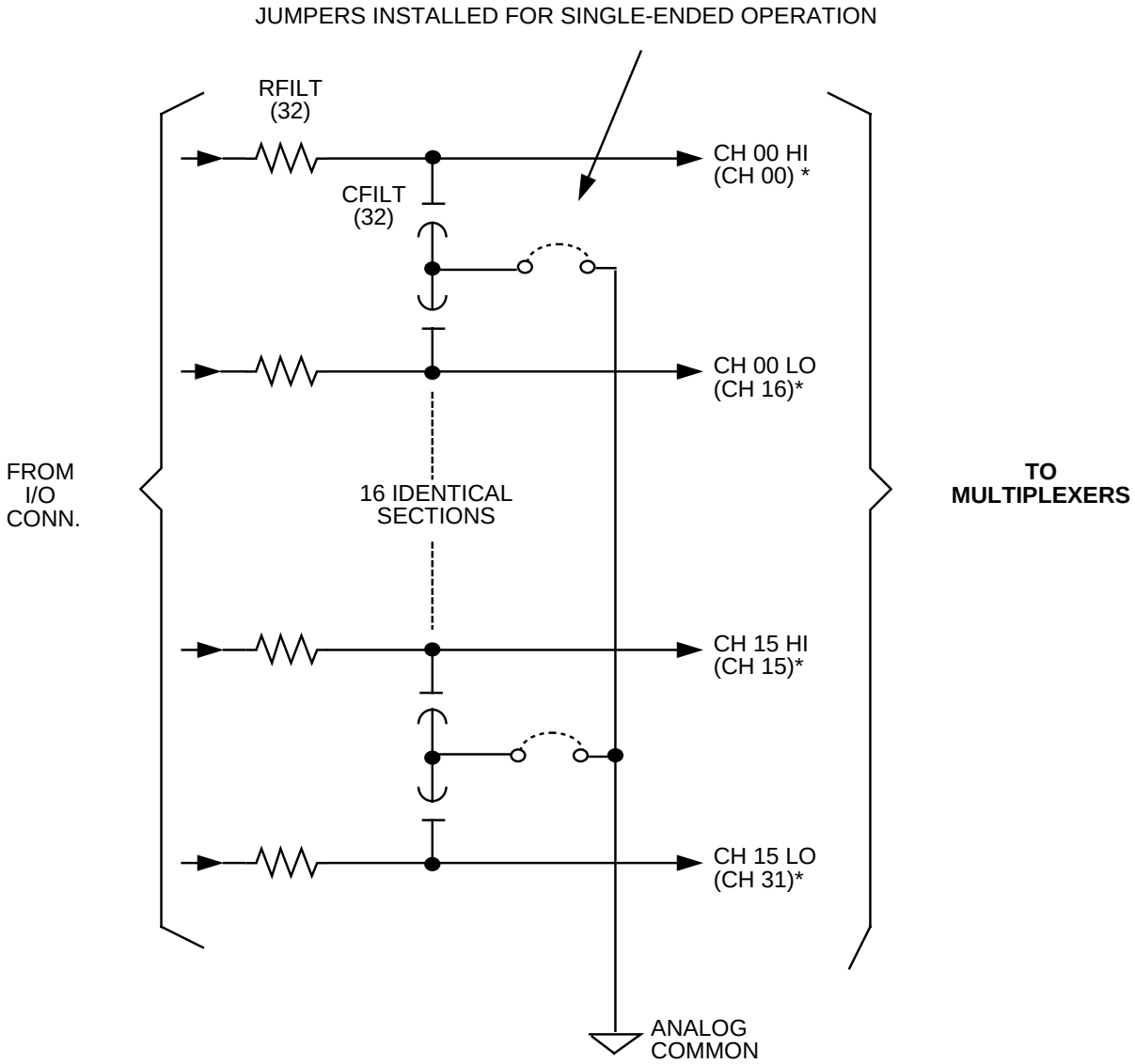
a. P2 input channels 00, 04, 08, 12
b. P3 input channel 00
c. Analog output channels 00 and 01
d. Calibration reference voltage
e. Internal signal return

During normal operation, the P2 and P3 inputs are simply switched back through their assigned multiplexer inputs. For loopback self-testing, the analog outputs are routed through the input multiplexers for measurement of actual output levels. The signal return input permits cancellation of zero offset

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errors at the multiplexer inputs. Operation of the self-test multiplexer is described in detail later in this section and in Section 4.

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*Single-ended channel.

M3111/F3.6-1

Figure 3.6-1. 32-Channel Filtered Analog Inputs

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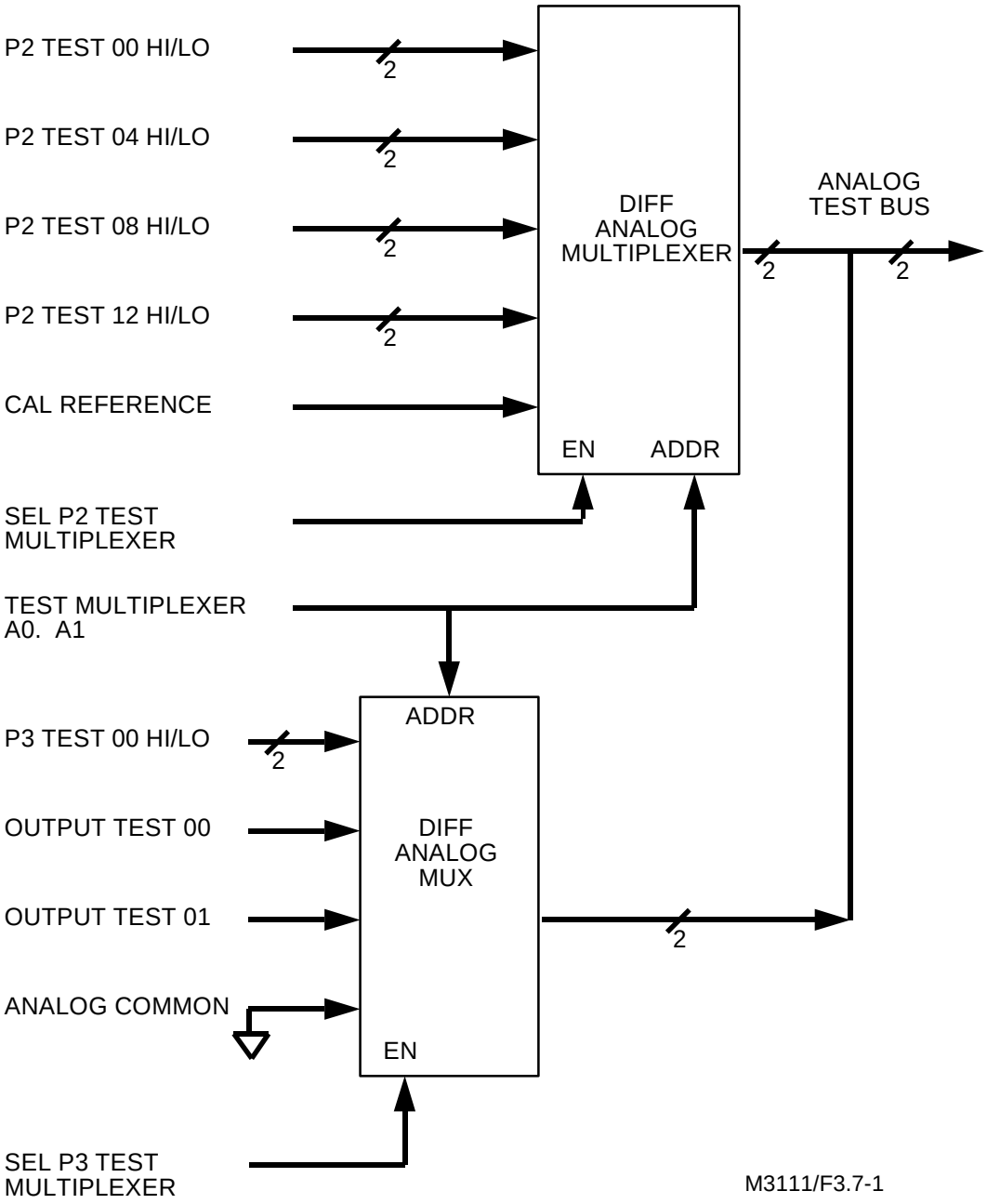


Figure 3.7-1. Self-Test Multiplexer

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3.7.2 Analog Configuration Network

The configuration networks are used to select the analog output channels, or the self-test reference voltage, in addition to the P2 and P3 input channels. The configuration networks are controlled by CSR control bits D08 through D10, shown in Figure 3.5-1 as MODE A0 H through MODE A2 H.

3.8 ANALOG OUTPUTS

In addition to the 32 analog inputs, two analog outputs also are available at the P2 connector. The analog outputs shown in Figure 3.8-1 are derived from two dedicated 12-bit DACs which appear as two 16-bit registers in the assigned VMIVME-3111 address space. Update rates for the output channels are limited only by the board access time and by the associated VME controller overhead.

3.8.1 DACs

Each DAC responds to the lower 12 bits of data in its WRITE-ONLY Control Register (readback is not supported). Data is right-justified, and is latched into the converter immediately when the register is updated. The two converters share a common precision voltage reference which can be user-configured for full-scale range, and for either bipolar or unipolar operation.

3.8.2 Output Buffers and Switches

Voltage levels from the DACs are buffered then switched to the P2 connector for routing through the system I/O cables. The output buffers are low leakage, precision operational amplifiers which can supply 10 mA of drive current over the full available output voltage range of ±10 V, and which can withstand sustained short circuits to ground without damage.

Output switches permit the analog outputs to be disconnected from P2 for "off-line" self-testing and for low impedance, single-point analog input/output system applications. To eliminate the effect of switch resistance on output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operation. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ±15 V supply rails.

Both outputs are monitored through the self-test multiplexer. By monitoring the outputs at the sense inputs of the output buffers, the measured output signals are correct in both the on-line and off-line operating modes.

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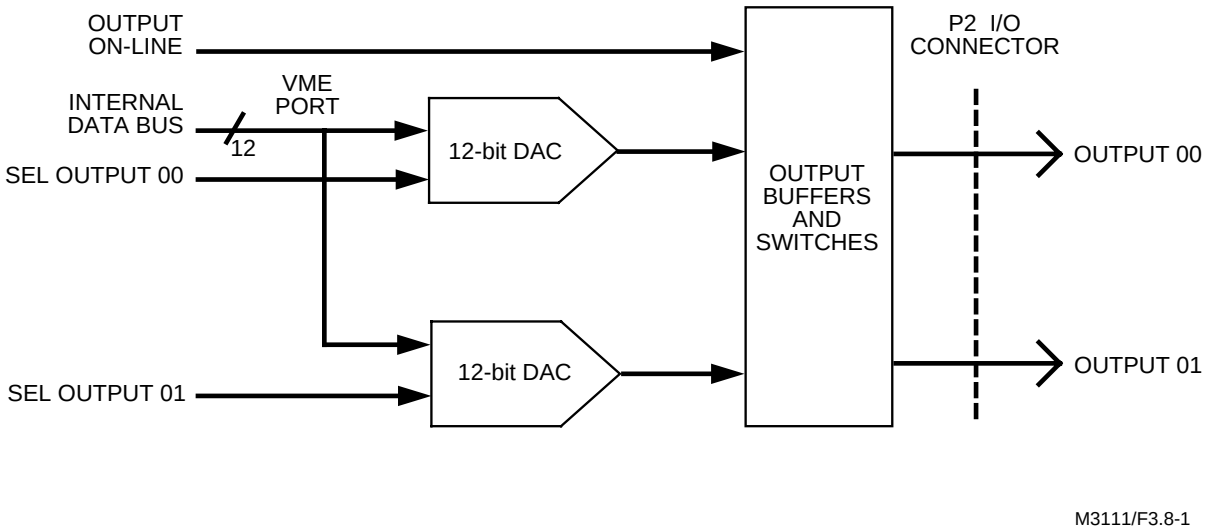


Figure 3.8-1. Analog Output Channels

3.9 BUILT-IN-TEST

Self-test provisions in the VMIVME-3111 design permit program-controlled verification of all active components on the board.

3.9.1 Self-Test Multiplexers

The signal routing paths and multiplexers involved in the board-level self-test are shown in Figure 3.7-1. The two analog outputs are connected by the self-test multiplexers to the low channel input of any of the analog input multiplexers. This arrangement permits any one of the analog outputs to be sampled by the ADC. It also verifies the operation of the analog input multiplexers by exercising them with known signal levels.

In addition to accepting the selected analog output signal, the self-test multiplexer permits the HIGH and LOW inputs of the Programmable Gain Amplifier (PGA) to be switched simultaneously to signal return. This feature provides a precision "zero" signal for software-correcting common zero offsets in the analog input channels.

Because the low channel inputs of the input multiplexers are shared by both the analog inputs and the self-test multiplexer signal, the corresponding input channels also are routed through the self-test multiplexer.

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3.9.2 Loopback Testing of Inputs and Outputs

By routing, the analog outputs through the analog input multiplexers (see previous section), all active components are exercised in a "loopback" arrangement. The controlling processor can perform a loopback test in either the on-line or off-line mode by sending a voltage-level code to a specific output channel, and by then verifying that the ADC produces the same code after sampling the signal. This technique is described in detail in Section 4.

3.9.3 Self-Test Standards

The on-board CAL TEST VOLTAGE REFERENCE is jumper-configurable to one of the following levels as nominally ±2.5 VDC, ±5.0 VDC, or ±10 VDC (actual voltages are slightly less than these in order to ensure in-range conversions during self-test and autocalibration). To provide both positive and negative references for testing and calibrating bipolar ranges, the CAL TEST voltage is routed to both the HIGH (noninverting) and LOW (inverting) inputs of the self-test multiplexer.

3.9.4 Gain Autocalibration

As shown in Figure 3.9.4-1, gain autocalibration is implemented by adjusting the reference input of the ADC. The output of the 12-bit autogain DAC is offset and attenuated to produce a gain adjustment range of ±1.2 percent which corresponds to an adjustment resolution of 0.0006 percent per DAC LSB. Control data for the gain DAC is written as 12 bits, right-justified, into a 16-bit WRITE ONLY register located at relative address 0A (HEX) in the VMIVME-3111 assigned address space.

3.9.5 Zero Autocalibration

In any high-gain, direct coupled, signal path, zero offset errors at the input are multiplied by the path gain and can, therefore, produce large output errors. For this reason, zero autocalibration in the VMIVME-3111 is performed at the input to the Programmable Gain Amplifier (PGA). As shown in Figure 3.9.4-1, the PGA accepts the output of the 12-bit autozero DAC. Autozero adjustment
range is ±10 mV, which correspond to an adjustment resolution of 4.7 µV per DAC LSB.

3.10 BUILT-IN POWER CONVERTER

Electrical power for the VMIVME-3111 analog networks is supplied by the DC-to-DC Converter shown in Figure 3.10-1. The converter transforms 5 V logic power into regulated and isolated ±15 VDC power with a load capacity of approximately 190 mA on each 15 V bus.

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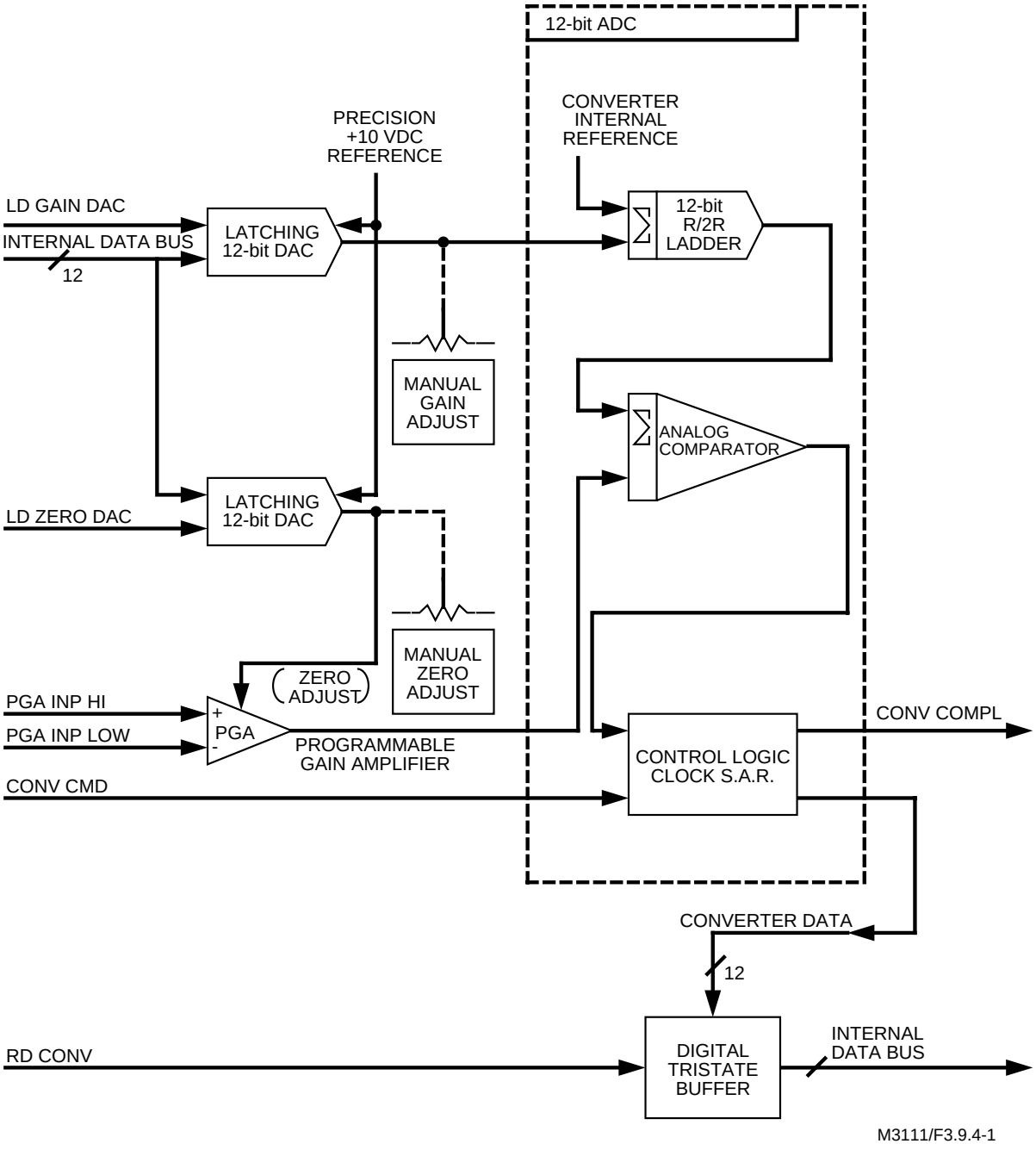


Figure 3.9.4-1. Converter Channel Autocalibration

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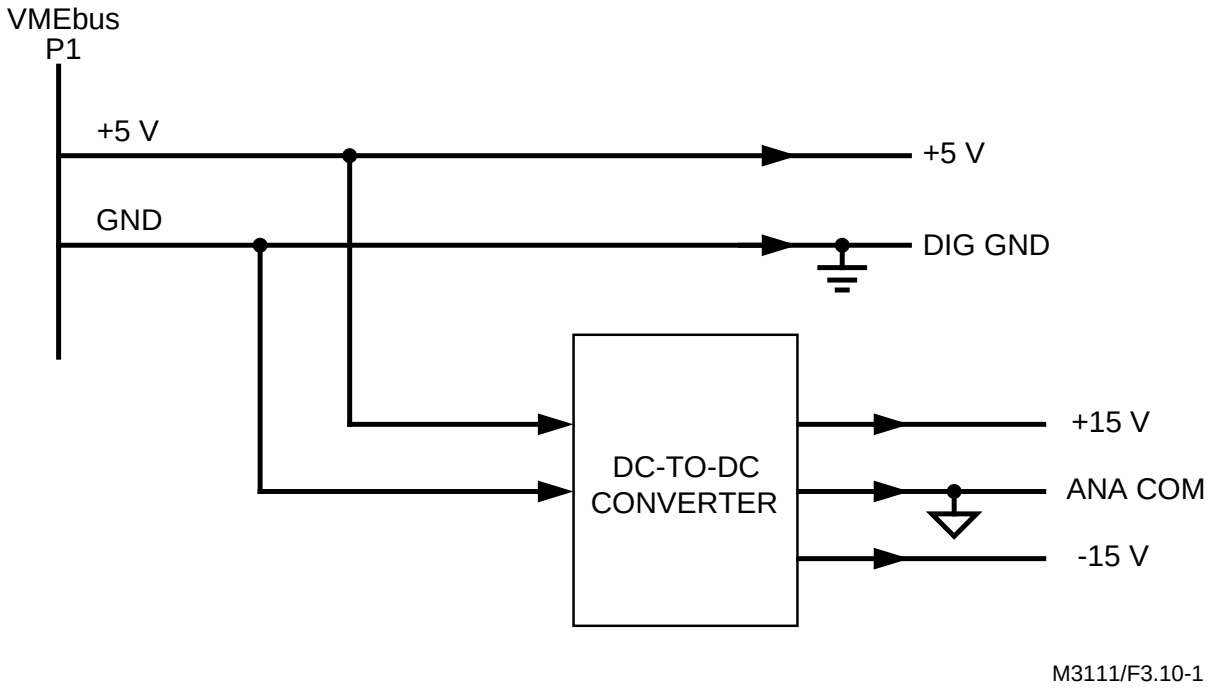


Figure 3.10-1. ±15 VDC Board Power

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-3111 BOARD

Communication with the VMIVME-3111 Analog-to-Digital Converter (ADC) Board takes place through sixteen contiguous 16-bit register locations which are mapped into the VME short I/O address space. Table 4.1-1 summarizes the functions of the communication registers which are discussed in detail in the following sections.

Table 4.1-1. Communications Register Map

RELATIVE ADDRESS* HEX	DEC	REGISTER NAME	ACTIVE BITS	ACCESS MODE
00	00	BOARD IDENTIFICATION	D08-D15	READ
02	02	CONTROL AND STATUS	D00-D15	READ/WRITE
04	04	OUTPUT D/A CHAN 00	D00-D11	WRITE
06	06	OUTPUT D/A CHAN 01	D00-D11	WRITE
08	08	AUTOZERO D/A CONV	D00-D11	WRITE
0A	10	AUTOGAIN D/A CONV	D00-D11	WRITE
0C	12	A/D CONVERTER DATA	D00-D11	READ
0E	14	PGA GAIN SELECTION	D00-D01	WRITE
10	16	INTERRUPT CONTROL	D00-D07	READ/WRITE
12-16	18-22	(RESERVED)		
18	24	INTERRUPT VECTOR	D00-D07	READ/WRITE
1A-1E	26-30	(RESERVED)		

*REGISTER ADDRESS is the sum of the RELATIVE ADDRESS and the BOARD ADDRESS.

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4.2 CONTROL AND STATUS REGISTER DESCRIPTIONS

The Communication Register located at relative address 02 is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

a. Analog input channel selection
b. Programmable gain selection
c. A/D conversion
d. Built-in-Test (BIT)
e. Analog outputs on-line/off-line
f. Analog outputs refresh rate
g. Front panel FAIL indicator
h. Board reset
i. Enable external trigger

The CSRs are 16 bits in length, and are summarized in Tables 4.2-1 and 4.2-2, respectively. The function of each control bit and status flag is described in detail subsequently in the associated programming discussions.

Table 4.2-1. Control Register Functions

CONTROL REGISTER DATA FORMAT

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0

CONTROL BIT	NAME	FUNCTION
D0	MUX A0 H	D0 through D4 select the analog input channel.
D1	MUX A1 H	
D2	MUX A2 H	
D3	MUX A3 H	
D4	MUX A4 H	
D5	BOARD RESET	When D5 is HIGH "1," all on-board flags and timing networks are cleared.
D6 *	START SETTLING H	Setting D6 to a "1" initiates the analog input settling (acquisition) interval.
D7	SELECT P3 MUX H	The front panel P3 analog inputs are selected when D7 is HIGH; rear panel P2 inputs are selected when D7 is LOW "0."

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Table 4.2-1. Control Register Functions (Concluded)

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CONTROL BIT	NAME	FUNCTION
D8	MODE A0 H	D8, D9, and D10 control the analog input mode, and are described in Section 4-4.
D9	MODE A1 H	
D10	MODE A2 H	
D11	OUTPUT ONLINE H	If D11 is set high "1," the analog outputs are connected to the P2 I/O connector. The analog outputs are disabled disconnected from P2 if D11 is low "0."
D12	TWO'S COMPL L	ADC coding format is Binary if D12 is high "1," Two's Complement if D12 is low "0."
D13 *	EN START CONV H	A single A/D conversion is enabled each time a "1" is written to this control bit. D13 will be ignored if the Converter Data Register (Table 4.1-1) contains unread data from a previous conversion. The current settling sequence will be sustained until the Converter Data Register is READ.
D14	FAIL LED L	The Fail LED is OFF if this bit is set to "1," and is ON if the bit is "0."
D15*	ENA EXT TRIG H	If this bit is set, it enables the P2 EXT TRIG L input signal to control the ADC. This permits external initiation of an ADC.

Each control bit is mapped directly into the corresponding bit in the Status Register unless it is indicated with "."

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Table 4.2-2. Status Register Flags

STATUS REGISTER DATA FORMAT

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

CONTROL BIT	NAME	FUNCTION
D0 *		
D1 *		
D2 *		
D3 *		
D4 *		
D5 *		
D6	SETTLING BUSY H	When set to a "1," this flag indicates that the input settling sequence is in progress, and that START SETTLING commands will be ignored. The START SETTLING command will be recognized if this flag is LOW "0."
D7 *		
D8 *		
D9 *		
D10 *		
D11 *		
D12 *		
D13	CONV BUSY H	Writing a "1" to the EN START CMD control bit causes the D13 flag to be set to "1." The flag will remain set until the next conversion has been completed and new data is available in the Converter Data Register. (The settling sequence will not run to completion if this flag is not set.)
D14 *		
D15	NEW DATA RDY	When set to a "1," this flag indicates that a conversion has been completed, and that data is available in the Converter Data Register. Reading the ADC DATA register clears this flag.

*The corresponding Control Register bit is mapped directly to this flag.

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4.3 INITIALIZATION

When SYSTEM RESET is applied to the board, the Control Register and all converter flags are cleared to the LOW state ("0"). The clearing process is sequential and a delay of at least 50 µs should be allowed before attempting to control the board after a RESET has occurred. An independent BOARD RESET can be generated by setting the BOARD RESET control bit to "1."

4.4 ANALOG INPUT MODES

Control of the analog input multiplexer configuration is provided by the three MODE selection bits: D8, D9, and D10 in the CSR. Table 4.4-1 lists the control codes for the available modes. Each mode is summarized here, and then it is described in detail in the section in which the mode is applied.

ZEROED INPUTS: Each input multiplexer is provided with a test input. In the ZEROED INPUTS mode, all test inputs are grounded to signal return (zero signal) on the board. This provides a zero reference for the autozero operations.

P2 DIFFERENTIAL: P2 input channels are configured as differential input pairs. CSR control bits D0 through D3 select one of 16 input channels. P3 inputs are configured as 16 single-ended channels.

P2 SINGLE-ENDED: P2 input channels are configured as single-ended inputs. CSR control bits D0 through D4 select one of 32 input channels. P3 inputs are configured as 16 single-ended channels.

POSITIVE REFERENCE: The on-board positive voltage reference is selected, either for autogain adjustment operations, or for board-level self-test.

NEGATIVE REFERENCE: The on-board negative voltage reference is selected for bipolar autogain adjustments.

ANALOG OUTPUT CHAN 00: Analog output channel "00" is connected to the test bus which can be routed through any of the P2 or P3 input multiplexers for loopback testing.

ANALOG OUTPUT CHAN 01: Analog output channel "01" is connected to the test bus for loopback testing.

RESERVED: This mode applies signal return (zero) to the test bus.

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Table 4.4-1. Analog Input Control Modes

ANALOG INPUT MODE	INPUT MODE ADDRESS (CSR CONTROL BITS) HEX	MODE A2 H	MODE A1 H	MODE A0 H
ZEROED INPUTS	0	0	0	0
P2 DIFFERENTIAL	1	0	0	1
P2 SINGLE-ENDED	2	0	1	0
POSITIVE REFERENCE	3	0	1	1
NEGATIVE REFERENCE	4	1	0	0
ANALOG OUTPUT CHAN 00	5	1	0	1
ANALOG OUTPUT CHAN 01	6	1	1	0
RESERVED (ZERO)	7	1	1	1

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4.5 ACCESSING THE ANALOG INPUT CHANNELS

Selection of each analog input channel requires program control of the following VMIVME-3111 Board parameters:

a. Analog Input Mode
b. Channel Gain
c. Channel and Input Connector (P2, P3) Selection

The analog input mode is discussed in Section 4.4. Definition of the remaining channel selection board parameters is described in this section.

4.5.1 Gain Selection

Analog-to-Digital Converter (ADC) gain is program-selectable as x1, x10, x100, or x500. The two least significant control bits (D1 and D0) of the Gain Selection Register at board-relative address 0E (HEX) control the gain as:

ADC GAIN	PGA REGISTER D1	D1
x1	0	0
x10	0	1
x100	1	0
x500	1	1

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Selection of a specific converter gain serves to divide the jumper-selected Full-Scale Range (FSR) by the selected gain. For example, if a VMIVME-3111 board has a ±5 V FSR, a gain of x100 would produce an effective FSR of ±0.05 V.

4.5.2 Channel Selection

Selection of the analog input channels is controlled by the five least significant control bits (D00 through D04) of the Control and Status Register (CSR), by the SEL P3 multiplexer control bit D7, and by the three MODE control bits D8, D9, and D10. The selection requirements for each input channel are shown in Table 4.5.2-1.

CSR control bit D7 is used to select either the front panel P3 analog inputs (D7 = "1"), or the rear panel P2 inputs (D7 = "0"). If the P3 inputs and control Mode-1 are selected, then CSR control bits D0 through D3 select one of the 16 single-ended inputs available at that connector.

P2 inputs can be configured as either differential or single-ended channels. In control Mode-1 the differential configuration is selected, and CSR D0 through D4 selects one of 16 differential input channels.

Each P2 differential input channel occupies the connector pins that would otherwise be allocated to two single-ended channels. Therefore, if the P2 inputs are configured as *a combination of both differential and single-ended input channels,* then the two single-ended channels which correspond to each differential channel are not available as inputs.

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Table 4.5.2-1. Analog Input Channel Selection

CONTROL REGISTER						SELECTED INPUT CHANNEL NUMBER		
						P2 (CSR D7 = 0)		P3
						SINGLE-ENDED	DIFFERENTIAL	(CSR D7 = 1)
HEX	D04	D03	D02	D01	D00	(MODE = 2)*	(MODE = 1)*	(MODE = 1)*
00	0	0	0	0	0	00	00	00
01	0	0	0	0	1	01	01	01
02	0	0	0	1	0	02	02	02
03	0	0	0	1	1	03	03	03
04	0	0	1	0	0	04	04	04
05	0	0	1	0	1	05	05	05
06	0	0	1	1	0	06	06	06
07	0	0	1	1	1	07	07	07
08	0	1	0	0	0	08	08	08
09	0	1	0	0	1	09	09	09
0A	0	1	0	1	0	10	10	10
0B	0	1	0	1	1	11	11	11
0C	0	1	1	0	0	12	12	12
0D	0	1	1	0	1	13	13	13
0E	0	1	1	1	0	14	14	14
0F	0	1	1	1	1	15	15	15
10	1	0	0	0	0	16 (00)**		
11	1	0	0	0	1	17 (01)		
12	1	0	0	1	0	18 (02)		
13	1	0	0	1	1	19 (03)		
14	1	0	1	0	0	20 (04)		
15	1	0	1	0	1	21 (05)		
16	1	0	1	1	0	22 (06)		
17	1	0	1	1	1	23 (07)		
18	1	1	0	0	0	24 (08)		
19	1	1	0	0	1	25 (09)		
1A	1	1	0	1	0	26 (10)		
1B	1	1	0	1	1	27 (11)		
1C	1	1	1	0	0	28 (12)		
1D	1	1	1	0	1	29 (13)		
1E	1	1	1	1	0	30 (14)		
1F	1	1	1	1	1	31 (15)		

*

MODE	D10	D9	D8
1	0	0	1
2	0	1	0

**If P2 is configured with a combination of single-ended *and* differential channels, the single-ended channels that are indicated with a differential channel (in parentheses) are no longer available as inputs.

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4.5.3 Gain and Channel Selection Precedence

To prevent driving the amplifiers into saturation and thus reduce the accuracy of the conversion, comply with one of the following methods when changing the gain setting.

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Method One

a. Increasing the Gain:
First, select the Channel, then select the increased Gain.

b. Decreasing the Gain:
First, select the lower Gain, then select the Channel.

Method Two

When changing the Gain:
First, select the Gain of x1; second, select the channel; then third, select the required Gain.

4.6 CONTROLLING AND READING THE ADC

Two principal methods are available for controlling the ADC on the VMIVME-3111 board. For applications in which conversion speed is not a critical factor, the basic method usually will provide suitable performance. This is the simpler of the two methods to implement and will produce a maximum throughput on the order of 35 kHz (35,000 samples per second).

If higher throughput is essential, the interleaved (pipelined) method can be used. The interleaved control approach permits the settling interval of a new channel to begin while a conversion is in progress. This technique eliminates the settling interval from the throughput equation (Section 3), and raises the throughput to approximately 59 kHz.

4.6.1 ADC Timing

All basic timing operations for the ADC are performed by the on-board controller. Control of the converter consists of the "handshake" programming sequences described in the following paragraphs.

4.6.2 ADC Controls and Flags

The following controls, flags, and registers are available for use in controlling the ADC (controls and flags are summarized in Tables 4.2-1 and 4.2-2).

CONTROLS (CONTROL REGISTER)

a. START SETTLING H D06
b. TWO'S COMPL L.....D12
c. EN START CONV H D13

FLAGS (STATUS REGISTER)

a. SETTLING BUSY H D06
b. CONV BUSY H D13
c. NEW DATA RDY H.....D15 (Set when data is available in the A/D Data Register)

*Effective only upon writings (i.e., "strobed").

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CONVERTER DATA REGISTER

a. 16-bit Read-Only Register at relative address 0C (HEX). Data in this register is 12 bits, right-justified. D12 through D15 are always "0" in the binary data mode and are sign extensions in the two's complement data mode.

The START SETTLING and EN START CONV controls are essentially strobes and are effective only at the moment of writing to the Control Register. Although supplied as two separate control bits for flexibility, these controls usually are written to the register simultaneously along with the operational mode and channel selections.

Figures 4.6.2-1 and 4.6.2-2 illustrate a measurement sequence which uses the basic conversion control method. The sequence is simplified by the fact that only the NEW DATA RDY flag must be monitored in order to determine when each conversion has been completed.

The interleaved (pipelined) control method is presented in Figures 4.6.2-3 and 4.6.2-4. A higher throughput is achieved by using a somewhat more complex control sequence. With this method, both the SETTLING BUSY and NEW DATA RDY flags are monitored.

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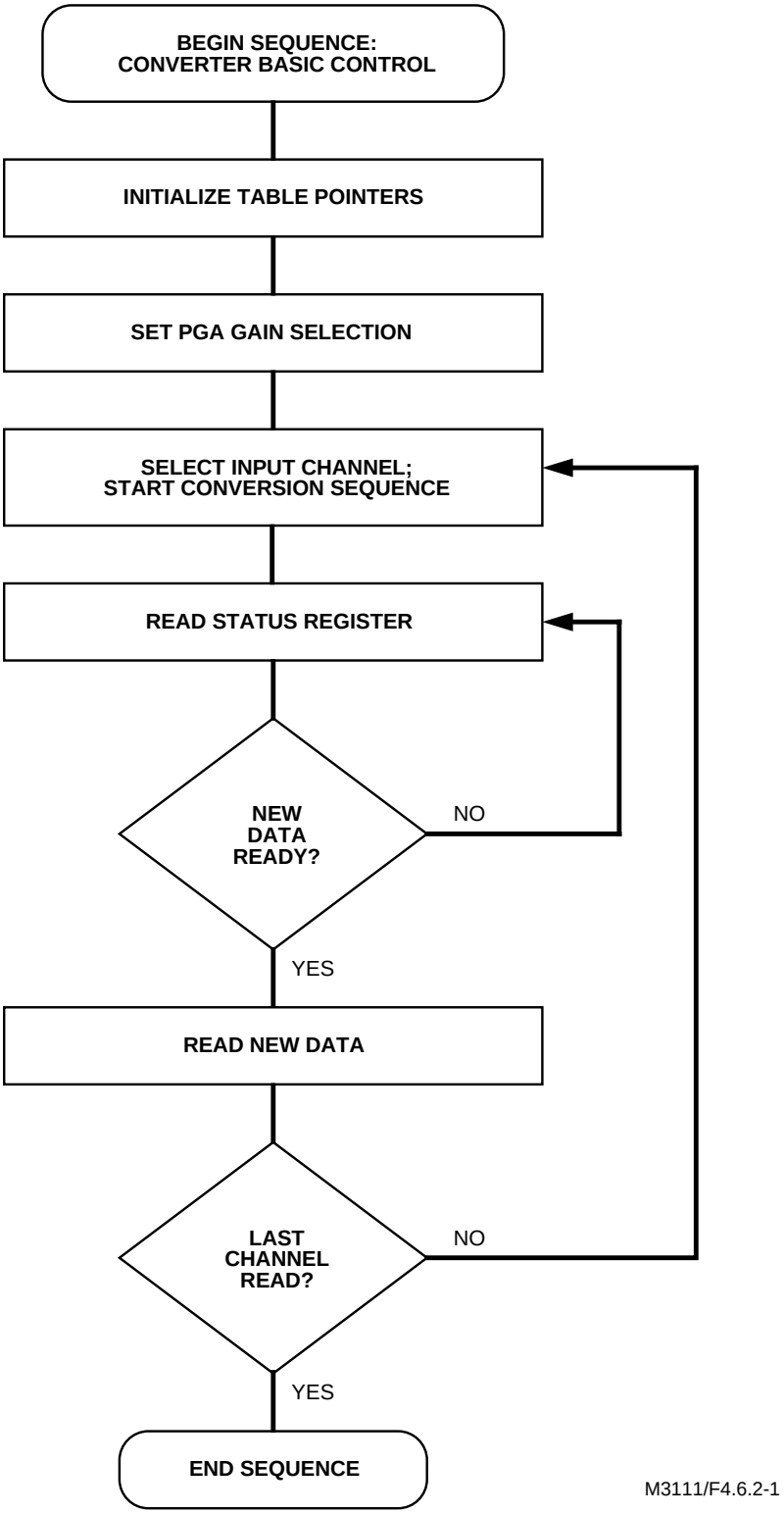


Figure 4.6.2-1. Program Flowchart - Basic ADC Control Sequence

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```
                LEA     #$FBFF000E, A1      PGA GAIN SELECTION REG
                LEA     #$FBFF0002, A2      CONTROL/STATUS REG
                LEA     #$FBFF000C, A3      A/D CONVERTER DATA REG
                LEA     #$FB000000, A4      DATA STORAGE ADDRESS
                MOVE.W  #$7240, D1          CONTROL WORD CH.00
                MOVE.W  #$725F, D2          CONTROL WORD CH.31
                MOVE.W  #$0000, (A1)        SELECT GAIN = X1
STRTSEQ         MOVE.W  D1, (A2)            WRITE CONTROL WORD
RDSTATUS        MOVE.W  (A2), D3            READ STATUS REG
                BTST    #15, D3             IS NEW DATA READY?
                BEQ.S   RDSTATUS            IF NOT CHECK AGAIN
                MOVE.W  (A3), (A4)+         READ AND STORE DATA
                CMP.W   D1, D2              LAST CHANNEL READ?
                BEQ.S   ENDSEQ              IF SO END SEQUENCE
                ADDQ.W  #$1, D1             GET NEXT CONTROL WORD
                BRA     STRTSEQ             DO NEXT CHANNEL
ENDSEQ          END
```

M3111/F4.6.2-2

Figure 4.6.2-2. Program Example - Basic ADC Control Sequence

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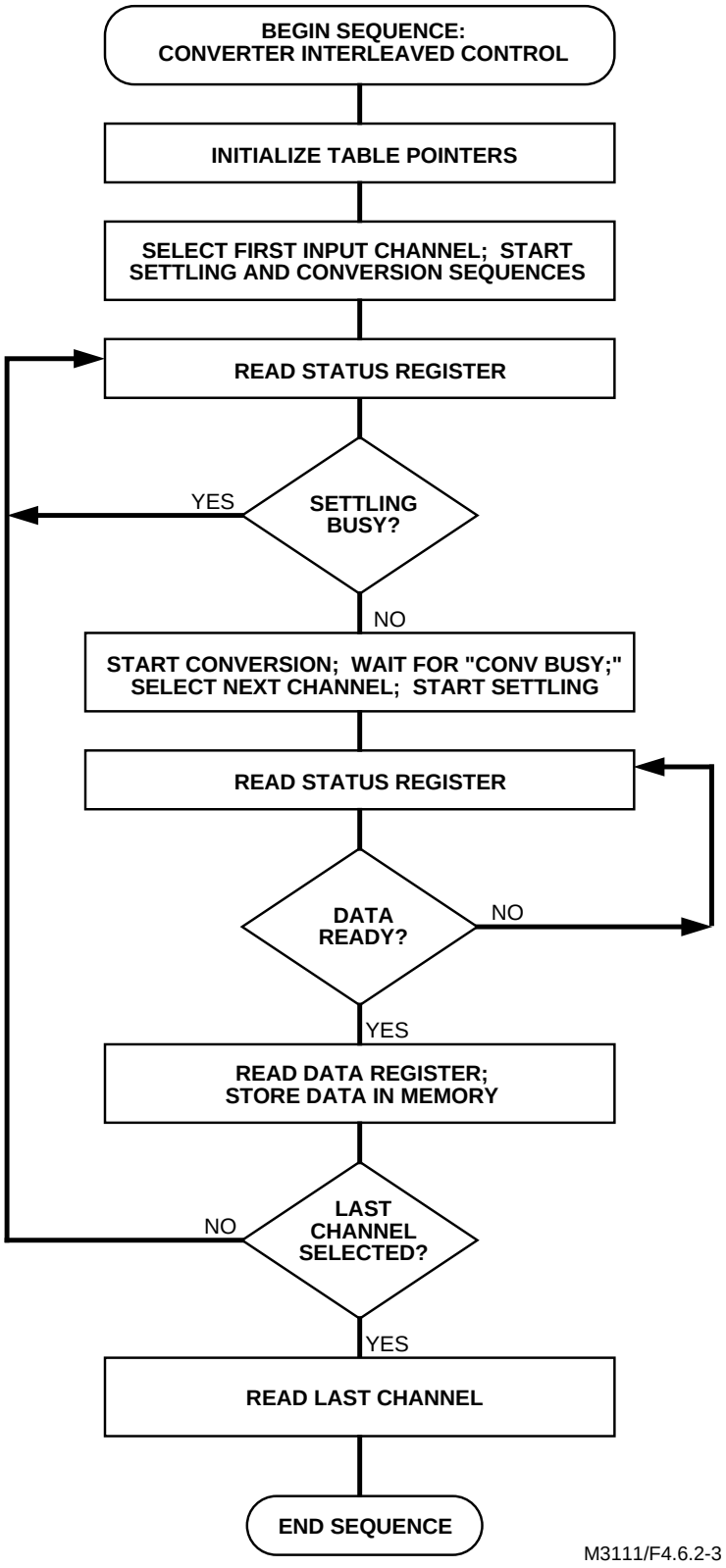


Figure 4.6.2-3. Program Flowchart - Pipelined ADC Control Sequence

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```
                LEA         #$FBFF000E, A1      PGA GAIN SELECTION REG
                LEA         #$FBFF0002, A2      CONTROL/STATUS REG
                LEA         #$FBFF000C, A3      A/D CONVERTER DATA REG
                LEA         #$FB000000, A4      DATA STORAGE ADDRESS
                MOVE.W      #$5240, D1          CONTROL WORD CH.00
                MOVE.W      #$525F, D2          CONTROL WORD CH.31
                MOVE.W      #$7200,D4           CONTROL WORD CONVERT
                MOVE.W      #$0000, (A1)        SELECT GAIN = X1
STRTSEQ         MOVE.W      D1, (A2)            WRITE CONTROL WORD
RDSTAT1         MOVE.W      (A2), D3            READ STATUS REG
                BTST        #6, D3              IS SETTLING BUSY?
                BNE.S       RDSTAT1             IF SO CHECK AGAIN
                MOVE.W      D4, (A2)            START CONVERSION
                ADD.W       #$1, D1             SELECT NEXT CHANNEL
                ADD.W       #$1, D4             SELECT NEXT CHANNEL
                MOVE.W      D1, (A2)            START SETTLING THAT CHANNEL
RDSTAT2         MOVE.W      (A2), D3            READ STATUS REG
                BTST        #15, D3             IS NEW DATA READY HIGH?
                BEQ.S       RDSTAT2             IF NOT CHECK AGAIN
                MOVE.W      (A3), (A4)+         READ AND STORE DATA
                CMP.W       D1, D2              LAST CHANNEL READ?
                BEQ.S       ENDSEQ              IF SO END SEQUENCE
                ADDQ.W      #$1, D1             GET NEXT CONTROL WORD
                BRA         STRTSEQ             DO NEXT CHANNEL
ENDSEQ          END
```

M3111/F4.6.2-4

Figure 4.6.2-4. Program Example - Pipelined ADC Control Sequence

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4.6.3 Reading ADC Codes

The data format which applies when reading the ADC Data Register is shown in Table 4.6.3-1. Coding can be straight binary, offset binary, or two's complement, depending upon the configuration of the ADC jumper selections and the state of the TWO'S COMPL control bit. Table 4.6.3-1 also summarizes the converter output codes that are produced at major points within the full-scale ranges shown.

For any offset binary converter output code (BIPOLAR RANGE), the associated input voltage is obtained with the expression:

$$\text{INPUT (Volts)} = -E_{FSR}/2 + [E_{FSR} \times (\text{DECIMAL OUTPUT CODE})] / [4096 \times \text{GAIN}]$$

where E_{FSR} is the full-scale range voltage (e.g.: E_{FSR} = 10 Volts for the ±5 V range), and gain is the program-selected gain of the Programmable Gain Amplifier (PGA).

The input voltage for a straight binary code (UNIPOLAR RANGE) is:

$$\text{INPUT (Volts)} = E_{FSR} \times [\text{ DECIMAL OUTPUT CODE }] / [4096 \times \text{GAIN}].$$

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Table 4.6.3-1. ADC Format and Coding

ADC DATA FORMAT

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*												

* = Zero (binary) or extended sign (two's complement).

ADC CODING

UNIPOLAR RANGES — STRAIGHT BINARY

INPUT	0 TO +10 V	0 TO +5 V	D15			D0
+FS-1 LSB	+9.9975 V	+4.9988 V	0000	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	0000	0000	0000	0001

BIPOLAR RANGES — OFFSET BINARY

INPUT	±10 V	±5 V	D15			D0
+FS-1 LSB	+9.9951 V	+4.9976 V	0000	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	0000	1000	0000	0001
ZERO	+0.0000 V	0.0000 V	0000	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	0000	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	0000	0000	0000	0000

BIPOLAR RANGES — TWO'S COMPLEMENT

INPUT	±10 V	±5 V	D15			D0
+FS-1 LSB	+9.9951 V	+4.9976 V	0000	0111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	0000	0000	0000	0001
ZERO	+0.0000 V	0.0000 V	0000	0000	0000	0000
-1 LSB	-0.0049 V	0.0024 V	1111	1111	1111	1111
-FS+1 LSB	-9.9951 V	-4.9976 V	1111	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	1111	1000	0000	0000

M3111/T4.6.3-1

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4.6.4 External Trigger Operation

The board may be programmed to respond to an external TTL active low or "zero" pulse. For external trigger operation, the user programs the channel, mode and Start Settling H bits of the CSR. Do not set the Enable Start Convert H bit D12 of the CSR, instead set the Enable External Trigger H bit D15 of the CSR to a "one." An external logic level "zero" trigger pulse of a least 100 ns may then be input to the board via the P2 connector pin A28. On the board, this input pin for external trigger is pulled high through a 4.7 k resistor to +5 V. The active low pulse will initiate a single A/D conversion. At the completion of the conversion, the new data ready flag will be set high.

In addition to enabling the External Trigger operation in the CSR, jumpers J41 and J42 must be configured. J41 must be omitted. J42 pin 1 should be connected to J42 pin 2, which connects the external trigger return (P2 pin C28) to the board ground. For location of the jumpers, refer to Section 5, Figure 5.4-1.

Be aware that the P2 I/O pins are sometimes used by other boards to perform different I/O functions. From a systems viewpoint, verify that multiple drivers/receivers are not using these user-defined P2 I/O lines: P2-A28 and P2-C28.

4.7 CONTROLLING THE ANALOG OUTPUTS

The analog output channels on the VMIVME-3111 appear to the controlling processor as two 16-bit data words in the address space assigned to the VMIVME-3111 board. The communication register map shown in Table 4.1-1 lists the board-relative address of each output channel.

4.7.1 Writing to Outputs

Digital codes are recognized in the Analog Output Registers as 12-bit binary right-justified data. Data written to the upper four most significant bits (D12 through D15) will be ignored. Table 4.7.1-1 shows the Digital-to-Analog Converter (DAC) coding conventions used by the DAC. Each output will respond to a new code within 15 µs after the code is written to the Output Register.

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Table 4.7.1-1. DAC Data Format and Coding

DAC DATA FORMAT

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DAC CODING

UNIPOLAR RANGES

OUTPUT	0 TO +10 V	0 TO +5 V
+FS-1 LSB	+9.9975 V	+4.9988 V
+1/2 FS	+5.0000 V	+2.5000 V
+1 LSB	+0.0024 V	+0.0012 V

STRAIGHT BINARY

D15			D0
XXXX	1111	1111	1111
XXXX	1000	0000	0000
XXXX	0000	0000	0001

BIPOLAR RANGES

OUTPUT	±10 V	±5 V
+FS-1 LSB	+9.9951 V	+4.9976 V
+1/2 FS	+5.0000 V	+2.5000 V
+1 LSB	+0.0049 V	+0.0024 V
ZERO	+0.0000 V	0.0000 V
-FS+1 LSB	-9.9951 V	-4.9976 V
-FS	-10.0000 V	-5.0000 V

OFFSET BINARY

D15			D0
XXXX	1111	1111	1111
XXXX	1100	0000	0000
XXXX	0000	0000	0001
XXXX	1000	0000	0000
XXXX	0000	0000	0001
XXXX	0000	0000	0000

x = "Don't care."

M3111/T4.7.1-1

4.7.2 Off-Line Operation

Setting the OUTPUT ON-LINE control bit HIGH (Table 4.2-1) connects the analog outputs to the P2 I/O connector for normal system cooperation. Clearing the bit LOW disconnects the analog outputs from P2. However, the output buffers can still be monitored through the self-test multiplexers.

4.8 SELF-TESTING THE VMIVME-3111 BOARD

Built-in-Test (BIT) provisions include loopback testing and the measurement of analog input offset voltages and on-board precision reference voltages. These capabilities permit self-contained, board-level verification of performance.

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4.8.1 Loopback Testing of Inputs and Outputs

By routing the analog outputs through the input multiplexers, the operation of all active components on the VMIVME-3111 board can be verified. This "loopback" test is performed by selecting either the ANALOG OUTPUT CHAN 00 or the ANALOG OUTPUT CHAN 01 in the analog input mode shown in Table 4.4-1. The selected output channel can then be exercised by the controlling processor, and monitored by the VMIVME-3111 ADC to verify that all components in the loopback signal path are operating correctly. This technique is illustrated in Figures 4.8.1-1 and 4.8.1-2.

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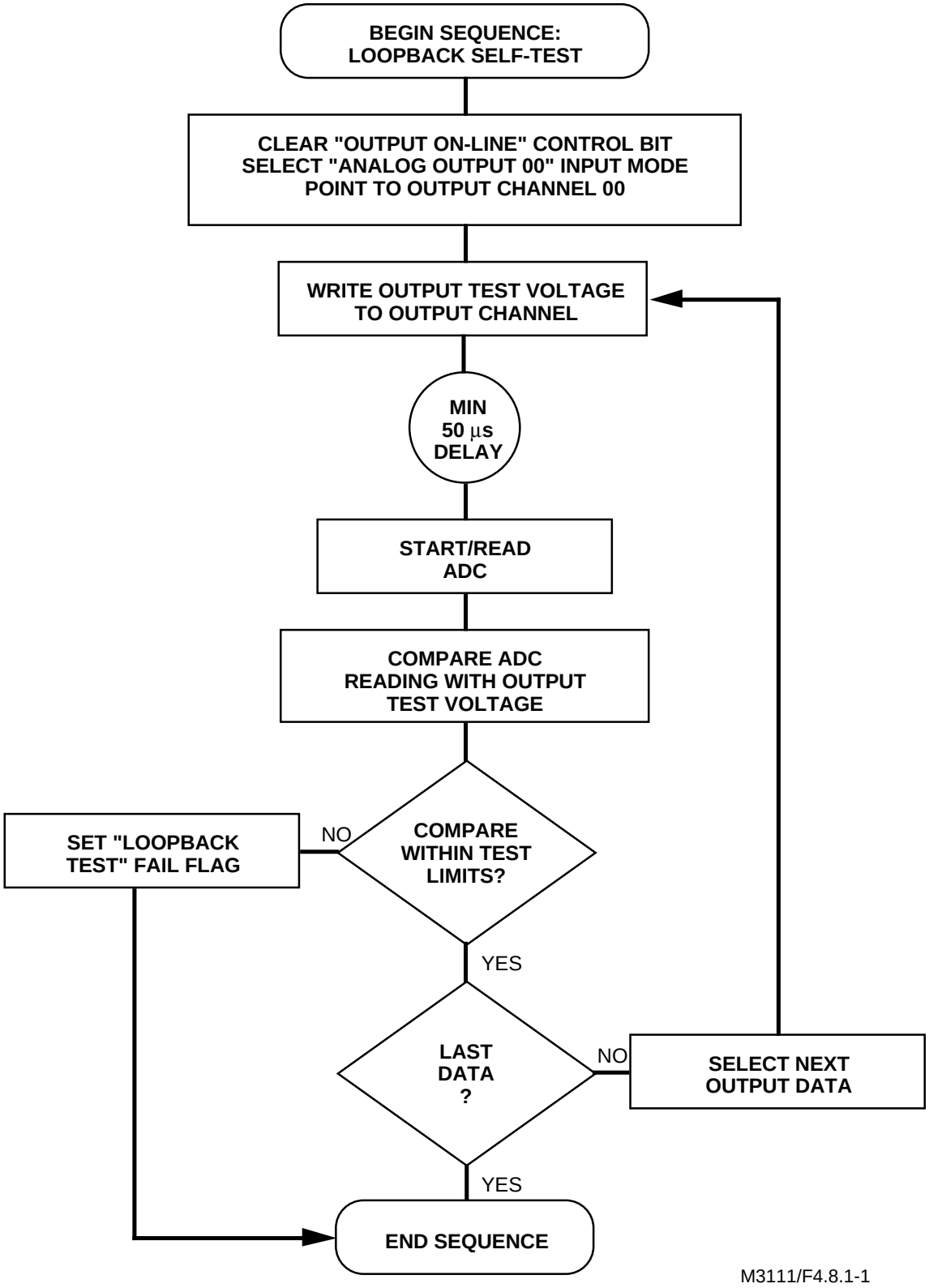


Figure 4.8.1-1. Program Flowchart - Loopback Self-Test

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```
            LEA     #$FBFF0002, A1      GET UUT CSR ADDRESS
            LEA     $FBFF000C, A5       A/D DATA ADDRESS
            MOVE.W  #$0000, $FBFF000E   SELECT GAIN = X1
            BCLR    #1, TFLAGS          CLEAR LOOPBACK FAIL FLAG
            MOVE.W  #$75C0, D3          CONTROL WORD D/A CH.00
            CLR.W   D1                  CLEAR DATA REGISTER
            LEA     #$FBFF0004, A3      ADDRESS CHANNEL 00
STARTSEQ    MOVE.W  D1, (A3)            WRITE DATA OUT
            MOVE.W  #$FF, D4            SET DELAY
DELAY       SUB.W   #$1, D4             DELAY
            BNE.W   DELAY               END DELAY?
            MOVE.W  D3, (A1)            WRITE CONTROL WORD
READ        MOVE.W  (A1), D5            READ STATUS REGISTER
            BTST    #15, D5             IS NEW DATA READY?
            BNE     READ                IF NOT CHECK AGAIN
            MOVE.W  (A5), D2            READ NEW DATA
            SUB.W   D1, D2              SUBTRACT WRITE FROM READ
            BPL     POS                 IF POS TRUE DON'T NEGATE
            NEG.W   D2                  NEGATE NEG TRUE TO POS TRUE
POS         SUB.W   #$4, D2             COMPARE TO MAX ERROR VALUE
            BGT     FAIL                FAIL IF > MAX ERROR VALUE
            ADD.W   #$0001, D1          INCREMENT DATA REGISTER
            CMP.W   #$1000, D1          DONE ALL DATA?
            BNE.W   STARTSEQ            IF NOT DO MORE DATA
            BRA.S   ENDSEQ              GO TO END SEQUENCE
FAIL        BSET    #1, TFLAGS          SET LOOPBACK FAIL FLAG
ENDSEQ      END                         END SEQUENCE
```

M3111/F4.8.1-2

Figure 4.8.1-2. Program Example - Loopback Self-Test

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4.8.2 Calibration Self-Testing

On-board precision reference voltages permit calibration, verification, and autocalibration of the ADC and the analog output channels during system operation. Reference voltages on the VMIVME-3111 board are jumper-selected for nominal ranges of as ±2.5 VDC, ±5 VDC, or ±10 VDC. The actual voltages are adjusted to be approximately 0.49 percent below their nominal values in order to produce full-range readings which are 10 (0A HEX) counts *below full-scale.* This is done in order to minimize the occurrence of ambiguous "end-of-scale" readings.

Table 4.8.2-1. Calibration Test Limits

NOMINAL SELF-TEST STANDARD (VDC)	REFERENCE VOLTAGE (VDC)	FULL-SCALE RANGE (VDC)	ACCEPTANCE RANGE (HEX)					
			±0 LSB (NOMINAL)	±2 LSB MAX	±2 LSB MIN	±4 LSB MAX	±4 LSB MIN
+10.0	+9.9512	0 TO +10	0FEC	0FEE	0FEA	0FF0	0FE8
		±10	0FF6	0FF8	0FF4	0FFA	0FF2
+5.0	+4.9756	0 TO +5	0FEC	0FEE	0FEA	0FF0	0FE8
		±5	0FF6	0FF8	0FF4	0FFA	0FF2
+2.5	+2.4878	±2.5	0FEC	0FEE	0FEA	0FF0	0FE8
ZERO	0.0000	ALL BIPOLAR RANGES	0800	0802	07FE	0804	07FC
ZERO	0.0000	ALL UNIPOLAR RANGES	0000	0002	0000	0004	0000
-2.5	-2.4878	±2.5	000A	000C	0008	000E	0006
-5.0	-4.9756	±5	000A	000C	0008	000E	0006
-10.0	-9.9512	±10	000A	000C	0008	000E	0006

All reference voltages are measured with converter PGA gain adjusted to unity (x1).

M3111/T4.8.2-1

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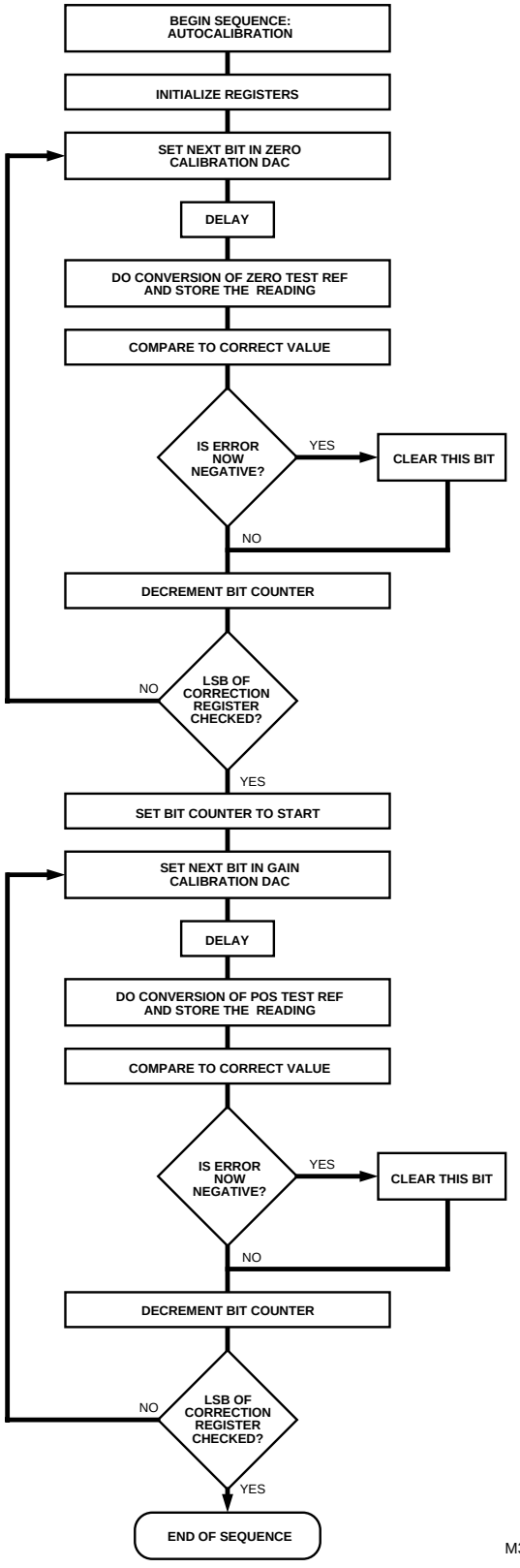


Figure 4.8.2-1. Program Flowchart - Converter Autocalibration

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```
*****************************************************************************************************************
*****************************************************************************************************************

AUTOCAL         PROMPT          AUTOMSG             SHOW DOING AUTOCALIBRATION
                LEA             UUT.AZ, A1          GET UUT AUTOZERO DAC ADDR
                LEA             UUT.AG, A2          GET UUT AUTOGAIN DAC ADDR
                LEA             UUT.PGA, A3         GET UUT P.G.A. SELECT ADDR
                LEA             UUT.CSR, A4         GET UUT CONTROL STATUS ADDR
                LEA             UUT.ADAT, A5        GET UUT ADC DATA REG ADDR
                MOVE.W          #$800, (A2)         SET UUT GAIN TO MID RANGE
                MOVE.W          #$3, D6             SET LOOP COUNTER TO START

AGAIN           MOVE.W          #$B, D7             SET THE BIT COUNTER START
                MOVE.W          #$0003, (A3)        SELECT P.G.A. GAIN = X500
                CLR.W           D5                  CLEAR ERROR CORRECT REG.

CALZERO         BSET            D7, D5              SET NEXT ERROR CORRECT BIT
                MOVE.W          D5, (A1)            WRITE ERROR CORRECTION REG
                MOVE.W          #$7040, D3          SELECT ZERO TEST REFERENCE
                JSR             AUTORD              DO ADC READING SUBROUTINE
                CMP.W           #$0800, D3          COMPARE TO EXPECTED READING
                BEQ             CALGAIN             IF ZEROED THEN DO CAL GAIN
                BGT             CONT                IF ERROR POSITIVE CONTINUE
                BCLR            D7, D5              IF ERROR NEGATIVE CLR BIT

CONT            SUB.W           #$1, D7             DECREMENT THE BIT COUNTER
                BCC             CALZERO             IF BIT COUNTER < 0 CALGAIN

CALGAIN         CMP.W           #$0, D6             DO CAL ZERO WITHOUT DOING
                BEQ             ENDSEQ              CAL GAIN ON THE LAST PASS
                MOVE.W          #$B, D7             SET THE BIT COUNTER START
                MOVE.W          #$0000, (A3)        SELECT P.G.A. GAIN = X1

CALGAINA        BSET            D7, D5              SET NEXT ERROR CORRECT BIT
                MOVE.W          D5, (A2)            WRITE ERROR CORRECTION REG
                MOVE.W          #$7340, D3          SELECT POSITIVE TEST REF.
                JSR             AUTORD              DO ADC READING SUBROUTINE
                CMP.W           #$0FF6, D3          COMPARE TO EXPECTED READING
                BEQ             ENDSEQ              IF GAIN CALLED THEN DO ENDSEQ
                BGT             CONTA               IF ERROR POSITIVE CONTINUE
                BCLR            D7, D5              IF ERROR NEGATIVE CLR BIT

CONTA           SUB.W           #$1, D7             DECREMENT THE BIT COUNTER
                BCC             CALGAINA            IF BIT COUNTER < 0 ENDSEQ

ENDSEQ          DBF             D6, AGAIN           LOOP TILL LOOP COUNTER < 0
                JMP             MAIN                END OF AUTO CAL SEQUENCE

*****************************************************************************************************************

AUTORD          MOVE.L          #$CFFF, D4          LOAD DELAY FOR DAC SETTLING
DELAYA          SUB.L           #$1, D4             NOW, DO THE DAC DELAY
                BNE             DELAYA              CHECK FOR END OF DELAY
                MOVE.W          D3, (A4)            WRITE CONTROL STATUS REG
AUTORDA         MOVE.W          (A4), D2            READ CONTROL STATUS REG
                BTST            #15, D2             IS NEW DATA READY HI?
                BEQ             AUTORDA             IF NOT READ C.S.R. AGAIN
                MOVE.W          (A5), D3            READ AND STORE A/D DATA
                RTS                                 RETURN FROM SUBROUTINE

*****************************************************************************************************************

AUTOMSG         DC.B CR, LF
                DC.B CR, LF, '*******************************************************
                DC.B CR, LF, 'A/D/C AUTOCALIBRATION ROUTINE             '
                DC.B CR, LF, '*******************************************************
                DC.B CR, LF, 'MOVE JUMPER J5 TO THE 2, 3 POSITION TO'
                DC.B CR, LF, 'SELECT AUTOGAIN CAL AND JUMPER J38    '
                DC.B CR, LF, 'TO THE 2, 3 POSITION TO SELECT AUTO       '
                DC.B CR, LF, 'ZERO CAL.'
                DC.B CR, LF, LF, 'PRESS ANY KEY TO CONTINUE. . . . . . . . . . . ', NUL


*****************************************************************************************************************
*****************************************************************************************************************
```

M3111/F4.8.2-2

Figure 4.8.2-2. Program Example - Converter Autocalibration

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4.8.3 Performing Autocalibration

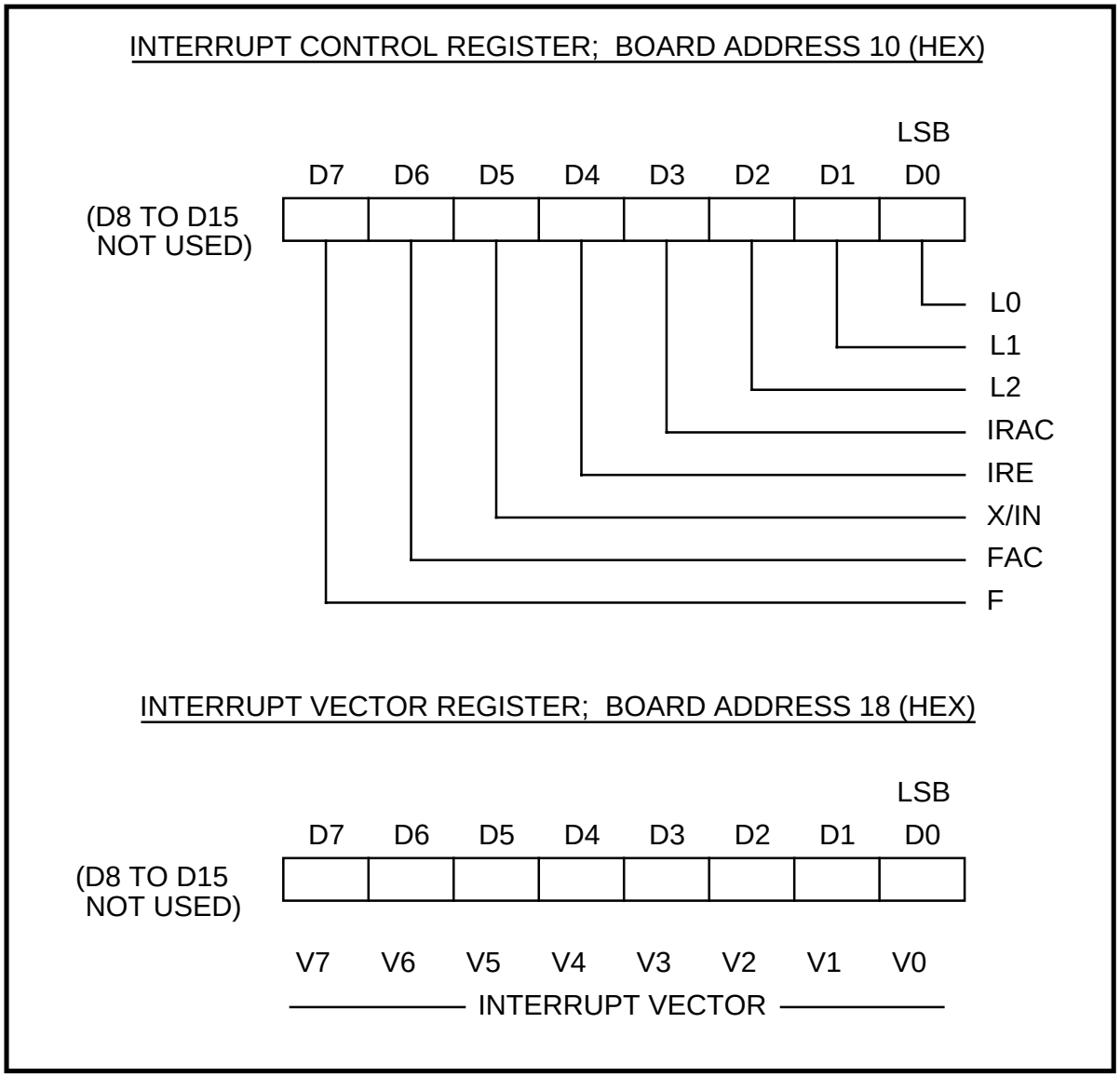
The VMIVME-3111 board implements two latching 12-bit Digital-to-Analog Converters (DACs). One DAC adjusts the channel zero offset, while the other adjusts the channel gain. Both of the DACs accept right-justified 12-bit data and are write-only devices. To do the actual calibration, we suggest the method of successive approximation shown in Figures 4.8.2-1 and 4.8.2-2. This autocalibration routine should always be performed after a power up or a system reset.

4.9 BUS INTERRUPT CONTROL

To eliminate the requirement for polling the VMIVME-3111 board during basic conversion sequencing, the VMIVME-3111 board is equipped to provide an interrupt at the end of each conversion sequence. The interrupt response is established through the INTERRUPT CONTROL and INTERRUPT VECTOR Registers (Table 4.6.2-1) which are described in the following paragraphs. During BOARD RESET or SYSTEM RESET, the Interrupt Control Register is cleared to "00," and the Interrupt Vector Register is preset to "0F" (HEX). Interrupt Register functions are summarized in Table 4.9-1 and Appendix B of this manual contains the data sheet for the Bus Interrupter Module (BIM).

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Table 4.9-1. Interrupt Registers



M3111/T4.9-1

4.9.1 Interrupt Control Register

The Interrupt Control Register (Table 4.9-1) controls the interrupt level as well as the enabling or disabling of the interrupt. The function of each register bit is described in the following definitions.

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INTERRUPT LEVEL (Bits L2, L1, L0):

Determines the level at which an interrupt will occur:

REGISTER BIT			
L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

INTERRUPT ENABLE (IRE, Bit 4):

When this bit is set HIGH, the bus interrupt associated with the Control Register is enabled; the interrupt is disabled if IRE is LOW.

INTERRUPT AUTO-CLEAR (IRAC, Bit 3):

If the IRAC bit is set HIGH, the Interrupt Enable bit (IRE) is cleared during the interrupt acknowledge cycle which responds to the request. The IRE bit must then be set HIGH again to enable the interrupt.

EXTERNAL/INTERNAL (X/IN, Bit 5):

This control bit has no valid function on the VMIVME-3111 board and *MUST* be cleared LOW at all times.

FLAG (F, Bit 7):

This control bit has no affect on the operation of the VMIVME-3111 board and is available for use by the controlling processor as a utility flag.

FLAG AUTO-CLEAR (FAC, Bit 6):

If "FAC" is set HIGH, the flag bit "F" is automatically cleared during an interrupt acknowledge cycle.

4.9.2 Interrupt Vector Register

Contents of the Interrupt Vector Register are supplied as a data byte (D00 through D07) on the data bus during the board's INTERRUPT

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ACKNOWLEDGE CYCLE. The function of the data byte is determined by the system user, and in typical applications, would be interpreted as an identification of the board, or as an address vector.

4.10 BOARD IDENTIFICATION REGISTER

By reading the Board Identification Register located at address 00 (Table 4.6.2-1), an 8-bit, left-justified identification code of "0D" will be obtained from the VMIVME-3111 board.

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
*****************
*     CAUTION   *
*****************
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
*****************
*     CAUTION   *
*****************
```

DO NOT INSTALL OR REMOVE THE BOARDS WHILE THE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

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a. Have the sections pertaining to theory and programming, Sections 3 and 4, been reviewed and applied to system requirements?

b. Review Section 5.4.1 and Table 5.4-1 to verify that all factory-installed jumpers are in place. To change the board address or address modifier response, refer to Section 5.4.2. _____

c. Have the I/O cables, with the proper mating connectors, been connected to the input connectors P2 and P3? Refer to Section 5.6 for connector descriptions. _____

d. Calibration has been performed at the factory. If recalibration is required, refer to Section 5.5. _____

After the above checklist has been completed, the board can be installed in a VMEbus system. This board may be installed in any slot position, except slot one which is usually reserved for the master processing unit.

```
*****************
*     CAUTION     *
*****************
```

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.4 OPERATIONAL CONFIGURATION

Control of the VMIVME-3111 board address and I/O Access Mode are determined by field-replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all VMIVME-3111 jumpers are shown in Figure 5.4-1 and Table 5.4-1.

5.4.1 Factory-Installed Jumpers

Each VMIVME-3111 board is configured at the factory with the specific jumper arrangement shown in Table 5.4-1. The factory configuration establishes the following functional baseline for the VMIVME-3111 board, and ensures that all essential jumpers are installed.

a. Board Address is 0000 HEX
b. I/O Access Mode is short supervisory
c. ±10 V analog inputs and outputs
d. Analog inputs single-ended
e. Analog input and output returns connected to analog ground.

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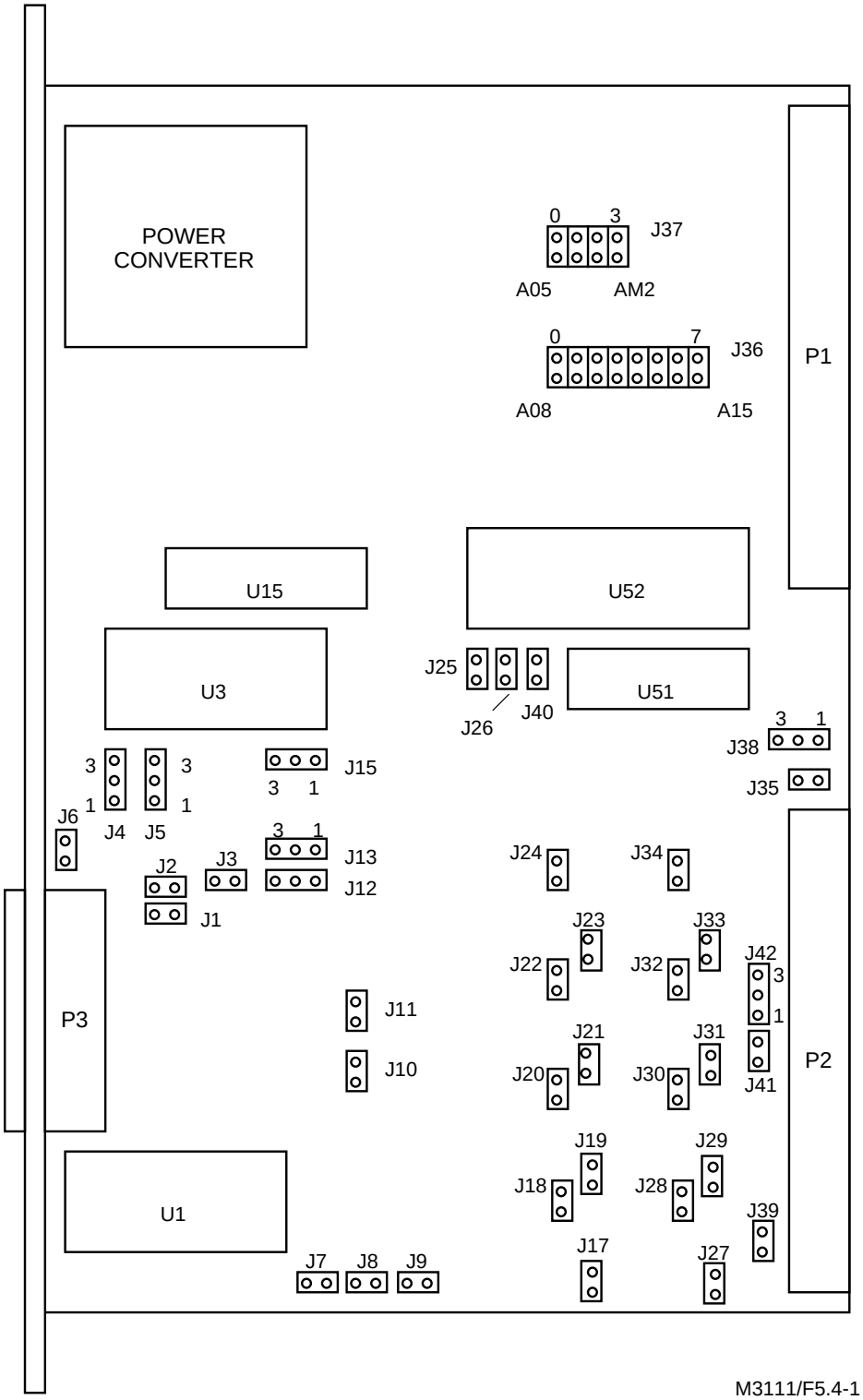


Figure 5.4-1. Jumper Locations

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Table 5.4-1. Programmable Jumper Functions

JUMPER IDENT	FUNCTION (INSTALLED)	FACT CONFIG	FIELD ALTERABLE
J37-0	BOARD ADDRESS BIT A05 = 0	INSTALLED	YES
J37-1	BOARD ADDRESS BIT A06 = 0	INSTALLED	YES
J37-2	BOARD ADDRESS BIT A07 = 0	INSTALLED	YES
J36-0	BOARD ADDRESS BIT A08 = 0	INSTALLED	YES
J36-1	BOARD ADDRESS BIT A09 = 0	INSTALLED	YES
J36-2	BOARD ADDRESS BIT A10 = 0	INSTALLED	YES
J36-3	BOARD ADDRESS BIT A11 = 0	INSTALLED	YES
J36-4	BOARD ADDRESS BIT A12 = 0	INSTALLED	YES
J36-5	BOARD ADDRESS BIT A13 = 0	INSTALLED	YES
J36-6	BOARD ADDRESS BIT A14 = 0	INSTALLED	YES
J36-7	BOARD ADDRESS BIT A15 = 0	INSTALLED	YES
J37-3	SHORT NONPRIVILEGED ACCESS	OMITTED	YES
J24	P2 CHAN 00, 16 SINGLE-ENDED	INSTALLED	YES
J23	P2 CHAN 01, 17 SINGLE-ENDED	INSTALLED	YES
J34	P2 CHAN 02, 18 SINGLE-ENDED	INSTALLED	YES
J33	P2 CHAN 03, 19 SINGLE-ENDED	INSTALLED	YES
J22	P2 CHAN 04, 20 SINGLE-ENDED	INSTALLED	YES
J21	P2 CHAN 05, 21 SINGLE-ENDED	INSTALLED	YES
J31	P2 CHAN 06, 22 SINGLE-ENDED	INSTALLED	YES
J32	P2 CHAN 07, 23 SINGLE-ENDED	INSTALLED	YES
J20	P2 CHAN 08, 24 SINGLE-ENDED	INSTALLED	YES
J19	P2 CHAN 09, 25 SINGLE-ENDED	INSTALLED	YES
J30	P2 CHAN 10, 26 SINGLE-ENDED	INSTALLED	YES
J29	P2 CHAN 11, 27 SINGLE-ENDED	INSTALLED	YES
J18	P2 CHAN 12, 28 SINGLE-ENDED	INSTALLED	YES
J17	P2 CHAN 13, 29 SINGLE-ENDED	INSTALLED	YES
J27	P2 CHAN 14, 30 SINGLE-ENDED	INSTALLED	YES
J28	P2 CHAN 15, 31 SINGLE-ENDED	INSTALLED	YES

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Table 5.4-1. Programmable Jumper Functions (Concluded)

JUMPER IDENT	FUNCTION (INSTALLED)	FACT CONFIG	FIELD ALTERABLE
J1	GROUND P3 RETURN	INSTALLED	YES
J2	GROUND P3 SENSE	INSTALLED	YES
J35	GROUND P2 SENSE	INSTALLED	YES
J7, 8	OMIT ANALOG OUTPUTS	(OPTION)	NO
J9, 10, 11	OMIT P3 INPUTS	(OPTION)	NO
J26	10 VDC REFERENCE	INSTALLED	YES
J40	5 VDC REFERENCE	OMITTED	YES
J25	2.5 VDC REFERENCE	OMITTED	YES
J3	5 V FULL-SCALE RANGE (FSR) INPUTS	OMITTED	YES
J15-2, 3	10 V, 5 V FSR INPUTS	OMITTED	YES
J15-1, 2	20 V FSR INPUTS	INSTALLED	YES
J4-2, 3	UNIPOLAR ADC	OMITTED	YES
J4-1, 2	BIPOLAR ADC	INSTALLED	YES
J6	UNIPOLAR ADC	OMITTED	YES
J38-2, 3	AUTO INPUT ZERO ADJUST	INSTALLED*	YES
J38-1, 2	MANUAL INPUT ZERO ADJUST	OMITTED*	YES
J5-1, 2	MANUAL INPUT GAIN ADJUST	OMITTED*	YES
J5-2, 3	AUTO INPUT GAIN ADJUST	INSTALLED*	YES
J12-2, 3	UNIPOLAR ANALOG OUTPUTS	OMITTED	YES
J12-1, 2	BIPOLAR ANALOG OUTPUTS	INSTALLED	YES
J13-2, 3	10 V FSR ANALOG OUTPUTS	OMITTED	YES
J13-1, 2	5 V FSR ANALOG OUTPUTS	OMITTED	YES
J39	GROUND ANALOG OUTPUTS RETURN	INSTALLED	YES
J41	CONNECTS EXT TRIG TO P2 GND SENSE	OMITTED	YES
J42-2, 3	CONNECTS TRIG RTN TO P2 GND SENSE	OMITTED	YES
J42-1, 2	CONNECTS TRIG RTN TO GROUND	INSTALLED	YES

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*For no autocal, no auto zero option:

J38-2, 3	Omitted
J38-1, 2	Installed
J5-1, 2	Installed
J5-2, 3	Omitted

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5.4.2 Board Address and Address Modifier Selection

Jumper blocks J36 and J37 permit the VMIVME-3111 board to be located on any 32-byte boundary within the short I/O address space available from the VMEbus (see Sections 3 and 4). Operation in the short I/O address space requires that 15 address lines be decoded to access all locations. Since four lines are used for decoding on-board functions (Section 4), the VMIVME-3111 board's address is defined by 11 lines; address bits A05 through A15.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in the jumper blocks J36 and J37, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A05 has a weight of 32-byte locations. As an example, the jumper arrangement shown in Table 5.4.2-1 would produce a board address of XXXX8F00 HEX. Address bits XXXX are CPU dependent.

I/O ACCESS MODE is programmed by selecting the value of the address modifier bit AM2 with jumper J37-3. Short nonprivileged access is selected by installing the jumper. Short supervisory access is selected by omitting the jumper.

Table 5.4.2-1. Typical Board Address (FF8F00 HEX) Selection

JUMPER	ADR BIT	STATE*
J37-0	A05	SHORTED
J37-1	A06	SHORTED
J37-2	A07	SHORTED
J36-0	A08	OPEN
J36-1	A09	OPEN
J36-2	A10	OPEN
J36-3	A11	OPEN
J36-4	A12	SHORTED
J36-5	A13	SHORTED
J36-6	A14	SHORTED
J36-7	A15	OPEN

*SHORTED = "ZERO."
OPEN = "ONE."

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5.4.3 Analog Input Voltage Range Selection

As indicated in the Electrical Specifications (see Document Number 800-003111-000), five voltage ranges are available for the VMIVME-3111 Board. Jumpers J3, J4, J6, and J15 control the ranges and are identified in Table 5.4.3-1. The board is factory configured for ±10 V range.

Table 5.4.3-1. Voltage Range Configuration

	J3	J4	J6	J15
±10 V	OFF	1,2	OFF	1,2
±5 V*	OFF	1,2	OFF	2,3
±2.5 V	ON	1,2	OFF	2,3
0 TO +5 V	ON	2,3	ON	2,3
0 TO +10 V**	OFF	2,3	ON	2,3

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*±5 V will also work with J3 ON, J4-1, 2, J6 OFF and J15-1, 2.
**0 to +10 V will also work with J3 ON, J4-2, 3, J6 ON and J15-1, 2.

Jumper J1 connects the P3 analog input return line to analog ground on the VMIVME-3111 board. P3 input remote ground sensing is disabled if jumper J2 is installed, and enabled if J2 is removed.

5.4.4 Current Loop Termination Resistors

The low pass input filter capacitors are replaced with 250 Ω, 0.02 percent precision resistors when the board is equipped with the current loop termination option.

5.4.5 Differential/Single-Ended Input Mode Selection

All P3 analog inputs are single-ended channels. The P2 analog inputs, however, can be jumper-programmed as either single-ended channels or as differential channel pairs. A channel pair is differential if the associated jumper (listed in Table 5.4-1) is removed. The pair becomes two independent single-ended inputs if the jumper is installed.

5.4.6 Analog Output Voltage Range Selection

The analog output voltage range is selected by jumpers J12 and J13, as indicated in Table 5.4-1. Jumper J39 connects the analog output return line to analog ground on the VMIVME-3111 board.

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5.5 CALIBRATION

Before delivery from the factory, the VMIVME-3111 board is fully calibrated to ±10 V operation and conforms to all applicable specifications as listed in Section 2. However, should recalibration be required, refer to Sections 5.5.1 through 5.5.3, and perform all of the calibration operations in the sequence shown. The locations of all adjustments and test points are shown in Figure 5.5-1.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. However, the seals are easily broken for recalibration. All adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

5.5.1 Equipment Required

a. Digital Voltmeter (DVM)	±1.000 VDC and ±10.000 VDC ranges; five or more digits; ±0.005 percent of voltage range measurement accuracy; 10 MΩ minimum input impedance.
b. Digital Voltage Source (Voltage Input Option Only)	±1.000 VDC and ±10.000 VDC output voltage ranges; ±0.005 percent of range accuracy. Maximum output impedance 10 Ω.
c. Digital Current Source (Current Input Option Only)	±0.040 A output current range; ±0.005 percent of range accuracy.
d. Chassis	VMEbus backplane or equivalent, J1 and J2 connectors, 68000 series master controller, +5 ±0.1 VDC, 3 A power supply.
e. Extender Board	VMEbus extender board.

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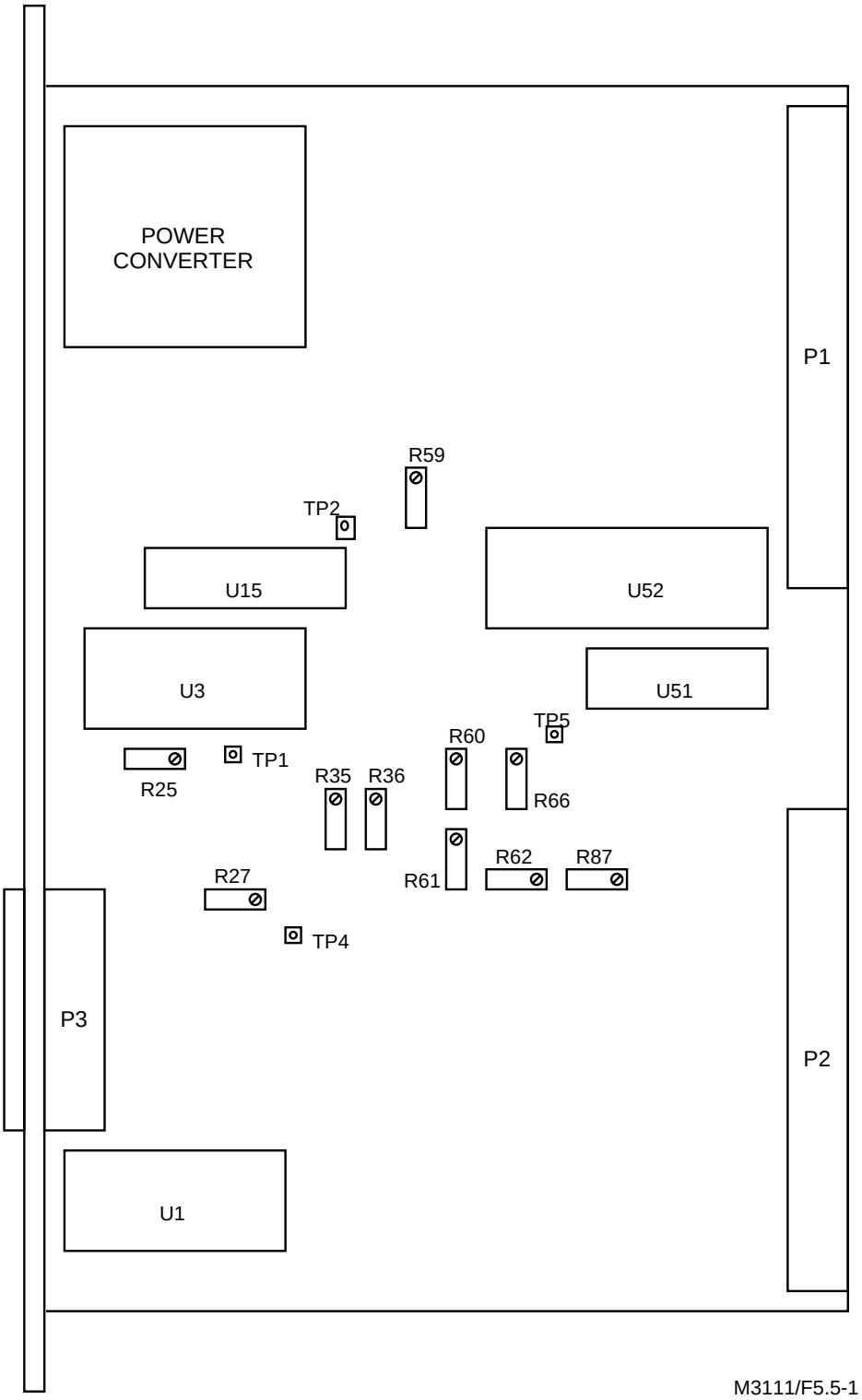


Figure 5.5-1. Test Point and Adjustment Locations

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5.5.2 Internal Reference Voltage Calibration

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*****************
*     CAUTION     *
*****************
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DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

a. Install the VMIVME-3111 board on an extender board in a slot of the VMEbus backplane.

b. Ensure that the J25 and J40 jumpers have been removed, and install jumper J26.

c. Apply power to the backplane. Allow a minimum warm-up interval of ten minutes after power has been applied before proceeding.

d. Connect the positive lead of the DVM to test point TP5 (CAL REF) and the negative lead to test point TP1 (REF RTN). Adjust R62 (REF ADJ) for a DVM indication of +9.9512 ±0.0020 VDC.

5.5.3 Programmable Gain Amplifier (PGA) Calibration

5.5.3.1 Voltage Input Option Calibration

a. Connect the positive lead of the digital voltage source to Pin A1 of P2. Jumper Pins A1 and C1 of P2 together. Connect the negative lead of the voltage source to Pin A2 of P2. Place the J38 jumper in the J38-1,2 (MAN ZERO) position.

b. Connect the positive lead of the DVM to test point TP4 (T/H INPUT) and the negative lead to the test point TP1 (SIG RTN).

c. Select the Self-Test Zero input by writing 0000 to the Control and Status Register (CSR) at board address 02. Select maximum gain (x500) by writing 0003 to the PGA Gain Selection Register at board address 0E.

d. Adjust R87 (MANUAL ADC ZERO ADJ) for a DVM indication of 0.00 ±0.025 VDC.

e. Select the P2 differential channel 00 by writing 0100 (HEX) to the CSR.

f. Adjust the voltage source output to +10.000 VDC.

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g. Adjust R66 (CMRR ADJ) for a DVM indication of lowest positive reading.

h. Adjust the voltage source output to +0.0200 VDC.

i. Remove the jumper between Pins A1 and C1 of P2. Connect the negative lead of the voltage source to Pin C1 of P2. Jumper pins C1 and C2 of P2 together.

j. Verify a DVM indication of +10.000 ±0.100 VDC.

k. Select a PGA gain of x100 by writing 0002 to the PGA Gain Selection Register.

l. Adjust the voltage source output to +0.1000 VDC. Adjust R59 (x100 ADJ) for a DVM indication of +10.000 ±0.002 VDC.

m. Select a PGA gain of x1 by writing 0000 to the PGA Gain Selection Register.

n. Adjust the voltage source output to +10.000 VDC. Verify that the DVM indicates +10.000 ±0.002 VDC.

5.5.3.2 Current Input Option Calibration

a. Adjust the current source output to 0.0 mA. Connect the positive lead of the current source to Pin A1 of P2. Connect the negative lead of the current source to Pin C2 of P2. Place the J38 jumper in the J38-1, 2 (MAN ZERO) position. Install jumper J24.

b. Connect the positive lead of the DVM to test point TP4 (T/H INPUT) and the negative lead to the testpoint TP1 (SIG RTN).

c. Select the Self-Test Zero input by writing 0000 to the Control and Status Register (CSR) at board address 02.

d. Select maximum gain (x500) by writing 0003 to the PGA Gain Selection Register at board address 0E.

e. Adjust R87 (Manual ADC Zero Adj) for a DVM indication of 0.00 ±0.025 VDC.

f. Select the P2 single-ended channel 00 by writing 0200 (Hex) to the CSR.

g. Adjust the current source output to +0.080 mA.

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h. Verify a DVM indication of +10.000 ±0.100 VDC.

i. Select a PGA gain of x100 by writing 0002 to the PGA Gain Selection Register.

j. Adjust the current source output to +0.400 mA. Adjust R59 (x100 Adj) for a DVM indication of +10.000 ±0.004 VDC.

k. Select a PGA gain of x1 by writing 0000 to the PGA Gain Select Register.

l. Adjust the current source output to +40.00 mA. Adjust R59 for a DVM indication of +10.000 ±0.006 VDC.

5.5.4 Manual ADC Calibration

a. Establish manual ADC calibration and the ±10 V range as follows:

JUMPER	FUNCTION	STATE
J3	5 V	REMOVED
J4-1, 2	BIPOLAR	INSTALLED
J5-1, 2	MANUAL GAIN	INSTALLED
J15-1, 2	20 V FSR	INSTALLED
J25	2.5 V REF	REMOVED
J26	10 V REF	INSTALLED
J40	5 V REF	REMOVED
J38-1, 2	MANUAL ZERO	INSTALLED
J6	UNIPOLAR	REMOVED

b. Select a PGA gain of x1 by writing 0000 to the PGA gain selection register. Select the SELF-TEST ZERO input and initiate A/D conversions by writing 6040 HEX to the CSR at intervals of 0.1-1.0 second. Display the ADC register after each conversion.

c. Adjust R25 (BIPOLAR ADC ZERO ADJ) for an ADC indication which varies between FFFF and 0000 HEX.

d. Select the Self-Test Reference Voltage input and initiate A/D conversions by writing 6340 HEX to the CSR at intervals of 0.1-1.0 second. Display the ADC Register after each conversion.

e. Adjust R27 (T/H GAIN ADJ) for an ADC indication which varies between 07F5 and 07F6 HEX.

5.5.5 Analog Outputs Calibration

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a. Establish bipolar, -10 to +10 V analog outputs as follows:

JUMPER	FUNCTION	STATE
J12-1, 2	BIPOLAR OUT	INSTALLED
J13	20 V OUTPUTS	REMOVED
J39	OUT RTN GND	INSTALLED

b. Connect the positive lead of the DVM to Pin A31 of P2, and the negative lead to Pin C31 of P2.

c. Establish zero output levels by writing 0800 to the output Digital-to-Analog Converter (DAC) Registers at board addresses 04 and 06. Place the outputs On-Line by writing 0800 to the CSR.

d. Adjust R36 (ANA CH-0 ZERO ADJ) for a DVM indication of 0.000 ±0.002 VDC.

e. Move the positive lead of the DVM to Pin A32 of P2. Adjust R61 (ANA CH-1 ZERO ADJ) for a DVM indication of 0.000 ±0.002 VDC.

f. Establish negative full-scale output levels by writing 0000 to the output DAC Registers.

g. Adjust R60 (ANA CH-1 GAIN ADJ) for a DVM indication of -10.000 ±0.002 VDC.

h. Move the positive lead of the DVM to Pin A31 of P2. Adjust R35 (ANA CH-0 GAIN ADJ) for a DVM indication of -10.000 ±0.002 VDC.

i. Establish positive full-scale outputs by writing 0FFF HEX to the output DAC Registers. Verify that the output levels on pins A31 and A32 of P2 are +9.995 ±0.004 VDC.

j. Calibration is completed. Remove all test connections. Remove power. Restore all board jumpers to their original locations.

5.6 CONNECTOR DESCRIPTIONS

Two 96-pin DIN connectors, P1 and P2 (Figure 2.1-1), connect the VMIVME-3111 board to the VMEbus backplane. P1 contains the address, data and control lines, and all additional signals necessary to control VMEbus functions related to the board.

Rear panel connector P2 accepts 32 single-ended analog inputs or 16 differential inputs, and mates with a 64-pin DIN cable connector. Pin configuration and signal assignments for P2 are shown in Figure 5.6-1 and Table 5.6-1. Sensing of remote signal returns through P2 is established by removing the J35 jumper. The

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P2 signal assignments produce a signal-signal-gnd-gnd signal sequence in a standard ribbon-cable.

Front panel connector P3 accepts 16 single-ended analog inputs, and is a 26-pin, Scotchflex Model 3429-5002 or equivalent connector header. Pin configuration and signal assignments for P3 are shown in Figure 5.6-2 and Table 5.6-2. P3 is configured to permit direct 26-wire ribbon-cable connection to the 3V/5V series of nonmultiplexed, voltage-output signal conditioner assemblies. Remote sensing of the 3V/5V assembly signal return is established on the VMIVME-3111 board by removing the J39 jumper.

NOTE:

IF P2 OR P3 IS CONFIGURED FOR CURRENT LOOP TERMINATION, THE INPUT RESISTANCE OF EACH CHANNEL WILL BE VERY LOW AND WILL PRODUCE SIGNIFICANT LOADING OF VOLTAGE INPUTS. EXCESSIVE HEATING AND DAMAGE OF VMIVME-3111 COMPONENTS MAY OCCUR IF CURRENT LOOP INPUTS ARE DRIVEN BEYOND ±10 V FOR EXTENDED INTERVALS.

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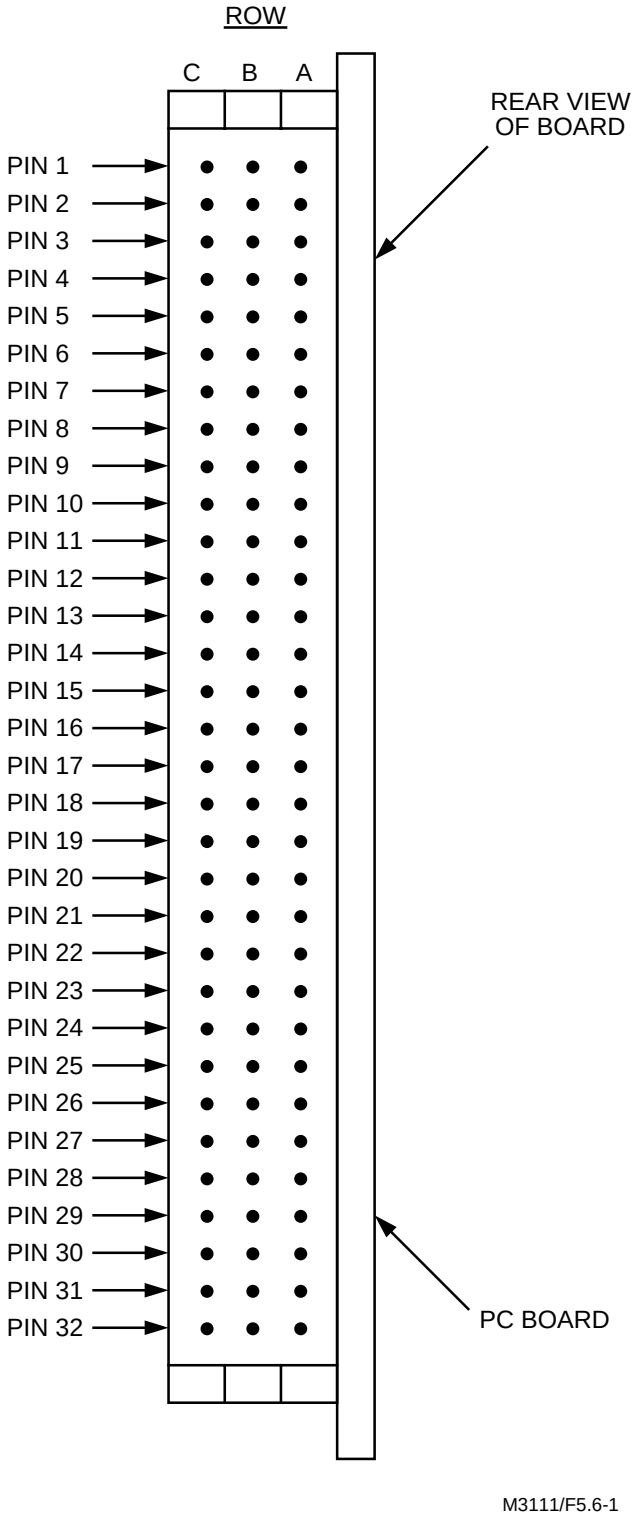


Figure 5.6-1. P2 Connector - Pin Configuration

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Table 5.6-1. P2 Connector (Rear Panel Inputs) Signal Assignments

PIN NO.	SINGLE-ENDED INPUTS		DIFFERENTIAL INPUTS	
	ROW-A SIGNAL	ROW-C SIGNAL	ROW-A SIGNAL	ROW-C SIGNAL
1	CH 00	CH 16	CH 00 HI	CH 00 LO
2	GND SEN	GND SEN	GND SEN	GND SEN
3	CH 01	CH 17	CH 01 HI	CH 01 LO
4	GND SEN	GND SEN	GND SEN	GND SEN
5	CH 02	CH 18	CH 02 HI	CH 02 LO
6	GND SEN	GND SEN	GND SEN	GND SEN
7	CH 03	CH 19	CH 03 HI	CH 03 LO
8	GND SEN	GND SEN	GND SEN	GND SEN
9	CH 04	CH 20	CH 04 HI	CH 04 LO
10	GND SEN	GND SEN	GND SEN	GND SEN
11	CH 05	CH 21	CH 05 HI	CH 05 LO
12	GND SEN	GND SEN	GND SEN	GND SEN
13	CH 06	CH 22	CH 06 HI	CH 06 LO
14	GND SEN	GND SEN	GND SEN	GND SEN
15	CH 07	CH 23	CH 07 HI	CH 07 LO
16	GND SEN	GND SEN	GND SEN	GND SEN
17	CH 08	CH 24	CH 08 HI	CH 08 LO
18	GND SEN	GND SEN	GND SEN	GND SEN
19	CH 09	CH 25	CH 09 HI	CH 09 LO
20	GND SEN	GND SEN	GND SEN	GND SEN
21	CH 10	CH 26	CH 10 HI	CH 10 LO
22	GND SEN	GND SEN	GND SEN	GND SEN
23	CH 11	CH 27	CH 11 HI	CH 11 LO
24	GND SEN	GND SEN	GND SEN	GND SEN
25	CH 12	CH 28	CH 12 HI	CH 12 LO
26	GND SEN	GND SEN	GND SEN	GND SEN
27	CH 13	CH 29	CH 13 HI	CH 13 LO
28	EXT TRIG	TRIG RTN	EXT TRIG	TRIG RTN
29	CH 14	CH 30	CH 14 HI	CH 14 LO
30	CH 15	CH 31	CH 15 HI	CH 15 LO

ANALOG OUTPUTS		
	ROW-A SIGNAL	ROW-C SIGNAL
31	OUTPUT CHAN-0	OUTPUT RETURN
32	OUTPUT CHAN-1	OUTPUT RETURN

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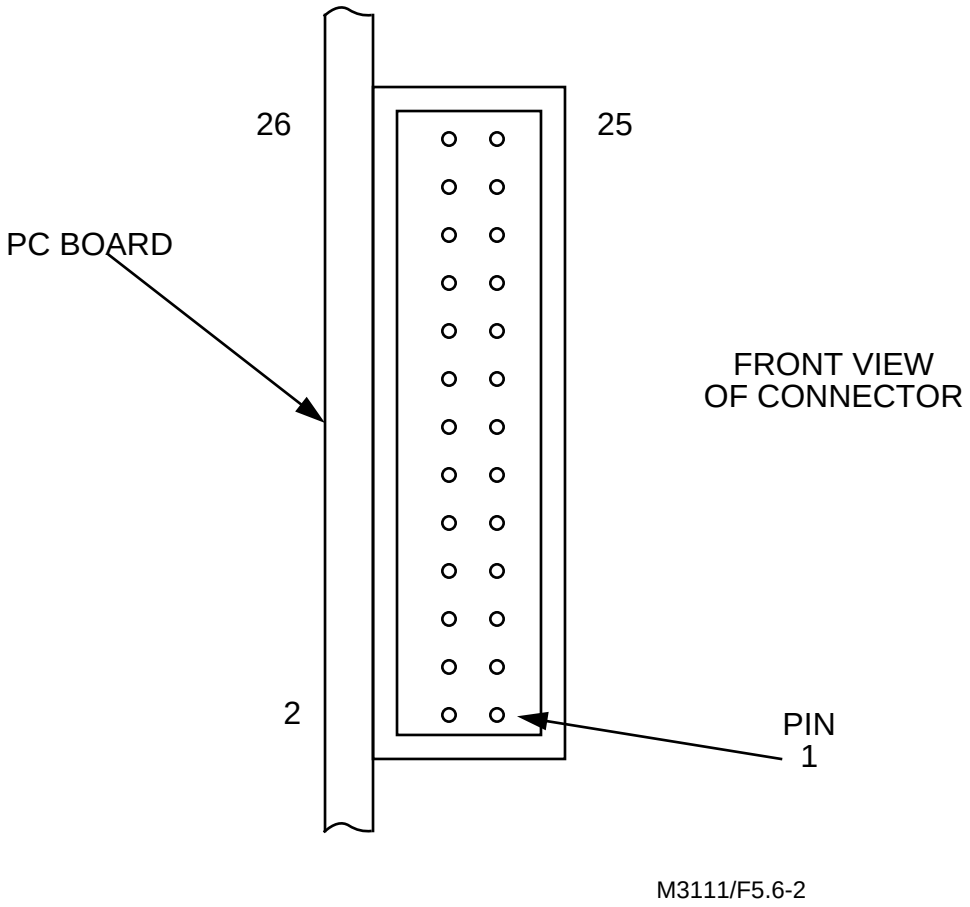


Figure 5.6-2. P3 Connector - Pin Configuration

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Table 5.6-2. P3 Connector Signal Assignments

PIN NUMBER	INPUT SIGNAL
1	CHAN 00
2	CHAN 08
3	RETURN
4	CHAN 09
5	CHAN 01
6	RETURN
7	CHAN 02
8	CHAN 10
9	RETURN
10	CHAN 11
11	CHAN 03
12	RETURN
13	CHAN 04
14	CHAN 12
15	RETURN
16	CHAN 13
17	CHAN 05
18	RETURN
19	CHAN 06
20	CHAN 14
21	RETURN
22	CHAN 15
23	CHAN 07
24	RETURN
25	GND SENSE
26	NO CONN

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

SCHEMATIC AND ASSEMBLY DRAWING

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