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VMIVME-3112

SCANNING 12-bit ANALOG-TO-DIGITAL CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-003112-000

Revised July 2, 1992

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	11/8/90	Release all	90-0099
B	11/8/90	Appendix A	90-0100
C	11/8/90	Appendix A	90-0158
D	03/25/91	Appendix A	91-0004
E	03/25/91	Convert ZZZ back to 500	91-0081
F	05/17/91	Cover, Page ii, Parts List, and Schematics	91-0132
G	06/05/91	Appendix A	91-0145
H	08/12/91	Appendix A	91-0209
J	12/16/91	Cover, Pages ii, 2-4, 2-5, 2-7, 3-9, 5-7, and Parts List	91-0317
K	02/29/92	Cover, Pages ii, 1-1, 1-2, and 2-5	92-0046
L	07/02/92	Cover, pages 5-3, 5-13, and Reformat Sections 2 and 6	92-0183

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VMIVME-3112
SCANNING 12-bit ANALOG-TO-DIGITAL CONVERTER BOARD

TABLE OF CONTENTS

Page

SECTION 1. GENERAL DESCRIPTION

1.1 INTRODUCTION..... 1-1
1.2 FUNCTIONAL BLOCK DIAGRAM 1-2
1.3 REFERENCE MATERIAL LIST..... 1-2

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. THEORY OF OPERATION

3.1 INTRODUCTION..... 3-1
3.2 INTERNAL FUNCTIONAL ORGANIZATION..... 3-1
3.3 VMEbus CONTROL INTERFACE..... 3-1
3.4 ANALOG-TO-DIGITAL (ADC) CONTROL AND TIMING..... 3-4
3.4.1 RANDOM POLLING and RANDOM INTERRUPT MODES..... 3-5
3.4.2 AUTO SCANNING MODE..... 3-5
3.4.3 SCANNING POLL and SCANNING INTERRUPT MODES 3-6
3.5 ADC CONVERSION AND TIMING..... 3-6
3.6 ANALOG INPUTS 3-7
3.6.1 Low Pass Filters and Input Multiplexers 3-7
3.6.2 Single-Ended Versus Differential Operation 3-7
3.7 JUMPER-PROGRAMMABLE GAIN AMPLIFIER 3-9
3.8 CHANNEL SEQUENCER AND DUAL PORT REGISTER CONTROL 3-9
3.9 PROGRAMMABLE INTERVAL TIMER 3-11
3.10 BUS INTERRUPTER MODULE (BIM) 3-11
3.11 BOARD ID REGISTER 3-11
3.12 BUILT-IN POWER CONVERTER 3-11

SECTION 4. PROGRAMMING

4.1 INTRODUCTION..... 4-1
4.2 CONTROL AND STATUS REGISTER DESCRIPTIONS 4-1
4.3 INITIALIZATION..... 4-6

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TABLE OF CONTENTS (Continued)

Page

SECTION 4. PROGRAMMING (Concluded)

4.4 CONTROLLING AND READING THE ANALOG-TO-DIGITAL CONVERTER DATA 4-6
4.4.1 AUTO SCANNING MODE 4-6
4.4.2 SCANNING POLL MODE 4-6
4.4.3 SCANNING INTERRUPT MODE 4-7
4.4.4 RANDOM POLLING MODE 4-8
4.4.5 RANDOM INTERRUPT MODE 4-8
4.4.6 Programmable Interval Timer (8254) 4-8
4.4.7 Programmable Interval Timer Programming Sequence 4-10
4.4.8 Programming the Bus Interrupter Module (BIM) 4-11
4.4.9 Bus Interrupter Module (BIM) Programming Sequence 4-11
4.4.10 External Trigger Operation 4-13
4.5 CHANGING A/D OPERATING MODES 4-13
4.6 PROGRAM EXAMPLE 4-15

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 BEFORE APPLYING POWER: CHECKLIST 5-1
5.4 OPERATIONAL CONFIGURATION 5-2
5.4.1 Factory Installed Jumpers 5-2
5.4.2 Board Address and Address Modifier Selection 5-2
5.4.3 Analog Input Modes 5-5
5.4.3.1 Differential or Single-Ended Operation 5-5
5.4.3.2 Input Voltage Range 5-7
5.4.3.3 Bipolar or Unipolar Operation 5-7
5.4.4 External Trigger Jumper Description 5-7
5.4.5 Internal Timer - 16-, 32-, or 48-Bit Timer Selection 5-9
5.4.6 A/D Scan Sequence Length Jumper Configuration 5-9
5.4.7 Programmable Gain Jumper Configuration 5-9
5.5 CALIBRATION 5-9
5.5.1 Equipment Required 5-11
5.5.2 Analog Inputs Calibration Procedure 5-11
5.6 CONNECTOR DESCRIPTIONS 5-13

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TABLE OF CONTENTS (Continued)

Page

SECTION 6. MAINTENANCE AND WARRANTY

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1
6.3 WARRANTY 6-1
6.4 OUT-OF-WARRANTY REPAIR POLICY 6-2
6.4.1 Repair Category 6-3
6.4.2 Repair Pricing 6-3
6.4.3 Payment 6-3
6.4.4 Shipping Charges 6-4
6.4.5 Shipping Instructions 6-4
6.4.6 Warranty on Repairs 6-4
6.4.7 Exclusions 6-4

LIST OF FIGURES

Figure Page

1.2-1 VMIVME-3112 Functional Block Diagram 1-3
3.2-1 VMIVME-3112 Functional Block Diagram 3-2
3.3-1 VMEbus Control Signals and Interface Logic 3-3
3.6.1-1 Single-Ended and Differential Input Configurations 3-8
3.7-1 Programmable Gain Amplifier 3-10
3.12-1 Power Converter 3-12
5.4-1 Programmable Jumper Test Points and Resistor Network Locations 5-4
5.6-1 P2 Connector Pin Configuration 5-14
5.6-2 P3 and P4 Connector Pin Configuration 5-16

LIST OF TABLES

Table Page

4.1-1 Communications Register Map 4-2
4.2-1 Control Register Functions 4-4
4.2-2 Status Register Flags 4-5
4.4.6-1 Programmable Timer (8254) Register Map 4-10
4.4.7-1 Timer Programming Sequence 4-11
4.4.9-1 Interrupt Control and Vector Registers (Bit Assignments) 4-12
4.4.9-2 Interrupt Control and Vector Registers (Bit Definitions) 4-12

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TABLE OF CONTENTS (Concluded)

LIST OF TABLES

Table		Page
4.5-1	Control Word Sequence for Switching from AUTO SCANNING MODE	4-14
5.3-1	Programmable Jumper Functions	5-3
5.4.2-1	Board Address Selection Example (NNNN85XX)	5-6
5.4.4-1	External Trigger Connections	5-8
5.4.5-1	Internal Timer Jumper Configurations	5-8
5.4.6-1	A/D Scan Length (Jumper) Example	5-10
5.4.7-1	Programmable Gain Jumper Configurations	5-10
5.5.2-1	Calibration Data Table	5-12
5.6-1	P2 Connector Signal Assignments	5-15
5.6-2	P3 Connector (Front Panel Inputs) Signal Assignments	5-17
5.6-3	P4 Connector (Front Panel Inputs) Signal Assignments	5-18

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-3112 64-Channel Scanning, 12-Bit Analog-to-Digital Converter (ADC) is one of the highest density/lowest cost per channel boards in the industry. In addition, it contains many features found only on more expensive products. The AUTO SCANNING MODE, which is automatically entered on power-up, performs Analog-to-Digital (A/D) conversions on all inputs and stores them in a dedicated channel dual port register. This allows the user to operate the board without any programming. The user simply reads the data from the dual port registers, which always contain the latest converted data for that particular channel. There are four other ADC operating modes which allow greater flexibility in controlling the ADC operation.

The VMIVME-3112 Board is useful for many applications which require a large number of differential inputs to be converted to digital form. Overvoltage protected inputs, input filters, programmable timers, and jumper-programmable gain features lend the board to such applications as factory automation and instrumentation, process control, laboratory instrumentation, and general data acquisition systems.

The following brief overview of principal features illustrates the flexibility and performance that is available with the VMIVME-3112 Board:

a. 64 differential or single-ended inputs
b. Powers-up in AUTO SCANNING MODE - no software initialization required
c. Continually digitizes input channels and stores the results in a dedicated channel dual port register (AUTO SCANNING MODE)
d. Five operating modes

    1. AUTO SCANNING MODE *
    2. RANDOM POLL MODE
    3. RANDOM INTERRUPT MODE
    4. SCANNING POLL MODE
    5. SCANNING INTERRUPT MODE

e. Jumper-selectable scanning of 2 to 64 channels
f. VMEbus interrupts may be programmed to interrupt upon completion of a single A/D conversion, or upon completion of a 16- through 64-channel scan

*only for gain = 1 and a minimum of 16 channels.

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g. User-programmable interval timer supports scanning of all channels at periodic intervals
h. Jumper-programmable gains of 1, 10, 100, 200, and 500
i. Selectable A/D ranges of 0 to +10 V, ±5 V, ±10 V
j. Low-level and high-level inputs: ±10 mV to ±10 V
k. Optional low pass filter
l. Overvoltage protected inputs
m. 5 x 10^6 Ω input impedance
n. 33 kHz conversion rate
o. Selectable output code: binary, offset binary, two's complement with sign extension
p. Front panel Fail LED is under program control and may be used for any purpose
q. Board ID register

1.2 FUNCTIONAL BLOCK DIAGRAM

A block diagram of the VMIVME-3112 Board is shown in Figure 1.2-1 which illustrates the board's components and their functions. Not shown on the block diagram is a DC-to-DC converter which provides the analog power supplies (±15 V). The user has only to supply +5 V to the board.

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Product (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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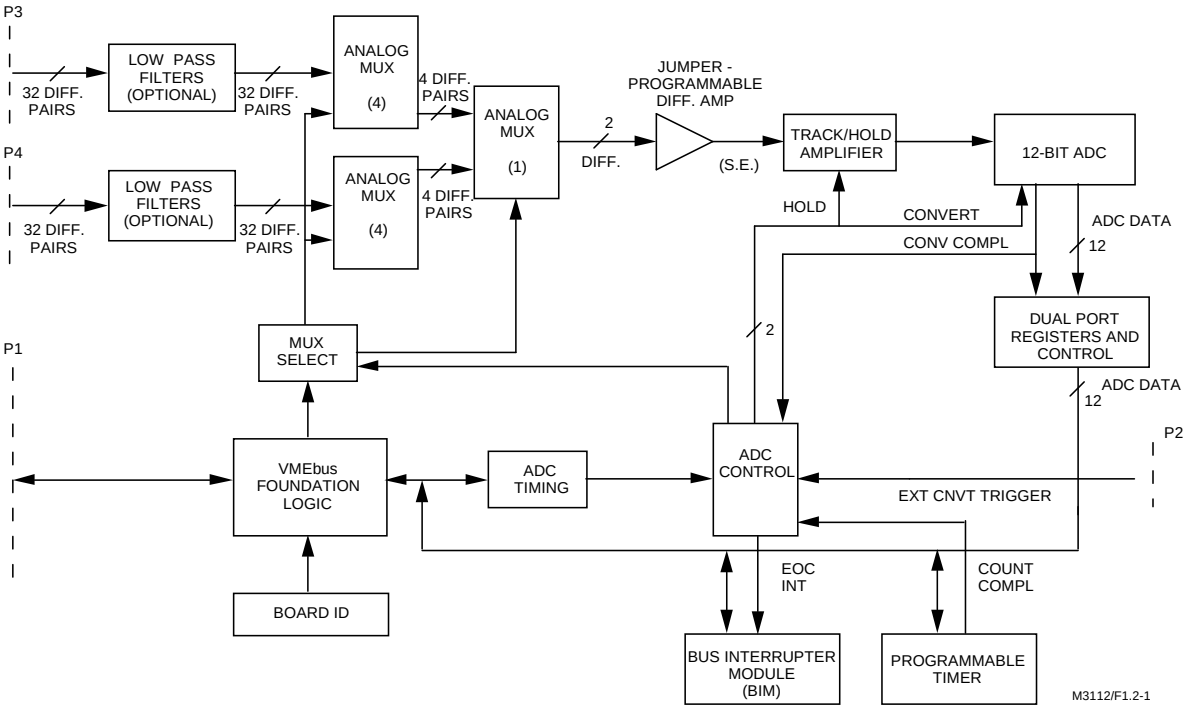


Figure 1.2-1. VMIVME-3112 Functional Block Diagram

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003112-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3112 is a 64-Channel, 12-Bit Analog Input Board. The board has many built-in features, resulting in a board that is capable of handling many data acquisition problems. For example, the AUTO SCANNING MODE on power-up allows for ease of programming. In AUTO SCANNING MODE each channel is continually digitized and stored in a dual port register. Any channel may be read at any time to get the latest data. The VMIVME-3112 is a flexible, low-cost analog input board with features not found in many competing products. These features are discussed in this section.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-3112 is divided into the following functional categories, as illustrated in Figure 3.2-1. All VMIVME-3112 functions are discussed in detail in this section.

a. VMEbus Interface
b. Analog-to-Digital Converter (ADC) and Control Logic
c. Analog Input Filters and Multiplexer
d. Programmable Timer
e. Bus Interrupter
f. Board ID Register

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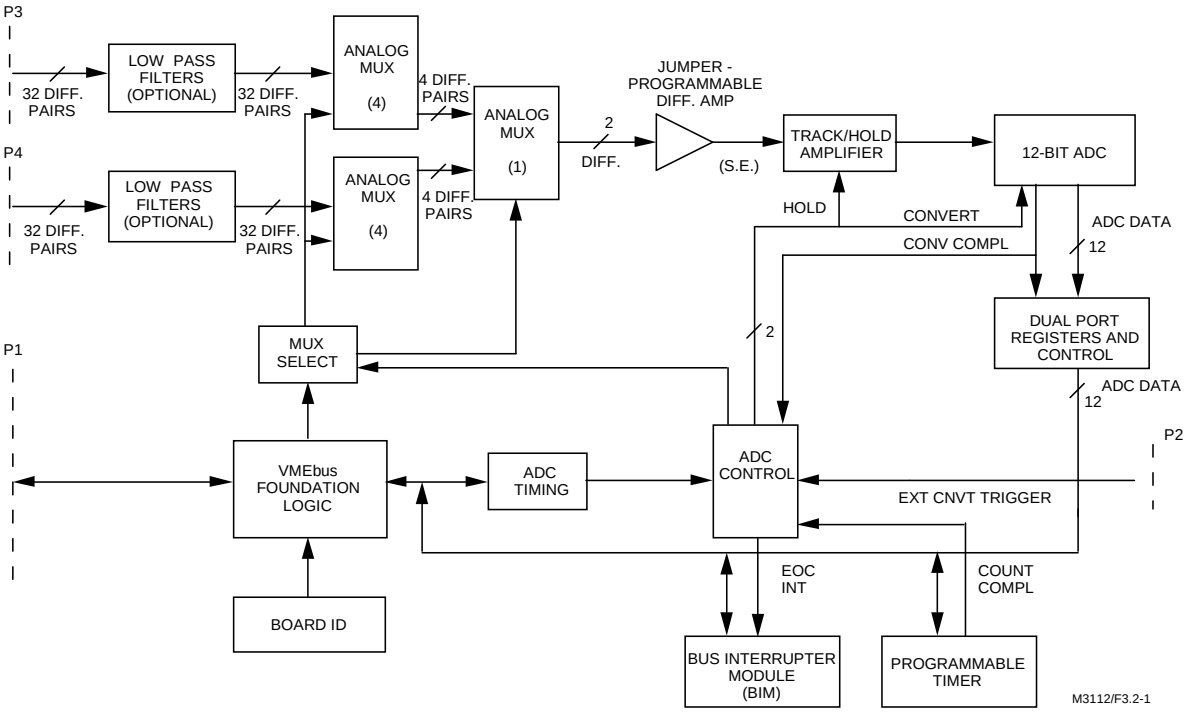


Figure 3.2-1. VMIVME-3112 Functional Block Diagram

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3.3 VMEbus CONTROL INTERFACE

The VMIVME-3112 communication registers are memory-mapped as 128 (decimal), 16-bit words. The registers are contiguous and may be user-located on any 256-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged bus communications or both.

During each read or write operation, all VMEbus control signals are ignored unless the board-selection comparator detects a match between the on-board selection jumpers shown in Figure 3.3-1, and the address and address modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open collector DTACK interface signal is asserted (driven LOW). Subsequent removal of the bus master's read or write command causes the board-generated DTACK signal to return to the OFF state.

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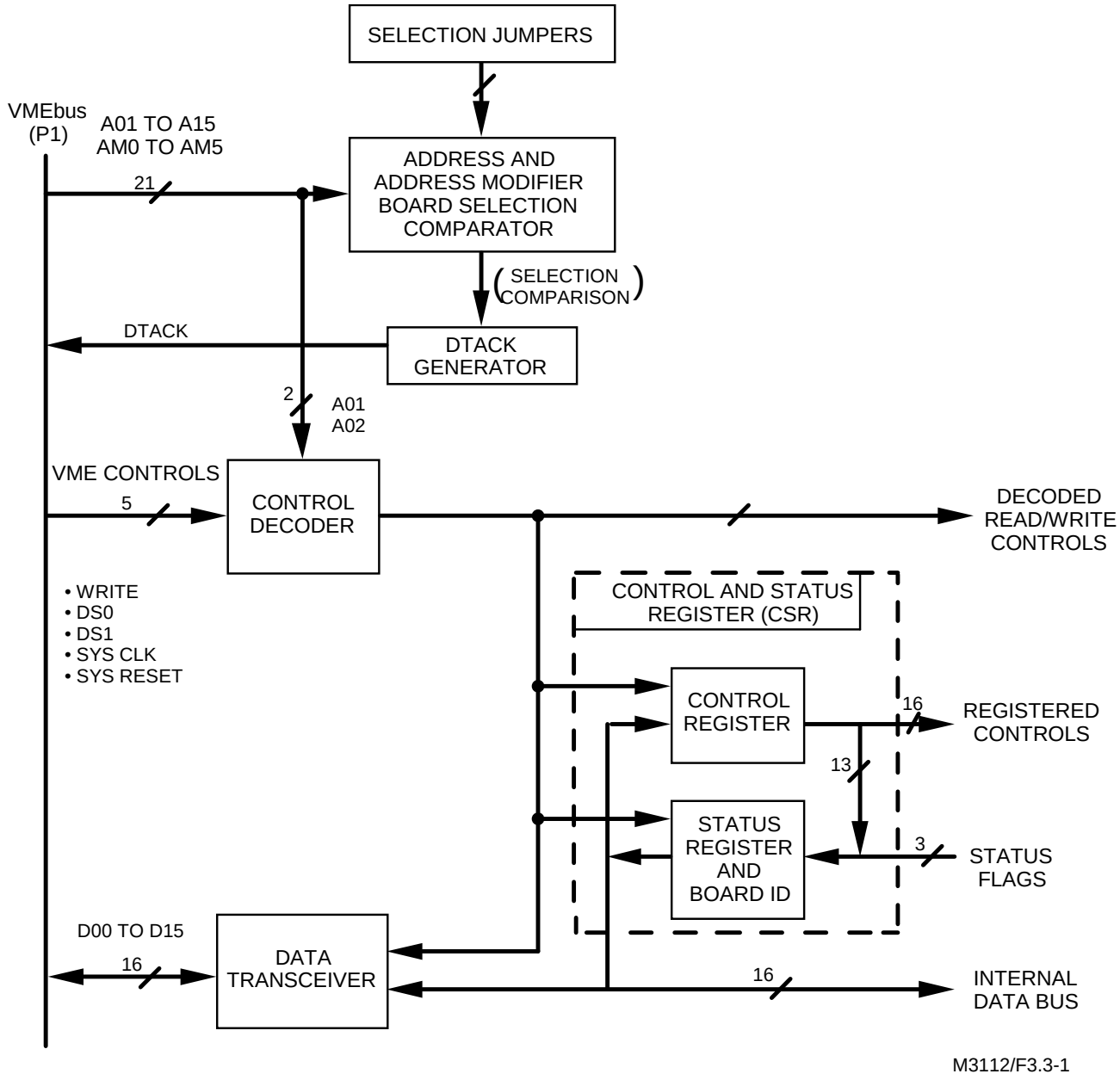


Figure 3.3-1. VMEbus Control Signals and Interface Logic

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After board-selection has occurred, three groups of VMEbus signals control communications with the board. They are as follows:

a. Data Bus lines D00 to D15
b. Address lines A01, A02, A03, A04, A05, A06, A07
c. Bus Control Signals:
    (1) WRITE
    (2) DS0,* DS1*
    (3) SYS CLK
    (4) SYS RESET*

Data bus lines are bi-directional and move data to and from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A07 map the 128 communication registers onto a 256-byte range within the VME address space (Section 4). The control signals determine whether data is to be moved to the VMIVME-3112 (write) or from the VMIVME-3112 (read), provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all timers and flags.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC are read through the Status Register. The control and status registers are referred to collectively as the Control and Status Register (CSR), since they are at the same address. The WRITE signal determines which one is accessed. Most of the control register outputs can be monitored directly through the Status Register.

3.4 ANALOG-TO-DIGITAL (ADC) CONTROL AND TIMING

Control commands and status flags associated with controlling the ADC are illustrated in Figure 3.3-1, and are described in Section 4 and the following sections.

There are three mode control bits in the CSR. The programming of these control bits (Mode 0H through Mode 2H) determine which one of five ADC operating modes the board is to operate in. The five ADC operating modes and the Control Register mode control bits are:

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	CSR CONTROL BITS		
	MODE2H D8	MODE1H D7	MODE0H D6
a. AUTO SCANNING MODE	0	0	0
b. RANDOM POLL MODE	0	0	1
c. RANDOM INTERRUPT MODE	0	1	0
d. SCANNING POLL MODE	0	1	1
e. SCANNING INTERRUPT MODE	1	0	0

The ADC operating modes basically determine if the on-board ADC and channel selection are controlled externally by a CPU board or by the on-board channel sequencer. They also determine whether an interrupt will be generated when the conversion(s) are complete. The five ADC operating modes will be described from a programming viewpoint in Section 4.

The AUTO SCANNING MODE (Mode 0), RANDOM POLL MODES, and SCANNING POLL MODE will be discussed here to reveal the ADC controls and timing intervals. The other two modes use interrupts instead of polling to determine when a conversion or a series of conversions are completed.

3.4.1 RANDOM POLLING and RANDOM INTERRUPT MODES

To enter the RANDOM POLLING MODE, the three mode control bits, Mode 0H through Mode 2H, must be set in the CSR to a "one", "zero" and "zero", respectively. In this mode the CPU board controls the channel to be converted, starts the conversion, and polls an end-of-conversion bit to determine when the conversion is complete. This mode is entitled RANDOM because the CPU board can select channels to be converted in any random order (i.e., CH2, CH0, CH63, CH14…). The RANDOM INTERRUPT MODE is entered when mode control bits Mode 0H through Mode 2H are set in the CSR to "zero", "one" and "zero", respectively. This mode is essentially the same as the RANDOM POLLING MODE except an end-of-conversion interrupt is generated.

3.4.2 AUTO SCANNING MODE

The AUTO SCANNING MODE is automatically entered at power-up of the board (or when the mode control bits Mode 0H through Mode 2H are set to "zeros" in the CSR). This mode performs a sequential scan of all configured inputs (minimum of 16; see Section 5.4.6), digitizing the input, and storing the results in dual port registers. The gain amplifier must be set to a gain of "one" in the AUTO SCANNING MODE. Once all inputs are digitized, the process begins over at channel "zero". Any time a particular channel is read, the latest digitized information is available in that channel's dual port register. This mode frees the programmer from selecting and starting a conversion on each channel thus, allowing the board to digitize at a faster rate and making programming of the board simpler.

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3.4.3 SCANNING POLL and SCANNING INTERRUPT MODES

The SCANNING POLL MODE is similar to the AUTO SCANNING MODE. This mode executes a single scan of all channels and then stops. An end-of-scan status bit is polled to determine when the scan is completed. The SCANNING INTERRUPT MODE differs in that the end-of-scan generates an interrupt to the CPU board. The SCANNING POLL MODE may be entered by setting MODE 0H through Mode 2H in the CSR to "one", "one" and "zero", respectively. The SCANNING INTERRUPT MODE may be entered by setting MODE 0H through Mode 2H in the CSR to "zero", "zero" and "one", respectively. A Bus Interrupter Module (BIM) handles the interrupt functions and is described in paragraph 3.10.

3.5 ADC CONVERSION AND TIMING

Regardless of which ADC OPERATING MODE, described in Section 3.4, is used, the A/D conversion sequence is the same. Once the conversion sequence has begun (for any of the five A/D operating modes), it consists of the following consecutive time intervals:

a. Settling Delay
b. Tracking Interval
c. Analog-to-Digital (A/D) Conversion

All ADC timing intervals discussed in this section are performed automatically by the on-board smart controller.

The settling delay occurs directly after a state-change has occurred in the analog networks (such as selecting a new input channel), and represents the settling time of the networks. After the settling delay has been completed, the Track-and-Hold (T&H) amplifier (Figure 1.2-1) enters the TRACKING MODE, and the tracking interval begins. During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage.

At the end of the tracking interval, the T&H amplifier enters the HOLD MODE, in which the output of the amplifier is held at a constant level, and a CONV CMD from the timing decoder causes the A/D conversion to begin. The A/D conversion digitizes the output of the T&H amplifier into a 12-bit data word, and then terminates the conversion sequence. The CONV COMPL L flag from the ADC is HIGH during the conversion, and is LOW otherwise.

In the RANDOM POLL MODE, completion of the A/D conversion causes the NEW DATA RDY flag to be set HIGH, indicating that valid data is present in the Random Converter Data Register (RCDR) (Section 4). The action of reading the RCDR resets the NEW DATA RDY and CONV COMPL L flag in the CSR.

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If the conversion is the last channel to be converted in the SCANNING POLL MODE, then a flag (REGD END OF SCAN H) is set in the Control and Status Register (CSR). This flag may be read to determine that all channels have been converted and stored and are available to be read.

3.6 ANALOG INPUTS

Sixty-four differential or single-ended analog input channels are available from two front panel connectors. It is recommended that the differential mode be used for increased noise and common mode rejection. Unused inputs should be grounded. This includes the low-side of differential inputs. For correct operation, both the high-side and low-side inputs must be within ±12 V of the VME chassis ground.

3.6.1 Low Pass Filters and Input Multiplexers

The 64 analog input channels can be provided with individual, single-pole, low pass filters as shown in Figure 3.6.1-1, and can be user-configured to operate either single-ended or differentially. See Section 2.3.2 for input filter specifications.

To achieve maximum system accuracy with filtered analog inputs, the sample rate should be limited to 2,000 Hz or less per channel. Higher sample rates will produce reflected "pump back" currents at the inputs which can induce error voltages across the filter input resistors. This implies that when filters are installed, a minimum of 16 channels can be continuously scanned in the AUTO SCAN MODE.

Each of the 64 analog inputs is selectable through one of eight input multiplexers. Each multiplexer accepts eight differential input pairs. A second tier multiplexer receives the selected channel from one of the eight input multiplexers.

Both multiplexer sections are controlled by the same set of six address lines (INP MUX ADDRESS), which are derived from control bits "MUX A00" through "MUX A05" from the Control Register.

3.6.2 Single-Ended Versus Differential Operation

Differential or single-ended operation of the analog inputs is selected by the location of single-in-line-package (SIP) resistors, as illustrated in Figure 3.6.1-1. The input multiplexers are ***always*** operated in the differential

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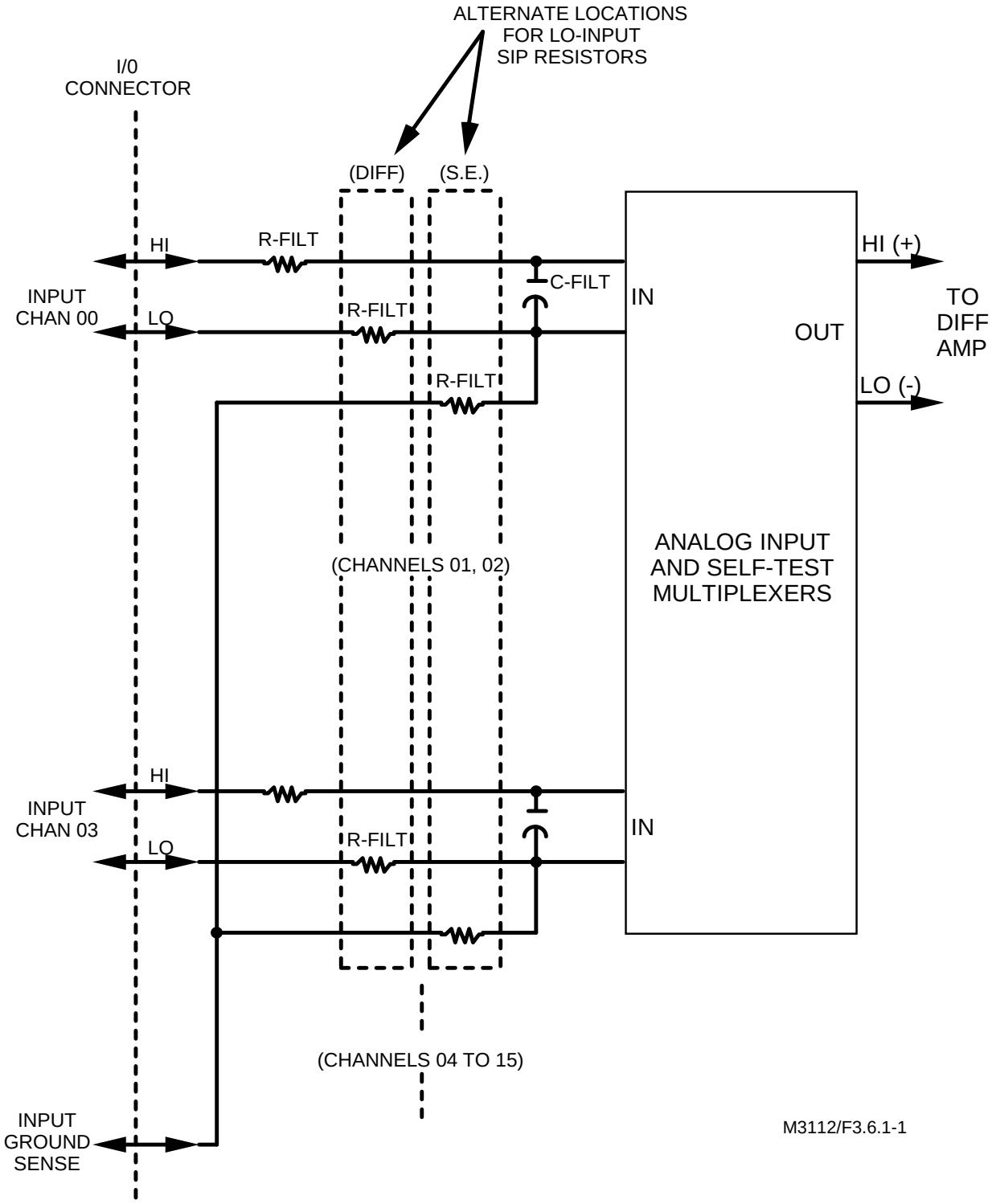


Figure 3.6.1-1. Single-Ended and Differential Input Configurations

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mode; single-ended (pseudo-differential) operation is obtained by connecting the LOW input resistor to the common INPUT GROUND SENSE input instead of to the individual LOW signal inputs.

To prevent high frequency noise from becoming a common mode signal and causing the data output of the VMIVME-3112 to fluctuate, the input circuits are made single-ended and all of the row C pins are grounded. This means that all of the RFILT resistor SIPs in the schematic are replaced with SIP headers. These are essentially 0 Ω SIP resistors. Jumper J2 is also installed. Now all of the inputs have their returns tied to local ground via a low resistance path. This also shifts the pole frequency of the input filter, since half of the input resistance is gone. The new frequency is twice that of the differential value.

All VMIVME-3112 input channels are overvoltage protected by current-limiting input resistors. See Section 2, paragraph 2.3 for input overvoltage specifications.

3.7 JUMPER-PROGRAMMABLE GAIN AMPLIFIER

Once an input channel has been selected and routed through the input multiplexers, it enters the Programmable Gain Amplifier as a differential input. The differential amplifier rejects COMMON MODE noise and delivers a scaled single-ended output to the Track-and-Hold (T&H) device. The Programmable Gain Amplifier may be jumpered for gains of 1, 10, 100, 200, and 500. This allows for an input in the -10 mV to +10 mV range to be scaled up to a -5 V to +5 V input range for the ADC. When a gain of 500 is selected the GAIN DEL bit (D15) in the CSR must be set. This increases the analog acquisition time from 15 µs to 28 µs to allow complete input setting for the new channel. Figure 3.7-1 shows the gain configuration for the Programmable Gain Amplifier.

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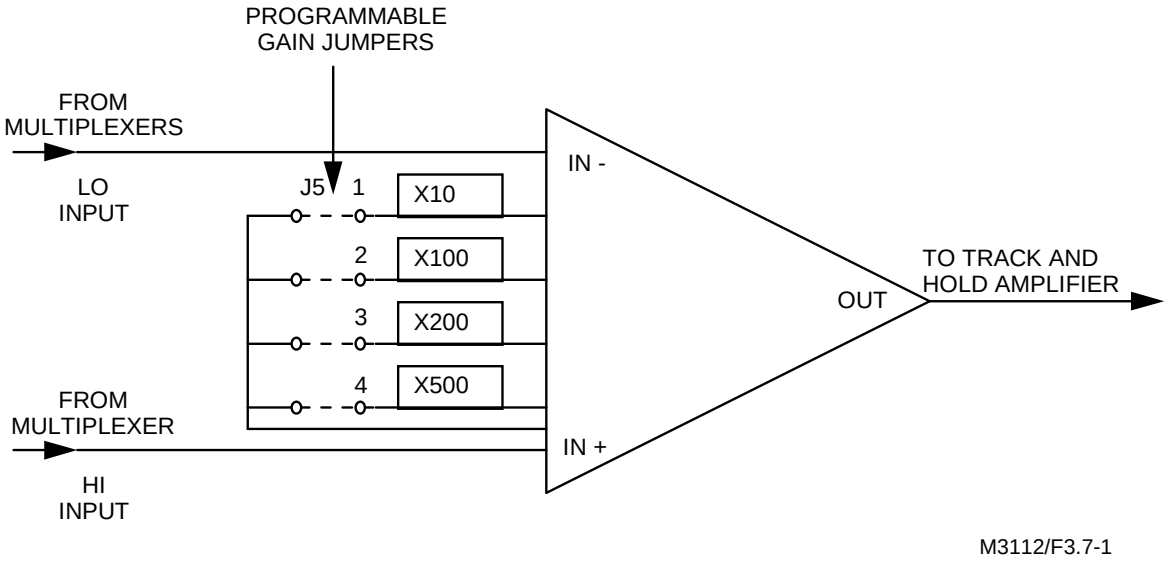


Figure 3.7-1. Programmable Gain Amplifier

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3.8 CHANNEL SEQUENCER AND DUAL PORT REGISTER CONTROL

When the VMIVME-3112 is operated in any of the scanning modes, the operation is controlled by an on-board channel sequencer. For example, when the board is powered-on, a conversion sequence begins at Channel 00 as discussed in Section 3.5.1. Once the A/D conversion is completed, the dual port control logic takes the converted data and stores it in that channel's appropriate dual port register. The channel counter is incremented by one, which selects the next channel to be multiplexed to the ADC. Concurrently with selecting the next channel, a new A/D conversion sequence is initiated. When all input channels have been converted and stored, the channel counter is reset to "zero" and starts the channel scanning sequence again (AUTO SCANNING MODE only).

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3.9 PROGRAMMABLE INTERVAL TIMER

A triple, 16-bit timer (cascadeable to 48 bits) may be programmed to trigger the start of an ADC scan sequence. For example, it might be required to get updated digitized data only once every second. The board could be set for the SCANNING INTERRUPT MODE. The timer would be set to generate a pulse once every second. That pulse would initiate the ADC scan sequence.
Once all channels are digitized and stored, an end of scan interrupt would be generated to the CPU to indicate that data is available. The interrupt service routine would read the data into memory and then re-initialize the Bus Interrupter Module (BIM) for the next interrupt.

3.10 BUS INTERRUPTER MODULE (BIM)

An MC68153 BIM handles all interrupt interfacing to the VMEbus. An interrupt may be generated on any VMEbus level (1 through 7). Depending on the mode used, an interrupt may be generated upon the completion of a single A/D conversion, or upon the completion of a 16- through 64-channel scan.

The BIM generates an 8-bit vector (D08(O)) after generating an Interrupt Request and in response to the Interrupt Acknowledge cycle from the CPU board. This 8-bit vector is multiplied by four in the 680X0 CPU and this calculated address plus the VBR (Vector Base Register) points to the location of the interrupt service routine to read the ADC digitized data. An interrupt program example is found in Section 4.

If there are empty backplane slots between the VMIVME-3112 and the CPU, then IACK jumpers may be needed on the backplane.

3.11 BOARD ID REGISTER

The first word location of the VMIVME-3112's register set is a read-only register. It always reads 08XX (HEX; the last two digits are not specified). Other VMIC products have similar registers which read different constants. This allows general-purpose system software to automatically determine what boards have been installed (by reading from a predetermined list of addresses). The configuration software must be able to handle a bus error if it might read an empty location.

3.12 BUILT-IN POWER CONVERTER

Electrical power for the VMIVME-3112 analog network is supplied by the DC-to-DC converter shown in Figure 3.12-1. The converter transforms 5 V logic power into regulated and isolated ±15 VDC power, with a load capacity of approximately 100 mA on each 15 V bus.

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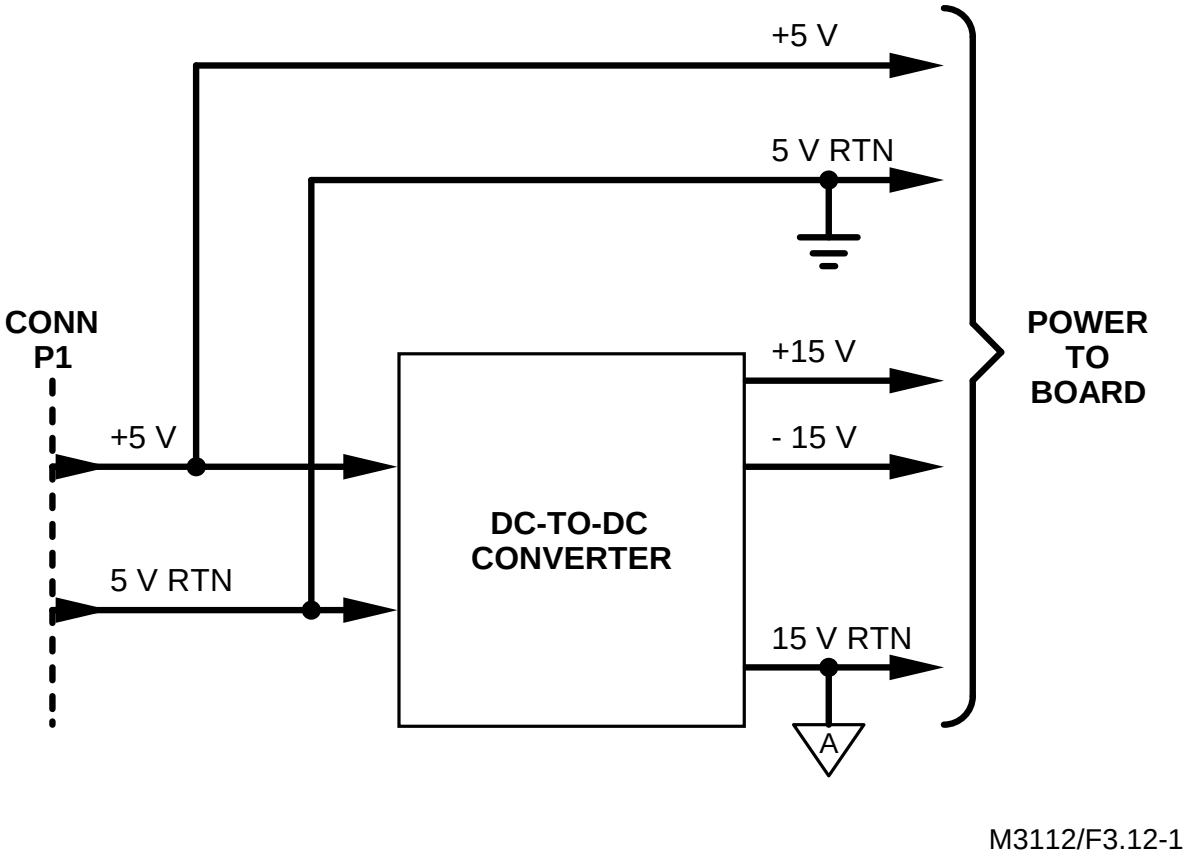


Figure 3.12-1. Power Converter

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

Communication with the VMIVME-3112 takes place through 128 contiguous, 16-bit register locations which are mapped into the VME short I/O address space. Most VMEbus CPUs access the short I/O space as if it were a 64-Kbyte block of conventional memory. Consult your CPU manual to determine the address of this block.

The VMIVME-3112 supports byte and word (16-bit) accesses. The order of the bytes within a word depends on the model of CPU used. For instance, most 68000-based CPUs put the most significant byte at the same address as the word. The least significant byte is at the next address. Note that if the AUTOSCAN data is read as two bytes, they may be from different conversion cycles. This can introduce a 256-count error in the reading.

Functions of the communications registers, which are discussed in detail within this section, are summarized in Table 4.1-1. Some of the registers are not used, and are labeled "reserved". Reserved registers may be duplicate mappings of normal Control Registers. They should not be used, since they could be affected by a design change.

4.2 CONTROL AND STATUS REGISTER DESCRIPTIONS

The communication register located at relative address 02H is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

a. Analog input channel selection
b. A/D operating modes
c. Start A/D conversion
d. Start Programmable Timer
e. Two's complement selection
f. Front panel Fail Indicator
g. Board RESET
h. Gain Delay

The CSR is 16 bits in length, and is detailed in Tables 4.2-1 and 4.2-2. The function of each control bit and status flag is described in detail, subsequently, in the associated programming discussions.

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Table 4.1-1. Communications Register Map

RELATIVE ADDRESS HEX	RELATIVE ADDRESS DEC	REGISTER NAME	ACCESS MODE
00	00	BOARD IDENTIFICATION	READ
02	02	CSR	READ/WRITE
04 THROUGH 0E	04 THROUGH 14	(RESERVED)	---
10 THROUGH 1E	16 THROUGH 30	BUS INTERRUPTER (BIM)	READ/WRITE
20 THROUGH 26	32 THROUGH 38	PROGRAMMABLE TIMER	READ/WRITE
28 THROUGH 2E	40 THROUGH 46	(RESERVED)	---
30	48	RCDR (SINGLE CONVERSION DATA)	READ
32 THROUGH 7E	50 THROUGH 126	(RESERVED)	---
80	128	SCAN DATA CH 00	READ/WRITE
82	130	SCAN DATA CH 01	READ/WRITE
84	132	SCAN DATA CH 02	READ/WRITE
86	134	SCAN DATA CH 03	READ/WRITE
88	136	SCAN DATA CH 04	READ/WRITE
8A	138	SCAN DATA CH 05	READ/WRITE
8C	140	SCAN DATA CH 06	READ/WRITE
8E	142	SCAN DATA CH 07	READ/WRITE
90	144	SCAN DATA CH 08	READ/WRITE
92	146	SCAN DATA CH 09	READ/WRITE
94	148	SCAN DATA CH 10	READ/WRITE
96	150	SCAN DATA CH 11	READ/WRITE
98	152	SCAN DATA CH 12	READ/WRITE
9A	154	SCAN DATA CH 13	READ/WRITE
9C	156	SCAN DATA CH 14	READ/WRITE
9E	158	SCAN DATA CH 15	READ/WRITE
A0	160	SCAN DATA CH 16	READ/WRITE
A2	162	SCAN DATA CH 17	READ/WRITE
A4	164	SCAN DATA CH 18	READ/WRITE
A6	166	SCAN DATA CH 19	READ/WRITE
A8	168	SCAN DATA CH 20	READ/WRITE
AA	170	SCAN DATA CH 21	READ/WRITE
AC	172	SCAN DATA CH 22	READ/WRITE
AE	174	SCAN DATA CH 23	READ/WRITE
B0	176	SCAN DATA CH 24	READ/WRITE
B2	178	SCAN DATA CH 25	READ/WRITE
B4	180	SCAN DATA CH 26	READ/WRITE
B6	182	SCAN DATA CH 27	READ/WRITE

M3112/T4.1-1/1

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Table 4.1-1. Communications Register Map (Concluded)

RELATIVE ADDRESS HEX	RELATIVE ADDRESS DEC	REGISTER NAME	ACCESS MODE
B8	184	SCAN DATA CH 28	READ/WRITE
BA	186	SCAN DATA CH 29	READ/WRITE
BC	188	SCAN DATA CH 30	READ/WRITE
BE	190	SCAN DATA CH 31	READ/WRITE
C0	192	SCAN DATA CH 32	READ/WRITE
C2	194	SCAN DATA CH 33	READ/WRITE
C4	196	SCAN DATA CH 34	READ/WRITE
C6	198	SCAN DATA CH 35	READ/WRITE
C8	200	SCAN DATA CH 36	READ/WRITE
CA	202	SCAN DATA CH 37	READ/WRITE
CC	204	SCAN DATA CH 38	READ/WRITE
CE	206	SCAN DATA CH 39	READ/WRITE
D0	208	SCAN DATA CH 40	READ/WRITE
D2	210	SCAN DATA CH 41	READ/WRITE
D4	212	SCAN DATA CH 42	READ/WRITE
D6	214	SCAN DATA CH 43	READ/WRITE
D8	216	SCAN DATA CH 44	READ/WRITE
DA	218	SCAN DATA CH 45	READ/WRITE
DC	220	SCAN DATA CH 46	READ/WRITE
DE	222	SCAN DATA CH 47	READ/WRITE
E0	224	SCAN DATA CH 48	READ/WRITE
E2	226	SCAN DATA CH 49	READ/WRITE
E4	228	SCAN DATA CH 50	READ/WRITE
E6	230	SCAN DATA CH 51	READ/WRITE
E8	232	SCAN DATA CH 52	READ/WRITE
EA	234	SCAN DATA CH 53	READ/WRITE
EC	236	SCAN DATA CH 54	READ/WRITE
EE	238	SCAN DATA CH 55	READ/WRITE
F0	240	SCAN DATA CH 56	READ/WRITE
F2	242	SCAN DATA CH 57	READ/WRITE
F4	244	SCAN DATA CH 58	READ/WRITE
F6	246	SCAN DATA CH 59	READ/WRITE
F8	248	SCAN DATA CH 60	READ/WRITE
FA	250	SCAN DATA CH 61	READ/WRITE
FC	252	SCAN DATA CH 62	READ/WRITE
FE	254	SCAN DATA CH 63	READ/WRITE

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Table 4.2-1. Control Register Functions

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

CONTROL BIT	NAME	FUNCTION
D0 D1 D2 D3 D4 D5	MUX A0 H MUX A1 H MUX A2 H MUX A3 H MUX A4 H MUX A5 H	D0 through D5 select the analog input channel to be converted. These bits only need to be selected in RANDOM POLLING or RANDOM INTERRUPT MODE.
D6 D7 D8	MODE 0H MODE 1H MODE 2H	These three bits specify 1 of 5 ADC operating modes. D8 D7 D6 0 0 0 - AUTO SCANNING MODE 0 0 1 - RANDOM POLLING MODE 0 1 0 - RANDOM INTERRUPT MODE 0 1 1 - SCANNING POLL MODE 1 0 0 - SCANNING INTERRUPT MODE
D9	SOFTWARE RESET H	When D9 is high "one", all on-board A/D timing networks are cleared.
D10	COUNT START H	When D10 is set high "one", the Programmable Timer starts counting if it has been previously programmed.
D11	ENA EXT STRT H	When D11 is set high "one", the on-board external A/D start logic is enabled to accept an external trigger.
D12	TWO'S COMPL H	ADC coding format is offset binary if D12 is low "zero", or two's complement if D12 is high "one".
D13	EN START CONV H	A single A/D conversion or conversion scan is enabled each time a "one" is written to this control bit and an ADC RANDOM or SCANNING OPERATING MODE is selected by D6 through D8.
D14	FAIL LED L	The Fail LED is OFF if this bit is set to "one", and is ON if the bit is zero.
D15	GAIN DELAY H	When this bit is set the Analog Input Acquisition time increases from 15 µs to 28 µs. This bit should be set when a gain of 500 is selected on the programmable gain amplifier.

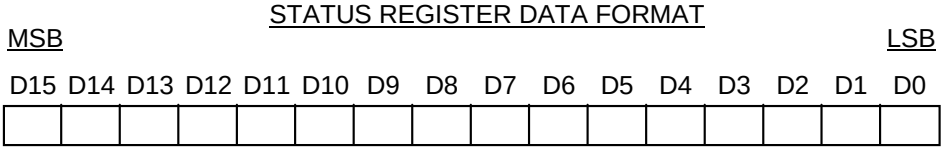
NOTE

ALL CONTROL BITS ARE POWERED-UP IN A LOGIC "ZERO" STATE

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Table 4.2-2. Status Register Flags

STATUS REGISTER DATA FORMAT



CONTROL BIT	NAME	FUNCTION
D0*	MUX A0 H	D0 through D5 select the analog input channel.
D1*	MUX A1 H	
D2*	MUX A2 H	
D3*	MUX A3 H	
D4*	MUX A4 H	
D5*	MUX A5 H	
D6*	MODE 0H	These three bits specify 1 of 5 ADC operating modes.
D7*	MODE 1H	
D8*	MODE 2H	
D9*	SOFTWARE RESET H	When D9 is high "one", all on-board A/D timing networks are cleared.
D10*	COUNT START H	When D10 is set high "one", the Programmable Timer starts counting if it has been previously programmed.
D11*	ENA EXT STRT H	When D11 is set high "one", the on-board external A/D start logic is enabled to accept an external trigger.
D12*	TWO'S COMPL H	ADC coding format is offset binary if D12 is low "zero", or two's complement if D12 is high "one".
D13	REGD END OF SCAN H	This flag when read high "one" indicates that a single A/D scan off all channels has been completed. Used only in SCANNING POLL MODE.
D14*	FAIL LED L	The Fail LED is OFF if this bit is set to "one", and is ON if the bit is "zero".
D15	NEW DATA RDY H	This flag when read high "one" indicates that an A/D conversion of a single channel has been completed. Used only in RANDOM POLLING MODE.

D8	D7	D6	
0	0	0	- AUTO SCANNING MODE
0	0	1	- RANDOM POLLING MODE
0	1	0	- RANDOM INTERRUPT MODE
0	1	1	- SCANNING POLL MODE
1	0	0	- SCANNING INTERRUPT MODE

M3112/T4.2-2

* These bits read back the corresponding CONTROL REGISTER bits.

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4.3 INITIALIZATION

When SYSTEM RESET is applied to the board, the Control Register and all Analog-to-Digital Converter (ADC) flags are cleared to the LOW state "zero". An independent BOARD RESET can be generated by setting the SOFTWARE RESET control bit to a "one". The board will remain reset until the SOFTWARE RESET bit is cleared.

4.4 CONTROLLING AND READING THE ANALOG-TO-DIGITAL CONVERTER DATA

The VMIVME-3112 has a number of features which allow the board to be used in a variety of applications. The simplest mode of operation is the AUTO SCANNING MODE which is automatically entered at power-up.

4.4.1 AUTO SCANNING MODE

This mode is entered at power-up, or the CSR may be programmed to enter this mode. The AUTO SCANNING MODE allows the user to operate the board without setting any control bits in the CSR and without selecting each channel to be converted. On power-up the VMIVME-3112 initiates a conversion on CH 0 and sequentially performs conversions through the last channel desired, then begins again at CH 0. After each conversion, the data for that channel is stored in a dual port register which is also accessible to the VMEbus and may be read at any time. Jumper field J6 controls how many channels are scanned. Refer to Section 5 for configuration of these jumpers. The gain amplifier must be set to a gain of "one" in the AUTO SCANNING MODE. A minimum of 16 channels must be scanned when filters are installed on the board. Refer to Section 3.6.1.

Every scan of the connected input channels results in digitized data written to the SCAN DATA registers, thus, overwriting the data from the previous scan. Any time a read is performed the latest data is always received.

To enter the AUTO SCANNING MODE (automatically entered at power-up), the following CSR bits must be set:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	0	0

4.4.2 SCANNING POLL MODE

The SCANNING POLL MODE performs a single scan of the input channels, but stops the scanning process after the last channel has been digitized. The REGD END OF SCAN H flag (bit D13) is then set in the Status Register.

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Polling this bit allows the CPU board to determine when the scan has been completed and the SCAN DATA registers have updated data.

The Programmable Timer (8254) may be set to periodically generate a signal which starts the SCANNING POLL MODE. For example, the timer may be programmed to generate a pulse once every second which starts the scan. The CPU must still poll the REGD END OF SCAN H bit until it goes high, so the SCANNING INTERRUPT MODE is a better candidate for use with the timer. The Programmable Timer (8254) programming considerations are detailed in Section 4.4.6.

To enter the SCANNING POLL MODE the following CSR bits must be set:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	1	1

4.4.3 SCANNING INTERRUPT MODE

The SCANNING INTERRUPT MODE performs a single scan of the input channels, then stops operating, the same as the SCANNING POLL MODE. Instead of setting a flag bit in the Status Register, a signal is generated to the Bus Interrupter Module (68153) which generates a VMEbus Interrupt to the CPU board. The Bus Interrupter Module (68153) must have previously been programmed to generate this VMEbus Interrupt and also to respond with an 8-bit vector during the Interrupt Acknowledge cycle generated by the CPU board. Programming of the Bus Interrupter Module (68153) is detailed in Section 4.4.7.

The SCANNING INTERRUPT MODE can be used along with the Programmable Timer (8254) to perform periodic data logging. To do this, it is necessary to set up the timer and interrupter chips as described in Sections 4.4.6 through 4.4.9. The control word for the CSR must have bit 10 (COUNT STARTH) set instead of bit 13 (EN START CONV H). In addition to having low CPU overhead, this mode minimizes digital activity on the VMIVME-3112 during conversions.

To enter the SCANNING INTERRUPT MODE the following CSR bits must be set :

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
1	0	0

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4.4.4 RANDOM POLLING MODE

The RANDOM POLLING MODE is the traditional method of controlling an A/D conversion. The CPU board writes to the Control Register selecting the channel to be converted using Control Registers bits MUX A5H through MUX A0H (D5 through D0). The CPU must then set the EN START CONV H bit (D13), which starts the multiplexer acquisition, and ADC timing sequence which was detailed in Section 3.5. The CPU must then poll the NEW DATA RDY H bit (D15) in the Status Register. When this flag goes high, the A/D conversion is complete and the data has been stored in the Random Conversion Data Register (RCDR). The CPU board then reads this data and selects the next channel to be converted. This mode is useful when channels desired to be converted are not in sequential order, thus channels can be selected in a Random order. It is also useful when some channels must be converted more often than others. Each time a new channel is selected for A/D Conversion, the Mode Control bits must be set to the RANDOM POLLING MODE. The following CSR bits must be set:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	0	1

4.4.5 RANDOM INTERRUPT MODE

The RANDOM INTERRUPT MODE operates the same as the RANDOM POLLING MODE described above. The only difference is that CPU is signaled that the A/D conversion is complete by a VMEbus Interrupt generated by the on-board Bus Interrupter Module (68153). The Bus Interrupt Module must be programmed before the first conversion is completed. Then after each interrupt is serviced the Bus Interrupter Module must be re-enabled by one load operation. Refer to Sections 4.4.8 and 4.4.9 for more information on programming the Bus Interrupter Module. Each time a new channel is selected for A/D conversion, the Mode Control bits must be set to the RANDOM INTERRUPT MODE. The following CSR bits must be set:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	1	0

4.4.6 Programmable Interval Timer (8254)

The 8254 is a very versatile counter/timer device with six different timing modes of operation. However, only one mode is described here. That mode is called RATE GENERATOR. Using this mode allows the board to operate similar to a data-logger. Basically this mode functions like a divide-by-n counter. The

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counter is loaded with n counts and is then told to start counting by setting a bit in the CSR (count START H-data bit 10). When the count has decremented to "one", a pulse is generated which starts the A/D scanning sequence which has previously been programmed. The scanning sequence must be either the SCANNING INTERRUPT MODE or the SCANNING POLL MODE as discussed in Sections 4.4.2 and 4.4.3.

When the scan is done and the board is in the SCANNING INTERRUPT MODE, an end-of-scan interrupt will be issued to the host CPU. Otherwise, the CPU must poll the registered end-of-scan H bit in the CSR to determine when the scan is done. The dual port registers are then read by the CPU. Concurrently with this, the Interval Timer reloads the counter and begins counting again. The counting time interval must be longer than the time required to read all the dual port registers plus the time for the A/D scan sequence to complete. This time is approximately 2 ms when all 64 channels are being scanned.

The 8254 has three counters of 16-bit width. The counter clock is 8 MHz which results in timer resolution of 125 ns or 0.125 µs. One 16-bit counter, if loaded with a maximum count of FFFF HEX, would generate a start scan pulse every 8.192 ms. This is determined as follows:

2^{16} = 65,536 (Decimal equivalent of loaded count)
x0.125×10^{-6} (Period of 8 MHz Clock) = 8.192×10^{-3} second

Three 16-bit counters may be cascaded to make a 48-bit counter. Two counters cascaded together and loaded with all "ones" would generate a start scan pulse every eight minutes and 57 seconds. Refer to Section 5.4.5 to determine jumper configurations for cascading counters.

The Programmable Timer occupies 4 words of address space and its relative address is shown in Table 4.1-1. Each write to the Programmable Timer is a word in length (D15 to D0) of which all necessary information is contained in the lower byte (D7 through D0). The relative address of each register in the 8254 is shown in Table 4.4.6-1.

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Table 4.4.6-1. Programmable Timer (8254) Register Map

REGISTER ADDRESS HEX	REGISTER ADDRESS DEC	REGISTER NAME
20	32	COUNTER 0 - LS BYTE
20	32	COUNTER 0 - MS BYTE
22	34	COUNTER 1 - LS BYTE
22	34	COUNTER 1 - MS BYTE
24	36	COUNTER 2 - LS BYTE
24	36	COUNTER 2 - MS BYTE
26	38	COUNTERS 0 TO 2 CONTROL WORD

M3112/T4.4.6-1

Since the 8254 stores only the data presented on D7 to D0, two loads are required to enter a full 16-bit count sequence. This can be seen by reviewing Table 4.4.6-1. Each counter register must be loaded twice. The first load sets the least significant byte of the count and the second load sets the most significant byte of the count. For each counter the control word must be written first, then the count is written.

4.4.7 Programmable Interval Timer Programming Sequence

Table 4.4.7-1 gives the address of each Counter Register and a description of the data to load into each register. Review Section 5.4.5 concerning jumper installation on cascading counters for maximum counter lengths of 16, 32, or 48 bits.

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Table 4.4.7-1. Timer Programming Sequence

COUNTER NUMBER	LOAD SEQUENCE	REGISTER ADDRESS (HEX)	REGISTER NAME	DATA (HEX)	MAX COUNT
COUNTER 0	1	26	CONTROL WORD	34	16 BITS
	2	20	CTR0 LS BYTE	LEAST SIGNIFICANT BYTE OF COUNT	
	3	20	CTR0 MS BYTE	MOST SIGNIFICANT BYTE OF COUNT	
COUNTER 1	4	26	CONTROL WORD	74	32 BITS
	5	22	CTRL1 LS BYTE	LEAST SIGNIFICANT BYTE OF COUNT	
	6	22	CTRL1 MS BYTE	MOST SIGNIFICANT BYTE OF COUNT	
COUNTER 2	7	26	CONTROL WORD	B4	48 BITS
	8	24	CTR2 LS BYTE	LEAST SIGNIFICANT BYTE OF COUNT	
	9	24	CTR2 MS BYTE	MOST SIGNIFICANT BYTE OF COUNT	

M3112/T4.4.7-1

4.4.8 Programming the Bus Interrupter Module (BIM)

The Bus Interrupt Module handles all interrupt interfacing to the CPU board. An interrupt may be generated on any VMEbus level (1 through 7). Interrupts are generated when the BIM is programmed to do so and when one of the following two ADC operating modes are employed: RANDOM INTERRUPT MODE and SCANNING INTERRUPT MODE.

The RANDOM INTERRUPT MODE generates an interrupt upon the completion of a single A/D conversion. The SCANNING INTERRUPT MODE generates an interrupt upon the completion of a 2- through 64-channel scan.

When one of the above interrupt conditions occurs, the BIM generates a VMEbus level 1 through 7 interrupt. The BIM interrupt must be previously enabled and the interrupt level must be previously programmed for the BIM to operate.

4.4.9 Bus Interrupter Module (BIM) Programming Sequence

The BIM uses only one of its four interrupt channels. Therefore, only one Interrupt Control Register (XX10) and one Interrupt Vector Register (XX18) need to be programmed. After each interrupt the Interrupt Control Register must be loaded to re-enable for the next interrupt. Table 4.4.9-1 shows the Interrupt Control and Vector Registers bit definitions. However, for most applications the bits defined in Table 4.4.9-2 are all that are necessary for proper interrupt operation.

When an interrupt is accepted by the CPU board, it responds with an Interrupt Acknowledge cycle. This is a type of read cycle in which the interrupting device (the BIM) responds with an 8-bit Interrupt Vector on data bits 0 to 7. For a 680X0 CPU board, this vector is multiplied by four and added to the Vector Base

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Table 4.4.9-1. Interrupt Control and Vector Registers (Bit Assignments)

INTERRUPT CONTROL REGISTER (AT ADDRESS XX10 HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0 = INT 1 = EXT	INTERRUPT ENABLE	INTERRUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

INTERRUPT VECTOR REGISTER (AT ADDRESS XX18 HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONE INTERRUPT VECTOR							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

M3112/T4.4.9-1

Table 4.4.9-2. Interrupt Control and Vector Registers (Bit Definitions)

INTERRUPT CONTROL REGISTER (AT ADDRESS XX10 HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X*	X*	0	1	1	Y**	Y**	Y**

*X = Don't care. **Y = Value of Interrupt Level (1 through 7).

INTERRUPT VECTOR REGISTER (AT ADDRESS XX18 HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTERRUPT VECTOR							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

M3112/T4.4.9-2

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Register. The resulting location must contain a user-programmed four bytes of data. These four bytes of data reside in the exception vector table and point to the location of the Interrupt Service routine. The Interrupt Service routine reads in the data from the dual port registers and then returns to the main program.

4.4.10 External Trigger Operation

The board may be enabled to respond to an external TTL pulse (active low or "zero" pulse required) a single A/D conversion or a scan of A/D conversions will be initiated. First, the user selects the A/D mode to be used by writing to the CSR and selecting a RANDOM MODE or SCANNING MODE, but do not set the EN START CONV H bit (D13) in the CSR. The control bit ENA EXT STRT H (D11) must be set to a "one" instead. This will generate a TTL high (logic "one") out the P2 connector pin A31 to signal the external equipment that the board is ready to receive an External Trigger. An external logic level ("zero") trigger pulse of at least 100 ns may then be input to the board via the P2 connector pin A27. This will start the A/D conversion(s) depending on the A/D Mode which was previously selected.

In addition to enabling the External Trigger operation there are some jumpers which must be installed to electrically connect the P2 connector pins to the External Trigger circuitry. Refer to Section 5.4.4 on selecting these jumpers. Be aware that the P2 I/O pins are sometimes used by other boards to perform different I/O functions. This needs to be checked from a system viewpoint to verify there are not multiple drivers/receivers using these P2 I/O lines: P2-A31, A32, A27, and A28.

4.5 CHANGING A/D OPERATING MODES

The board powers up in the AUTO SCANNING MODE. To switch the board into any of the other A/D operating modes, a software reset sequence must be performed before reprogramming the new A/D operating mode. This sequence includes: (1) writing a control word setting the SOFTWARE RESET H (D9) bit and the new A/D Mode (D8 through D6), (2) writing a control word clearing the SOFTWARE RESET H (D9) bit and including the new A/D mode (D8 through D6), (3) next rewrite the A/D mode and set the EN START CONV H (D13) in the control word to start the A/D conversion sequence.

The above sequence is only necessary when switching to an operating mode other than the AUTO SCANNING MODE. Any other mode switch can be directly programmed by changing the mode bits (D8 through D6) in the Control Register.

Table 4.5-1 shows the proper sequence and control words to switch to the four other A/D operating modes.

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Table 4.5-1. Control Word Sequence for Switching from AUTO SCANNING MODE

SWITCH FROM AUTO SCANNING MODE TO:	CONTROL WORD SEQUENCE (HEX)
RANDOM POLL MODE	1. 4240 (RESET TIMING NETWORK) 2. 4040 (REMOVE RESET) 3. 6040 (STARTS CONV. ON CH 0)
RANDOM INT. MODE	1. 4280 (RESET TIMING NETWORKS) 2. 4080 (REMOVE RESET) 3. 6080 (START CONV. ON CH 0)
SCANNING POLL MODE	1. 42C0 (RESET TIMING NETWORKS) 2. 40C0 (REMOVE RESET) 3. 60C0 (STARTS A/D SCAN)
SCANNING INT. MODE	1. 4300 (RESET TIMING NETWORKS) 2. 4100 (REMOVE RESET) 3. 6100 (STARTS A/D SCAN)

M3112/T4.5-1

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4.6 PROGRAM EXAMPLE

The following programming example demonstrates how to program most of the A/D operating modes. Refer to the program outline for a description of each programming module.

```
        opt     P=68020
* this program was written for a 68020 or later processor
        org     $1000
*******************************************************************************
* program outline
*    I. Leave autoscan mode.
*   II. Initialize on-board timer for part IV.
*  III. SCANNING POLL MODE + EXTERNAL TRIGGER example
*       Set up a scan which is started by an external trigger.
*       The end will be determined by reading a 3112 status bit.
*   IV. SCANNING INTERRUPT MODE + ON-BOARD TIMER example
*       Set up a scan which is started by the on-board timer.
*       The end will be signaled by an interrupt.
*    V. RANDOM POLL MODE example
*       Do 64 conversions using the random access/poll mode.
*   VI. Put the board back in autoscan mode.
*  VII. End program.
* VIII. Interrupt handler
* The data from parts III, IV, and V are put in memory at $20000, $20080, $20100.

        lea.l   $FBFF0000,A0        3112 address (CPU board specific)
* I. Leave autoscan mode
        move.w  #$02C0,(2,A0)       put software reset + mode 3 in CSR
* II. Initialize on-board timer for part IV.
*If the timer was shut off abruptly (before output strobe returns high) it
* can prevent external trigger operation until the timer is re-initialized.
* The time the strobe takes is equal to the period of the second-to-last
* counter if 2 or 3 are cascaded. For the example here, it is 1 millisecond.
*This sets up the timer for a 1 second delay. Jumper J7-2 should be connected
* to J8-2 by a shunt. The rest of J7 and J8 should not have shunts. The timer
* is an Intel 8254.
            move.w      #$0034,($26,A0)    set counter 0 to rate gen, load 2 bytes
            move.w      #$0040,($20,A0)  load with 8000.= $1F40 = 1ms:LSB first!
            move.w      #$001F,($20,A0)  load 1ms constant: MSB second!
            move.w      #$0078,($26,A0)  set counter 1 to 'software trig. strobe'
            move.w      #$00E8,($22,A0)  load with $03E8 = 1000ms LSB first!
            move.w      #$0003,($22,A0)  load with $03E8 = 1000ms MSB second!
```

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```
* III. Set up a scan which is started by an external trigger. The end will
*  be determined by reading a 3112 status bit (SCANNING POLL MODE).
* An easy way to trigger this is to briefly short one pin of jumper J10 to
* on board ground (the - leg of the 47uF capacit or next to J10). You can short
* both pins of J10 if you are not using the VMEbus User-Defined Pin P2-A27.
            move.w      #$08C0,(2,A0)     put mode 3 (no reset) X-trig in CSR
*           move.w      #$40C0,(2,A0)     use these two lines instead of the one
*           move.w      #$60C0,(2,A0)     above to start a scan without X.trigger.

clrwait     btst.b      #5,(2,A0)           these two lines wait for the external...
            bne.s       clrwait             ...trigger to clear the flag (if set)
scanwait    btst.b      #5,(2,A0)           read scan done H flag
            beq.s       scanwait            repeat until flag is set
* now read the data
            lea.l       $20000,A1           pointer to conversion data buffer
            lea.l       ($80,A0),A2         pointer to scan data on-board 3112
            moveq.l     #63,D0              initialize data transfer loop
getdata1 move.w         (A2)+,(A1)+         get data from scan
            dbf         D0,getdata1         loop

* IV. Set up a scan which is started by the on-board timer.
*  The end will be signaled by an interrupt (SCANNING INTERRUPT MODE).

*set up the 68153 on-board the 3112. This example enables the interrupt once.
            move.w      #$0099,($18,A0)   set BIM channel 0 vector to $99
            move.w      #$001D,($10,A0)   enable BIM channel 0, int level 5

*set up the 68020 CPU to accept level 5 (or any other) interrupts, and to
* route interrupt vector $99 to this program.
            andi.w      #$F8FF,SR         set CPU interrupt mask to 0
            movec       VBR,A3            load vector base register
            adda.w      #$264,A3          point to vector $99.  $99 x 4 = $264
            lea.l       ihandler,A4       address of example interrupt handler
            move.l      A4,(A3)           insert address in table

*start 3112
            clr.w       D1                D1.W=0: no int yet else D1.B=i.vector
            move.w      #$0500,(2,A0)     enable 3112 timer/scan/interrupt
waitint     tst.w       D1                check flag: 0 = keep waiting
            beq.s       waitint           repeat until interrupt

* V. Do some conversions using the RANDOM (access) POLL MODE.
            move.w      #$2040,D0         initialize 3112 control word
raccess     move.w      D0,(2,A0)         write control word
waitracp    btst.b      #7,(2,A0)         Z set = conversion not done yet
            beq.s       waitracp          repeat until Z clear
            move.w      ($30,A0),(A1)+    read data into buffer just after scans
```

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```
            add.w       #1,D0           change control word to next channel
            cmp.w       #$2080,D0       $207F is last channel control word
            bne.s       raccess         loop: convert next channel

* VI. Put the board back in AUTOSCAN MODE.
            move.w      #$0000,(2,A0)   autoscan=just read conversions
* VII. End program. This particular code is for 'Forcebug'
            dc.w        $A002           END - return control to debugger

* VIII. Interrupt handler
* the following is the interrupt handler for part IV.
*read data, and store it next to the other set of scan data
ihandler    lea.l       ($80,A0),A2     pointer to scan data on-board 3112
            moveq.l     #63,D0          initialize data transfer loop
getdata2    move.w      (A2)+,(A1)+     get data from scan
            dbf         D0,getdata2     loop
            move.w      (6,A7),D1       read format+vec-ofs from exception frame
            lsr.w       #2,D1           offset divided by four = vector in D1.B
            rte
            END
```

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board (s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

a. Have the sections pertaining to theory and programming, Sections 3 and 4, been reviewed and applied to system requirements?

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b. Review Section 5.4.1 and Table 5.3-1 to verify that all factory-installed jumpers are in place. To change the board address or address modifier response, refer to Section 5.4.2.

c. Have the input cables, with the proper mating connectors, been connected to the input connectors P3 and P4? Refer to Section 5.6 for a description of the connector.

d. Calibration has been performed at the factory. If recalibration should be required, refer to Section 5.5.2.

e. Ground unused inputs (both high side and low side) to VMEbus ground.

CAUTION

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.4 OPERATIONAL CONFIGURATION

Control of the VMIVME-3112 Board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all VMIVME-3112 jumpers are shown in Figure 5.4-1 and Table 5.3-1.

5.4.1 Factory Installed Jumpers

Each VMIVME-3112 Board is configured at the factory with the specific jumper arrangement shown in Table 5.3-1. The factory configuration establishes the following functional baseline for the VMIVME-3112 Board, and ensures that all essential jumpers are installed.

a. Board short address is set at 0000 HEX
b. I/O access mode is short supervisory access
c. Analog input range is set to ±10 V full scale range
d. The number of channels for an A/D Scan is set to 64
e. The gain amplifier is set to a gain of "one"

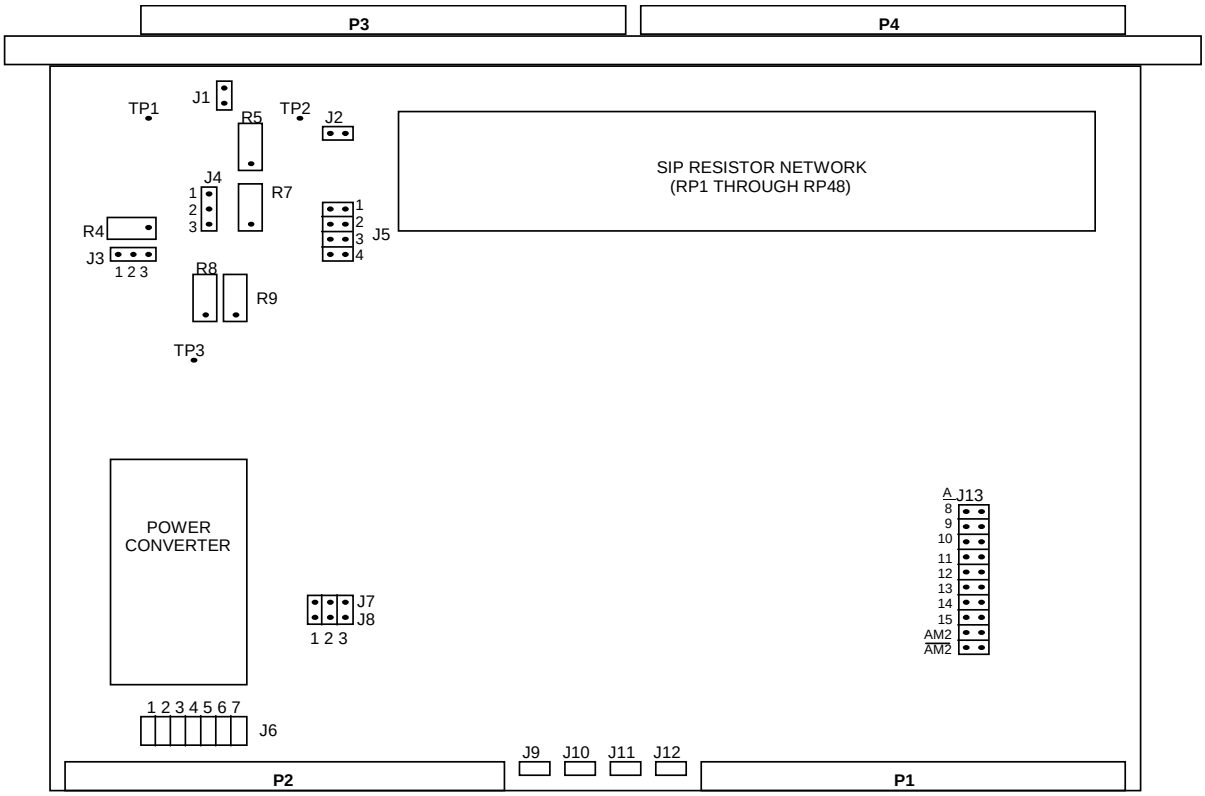
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Table 5.3-1. Programmable Jumper Functions

JUMPER IDENTITY	FUNCTION (INSTALLED)	FACTORY CONFIGURED
J13-8	BOARD ADDRESS BIT A08 = 0	INSTALLED
J13-9	BOARD ADDRESS BIT A09 = 0	INSTALLED
J13-10	BOARD ADDRESS BIT A10 = 0	INSTALLED
J13-11	BOARD ADDRESS BIT A11 = 0	INSTALLED
J13-12	BOARD ADDRESS BIT A12 = 0	INSTALLED
J13-13	BOARD ADDRESS BIT A13 = 0	INSTALLED
J13-14	BOARD ADDRESS BIT A14 = 0	INSTALLED
J13-15	BOARD ADDRESS BIT A15 = 0	INSTALLED
J13-AM2	SHORT SUPERVISORY OR NONPRIVILEGED ACCESS	INSTALLED
J13-~~AM2~~	SHORT NONPRIVILEGED ACCESS	OMITTED
J13-AM2 + ~~AM2~~	OMIT BOTH JUMPERS FOR SHORT SUPERVISORY ACCESS ONLY	OMITTED
J12	STATUS SIGNAL FOR EXTERNAL TRIGGER INPUT (P2 OUTPUT)	OMITTED
J11	GROUND CONNECTION FOR ABOVE SIGNAL (P2 OUTPUT)	OMITTED
J10	ENABLE EXTERNAL TRIGGER INPUT (P2 INPUT)	OMITTED
J9	GROUND CONNECTION FOR ABOVE SIGNAL (P2 INPUT)	OMITTED
J7-3 TO J8-3	ENABLES CTR0 TO START A/D CONVERSION CIRCUITRY (16-BIT CTR)	OMITTED
J7-2 TO J8-2	CASCADES CTR0 TO CTR1 (32-BIT CTR)	INSTALLED
J7-1 TO J8-1	CASCADES CTR1 TO CTR2 (48-BIT CTR)	OMITTED
J6-1 TO J6-7	THESE 7 JUMPERS SELECT THE NUMBER OF CHANNELS TO BE CONVERTED IN AN A/D SCAN	J6-7 THROUGH J6-2 INSTALLED-SETS THE SCAN LENGTH TO 64 CHANNELS
J1	CONNECTS P3-C1 AS THE GROUND REFERENCE CONNECTION FOR ALL 64 CHANNELS (PSEUDO-DIFFERENTIAL INPUTS)	OMITTED
J2	CONNECTS THE ON-BOARD GND AS THE GROUND REFERENCE CONNECTION FOR ALL 64 CHANNELS (SINGLE-ENDED INPUT)	OMITTED
J5-1	SETS THE PROGRAMMABLE GAIN AMPLIFIER TO A GAIN OF 10	OMITTED
J5-2	SETS THE PROGRAMMABLE GAIN AMPLIFIER TO A GAIN OF 100	OMITTED
J5-3	SETS THE PROGRAMMABLE GAIN AMPLIFIER TO A GAIN OF 200	OMITTED
J5-4	SETS THE PROGRAMMABLE GAIN AMPLIFIER TO A GAIN OF 500	OMITTED
J4-2, J4-3	INPUTS, 20 V FULL SCALE RANGE	INSTALLED
J4-1, J4-2	INPUTS, 10 V FULL SCALE RANGE	OMITTED
J3-1, J3-2	INPUTS, BIPOLAR OPERATION	INSTALLED
J3-2, J3-3	INPUTS, UNIPOLAR OPERATION	OMITTED

M3112/T5.3-1

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M3112/F5.4-1

Figure 5.4-1. Programmable Jumper Test Points and Resistor Network Locations

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5.4.2 Board Address and Address Modifier Selection

Jumper header J13 permits the VMIVME-3112 Board to be located on any 256-byte boundary within the short I/O address space. The short I/O address space consists of all addresses between NNNN0000 HEX* and NNNNFFFF HEX, and requires that 15 (word) address lines be decoded in order to account for all

*The value NNNN depends on the make and model of CPU board used.

Table 5.4.2-1. Board Address Selection Example (NNNN85XX)*

JUMPER	ADDRESS BIT	STATE**
J13-8	A08	OPEN
J13-9	A09	SHORTED
J13-10	A10	OPEN
J13-11	A11	SHORTED
J13-12	A12	SHORTED
J13-13	A13	SHORTED
J13-14	A14	SHORTED
J13-15	A15	OPEN
AM2	ADDRESS MODIFIER BIT 2***	OPEN
$\overline{AM2}$		SHORTED

M3112/T5.4.2-1

*(NNNN) HEX is CPU board dependent. (85) HEX is address bits A15 through A08 as shown. (XX) HEX selects on-board registers (see Table 4.1-1).

**Shorted = "zero" (jumper installed)
Open = "one" (jumper not installed) (see Table 5.3-1).

***AM2 + $\overline{AM2}$ select short supervisory access, short nonprivileged access, or both (the example shown is for short nonprivileged access).

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locations. Since seven lines are used for decoding on-board functions (Section 4), the VMIVME-3112 Board address is defined by eight lines, address bits A08 through A15.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit jumper positions, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A06 has a weight of 64 byte-locations. As an example, the jumper arrangement shown in Table 5.4.2-1 would produce a board address of NNNN85XX HEX.*

The I/O access mode is programmed by proper selection of jumpers AM2 bar (AM2 with a line over it) and AM2. To select short nonprivileged access install jumper AM2 bar (AM2 with a line over it). To select short supervisory access omit both jumpers. The installation of jumper AM2 allows the board to respond to either type of access.

5.4.3 Analog Input Modes

5.4.3.1 Differential or Single-Ended Operation

The VMIVME-3112 Board is shipped with the analog inputs configured for differential operation. The analog input mode is controlled by the positions of 32-resistor SIPs within 48 sockets (labeled RP1 through RP 48). If the VMIVME-3112 is held with the component side up and the front panel facing left, then the SIP sockets form six columns. The two left-most columns should always have SIPs installed. The two middle columns should have SIPs installed to configure differential inputs. The two right-most columns should have SIPs installed to configure single-ended inputs. The SIPs are symmetrical. It will not hurt to install them backwards.

In the single-ended mode, the external field ground sense input can be used to compensate for the potential differences between equipment signal returns. If the J1 jumper is installed, pin C1 of the input connector P3 serves as a ground sense for all single-ended inputs. There is a 40.2 K resistor on board the VMIVME-3112 which will tend to pull this ground sense to VME bus digital ground. If the J2 jumper is installed (instead of J1) then the single-ended inputs will operate relative to VME bus digital ground (which may be quite noisy). It is recommended that the board be used in the differential input mode.

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NOTE ON INPUT VOLTAGE:

FOR PROPER OPERATION, THE VOLTAGE ON ANY INPUT PIN MAY NOT EXCEED (+) OR (-) 12 V RELATIVE TO THE VMEbus GROUND.

AN ISOLATED INPUT SOURCE WILL HAVE AN INDETERMINATE COMMON MODE VOLTAGE RELATIVE TO VMEbus GROUND. IN SUCH CASES IT MAY BE NECESSARY TO PROVIDE SIGNAL SOURCES WITH THE VME GROUND REFERENCE.

IN DIFFERENTIAL MODE THERE IS NORMALLY NO GROUND REFERENCE AVAILABLE ON P3 OR P4 OF THE VMIVME-3112. VME GROUND IS AVAILABLE ON THE VME BACKPLANE. AN ALTERNATE METHOD OF OBTAINING A GROUND REFERENCE IS TO INSTALL JUMPERS J1 AND J2. WITH J1 AND J2 INSTALLED, INPUT CHANNEL 0 WOULD NOT BE USABLE AS A DIFFERENTIAL INPUT BUT, PIN C1 ON P3 WOULD BE CONNECTED TO VMEbus GROUND. CHANNEL 0 MAY STILL BE USED AS A SINGLE-ENDED INPUT. CURRENT THROUGH PIN C1 ON P3 SHOULD NOT EXCEED 750 mA CONTINUOUS.

If the Improved High Frequency Rejection option is ordered, J2 is installed and should NOT be removed. All of the RFILT input SIPs will be occupied with SIP headers. These are SIP resistors of 0 Ω. J1 may be installed but it is not necessary. These SIPs supply the input source with the VME ground reference. Isolated input sources, such as the 3V/5V input modules, require this configuration to prevent high frequency noise from becoming a common mode signal and causing fluctuations in the output data.

5.4.3.2 Input Voltage Range

Input voltage range is controlled by jumpers J4-1, 2, 3. The maximum full scale range is 20 V. To modify the full scale range to 10 V configure the jumpers as indicated in Table 5.3-1. All input voltages must be within 12 V of VMEbus ground for linear operation. For gains other than "one", all input voltages must be within 10 V of VMEbus ground. For single-ended operation, the ground sense counts as an input.

5.4.3.3 Bipolar or Unipolar Operation

Bipolar or unipolar operation of the analog inputs is selected with jumpers J3-1, 2, 3 as indicated in Table 5.3-1.

5.4.4 External Trigger Jumper Description

The external trigger circuitry allows the user to input a TTL level "zero" to start an A/D conversion or an A/D conversion scan sequence. This input must be enabled to the PC connector by installing jumpers J9 and J10. J9 allows a ground reference connection. J10 enables the trigger signal and is labeled EXT STRT CONVERT L on the schematic (SH6). In addition to the jumper, the ENA EXT STRT H (D11) must be set in the control register. This signal is also brought out to the user via the P2 connector. External circuitry can monitor this TTL signal, and when

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it goes High to a logic "one" then the board is ready for the EXT STRT CONVERT L input to begin a conversion(s). Table 5.4.4-1 gives the connector description for the External Trigger signal.

Table 5.4.4-1. External Trigger Connections

SIGNAL	FUNCTION	JUMPER	CONNECTOR
EXT STRT CONVT L	EXTERNAL TRIGGER INPUT	J10	P2-A27
GND	BOARD GROUND REF	J9	P2-A28
ENA EXT STRT H	CONTROL REGISTER ENABLE OUTPUT	J12	P2-A31
GND	BOARD GROUND REF	J11	P2-A32

M3112/T5.4.4-1

Table 5.4.5-1. Internal Timer Jumper Configurations

COUNTER LENGTH	INSTALL JUMPER	TIME DELAY RANGE
16 BITS	J7-3 to J8-3	0 to 8.192 ms
32 BITS	J7-2 to J8-2	8.192 ms to 536 sec.
48 BITS	J7-1 to J8-1	536 sec to 9773 hours

M3112/T5.4.5-1

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5.4.5 Internal Timer - 16-, 32-, or 48-Bit Timer Selection

The internal timer (8254) has three 16-bit counters. These three timers may be jumpered in a way to generate a maximum count length of 16, 32, or 48 bits (refer to Section 4.4.6 to determine counter resolution and programming). Table 5.4.5-1 shows the possible jumper configurations.

5.4.6 A/D Scan Sequence Length Jumper Configuration

The three scanning modes (AUTO SCANNING MODE, SCANNING POLL MODE, SCANNING INTERRUPT MODE) use the jumpers at J6 to determine how many channels to scan. Scans always begin with Channel 0 and continue with the next higher channel until J6 matches the total number of channels scanned. For example, the factory setting does all 64 channels (0 through 63) by encoding 64 in J6. J6-1 is the most significant bit. J6-7 is the least significant bit. J6-1, J6-2, J6-3, J6-4, J6-5, J6-6, J6-7 have weights of 64, 32, 16, 8, 4, 2, and 1 channels, respectively. An installed jumper signifies a "zero". Table 5.4.6-1 gives some examples of the jumpers to be installed for different scan lengths. See Section 3.6.1 for restrictions on jumper settings.

5.4.7 Programmable Gain Jumper Configuration

The Gain Amplifier may be configured for gains of 1, 10, 100, 200, and 500 to handle signal levels as low as ±10 mV. Table 5.4.7-1 shows which jumper is to be installed. The board is factory configured for a gain of "one" (no jumper installed).

5.5 CALIBRATION

Before delivery from the factory, the VMIVME-3112 Board is fully calibrated and conforms to all specifications listed in Section 2. Should recalibration be required, however, perform the procedures in Sections 5.5.2 and 5.5.3 with the equipment listed in Section 5.5.1. The locations of all adjustments and test points are shown in Figure 5.4-1.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however. All adjustments should be resealed with a suitable fact curing sealing compound after recalibration has been completed.

CAUTION

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

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Table 5.4.6-1. A/D Scan Length (Jumper) Example

NUMBER OF CHANNELS TO BE SCANNED	INSTALL ALL J6 JUMPERS EXCEPT
16	J6-3
20	J6-3, J6-5
32	J6-2
37	J6-2, J6-5, J6-7
45	J6-2, J6-4, J6-5, J6-7
61	REMOVE ALL BUT J6-6
64	J6-1

M3112/T5.4.6-1

Table 5.4.7-1. Programmable Gain Jumper Configurations

GAIN (X)	INSTALL JUMPER
1	NONE
10	J5-1
100	J5-2
200	J5-3
500	J5-4

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5.5.1 Equipment Required

a. Digital Voltmeter (DVM). ±1.0000 VDC and ±10.000 VDC ranges; 5 or more digits; ±0.005 percent of reading voltage measurement accuracy; 10 MΩ minimum input impedance.

b. Analog Voltage Source. ±10.000 VDC Range; resolution 0.0005 VDC; Accuracy, ±0.005 percent of expected value; 0.10 Ω maximum output impedance.

c. Chassis. VMEbus backplane or equivalent, J1 and J2 connectors, VMEbus master controller, +5 ±0.1 VDC, power supply. One slot allocated for testing the VMIVME-3112 Board.

d. Extender Board. VMEbus extender board.

e. Test Cables. Test cables for the equipment listed above.

5.5.2 Analog Inputs Calibration Procedure

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), next adjusting the most positive output to its ideal value (Gain Adjustment). The calibration must be performed when changing the A/D's input full scale range from one value to another (for example, from ±10 V to ±5 V). The procedure is as follows:

a. Install the VMIVME-3112 Board on an extender board in a VMEbus backplane.
b. Configure the analog inputs to the desired voltage range (i.e. ±10 V, ±5 V, 0 to +10 V).
c. Apply power to the backplane. Allow a minimum warm up interval of ten minutes after power has been applied before proceeding.
d. Connect the analog voltage source at CH0, between connector pins P3-A1 (+) and P3-C1 (-).
e. Adjust the analog voltage source for the most negative calibration value of the full scale range selected. Refer to Table 5.5.2-1.
f. While reading CH0 adjust R4 for unipolar ranges or R8 for bipolar angles. CH0 address is XXXX0080. Continue adjusting the potentiometer until the value read flickers between 000 HEX and 001 HEX.
g. Adjust the analog voltage source for the most positive calibration value of the full scale range selected. Refer to Table 5.5.2-1.
h. While reading CH0 adjust R9 until the value read flickers between FFE and FFF HEX.
i. Calibration is now complete. Remove all test connections, and restore the board to its original configuration.

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Table 5.5.2-1. Calibration Data Table

VOLTAGE RANGE	OFFSET ADJUSTMENT POTENTIOMETER	GAIN ADJUSTMENT POTENTIOMETER	NEGATIVE CALIBRATION VOLTAGE	POSITIVE CALIBRATION VOLTAGE
-5 V TO +5 V	R8	R9	-4.9988 V	+4.9963 V
-10 V TO +10 V	R8	R9	-9.9976 V	+9.9927 V
0 TO +10 V	R4	R9	+1.22 mV	+9.9963 V

M3112/T5.5.2-1

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5.6 CONNECTOR DESCRIPTIONS

Two connectors, P1 and P2, connect the VMIVME-3112 Board to the VMEbus backplane. The connectors are 96-pin DIN type. The primary connector, P1, contains the address data and control lines and all additional signals necessary to control data transfer and other bus functions. The VMIVME-3112 Board uses four of the user I/O pins to allow an external trigger input and a status output. The P2 connector pin and signal assignments are shown in Figure 5.6-1 and Table 5.6-1.

The P3 and P4 connectors are Panduit 64-pin male connectors, type 120-964-033A. The matching Panduit connector for the input cable is a female connector, type 120-964-435E. This connector supports the 32 single-ended or 32 differential analog inputs each with an associated analog ground pin. For P3 connector pin and signal assignments, refer to Figure 5.6-2 and Table 5.6-2. For P4 connector pin and signal assignments, refer to Figure 5.6-2 and Table 5.6-3.

The P3 and P4 connectors have an "A" row (A1 through A32) and a "C" row (C1 through C32). All "A" row pins are the high side of the input signal. All "C" row pins are the low side of the input signal. The preferred method of connecting analog input signals is to connect both high and low inputs for each channel (differential). Differential inputs provide for very high common mode noise rejection by rejecting differences in ground potential between the analog transmitter and the VMIVME-3112 Board. The board is factory configured to accept differential inputs.

A second method of connecting analog inputs is called pseudo-differential. In this connection scheme only one ground reference is brought to the board and connected to the P3 connector at pin C1. This implies that all connected channels from the field must be referenced to the same ground. This method has some of the advantages of differential inputs in that it helps reject ground differences, but is not as good in common mode noise rejection. Jumper J1 must be installed to enable this mode. In addition, the SIP resistors on the inputs must be in the single-ended position as described in Section 5.4.3.1.

A third method of connecting analog inputs is single-ended inputs. This method uses the on-board analog ground as the input signal reference. This is generally the least accurate of the three methods. However, in a low noise environment and when short cabling is used this method will work well. The input sip resistors must be moved from the differential to single-ended sockets (refer to 5.4.3.1) and jumper J2 must be installed.

A Connector and I/O Cable Applications Guide (VMIC Document No. 825-000000-006) is available from VMIC that provides additional information concerning field connections, the use of round cables, and a thorough explanation of compatible connectors and cabling techniques.

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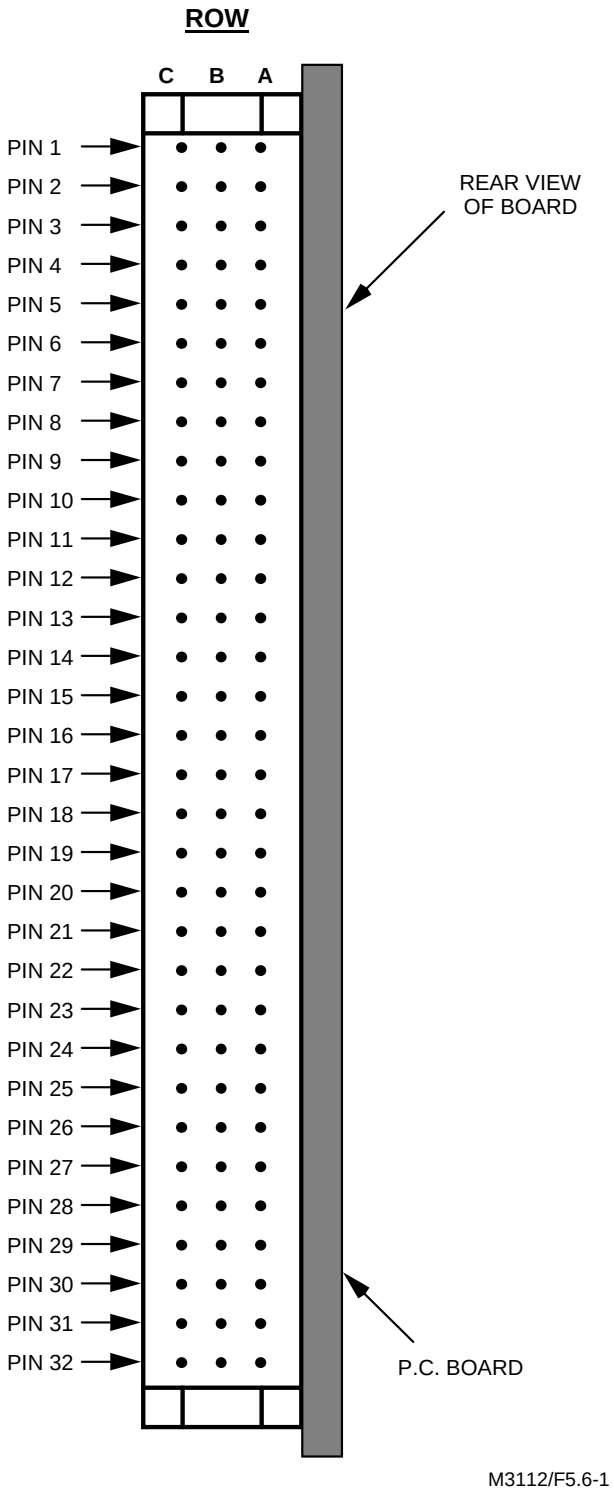


Figure 5.6-1. P2 Connector Pin Configuration

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Table 5.6-1. P2 Connector Signal Assignments

	ROW A	ROW B
PIN NUMBER	**SIGNAL MNENOMIC**	**SIGNAL MNENOMIC**
1		+5 V
2		GND
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		+5 V
14		GND
15		
16		
17		
18		
19		
20		
21		
22		
23		GND
24		
25		
26		
27	EXT STRT CONVERT L (IN)	
28	GND	
29		
30		
31	ENA EXT START H (OUT)	
32	GND	
		GND
		+5 V

M3112/T5.6-1

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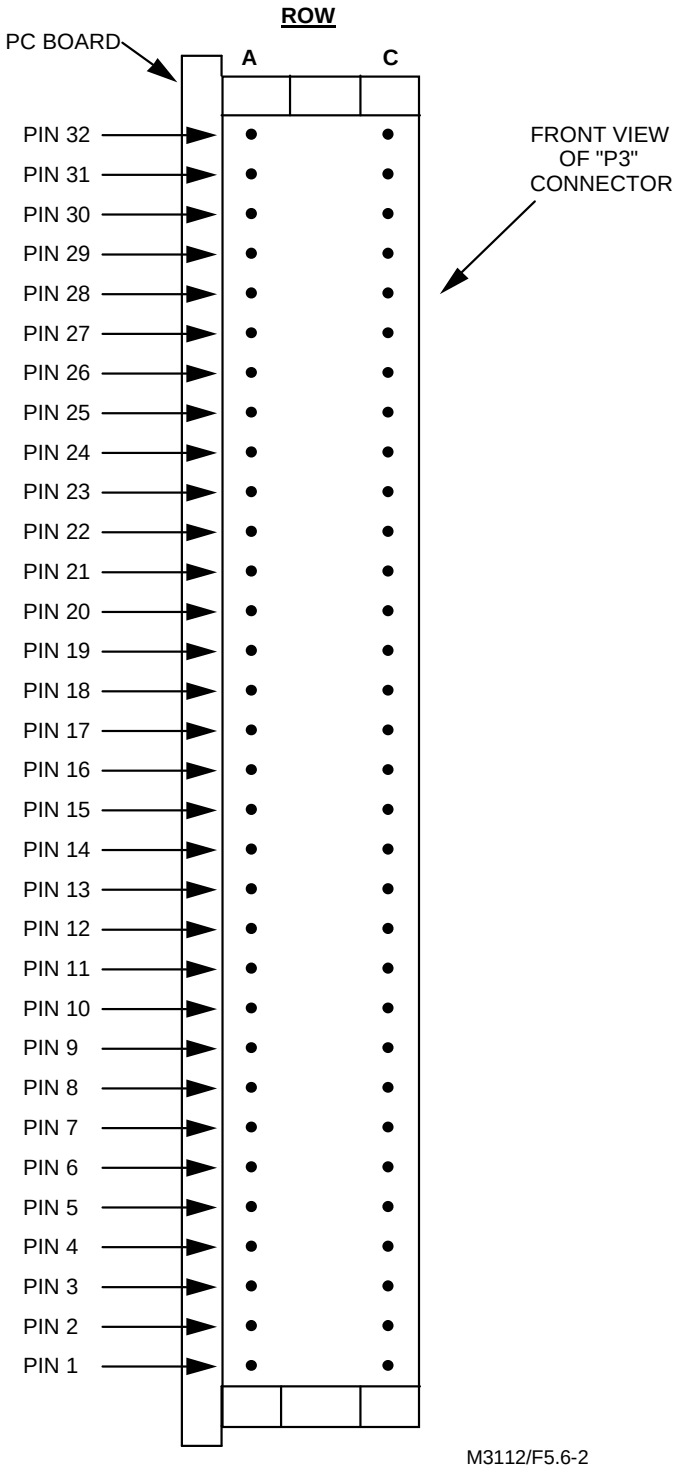


Figure 5.6-2. P3 and P4 Connector Pin Configuration

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Table 5.6-2. P3 Connector (Front Panel Inputs) Signal Assignments

PIN NO.	SIGNAL NAME	
	ROW A SIGNAL	ROW C SIGNAL
1	CH00 - HI	CH00 - LO*
2	CH01 - HI	CH01 - LO
3	CH02 - HI	CH02 - LO
4	CH03 - HI	CH03 - LO
5	CH04 - HI	CH04 - LO
6	CH05 - HI	CH05 - LO
7	CH06 - HI	CH06 - LO
8	CH07 - HI	CH07 - LO
9	CH08 - HI	CH08 - LO
10	CH09 - HI	CH09 - LO
11	CH10 - HI	CH10 - LO
12	CH11 - HI	CH11 - LO
13	CH12 - HI	CH12 - LO
14	CH13 - HI	CH13 - LO
15	CH14 - HI	CH14 - LO
16	CH15 - HI	CH15 - LO
17	CH16 - HI	CH16 - LO
18	CH17 - HI	CH17 - LO
19	CH18 - HI	CH18 - LO
20	CH19 - HI	CH19 - LO
21	CH20 - HI	CH20 - LO
22	CH21 - HI	CH21 - LO
23	CH22 - HI	CH22 - LO
24	CH23 - HI	CH23 - LO
25	CH24 - HI	CH24 - LO
26	CH25 - HI	CH25 - LO
27	CH26 - HI	CH26 - LO
28	CH27 - HI	CH27 - LO
29	CH28 - HI	CH28 - LO
30	CH29 - HI	CH29 - LO
31	CH30 - HI	CH30 - LO
32	CH31 - HI	CH31 - LO

M3112/T5.6-2

*For pseudo-differential input P3-C1 is the Low side (GND) reference for all 64 input channels. Refer to Section 5.6 for pseudo-differential input description.

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Table 5.6-3. P4 Connector (Front Panel Inputs) Signal Assignments

PIN NO.	SIGNAL NAME	
	ROW A SIGNAL	ROW C SIGNAL
1	CH32 - HI	CH32 - LO
2	CH33 - HI	CH33 - LO
3	CH34 - HI	CH34 - LO
4	CH35 - HI	CH35 - LO
5	CH36 - HI	CH36 - LO
6	CH37 - HI	CH37 - LO
7	CH38 - HI	CH38 - LO
8	CH39 - HI	CH39 - LO
9	CH40 - HI	CH40 - LO
10	CH41 - HI	CH41 - LO
11	CH42 - HI	CH42 - LO
12	CH43 - HI	CH43 - LO
13	CH44 - HI	CH44 - LO
14	CH45 - HI	CH45 - LO
15	CH46 - HI	CH46 - LO
16	CH47 - HI	CH47 - LO
17	CH48 - HI	CH48 - LO
18	CH49 - HI	CH49 - LO
19	CH50 - HI	CH50 - LO
20	CH51 - HI	CH51 - LO
21	CH52 - HI	CH52 - LO
22	CH53 - HI	CH53 - LO
23	CH54 - HI	CH54 - LO
24	CH55 - HI	CH55 - LO
25	CH56 - HI	CH56 - LO
26	CH57 - HI	CH57 - LO
27	CH58 - HI	CH58 - LO
28	CH59 - HI	CH59 - LO
29	CH60 - HI	CH60 - LO
30	CH61 - HI	CH61 - LO
31	CH62 - HI	CH62 - LO
32	CH63 - HI	CH63 - LO

M3112/T5.6-3

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SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The

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defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, over temperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

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6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

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