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VMIVME-3113A

Scanning 12-bit Analog-to-Digital Converter Board with Built-In-Test

Product Manual

A GE Fanuc Company

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500-103113-000 Rev. H

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Overview

Introduction

The VMIVME-3113A 64-Channel Scanning, 12-bit Analog-to-Digital Converter (ADC) is one of the highest density / lowest cost per channel boards in the industry. In addition, it contains many features found only on more expensive products. The AUTOSCANNING MODE, which is automatically entered on power up, performs Analog-to-Digital (A / D) conversions on all inputs and stores them in a dedicated channel dual-port register. This allows the user to operate the board without any programming. The user simply reads the data from the dual-port registers which always contain the latest converted data for that particular channel. There are five other ADC operating modes which allow greater flexibility in controlling the ADC operation.

The VMIVME-3113A Board is useful for many applications which require a large number of differential inputs to be converted to digital form. Overvoltage protected inputs, input filters, programmable timers and jumper-programmable gain features lend the board to such applications as factory automation and instrumentation, process control, laboratory instrumentation and general data acquisition systems. A Built-in-Test (BIT) mode permits verification of the input multiplexer and A / D converter.

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Features

The following brief overview of principal features illustrates the flexibility and performance that is available with the VMIVME-3113A Board:

- 64 differential or single-ended inputs
- Powers up in AUTOSCANNING MODE - no software initialization required
- Continually digitizes all input channels and stores the results in a dedicated channel dual-port register (AUTOSCANNING MODE)
- Six operating modes
  - — AUTOSCANNING MODE *
  - — RANDOM POLL MODE
  - — RANDOM INTERRUPT MODE
  - — SCANNING POLL MODE
  - — SCANNING INTERRUPT MODE
  - — AUTOSCANNING MODE with BIT

  * Only for gain = 1 and a minimum of 16 channels.
- VMEbus interrupts may be programmed to interrupt upon completion of a single A / D conversion, or upon completion of a 16 through 64-channel scan (see “Analog-to-Digital (ADC) Control and Timing” on page 26)
- User-programmable interval timer supports scanning of all channels at periodic intervals
- Jumper-programmable gains of 1, 10, 100, 200 and 500
- Selectable A / D ranges of 0 to +10V, ±5V and ±10V
- Low-level and high-level inputs: ±10mV to ±10V
- Optional low pass filter
- Overvoltage protected inputs
- 5 x $10^6\Omega$ input impedance differential and $2x10^6\Omega$ input impedance single-ended
- 33 kHz conversion rate at GAIN<500 (23kHz for GAIN = 500)
- Selectable output code: binary, offset binary, two's complement with sign extension
- Front panel Fail LED is under program control and may be used for any purpose
- Board ID register

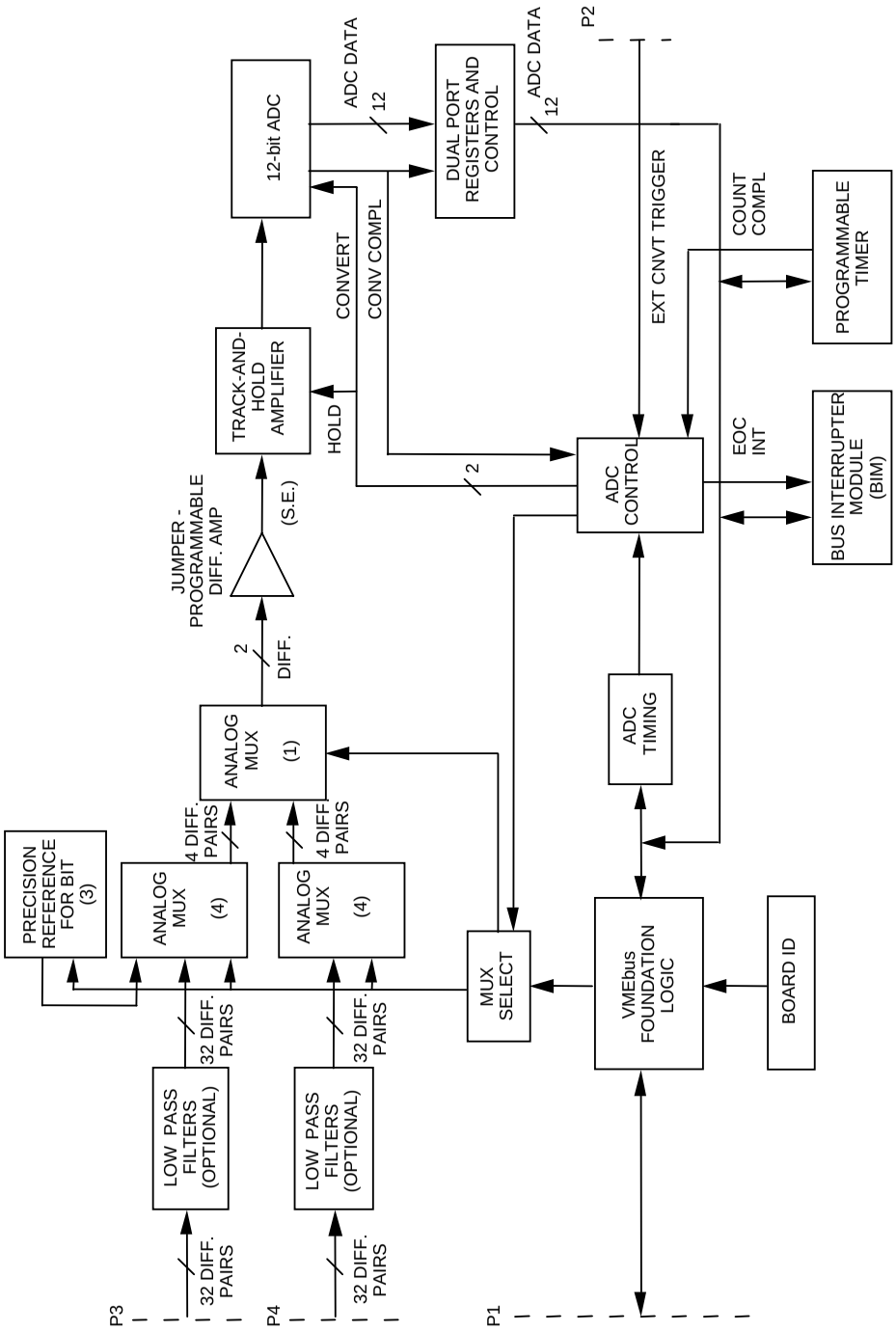
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Functional Block Diagram

A block diagram of the VMIVME-3113A Board is shown in Figure 1 on page 16 which illustrates the board's components and their functions. Not shown on the block diagram is a DC-to-DC converter which provides the analog power supplies (±15V). The user has only to supply +5V to the board.

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Figure 1 VMIVME-3113A Functional Block Diagram



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References

For a detailed description and specification of the VMEbus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook
VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

The following application and configuration guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products.

Digital Input Board Application Guide (Document No. 825-000000-000)

Change-of-State Application Guide (Document No. 825-000000-002)

Digital I/O (with Built-in-Test) Product Line Description (Document No. 825-000000-003)

Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide (Document No. 825-000000-004)

Analog I/O Products (with Built-in-Test) Configuration Guide (Document No. 825-000000-005)

Connector and I/O Cable Application Guide (Document No. 825-000000-006)

Physical Description and Specification

Refer to VMIC's Specification No. 800-103113-000 for detailed specifications.

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

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CHAPTER 1

Theory of Operation

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Introduction

The VMIVME-3113A is a 64-Channel, 12-bit Analog Input Board with program-controlled Built-in-Test (BIT). The board has many built-in features, resulting in a board that is capable of handling many data acquisition problems. For example, the AUTOSCANNING MODE on power up allows for ease of programming. In AUTOSCANNING MODE each channel is continually digitized and stored in a dual-port register. Any channel may be read at any time to get the latest data. The VMIVME-3113A is a flexible, low-cost analog input board with features not found in many competing products. These features are discussed in this section.

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Internal Functional Organization

The VMIVME-3113A is divided into the following functional categories, as illustrated in Figure 1-1 on page 24. All VMIVME-3113A functions are discussed in detail in this section.

- VMEbus Interface
- Analog-to-Digital Converter (ADC) and Control Logic
- Analog Input Filters and Multiplexer
- Programmable Timer
- Bus Interrupter
- Board ID Register

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VMEbus Control Interface

The VMIVME-3113A communication registers are memory mapped as 128 (decimal), 16-bit words. The registers are contiguous and may be user-located on any 256-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to short supervisory or short nonprivileged data accesses, or both.

During each read or write operation, all VMEbus control signals are ignored unless the board-selection comparator detects a match between the on-board selection jumpers shown in Figure 1-2 on page 25 and the address and address modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted (driven LOW). Subsequent completion of the bus master's read or write cycle causes the board-generated DTACK signal to return to the OFF state.

After board-selection has occurred, three groups of VMEbus signals control communications with the board. They are as follows:

1. Data Bus lines D00 to D15
2. Address lines A01, A02, A03, A04, A05, A06, A07
3. Bus Control Signals:
    a. WRITE
    b. DS0,* DS1*
    c. SYS CLK
    d. SYS RESET*

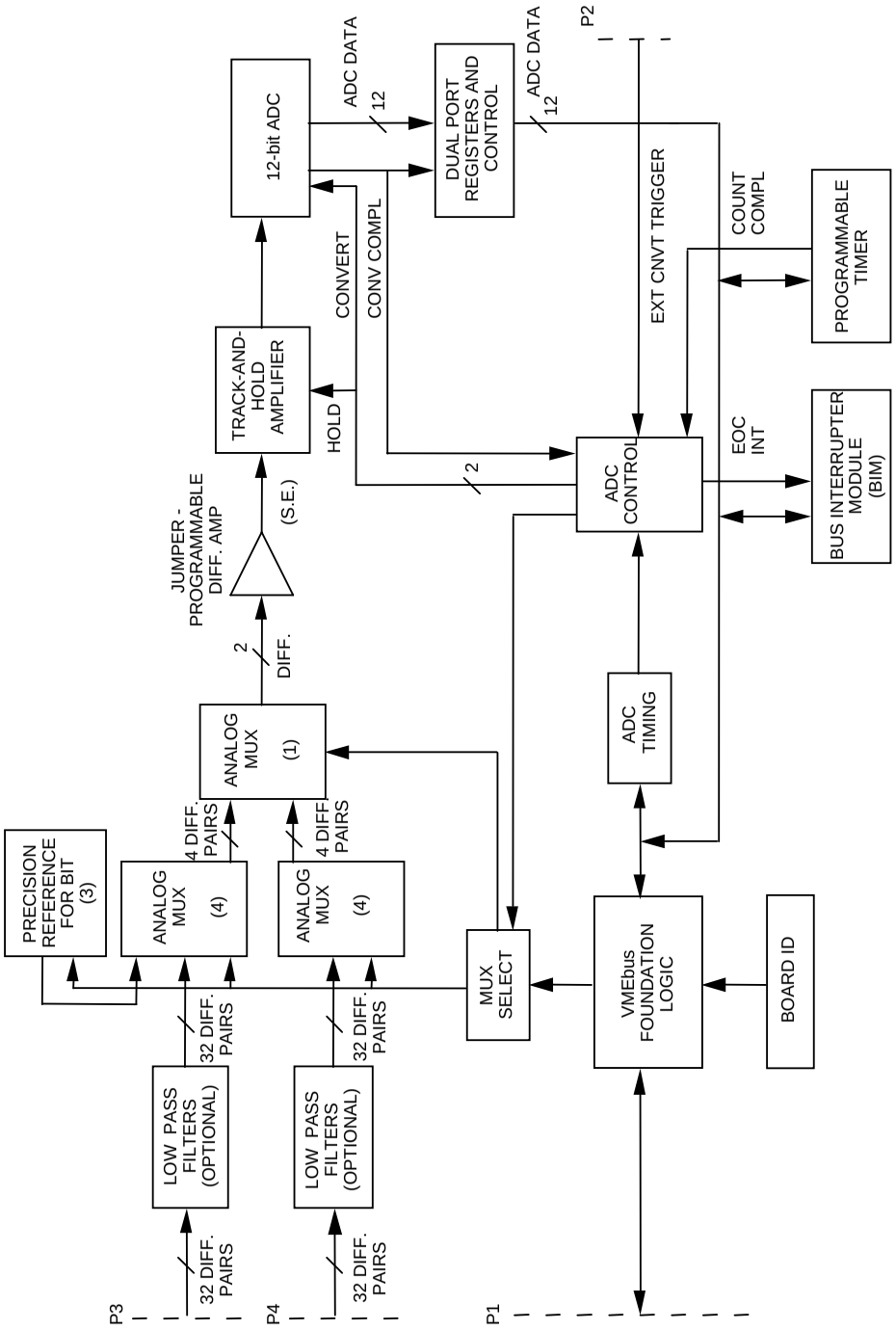
Data bus lines are bi-directional and move data to and from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A07 map the 128 registers onto a 256-byte range within the VME address space described in “Programming” on page 59. The control signals determine whether data is to be moved to the VMIVME-3113A (write) or from the VMIVME-3113A (read), provide the necessary data strobes (DS0, DS1) and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all of the timers and flags.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC, are read through the Status Register. The control and status registers are referred to collectively as the Control and Status Register (CSR), since they are at the same address. The WRITE signal determines which one is accessed. Most of the control register outputs can be monitored directly through the Status Register.

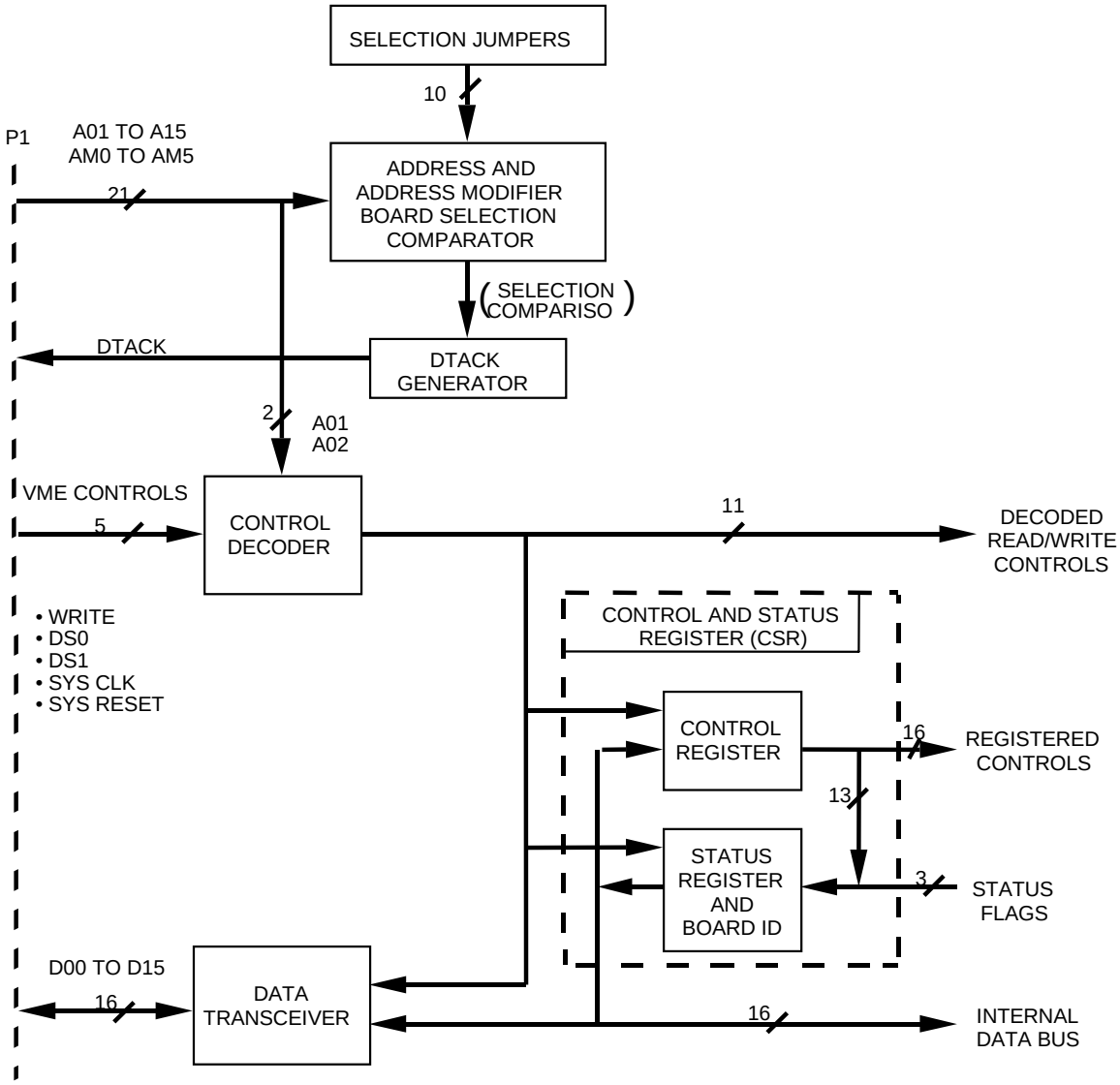
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Figure 1-1 VMIVME-3113A Functional Block Diagram



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Figure 1-2 VMEbus Control Signals and Interface Logic



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Analog-to-Digital (ADC) Control and Timing

Control commands and status flags associated with controlling the ADC are illustrated in Figure 1-2 on page 25 and are described in "Programming" on page 59 and the following sections.

There are three mode control bits in the CSR. The programming of these control bits (Mode 0H through Mode 2H) determine which one of six ADC operating modes the board is to operate in. The six ADC operating modes and the Control Register mode control bits are:

	CSR Control Bits		
	MODE2H	MODE1H	MODE0H
	D8	D7	D6
Autoscanning Mode	0	0	0
Random Polling Mode	0	0	1
Random Interrupt Mode	0	1	0
Scanning Poll Mode	0	1	1
Scanning Interrupt Mode	1	0	0
Autoscanning Mode with BIT	1	1	1

The ADC operating modes determine if the on-board ADC and channel selection are controlled externally by a CPU board or by the on-board channel sequencer. They also determine if an interrupt will be generated when the conversion(s) are complete. The six ADC operating modes will be described from a programming viewpoint in "Programming" on page 59.

The Autoscanning Mode, Scanning Poll Mode, Scanning Interrupt Mode and Autoscanning Mode with BIT scan a selectable number of channels. The scans run from channel 0 through channel (n-1), where n is encoded in the jumper field J10. During scans, there is a small charge transfer from each channel to the next. The charge transfers are more frequent (at each channel) when a small number of channels are scanned. To minimize this effect, at least 16 channels must be scanned.

NOTE: In order to fully utilize jumper field J10, it is recommended that the user assign inputs to channels starting at channel zero and continuing with the next highest channel such that no unused channels exist between any two used channels. Scanning unused inputs that are not grounded can adversely affect the conversion accuracy of used channels.

Random Polling and Random Interrupt Modes

In this mode, the CPU board controls the channel to be converted, starts the conversion and polls an end-of-conversion bit to determine when the conversion is complete. This mode is entitled random because the CPU board can select channels to be converted in any random order (that is, CH2, CH0, CH63, CH14…). The *Random*

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Interrupt Mode is essentially the same as the *Random Polling Mode* except an end-of-conversion interrupt is generated.

Autoscanning Mode

The *Autoscanning Mode* is automatically entered at power up of the board (or under program control). This mode performs a sequential scan of all configured inputs (minimum of 16; see “A / D Scan Sequence Length Jumper Configuration” on page 47), digitizing the input and storing the results in dual-port registers. The gain amplifier must be set to a gain of "one" in the Autoscanning Mode. Once all inputs are digitized, the process begins over at channel "zero". Any time a particular channel is read, the latest digitized information is available in that channel's dual-port register. This mode frees the programmer from selecting and starting a conversion on each channel, thus allowing the board to digitize at a faster rate and making programming of the board simpler.

Scanning Poll and Scanning Interrupt Modes

The *Scanning Poll Mode* is similar to the Autoscanning Mode. This mode executes a single scan of all channels and then stops. An end-of-scan status bit must be polled to determine when the scan is completed. The *Scanning Interrupt Mode* differs in that the end-of-scan generates an interrupt to the CPU board. A Bus Interrupter Module (BIM) handles the interrupt functions and is described in “Programming the Bus Interrupter Module (BIM)” on page 69.

Autoscanning Mode with BIT

This mode is identical to the Autoscanning Mode, except the channel 00 input may be replaced with one of three internal precision reference voltages: +4.980VDC, +0.4928VDC or +9.91mV. The reference is selected with CSR bits D00 and D01 as:

D01	D00	Channel 0:
0	0	Channel 0 input (same as AUTOSCAN)
0	1	+4.980V reference
1	0	+0.4928V reference
1	1	+9.91mV reference

NOTE: Scanning unused inputs that are not grounded can adversely affect the autoscanning mode with BIT. Therefore, for the BIT to function properly, it is necessary to short all unused input channels to ground. An unused channel can be shorted to ground by connecting the channel’s INPUT HI TO INPUT LO to the board’s ANALOG COMMON (see “Connector Descriptions” on page 51).

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Autoscan Mode and Scan Rate

In Autoscan Mode, the scan rate is equal to (Number of Channels) x 30.303 µs. However, a VMEbus interrupt cycle that is passed through the VMIVME-3113A (the VMIVME-3113A asserts IACKOUT) can hold off a write to memory by the VMIVME-3113A's scanning logic and add delays to completing a scan. The delay occurs when the A / D logic wants to perform a write to memory and an IACKIN cycle to the VMIVME-3113A is in progress. Thus, for a scan in which an A / D write to memory is delayed by an IACK cycle, the actual scan rate will be the normal scan rate + IACK time. For example, the autoscan rate for 64 channels would be (64) x 30.303µs or 1.9394ms. If an IACKIN / IACKOUT cycle of 1 µs occurred during the 64-channel scan, the scan rate would increase to 1.9404ms. It is recommended that the VMIVME-3113As be placed at the end of the IACK daisy chain preventing these possible delays.

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ADC Conversion and Timing

Regardless of which ADC OPERATING MODE, described in "Analog-to-Digital (ADC) Control and Timing" on page 26, is used, the A / D conversion sequence is the same. Once the conversion sequence has begun (for any of the six A / D operating modes), it consists of the following consecutive time intervals:

- Settling Delay
- Tracking Interval
- Analog-to-Digital (A / D) Conversion

All ADC timing intervals discussed in this section are performed automatically by the on-board smart controller.

The settling delay occurs directly after a state-change has occurred in the analog networks (such as selecting a new input channel) and represents the settling time of the networks. After the settling delay has been completed, the Track-and-Hold (T&H) amplifier (Figure 1-1 on page 24) enters the TRACKING MODE and the tracking interval begins. During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage.

At the end of the tracking interval, the T&H amplifier enters the HOLD MODE, in which the output of the amplifier is held at a constant level, and a CONV CMD from the timing decoder causes the A / D conversion to begin. The A / D conversion digitizes the output of the T&H amplifier into a 12-bit data word, and then terminates the conversion sequence. The CONV COMPL L signal from the ADC is HIGH during the conversion, and is LOW otherwise.

In the RANDOM POLL MODE, completion of the A / D conversion causes the NEW DATA RDY flag to be set HIGH, indicating that valid data is present in the Random Converter Data Register (RCDR) ("Programming" on page 59). The action of reading the RCDR resets the NEW DATA RDY flag in the CSR.

If the conversion is the last channel to be converted in the SCANNING POLL MODE, then a flag (END OF SCAN H) is set in the Control and Status Register (CSR). This flag may be read to determine that all channels have been converted and stored and are available to be read. This flag is cleared when the next scan is started.

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Analog Inputs

Sixty-four differential or single-ended analog input channels are available from two front panel connectors. It is recommended that the differential mode be used for increased noise and common-mode rejection. Unused inputs should be grounded. This includes the low-side of differential inputs. For correct operation, both the high-side and low-side inputs must be within ±12V of the VMEbus chassis ground.

Low Pass Filters and Input Multiplexers

The 64 analog input channels can be provided with individual, single-pole, low pass filters, as shown in Figure 1-3 on page 31, and can be user-configured to operate either single-ended or differentially. See the specification for input filter specifications.

Each of the 64 analog inputs is selectable through one of eight input multiplexers. Each multiplexer accepts eight differential input pairs. A second tier multiplexer receives the selected channel from one of the eight input multiplexers.

Both multiplexer sections are controlled by the same set of six address lines (INP MUX ADDRESS) which are derived from control bits "MUX A00" through "MUX A05" from the Control Register.

Single-Ended Versus Differential Operation

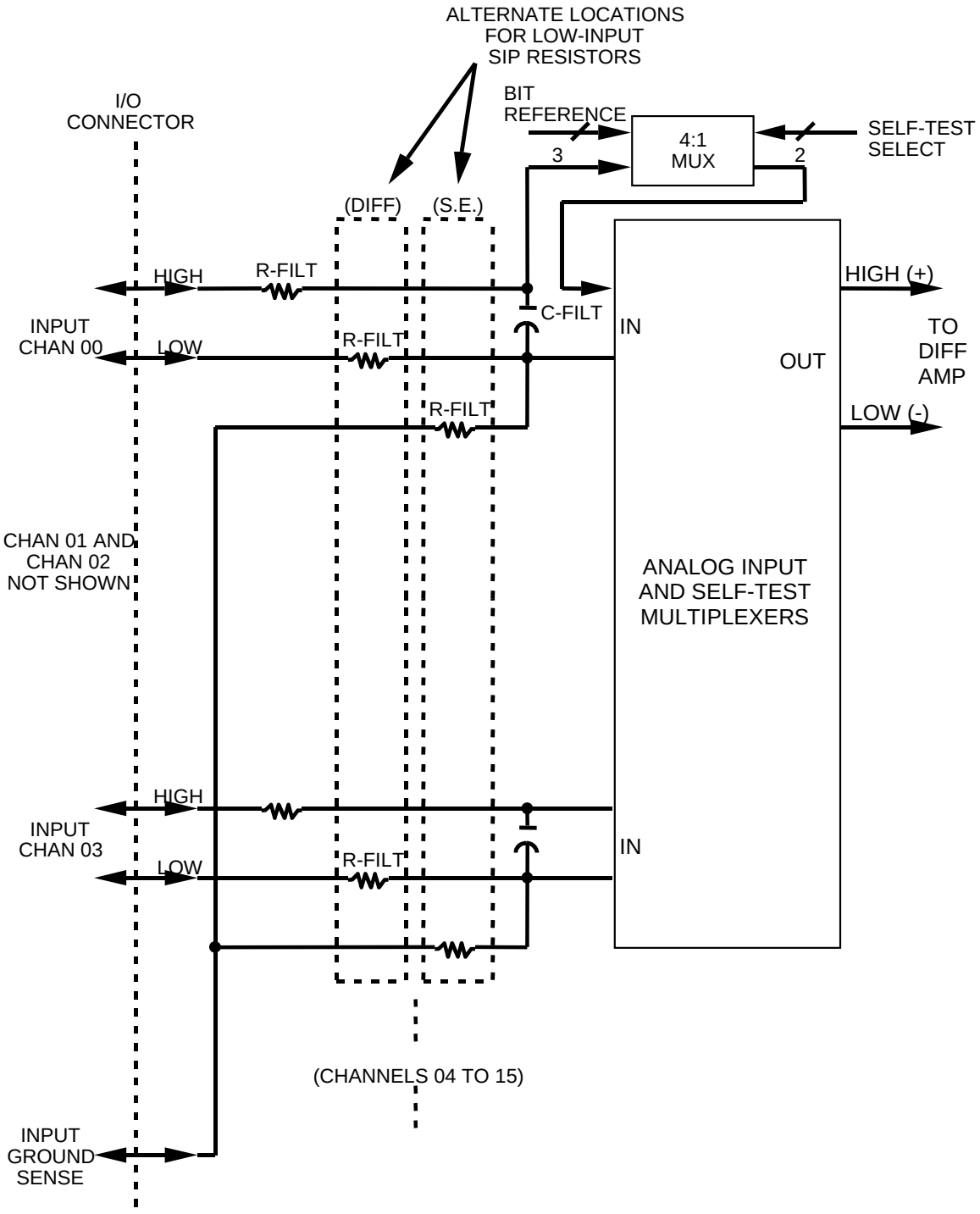
Differential or single-ended operation of the analog inputs is selected by the location of Single-In-Line-Package (SIP) resistors, as illustrated in Figure 1-3 on page 31. The input multiplexers are always operated in the differential mode; single-ended (pseudo-differential) operation is obtained by connecting the LOW input resistor to the common INPUT GROUND SENSE input instead of to the individual LOW signal inputs.

To prevent high frequency noise from becoming a common-mode signal and causing the data output of the VMIVME-3113A to fluctuate, the input circuits can be made single-ended and all of the row C pins are grounded. This means that all of the RFILT resistor SIPs in the schematic are replaced with SIP headers. These are essentially 0Ω SIP resistors. Jumper J2 is also installed. Now all of the inputs have their returns tied to local ground via a low resistance path. This also shifts the pole frequency of the input filter, since half of the input resistance is gone. The new frequency is twice that of the differential value.

All VMIVME-3113A input channels are overvoltage protected by current-limiting input resistors. These provide protection to ±40V.

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Figure 1-3 Single-Ended and Differential Input Configurations



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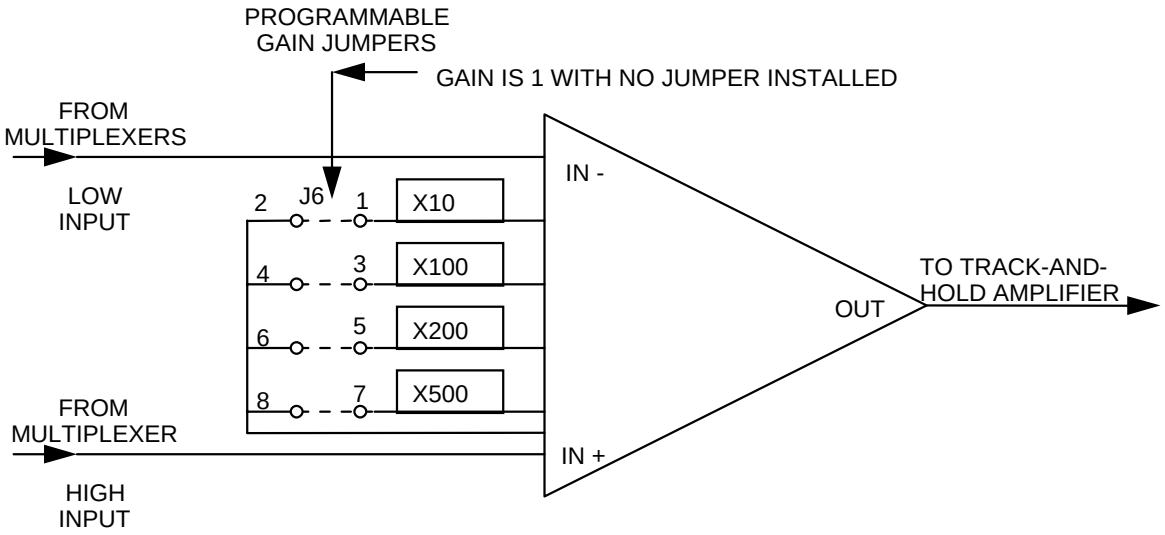
Jumper-programmable Gain Amplifier

Once an input channel has been selected and routed through the input multiplexers, it enters the Programmable-Gain Amplifier as a differential input. The differential amplifier rejects common mode noise and delivers a scaled single-ended output to the Track-and-Hold (T&H) device. The Programmable-Gain Amplifier may be jumpered for gains of 1, 10, 100, 200 and 500. This allows for an input in the -10 to +10mV range to be scaled up to a -5 to +5V input range for the ADC. When a gain of 500 is selected the GAIN DEL bit (D15) in the CSR must be set. This increases the analog acquisition time from 15 to 28 µs to allow complete input setting for the new channel. Figure 1-4 below shows the gain configuration for the Programmable-Gain Amplifier.

Channel Sequencer and Dual-port Register Control

When the VMIVME-3113A is operated in any of the scanning modes, the operation is controlled by an on-board channel sequencer. For example, when the board is powered-on, a conversion sequence begins at channel 00, as discussed in "Analog-to-Digital (ADC) Control and Timing" on page 26. Once the A/D conversion is completed, the dual-port control logic takes the converted data and stores it in that channel's appropriate dual-port register. The channel counter is incremented by one, which selects the next channel to be multiplexed to the ADC. Concurrently with selecting the next channel, a new A/D conversion sequence is initiated. When all input channels the channel scanning sequence again (AUTOSCANNING MODES only).

Figure 1-4 Programmable Gain Amplifier



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Programmable Interval Timer

A triple, 16-bit timer (cascadeable to 48 bits) may be programmed to trigger the start of an ADC scan sequence. For example, it might be required to obtain updated digitized data only once every second. The board could be set for the SCANNING INTERRUPT MODE. The timer would be set to generate a pulse once every second. That pulse would initiate the ADC scan sequence. Once all channels are digitized and stored, an end-of-scan interrupt would be generated to the CPU to indicate that data is available. The interrupt service routine would read the data into memory and then re-initialize the Bus Interrupter Module (BIM) for the next interrupt.

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Bus Interrupter Module (BIM)

A BIM handles all interrupt interfacing to the VMEbus. An interrupt may be generated on any VMEbus level (1 through 7). Depending on the mode used, an interrupt may be generated upon the completion of a single A / D conversion, or upon the completion of a 16- through 64-channel scan.

The BIM generates an 8-bit vector (D08(O)) after generating an Interrupt Request and in response to the Interrupt Acknowledge cycle from the CPU board. Typically, the CPU will use the 8-bit vector to select an interrupt handler from a table of addresses. An interrupt program example is found in “Programming” on page 59.

If there are empty backplane slots between the VMIVME-3113A and the CPU, then IACK jumpers may be needed on the backplane.

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Board ID Register

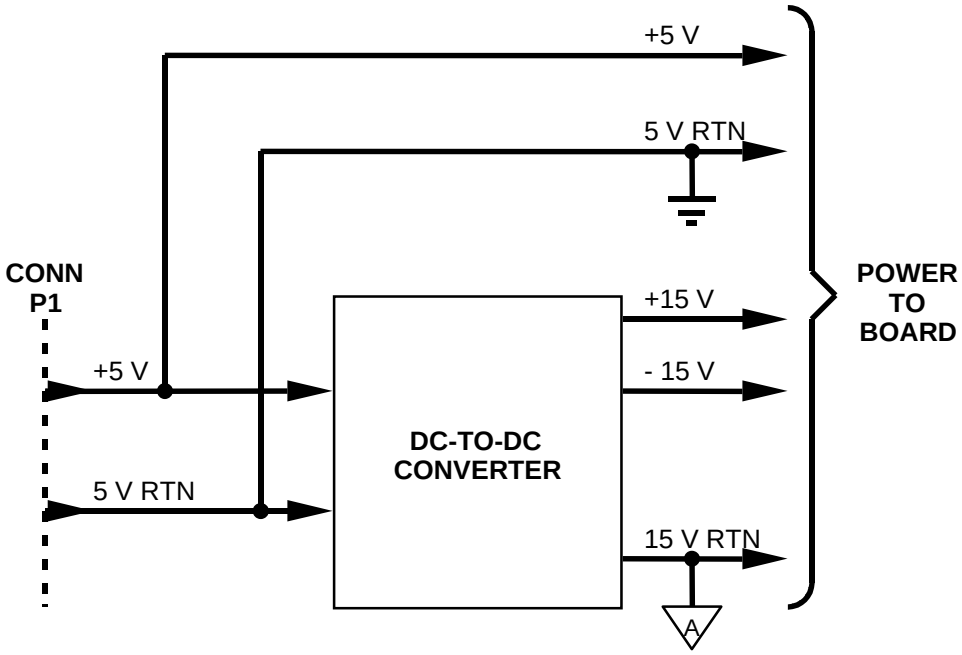
The first word location of the VMIVME-3113A's register set is a read-only register. It always reads 11XX (HEX; the last two digits are not specified). Other VMIC products have similar registers which read different constants. This allows general-purpose system software to automatically determine what boards have been installed (by reading from a predetermined list of addresses).

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Built-in Power Converter

Electrical power for the VMIVME-3113A analog network is supplied by the DC-to-DC converter shown in Figure 1-5 below. The converter transforms +5V logic power into regulated and isolated ±15VDC power, with a load capacity of approximately 100mA on each 15V bus.

Figure 1-5 Power Converter



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CHAPTER
2

Configuration and Installation

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Before Applying Power: Checklist 40
Operational Configuration 41
Calibration 49
Connector Descriptions 51

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

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Physical Installation

NOTE: Do not install or remove board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

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Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming of the DAC board, "Theory of Operation" on page 21 and "Programming" on page 59, been read and applied to system requirements?
2. Review "Factory-Installed Jumpers" on page 41 and Table 2-1 on page 43 to verify that all factory-installed jumpers are in place. To change the board address or address modifier response, refer to "Board Address and Address Modifier Selection" on page 44.
3. Have the input cables, with the proper mating connectors, been connected to the input connectors P3 and P4? Refer to "Connector Descriptions" on page 51 for a description of the connector.
4. Calibration has been performed at the factory. If recalibration should be required, refer to "Analog Inputs Calibration Procedure" on page 49.
5. Ground unused inputs (both high-side and low-side) to VMEbus ground.

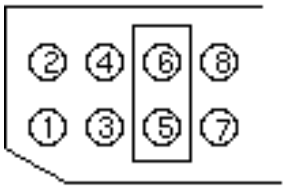
WARNING: Do not install or remove this board with the power applied to the system.

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Operational Configuration

Control of the VMIVME-3113A board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers and their effects on board performance. The locations and functions of all VMIVME-3113A jumpers are shown in Figure 2-1 on page 42 and Table 2-1 on page 43.

NOTES:
Rectangular jumper fields (J5, J6, J7, J9, J10) are numbered and used along the short direction.



These fields are up to 20 pins in length (10 position) and indicate open-ended header drawing.

Factory-Installed Jumpers

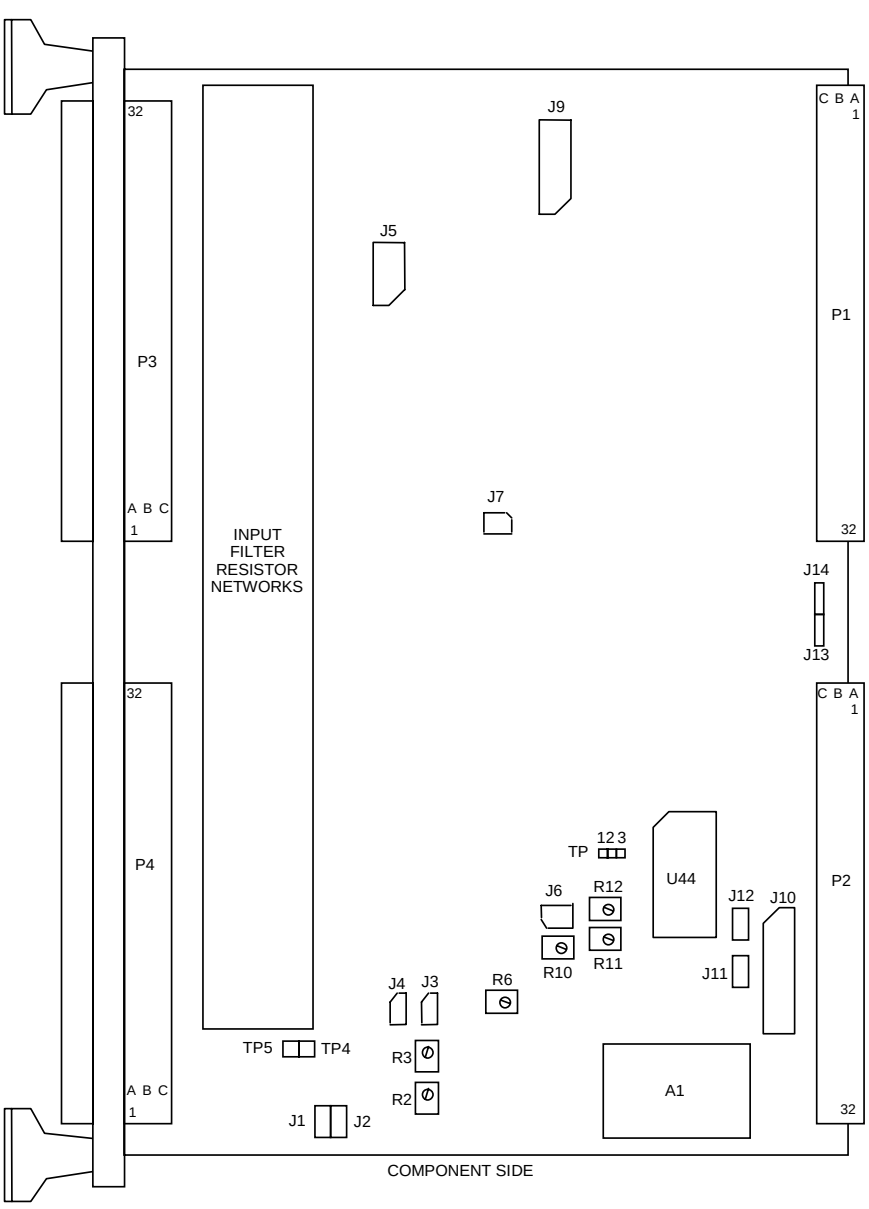
Each VMIVME-3113A board is configured at the factory with the specific jumper arrangement shown in Table 2-1 on page 43. The factory configuration establishes the following functional baseline for the VMIVME-3113A board, and ensures that all essential jumpers are installed.

- Board short address is set at 0000 HEX.
- I/O access mode is both short supervisory access and short nonprivileged access.
- Analog input range is set to ±10V full-scale range.
- The number of channels for an A/D Scan is set to 64.
- The gain amplifier is set to a gain of "one".

NOTE: Jumper J5 has no effect on the analog circuit. It is provided to allow the software to determine the analog configuration of the board. Factory configuration loads all J5 jumpers for the user's convenience. Please remove jumpers J5-1,2 and J5-3,4 to match the hardware configuration jumpers (see "Configuration Register" on page 63 for jumper configuration usage).

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Figure 2-1 Programmable Jumpers, Test Points and Resistor Network Locations



J1 Connects On-Board GND and GND Reference
For All 64 Channels, Installed

J2 Connects P4C1 "GND REF"
For All 64 Channels, Omitted

J3 Inputs Bipolar or Unipolar
Pins 1, 2 Bipolar, Jumper Installed
Pins 2, 3 Unipolar, Omitted

J4 Inputs Full-Scale Range
Pins 1, 2 = 20 V, Jumper Installed
Pins 2, 3 = 10 V, Omitted

J5 Configuration Register Bits 4 through 0
Installed = 0
Omitted = 1

J6 Programmable Gain Amplifier
Pins 1, 2 Gain of 10, Omitted
Pins 3, 4 Gain of 100, Omitted
Pins 5, 6 Gain of 200, Omitted
Pins 7, 8 Gain of 500, Omitted

J7: Pins 5, 6 Enables CTR0 to Start A/D Conversion
No Jumper Installed

J7: Pins 3, 4 Cascades CTR0 to CTR1
No Jumper Installed

J7: Pins 1, 2 Cascades CTR1 to CTR2
Jumper Installed

J9 Board Address and Board Access
Pins 1 Through 16 Jumpered for Board Addresses A08 through A15. Pins 17 and 18 for Short Supervisory or Nonprivileged, Pins 19 and 20 for Short Nonprivileged. Omit both J9-17, 18 and J9-19, 20 for Short Supervisory Access.

J10 Select CHs to Convert in A/D SCAN
J10 Pins 1, 2 to 13, 14 Installed
(SCAN Length to 64 Chs)

J11 GND for Status Signal (P2 Output)
No Jumper Installed

J12 GND for EXT Trigger Input (P2 Input)
No Jumper Installed

J13 States Signal for EXT Trigger Input (P2 Output)
No Jumper Installed

J14 Enable EXT Trigger Input (P2 Input)
No Jumper Installed

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Table 2-1 Configuration Jumper Functions

Jumper ID	Function	Factory Configuration
J9 - 1,2 J9 - 3,4 J9 - 5,6 J9 - 7,8 J9 - 9,10 J9 - 11,12 J9 - 13,14 J9 - 15,16 J9 - 17,18 J9 - 19,20	Board Address Bit A08 = 0 Board Address Bit A09 = 0 Board Address Bit A10 = 0 Board Address Bit A11 = 0 Board Address Bit A12 = 0 Board Address Bit A13 = 0 Board Address Bit A14 = 0 Board Address Bit A15 = 0 *Short Supervisory or Nonprivileged Access *Short Nonprivileged Access	Installed Installed Installed Installed Installed Installed Installed Installed Installed Omitted
J13	Status Signal for External Trigger Input (P2 Output)	Omitted
J11	Ground Connection for J13 Status Signal (P2 Output)	Omitted
J14	Enable External Trigger Input (P2 Input)	Omitted
J12	Ground Connection for Enable External Trigger (P2 Input)	Omitted
J7 - 5,6 J7 - 3,4 J7 - 1,2	Enables CTR0 to Start A / D Conversion Circuitry (16-bit CTR) Cascades CTR0 to CTR1 (32-bit CTR) Cascades CTR1 to CTR2 (48-bit CTR)	Omitted Omitted Installed
J10 - 1,2 to J10 - 13,14	These Seven Jumpers Select the Number of Channels to Be Converted in A / D Scan. J10 - 1,2 is the LSB. J10 - 13,14 is the MSB.	1,2 to 11,12 Installed13,14 Omitted
J2	Connects P4-C1 as the GND REF Connection for All 64 CHs	Omitted
J1	Connects the On-Board GND as the GND REF for All 64 CHs	Installed
J6 - 1,2 J6 - 3,4 J6 - 5,6 J6 - 7,8	Sets the Programmable-Gain Amplifier to a Gain of 10 Sets the Programmable-Gain Amplifier to a Gain of 100 Sets the Programmable-Gain Amplifier to a Gain of 200 Sets the Programmable-Gain Amplifier to a Gain of 500	Omitted Omitted Omitted Omitted
J4 - 1,2 J4 - 2,3	Inputs, 20V Full-Scale Range Inputs, 10V Full-Scale Range	Installed Omitted
J3 - 1,2 J3 - 2,3	Inputs, Bipolar Operation Inputs, Unipolar Operation	Installed Omitted
J5 - 1,2 to J5 - 9,10	CFR Bit 4 to CFR Bit 0, Respectively. Each of the Configuration Register Bits Reads Zero When Its Jumper is Installed. The Other CFR Bits are Fixed. See "Configuration Register" on page 63 for Configuration Usage.	Installed

* Omit both J9 - 17,18 and J9 - 19,20 for Short Supervisory Access only.

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Board Address and Address Modifier Selection

Jumper header J9 permits the VMIVME-3113A Board to be located on any 256-byte boundary within the short I/O address space. The short I/O address space consists of all addresses between NNNN0000 HEX* and NNNNFFFF HEX, and requires that fifteen (word) address lines be decoded in order to account for all the locations. Since seven lines are used for decoding on-board functions ("Programming" on page 59), the VMIVME-3113A board address is defined by eight lines, address bits A08 through A15. The board address is programmed by installing shorting plugs at all "zero" or LOW address bit jumper positions, and by omitting the shorting plugs at the "one" or HIGH positions. As an example, the jumper arrangement shown in Table 2-2 below would produce a board address of NNNN8500 HEX.*

VMEbus accesses may be supervisory or nonprivileged. Leave J9-17,18 and J9-19,20 empty for supervisory access. Install J9-17,18 to allow either access. Install J9-19,20 for nonprivileged only access.

*The value NNNN depends on the make and model of the CPU board used.

Table 2-2 Board Address Selection Example (NNNN8500)*

Address Bit	Jumper	State**
A08	J9-1,2	Open
A09	J9-3,4	Shorted
A10	J9-5,6	Open
A11	J9-7,8	Shorted
A12	J9-9,10	Shorted
A13	J9-11,12	Shorted
A14	J9-13,14	Shorted
A15	J9-15,16	Open
Address Modifier Bit 2 ***	J9-17,18 J9- 19,20	Open Shorted

* (NNNN) HEX is CPU board dependent. (85) HEX is address bits A15 through A08 as shown.

** Shorted = "zero" (jumper installed).
Open = "one" (no jumper installed) (see Table 2-1 on page 43).

*** AM2 + AM2 select short supervisory access, short nonprivileged acces or both (the example shown is for short nonprivileged access).

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Analog Input Modes

Differential or Single-Ended Operation

The VMIVME-3113A is shipped with its inputs configured for differential operation. All 64 inputs can be changed to single-ended mode by moving some resistor SIPs: take the SIPs from RP1-16 and put them in RP17-32. All of the sockets for these SIPs are in four columns next to the front panel.

In the single-ended mode, the external field ground sense input can be used to compensate for the potential differences between equipment signal returns. If the J2 jumper is installed, pin C1 of the input connector P4 serves as a ground sense for all single-ended inputs. There is a 40.2 k? resistor on-board the VMIVME-3113A which will tend to pull this ground sense to VMEbus digital ground. If the J1 jumper is installed (instead of J2), then the single-ended inputs will operate relative to VMEbus digital ground (which may be quite noisy). It is recommended the board be used in the differential input mode.

NOTES ON INPUT VOLTAGE:
For proper operation, the voltage on any input pin may not exceed (+) or (-) 12V relative to the VMEbus ground.

An isolated input source will have an indeterminate common-mode voltage relative to VMEbus ground. In such cases, it may be necessary to provide signal sources with the VME ground reference.

An internal ground reference is available at any row B pin in both P3 and P4. Access to row B requires a 96-wire cable with 0.033-inch spacing. An alternate method of obtaining a ground reference is to install jumpers J1 and J2. With J1 and J2 installed, input channel 0 would not be usable as a differential input, but pin C1 on P4 would be connected to VMEbus ground. Channel 0 may still be used as a single-ended input. Current through pin C1 on P4 should not exceed 750mA continuous.

Input Voltage Range

Input voltage range is controlled by jumpers J4-1, 2, 3. The maximum full-scale range is 20V. To modify the full-scale range to 10V, configure the jumpers as indicated in Table 2-1 on page 43. All input voltages must be within 12V of VMEbus ground for linear operation. For gains other than one, all input voltages must be within 10V of VMEbus ground. For single-ended operation, the ground sense counts as an input.

Bipolar or Unipolar Operation

Bipolar or unipolar operation of the analog inputs is selected with jumpers J3-1, 2, 3 as indicated in Table 2-1 on page 43.

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External Trigger Jumper Description

The external trigger circuitry allows the user to input a TTL level "zero" to start an A / D conversion or an A / D conversion scan sequence. This input must be enabled to the PC connector by installing jumpers J12 and J14. J12 allows a ground reference connection. J14 enables the trigger signal and is labeled EXT STRT CONVERT L on the schematic. In addition to the jumper, the ENA EXT STRT H (D11) must be set in the Control Register. This signal is also brought out to the user via the P2 connector. External circuitry can monitor this TTL signal, and when it goes High to a logic "one", then the board is ready for the EXT STRT CONVERT L input to begin a conversion(s). The ENA EXT START H signal is enabled to the P2 connector via Jumpers J11 and J13. This signal is a TTL High (Logic "one") which is used to signal external equipment that the board is ready to receive an external trigger. Install J13 to connect ENA EXT START H to the P2 connector and install J11 to connect a reference ground to the P2 connector. Table 2-3 on page 46 gives the connector description for the External Trigger signal.

Interval Timer - 16-, 32- or 48-bit Timer Selection

The interval timer has three 16-bit counters. These three timers may be jumpered in ways to generate a maximum count length of 16, 32 or 48 bits (refer to "Programmable Interval Timer" on page 68 to determine counter resolution and programming). Table 2-4 below shows the possible jumper configurations.

Table 2-3 External Trigger Connections

Signal	Function	Jumper	Connector
EXT STRT CONVT L	External Trigger Input	J14	P2 - A27
GND	Board GND REF	J12	P2 - A28
ENA EXT STRT H	Control Register Enable Output	J13	P2 - A31
GND	Board GND REF	J11	P2 - A32

Table 2-4 Interval Timer Jumper Configurations

Counter Length	Install Jumper	Time Delay Range
16 bits	J7 - 5,6	0 to 8.192msec
32 bits	J7 - 3,4	8.192msec to 536 sec
48 bits	J7 - 1,2	536 sec to 9773 hr

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A/D Scan Sequence Length Jumper Configuration

The three scanning modes (AUTOSCANNING MODE, SCANNING POLL MODE and SCANNING INTERRUPT MODE) use the jumpers at J10 to determine how many channels to scan. Scans always begin with channel 0 and continue with the next higher channel until J10 matches the total number of channels scanned. For example, the factory setting does all 64 channels (0 through 63) by encoding 64 in J10. J10-13, 14 is the most significant bit. J10-1, 2 is the least significant bit. J10-3, 4; J10-5, 6; J10-7,8; J10-9, 10; J10-11, 12 have weights of 2, 4, 8, 16 and 32 channels, respectively. An installed jumper signifies a "zero". Table 2-5 on page 47 gives some examples of the jumpers to be installed for different scan lengths. See "Analog-to-Digital (ADC) Control and Timing" on page 26 for restrictions on jumper settings.

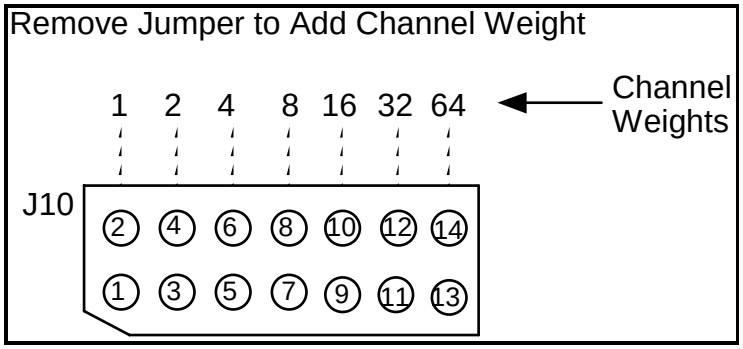


Table 2-5 A/D Scan Length (Jumper) Example

Number of Channels to Be Scanned	Installed All J10 Jumpers Except
16	J10 - 9,10
20	J10 - 5,6; J10 - 9,10
32	J10 - 11,12
37	J10 - 1,2; J10 - 5,6; J10 - 11,12
64	J10 - 13,14

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Programmable Gain Jumper Configuration

The Gain Amplifier may be configured for gains of 1, 10, 100, 200 and 500 to handle signal levels as low as ±10mV. Table 2-6 below shows which jumper is to be installed. The board is factory configured for a gain of "one" (no jumper installed).

Table 2-6 Programmable Gain Jumper Configurations

Gain (X)	Install Jumper
1	None
10	J6 - 1,2
100	J6 - 3,4
200	J6 - 5,6
500	J6 - 7,8

Configuration Register Jumper

The VMIVME-3113A input range and gain are determined by jumpers J3, J4 and J6 in the analog circuitry. The configuration of these jumpers cannot be read, but the Configuration Register (CFR) reads digital jumpers (J5) which can be configured to provide the same information. By convention, the CFR bits read as follows:

Jumper	CFR Bit	Configuration
J5-1,2	D4	Installed = Unipolar Inputs (0 to +10V) Removed = Bipolar Inputs (±10V, ±5V)
J5-3,4	D3	Installed = 10V FSR (±5V, 0 to +10V Inputs) Removed = 20V FSR (±10V Inputs)

These three jumpers specify gain configuration as follows:

	D2 J5-5,6	D1 J5-7,8	D0 J5-9,10	Gain Setting
J5-5,6 = D2	0	0	0	X1
J5-7,8 = D1	0	0	1	X10
J5-9,10 = D0	0	1	0	X100
	0	1	1	X200
	1	0	0	X500

NOTE: Zero (0) Indicates a jumper installed.

Bit 4 is set unless a shunt is installed over J5-1,2. Bit 3 is set unless a shunt is installed over J5-3,4. Similarly, bits 2,1 and 0 correspond to J5-5,6, J5-7,8 and J5-9,10.

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Calibration

Before delivery from the factory, the VMIVME-3113A Board is fully calibrated and conforms to all specifications listed in the specification sheet. Should recalibration be required, however, perform the procedures in "Analog Inputs Calibration Procedure" on page 49 and "Built-in-Test Calibration Procedure" on page 50 with the equipment listed in "Equipment Required" on page 49. The locations of all adjustments and test points are shown in Figure 2-1 on page 42.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however. All adjustments should be resealed with a suitable fast curing sealing compound after recalibration has been completed.

CAUTION: Do not install or remove this board with the power applied to the system.

Equipment Required

- **Digital Voltmeter (DVM)** — ±1.0000VDC and ±10.000VDC ranges; 5 or more digits; ±0.005 percent of reading voltage measurement accuracy; 10MΩ minimum input impedance.
- **Analog Voltage Source** — ±10.000VDC Range; resolution 0.0005VDC; Accuracy, ±0.005 percent of expected value; 0.10Ω maximum output impedance.
- **Chassis** — VMEbus backplane or equivalent, J1 and J2 connectors, VMEbus master controller, +5 ±0.1VDC, power supply. One slot allocated for testing the VMIVME-3113A Board.
- **Extender Board** — VMEbus extender board.
- **Test Cables** — Test cables for the equipment listed above.

Analog Inputs Calibration Procedure

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), next adjusting the most positive output to its ideal value (Gain Adjustment). The calibration must be performed when changing the A/D's input full-scale range from one value to another (for example, from ±10 to ±5V). The procedure is as follows:

1. Install the VMIVME-3113A Board on an extender board in a VMEbus backplane.
2. Configure the analog inputs to the desired voltage range (i.e., ±10V, ±5V, 0 to +10V).
3. Apply the power to the backplane. Allow a minimum warm-up interval of ten minutes after power has been applied before proceeding.
4. Connect the analog voltage source at CH0, between connector pins P4-A1 (+) and P4-C1 (-).

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5. Adjust the analog voltage source for the most negative calibration value of the full-scale range selected. Refer to Table 2-7 on page 50.
6. While reading CH0, adjust R12 for unipolar ranges or R3 for bipolar ranges. CH0 board offset is 80 (HEX). Continue adjusting the potentiometer until the value read flickers between 000 HEX and 001 HEX.
7. Adjust the analog voltage source for the most positive calibration value of the full-scale range selected. Refer to Table 2-7 on page 50.
8. While reading CH0, adjust R2 until the value read flickers between FFE and FFF HEX.
9. Calibration is now complete. Remove all of the test connections, and restore the board to its original configuration.

Table 2-7 Calibration Data Table

Voltage Range	Offset Adjustment Potentiometer	Gain Adjustment Potentiometer	Negative Calibration Voltage	Positive Calibration Voltage
-5 to +5V	R3	R3	-4.9988V	+4.9963V
-10 to +10V	R3	R2	-9.9976V	+9.9963V
0 to +10V	R12	R2	+1.22mV	+9.9963V

Built-in-Test Calibration Procedure

The three self-test reference voltages are derived from one adjustable reference via a resistor divider. The divider resistors are matched to ±0.25 percent. This means that one voltage must be chosen for perfect adjustment based on the intended VMIVME-3113A gain. The other two voltages will be close to nominal, but not perfect.

1. Install the VMIVME-3113A into a chassis / extender board; turn it on.
2. Determine at what gain the VMIVME-3113A will be configured.
3. Write (HEX) 3C1 (for a gain of 1), or 3C2 (G=10), or 3C3 (other gains) to the CSR at board offset 2.
4. Connect a voltmeter to TP4 (+) and TP5 (-).
5. Adjust R6 until the voltmeter reads the desired voltage. The nominal voltages are: 4.980V, 492.8mV and 9.92mV for gains of 1, 10 and 100-500, respectively.

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Connector Descriptions

Two connectors, P1 and P2, connect the VMIVME-3113A Board to the VMEbus backplane. The connectors are 96-pin DIN type. The primary connector, P1, contains the address data and control lines and all additional signals necessary to control data transfer and other bus functions. The VMIVME-3113A Board uses four of the user I/O pins of connector P2 to allow an external trigger input and a status output. The P2 connector pin and signal assignments are shown in Figure 2-2 on page 52 and Table 2-8 on page 53.

The P3 and P4 connectors are 96-pin male DIN connectors. Their primary source is Panduit, PN 100-096-033. A compatible connector is AMP 925486-1 with AMP 530151-6 crimp pins. These connectors support the 32 single-ended or 32 differential analog inputs each with an associated analog ground pin. For P3 connector pin and signal assignments, refer to Figure 2-3 on page 54 and Table 2-9 on page 55. For P4 connector pin and signal assignments, refer to Figure 2-4 on page 56 and Table 2-10 on page 57.

The P3 and P4 connectors have an "A" row (A1 through A32), a "B" row (B1 through B32) and a "C" row (C1 through C32). All "A" row pins are the high side of the input signal. All "C" row pins are the low side of the input signal. The preferred method of connecting analog input signals is to connect both high and low inputs for each channel (differential). Differential inputs provide for very high common-mode noise rejection by rejecting differences in ground potential between the analog transmitter and the VMIVME-3113A Board. The board is factory configured to accept differential inputs.

All "B" row pins are connected to the internal analog ground, and are available to the system if 96-wire cables with 0.033-inch spacing are used for the P3 and P4 connections.

A second method of connecting analog inputs is referred to as "pseudo-differential". In this connection scheme, only one ground reference is brought to the board and connected to the P4 connector at pin C1. This implies that all connected channels from the field must be referenced to the same ground. This method has some of the advantages of differential inputs in that it rejects ground differences, but is not as effective in common-mode noise rejection. Jumper J2 must be installed to enable this mode. In addition, the SIP resistors on the inputs must be in the single-ended position as described in "Differential or Single-Ended Operation" on page 45.

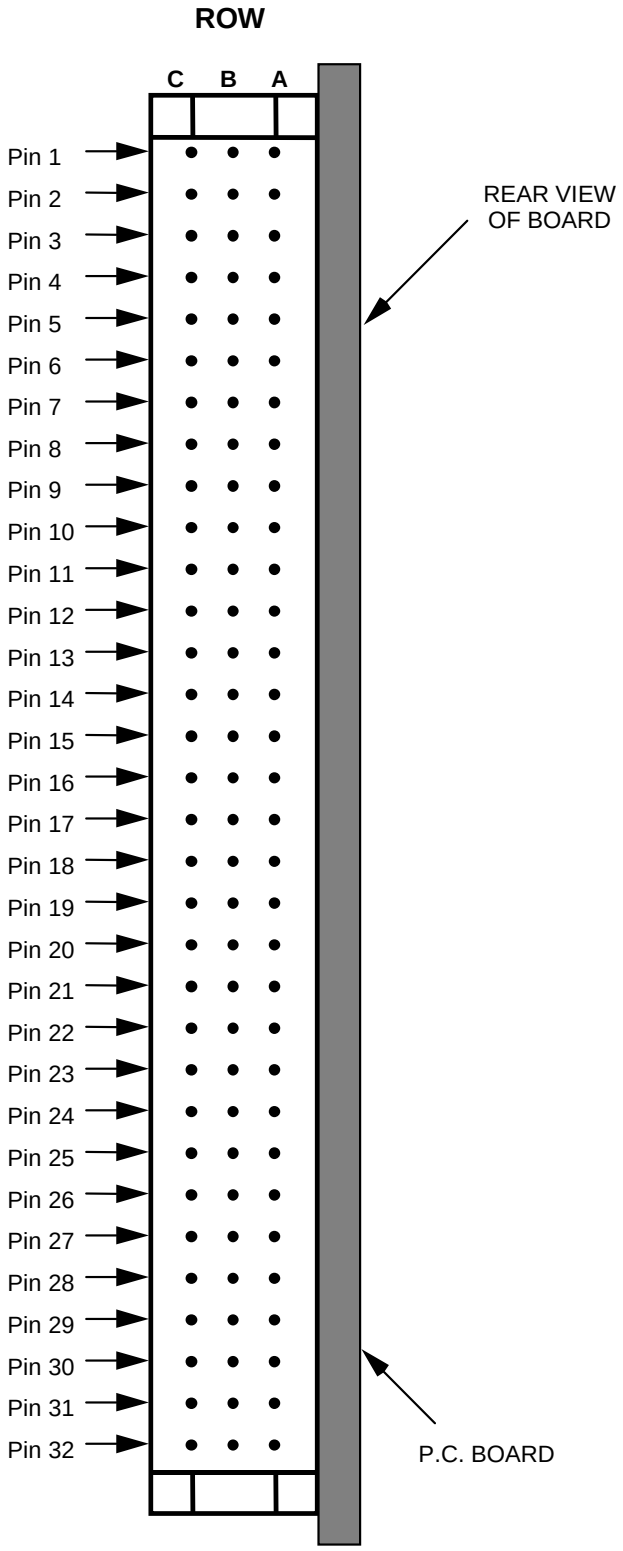
A third method of connecting analog inputs is as "single-ended" inputs. This method uses the on-board analog ground as the input signal reference. This is generally the least accurate of the three methods. However, in a low-noise environment and when short cabling is used, this method will work well. The input SIP resistors must be moved from the differential to single-ended sockets (refer to "Differential or Single-Ended Operation" on page 45.) and jumper J1 must be installed.

A *Connector and I/O Cable Application Guide* (Document No. 825-000000-006) is available from VMIC that provides additional information concerning the field connections, the use of round cables and a thorough explanation of compatible connectors and cabling techniques.

NOTE: For proper operation, unused-scanned channels must be terminated by connecting the INPUT HI TO INPUT LOW AND to the ANALOG COMMON.

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Figure 2-2 P2 Connector Pin Configuration



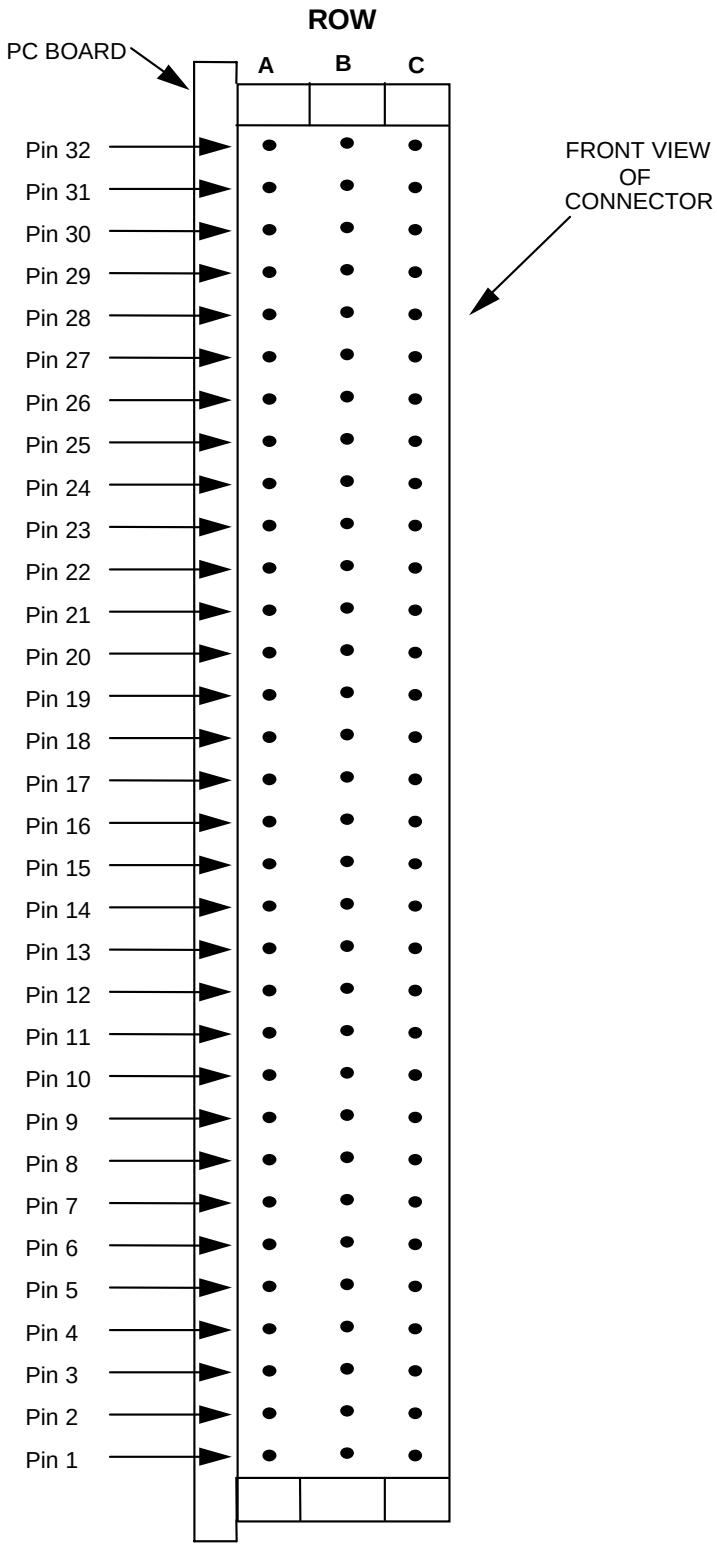
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Table 2-8 P2 Connector Signal Assignments

Pin	Row C	Row B	Row A
01	N / C	+5VDC	N / C
02	•	GND	•
03	•	•	•
04	•	•	•
05	•	•	•
06	•	•	•
07	•	•	•
08	•	•	•
09	•	•	•
10	•	•	•
11	•	•	•
12	•	GND	•
13	•	+5VDC	•
14	•	•	•
15	•	•	N / C
16	•	•	•
17	•	•	•
18	•	•	•
19	•	•	•
20	•	•	•
21	•	•	•
22	•	GND	•
23	•	•	•
24	N / C	•	•
25	•	•	•
26	•	•	N / C
27	•	•	EXT STRT CONVERT L (IN)
28	•	•	GND
29	•	•	•
30	•	•	•
31	•	GND	ENA EXT STRT H (OUT)
32	•	+5V	GND

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Figure 2-3 P3 Connector Pin Configuration



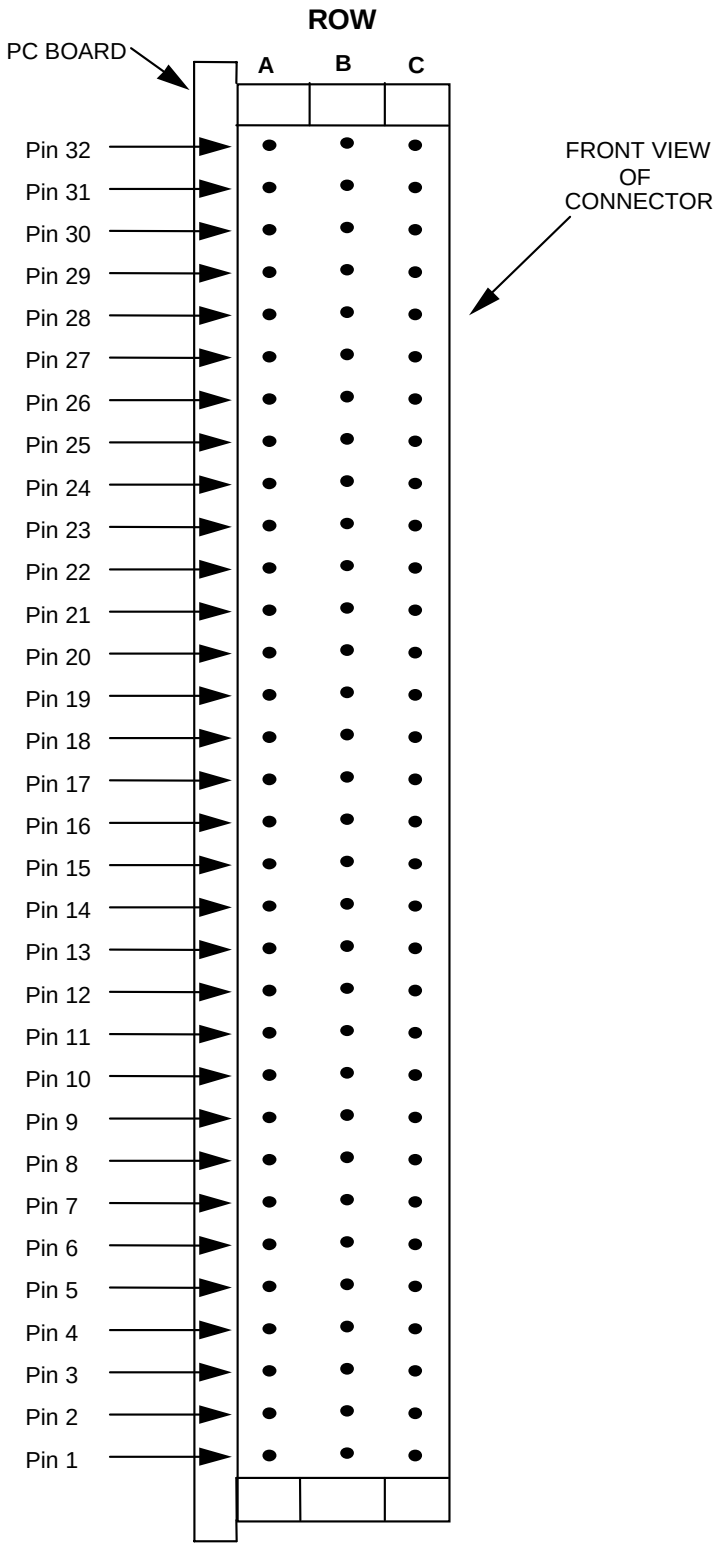
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Table 2-9 P3 Connector (Front Panel Inputs) Signal Assignments

Pin	Row A	Row B	Row C
01	CH 32 HIGH	•	CH 32 LOW
02	CH 33 HIGH	•	CH 33 LOW
03	CH 34 HIGH	AGND	CH 34 LOW
04	CH 35 HIGH	•	CH 35 LOW
05	CH 36 HIGH	•	CH 36 LOW
06	CH 37 HIGH	•	CH 37 LOW
07	CH 38 HIGH	•	CH 38 LOW
08	CH 39 HIGH	•	CH 39 LOW
09	CH 40 HIGH	•	CH 40 LOW
10	CH 41 HIGH	•	CH 41 LOW
11	CH 42 HIGH	•	CH 42 LOW
12	CH 43 HIGH	•	CH 43 LOW
13	CH 44 HIGH	•	CH 44 LOW
14	CH 45 HIGH	•	CH 45 LOW
15	CH 46 HIGH	•	CH 46 LOW
16	CH 47 HIGH	•	CH 47 LOW
17	CH 48 HIGH	AGND	CH 48 LOW
18	CH 49 HIGH	•	CH 49 LOW
19	CH 50 HIGH	•	CH 50 LOW
20	CH 51 HIGH	•	CH 51 LOW
21	CH 52 HIGH	•	CH 52 LOW
22	CH 53 HIGH	•	CH 53 LOW
23	CH 54 HIGH	•	CH 54 LOW
24	CH 55 HIGH	•	CH 55 LOW
25	CH 56 HIGH	•	CH 56 LOW
26	CH 57 HIGH	•	CH 57 LOW
27	CH 58 HIGH	•	CH 58 LOW
28	CH 59 HIGH	•	CH 59 LOW
29	CH 60 HIGH	•	CH 60 LOW
30	CH 61 HIGH	•	CH 61 LOW
31	CH 62 HIGH	AGND	CH 62 LOW
32	CH 63 HIGH	•	CH 63 LOW

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Figure 2-4 P4 Connector Pin Configuration



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Table 2-10 P4 Connector (Front Panel Inputs) Signal Assignments

Pin	Row A	Row B	Row C
01	CH 00 HIGH	•	CH 00 LOW*
02	CH 01 HIGH	•	CH 01 LOW
03	CH 02 HIGH	AGND	CH 02 LOW
04	CH 03 HIGH	•	CH 03 LOW
05	CH 04 HIGH	•	CH 04 LOW
06	CH 05 HIGH	•	CH 05 LOW
07	CH 06 HIGH	•	CH 06 LOW
08	CH 07 HIGH	•	CH 07 LOW
09	CH 08 HIGH	•	CH 08 LOW
10	CH 09 HIGH	•	CH 09 LOW
11	CH 10 HIGH	•	CH 10 LOW
12	CH 11 HIGH	•	CH 11 LOW
13	CH 12 HIGH	•	CH 12 LOW
14	CH 13 HIGH	•	CH 13 LOW
15	CH 14 HIGH	•	CH 14 LOW
16	CH 15 HIGH	AGND	CH 15 LOW
17	CH 16 HIGH	•	CH 16 LOW
18	CH 17 HIGH	•	CH 17 LOW
19	CH 18 HIGH	•	CH 18 LOW
20	CH 19 HIGH	•	CH 19 LOW
21	CH 20 HIGH	•	CH 20 LOW
22	CH 21 HIGH	•	CH 21 LOW
23	CH 22 HIGH	•	CH 22 LOW
24	CH 23 HIGH	•	CH 23 LOW
25	CH 24 HIGH	•	CH 24 LOW
26	CH 25 HIGH	•	CH 25 LOW
27	CH 26 HIGH	•	CH 26 LOW
28	CH 27 HIGH	•	CH 27 LOW
29	CH 28 HIGH	•	CH 28 LOW
30	CH 29 HIGH	•	CH 29 LOW
31	CH 30 HIGH	AGND	CH 30 LOW
32	CH 31 HIGH	•	CH 31 LOW

* For pseudo-differential input, P4-C1 is the low-side (GND) reference for all input channels. Refer to "Connector Descriptions" on page 51 for pseudo-differential input description.

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CHAPTER

3

Programming

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Controlling and Reading the Analog-to-Digital Converter Data 65
Changing A/D Operating Modes 71
Program Example 74

Introduction

Communication with the VMIVME-3113A takes place through 128 contiguous, 16-bit register locations which are mapped into the VME short I/O address space. Most VMEbus CPUs access the short I/O space as if it were a 64-Kbyte block of conventional memory. Consult your CPU manual to determine the address of this block.

The VMIVME-3113A supports byte and word (16-bit) accesses. The order of the bytes within a word depends on the model of CPU used. For instance, most 68000-based CPUs put the most significant byte at the same address as the word. The least significant byte is at the next address. When registers are described as words here, this byte order is used. Note that if the AUTOSCAN data is read in two separate byte reads, they may be from different conversion cycles. This can introduce a large error in the reading.

Functions of the communications registers, which are discussed in detail within this section, are summarized in Table 3-1 on page 60. Some of the registers are not used, and are labeled "reserved". Reserved registers may be duplicate mappings of normal Control Registers. They should not be used, since they could be affected by a design change. Location 0 (word) simply reads the constant 11xx HEX. This is the board ID.

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Control and Status Register Descriptions

The register located at relative address 02H is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

- Analog input channel selection
- A/D operating modes
- Start A/D conversion
- Start Programmable Timer
- Two's complement selection
- Front panel Fail Indicator
- Board RESET
- Gain Delay

The CSR is 16 bits in length, and is detailed in Table 3-2 on page 61 and Table 3-3 on page 62. The function of each control bit and status flag is described in detail, subsequently, in the associated programming discussions.

Table 3-1 VMIVME-3113A Register Map

Relative Address		Register Name
HEX	**DEC**	
00	00	Board ID constant ($11xx)
02	02	Control and Status (CSR)
04	04	Configuration (CFR)
06-0E	06-14	(Reserved)
10	16	Interrupt Control (ICR)
12-16	18-22	(Reserved)
18	24	Interrupt Vector (IVR)
1A-1E	26-30	(Reserved)
20	32	Timer 0 (TR0)
22	34	Timer 1 (TR1)
24	36	Timer 2 (TR2)
26	38	Timer Control (TCR)
28-2E	40-46	(Reserved)
30	48	Random Conversion Data (RCDR)
32-7E	50-126	(Reserved)
80	128	Scan Data Channel 0
82-FC	130-252	Scan Data for Channels 1-62, respectively
FE	254	Scan Data Channel 63

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Table 3-2 Control Register Functions

Control Register, Byte 2 (MSB)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
GAIN DELAY	LED OFF	START CONV	TWO'S COMPL	ENA EXT STRT	TIMER START	SOFTWARE RESET	MODE 2

Control Register, Byte 3 (LSB)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
MODE 1	MODE 0	MUX A5	MUX A4	MUX A3	MUX A2	MUX A1	MUX A0

Control Register Bit Definitions:

Bit D15 — GAIN DELAY — When this bit is set, the Analog Input Acquistion time increases from 15 to 28µs. This bit should be set when a gain of 500 is selected on the Programmable Gain Amplifier.

Bit D14 — LED OFF — The FAIL LED is OFF if this bit is set to "one", and is ON if the bit is "zero".

Bit D13 — START CONV — A single A/D conversion or conversion scan is enabled each time a "one" is written to this control bit and an ADC RANDOM POLLING/INTERRUPT or SCANNING POLL/INTERRUPT OPERATING MODE is selected by D6 through D8.

Bit D12 — TWO'S COMPL — ADC coding format is offset binary if D12 is low "zero", or two's complement if D12 is high "one". For Unipolar: D12=0 is Straight Binary (recommended).

Bit D11 — ENA EXT STRT — When D11 is set high "one", the on-board external A/D start logic is enabled to accept an external trigger.

Bit D10 — TIMER START — When D10 is set high "one", the Programmable Timer starts counting if it has been previously programmed.

Bit D09 — SOFTWARE RESET — When D9 is set high "one", all on-board A/D timing networks are cleared. This must be done when changing operating modes. D9 must be cleared to end the reset.

Bits D08 through D6 — MODE 2, MODE 1 and MODE 0 — These three bits specify 1 of 6 ADC operating modes.

D8	D7	D6	
0	0	0	AUTO SCANNING MODE
0	0	1	RANDOM POLLING MODE
0	1	1	RANDOM INTERRUPT MODE
0	1	0	SCANNING POLL MODE
1	0	0	SCANNING INTERRUPT MODE
1	1	1	AUTO SCANNING MODE with BIT

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Bit D05 through D00 MUX A5, MUX A4, MUX A3, MUX A2, MUX A1, MUX A0 — D0 through D5 select the analog input channel or the BIT reference voltage, and are active only in the RANDOM POLLING, RANDOM INTERRUPT and AUTO SCANNING with BIT modes.

Table 3-3 Status Register Flags

Status Register Data Format, Byte 2 (MSB)							
Bit D15	**Bit D14**	**Bit D13**	**Bit D12**	**Bit D11**	**Bit D10**	**Bit D09**	**Bit D08**
NEW DATA RDY	LED OFF	END OF SCAN	TWO'S COMPL	ENA EXT STRT	TIMER START	SOFTWARE RESET	MODE 2

Status Register Data Format, Byte 3 (LSB)							
Bit D07	**Bit D06**	**Bit D05**	**Bit D04**	**Bit D03**	**Bit D02**	**Bit D01**	**Bit D00**
MODE 1	MODE 0	MUX A5	MUX A4	MUX A3	MUX A2	MUX A1	MUX A0

Status Register Bit Definitions:

Bit D15 NEW DATA RDY — This flag, when read high "one", indicates that an A/D conversion of a single channel has been completed. Used only in RANDOM POLLING MODE. This flag clears when the RCDR is read.

Bit D14* LED OFF — The FAIL LED is OFF if this bit is set to "one", and is ON if the bit is "zero".

Bit D13 END OF SCAN — This flag, when read high "one", indicates that a single A/D scan of all channels has been completed. Used only in SCANNING POLL MODE. This flag clears when the next scan starts.

Bit D12* TWO'S COMPL — ADC coding format is offset binary if D12 is low "zero", or two's complement if D12 is high "one". For Unipolar: D12=0 is Straight Binary (recommended).

Bit D11* ENA EXT STRT — When D11 is set high "one", the on-board external A/D start logic is enabled to accept an external trigger.

Bit D10* TIMER START — When D10 is set high "one", the Programmable Timer starts counting if it has been previously programmed.

Bit D09* SOFTWARE RESET — When D9 is set high "one", all on-board A/D timing networks are cleared.

Bits D08 through D6* MODE 2, MODE 1 and MODE 0 — These three bits specify 1 of 6 ADC operating modes.

D8	D7	D6	
0	0	0	AUTO SCANNING MODE
0	0	1	RANDOM POLLING MODE
0	1	1	RANDOM INTERRUPT MODE
0	1	0	SCANNING POLL MODE
1	0	0	SCANNING INTERRUPT MODE
1	1	1	AUTO SCANNING MODE with BIT

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Bit D05 through D00*	MUX A5, MUX A4, MUX A3, MUX A2, MUX A1, MUX A0 — D0 through D5 select the analog input channel or the BIT reference voltage.

* These bits read back the corresponding CONTROL REGISTER bits.

Configuration Register

The VMIVME-3113A input range and gain are determined by jumpers in the analog circuitry. The configuration of these jumpers cannot be read. However, J5 and the Configuration Register (CFR) are provided to allow the software to determine the analog configuration of the board. D0 through D4 contain the status of the five jumpers of J5 (1 = not installed), which do not have any effect on the operation of the board. The following convention is assumed:

Table 3-4 Configuration Register Definition

BIT	FUNCTION
D15-D8	Undefined
D7-D5	Read as 0
D4	1 = Bipolar inputs (±10V, ±5V) 0 = Unipolar inputs (0 to +10V)
D3	1 = ±10V inputs 0 = ±5V inputs, 0 to 10V inputs
D2-D0	GAIN SETTING

D2	D1	D0	GAIN
0	0	0	X1
0	0	1	X10
0	1	0	X100
0	1	1	X200
1	0	0	X500

Refer to "Configuration Register Jumper" on page 48 for configuring J5 to encode CFR bits 0...4. The CFR is at board relative address $04. They can be used with a convention different from the above, or simply ignored.

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Initialization By Reset

When SYSTEM RESET is applied to the board, the Control Register and all Analog-to-Digital Converter (ADC) flags are cleared to the LOW state "zero". The board will AUTOSCAN when SYSTEM RESET is removed. An independent BOARD RESET can be generated by setting the SOFTWARE RESET control bit to a "one". The board will remain reset until the SOFTWARE RESET bit is cleared. SOFTWARE RESET is used when shifting from AUTOSCAN to the other modes (see "Changing A/D Operating Modes" on page 71).

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Controlling and Reading the Analog-to-Digital Converter Data

The VMIVME-3113A has a number of features which allow the board to be used in a variety of applications. The simplest mode of operation is the AUTOSCANNING MODE which is automatically entered at power up.

AUTOSCANNING MODE

This mode is entered at power up, or the CSR may be programmed to enter this mode. The AUTOSCANNING MODE allows the user to operate the board without setting any control bits in the CSR and without selecting each channel to be converted. On power-up, the VMIVME-3113A initiates a conversion on CH 0 and sequentially performs conversions through the last channel configured, then begins again at CH 0. After each conversion, the data for that channel is stored in a dual-port register which is also accessible to the VMEbus and may be read at any time. Jumper field J10 controls how many channels are scanned. Refer to "Configuration and Installation" on page 37 for the configuration of these jumpers. The gain amplifier must be set to a gain of "one" in the AUTOSCANNING MODE. A minimum of 16 channels must be scanned when filters are installed on the board. Refer to "Analog-to-Digital (ADC) Control and Timing" on page 26.

Every scan of the connected input channels results in digitized data written to the SCAN DATA registers, thus overwriting the data from the previous scan. Any time a read is performed the latest data is always received.

To enter the AUTOSCANNING MODE (automatically entered at power-up), the following CSR bits must be set to the states indicated:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	0	0

SCANNING POLL MODE

The SCANNING POLL MODE performs a single scan of the input channels, but stops the scanning process after the last channel has been digitized. The END OF SCAN flag (bit D13) is then set in the Status Register. Polling this bit allows the CPU board to determine when the scan has been completed and the SCAN DATA registers have updated data. Scans are normally started by writing a "one" to bit D13 of the control register (START CONV).

The Programmable Timer may be set to periodically generate a signal which starts the SCANNING POLL MODE. For example, the timer may be programmed to generate a pulse once every second which starts the scan. The CPU must still poll the END OF SCAN bit until it goes high, so the SCANNING INTERRUPT MODE is a better candidate for use with the timer. The timer programming considerations are discussed in "Programmable Interval Timer" on page 67.

To enter the SCANNING POLL MODE, the following CSR bits must be set to the states indicated:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	1	1

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SCANNING INTERRUPT MODE

The SCANNING INTERRUPT MODE, like the SCANNING POLL MODE, performs a single scan of the input channels, then stops operating. Instead of setting a flag bit in the Status Register, a signal is generated to the Bus Interrupter Module which generates a VMEbus Interrupt to the CPU board. The Bus Interrupter Module must have been previously programmed to generate this VMEbus Interrupt, and also to respond with an 8-bit vector during the Interrupt Acknowledge cycle generated by the CPU board. Programming of the Bus Interrupter Module is detailed in "Programming the Bus Interrupter Module (BIM)" on page 69.

The SCANNING INTERRUPT MODE can be used along with the Programmable Timer to perform periodic data logging. To do this, it is necessary to set up the timer and interrupter chips as described in "Programmable Interval Timer" on page 67, and "Programmable Interval Timer Programming Sequence" and "Programming the Bus Interrupter Module (BIM)" on page 69. The control word for the CSR must have bit 10 (TIMER START) set instead of bit 13 (START CONV). In addition to having low CPU overhead, this mode minimizes digital activity on the VMIVME-3113A during conversions.

To enter the SCANNING INTERRUPT MODE, the following CSR bits must be set to the states indicated:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
1	0	0

RANDOM POLLING MODE

The RANDOM POLLING MODE is the traditional method of controlling an A/D conversion. The CPU board writes to the Control Register selecting the channel to be converted using Control Register bits MUX A5 through MUX A0 (D5 through D0). The same control word sets the START CONV bit (D13), which starts the multiplexer acquisition, and ADC timing sequence which was detailed in "ADC Conversion and Timing" on page 29. The CPU must then poll the NEW DATA RDY bit (D15) in the Status Register. When this flag goes high, the A/D conversion is complete and the data has been stored in the Random Conversion Data Register (RCDR). The RCDR is at board relative address $30. The CPU board then reads this data and selects the next channel to be converted. This mode is useful when channels desired to be converted are not in sequential order; channels can be selected in a Random order. It is also useful when specific channels must be converted more often than others.

Each time a new channel is selected for A/D Conversion, the Mode Control bits must be set to the RANDOM POLLING MODE. The following CSR bits must be set to the states indicated:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	0	1

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RANDOM INTERRUPT MODE

The RANDOM INTERRUPT MODE operates the same as the RANDOM POLLING MODE described above. The only difference is the CPU is signaled when the A/D conversion is complete by a VMEbus Interrupt generated by the on-board Bus Interrupter Module. The Bus Interrupter Module must be programmed before the first conversion is completed. Refer to "Programming the Bus Interrupter Module (BIM)" on page 69 for more information on programming the Bus Interrupter Module. Each time a new channel is selected for A/D conversion, the Mode Control bits must be set to the RANDOM INTERRUPT MODE. The following CSR bits must be set to the states indicated:

MODE 2H (D8)	MODE 1H (D7)	MODE 0H (D6)
0	1	0

AUTOSCANNING MODE with BIT

This mode is identical to the AUTOSCANNING MODE, except that one of three internal reference voltages may replace the channel 00 input signal. To select the BIT mode, select the appropriate CSR control bits as follows:

Ref Voltage	Mode 2 (D8)	Mode 1 (D7)	Mode 0 (D6)	MUX A1 (D1)	MUX A0 (D0)
CH00	1	1	1	0	0
+4.980VDC	1	1	1	0	1
+0.4928VDC	1	1	1	1	0
+9.92mVDC	1	1	1	1	1

NOTE: The gain and input range should be taken into consideration when choosing a reference voltage.

Programmable Interval Timer

The timer chip lets the VMIVME-3113A do delayed or periodic scans. It works with the SCANNING INTERRUPT and SCANNING POLL modes. The 8254 PIT chip used has three 16-bit counters and six counter modes. For the VMIVME-3113A, the counters are a timer and two optional prescalers for the 8 MHz clock. The "RATE GENERATOR" mode is used for prescalers and periodic scans. The "HARDWARE TRIGGERED STROBE" mode is used for single, delayed scans. This section will cover only the straightforward, likely uses of the 8254.

When J7 is in the [5-6] position, counter 0 is the timer. There are no prescalers. To initialize this counter as a one-shot scan trigger, write $xx3A to the Timer Control Register. The TCR is at board relative address $26 (word access or $27 byte access). To make counter 0 a repeating trigger or prescaler, write $xx34 to the TCR.

When J7 is in the [3-4] position, counter 1 is the timer. Counter 0 is the prescaler. To initialize counter 1 as a one-shot scan trigger, write $xx7A to the TCR. To make counter 1 a repeating trigger or prescaler, write $xx74 to the TCR.

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When J7 is in the [1-2] position, counter 2 is the timer. Counters 0 and 1 are prescalers (multiply their counts). To initialize counter 2 as a one-shot scan trigger, write $xxBA to the TCR. To make counter 2 a repeating trigger, write $xxB4 to the TCR.

Although all three counters are initialized through the TCR, they are loaded through separate registers (TR0, TR1 and TR2). Each load requires two separate writes, since the 8254 is a byte-wide device. After any of the above control words is used, the targeted counter will route the first write to it to its least significant byte. The second write will go to the counter's MSB. Right-justify the data, i.e., $xxLL or $xxHH. The writes to TR0, TR1 and TR2 may be arbitrarily arranged as long as each counter is loaded LSB first.

Counter 0 decrements once every 125nsec. Its delay/period can reach 8.192msec. Counter 1 can reach 536 seconds, given a 8.192msec prescaler. Counter 2 can reach 35 million seconds, given a 536sec prescaler. Prescalers decrease timing resolution: the minimum step rises from 125nsec up to whatever the prescaler period is.

It is possible to latch and read the counters without affecting them. The first step is to write a counter latch command. Write $0000, $0040 or $0080 to the TCR in order to latch counter 0, 1 or 2, respectively. Read TR0, TR1 or TR2, respectively to get the low byte of the count. Read it again to get the high byte of the count. The count will remain latched until it is read even if a second latch command is issued.

Timed scans require bit 10 set and bit 13 reset in the Control Register. The PIT chip is ultimately controlled by CSR bit 10, "TIMER START". TIMER START must be high for the counters to run. A rising edge on TIMER START will restart each counter after the next clock pulse into that counter. This can be used to synchronize the VMIVME-3113A. Note that a counter loaded with N will require N+1 clocks to generate its first signal. RATE GENERATORS will run with a period of N after that.

For byte accesses, here are the timer register relative addresses (HEX): The TCR is at 27. TR0, TR1 and TR2 are at 21, 23 and 25, respectively. For word accesses, TR0, TR1 and TR2 are at 20, 22 and 24, respectively.

Programmable Interval Timer Programming Sequence

Table 3-5 below gives the address of each Counter Register and a description of the data to load into each register. Review "Interval Timer - 16-, 32- or 48-bit Timer Selection" on page 46 concerning the jumper installation on the cascading counters for maximum counter lengths of 16, 32 or 48 bits.

Table 3-5 Timer Programming Sequence

Counter Number	Load Sequence	Register Address (HEX)	Register Name	Data (HEX)	Max Interval
COUNTER 0	1 2 3	26 20 20	TCR TR0 TR0	$0034 or $003A LEAST SIGNIFICANT BYTE OF COUNT MOST SIGNIFICANT BYTE OF COUNT	8.192 milliseconds
COUNTER 1	1 2 3	26 22 22	TCR TR1 TR1	$0074 or $007A LEAST SIGNIFICANT BYTE OF COUNT MOST SIGNIFICANT BYTE OF COUNT	536.8 seconds
COUNTER 2	1 2 3	26 24 24	TCR TR2 TR2	$00B4 or $00BA LEAST SIGNIFICANT BYTE OF COUNT MOST SIGNIFICANT BYTE OF COUNT	35 megaseconds

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Count data must be right-justified, i.e., $00LL or $00HH.

Programming the Bus Interrupter Module (BIM)

The Bus Interrupter Module handles all interrupt interfacing to the VMEbus. An interrupt may be generated on any VMEbus level (1 through 7). Interrupts are generated when the BIM is programmed to do so and when one of the following two ADC operating modes are employed: RANDOM INTERRUPT MODE and SCANNING INTERRUPT MODE.

Two registers must be programmed to use the BIM. The Interrupt Vector Register (IVR) is at offset 18 HEX (19 for byte access). It simply holds the 8-bit vector which the BIM delivers to the interrupted CPU. The vector normally points to an interrupt handler address within a jump table.

The Interrupt Control Register (ICR) determines the level of the interrupt and whether the BIM is armed or not. ICR bits 0-2 encode the interrupt request level. Level 7 is the highest priority, level 1 is the lowest and 0 disables the BIM. The BIM is also disabled when ICR bit 4 is cleared. Bit 3, if set, makes the BIM automatically clear bit 4 (and disable itself) after each interrupt. If bit 3 is set, then the software must load the ICR to re-arm the BIM after each interrupt. This can be useful as a debugging aid or safety precaution.

The other ICR bits are straightforward. Bit 5 must be cleared. Bit 7 is a utility flag with no control function. Bit 6, if set, clears the bit 7 flag in the event of an interrupt. The ICR is at offset 10 HEX (11 for byte access).

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External Trigger Operation

The board may be programmed to respond to an external TTL pulse (active low or "zero" pulse required). A single A/D conversion or a scan of A/D conversions will be initiated in response to this trigger. First, the user selects the A/D mode to be used by writing to the CSR and selecting a RANDOM MODE or SCANNING MODE, but do not set the START CONV bit (D13) in the CSR. The control bit ENA EXT STRT (D11) must be set to a "one" instead. This will generate a TTL high (logic "one") out the P2 connector pin A31 to signal the external equipment that the board is ready to receive an External Trigger. An external logic level ("zero") trigger pulse of at least 100nsec may then be input to the board via the P2 connector pin A27. This will start the A/D conversion(s).

In addition to enabling the External Trigger operation, there are certain jumpers which must be installed to electrically connect the P2 connector pins to the External Trigger circuitry. Refer to "External Trigger Jumper Description" on page 46 for information on selecting these jumpers. Be aware that the P2 I/O pins are sometimes used by other boards to perform different I/O functions. This needs to be checked from a system viewpoint to verify there are not multiple drivers/receivers using these user-defined P2 I/O lines: P2-A31, A32, A27 and A28.

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Changing A/D Operating Modes

The board powers up in the AUTOSCANNING MODE. To switch the board from an autoscanning mode to a nonautoscanning mode, a software reset sequence must be used. The three steps of a reset sequence are: (1) write a word to the CSR setting the SOFTWARE RESET bit (D9) and the new mode (in D6, D7, D8), (2) write a word to the CSR clearing the SOFTWARE RESET bit but having the same new mode and (3) write a word to the CSR having the new mode and enabling/starting the conversion; i.e., set either START CONV (D13), ENA EXT STRT (D11) or TIMER START (D10). Table 3-6 below shows the sequences for switching from an autoscanning mode to each of the other four A/D operating modes. The table examples for the RANDOM POLL and RANDOM INT work for channels other than 0.

A software reset is not necessary when switching between the autoscanning modes (AUTOSCANNING, AUTOSCANNING with BIT). Neither is it necessary when switching from one of the RANDOM or SCANNING modes to any other mode. In these cases, (1) write a word to the CSR with the new mode in D6, D7 and D8 and (2) write a word to the CSR having the new mode and enabling/starting the conversion.

Table 3-6 below shows the proper sequence and control words to switch to the four other A/D operating modes.

Table 3-6 Control Word Sequence for Switching from AUTOSCANNING MODE

SWITCH FROM AUTOSCANNING MODE TO:	CONTROL WORD SEQUENCE (HEX)
RANDOM POLL MODE	1. 4240 (RESET TIMING NETWORK) 2. 4040 (REMOVE RESET) 3. 6040 (STARTS CONV. ON CH 0)
RANDOM INT. MODE	1. 4280 (RESET TIMING NETWORKS) 2. 4080 (REMOVE RESET) 3. 6080 (STARTS CONV. ON CH 0)
SCANNING POLL MODE	1. 42C0 (RESET TIMING NETWORKS) 2. 40C0 (REMOVE RESET) 3. 60C0 (STARTS CONV. ON CH 0)
SCANNING INT. MODE	1. 4300 (RESET TIMING NETWORKS) 2. 4100 (REMOVE RESET) 3. 6100 (STARTS A/D SCAN)

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Scan Data Register Description

The format of the data stored in the scan data registers depends on the setting of bit 12 in the Control and Status Register (CSR). If bit 12 equals zero and the range is uniploar, then use Table 3-7. If bit 12 equals one and the range is unipolar, then use Table 3-8. If bit 12 equals zero and the range is bipolar, use Table 3-9. If bit 12 equals one and the range is bipolar, use Table 3-10.

Table 3-7 Conversion for Unipolar Range in Straight Binary Format

Input	Unipolar Range		Straight Binary				Hex
	+5V V_{FSR}=5 V	±10 V_{FSR}=10 V	D15*			D00	
+FS - 1 LSB	+4.9988 V	+9.9976 V	0000	1111	1111	1111	FFF
3/4 FS	+3.7500 V	+7.5000 V	0000	1100	0000	0000	C00
1/2 FS	+2.5000 V	+5.0000 V	0000	1000	0000	0000	800
1/4 FS	+1.2500 V	+2.5000 V	0000	0100	0000	0000	400
1 LSB	+0.0012 V	+0.0024 V	0000	0000	0000	0001	001
Zero	0.0000 V	0.0000 V	0000	0000	0000	0000	000

Straight Binary: $V = V_{FSR}$ (D/4096)
D is the decimal equivalent of the Hex value

**= Zero for Binary or extended sign for 2's Complement*

Table 3-8 Conversion for Unipolar Range in 2's Complement Format

Input	Unipolar Range		2's Complement				Hex
	+5V V_{FSR}=5 V	+10 V_{FSR}=10 V	D15*			D00	
+FS - 1 LSB	+4.9988 V	+9.9976 V	0000	0111	1111	1111	7FF
3/4 FS	+3.7500 V	+7.5000 V	0000	0100	0000	0000	400
1/2 FS	+2.5000 V	+5.0000 V	0000	0000	0000	0000	000
1/4 FS	+1.2500 V	+2.5000 V	1111	1100	0000	0000	C00
1 LSB	+0.0012 V	+0.0024 V	1111	1000	0000	0001	801
Zero	0.0000 V	0.0000 V	1111	1000	0000	0000	800

2's Complement: $V = V_{FSR}$ (D1/4096) - $V_{FSR}/2$
D1 is the decimal equivalent of (Hex value ⊕ $800).

**= Zero for Binary or extended sign for 2's Complement*

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Table 3-9 Conversion for Unipolar Range in 2's Complement Format

Input	Unipolar Range		Offset Binary				
	±5V V_{FSR}=10 V	±10 V_{FSR}=20 V	D15*			D00	Hex
+FS - 1 LSB	+4.9976 V	+9.9951 V	0000	1111	1111	1111	FFF
+3/4 FS	+3.7500 V	+7.5000 V	0000	1110	0000	0000	E00
+1/2 FS	+2.5000 V	+5.0000 V	0000	1100	0000	0000	C00
+1/4 FS	+1.2500 V	+2.5000 V	0000	1010	0000	0000	A00
+1 LSB	+0.0024 V	+0.0048 V	0000	1000	0000	0001	801
Zero	0.0000 V	0.0000 V	0000	1000	0000	0000	800
-1/4 FS	-1.2500 V	-2.5000V	0000	0110	0000	0000	600
-1/2 FS	-2.5000 V	-5.0000 V	0000	0100	0000	0000	400
-3/4 FS	-3.7500 V	-7.5000 V	0000	0010	0000	0000	200
-FS + 1 LSB	-4.9976 V	-9.9951 V	0000	0000	0000	0001	001
-FS	-5.0000 V	-10.0000 V	0000	0000	0000	0000	000

Offset Binary: $V = V_{FSR}\ (D/4096) - V_{FSR}/2$

D is the decimal equivalent of the Hex value.

**= Zero for Binary or extended sign for 2's Complement*

Table 3-10 Conversion for Unipolar Range in 2's Complement Format

Input	Unipolar Range		2's Complement				
	±5V V_{FSR}=10 V	±10 V_{FSR}=20 V	D15*			D00	Hex
+FS - 1 LSB	+4.9976 V	+9.9951 V	0000	0111	1111	1111	7FF
+3/4 FS	+3.7500 V	+7.5000 V	0000	0110	0000	0000	600
+1/2 FS	+2.5000 V	+5.0000 V	0000	0100	0000	0000	400
+1/4 FS	+1.2500 V	+2.5000 V	0000	0010	0000	0000	200
+1 LSB	+0.0024 V	+0.0048 V	0000	0000	0000	0001	001
Zero	0.0000 V	0.0000 V	0000	0000	0000	0000	000
-1/4 FS	-1.2500 V	-2.5000V	1111	1110	0000	0000	E00
-1/2 FS	-2.5000 V	-5.0000 V	1111	1100	0000	0000	C00
-3/4 FS	-3.7500 V	-7.5000 V	1111	1010	0000	0000	A00
-FS + 1 LSB	-4.9976 V	-9.9951 V	1111	1000	0000	0001	801
-FS	-5.0000 V	-10.0000 V	1111	1000	0000	0000	800

2's Complement: $V = V_{FSR}\ (D1/4096) - V_{FSR}/2$

D is the decimal equivalent of (Hex value $\oplus$ $800).

**= Zero for Binary or extended sign for 2's Complement,* $\oplus$ = Exclusive OR'd with

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Program Example

The following example consists of three files: 3113A.h, example.c and eos.sa. The first two files are "C" code to demonstrate various modes. The third file is an interrupt handler written in 68000 assembly language to support the "C" code.

File example.c:

```
/*
**  VMIVME-3113A SCANNING ANALOG-TO-DIGITAL BOARD
**
**  Assumes use of Force CPU-33 with VMEPROM (pdos).
**
**  example program outline:
**
**  > Example exit AUTOSCAN mode (power on default mode).
**  > Example TIMER initialization.
**  > Example SCANNING POLL mode with EXTERNAL START.
**  > Example SCANNING INTERRUPT mode with Timer.
**  > Example RANDOM POLL mode.
**  > Example re-enter AUTOSCAN mode.
**  > Example dump of above data.
**  > End example program.
**  > Interrupt handler example (in assembler).
*/

#include  <stdio.h>
#include  "3113A.h"

/*
**  declare global pointer to board
**
**  Force CPU-33 short io space is  $fbff0000 ~ $fbffffff.
**  VMIVME-3113A board base address (jumpers) is $0000.
**  (short io space) + (board base address)  =  $fbff0000.
*/


Vmic3113A * board = (( Vmic3113A * )( 0xfbff0000 ));


/*
** declare global 3113A data storage arrays (for mode examples)
*/


unsigned short  scan_poll_data[64],       /* scanning poll mode data */

                scan_intr_data[64],       /* scanning intr mode data */

                rand_poll_data[64];       /* random poll mode data */


/*
**  declare external functions (in this case interrupt handlers)
*/

void  eos( void );    /* end of scan interrupt service */

extern int eos_flag;  /* end of scan flag */
```


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```
/*
**  declare miscellaneous vars and constants
*/

unsigned  short soft_csr;           /* csr image */

unsigned  int loop;          /* general loop var */


main()
{
   /*
   **  Example exit (default) autoscan mode
   */

   board->csr = ( FAIL_LED_OFF | SCANNING_POLL );

   /*
   **  Example timer initialization  ( see manual for details ).
   **
   **  set up timer 0 for 1 msec rate generator and cascade that
   **  into timer 1 which is set up for 1000 counts and generate
   **  a strobe. So 1000 X 1 msec = 1 second.
   */

   board->tmc = ( SELECT_COUNTER_0 | RW_LSB_MSB |
                    RATE_GENERATOR | BINARY_COUNTER );



   board->tm0 = 0x40;      /* 8000 = $1f40 = 1 msec lsb/msb */
   board->tm0 = 0x1f;

   board->tmc = ( SELECT_COUNTER_1 | RW_LSB_MSB | SOFT_TRIG_STROBE |
                    BINARY_COUNTER );

   board->tm1 = 0xe8;      /* 1 sec = 1000 msec = $3e8 lsb/msb */
   board->tm1 = 0x03;

   /*
   ** Example scanning poll mode with external start.
   **
   ** set up a scan which is started by external trigger.
   ** The end will be determined by polling END OF SCAN.
   ** Starting the scan requires EXT_START_CONVERT_L signal to
   ** go low momentarily. (Shorting to ground with a clip lead
   ** should suffice. See manual for electrical precautions).
   ** (also do software reset - see manual for details).
   */

   printf("\r\n\nPlease provide external trigger input ... ");

   board->csr = ( FAIL_LED_OFF | SOFTWARE_RESET | SCANNING_POLL );
   board->csr = ( FAIL_LED_OFF | EN_EXTERNAL_START | SCANNING_POLL );


   /***  note:

   The following two lines can be used to start convert without using the hardware
   signal mentioned in the comment above ...

   board->csr = ( FAIL_LED_OFF | SCANNING_POLL );
   board->csr = ( FAIL_LED_OFF | START_CONVERT | SCANNING_POLL );
```


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```
***/

while( board->csr & END_OF_SCAN );        /* wait for status cleared */

while( ! ( board->csr & END_OF_SCAN ));   /* wait for status set */

printf("thank you\r\n");

/*
**  on end of scan move data from the channel buffers into
**  the scan_poll_data array.
*/

for( loop = 0; loop < 64; loop++ )
scan_poll_data[loop] = board->chan[loop];

/*
** Example scanning interrupt mode with timer start
**
**  The end will be signaled by an interrupt. Interrupts
**  are system dependent and requires your understanding

**  of your particular system. The interrupt service
**  routine for this example (shown later) moves the data
**  into the scan_intr_data array.
*/

board->ivr = 0x54;  /* first available user vector on Force CPU-33 */

setvect( 0x54, &eos );         /* install vector with system call */

board->icr = ( INTERRUPT_ENABLE | INTR_AUTO_CLEAR | REQUEST_LEVEL_5 );

board->csr = ( FAIL_LED_OFF | TIMER_START | SCANNING_INTERRUPT );

while( ! ( eos_flag ));  /* do nothing until you see eos flag */
eos_flag = 0;            /* clear eos flag for another pass   */



/*
**  Example random poll mode (single conversions)
*/

soft_csr = ( FAIL_LED_OFF | START_CONVERT | RANDOM_POLL );

for( loop = 0; loop < 64; loop++ ) {        /* channel loop */

     board->csr = soft_csr;              /* start conversion */

     while( ! ( board->csr & NEW_DATA_READY ));       /* wait */

     rand_poll_data[loop] = board->word_reg[0x15]/* save data */

     soft_csr++;                     /* point to next channel (mux) */
}

/*
**  Example return to autoscan mode dump data and exit
*/

board->csr = ( FAIL_LED_OFF );
```


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```
    /*
    **  Dump example mode data arrays
    **
    **  assumes that sixteen data words with a single space
    ** after each will fit evenly on a line of the terminal
    ** then wrap to the next line (auto wrap mode).
    */

    printf("\r\n\n\nDumping scanning poll mode data: \r\n\n");

    for( loop = 0; loop < 64; loop++ )
    printf("%.4X ", scan_poll_data[ loop ] );


    printf("\r\n\nDumping interrupt poll mode data: \r\n\n");

    for( loop = 0; loop < 64; loop++ )
         printf("%.4X ", scan_intr_data[ loop ] );

    printf("\r\n\n\nDumping random poll mode data: \r\n\n");

    for( loop = 0; loop < 64; loop++ )
    printf("%.4X ", rand_poll_data[ loop ] );

} /* end main */
```


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File 3113A.h:

```
/*
**  VMIVME-3113A SCANNING 12-bit ANALOG-TO-DIGITAL WITH BUILT-IN-TEST
*/

struct vmivme_3113A_registers {
    union {
        unsigned char  byte_reg[128/1];
        unsigned short word_reg[128/2];
    } offset;
    unsigned short chan[128];
};

typedef struct vmivme_3113A_registers Vmic3113A;

#define    bid         offset.word_reg[0x00/2]     /* board id register */
#define    csr         offset.word_reg[0x02/2]     /* control and status register */
#define    cfr         offset.word_reg[0x04/2]     /* configuration register */
#define    icr         offset.byte_reg[0x11/1]     /* interrupt control register */
#define    ivr         offset.byte_reg[0x19/1]     /* interrupt vector register */
#define    tm0         offset.byte_reg[0x21/1]     /* timer count 0 register */
#define    tm1         offset.byte_reg[0x23/1]     /* timer count 1 register */
#define    tm2         offset.byte_reg[0x25/1]     /* timer count 2 register */
#define    tmc         offset.byte_reg[0x27/1]     /* timer control register */

#define    VALID_3113A_ID                0x0000   /* board id */

#define    GAIN_DELAY                    0x8000   /* csr control bit def's */
#define    FAIL_LED_OFF                  0x4000
#define    START_CONVERT                 0x2000
#define    TWO'S_COMPLEMENT              0x1000
#define    EN_EXTERNAL_START             0x0800
#define    TIMER_START                   0x0400
#define    SOFTWARE_RESET                0x0200
#define    AUTOSCAN_BIT                  0x01C0
#define    SCANNING_INTERRUPT            0x0100
#define    SCANNING_POLL                 0x00C0
#define    RANDOM_INTERRUPT              0x0080
#define    RANDOM_POLL                   0x0040
#define    AUTOSCANNING                  0x0000
#define    BIT_4                         0x0003
#define    BIT_3                         0x0002
#define    BIT_2                         0x0001
#define    BIT_1                         0x0000
#define    MUX_CH0                       0x0000
#define    MUX_END                       0x003E

#define    NEW_DATA_READY                0x8000   /* csr status bit def's */
#define    END_OF_SCAN                   0x2000   /* where diff from ctrl */

#define    FLAG_BIT                      0x80     /* BIM control bits */
#define    FLAG_AUTO_CLEAR               0x40
#define    EXTERNAL_VECTOR               0x20

#define   INTERRUPT_ENABLE               0x10
#define   INTR_AUTO_CLEAR                0x08
#define   REQUEST_LEVEL_7                0x07
#define   REQUEST_LEVEL_6                0x06
#define   REQUEST_LEVEL_5                0x05
#define   REQUEST_LEVEL_4                0x04
#define   REQUEST_LEVEL_3                0x03
#define   REQUEST_LEVEL_2                0x02
#define   REQUEST_LEVEL_1                0x01
#define   INTERRUPTS_OFF                 0x00
```


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```
#define   READ_BACK_COMMAND             0xC0    /* tmc bit def's */
#define   SELECT_COUNTER_2              0x80
#define   SELECT_COUNTER_1              0x40
#define   SELECT_COUNTER_0              0x00
#define   RW_LSB_MSB                    0x30
#define   RW_MSB                        0x20
#define   RW_LSB                        0x10
#define   LATCH_COUNTER                 0x00
#define   HARD_TRIG_STROBE              0x0a
#define   SOFT_TRIG_STROBE              0x08
#define   SQUARE_WAVE                   0x06
#define   RATE_GENERATOR                0x04
#define   HARD_TRIG_ONE_SHOT            0x02
#define   INTR_ON_TERM_COUNT            0x00
#define   BCD_COUNTER                   0x01
#define   BINARY_COUNTER                0x00
```


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File eos.sa:

```
*
* interrupt service routine example for End_of_scan (eos)
*
* note: the C compiler we are using prefixes all labels with
*       an underbar. So we must do that in our assembler code
*       so when the programs are linked the labels can be found.
*
            xdef        _eos                    end of scan intr svc
            xdef        _eos_flag               end of scan flag

            xref        _board                  assumes global board in main
            xref        _scan_intr_data         assumes global ...

icr         equ         $11                     offset to intr ctrl reg
ch0         equ         $80                     offset to chan data reg's

            section     code

_eos        movem.l     a0-a2/d0,-(a7)          preserve registers
            move.l      _board,a0               get board address (ptr)
            move.l      a0,a1                   into a1 also so we can
            adda.l      #ch0,a1                 point to channel start

            lea         _scan_intr_data,a2      get data storage address (label)
            move.l      #64-1,d0                64 chan - 1 for dbf
bm          move.w      (a1)+,(a2)+             move channel data to data
            dbf         d0,bm                   storage at adc_data
            bset        #4,(icr,a0)             re-arm interrupt
            move.l      #-1,_eos_flag           set end of scan TRUE;
            movem.l     (a7)+,a0-a2/d0          restore registers
            rte                                 and return from exception

            section     ram

_eos_flag   dc.l        0                       end of scan flag
```


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Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

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Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.

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