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VMIVME-4100

16-CHANNEL 12-BIT DIGITAL-TO-ANALOG CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-004100-000

Revised April 21, 1992

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	03/06/86	Entire Manual	Manual - 01
B	11/06/86	Schematic	4100 - 05
C	03/25/87	P. 2-3, P. 4-1, Cover, and Record of Revisions Page	4100 - 07
D	09/30/88	Update Appendix A	88-0091
E	10/19/88	Update Appendix A	88-0194
F	11/06/88	Revise Manual	88-0319
G	05/03/89	Cover, pages ii, vi, vii, 3-2, 3-6, 3-10, 3-11, 5-5, 5-8, 5-10, Section 6, and Appendix A. Reformat Manual.	89-0017
H	08/14/89	Cover, page ii, Appendix A	89-0083
J	10/12/90	Cover, pages ii, and Appendix A	89-0195
K	10/12/90	Cover, pages ii, 4-4, and Appendix A	90-0137
L	03/12/91	Cover, page ii, Appendix A	91-0029
M	05/28/91	Cover, page ii, vii, Section 2, page 3-2, Section 5 and 6, and Appendix A	91-0148
N	12/19/91	Cover, pages ii, 2-7, and Appendix A	91-0320
P	01/24/92	Cover, page ii, and Appendix A	92-0015
R	04/21/92	Cover, page ii, Sections 2 and 6, and Appendix A	92-0110

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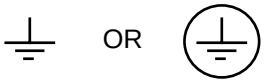
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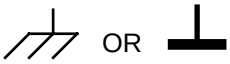
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



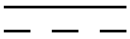
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



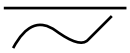
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

```
**************
*  CAUTION   *
**************
```

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

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VMIVME-4100
16-CHANNEL 12-BIT DIGITAL-TO-ANALOG CONVERTER BOARD

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A Assembly Drawing, Parts List, and Schematic

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SECTION 1

VMIVME-4100 16 CHANNEL 12-BIT DIGITAL-TO-ANALOG CONVERTER BOARD

1.1 INTRODUCTION

The VMIVME-4100 16-Channel 12-Bit Digital-to-Analog Converter (DAC) Board delivers ±10 V outputs with positive true offset binary input coding. The DAC Board features double buffered data latches, buffered voltage outputs, and selectable external or internal update control strobes. The DAC Board may be ordered with Built-in-Test hardware that can isolate the 16 analog outputs from field connections during diagnostic testing. In the test mode analog outputs are multiplexed to an analog test bus on the VME P2 backplane (user I/O pins) for analog-to-digital conversion by VMIC's Analog-to-Digital Converter (ADC) Board (VMIVME-3100). A front panel Fail LED is provided for quick fault location identification. The DAC Board is shown in Figure 1.1-1.

This document will primarily describe the operation of the DAC Board, but some details of the VMIVME-3100 12-Bit ADC Board and the VMIVME-3200 32-Channel Multiplexer Board will be included for clarity. It is also intended to give the user a better understanding of the test capabilities of a data acquisition system using the DAC Board in conjunction with the VMIC MUX Expander Board, (VMIVME-3200) and the ADC Board, (VMIVME-3100).

For a thorough understanding the reader should have access to the following documents:

VMIVME-3200 32 Channel Analog Input Instruction Manual, Document No. 500-003200-000

VMIVME-3100 12-Bit Analog-to-Digital Converter Board Instruction Manual Document No. 500-003100-000

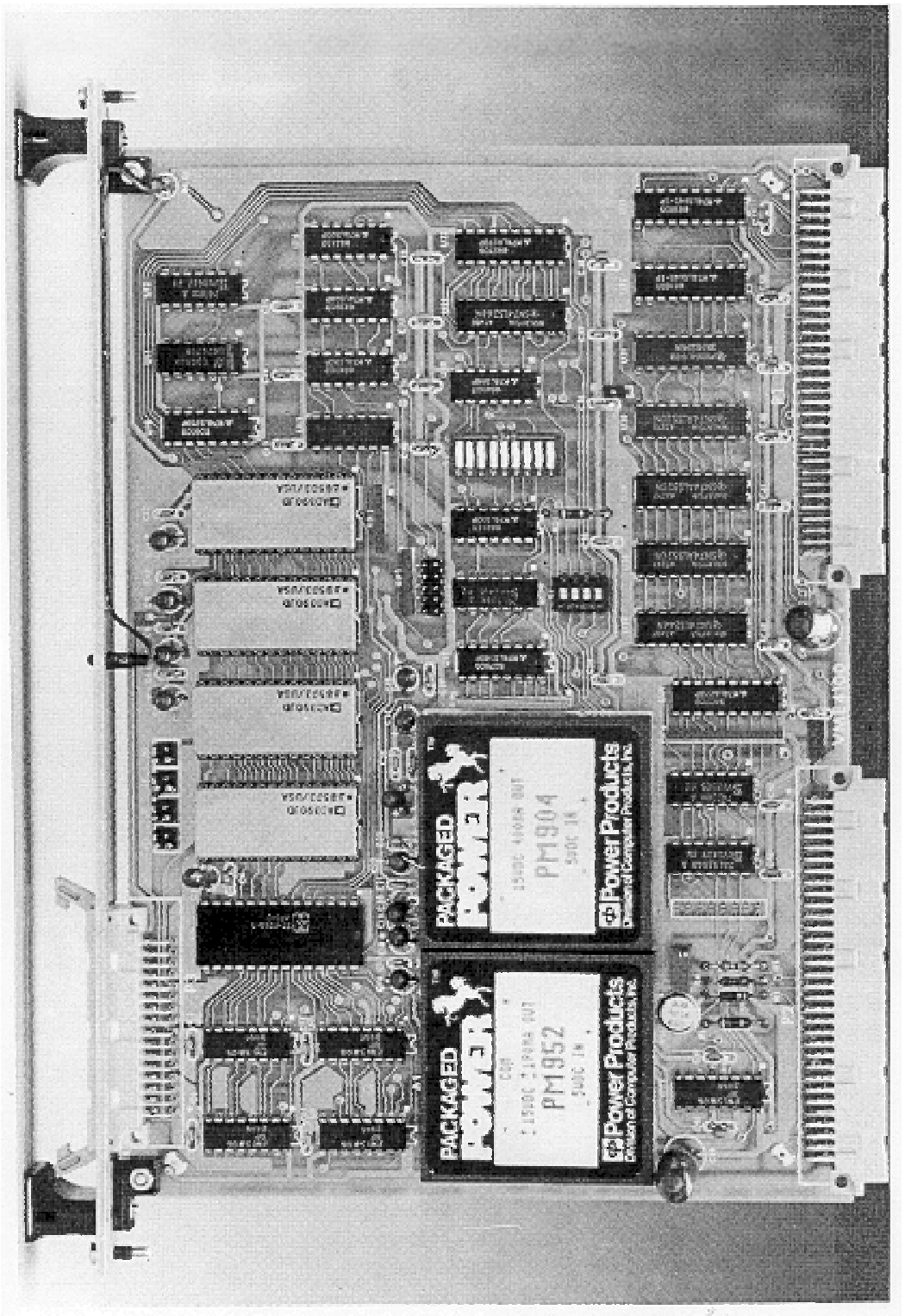
VMIC Analog Input/Output Products (with Built-in-Test) Configuration Guide, Document No. 825-000000-005

1.2 VMIVME-4100 12-BIT DAC BOARD BRIEF OVERVIEW

The primary features of the 4100 DAC Board are as follows:

a. Buffered voltage output
b. Double buffered data latches

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M4100/F1.1-1

Figure 1.1-1. 16-Channel DAC Board

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c. 16 channels per card
d. 12-bit DACs
e. Front panel Fail LED
f. High reliability Din type 96-pin I/O connectors
g. Multiplexed programmable outputs for testing analog input multiplexer cards
h. Multiplexed programmable outputs for testing analog outputs
i. Individually keyed VME connector design
j. Double Eurocard form factor
k. All 16 DAC outputs can be updated by one of the following three user selectable methods:
   (1) Each DAC can be immediately updated when a 12-bit positive true offset binary word is written to the DACs address.
   (2) Any DAC may be loaded with new data and then be converted some time later by the user under program control.
   (3) Any DAC that has been previously loaded with new data may be updated by an external TTL compatible device.
l. 5 mA output drive current
m. Single +5 V supply operation
n. Factory trimmed gain and offset - requires no calibration

A unique feature of the VMIVME-4100 is the Built-in-Test logic that allows the testing of any one of the analog output channels through the use of an on-board multiplexer and the VMIVME-3100 ADC Board. When in test mode, the field connections through connector P3 may be isolated and any of the 16 channels may be routed to the 12-bit ADC Board via VMIC's Analog Backplane (AMXbus™). An ADC Board under program control may have the analog signal converted to a 12-bit digital word and compared with the original 12-bit word written to the DAC Board. In this manner, each of the 16 analog output channels may be verified without disturbing the field connected devices. The analog output channels may also be multiplexed to the Analog Test Bus, simultaneously controlling the P3 connected field devices, providing real-time fault detection of the outputs. If a board fails its self-test, a Fail LED on the front panel may be turned on to indicate the board is in a failed condition. The complete operation and requirements for the self-test mode are explained in detail in this manual in Section 3, Theory of Operation, and Section 4, Programming.

1.3 REFERENCE MATERIAL

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

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VMEbus International Trade Association
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Scottsdale, AZ 85253
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The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Change of State Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006
Low Level Analog I/O Configuration Guide	825-000000-001
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004100-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The Digital-to-Analog Converter (DAC) Board performs digital-to-analog conversion on 12-bit positive true offset binary input coded words, with an analog output range of -10 to +10 volts. This provides for a resolution of 4.88mV for each digital input of 1 LSB change. The buffered output voltage settles to within 1/2 LSB in 8 microseconds (max).

The VMIVME-4100 offers high channel density by using four quad 12-bit Digital-to-Analog (DA) Converters. A Control Status Register (CSR) is loaded by the processor, and this register controls the functioning of the board. The CSR can be read by the processor at any time. The DAC Board block diagram is shown in Figure 3.1-1, and the four quad DACs are represented in Figure 3.1-2.

Each of the 16 DACs is preceded by double-buffered data latches. The data latches allow versatility in the way that DAC analog output may be updated.

There are three methods by which new data can be converted by a DAC. Each method is enabled/disabled by on-board jumpers and is further controlled by a control register that must be loaded by the user. The control register contents are described in Tables 4.2.2-2 and 4.2.2-3, pp. 4-5 and 4-6.

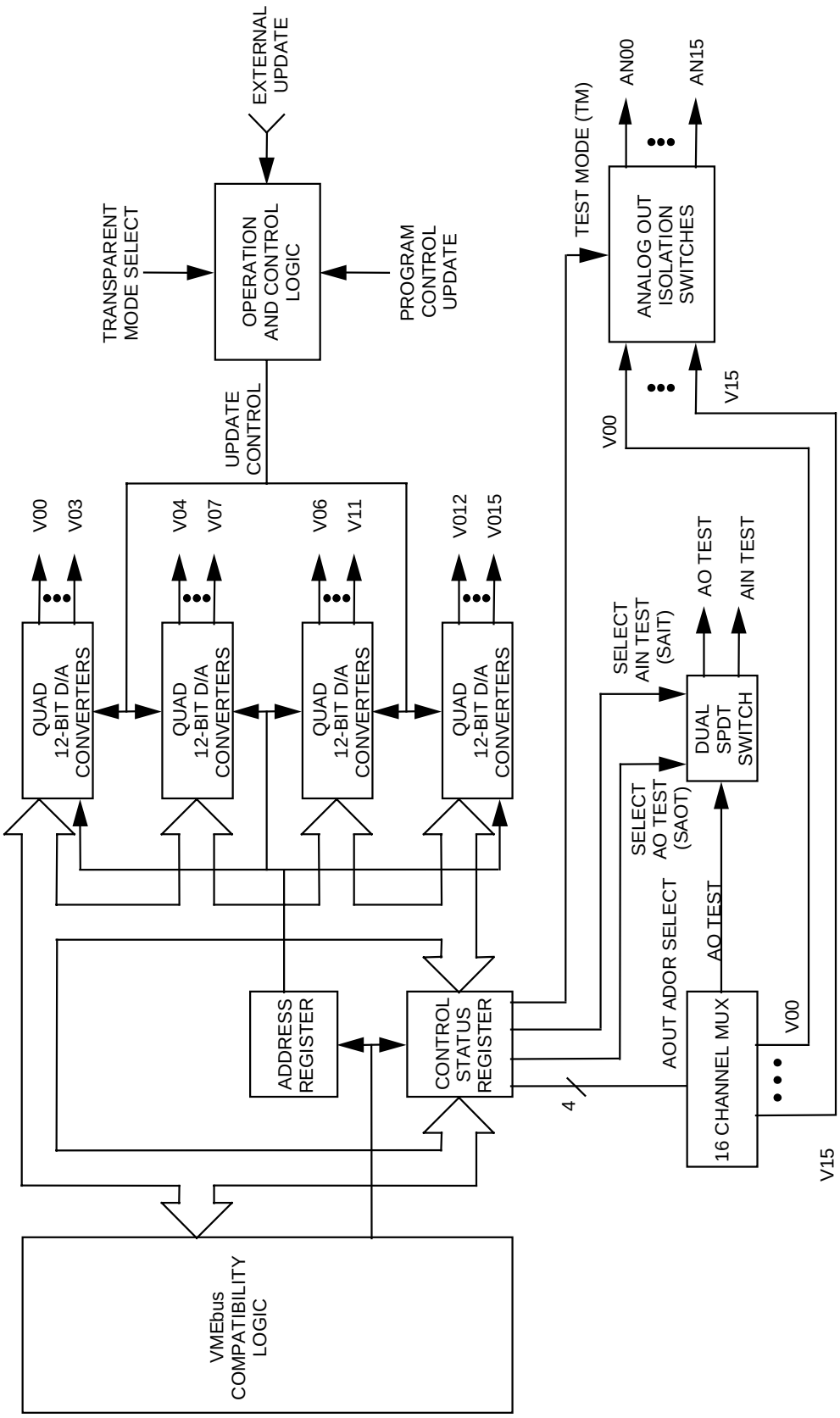
3.2 IMMEDIATE DAC UPDATE MODE

The processor unit sends the 12-bit word to be converted to the first register of the selected DAC. If that DAC channel has previously been jumpered to, it will automatically pass the contents of the first DAC register into the second register and update the analog output. There are four jumpers, each one enables/disables four DAC channels to be in the immediate update mode, as described above, or the delayed update mode, as described below. Jumper definition and locations are described in Section 5.7.

3.3 DELAYED DAC UPDATE MODE

In the delayed DAC update mode, the processor sends the 12-bit word to be converted to the first DAC register of the selected DAC. The data is stored there and transferred to the second DAC register in one of two possible methods, as described in Sections 3.3.1 and 3.3.2.

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M4100/F3.1-1

Figure 3.1-1. VMIVME-4100 Board

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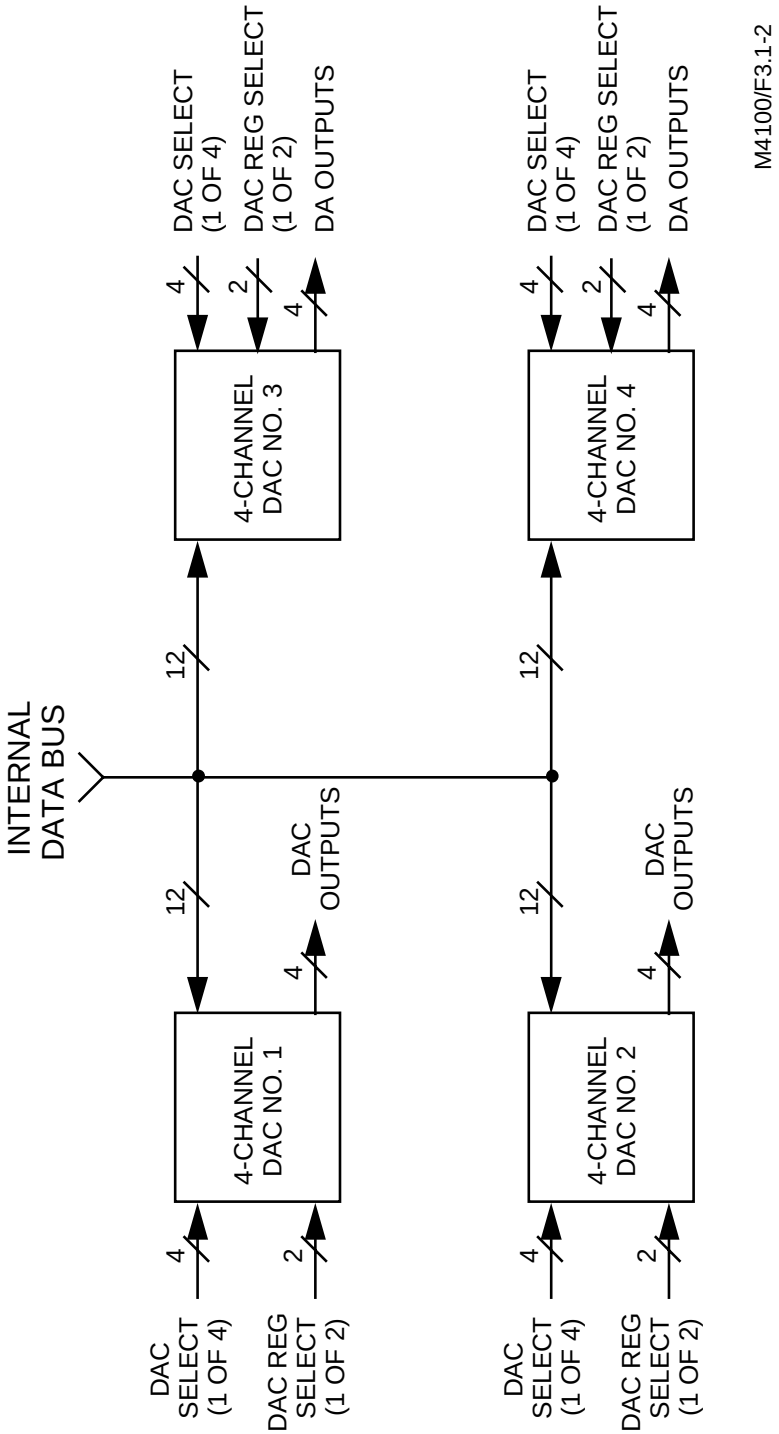


Figure 3.1-2. Analog Output Isolation Switches

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3.3.1 Program Control Update

One way for the transfer to occur is writing a specified control bit to the control register. When the data is transferred to the second register, digital-to-analog conversion begins and the analog output settles to within 1/2 LSB in 8 microseconds. Maximum load capacitance is 300 pf. This method of updating the analog output under program control is useful when more than one DAC channel output is desired to change at a precise time. All 16 DAC outputs could be synchronized to change at certain periodic intervals under software control.

3.3.2 External Trigger Update

The second method to update the second storage register, and therefore the DAC output, is by an external TTL compatible trigger. This trigger must first be enabled to be received by the external trigger circuitry by installing an on-board jumper, as described in Section 5.8. When the external trigger is received active low for a minimum of 150ns, then the value stored in the first DAC register will be transferred to the second DAC register to begin conversion. Using this method of update, all conversions can be synchronized to an external device.

3.4 VMIVME-4100 TEST MODE DESCRIPTION

The test mode hardware is optional (refer to VMIC's Price Guide for options) and is only needed when the VMIVME-4100 is used along with the VMIVME-3100 12-bit ADC Board as a minimum and possibly the VMIVME-3200 Multiplexer Board. Both of these boards support the Built-in-Test capabilities of the DAC Board and will be further explained here. A typical data acquisition configuration with Built-in-Test capabilities is shown in Figure 3.4-1. Up to 16 multiplexer boards or 16 DAC Boards may be interconnected with one VMIVME-3100 Analog-to-Digital Converter (ADC) Board. Thus, a single chassis system could accommodate 528 single-ended analog inputs or 256 analog outputs.

If testing the accuracy of the analog output channels of the DAC Board is desired, then a VMIVME-3100 ADC Board is required. These two boards must exist in the same VMIC (P2) Analog Backplane, VMIC has a low-noise Analog Multiplexer Bus Backplane (AMXbus™). The AMXbus™ Backplane is available in 5-, 9-, and 19-slot widths to accommodate different analog I/O sizing requirements.

The AMXbus™ allows DAC analog outputs to be routed to the VMIVME-3100 A/D where they can be digitized and compared with the 12-bit word originally written to the DAC Board. This digital-to-analog back-to-digital wrapback test can be done with the field devices (at P3 connector) connected or disconnected. This is accomplished by analog isolation switches (Figure 3.4-2) at the output of the DACs. These switches are turned ON or OFF by the outputs of the on-board CSR.

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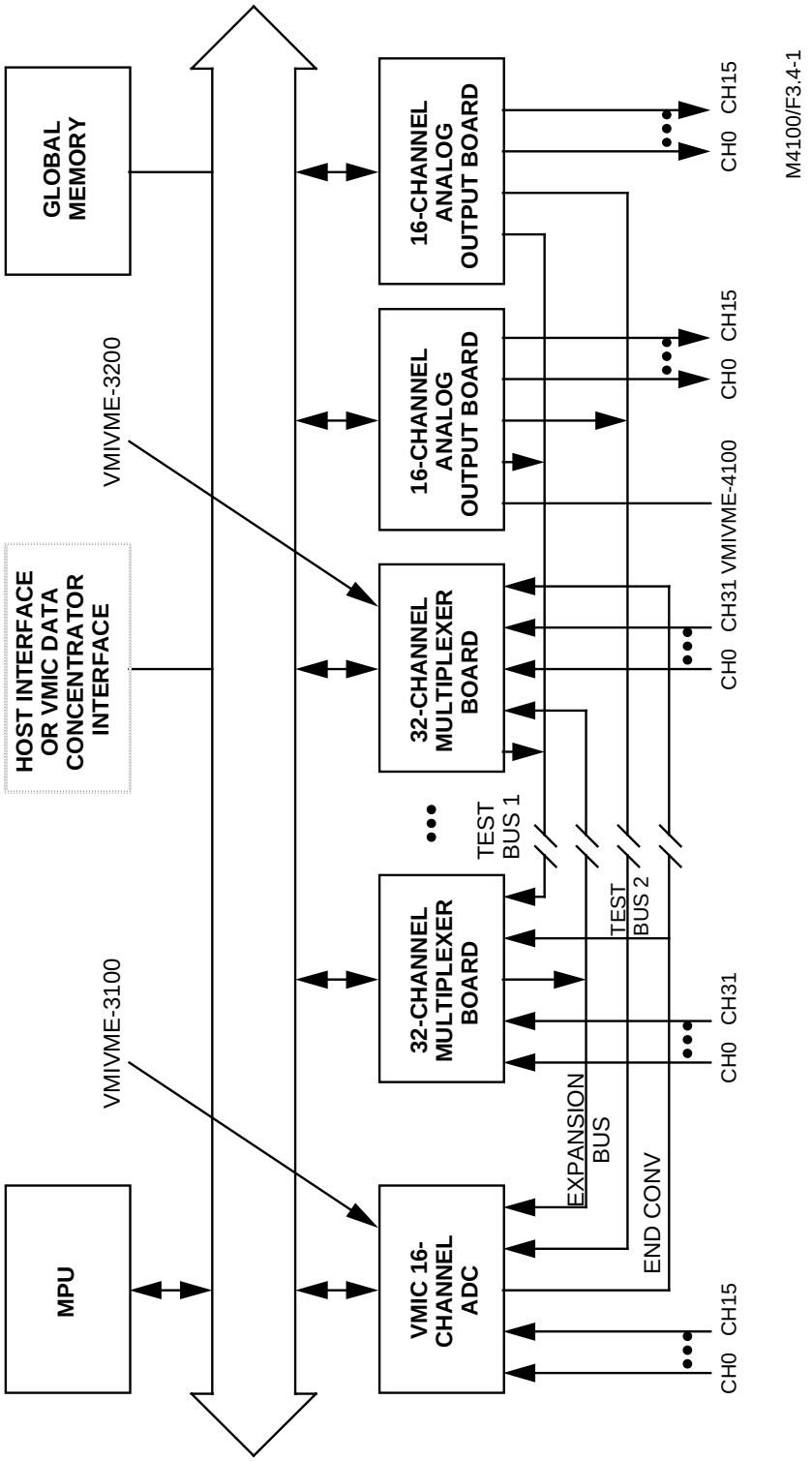


Figure 3.4-1. VMIC High Performance Analog Input/Output Configuration

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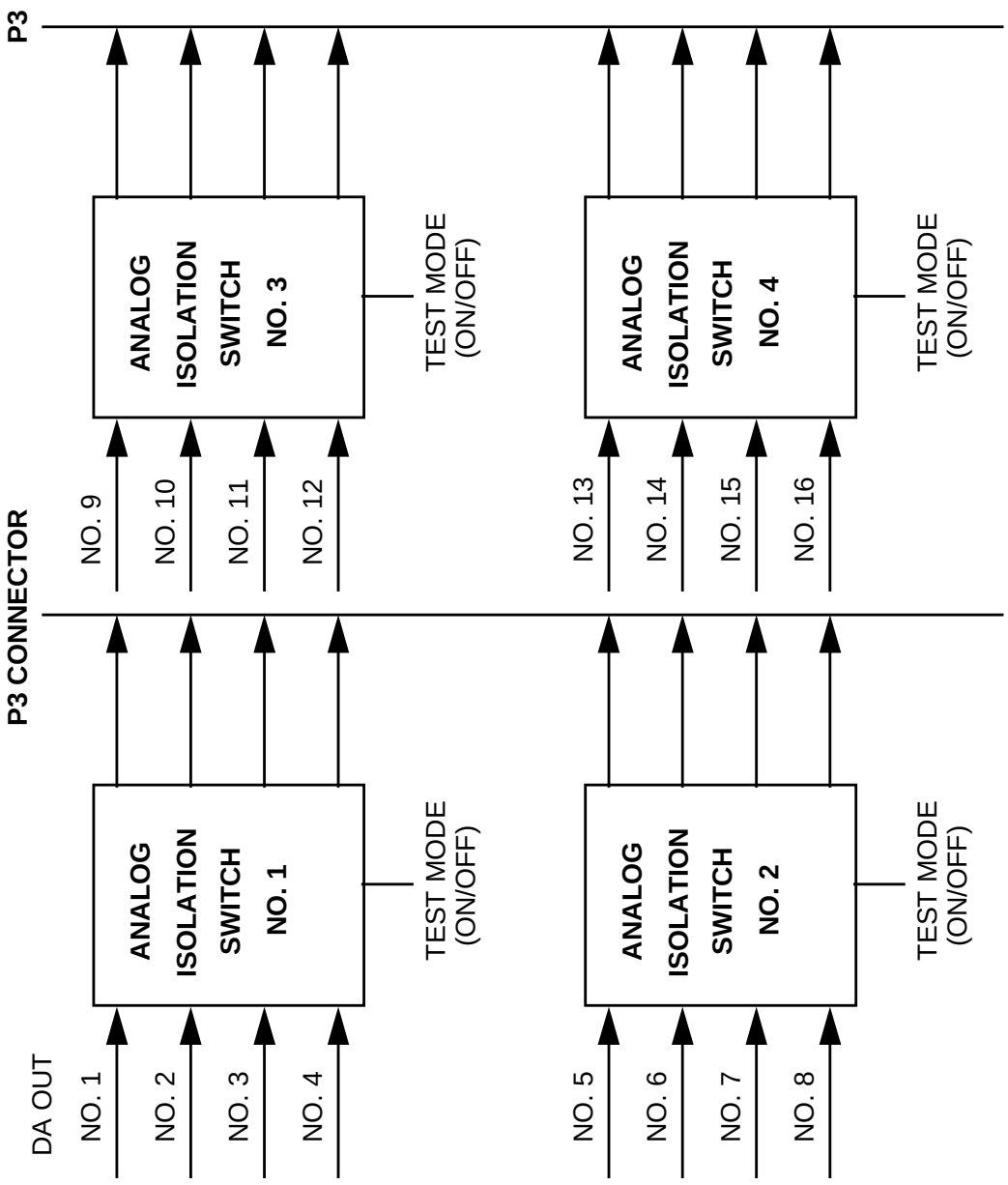


Figure 3.4-2. Analog Output Isolation Switches

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Each of the DAC outputs may be multiplexed one at a time via the Test Mux shown in Figure 3.4-3. First, a control word must be written to the CSR to determine whether the analog output is to be connected or disconnected from the P3 connector and to which one of two test busses the output is to be routed. The DAC channel to be tested is written to in the immediate update mode. Address bits A01 through A04 are latched into the test address register. The output of this register selects, via the test MUX, the DAC channel that has just been updated. Test control information, previously latched in the CSR, passes the DAC output through the analog test switch to Test Bus 2. Test Bus 2 is routed via the Analog Backplane AMXbus™ to the input of the VMIVME-3100 ADC Board where it is available for Analog-to-Digital conversion. When the VMIVME-3100 completes conversion, it sends an end-of-conversion signal down the P2 backplane to the DAC Board. This signal removes either of the two test bus outputs from the analog backplane. Along with the Test Bus 2 signal being sent to the ADC Board, the analog ground (GND SEN) is switched out to the ADC Board. This provides an input to the ADC Board which is similar to a differential signal called pseudo differential. Pseudo differential solves some of the common mode error problems associated with single-ended signals. The input to the ADC Board is referenced to the ground of the DAC Board instead of the local ground at the ADC Board, effectively cancelling out common mode errors associated with different ground potentials at each of the boards.

3.4.1 Using the VMIVME-4100 to Test the Multiplexer Channels of the VMIVME-3200

In a similar way as described in Section 3.3, any one of the DAC outputs can be selected, via the test MUX and analog test switch (Figure 3.4-3), to be routed out a separate dedicated analog bus entitled Test Bus 1. This test bus is a dedicated input to any VMIVME-3200 that resides in the same VMIC Analog Backplane. This test bus can be used by the VMIVME-3200 Board to verify each of the 32 multiplexer channels by multiplexing the test bus input, one at a time, throughout a selected channel of the VMIVME-3200 onto the VMIVME-3100 ADC Board. For more details, refer to the VMIVME-3200 Instruction Manual and the VMIC High Level Analog Data Acquisition System Manual.

3.5 VMEbus INTERFACE DESCRIPTION

The VMEbus interface (Figure 3.5-1) contains the necessary logic to interface a slave board (VMIVME-4100) to the VMEbus. The VMIVME-4100 is memory mapped in the VMEbus short I/O address space. During a *write* cycle to the board address, bits A05 through A15 are compared with the previously selected board address. The board address is selected by DIP switches. If the address compares, then a board select signal is issued. This signal, along with the control signals received at the board, gate the data (D0-D15) to a selected DAC or the CSR on the VMIVME-4100. Address bits A01 through A04 select one of the

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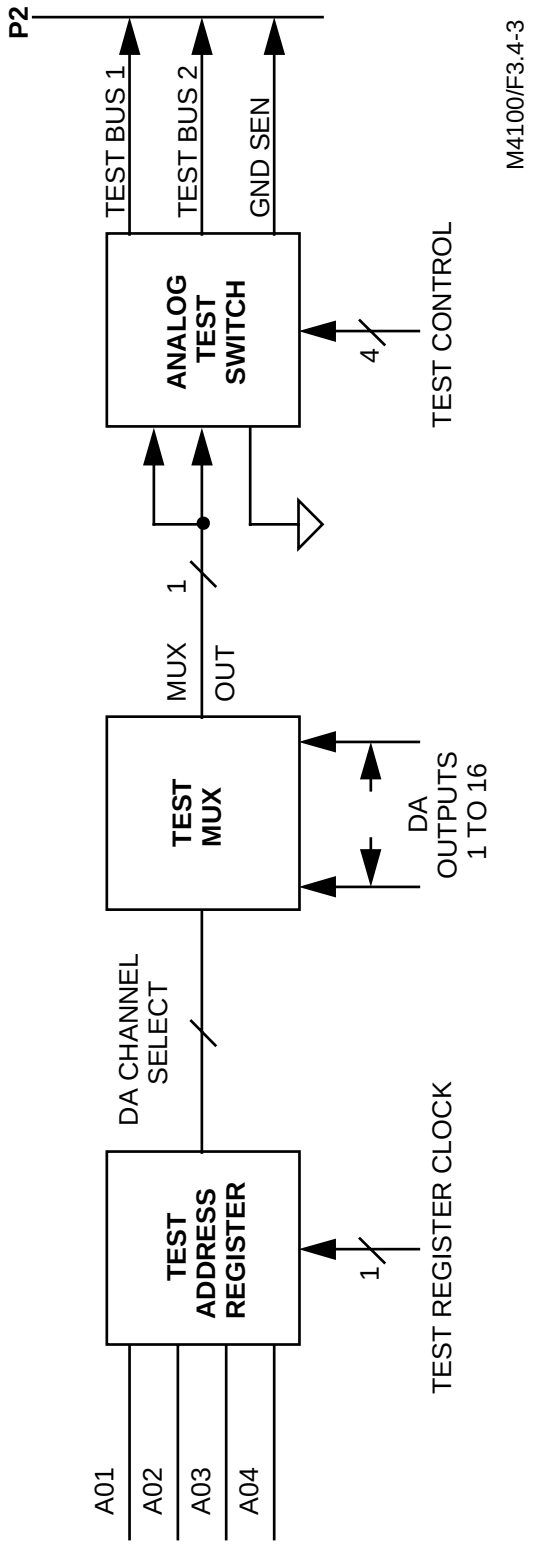


Figure 3.4-3. Test Bus Logic

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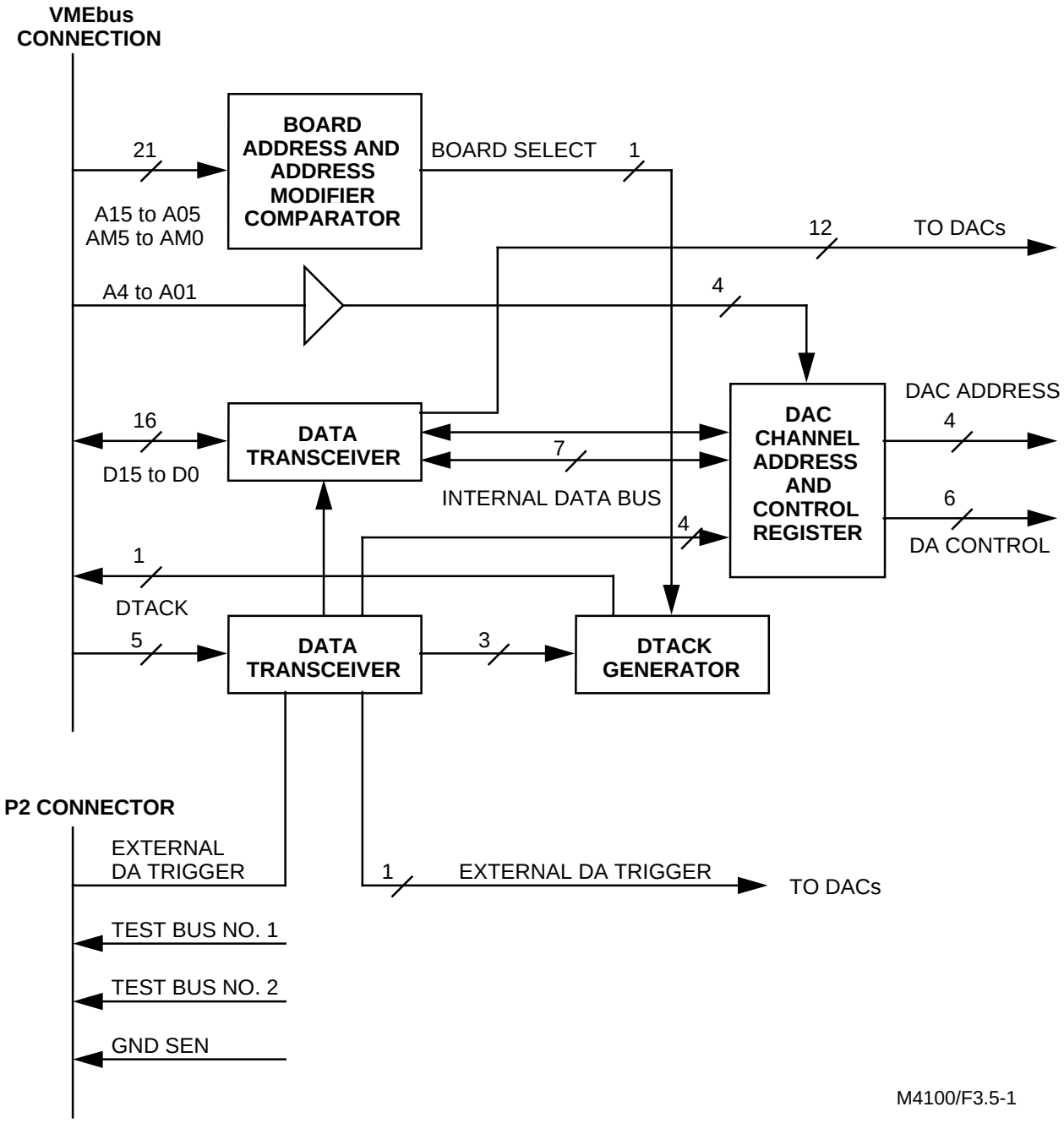


Figure 3.5-1. VMEbus Interface Logic and Interface Signals

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16 DAC channels when D15 is written low; data D0 through D11 is latched into the selected DAC. When D15 is written high to the board, then data D08 through D14 is latched into the CSR.

The VMIVME-4100 circuitry requires +5V, +15V and -15V. The +5V is supplied to the board via the P1 and P2 connectors. An on-board DC-to-DC converter generates the +15V and -15V for the analog circuitry, refer to Figure 3.5-2.

3.6 P2 CONNECTOR I/O SIGNAL DEFINITION

a. AINTESTBS (Test Bus 1). An analog test signal that originates from the DAC Board and is optionally used by the VMIVME-3200 MUX Expander Board to verify the multiplexer channels. Test Bus 1 may be multiplexed through each channel of the VMIVME-3200 MUX Board to a VMIVME-3100 ADC Board for conversion.

b. AOTESTBS (Test Bus 2). A second analog test bus from the DAC Board, used in conjunction with the VMIVME-3100 ADC Board to verify the 16 analog output channels of the DAC Board.

c. EXTSCL (External Start Convert - Low). An externally provided active low input. When this line is input low, any word stored in the DAC first rank registers will begin analog conversion. To initiate a conversion, EXTSCL must go to a TTL low state for at least 150 ns before returning to a TTL high state. The board must have previously been jumpered to enable the board to receive an external start convert signal (see Section 5).

d. GND SEN. In test mode when Test Bus 2 is used, an analog ground from the DAC Board is routed out the GND SEN line. The GND SEN line provides for a pseudo-differential input to a receiving ADC Board.

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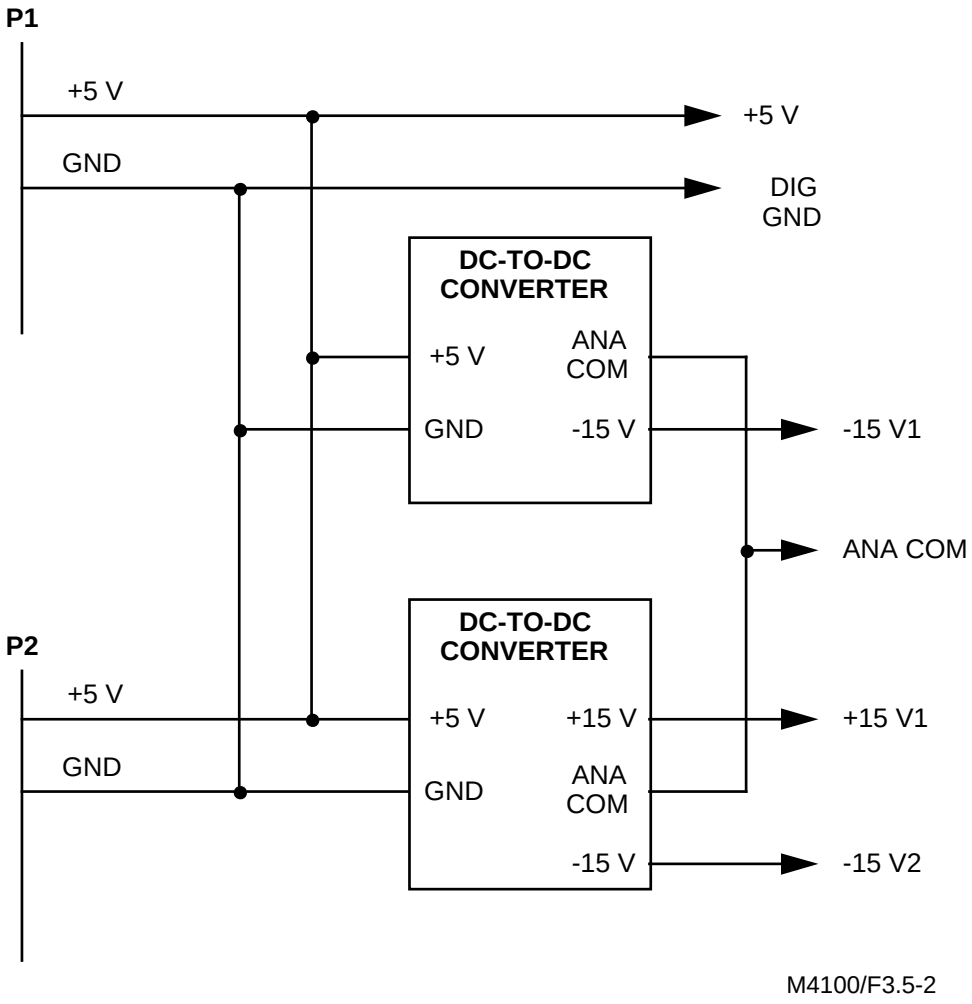


Figure 3.5-2. DAC Board Power

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The Digital-to-Analog Converter (DAC) Board is memory mapped in the short I/O address space. The board occupies 16 successive word locations in the VME short I/O address space of 65,535 bytes. The short I/O space is located from FF0000 HEX to FFFFFF HEX. Each write or read cycle must be a word transfer to an even address, due to the DAC output resolution of 12 bits. The board base address (XXXXX0 HEX) may be selected by DIP switches, as shown in Section 5.5. Figure 4.1-1 represents the VMIVME-4100 address map, assuming the factory set base address of FF0000 HEX. Note that the Control Status Register (CSR) can be written to and read from any of the 16 word locations that the board occupies. When the board is written to, the destination of the data is controlled by data bit 15. If data bit 15 is a "one", the word is written to the control register; whereas, when data bit 15 is a "zero", the data is written to the DAC which is addressed. Reading any address on the board will return the status of the board.

NOTE

JUMPER JB DETERMINES WHETHER THE BOARD OPERATES IN SHORT SUPERVISORY I/O ACCESS OR SHORT NON-PRIVILEGED I/O ACCESS. WITH THE JUMPER INSTALLED, SHORT NON-PROVILEGED I/O ACCESS IS SELECTED.

4.2 DAC BOARD PROGRAMMING OPTIONS

4.2.1 Introduction

There are two types of registers that must be written to for proper operation of the DAC Board. One is the CSR, the other is the DACs. The order in which they are written to may differ, depending on the desired mode of operation for DAC channel start convert.

4.2.2 Immediate DAC Update Mode

The immediate DAC update mode is described in Section 3.1.1 and must be enabled by the jumper configuration described in Section 5.7. Once this has been set up, a 12-bit word can be written to any DAC channel where it will begin immediate analog conversion.

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CONTROL STATUS (READ/WRITE) ADDRESS

	(MSB) D15	D14 … D8	D7 … D0 (LSB)
FF0000 FF0002 • • FF001E	1	CONTROL STATUS BITS	NOT USED

DAC CHANNELS (0 TO 15) ADDRESS (WRITE ONLY)

ADDRESS	(MSB) D15	D14	D13	D12	D11 … D0 (LSB)
FF0000	0	NOT USED			DAC OUT 0
FF0002	0	NOT USED			DAC OUT 1
FF0004	0	NOT USED			DAC OUT 2
FF0006	0	NOT USED			DAC OUT 3
FF0008	0	NOT USED			DAC OUT 4
FF000A	0	NOT USED			DAC OUT 5
FF000C	0	NOT USED			DAC OUT 6
FF000E	0	NOT USED			DAC OUT 7
FF0010	0	NOT USED			DAC OUT 8
FF0012	0	NOT USED			DAC OUT 9
FF0014	0	NOT USED			DAC OUT 10
FF0016	0	NOT USED			DAC OUT 11
FF0018	0	NOT USED			DAC OUT 12
FF001A	0	NOT USED			DAC OUT 13
FF001C	0	NOT USED			DAC OUT 14
FF001E	0	NOT USED			DAC OUT 15

M4100/F4.1-1

Figure 4.1-1. Control Status Register and DAC Channels Address Map

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By the operation of the CSR and its control of the analog isolation switches between the DAC outputs and the P3 (user) connector, all 16 DAC channels can be initiated to the proper value as described in the preceding paragraph. After powering up the board, load the DAC channels with the initial 12-bit word (positive-true offset binary coding, Table 4.2.2-1) required. A control word can then be written to the CSR to enable the DAC outputs to the P3 connector. The CSR bit description for this mode of operation is detailed in Tables 4.2.2-2 and 4.2.2-3. A programming example of the immediate DAC update mode is detailed in Section 4.5.

4.3 DELAYED DAC UPDATE MODE

The delayed DAC update mode operation is described in Section 3.2. This mode must have previously been enabled by the jumper configuration given in Section 5.7. There are two ways for a DAC channel to be updated after the 12-bit word is loaded into the DACs first register. The first, is under program control when data bit D9 is written high to the CSR. Data bit D15 must always be high when writing to the CSR. It should be noted that when setting D9 to initiate the DAC update, control bits D8 and D10 through D14 should be set or reset according to where the user wants the converted output to be routed (refer to Tables 4.2.2-2 and 4.2.2-3). Also, a previously loaded DAC may be updated by an external trigger input from another device. A programming example of the delayed DAC update mode is detailed in Section 4.6.

4.4 TEST MODE PROGRAMMING

As described in Section 3.3, any of the 16 DAC outputs may be selected to pass to a VMIVME-3100 ADC Board over Test Bus 2 to verify the DAC outputs. If a VMIVME-3200 is present in the analog backplane, then any DAC output can be selected to go to that board for test purposes over Test Bus 1. Generally, the programming sequence for utilizing one of the two test busses is as follows:

If immediate DAC update mode is employed, then a control word should be written to the CSR. In this control word, information is included as to which test bus the DAC output is to be routed and whether the output is to be isolated or connected to the P3 connectors (refer to Tables 4.2.2-2 and 4.2.2-3). The DAC to be updated is then loaded with a 12-bit word. The channel is updated and passes out the selected test bus.

An output may be also updated under program control to route to a specified test bus. The board must have previously been jumpered to accommodate the delayed DAC update mode, as shown in Section 5.7. The programming sequence is as follows:

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Table 4.2.2-1. DAC Data Format Analog Output vs Digital Input (±10 V Scale)

DIGITAL INPUT CODE (MSB) D15			(LSB) D0	ANALOG OUTPUT VOLTAGE	
0XXX	0000	0000	0000	-10.000 V	-FULL SCALE
0XXX	0100	0000	0000	-5.000 V	-1/2 SCALE
0XXX	1000	0000	0000	0.000 V	ZERO
0XXX	0000	0000	0001	4.88 mV	+1 LSB
0XXX	1100	0000	0000	+5.000 V	+1/2 SCALE
0XXX	1111	1111	1111	9.9951V	+FULL SCALE - 1 LSB

The analog output may be calculated by the input code written by the processor to the selected DAC channel as follows:

$$\text{Analog Output} = -10\text{ V} + (\text{Digital Input Code in Decimal}) \times \frac{20}{4096}$$

Example: The Analog output for a digital input of 0A00H would be:

(1) 0A00H decimal equivalent is 2560

(2) $\text{Analog Out} = -10\text{ V} + (2560) \frac{20}{4096}$

$$= 2.5$$

M4100/T4.2.2-1

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Table 4.2.2-2. Control Register Data Format and Definitions

D15	D14	D13	D12	D11	D10	D09	D08	D07	D00
1								← NOT USED →	

D08 When written high, engages DAC outputs to the P3 connector, and disengages DAC outputs from P3 connector when written low. At power-up, this control bit is low.

D09 Program Control Start Convert, when input high, generates a signal that transfers contents of previously loaded DACs to the second rank register and updates the analog ouput.

D10 In test mode, written high to clock channel address bits A01 through A04 into test register to select one of 16 DAC channel outputs. Used in conjunction with D11, D12 and D13 to determine test modes.

D11 When written high, engages analog outputs from DAC to one of two test busses. Used in conjunction with D12 and D13 to determine which test bus is selected. At power up, this control bit is low which disengages the test busses.

D12 A high state enables the selected test analog output to pass out the P2 connector on Test Bus 1 (AINTESTBS). At power up this control bit is low.

D13 A high state enables the selected test analog output to pass out the P2 connector on Test Bus 2 (AOTESTBS). At power up this control bit is low.

D14 A low state turns the Fail LED ON. A high state turns it OFF. At power up, this control bit is low.

D15 This bit is used as a register select bit to determine which type of device is to be selected during a *write* cycle. D15 must be high when writing to the control register. Otherwise, D15 is low when writing to the DAC channels.

M4100/T4.2.2-2

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Table 4.2.2-3. Programming the CSR for Different Analog Output Variations - Bit Definitions

1. Analog output over TEST BUS 1 (AINTESTBS).

D15	D14	D13	D12	D11	D10	D09	D08
1	1	0	1	1	1	0 or 1*	0

2. Analog output over TEST BUS 2 (AOTESTBS).

D15	D14	D13	D12	D11	D10	D09	D08
1	1	1	0	1	1	0 or 1*	0

3. Analog output out TEST BUS 2 and out P3 connector to field connected device (used for real-time fault detection of DACs).

D15	D14	D13	D12	D11	D10	D09	D08
1	1	1	0	1	1	0 or 1*	1

4. Analog output over P3 connector only.

D15	D14	D13	D12	D11	D10	D09	D08
1	1	0	0	0	0	0 or 1*	1

*See Table 4.2.2-2.

M4100/T4.2.2-3

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First, a 12-bit word is written to the address of the DAC channel that is to be updated. The data is stored in the DAC register and will be converted by setting the proper bits in a *write* cycle to the CSR. The CSR must be written to at the same address as that of the DAC channel that has previously been loaded. The difference being that data bit D15 must be a "zero" when writing to the DAC channel register and a "one" when writing to the CSR. Data bit D09, when written as "one" to the CSR, initiates the analog conversion of the previously stored 12-bit word.

The test modes can only be used if a VMIVME-3100 ADC Board exists in the same VMIC Analog (P2) Backplane (AMXbus™) as the VMIVME-4100.

4.5 MC68000 ASSEMBLY LANGUAGE PROGRAMMING OF THE VMIVME-4100 DAC BOARD

Only a few assembly language statements are necessary to properly control and utilize the DAC board. It will be assumed that the base address of the board in this example is FF0060H. The board address can be determined by information given in Sections 4.1 and 5.5.

The first example will be the loading of all the 16 DACs with a full scale value of FFFH, giving an analog output over the P3 connector of 9.9951 volts. The DAC output value will be updated immediately upon being written to. This is the immediate DAC update mode explained in Section 4.1.2. The following program is intended as an instructional example ***only*** and may not be useful in the user's application. To enable the DAC immediate update mode, the jumper configuration given in Section 5.7 must be employed. A flow chart of this example is shown in Figure 4.5-1, and the assembly language program is shown in Figure 4.5-2.

4.6 PROGRAM EXAMPLE (DELAYED DAC UPDATE MODE)

In the programming example in Section 4.4, all 16 DACs were loaded with a full scale value of FFFH in the immediate update mode. For illustration purposes, the same result will be obtained by this programming example by using the delayed DAC update mode. The delayed DAC mode is jumper selectable, as described in Section 5.7. The flow chart in Figure 4.6-1 shows the programming sequence and example program listing, and comments are shown in Figure 4.6-2. A base address of FF0060H is assumed.

In the following program example, all 16 DAC channels are loaded with new data then updated under program control. Alternatively, if previously enabled, an external trigger input could have initiated the DA conversion process.

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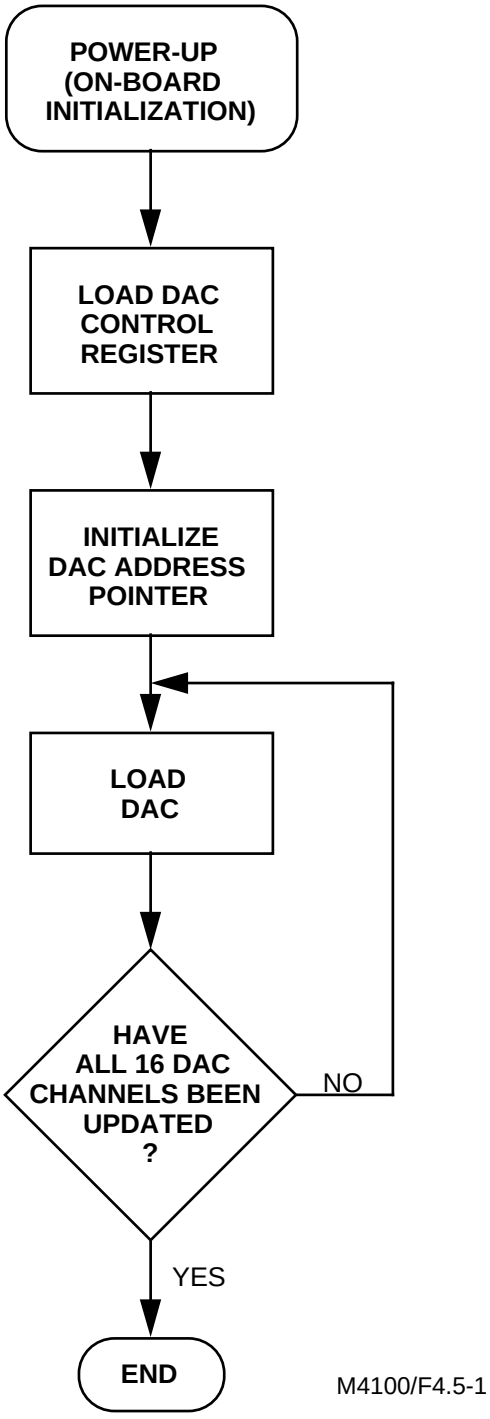


Figure 4.5-1. DAC Programming Sequence (Immediate DAC Start Convert Mode)

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```
                                                        COMMENT
                MOVE.W      #$ 0, D0                    1
                MOVE.W      #C100H,$FF0060              2
                LEA         $ FF0060, A0                3
LOAD NEXT DA    MOVE.W      #$ 0FFF, (A0)+              4
                ADD.W       #1, D0                      5
                CMP.W       #$ 0010, D0                 6
                BNE         LOAD NEXT DA                7
                STOP                                    8
```

COMMENTS:

1. Initialize register D0 (used as a counter) to 0.
2. Load control register (D15 must be a 1) to enable analog outputs to P3 connector.
3. Load address of DAC Channel no. 1 into address register A0
4. Load DAC channel with maximum value. Address pointer is automatically incremented to next DAC channel.
5. Increment counter stored in D0.
6. If all 16 DAC channels have not been loaded, then go to step 7.
7. Load next DAC channel.
8. STOP

In step 2, the control register was set to enable the analog outputs over the P3 connector. The outputs could have also been selected to pass out either of the two test busses, or out the AOTESTBS and the P3 connector simultaneously by selecting the proper control word as determined from Table 4.2.2-3 and the HEX value for the different control words shown in Table 4.5-1.

M4100/F4.5-2

Figure 4.5-2. Program Example (Immediate DAC Update Mode)

Table 4.5-1. Analog Output Control in Immediate Update Mode

ANALOG OUT PATHWAY	CONTROL WORD (D15 TO D0) HEX VALUE
P3 CONNECTOR	C100
AOTESTBS (TEST BUS 2)	EC00
AINTESTBS (TEST BUS 1)	DC00
AOTESTBS & P3 CONNECTOR	ED00

M4100/T4.5-1

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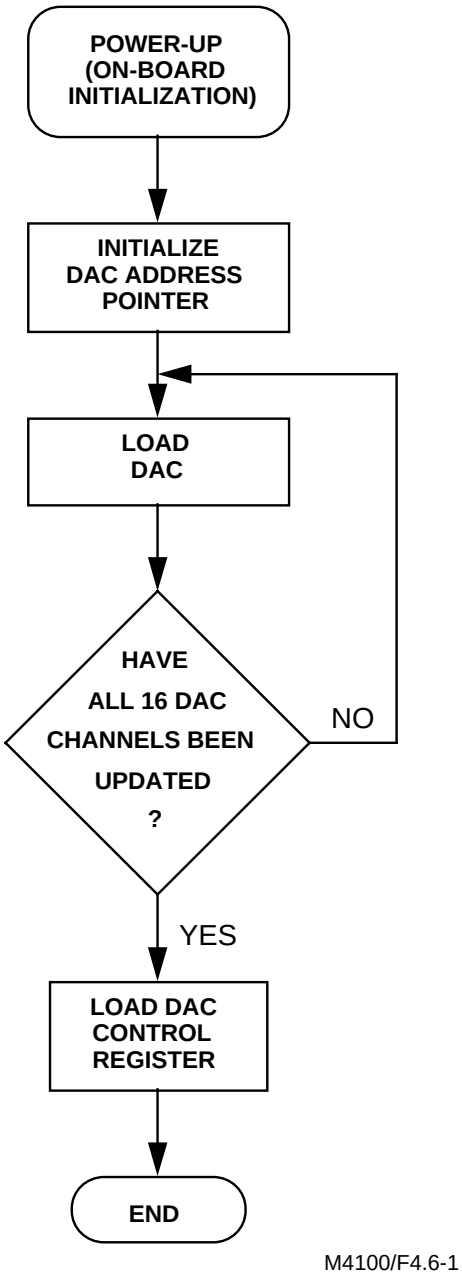


Figure 4.6-1. DAC Programming Sequence (Delayed DAC Update Mode)

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```
                                                        COMMENT
                MOVE.W      #$ 0, D0                    1
                LEA         $ FF0060, A0                2
LOAD NEXT DAC   MOVE.W      #$ 0FFF, (A0)+              3
                ADD.W       #1, D0                      4
                CMP.W       #$ 0010, D0                 5
                BNE         LOAD NEXT D/A               6
                MOVE.W      #$ C300, $FF0060            7
                STOP                                    8
```

COMMENTS:

1. Initialize register D0 (used as a counter) to 0.
2. Load address of DAC Channel no. 1 into address register A0.
3. Load DAC channel with maximum value. Address pointer is automatically incremented to next DAC channel.
4. Increment counter stored in D0.
5. If all 16 DAC channels have not been loaded, then go to step 6.
6. Load next DAC channel.
7. Load control register to start digital-to-analog conversion of all 16 DAC channels. Analog outputs are routed out P3 connector.
8. STOP

In step 7, the control register was set to enable the analog outputs to pass out the P3 connector. The outputs could have also been selected to pass out either of the two test busses or out the AOTESTBS (Test Bus 2) and the P3 connector simultaneously by selecting the proper control word as determined from Table 4.1-3 and the HEX value for the different control words shown below in Table 4.6-1.

M4100/F4.6-2

Figure 4.6-2. Program Example (Delayed DAC Update Mode)

Table 4.6-1. Analog Output Control in the Delayed DAC Update Mode

ANALOG OUT PATHWAY	CONTROL WORD (D15 TO D0) HEX VALUE
P3 CONNECTOR	C300
AOTESTBS (TEST BUS 2)	EE00
AINTESTBS (TEST BUS 1)	DE00
AOTESTBS & P3 CONNECTOR	EF00

M4100/T4.6-1

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

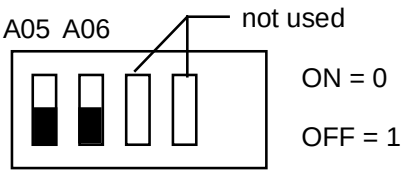
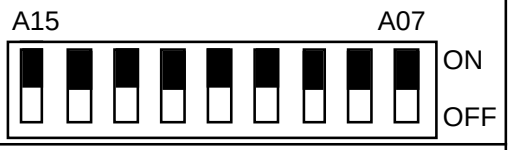
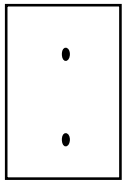
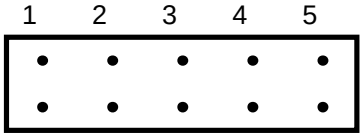
To install the board, de-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated. Review Sections 5.3 and 5.4 before operating the board.

5.3 INSTALLATION

This section describes the VMIVME-4100 Digital-to-Analog Converter (DAC) Board setup procedure and jumper configuration. The board select base address and board jumper configuration are factory preset and are shown in Table 5.3-1. The base address selection switches (S1 and S2) are all shown in the factory configured position. This implies a base address for the board at FF0060H.

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Table 5.3-1. VMIVME-4100 Factory Set Jumpers and Address Switch Configurations

JUMPER	FUNCTION	PRESET CONDITION
S1	BASE ADDRESS SELECTION SWITCH (A05, A06)	
S2	BASE ADDRESS SELECTION SWITCH (A15 TO A07)	
JA JB	NOT USER SELECTABLE DETERMINES ADDRESS MODIFIER RESPONSE OF THE BOARD. JUMPER NOT INSTALLED INDICATES RESPONSE TO SHORT SUPERVISORY I/O ACCESS	 NOT INSTALLED AT FACTORY
JC	JC JUMPERS 1 TO 4 DETERMINE DAC UPDATE MODE. FACTORY PRESET TO IMMEDIATE DAC UPDATE MODE. JC JUMPER 5 ENABLES/DISABLES DAC EXTERNAL TRIGGER. FACTORY PRESET TO DISABLE EXTERNAL JUMPER	 NO JUMPERS INSTALLED AT FACTORY

M4100/T5.3-1

5.4 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, go through the following checklist to verify the board is ready for the intended operation:

1. Have the sections on Theory and Programming of the DAC Board, Sections 3.0 and 4.0, been read and applied to system requirements? ___√___

2. Review Table 5.3-1 to verify the factory installed jumpers and board address select switches are set to desired positions. _____

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a. To change DAC Board Address Switches (S1 and S2) see Section 5.5.
b. To change address modifier response jumper (JB), see Section 5.6.
c. To change DAC update mode jumpers JC 1 to 4, see Section 5.7.
d. To change enable/disable DAC external trigger jumper JC-5, see Section 5.8.

3. To calibrate the +10 V precision reference, see Section 5.9 _____

4. Has the cable, with proper mating connector, been connected to the analog output connector (P3)? See Section 5.10. _____

5. When optional output isolation hardware is employed on the VMIVME-4100, review Section 5.11 for load impedance requirement. _____

5.4.1 DAC Board Installation

After steps 1 through 5 have been reviewed in Section 5.4, then the DAC Board may be installed in a VMEbus system ***(do not install or remove the board with power ON)***. The DAC Board may generally be installed in any slot position, except slot one which is usually reserved for the master processing unit.

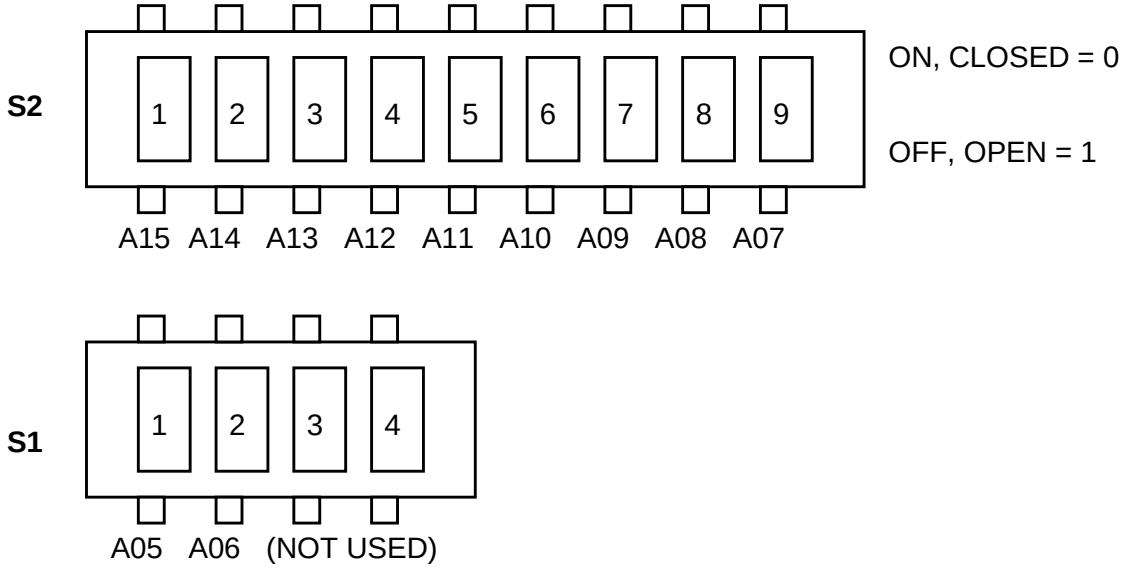
5.5 BOARD ADDRESS SELECTION-SWITCHES

There are two address select DIP switches on board the VMIVME-4100 board. Each individual switch corresponds to an address bit or is not used. If the switch is ON, the corresponding address bit is compared to a logic "zero". All corresponding address bits must compare with the switch positions during a *write/read* of the DAC Board. The way in which each switch corresponds to the address bits is shown in Figure 5.5-1. See Figure 5.5-2 for switch locations on the board.

5.6 ADDRESS MODIFIER RESPONSE SELECTION

The DAC Board is memory mapped in the short I/O address space, as described previously in Section 4.1. The DAC Board will respond to either of the two address modifier codes that may be issued to the DAC Board by a CPU board during a *write* or *read* cycle. The DAC Board is factory set to respond to supervisory short I/O access. To select non-privilege short I/O access, install the jumper installed at jumper location (JB). See Figure 5.5-2 for jumper location on the board.

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For the VMIVME-4100 to respond to a base address of $(FFFF00)_{16}$ the S1 and S2 switches would be set accordingly.

	1	2	3	4	5	6	7	8	9
S2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
S1	ON	ON	X	X					

M4100/F5.5-1

Figure 5.5-1. Base Address DIP Switch Setup

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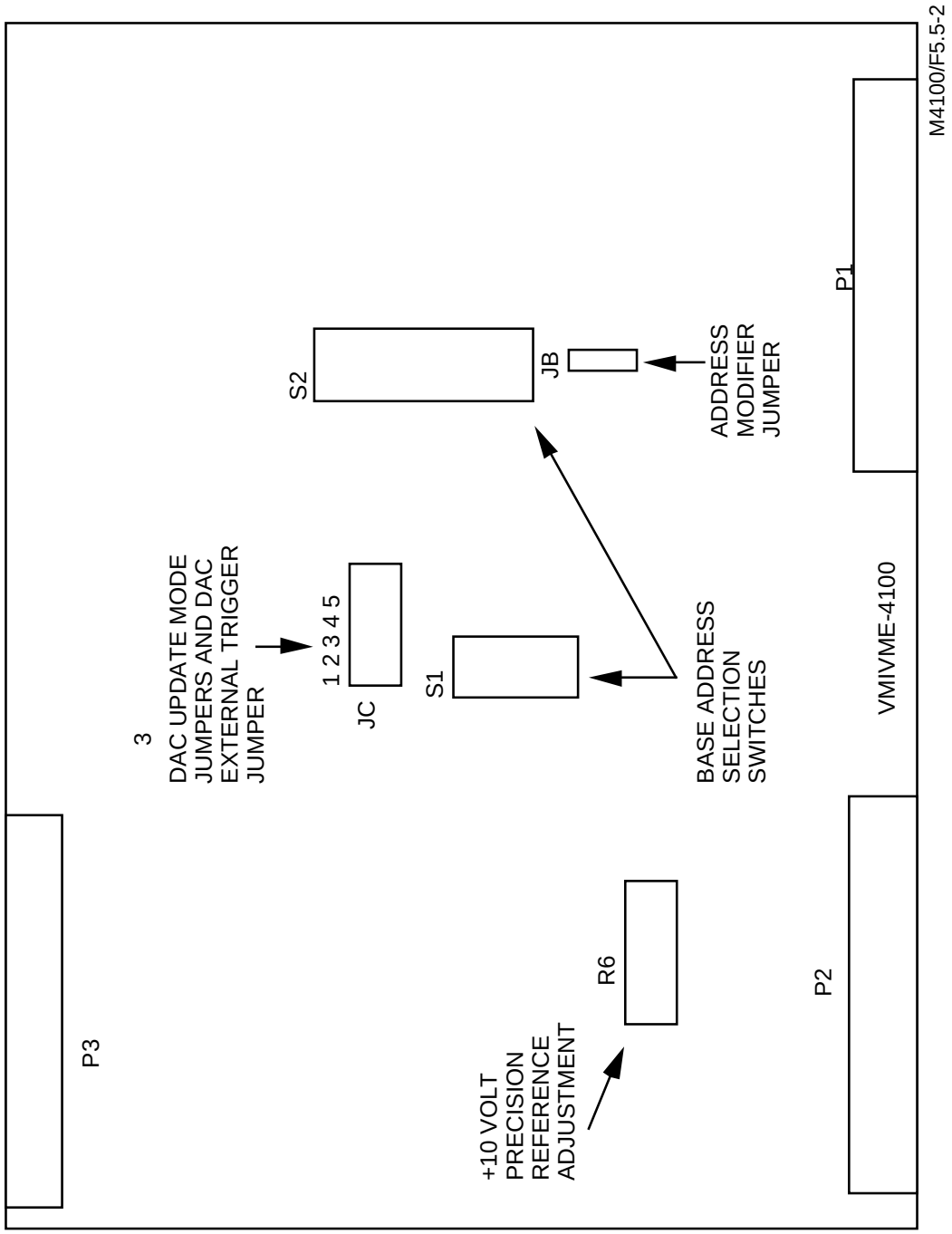


Figure 5.5-2. Jumper and Switch Locations on VMIVME-4100 (Component Side Shown)

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5.7 DAC UPDATE MODE SELECT JUMPERS

There are four jumpers and each jumper corresponds to a set of four DAC channels. To enable a set of channels for the immediate DAC update mode, the corresponding jumper is removed (not installed). If a jumper is installed, then that set of four channels will operate in the delayed DAC update mode. Jumper location (JC) is shown in Figure 5.7-1.

DAC Channels 1 to 4	-	Install Jumper JC-1
DAC Channels 5 to 8	-	Install Jumper JC-2
DAC Channels 9 to 12	-	Install Jumper JC-3
DAC Channels 13 to 16	-	Install Jumper JC-4

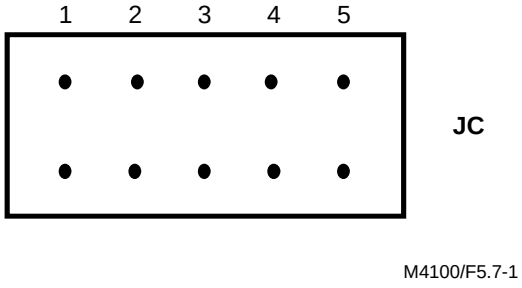


Figure 5.7-1. Jumper Configuration

5.8 EXTERNAL DAC UPDATE TRIGGER ENABLE/DISABLE

Install jumper JC-5 if external trigger operation is desired. Otherwise, remove jumper JC-5. See Figure 5.7-1 for jumper locations on board.

5.9 CALIBRATING THE +10 VOLT PRECISION REFERENCE

The +10 V precision reference has been adjusted at the factory and lock-tight has been applied to the potentiometer adjustment to insure no changes in shipping and handling. However, the lock-tight is easily broken away for user adjustment if necessary. Long-term drift of the reference is very low (0.25 mV/1000 hrs). It is advised that after 6,000 hours of operation, or if the reference output (P2 connector) is being used by other devices, that the reference voltage be checked with a 5-1/2 digit voltmeter. The procedure is as follows:

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a. Remove any cable connected to the P3 connector.

b. Apply power to the board and let warm up 15 minutes.

c. Attach the negative lead of the voltmeter to the P3 connector pin C-1.

d. Attach the positive lead of the voltmeter to the jumper JD pin 2 wire jumper (see Figure 5.5-2 for board location of jumper JD).

e. If voltage is not within 1.0 mV of +10 V, then re-calibrate reference.

f. Re-calibrate reference by adjusting potentiometer R6 (board location shown in Figure 5.5-2) to +10 V(± 0.5 mV).

5.10 CONNECTOR DESCRIPTIONS

Two connectors, P1 and P2, connect the DAC Board to the VMEbus backplane. The connectors are 96-Pin DIN type. The primary connector, P1, contains the address data and control lines, and all additional signals necessary to control data transfer and other bus functions. P2 connector carries the I/O lines necessary to join the DAC Board with the optional VMIVME-3200 MUX Expander Board and the VMIVME-3100 12-Bit Analog-to-Digital Converter (ADC) Board. The P2 connector connects the DAC Board with the Analog P2 Backplane (AMXbus™). See Figure 5.10-1 for P2 pin and signal assignments.

If the test bus option is to be used in conjunction with other VMIC Analog Input/Output (AIO) Boards, then the user must use a VMIC printed circuit Analog P2 Backplane (AMXbus™). These backplanes are available in different slot widths to accommodate almost any combination of boards.

The P3 connector is a Panduit 32-pin male connector type 120-332-033A. The matching Panduit connector for the input cable is a female connector type 120-332-435E. This connector handles 16 analog outputs each, with an associated analog ground wire. See Figure 5.10-2 for P3 connector pin and signal assignments.

5.11 ANALOG OUTPUT ACCURACY WHEN OPTIONAL OUTPUT ISOLATION HARDWARE IS USED

The VMIVME-4100 is offered in several option configurations to the user. One of which is the use of Built-in-Test functions when used with other VMIVME boards as discussed previously in Section 3.3.

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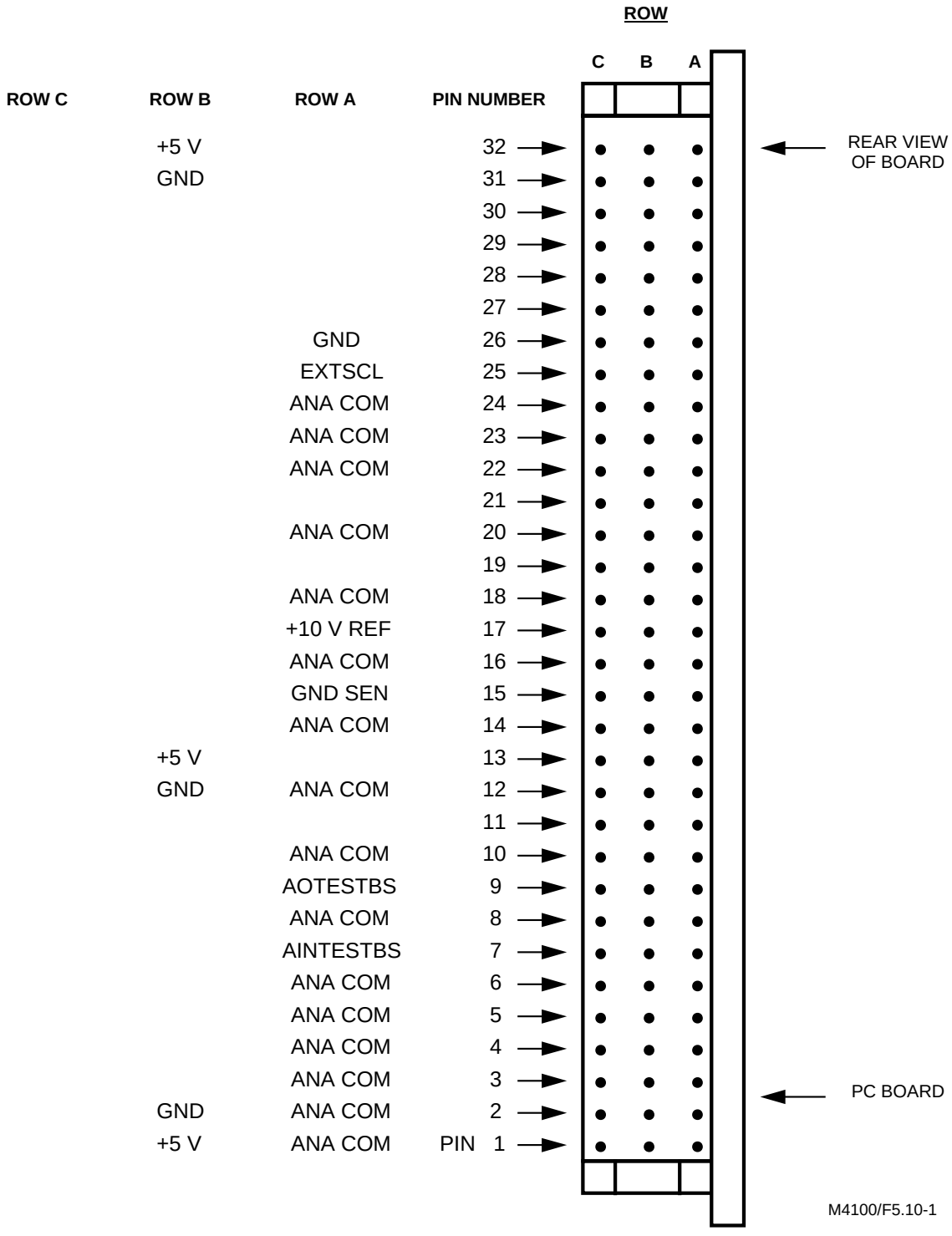


Figure 5.10-1. P2 Connector - Pin Assignments

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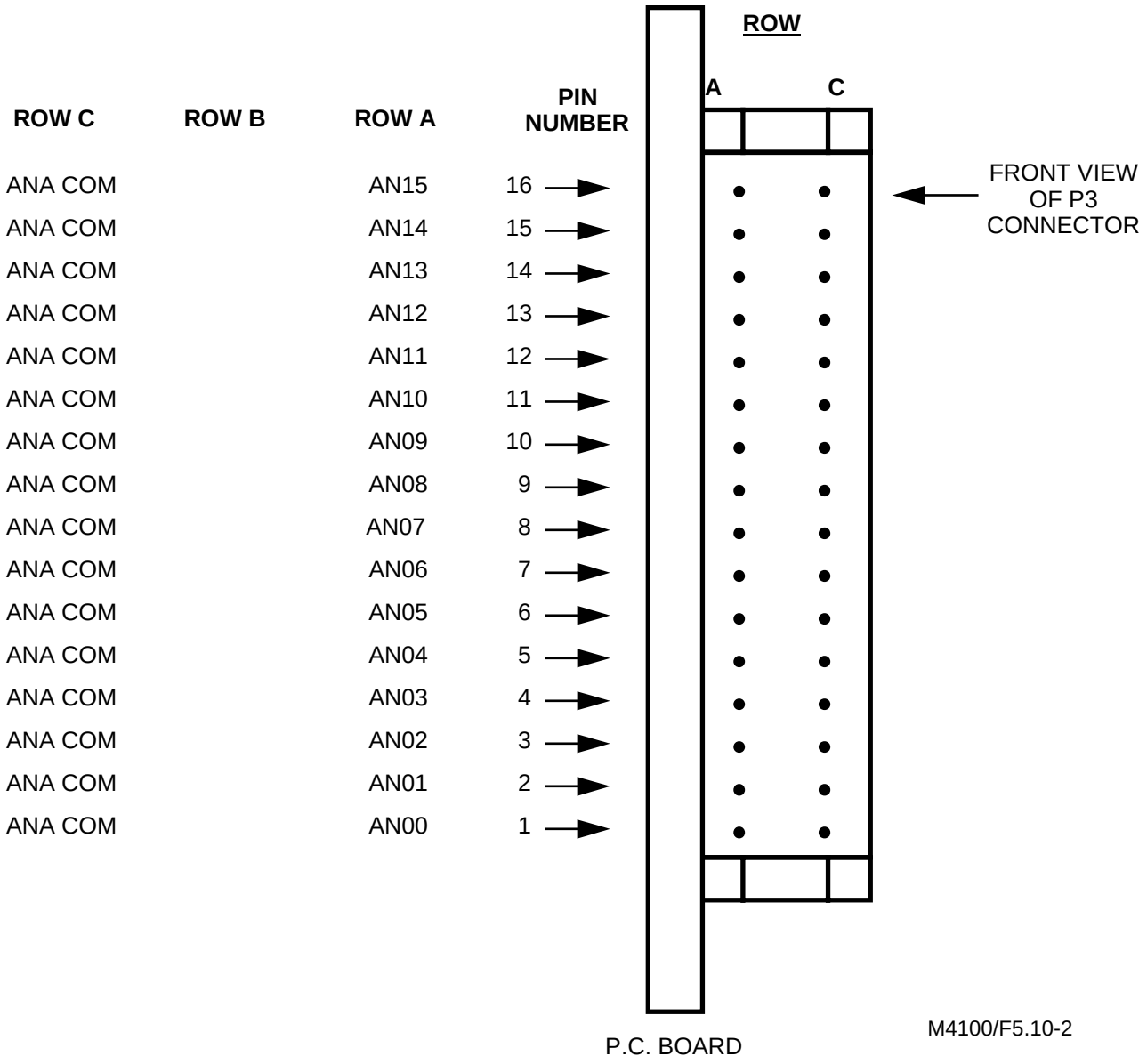


Figure 5.10-2. P3 Connector - Pin Assignments

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The Built-in-Test hardware features analog output isolation switches for all 16 channels that can be turned OF/OFF by software commands. These switches are in series with the analog output and the user-connected device at the P3 connector. These switches have an ON resistance of approximately 100 ohms (max). If the user-connected load does not have a high impedance input, then a possible voltage division error is introduced. For example, if R(LOAD) is 10 kΩ, then a 1% error is introduced. R(LOAD) should be one megohm or greater for an error of .01% or less.

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SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The

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defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

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6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

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6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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