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VMIVME-4120

12-BIT ANALOG OUTPUT BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-004120-000 C

Revised 21 January 1993

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
(205) 880-0444
1-800-322-3616

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	10/10/91	Release ZZZ	91-0266
B	02/03/92	Cover, Pages ii, 2-7, 4-5, and 5-3	92-0031
C	01/20/93	Cover, Pages ii, v, vi, vii, Sections 2 and 6, and Appendix	92-0380

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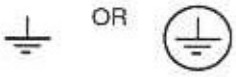
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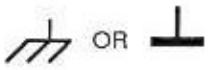
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



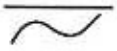
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

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VMIVME-4120

12-BIT ANALOG OUTPUT BOARD

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APPENDIX

A Assembly Drawing, Parts List, and Schematic

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-4120 12-bit Analog Output Board provides 16 high-quality analog output channels. These channels are jumper-selectable for voltage outputs, current loop outputs, or a combination of voltage and current loop outputs. Each output current range is also jumper-selectable. On-board ±15 V DC-to-DC converters are used to supply ± 15 V. A reduced price version of the board without these converters can be purchased (see Ordering Information for more details). A picture of the board is shown in Figure 1.2-1. The following brief overview of principal features illustrates the flexibility and the performance that is available with the VMIVME-4120 Board:

a. 16 analog output channels

b. Jumper-selectable voltage or current outputs

c. 12-bit DAC resolution

d. Output current ranges of 4 to 20 mA, 0 to 20 mA, and 5 to 25 mA (4 to 12 mA, 0 to 10 mA, and 5 to 15 mA are also available)

e. Output voltage ranges of ± 2.5 V, ± 5.0 V, ± 10 V, 0 to + 10 V, and 0 to + 5 V

f. Output short-circuit protection

g. Front panel outputs (P3)

h. Front panel Fail LED indicator

i. Double height Eurocard form factor

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-4120 (Figures 1.2-1 and 1.2-2) is a self-contained, 16-channel, 12-bit VMIVME Analog Output Board. Each of the 16 channels is programmable by the user via 16 12-bit RAM locations. Each RAM location corresponds to an output channel. The VMIVME-4120 periodically fetches the 12-bit binary values out of the RAM locations and uses them as the inputs to the on-board DAC. The output of the DAC is distributed to the sample-and-hold circuits associated with each output channel. See Section 2 for specifications.

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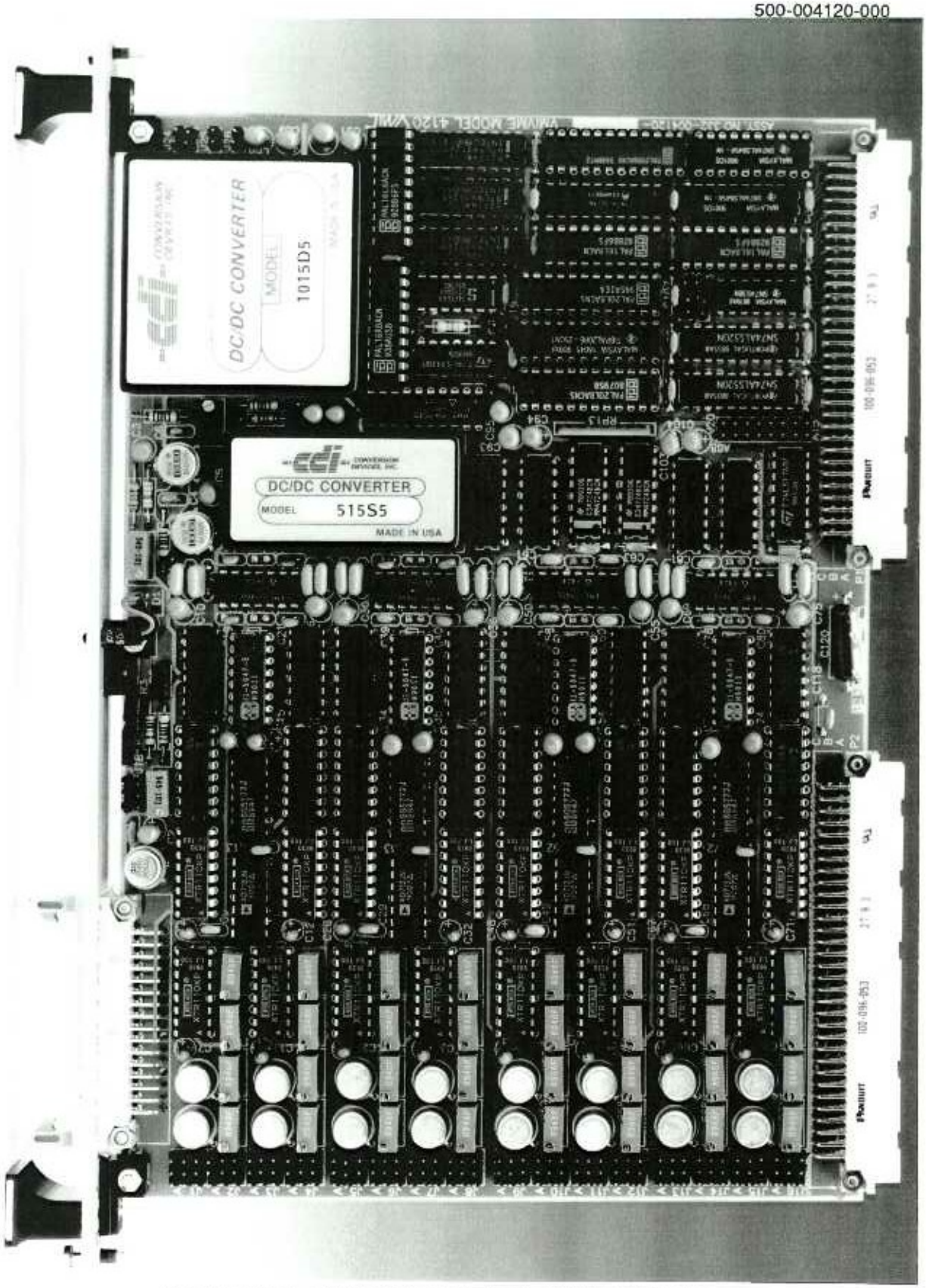


Figure 1.2-1. VMIVME-4120 Analog Output Board

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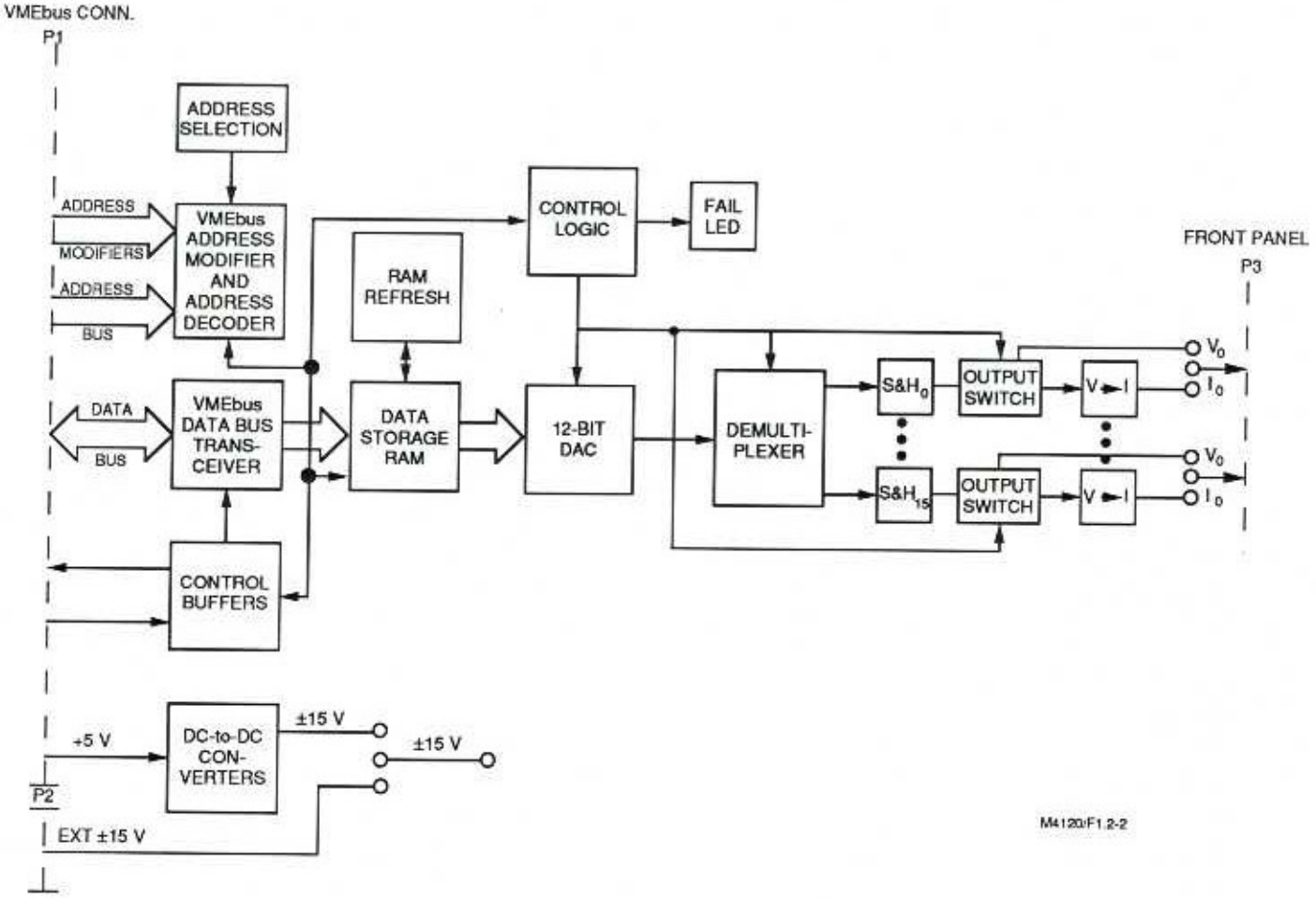


Figure 1.2-2. VMIVME-4120 Functional Block Diagram

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See Sections 3, 4, and 5 for more detailed information pertaining to the VMIVME-4120.

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Product (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004120-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-4120 is a 16-Channel, 12-Bit Analog Output Board which is designed to operate in a VMEbus chassis. The following sections describe in detail the theory of operation of the VMIVME-4120.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-4120 is divided into the following functional categories. All VMIVME-4120 functions are discussed in detail in this section.

a. VMEbus interface
b. Data storage
c. DAC and analog distributor
d. Analog output buffers and switches
e. Voltage-to-current converters
f. Analog outputs refresh logic
g. Power converter

3.3 VMEbus CONTROL INTERFACE

The VMIVME-4120 communications registers are memory mapped as 32 (decimal) 16-bit words. The registers are contiguous, and may be user located on any 64-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged bus communications.

During each *read* or *write* operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers shown in Figure 3.3-1 and the address and address-modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted (driven LOW). Subsequent removal of the Central

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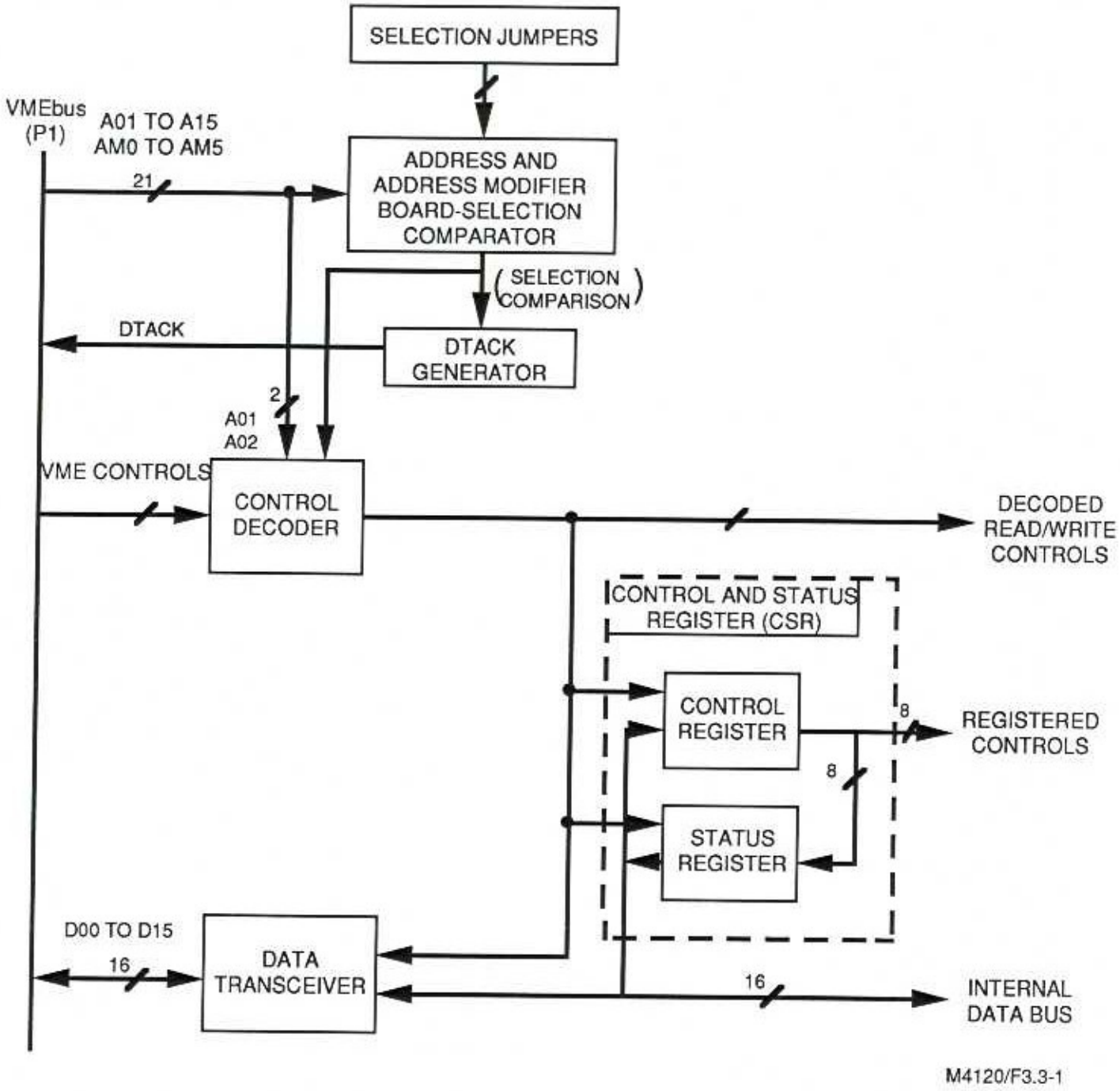


Figure 3.3-1. VMEbus Control Signals and Interface Logic

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Processing Unit (CPU) *read* or *write* command causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communications with the board, they are as follows:

a. Data bus lines D00 to D15
b. Address lines A01, A02, A03, A04, A05
c. Bus control signals:

(1) WRITE
(2) DS0*, DS1*
(3) SYS CLK
(4) SYS RESET*

Data bus lines are bi-directional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A05 map the 32 communication registers onto a 64-byte range within the VME address space (Section 4). The control signals determine whether data is to be moved to the board (*write*) or from the board (*read*), provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all timers and flags.

Static controls are latched into the Control and Status Register (CSR) and are used primarily to establish the operational mode of the board. The CSR is a *read/write* register. The *WRITE* signal determines whether the CSR is being written to (control), or read from (status).

Each of the 16 analog output channels is controlled by writing 12-bit right-justified data into a dedicated 16-bit *read/write* register. The 16 analog output control registers constitute the VME port of a 16-word dual port memory. The other memory port is controlled by the analog output refresh logic.

3.4 ANALOG OUTPUTS

Sixteen analog outputs are available at the P3 connector. The analog outputs are updated (refreshed) periodically from dual port memory by the REFRESH control logic, as illustrated in Figure 3.4-1. Each output receives an update once every 1.7 ms in the default refresh mode. A program controlled FAST REFRESH control bit can be used to reduce the refresh cycle time to approximately 0.6 ms, thereby raising the maximum output sampling rate from 588 Hz to 1.6 kHz.

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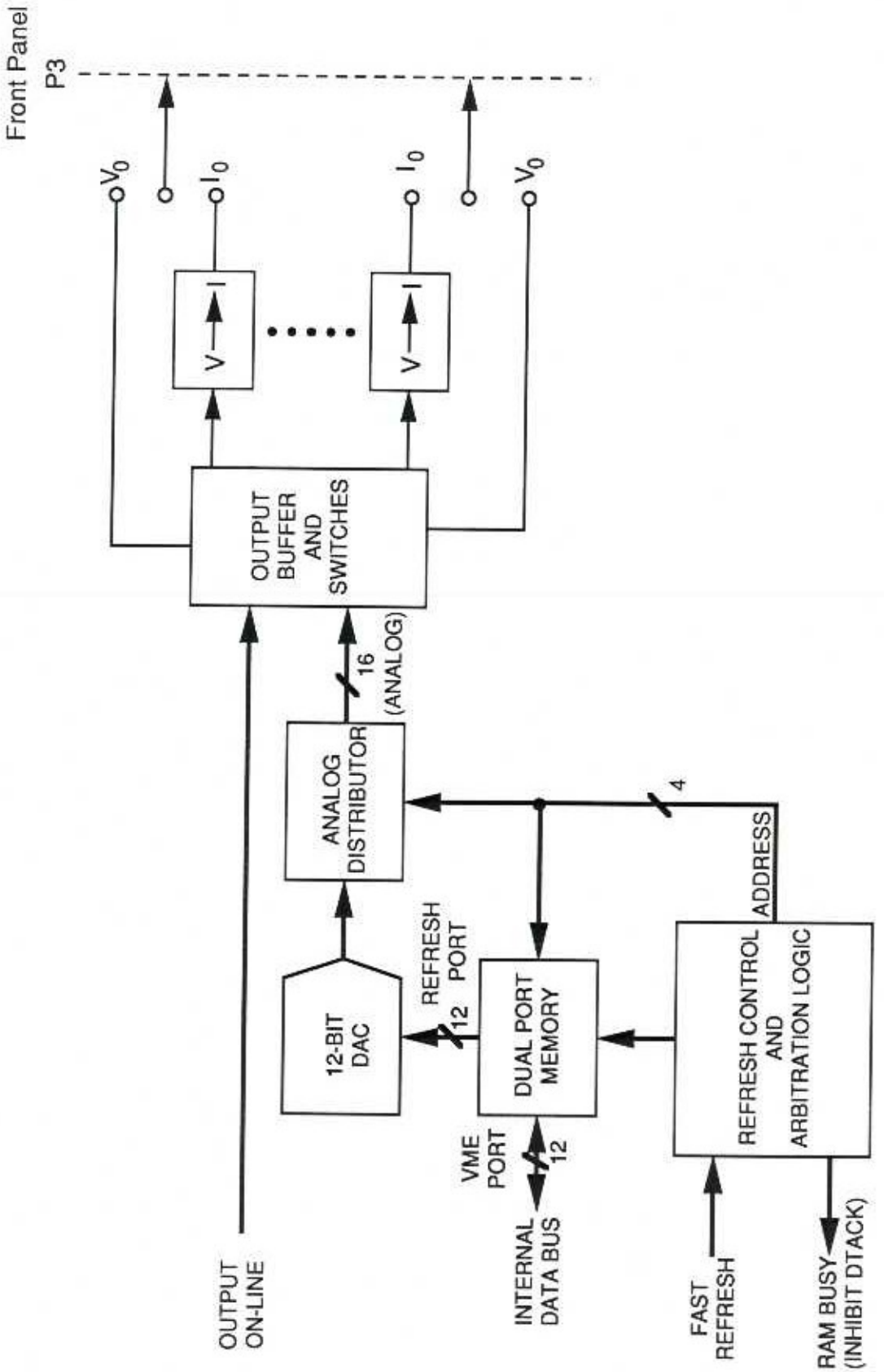


Figure 3.4-1. Analog Output Circuitry

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3.4.1 Digital-to-Analog Converter (DAC)

All 16 analog outputs are serviced by a single 12-bit DAC. The DAC is controlled by the REFRESH control logic, which periodically transfers data from the dual port memory to the DAC, and simultaneously connects the DAC to the appropriate section of the analog distributor. Analog output data in the dual port memory is placed there through the VME port by the controlling processor.

3.4.2 Analog Distributor

The analog distributor consists of the following elements:

a. One of 16 decoder
b. Low charge injection analog demultiplexer
c. Sixteen capacitive storage elements

As the DAC is updated with data for each channel in the output REFRESH sequence, the one of 16 decoder receives the same four address lines that are used to select the dual port memory data location. In this manner, the converted analog level is always routed to the distributor section which corresponds to the dual port memory location for the same channel.

After allowing the DAC to settle, the REFRESH logic enables (turns ON) the demultiplexer, and the converted voltage level is transferred to the corresponding storage capacitor. A settling interval of approximately 100 µs is provided by the REFRESH logic, after which the demultiplexer is disabled and the next channel in the REFRESH sequence is accessed.

3.4.3 Output Buffers and Switches

Voltage levels stored by the analog distributor are buffered and then switched to either the P3 connector, or to the voltage-to-current converters. The output buffers are low leakage, precision operational amplifiers which can supply 5 mA of drive current over the full available output voltage range of ±10 V (at the specified accuracy), and which can withstand sustained short circuits-to-ground without damage.

Output switches permit the analog voltage outputs to be disconnected from P3. To eliminate the effect of switch resistance on output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operation. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ±15 V supply rails.

Current outputs are produced by connecting the voltage levels discussed previously in this section to the voltage-to-current conversion circuitry and connecting the current outputs to the P3 connector (both of these connections are made with jumpers as shown in Figure 5.4.3-1). Typically the voltage range is set to 0 to +10 V to produce 4 to 20 mA, 0 to 20 mA or

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5 to 25 mA. A voltage range of 0 to +5 V can be selected to produce 4 to 12 mA, 0 to 10 mA or 5 to 15 mA.

3.4.4 Data RAM and Refresh Control

The dual port memory which services the analog outputs is organized as a 12-bit wide, 16-location array, in which each location can be accessed from either of two ports. The random access VME port is used by the VME host to load the analog output digital codes into the memory. The digital codes are then transferred sequentially through the DAC port to the DAC, where they are converted into voltage levels and subsequently distributed to the appropriate analog output channels. The REFRESH logic control sequence is shown in flow diagram form in Figure 3.4.4-1.

Operation of the dual port memory is controlled by the REFRESH control logic which derives its timing from the 16 MHz system clock. The REFRESH control logic supervises all data transfers between the memory and the DAC, and controls the distribution of analog voltage levels to the analog outputs. (Refer to the preceding sections for specific functions of the REFRESH logic.)

Because the dual port memory must be accessed through both the VME and DAC ports, arbitration logic is employed during the transfer of data to the DAC to ensure that only one port is active at any time.

3.5 BUILT-IN POWER CONVERTER

Electrical power for the VMIVME-4120 analog network is supplied by the DC-to-DC converters. The converters transform 5 V logic power into regulated and isolated ±15 VDC power, with a load capacity of approximately 670 mA at +15 V and 330 mA at -15 VDC. A reduced price version of the board without these converters can be purchased (see Ordering Information for more details).

3.6 BOARD ID REGISTER

The first word location of the VMIVME-4120's memory map is a read-only register. It always reads 16xx (HEX; the last two digits are not specified). Other VMIC products have similar registers which read different constants. This allows general purpose system software to automatically determine which boards have been installed (by reading from a predetermined list of addresses). The configuration software must be able to handle a bus error if it happens to read an empty location.

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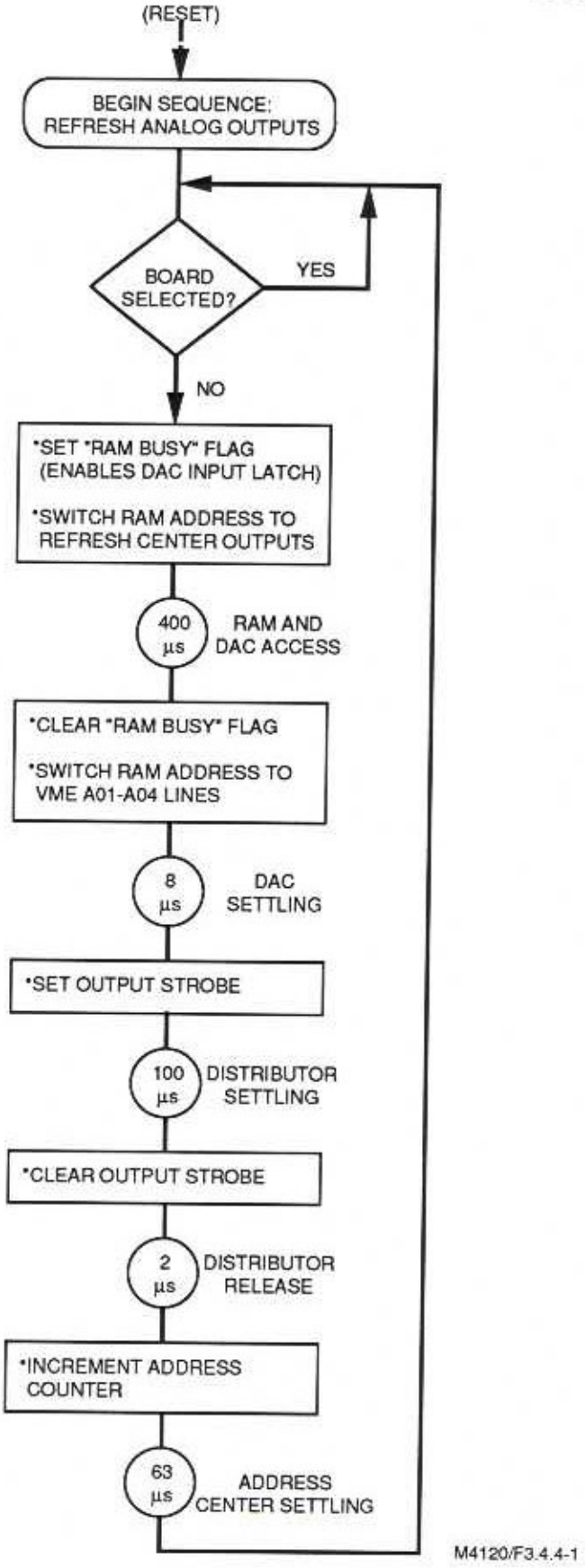


Figure 3.4.4-1. Analog Outputs Refresh Logic; Flow Diagram

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

Communication with the VMIVME-4120 Analog Output Board takes place through 32 contiguous 16-bit register locations which are mapped into the VME short I/O address space. The short I/O address space consists of all locations within the address range from NNNN0000 HEX to NNNNFFFF HEX*. A memory map for the VMIVME-4120 is given in Table 4.1-1.

4.2 CONTROL AND STATUS REGISTER DESCRIPTION

The communication register located at relative address 02H is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

a. Front panel Fail indicator (LED)
b. Two's complement or straight binary operation
c. Analog voltage outputs on-line/off-line
d. Analog current outputs on-line/off-line
e. Analog outputs refresh rate
f. SCAN HALT

The CSR is 8 bits in length, and is detailed in Table 4.2-1. The function of each CSR bit is described in detail subsequently in the associated programming discussions.

4.3 INITIALIZATION

When SYSTEM RESET is applied to the board, all bits of the Control Register are cleared to the LOW state "zero".

*The value of NNNN depends on the make and model of the controlling CPU.

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Table 4.1-1. VMIVME-4120 Memory Map

RELATIVE HEX	ADDRESS DEC	REGISTER NAME	ACCESS MODE
00	00	BOARD IDENTIFICATION	READ (16XX HEX)
02	02	CSR	READ/WRITE
04 TO 1E	04 TO 30	(RESERVED)	---
20	32	ANALOG OUTPUT CHANNEL 00	READ/WRITE
22	34	ANALOG OUTPUT CHANNEL 01	READ/WRITE
24	36	ANALOG OUTPUT CHANNEL 02	READ/WRITE
26	38	ANALOG OUTPUT CHANNEL 03	READ/WRITE
28	40	ANALOG OUTPUT CHANNEL 04	READ/WRITE
2A	42	ANALOG OUTPUT CHANNEL 05	READ/WRITE
2C	44	ANALOG OUTPUT CHANNEL 06	READ/WRITE
2E	46	ANALOG OUTPUT CHANNEL 07	READ/WRITE
30	48	ANALOG OUTPUT CHANNEL 08	READ/WRITE
32	50	ANALOG OUTPUT CHANNEL 09	READ/WRITE
34	52	ANALOG OUTPUT CHANNEL 10	READ/WRITE
36	54	ANALOG OUTPUT CHANNEL 11	READ/WRITE
38	56	ANALOG OUTPUT CHANNEL 12	READ/WRITE
3A	58	ANALOG OUTPUT CHANNEL 13	READ/WRITE
3C	60	ANALOG OUTPUT CHANNEL 14	READ/WRITE
3E	62	ANALOG OUTPUT CHANNEL 15	READ/WRITE

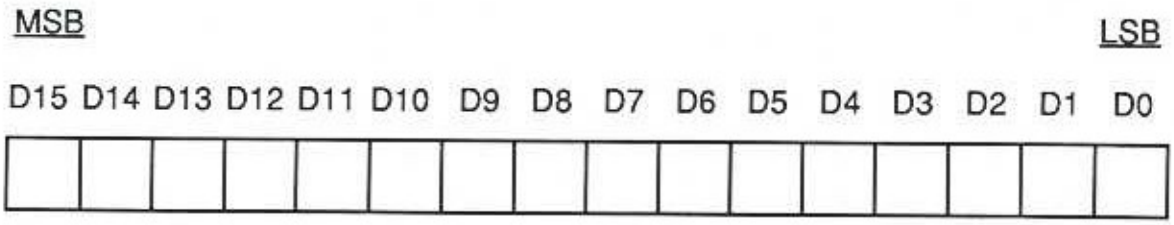
*Register address is the sum of the relative address and the board address.

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Table 4.2-1. Control and Status Register (CSR) Functions

CONTROL REGISTER DATA FORMAT



CONTROL BIT	NAME	FUNCTION
D15	————	(Reserved - write a "zero" to this bit.)
D14	Fail LED L	The Fail LED is OFF if this bit is set to "one", and is ON if the bit is "zero".
D13	————	(Reserved - write a "zero" to this bit.)
D12	Two's COMPL L	DAC coding format is straight binary if D12 is "one" (HIGH), two's complement if D12 is "zero" (LOW).
D11	V OUTPUT on H	(Also called "ANALOG VOLTAGE OUTPUT ON-LINE.") If D11 is set to "one", the voltage outputs are enabled.
D10	CURRENT on H	(Also called "ANALOG CURRENT OUTPUT ON-LINE.") If D10 is set to "one", the current outputs are enabled. NOTE: D11 and D10 must both be set for the current output to operate correctly.
D9	SCAN HALT	When D9 is set to "one", the refresh control logic sequencer is halted.
D8	FAST REFRESH H	The nominal analog output refresh interval is 1.7 ms if D8 is "zero", 0.6 ms if D8 is "one".
D7 ◄ D0	————	(Reserved - write a "zero" to these bits.)

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4.4 CONTROLLING THE ANALOG OUTPUTS

The 16 analog output channels appear to the controlling processor as 16 consecutive 12-bit words in the address space assigned to the VMIVME-4120 Board. The communication register map shown in Table 4.1-1 lists the board-relative address of each output channel. Each analog output register supports both *read* and *write* operations, eliminating the need for corresponding "shadow" latches in the processor Random Access Memory (RAM) space.

4.4.1 Writing to Outputs

Digital codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four Most Significant Bits (MSBs) (D12 to D15) will be ignored, and will not be retained for read back. Each output will respond to a new code within 1.7 ms after the code is written to the output register (0.6 ms in FAST REFRESH MODE).

The Digital-to-Analog (D/A) coding conventions used by the D/A Converter (DAC) are shown below. A few examples are given in Table 4.4.1-1.

OUTPUT (straight binary) = (DAC_INPUT/4096) x (MAX_OUT - MIN_OUT) + MIN_OUT
where DAC_INPUT ranges from 0 to 4095 decimal (0 to FFF HEX), MAX_OUT is the DAC output with FFF HEX as the input and MIN_OUT is the DAC output with "000" as the input.

OUTPUT (two's complement) = (MAX_OUT - MIN_OUT)/2 + (DAC_INPUT/4096) x (MAX_OUT - MIN_OUT)
where DAC_INPUT ranges from -2048 to 2047 decimal (800 to 7FF HEX), MAX_OUT is the DAC output with 7FF HEX as the input and MIN_OUT is the DAC output with 800 HEX as the input.

4.4.2 "FAST REFRESH"

Setting the FAST REFRESH control bit (Table 4.2-1) HIGH will reduce the analog output REFRESH time from the default value of 1.7 ms to 0.6 ms. As each channel is refreshed, there exists associated transient noise which is injected onto the specified output channel. Operating in "FAST REFRESH" mode will increase the rate of these transients. For this reason two refresh rates are available even though this high frequency noise is negligible and will be virtually eliminated when a cable is connected to P3.

4.4.3 Off-Line Operation

Setting the V OUTPUT ON H bit enables all channels configured for voltage output. It must be set along with the CURRENT ON H bit to enable the

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Table 4.4.1-1. DAC Data Format and Coding

DAC DATA FORMAT

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D

DAC CODING

UNIPOLAR RANGES — STRAIGHT BINARY

OUTPUT	0 TO +10 V	0 TO +5 V	D15			D0
+FS LSB	+9.9975 V	+4.9988 V	XXXX	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	XXXX	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001

BIPOLAR RANGES — OFFSET BINARY

OUTPUT	±10 V	±5 V	±2.5 V	D15			D0
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	1000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	0000	0000	0000

BIPOLAR RANGES — TWO's COMPLEMENT

OUTPUT	±10 V	±5 V	±2.5 V	D15			D0
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	0111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	0000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	1000	0000	0000

CURRENT RANGES — STRAIGHT BINARY

OUTPUT	0 to 20 mA	4 to 20 mA	5 to 25 mA	D15			D0
+FS LSB	19.9951 mA	19.9961 mA	24.9951 mA	XXXX	1111	1111	1111
+1/2 FS	10.0000 mA	12.0000 mA	15.0000 mA	XXXX	1000	0000	0000
+1 LSB	0.0049 mA	4.0039 mA	5.0049 mA	XXXX	0000	0000	0001
ZERO	0.0000 mA	4.0000 mA	5.0000 mA	XXXX	0000	0000	0000

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channels configured for current output. See Section 5 for configuration information. Voltage output channels are in a high-impedance state when they are disabled.

Setting the CURRENT ON H bit (and V OUTPUT ON H) enables all current-output channels. When this bit is low, each channel delivers the minimum for its selected range. For example, any channel set to 4 to 20 mA will source 4 mA. See Section 5 for range selection information.

****
* CAUTION *
****

IF THE 4120 IS ACCESSED BY BOTH USER-MODE PROGRAMS AND SUPERVISORY PROGRAMS (SUCH AS INTERRUPT HANDLERS), THEY MUST TAKE CARE TO USE THE SAME PRIVILEGE LEVEL. THIS IS BECAUSE THE VMIVME-4120 CAN NOT BE JUMPERED TO ALLOW BOTH SUPERVISORY AND NONPRIVILEGED ACCESSES AT THE SAME TIME. ONE OR THE OTHER MUST BE SELECTED, BUT NOT BOTH.

4.4.4 "SCAN HALT"

Setting the SCAN HALT bit to "one" causes the refresh control logic sequencer to halt. Output accuracy can not be guaranteed with this bit set because the sample-and-hold voltages will begin to droop. Typically, the SCAN HALT bit will not be used during normal operation. Users are advised not to use it (allow it to remain "zero").

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

a. Have the sections pertaining to theory and programming, Sections 3 and 4, been reviewed and applied to system requirements?

b. Review Section 5.4.1 and Table 5.3-1 to verify that all factory installed jumpers are in place. To change the board address or address modifier response, refer to Section 5.4.2.

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c. Have the I/O cables, with the proper mating connectors, been connected to the input/output connector P3? Refer to Section 5.6 for a description of the P3 connector.

d. Calibration has been performed at the factory. If recalibration should be required, refer to Section 5.5.

5.4 OPERATIONAL CONFIGURATION

Control of the VMIVME-4120 Board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all VMIVME-4120 jumpers are shown in Figure 5.4-1 and Table 5.3-1, respectively.

5.4.1 Factory Installed Jumpers

Each VMIVME-4120 Board is configured at the factory with the specific jumper arrangement shown in Table 5.3-1. The factory configuration establishes the following functional baseline for the VMIVME-4120 Board, and ensures that all essential jumpers are installed.

a. Board short address is set at 0000 HEX
b. I/O access mode is short nonprivileged
c. Current loop outputs on all channels
d. 4 to 20 mA current range on all channels

5.4.2 Board Address and Address Modifier Selection

Jumper J20, and jumpers J22 and J23 permit the VMIVME-4120 Board to be located on any 64-byte boundary within the short I/O address space. The short I/O address space consists of all addresses between NNNN0000 HEX* and NNNNFFFF HEX, and requires that 15 (word) address lines be decoded in order to account for all locations. Since five lines are used for decoding on-board functions (A1 through A5), the VMIVME-4120 Board address is defined by ten lines; address bits A06 through A15.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit jumper positions, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A06 has a weight of 64-byte locations. As an example, the jumper arrangement shown in Table 5.4.2-1 would produce a board address of NNNN8840 HEX.

I/O access mode is programmed by selecting address modifier AM2 with jumper J21. Short supervisory access is selected by omitting the jumper. Short nonprivileged access is selected by installing the jumper.

*The value NNNN depends on the make and model of CPU board used.

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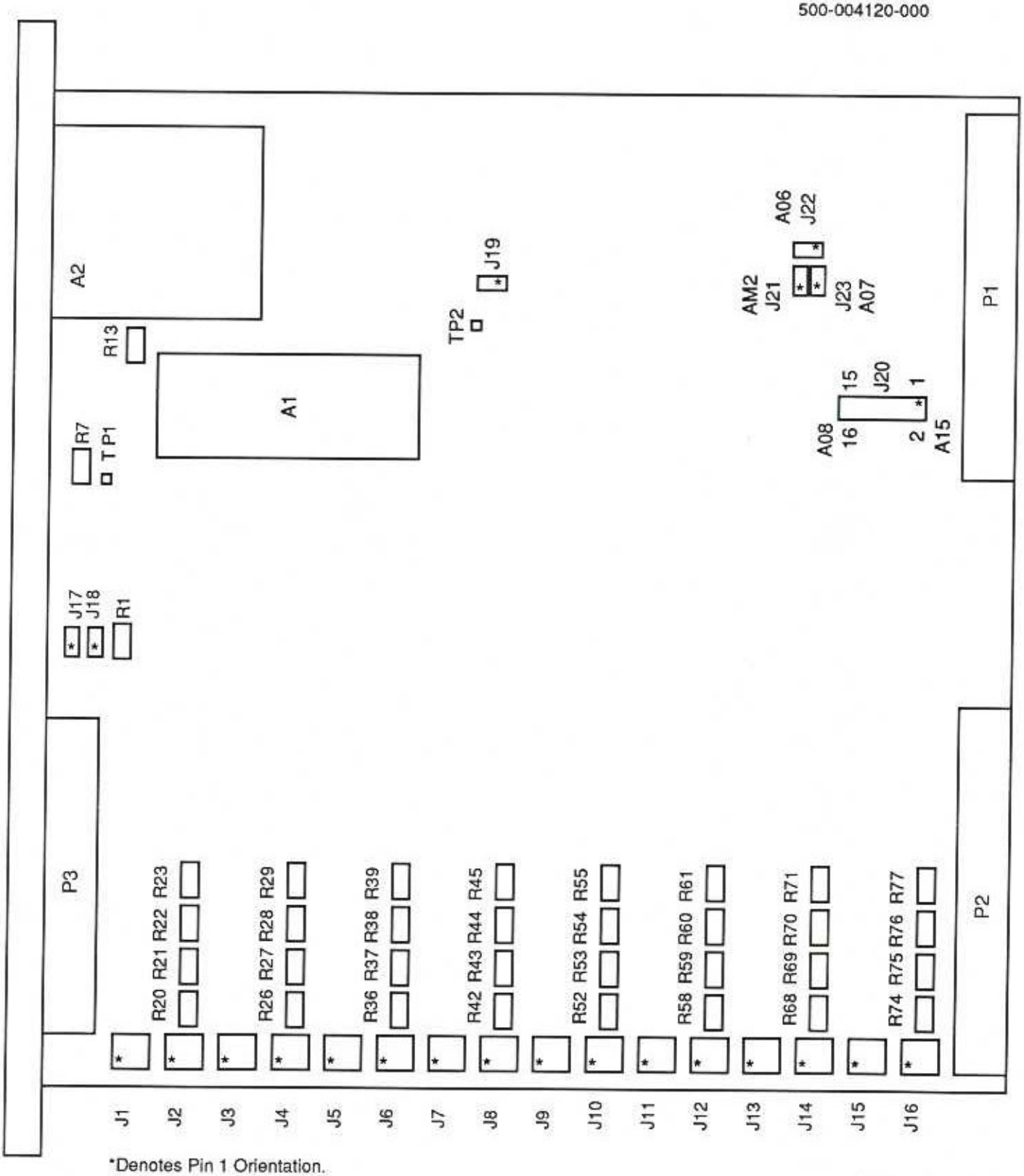
Table 5.3-1. Programmable Jumper Functions

JUMPER	FUNCTION	FACTORY CONFIGURED**
J20-1,2	BOARD ADDRESS BIT A15 = 0	INSTALLED
J20-3,4	BOARD ADDRESS BIT A14 = 0	INSTALLED
J20-5,6	BOARD ADDRESS BIT A13 = 0	INSTALLED
J20-7,8	BOARD ADDRESS BIT A12 = 0	INSTALLED
J20-9,10	BOARD ADDRESS BIT A11 = 0	INSTALLED
J20-11,12	BOARD ADDRESS BIT A10 = 0	INSTALLED
J20-13,14	BOARD ADDRESS BIT A09 = 0	INSTALLED
J20-15,16	BOARD ADDRESS BIT A08 = 0	INSTALLED
J23-1,2	BOARD ADDRESS BIT A07 = 0	INSTALLED
J22-1,2	BOARD ADDRESS BIT A06 = 0	INSTALLED
J21-1,2	SHORT SUPERVISORY ACCESS	OMITTED
J19-1,2	"8 CH L" (NOT USED)	OMITTED
J18-1,2	UNIPOLAR OPERATION	INSTALLED
J18-2,3	BIPOLAR OPERATION	OMITTED
J17-1,2*	10 V FULL SCALE RANGE	INSTALLED
J17-2,3*	5 V FULL SCALE RANGE	OMITTED
J1→J16	SEE FIGURE 5.4-2	

*The J17 jumper is omitted for the 20 V FSR.
**The factory configuration shown is for the VMIVME-4120-000 option.

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*Denotes Pin 1 Orientation.

M4120/F5.4-1

Figure 5.4-1. Locations of Programmable Jumpers, Adjustment Potentiometer, and Test Points

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Table 5.4.2-1. Example Board Address (NNNN8840 HEX) Selection

JUMPER	ADDRESS BIT	STATE*
J22-1,2	A06	OPEN
J23-1,2	A07	SHORTED
J20-15,16	A08	SHORTED
J20-13,14	A09	SHORTED
J20-11,12	A10	SHORTED
J20-9,10	A11	OPEN
J20-7,8	A12	SHORTED
J20-5,6	A13	SHORTED
J20-3,4	A14	SHORTED
J20-1,2	A15	OPEN

*Shorted = "zero" (Jumper installed).
Open = "one".

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5.4.3 Analog Voltage Output Mode

Figure 5.4.3-1 shows how to configure each individual channel for voltage output mode.

5.4.3.1 Output Voltage Range

Output voltage range is controlled by jumper J17. The maximum full scale range is 20 V. To modify the full scale range to 10 V or 5 V, configure jumper J17 as indicated in Table 5.3-1. The 20 V full scale range is selected by omitting the J17 jumper entirely.

5.4.3.2 Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog voltage outputs is selected with jumper J18, as indicated in Table 5.3-1.

5.4.4 Analog Current Output Mode

Figure 5.4.3-1 shows how to configure each individual channel for current output mode at any of the specified ranges. In order to produce current loop outputs, the voltage outputs must be configured for unipolar operation. Typically the voltage range is set to 0 to +10 V to produce 4 to 20 mA, 0 to 20 mA or 5 to 25 mA. A voltage range of 0 to +5 V can be selected to produce 4 to 12 mA, 0 to 10 mA or 5 to 15 mA.

5.5 CALIBRATION

Before delivery from the factory, the VMIVME-4120 Board is fully calibrated and conforms to all specifications listed in Section 2. Should recalibration be required, however, perform the procedures in Sections 5.5.2 with the equipment listed in Section 5.5.1. The locations of all adjustments and test points are shown in Figure 5.4-1. Adjustment potentiometers and their functions are listed in Table 5.5-1.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however. All adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

```
**********
*  CAUTION  *
**********
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DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

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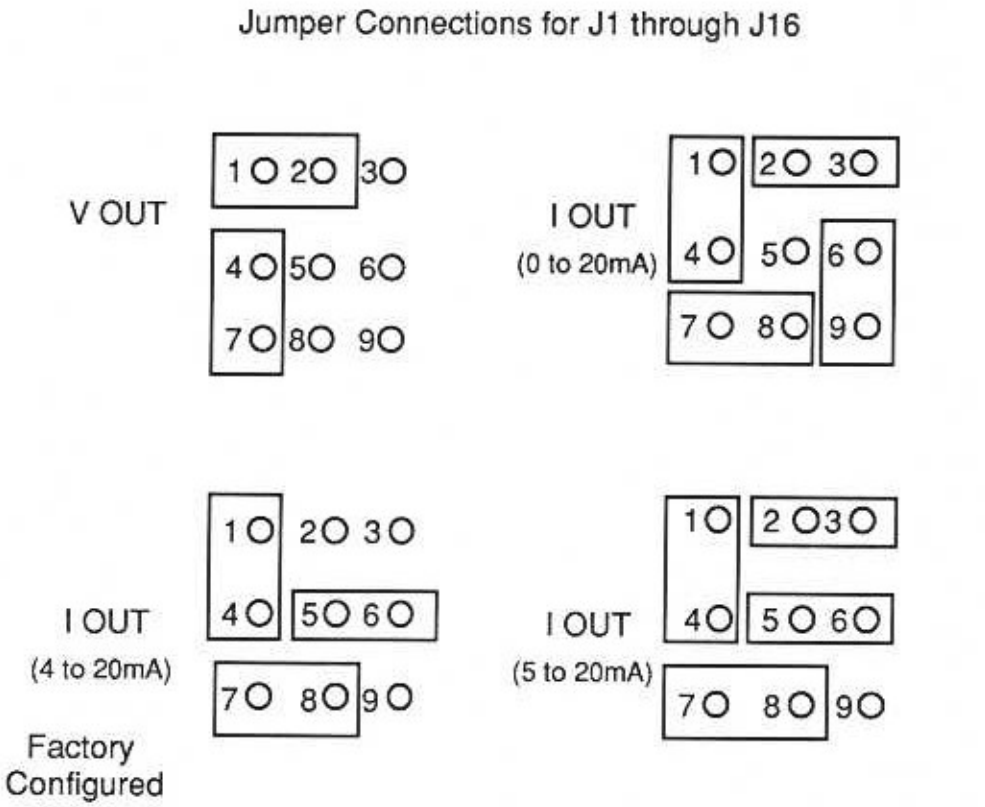


Figure 5.4.3-1. Output Channel Jumper Configurations

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Table 5.5-1. Adjustment Potentiometer Functions

CHANNEL NUMBER	ZERO ADJUST	SPAN ADJUST	
0	R21	R20	CURRENT ADJUSTMENTS
1	R23	R22	
2	R27	R26	
3	R29	R28	
4	R37	R36	
5	R39	R38	
6	R43	R42	
7	R45	R44	
8	R53	R52	
9	R55	R54	
10	R59	R58	
11	R61	R60	
12	R69	R68	
13	R71	R70	
14	R75	R74	
15	R77	R76	

R1	BIPOLAR OUTPUTS ZERO ADJUST	VOLTAGE ADJUSTMENTS
R7	OUTPUTS GAIN ADJUST	
R13	UNIPOLAR OUTPUTS ZERO ADJUST	

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5.5.1 Equipment Required

a. Digital Multimeter (DMM). ±1.0000 VDC and ±10.000 VDC ranges; 5 or more digits; ±0.005 percent of reading voltage measurement accuracy; 10 MΩ minimum input impedance. Current measurements at 1 μA resolution; 5 or more digits.

b. Chassis. VMEbus backplane or equivalent, J1 and J2 connectors, VMEbus master controller, +5 ±0.1 VDC, power supply. One slot allocated for testing the VMIVME-4120 Board. (A ±15 VDC power supply will be required only when calibrating a VMIVME-4120-100 option board.)

c. Extender board. VMEbus extender board.

d. Test cables. Test cables for the equipment listed above.

5.5.2 Analog Outputs Calibration Procedure

The following Sections provide detailed calibration procedures for all of the voltage/current ranges provided by the VMIVME-4120.

Section 5.5.2.1	0 to 10 V
Section 5.5.2.2	0 to 5 V
Section 5.5.2.3	± 2.5 V
Section 5.5.2.4	± 5 V
Section 5.5.2.5	± 10 V
Section 5.5.2.6	4 to 20 mA
Section 5.5.2.7	0 to 20 mA
Section 5.5.2.8	5 to 25 mA

The following procedures are performed with the FAIL LED L bit set to a "one", the TWO'S COMPL L bit set to a "one", and the FAST REFRESH H bit set to a "zero" in the CSR.

NOTICE

CALIBRATON OF OUTPUTS TO A SPECIFIC RANGE DOES NOT NECESSARILY MEAN THAT IF THE JUMPERS ARE RECONFIGURED, THIS CHANNEL WILL STILL BE CALIBRATED.

5.5.2.1 Calibration Procedure for 0 to 10 V Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for voltage outputs (see Figure 5.4.3-1).
c. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

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DAC OUTPUT ADJUSTMENTS:

e. Write 5800 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R13 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +9.9976 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.
l. Calibration of the analog outputs is completed. Remove power and all test connections.

5.5.2.2 Calibration Procedure for 0 to 5 V Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for voltage outputs (see Figure 5.4.3-1).
c. Configure J17 and J18 for unipolar operation and 5 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5800 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R13 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +4.9988 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.
l. Calibration of the analog outputs is completed. Remove power and all test connections.

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5.5.2.3 Calibration Procedure for ± 2.5 V Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for voltage outputs (see Figure 5.4.3-1).
c. Configure J17 and J18 for bipolar operation and 5 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5800 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R1 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +2.4988 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.
l. Calibration of the analog outputs is completed. Remove power and all test connections.

5.5.2.4 Calibration Procedure for ± 5.0 V Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for voltage outputs (see Figure 5.4.3-1).
c. Configure J17 and J18 for bipolar operation and 10 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5800 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).

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h. Adjust potentiometer R1 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +4.9976 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.
l. Calibration of the analog outputs is completed. Remove power and all test connections.

5.5.2.5 Calibration Procedure for ± 10.0 V Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for voltage outputs (see Figure 5.4.3-1).
c. Configure J17 and J18 for bipolar operation and 20 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5800 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R1 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +9.9951 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.
l. Calibration of the analog outputs is completed. Remove power and all test connections.

5.5.2.6 Calibration Procedure for 4 to 20 mA Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for 4 to 20 mA (see Figure 5.4.3-1).

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c. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5C00 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R13 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +9.9976 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.

CURRENT OUTPUT ADJUSTMENTS

l. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a 1 µA or better resolution).
m. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See Table 5.6-2 for P3 connector pin assignments.
n. Write 0000 to relative addresse 20 HEX. See Table 4.1-1 for the VMIVME-4120 memory map.
o. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 4.000 ±0.001 mA.
p. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
q. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 19.996 ±0.002 mA.
r. Span adjustments (Steps p and q) may appreciably alter the offset adjustment and vice versa; therefore, Steps n through q must be repeated as many times as required.
s. Repeat Steps m through r for channels 1 through 15. See Table 4.1-1 for a memory map of VMIVME-4120. See Table 5.3-2 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
t. Calibration of the analog outputs is completed. Remove power and all test connections.

5.5.2.7 Calibration Procedure for 0 to 20 mA Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.

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b. Configure all output channels for 0 to 20 mA (see Figure 5.4.3-1).
c. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5C00 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R13 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +9.9976 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.

CURRENT OUTPUT ADJUSTMENTS

l. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a 1 µA or better resolution).
m. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See Table 5.6-2 for P3 connector pin assignments.
n. Write 0001 to relative addresse 20 HEX. See Table 4.1-1 for the VMIVME-4120 memory map.
o. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 0.005 ±0.001 mA.
p. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
q. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 19.995 ±0.002 mA.
r. Span adjustments (Steps p and q) may appreciably alter the offset adjustment and vice versa; therefore, Steps n through q must be repeated as many times as required.
s. Repeat Steps m through r for channels 1 through 15. See Table 4.1-1 for a memory map of VMIVME-4120. See Table 5.3-2 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
t. Calibration of the analog outputs is completed. Remove power and all test connections.

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5.5.2.8 Calibration Procedure for 5 to 25 mA Output Range

SETUP:

a. Install the VMIVME-4120 Board on an extender board in a VMEbus backplane.
b. Configure all output channels for 5 to 25 mA (see Figure 5.4.3-1).
c. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 5.3-1).
d. Turn ON the power to the VMEbus backplane.

DAC OUTPUT ADJUSTMENTS:

e. Write 5C00 HEX to relative address 02.
f. Connect the (+) lead of the DMM to Test Point No. 1 (TP1). Connect the (-) lead of the DMM to TP2.
g. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
h. Adjust potentiometer R13 for a DMM indication of 0.0000 ±0.0010 VDC.
i. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
j. Adjust potentiometer R7 for a DMM indication of +9.9976 ±0.0010 VDC .
k. Gain adjustments (Steps i and j) may appreciably alter the offset adjustment and vice versa; therefore, Steps g through j must be repeated as many times as required.

CURRENT OUTPUT ADJUSTMENTS

l. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a 1 µA or better resolution).
m. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See Table 5.6-2 for P3 connector pin assignments.
n. Write 0000 to relative addresse 20 HEX. See Table 4.1-1 for the VMIVME-4120 memory map.
o. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 5.000 ±0.001 mA.
p. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
q. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 24.995 ±0.002 mA.
r. Span adjustments (Steps p and q) may appreciably alter the offset adjustment and vice versa; therefore, Steps n through q must be repeated as many times as required.
s. Repeat Steps m through r for channels 1 through 15. See Table 4.1-1 for a memory map of VMIVME-4120. See Table 5.3-2 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
t. Calibration of the analog outputs is completed. Remove power and all test connections.

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5.6 CONNECTOR DESCRIPTIONS

Three connectors, P1, P2, and P3 (Figure 2.1-1), provide all connections to the VMIVME-4120 Board. P1 contains the address, data and control lines, and all additional signals necessary to control VMEbus functions related to the board. P2 provides additional VMEbus power and ground connections as well as the external power connections. P3 provides the connections for the 16 analog output channels.

Orientation of the P2 connector is shown in Figure 5.6-1, and the P2 signal assignments are listed in Table 5.6-1. This information is provided so that the user can supply ±15 VDC to the VMIVME-4120-100.

Orientation of the P3 connector is shown in Figure 5.6-2, and the P3 signal assignments are listed in Table 5.6-2. The mating connector for P3 (Panduit Model 120-332-435E or equivalent) is designed to be used with a standard 32-wire ribbon-cable with a conductor spacing of 0.050 inches. A twisted-pair ribbon cable with an overall shield is recommended for applications involving low level signals in high electrical noise environments.

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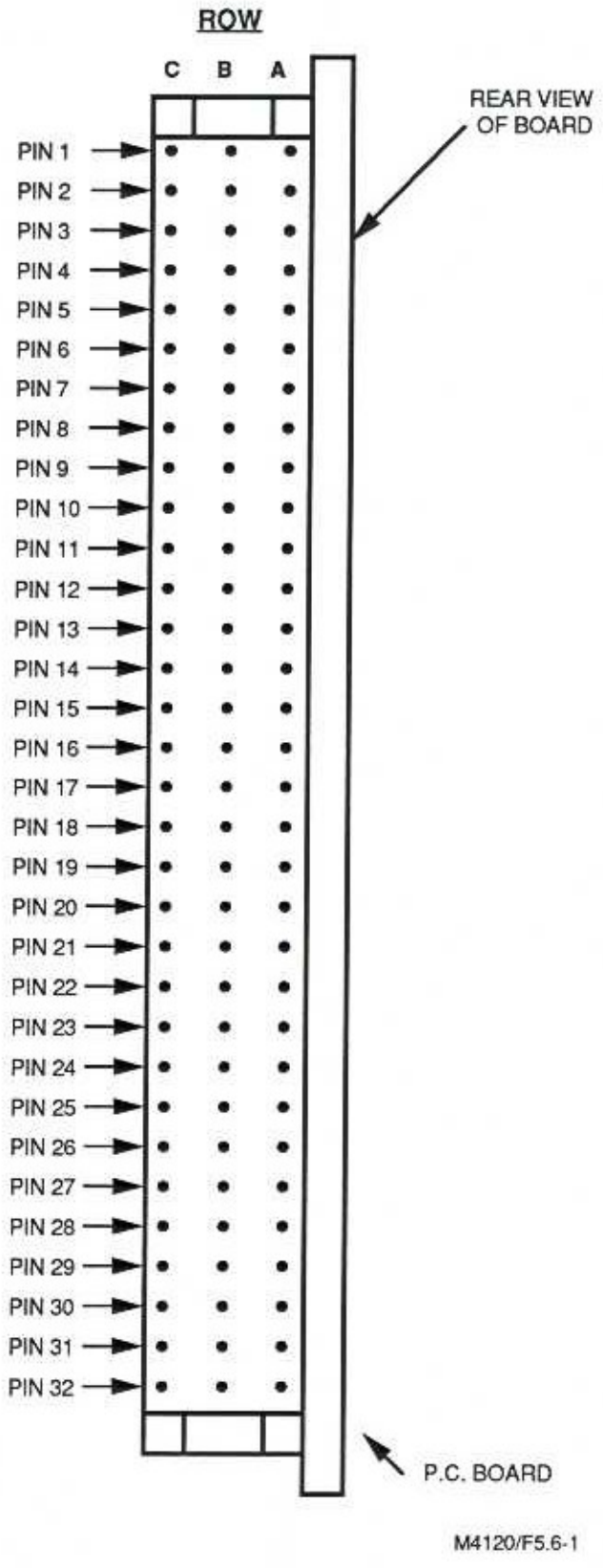


Figure 5.6-1. P1/P2 Connector - Pin Assignments

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Table 5.6-1. P2 Connector Signal Assignments

PIN NO.	A	B	C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25	EXT +15 V		
26	EXT +15 V		
27			
28	EXT ANA COM		
29	EXT ANA COM		
30			
31	EXT -15 V	GND	
32	EXT -15 V	+5 V	

M4120/T5.6-1

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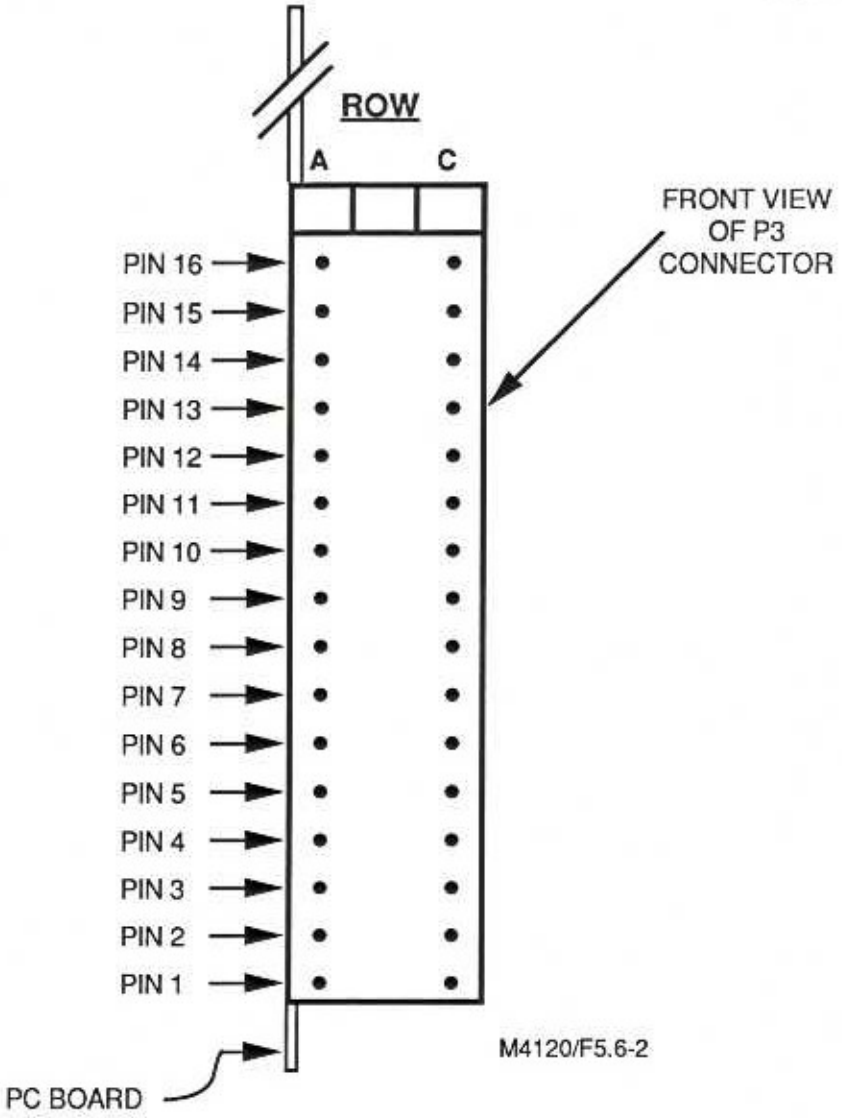


Figure 5.6-2. P3 Connector - Pin Configuration

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Table 5.6-2. P3 Connector Pin Assignments

PIN NO.	A	C
16	CH15 OUT	AGND
15	CH14 OUT	AGND
14	CH13 OUT	AGND
13	CH12 OUT	AGND
12	CH11 OUT	AGND
11	CH10 OUT	AGND
10	CH9 OUT	AGND
9	CH8 OUT	AGND
8	CH7 OUT	AGND
7	CH6 OUT	AGND
6	CH5 OUT	AGND
5	CH4 OUT	AGND
4	CH3 OUT	AGND
3	CH2 OUT	AGND
2	CH1 OUT	AGND
1	CH0 OUT	AGND

M4120/T5.6-2

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SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

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In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

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6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

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6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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