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VMIVME-4514

16-CHANNEL SCANNING ANALOG I/O BOARD WITH BUILT-IN-TEST AND P2 I/O

INSTRUCTION MANUAL

DOCUMENT NO. 500-004514-000 L

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Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

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Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

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DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

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SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



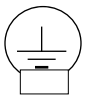
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).


OR

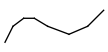

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



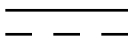
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.


OR

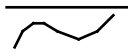

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

```
*****************
*    CAUTION    *
*****************
```

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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16-CHANNEL SCANNING ANALOG I/O BOARD WITH BUILT-IN-TEST AND P2 I/O

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-4514 is a 16-Channel, 12-bit Analog Input/Output (AIO) Board. It provides both the stimulus and the response functions encountered in VMEbus based closed-loop analog systems. The analog signals are available at the P2 backplane connector. It is self-contained, with a resident 12-bit Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC). The board also supports a Built-in-Test feature that checks all of the active components on the board. The VMIVME-4514 provides a single board solution to the analog input/output requirements of such VMEbus applications as process control, simulators, trainers, and supervisory control.

The VMIVME-4514 provides the user with 16 analog outputs with 12 bits of resolution. The outputs are designed with individual Sample-and-Hold (S&H) amplifiers, one per channel. The outputs can be programmed (via on-board jumpers) to operate in a variety of voltage ranges. These ranges are 0 to +5 V, 0 to +10 V (unipolar), ±2.5, ±5.0, or ±10 V (bipolar). Each output can source or sink up to 10 mA at ±10 V. The outputs can be disconnected from the I/O connector for off-line testing.

The board also accepts 16 analog inputs. These inputs may be differential or pseudo-differential (single-ended). A 36 Hz single pole input filter may be ordered for the inputs. The input ADC can be programmed (via on board jumpers) to operate in a variety of voltage ranges. These ranges are 0 to +5 V, 0 to +10 V (unipolar), ±2.5, ±5.0, or ±10 V (bipolar). The inputs have 12 bits of resolution. The inputs can be scanned by on board multiplexers, and the data stored in a dual port memory.

The VMIVME-4514 has three ADC operating modes. They are RANDOM POLLING, SCANNING POLL, and AUTO SCANNING. AUTO SCANNING MODE is entered when power is applied to the board, after a system reset, or under program control. In this mode, all 16 channels are continuously scanned. Their inputs are digitized and stored in sixteen 12-bit dual port registers. No programming is required other than reading the data from these registers. The RANDOM POLLING and SCANNING POLL modes will be described later in this manual.

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A brief overview of the principal features of the VMIVME-4514 illustrates the flexibility and the performance that is available with this board:

a. 16 differential or single-ended analog input channels
b. 16 analog output channels with 10 mA drive capability
c. On board 12-bit ADC and DAC
d. Three A/D operating modes:
    1. AUTO SCANNING MODE
    2. SCANNING POLL MODE
    3. RANDOM POLLING MODE
e. Powers up in AUTO SCANNING MODE — no software initialization required
f. Input and output voltage ranges are jumper-selectable as 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, ±10 V
g. Optional low pass filter is available for analog input noise elimination and anti-aliasing
h. Program-controlled off-line operation of analog outputs
i. A/D data coding is program-selectable as either binary, offset binary, or two's complement format
j. Total acquisition and conversion time is 25 µsec resulting in 40 kHz maximum throughput
k. All inputs and outputs are protected against line transients and short circuits
l. Front panel Fail LED indicator
m. Double Eurocard form factor
n. Individually coded/keyed VME connectors
o. P2 I/O connections

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-4514 is a self-contained, 16-channel, 12-bit Analog I/O Board. Figure 1.2-1 is a block diagram of the board and Figure 1.2-2 is a photograph of the board. The analog inputs are user-selectable either as single-ended (pseudo-differential) or as differential-pair channels. Each of the 16 analog outputs will supply up to 10 mA of drive current. The outputs can be operated off-line for both loopback self-testing and for single-point analog input/output applications. Built-in-test checks all of the active components on the board. It is done by looping back either the on-line or off-line analog outputs to the analog input's DAC via the input multiplexers.

An on board ADC smart controller with a channel sequencer provides the highest throughput with minimal CPU intervention. This sequencer is used in the scanning modes. In these modes each channel is converted and stored in a dual

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port register which is accessible from the VMEbus. The block diagram of the VMIVME-4514 shown in Figure 1.2-1 illustrates the board's components and their basic functions.

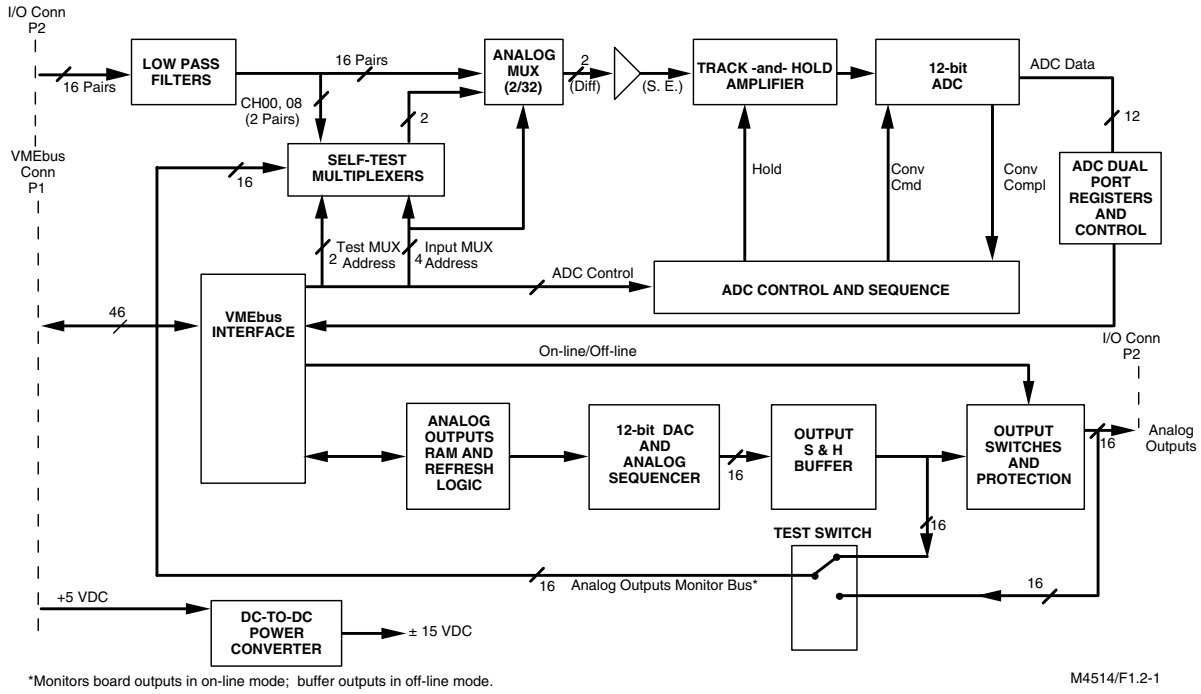


Figure 1.2-1. VMIVME-4514 Functional Block Diagram

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Photograph not available at this time.

Figure 1.2-2. Photograph of the VMIVME-4514 Board

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1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Product (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004514-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-4514 is a 16-channel, 12-bit Analog Input/Output (AIO) Board which is designed to operate in a standard VMEbus system. The board is self-contained with a resident 12-bit Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC), as well as, loopback circuitry to support the self-test feature. There is an on-board smart sequencer that allows the board to continuously scan the inputs.

This scanning mode converts the input signal and stores it in some on-board dual port memory. This simplifies the programming of the board. The user only has to read the register associated with the input in question to get the latest data.

The VMIVME-4514 does not require additional boards to provide high quality analog input and output functions. The VMIVME-4514 is a flexible element in an analog I/O system. It offers Built-in-Test and off-line operating features not found in many other products.

3.2 INTELLIGENT I/O CONTROLLER

The VMIVME-4514 can be used in a VMIC Intelligent I/O Controller (IIOC). The IIOC consists of up to three 680XX Central Processing Units (CPUs) and their coprocessors, global memory, a host computer interface, VMIC firmware, and a variety of VMIC board level products. The IIOC is designed to give the user a total turnkey solution to a VMEbus system design.

3.3 FUNCTIONAL ORGANIZATION

The VMIVME-4514 is divided into the following functional categories, as illustrated in Figure 3.3-1. All of these functions are discussed in detail in this section.

a. VMEbus interface.
b. ADC control.
c. A/D conversion and timing.
d. Analog input filters and multiplexer.
e. DAC and analog distributor.

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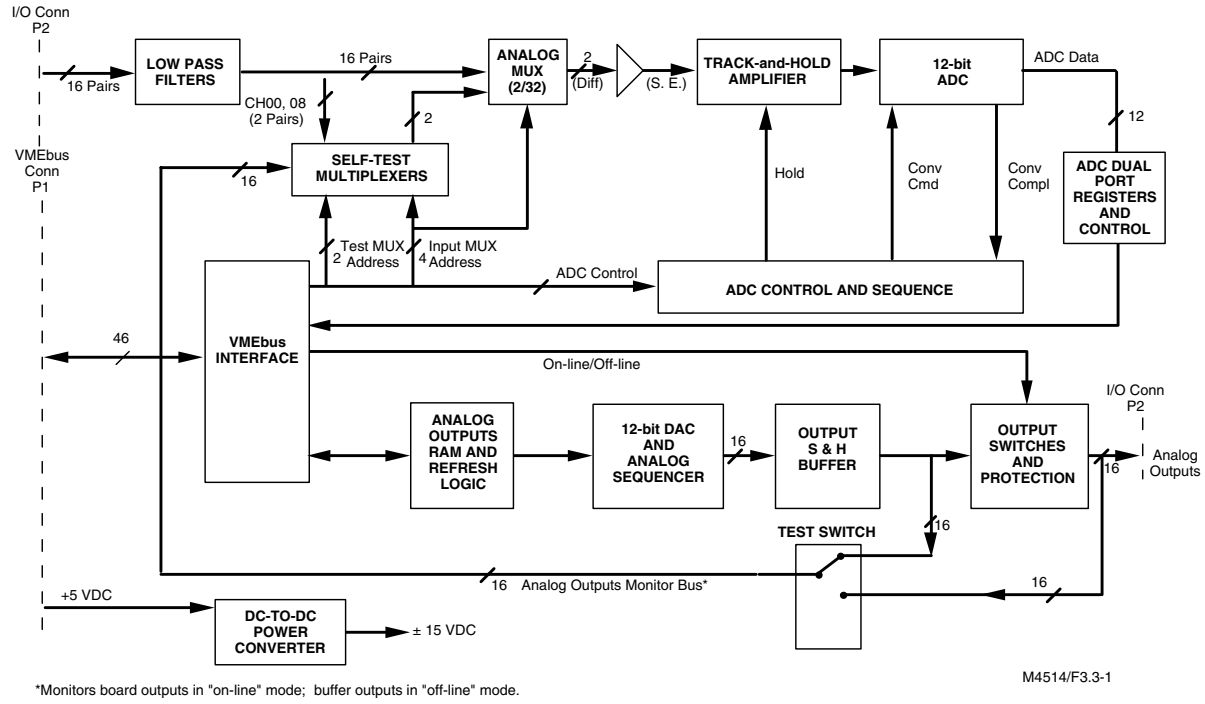


Figure 3.3-1. VMIVME-4514 Functional Block Diagram

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f. Analog output buffers and switches.
g. Analog output refresh logic.
h. Self-test multiplexers.
i. Power converter.

3.4 VMEbus INTERFACE

The VMIVME-4514 communications registers are memory mapped as 64 (decimal) 16-bit words. The registers are contiguous, and may be user-located on any 128-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged.

During each read or write operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers (shown in Figure 3.4-1) and the address and address modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted (driven LOW). Subsequent removal of the Central Processing Unit (CPU) read or write command causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communications with the board, as follows:

a. Data Bus lines D00 to D15.
b. Address lines A01, A02, A03, A04, A05, A06.
c. Bus Control Signals:

    1. WRITE*.
    2. DS0,* DS1*.
    3. SYS CLK.
    4. SYS RESET*.

The Data Bus lines are bi-directional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all of the data devices on the board.

Address lines A01 through A06 map the 64 communication registers into a 128-byte range within the VME address space (Section 4). The control signals determine whether data is to be moved to the board (write) or from the board (read), provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all timers and flags.

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Static controls are latched into the Control Register and are used primarily to establish the operating mode of the board. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC, are read through the Status Register. The control and status registers are referred to collectively as the Control and Status Register (CSR), since they are at the same address. The WRITE* signal determines which one is accessed. Most of the Control Register outputs can be monitored directly through the Status Register.

Each of the 16 analog output channels is controlled by writing 12-bit right-justified data into a dedicated 16-bit read/write register. The 16 analog output control registers constitute the VME port of a 16-word dual port memory. The other memory port is controlled by the analog output refresh logic.

3.5 ADC CONTROL

Control commands and status flag's bit locations associated with controlling the ADC are described in more detail in Section 4 of this manual. There are two mode control bits in the CSR used by the ADC. They are called A/D Mode 1H and A/D Mode 0H. The state of these bits determines which one of the three possible operating modes the ADC will use. The following truth table shows these functions:

A/D Mode 1H	A/D Mode 0H	ADC Operating Mode
0	0	AUTO SCANNING
0	1	RANDOM POLLING
1	0	SCANNING POLL
1	1	Not Used

The ADC operating mode basically determines if the ADC and the channel selection logic are controlled externally by a CPU or internally by the on-board channel sequencer. The programming associated with these operating modes will be described in Section 4 of this manual. The following discussions are here to reveal the ADC controls and timing intervals.

3.5.1 AUTO SCANNING MODE

The AUTO SCANNING MODE is the default mode of operation. It is entered after power is applied to the board, a hardware system reset, or when a program clears the A/D mode control bits (A/D Mode 1H and A/D Mode 0H) to "zeros" in the CSR. This mode performs a sequential scan of all the inputs, digitizing their values and storing this data in a dual port register. Once all of the inputs have been digitized, the process starts all over at the first channel. The VMEbus has access to this data at any time. Whenever a channel is read, the latest data is used. This mode frees the programmer from much of the overhead required to process analog conversions. This can allow the board to digitize the inputs at a faster rate; increasing throughput. If the Scan Size Register (SSR, located at offset 06) is

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loaded, then only the indicated number of channels will be scanned. If input filters are going to be used, then all 16 channels must be scanned. This prevents the filter caps from injecting a "pumpback" current error to the ADC. Any unused input should be grounded.

3.5.2 RANDOM POLLING MODE

To enter this mode, the CSR A/D Mode 1H and A/D Mode 0H bits must be set to "zero" and "one," respectively. In this mode, the CPU controls and monitors every aspect of a conversion. It must select the channel to convert and start the conversion. The CPU must wait for the conversion to finish, then check (or poll) a status bit in the CSR (end-of-conversion). When it is asserted, this tells the program that the conversion is complete. The host can now read the data. This mode is called "random" because the CPU can select the channel to use in any order (i.e., CH2, CH0, CH8, CH14, CH2, etc.). This is the only mode which can be used to self-test the outputs.

3.5.3 SCANNING POLL MODE

The SCANNING POLL MODE is very similar to the AUTO SCANNING MODE. This mode does everything the AUTO SCANNING MODE does except it does only one (1) scan of the inputs. An "end-of-scan" status bit must be polled to determine when the scan is complete. To start this mode, the A/D Mode 1H and A/D Mode 0H control bits in the CSR must be set to "one" and "zero," respectively. The SSR must be loaded prior to starting the first scan.

3.5.4 Scan Size Register

The SCANNING POLL MODE and the AUTOSCAN MODE do not necessarily convert all 16 inputs. If fewer than 16 inputs are used, higher throughput is possible by scanning only the lowest numbered input channels. For example, if the SSR is loaded with 8, only the Channels 0 through 7 will be scanned. The SSR is at offset address 06 from the VMIVME-4514's base address. Its use is optional in the AUTOSCAN MODE (16 channels will be assumed). It must be loaded prior to using SCANNING POLL MODE.

3.6 A/D CONVERSION AND TIMING

Regardless of which ADC operating mode described in Section 3.5 is used, the A/D conversion sequence is the same. All of the ADC timing intervals discussed in this section are performed automatically by the on-board controller. Program control consists basically of some handshake sequences (start something, wait for it to finish, and then poll a status bit to confirm it).

3.6.1 Converter Controls and Status Flags

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Once the conversion sequence has begun (initiated by one of the above A/D operating modes), it consists of the following *consecutive* time intervals:

a. Settling delay.
b. Tracking interval.
c. A/D conversion.

The settling delay occurs directly after a state change has occurred in the analog networks (such as selecting a new input channel). It represents the settling time of the networks. After the settling delay has been completed, the Track-and-Hold (T&H) amplifier (Figure 3.3-1) enters the tracking mode, and the tracking interval begins. During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage.

The SETTLING BUSY flag is a handshake signal that tells the CPU when the input has settled to its input value. It is set HIGH at the beginning of the settling delay, and is cleared LOW at the end of the tracking interval. Any START SETTLING commands issued when this flag is set will be ignored.

At the end of the tracking interval, the T&H amplifier enters the HOLD MODE. The amplifier's output is held at a constant level. Now if the board is controlling the conversions, a CONV CMD from the timing decoder is issued. If the CPU is controlling the conversions, it must set the EN START CONV control bit in the CSR. Either way this causes the A/D conversion to begin. The A/D conversion digitizes the output of the T&H amplifier into a 12-bit data word. It then terminates the conversion sequence. The CONV COMPL L flag from the ADC is HIGH during the conversion, and is LOW otherwise. The EN START CONV control bit sets the CONV BUSY flag HIGH. It remains HIGH until the conversion sequence has been completed.

In the RANDOM POLLING MODE, completion of the A/D conversion causes the NEW DATA RDY flag to be set HIGH, indicating that valid data is present in the Converter Data Register (CDR). This register is only used by the RANDOM POLLING MODE. The action of reading the CDR clears the NEW DATA RDY and CONV BUSY flags to the LOW ("zero") state.

In the SCANNING POLL MODE, when the A/D conversion is completed on the last channel to be scanned, the REGD END OF SCAN flag is set in the CSR. This flag can be polled to determine when all of the channels have been converted and their data is available to be read.

The on-board smart ADC controller uses a microsecond timer. The microsecond timer uses the 16 MHz system clock to generate the TRACKING and CONV CMD control signals for the converter. It also provides the settling time delay. The CSR contains a SHORT SETTLING control bit. Setting this bit HIGH provides increased throughput by reducing the time allocated to both the settling delay and

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the tracking interval.

3.7 ANALOG INPUTS

Sixteen differential or single-ended analog input channels are available at the rear panel through the P2 connector. By connecting the analog return in the remote device to the INPUT GROUND SENSE input on the P2 connector as shown in Figure 3.7-1, the single-ended lines can be operated as pseudo-differential inputs. However, it is recommended that the differential mode be used for increased noise and common mode rejection. All VMIVME-4514 input channels are overvoltage protected by current-limiting input resistors. See document number 800-004514-000 for the input overvoltage specifications. All unused inputs should be grounded.

3.7.1 Low Pass Filters and Input Multiplexer

The 16 analog input channels can be provided with individual, single pole, low pass filters as shown in Figure 3.7-1, and can be user-configured to operate either as single-ended or differential. See document number 800-004514-000 for the input filter specifications.

To achieve maximum system accuracy with filtered analog inputs, the sample rate should be limited to 2,000 Hz or less per channel. Higher sample rates will produce reflected or "pumpback" currents at the inputs which can induce error voltages across the filter input resistors. Thus, when the filters are installed, all 16 channels must be used in the AUTO SCANNING MODE.

Each of the 16 analog inputs is selectable through one of two input multiplexer sections. Each input multiplexer accepts eight differential input pairs. A second tier of multiplexers receives the selected channel from one of the input multiplexers. Both multiplexer sections are controlled by the same set of four address lines (INP MUX ADDRESS) which are derived from control bits "MUX A00" through "MUX A03" in the Control Register.

3.7.2 Single-Ended Operation

Differential or single-ended operation of the analog inputs is selected by the location of Single-In-line-Package (SIP) resistors as illustrated in Figure 3.7-1. The input multiplexers are always operated in the differential mode. Single-ended (pseudo-differential) operation is obtained by positioning the "LOW" input resistor so that it connects to the common INPUT GROUND SENSE input instead of to the individual "LOW" signal inputs.

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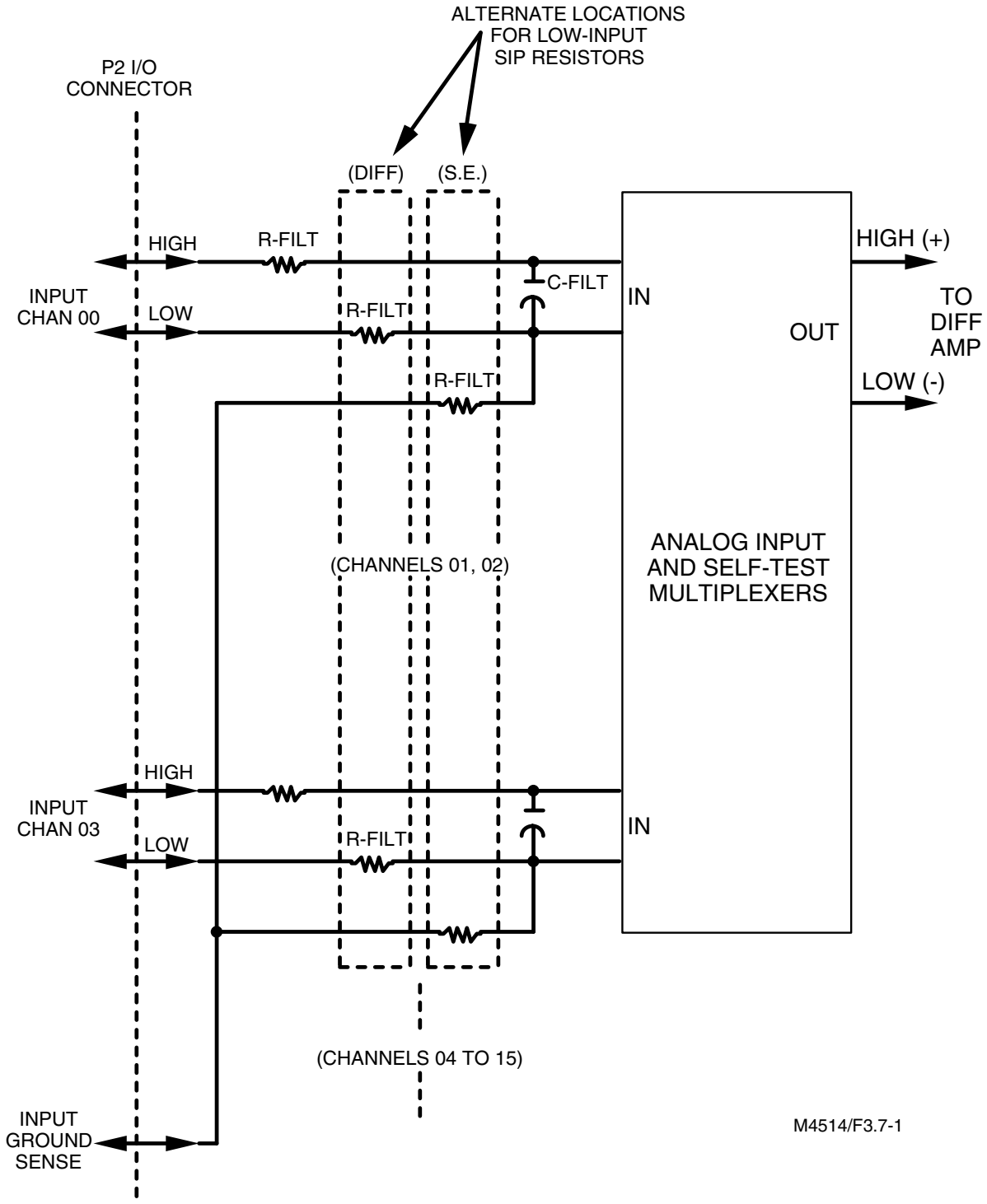


Figure 3.7-1. Single-Ended and Differential Input Configurations

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3.8 ANALOG OUTPUTS

In addition to the analog inputs, there are 16 analog outputs available at the P2 connector. The analog outputs are updated (refreshed) periodically from the dual port memory by a refresh control logic, as illustrated in Figure 3.8-1. Each output receives an update once every 1.7 msec in the default refresh mode. A program controlled FAST REFRESH flag can be used to reduce the refresh cycle time to approximately 0.4 msec, and thereby raising the maximum output sampling rate from 550 Hz to 1.6 kHz.

3.8.1 Digital-to-Analog Converter (DAC)

All 16 analog outputs are serviced by a single 12-bit DAC. The DAC is controlled by the refresh control logic. This logic periodically transfers data from the dual port memory's refresh port to the DAC. This logic simultaneously connects the DAC to the appropriate section of the analog distributor. The analog output data is placed in the dual port memory through the VME port by the controlling processor.

3.8.2 Analog Distributor

The analog distributor consists of the following elements:

a. One of 16 decoders.
b. Low charge injection analog demultiplexer.
c. Sixteen capacitive storage elements.

As the DAC is updated with data for each channel in the output refresh sequence, the decoder receives the same four address lines used by the dual port memory. In this manner, the converted analog level is always routed to the distributor section which corresponds to the dual port memory location for the same channel. After allowing the DAC to settle, the refresh logic enables (turns ON) the demultiplexer. Then the converted voltage level is transferred to the corresponding storage capacitor. After a settling interval of approximately 100 µsec is provided by the REFRESH logic, the demultiplexer is disabled and the next channel in the REFRESH sequence is processed.

3.8.3 Output Buffers and Switches

Voltage levels stored by the analog distributor are buffered and then switched to the P2 connector for routing through system I/O cables. The output buffers are low leakage, precision operational amplifiers which can supply 10 mA of drive current over the full available output voltage range (up to ±10 V). These buffers can withstand sustained short circuits-to-ground without damage.

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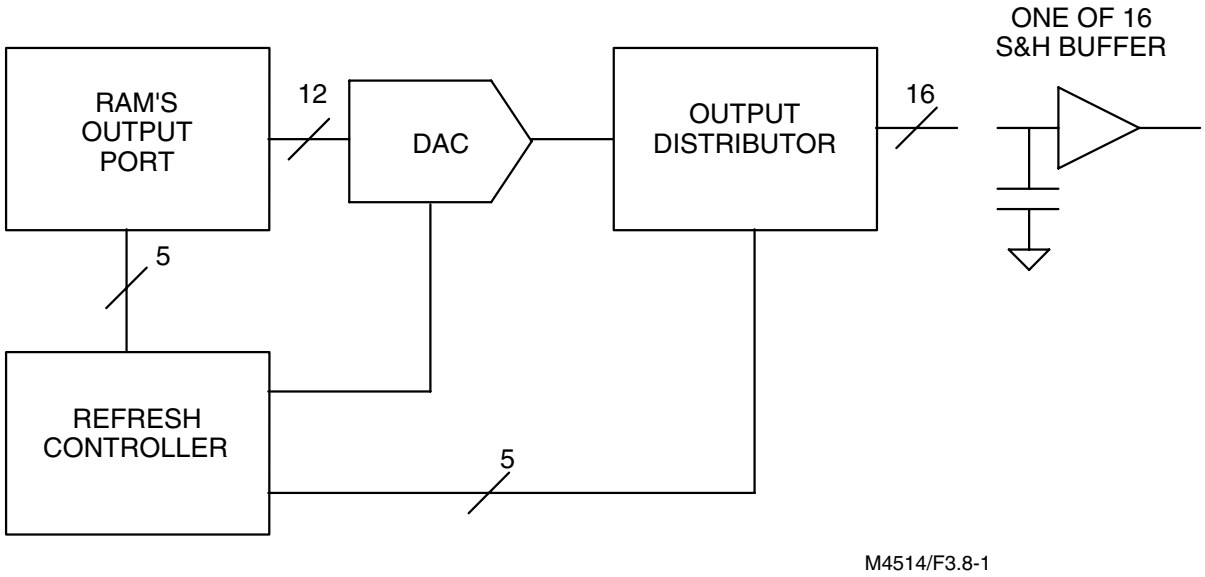


Figure 3.8-1. Analog Outputs Block Diagram

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Output switches permit the analog outputs to be disconnected from the P2 connector for "off-line" self-testing and for low impedance, single-point analog input/output system applications. To eliminate the effect of switch resistance on the output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operation. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ±15 V supply rails.

3.8.4 Data RAM and Refresh Control

The dual port memory which services the analog outputs is organized as a 16-bit wide, 16-location array, in which each location can be accessed from either of the two ports. The VMEbus port is used by the VME host to load the analog output data into the memory. These accesses may be made in any order. The digital codes are then transferred sequentially through the DAC port to the DAC. Then they are converted into voltage levels and subsequently distributed to the appropriate analog output channels. A flowchart of the BASIC REFRESH logic control sequence is shown in Figure 3.8.4-1.

Operation of the dual port memory is controlled by the REFRESH control logic. This circuitry derives its timing from the 16 MHz system clock. The REFRESH control logic supervises all data transfers between the memory and the DAC, and controls the distribution of analog voltages to the analog outputs. (Refer to the preceding sections for specific functions of the REFRESH logic.) Because the dual port memory must be accessed through both the VMEbus and DAC ports (and possibly by the ADC) arbitration logic is employed during the transfer of data to the DAC to ensure that only one port is active at any time.

3.9 BUILT-IN-TEST (BIT)

Self-test provisions in the VMIVME-4514 design permit program-controlled verification of all active components on the board. The following paragraphs explain how this is done.

3.9.1 Self-Test Multiplexers

The signal routing paths and multiplexers involved in board level self-test are shown in Figure 3.9.1-1. The 16 analog outputs are decoded by the output monitor multiplexer onto a single line which is, in turn, connected by the self-test multiplexer to the input of an analog input multiplexer. This arrangement permits any one of the analog outputs to be sampled by the ADC. It also verifies the operation of the analog input multiplexers by exercising them with known signal levels.

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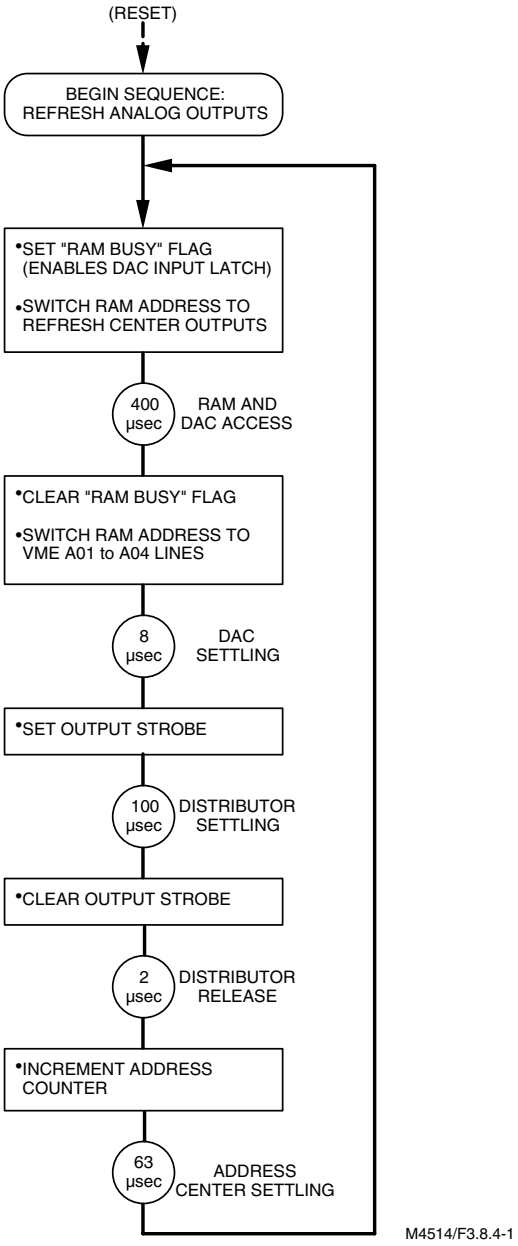


Figure 3.8.4-1. Analog Outputs Refresh Logic; Flowchart

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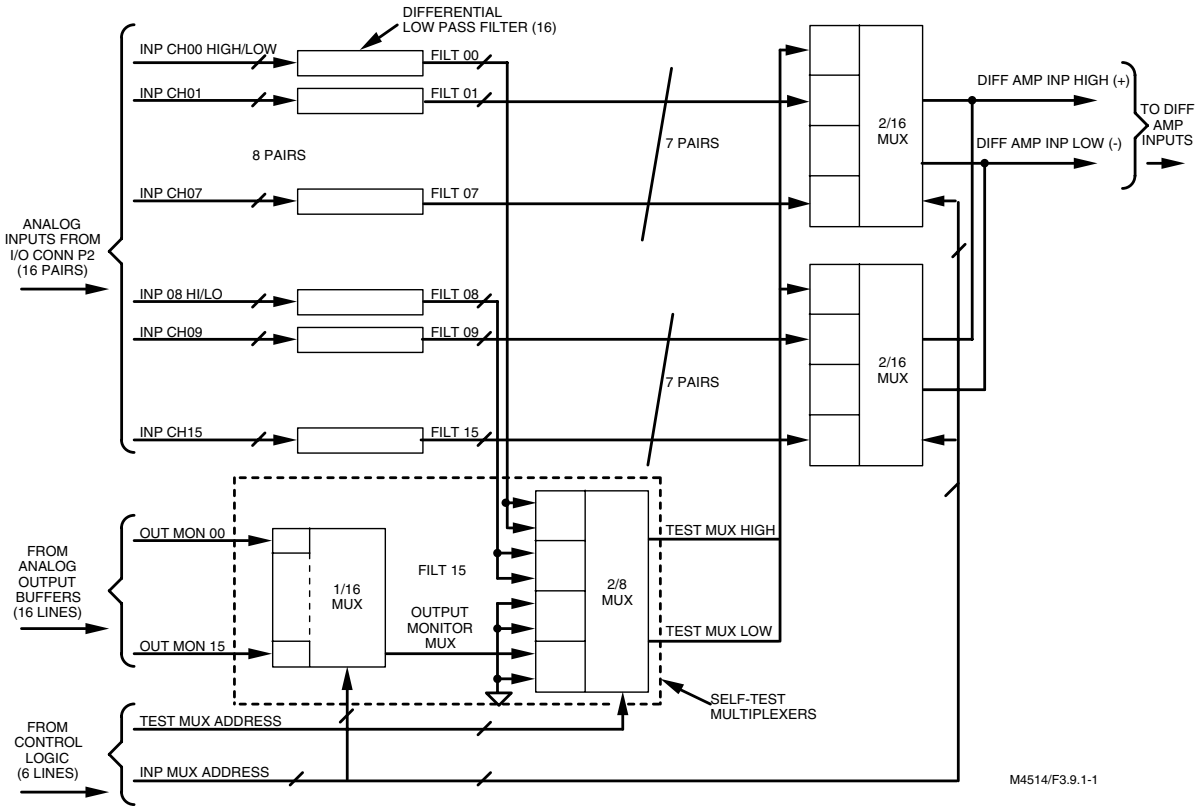


Figure 3.9.1-1. Analog Inputs and Signal Routing

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In addition to accepting the selected analog output signal, the self-test multiplexer permits the HIGH and LOW inputs of the differential amplifier to be switched simultaneously to signal return. This feature provides a precision "zero" signal for software to use in correcting common "zero" offsets in the analog input channels. There will rarely be a need for this software adjustment. It is used when the input hardware is poorly or strangely calibrated.

Because the high input side of two input signals are used by the output monitor multiplexer (Channels 00 and 08), the low input side of these channels are also routed through this multiplexer. This will give both input lines of these channels the same path impedance and eliminate any offsets due to different input path impedances.

3.9.2 Loopback Testing of Inputs and Outputs

By routing the analog outputs back through the analog input multiplexers, all of the active components on the board can be exercised in a "loopback" arrangement. The controlling processor can perform a loopback test in either the on-line or off-line mode by setting the output monitor switches appropriately. Then, by sending a specific code to a specific output channel and verifying that the ADC produces approximately the same code after sampling the same channel, the user can verify the operations of the board. Random polling mode is the only mode that can be used for loopback testing on the analog outputs. This technique is described in Sections 3.5.2 and 4.4.3.

3.10 BUILT-IN POWER CONVERTER

Electrical power for the VMIVME-4514 analog circuitry is supplied by the DC-to-DC converter shown in Figure 3.10-1. This converter transforms +5 V logic power into a regulated and isolated ±15 VDC power source for the analog circuitry, with a load capacity of approximately 300 mA on each 15 V bus.

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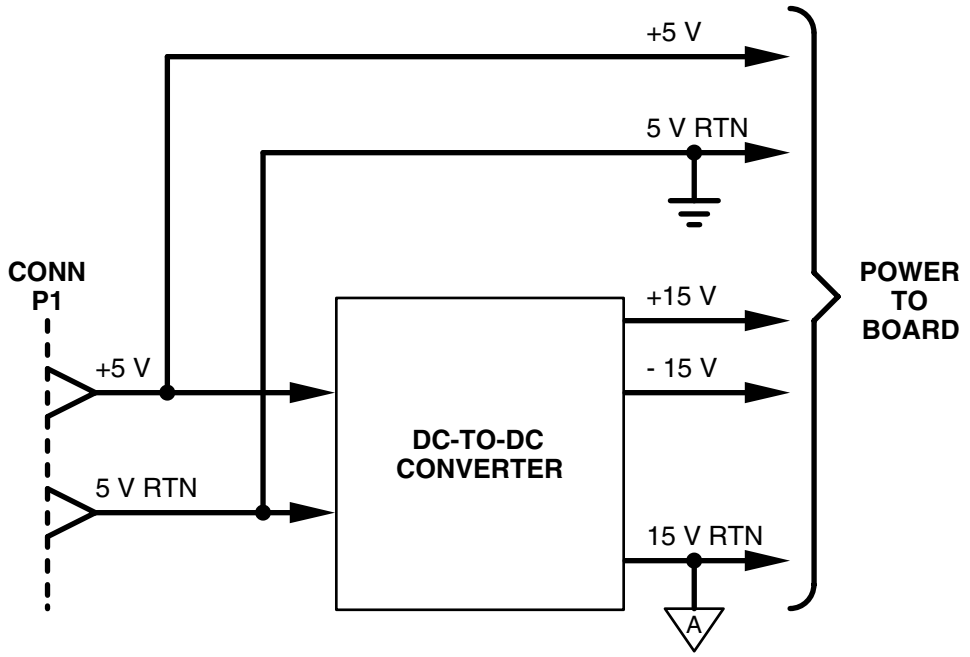


Figure 3.10-1. Power Converter

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION

Communication with the VMIVME-4514 Analog I/O (AIO) Board takes place through 64 contiguous 16-bit register locations mapped into the VME short I/O address space. The short I/O address space consists of all locations within the address range from XXXX0000 HEX to XXXXFFFF HEX*. The function of each communication register and its offset address is summarized in Table 4.1-1. These registers will be discussed in more detail in this section of the manual.

4.2 CONTROL AND STATUS REGISTER DESCRIPTIONS

The Control and Status Register (CSR) located at relative (or offset) address 02H contains all of the flags necessary to control and monitor the following board operations:

a. Analog input channel selection.
b. Analog-to-Digital (A/D) conversion.
c. Built-in-Test (BIT).
d. Analog outputs on-line/off-line.
e. Analog outputs refresh rate.
f. Front panel Fail indicator.
g. Board RESET.

The CSR is 16 bits in length. The function of each control bit and status flag is described in Table 4.2-1 and in more detail in the programming discussions that follow.

4.3 INITIALIZATION BY RESET

When a SYSTEM RESET (the VMEbus signal) is applied to the board, all of the bits in the CSR are cleared to the LOW state or "zero". VMEbus systems automatically apply a SYSTEM RESET when they power-up. After SYSTEM RESET is removed, the VMIVME-4514 will AUTOSCAN its inputs, and its outputs will be off-line.

*XXXX indicates "Don't Care" on the upper 16 address lines. The VMEbus modifiers indicate access to the short I/O (A16) address space. The CPU will access the short I/O address space via some 32-bit address range. Please refer to the CPU's manual for this information.

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Table 4.1-1. Register Map

Offset Address	Offset Address in DEC	Name	Description (The BD ID and CDR are read only registers. All **in HEX** of the other registers are read/write.)
00	00	BD ID	ID register with a fixed value of $09xx
02	02	CSR	Control and Status flags are stored here
04	04	CDR	Random Poll mode input data is stored here
06	06	SSR	Sets the number of channels to be scanned
08-1E	08-30		RESERVED*
20	32	ODPR00	Output data's Dual Port Register for Channel 00
22	34	ODPR01	Output data's Dual Port Register for Channel 01
24	36	ODPR02	Output data's Dual Port Register for Channel 02
26	38	ODPR03	Output data's Dual Port Register for Channel 03
28	40	ODPR04	Output data's Dual Port Register for Channel 04
2A	42	ODPR05	Output data's Dual Port Register for Channel 05
2C	44	ODPR06	Output data's Dual Port Register for Channel 06
2E	46	ODPR07	Output data's Dual Port Register for Channel 07
30	48	ODPR08	Output data's Dual Port Register for Channel 08
32	50	ODPR09	Output data's Dual Port Register for Channel 09
34	52	ODPR10	Output data's Dual Port Register for Channel 10
36	54	ODPR11	Output data's Dual Port Register for Channel 11
38	56	ODPR12	Output data's Dual Port Register for Channel 12
3A	58	ODPR13	Output data's Dual Port Register for Channel 13
3C	60	ODPR14	Output data's Dual Port Register for Channel 14
3E	62	ODPR15	Output data's Dual Port Register for Channel 15
40	64	IDPR00	Input data's Dual Port Register for Channel 00
42	66	IDPR01	Input data's Dual Port Register for Channel 01
44	68	IDPR02	Input data's Dual Port Register for Channel 02
46	70	IDPR03	Input data's Dual Port Register for Channel 03
48	72	IDPR04	Input data's Dual Port Register for Channel 04
4A	74	IDPR05	Input data's Dual Port Register for Channel 05
4C	76	IDPR06	Input data's Dual Port Register for Channel 06
4E	78	IDPR07	Input data's Dual Port Register for Channel 07
50	80	IDPR08	Input data's Dual Port Register for Channel 08
52	82	IDPR09	Input data's Dual Port Register for Channel 09
54	84	IDPR10	Input data's Dual Port Register for Channel 10
56	86	IDPR11	Input data's Dual Port Register for Channel 11
58	88	IDPR12	Input data's Dual Port Register for Channel 12
5A	90	IDPR13	Input data's Dual Port Register for Channel 13
5C	92	IDPR14	Input data's Dual Port Register for Channel 14
5E	94	IDPR15	Input data's Dual Port Register for Channel 15
60-7E	96-126		RESERVED*

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* Reserved locations are generally duplicates of useful registers. For instance, offset 0A here currently has the same functionality as the formal CSR location. In future revisions, reserved locations may have different effects. It would be poor programming practice to use them.

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Table 4.2-1. CSR Description

MSB LSB

D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00

BIT	NAME	FUNCTION
D15	SHORT SETTLING/ NEW DATA READY	Writing a "one" here will decrease the refresh time and thus increase the input scan rate. When read, this bit shows the status of the CDR. If it is a "one", there is valid data in the CDR for the host to read.
D14	Fail LED	This bit turns ON and OFF the front panel LED. Writing a "one" here will turn off the LED. A "zero" turns it ON.
D13	START CONVERT/ END-OF-SCAN	END-OF-SCAN Writing a "one" to this bit will begin a conversion sequence. Reading a "one" at this bit indicates a scan has finished.
D12	TWO'S COMPLEMENT	When this bit is low, the data format used is two's complement. Write a "one" to this bit to change to offset binary for the data format.
D11	OUTPUTS ON-LINE	Write a "one" to this position when the outputs are to be connected to the external circuits.
D10	TEST MODE 1	The Test Mode bits determine what the loopback registers will monitor.
D09	TEST MODE 0	
D08	FAST REFRESH	Writing a "one" here will decrease the refresh time and thus increase the scan rate for the outputs.
D07	MODE 1	This bit and D04 (Mode 0) establish the operating mode of the board.
D06	START SETTLING/ reads as a logic "zero"	When a "one" is written to this bit, the switching multiplexers will change to the channel stated in the "MUX" address lines (D03 to D00).
D05	SCAN HALT	Writing a "one" here will stop the sequencer. This bit **MUST** be cleared before normal operations can commence.
D04	MODE 0	This bit and D07 (Mode 1) establish the operating mode of the board. (D7) MODE 1 (D4) MODE 0 FUNCTION 0 0 AUTO SCANNING 0 1 RANDOM POLLING 1 0 SCANNING POLL 1 1 Not Used
D03	MUX A3	These bits are used to select the input channel to convert.
D02	MUX A2	
D01	MUX A1	
D00	MUX A0	

M4514/T4.2-1

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4.4 CONTROLLING AND READING THE ANALOG-TO-DIGITAL CONVERTER (ADC)

The VMIVME-4514 has a number of features which allow it to be used in a variety of applications. The simplest mode of operation is the AUTO SCANNING MODE. Activating the other control modes is discussed in Section 4.7.

4.4.1 AUTO SCANNING MODE

This mode is entered when the board has power applied to it, after a hardware reset, or when the A/D mode control bits in the CSR are cleared to "zero." This mode allows the user to operate the board without setting any of the control bits in the CSR or selecting any channel for conversion. When the auto scan is activated, the board initiates a conversion on CH0. When that is finished, the board moves on to CH1 and so on. After CH15 has been digitized, the cycle begins again with CH0.

After each conversion, the data for that particular channel is stored in a dual port register assigned to that input. With every scan, new data is put in the register. This overwrites the old data. Thus, only the freshest data is in the register. This register is accessible by the VMEbus and may be *read* at any time.

To enter the AUTO SCANNING MODE under program control, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be cleared (or set to "zero"). These bits are part of a data word that is written to the CSR. An example of how to enter this mode is shown in Section 4.8.

4.4.2 SCANNING POLL MODE

The SCANNING POLL MODE performs a single scan of all the input channels and then stops. Data bit D13 in the CSR is used by the host CPU to monitor the completion of this scan. D13 is called REGD END OF SCAN H. When it goes high (a logic "one"), the scan is complete and data is ready for the host to read.

To enter the SCANNING POLL MODE under program control, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be set to "one" and "zero," respectively. These bits are part of a data word that is written to the CSR. An example of how to enter this mode is shown in Section 4.8.

4.4.3 Scan Size Register

The SCAN SIZE REGISTER (SSR) is a write only register and is located at relative (or offset) address 06 Hex. This register is used during Auto Scan and Scan

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Poll modes. It can be loaded with a value of 0 through 10 Hex for scanning from 1 to 16 channels. Table 4.4.3-1 shows which channels are scanned when writing to the SSR if utilizing Auto Scan or Sxcanning Poll modes.

At power up or after a system reset, Auto Scanning Mode is entered with all 16 channels scanned. If the user does not wish to Auto Scan all 16 inputs, a value smaller than 10 Hex can be written to the SSR. If the user is using Scan Polling mode, the SSR must be loaded with the desired number of channels to scan prior to starting the scan.

Table 4.4.3-1. Scan Size Register

SSR Programming Value (HEX)	Number of Channels Scanned	Scanned Channels
0	1	0
1	1	0
2	2	0-1
3	3	0-2
4	4	0-3
5	5	0-4
6	6	0-5
7	7	0-6
8	8	0-7
9	9	0-8
A	10	0-9
B	11	0-10
C	12	0-11
D	13	0-12
E	14	0-13
F	15	0-14
10	16	0-15

M4514/T4.4.3-1

4.4.4 RANDOM POLLING MODE

The RANDOM POLLING MODE is the traditional method of controlling an A/D conversion. The CPU selects the channel to be converted. This is done by setting the MUX A3 through MUX A0 bits (D3 to D0) in the CSR to the value for the input in question. At the same time, D13 of the CSR (EN START CONV H) is set HIGH. This starts the multiplexer acquisition and the ADC timing sequence. Section 3.5 has a detailed explanation of this. Now the CPU must poll the NEW DATA RDY H bit (D15) in the CSR. If this is done by successively reading the CSR, digital noise may corrupt the reading. It is better to wait until the conversion time has expired,

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then read the CSR and test the bit. When this bit goes HIGH, the conversion is complete and the data is ready. Finally, the CPU reads the data. A new channel is selected and this process is repeated. Figure 4.4.4-1 is a flowchart for such a process.

This method is useful when the desired channels are not in sequence. Here any channel can be selected in any "random" order. It is also used when the same channel must be converted more often (or exclusively) than the others. This is the only mode which can test the outputs.

Each time a new channel is selected for conversion, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be set to "zero" and "one," respectively. These bits are part of a data word that is written to the CSR. An example of how to enter this mode is show in Section 4.8.

4.4.5 Converter Data Register (CDR)-RANDOM POLLING MODE Only

A 16-bit *read only* register at offset address 04 (HEX) is used to store the data converted during the random poll mode. Data in this register is 12 bits, right-justified. D12 through D15 are always "zero" in the binary or offset binary data mode. In the two's complement data mode they are the sign extension of the data (see Table 4.4.5-1).

4.4.6 Reading ADC Codes

The data format of the ADC is shown in Table 4.4.5-1. This data can be straight binary, offset binary, or two's complement. This is controlled by the configuration of the ADC input range selection jumpers and the state of the TWO's COMPL control bit in the CSR. Some converter output codes are summarized in Table 4.4.5-1. This table shows the values of data produced at major points within the full-scale ranges of the board.

For any offset binary converter code using the BIPOLAR RANGE, the associated input voltage is obtained from the following equation:

$$\text{OUTPUT/INPUT(Volts)} = -E_{FSR}/2 + E_{FSR} \times [\text{CHANNEL DATA IN DECIMAL}] / 4096,$$

where E_{FSR} is the full-scale range voltage. (e.g., E_{FSR} = 10 V for the ±5 V range.)

If the input voltage is for a straight binary code (UNIPOLAR RANGE) or for a two's complement code (BIPOLAR RANGE), then use this equation:

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OUTPUT/INPUT (Volts) = $+E_{FSR}$ X [CHANNEL DATA IN DECIMAL] / 4096.

Note that negative two's complement numbers must be translated to negative decimal output codes, e.g., FC00 (HEX) = -1024 (DECIMAL). If this code is for a +5 V input range, then the input voltage is +1.25 V (1.25 V = +5 V (1024/4096)).

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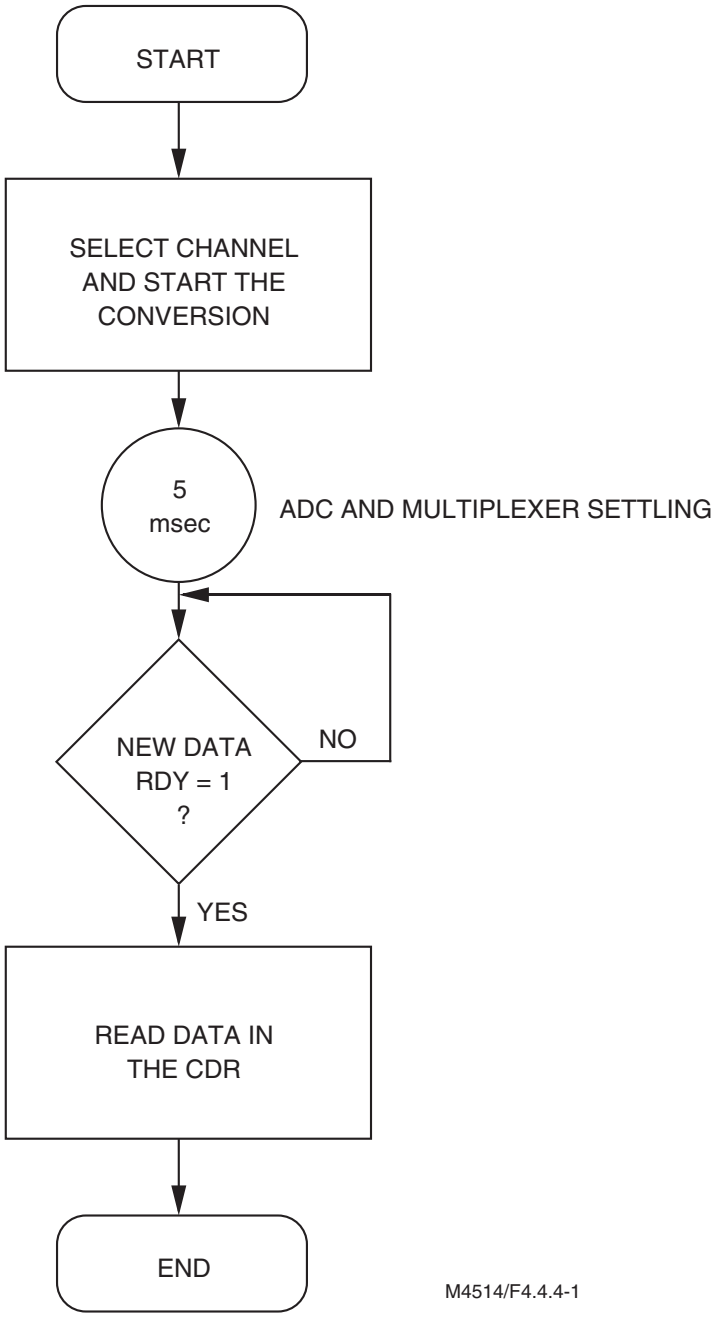


Figure 4.4.4-1. Random Polling Flowchart

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Table 4.4.5-1. Data Formats (in HEX)

Unipolar Voltage	Bipolar Voltage	Offset Binary	Two's Complement
0 V	-10 V	000	800
2.5 V	-5 V	400	C00
5.0 V	0 V	800	000
7.5 V	5 V	C00	400
9.9951 V	9.9951 V	FFF	7FF

M4514/T4.4.5-1

4.4.7 Operating Sequence Examples

Table 4.4.7-1 shows an example of each of the different operating sequences available with the VMIVME-4514. Please note that these examples show only one variation of each possible control word. Other valid control words are formed by adding $8000, $4000, $1000, $800, and/or $100 ($ implies hexadecimal values) to the examples for any write to the CSR.

Table 4.4.7-1. Operation Sequence Examples

MODE	**EXAMPLE SEQUENCE** (all numbers are in hexadecimal)
AUTO SCANNING	1. Read data from the IDPRs (offset addresses 40 through 5E).
SCANNING POLL	1. Write the number of channels (e.g., 10) to the SSR (offset address 06). This must be done after the board is powered-up or whenever a change is desired. 2. Write 2080 to the CSR (offset 02). 3. Wait for the scan to finish. Bit D13 of the CSR will go HIGH. 4. Read the data from the IDPRs.
RANDOM POLL	1. Write 201x to the CSR. X is the desired channel number (0.F). 2. Wait for the conversion to finish. Bit D15 of the CSR will go HIGH. 3. Read the data from the CDR (offset address 04).

M4514/T4.4.7-1

4.5 CONTROLLING THE ANALOG OUTPUTS

The 16 analog output channels appear to the controlling processor as 16 consecutive 16-bit words in the address space assigned to the VMIVME-4514 board starting at an offset address of 20 (HEX). The register map shown in Table 4.1-1 lists the board's offset address for each output channel. Each analog output register supports both read and write operations, eliminating the need for corresponding "shadow" registers in the processor Random Access Memory (RAM) space.

4.5.1 Writing to the Outputs

Digital voltage codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four bits (D12 to D15) will

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be ignored and not retained for read back. The Digital-to-Analog (D/A) data format and coding conventions are shown in Table 4.4.5-1. Each output will respond to a new code within 1.7 msec (0.4 msec in the FAST REFRESH MODE) after the code is written to the Output Register.

4.5.2 "FAST REFRESH"

Setting the FAST REFRESH control bit (Table 4.2-1) HIGH will reduce the analog output REFRESH time from the default value of 1.7 to 0.4 msec. The FAST REFRESH MODE raises the output Nyquist frequency (maximum output signal frequency) from approximately 300 Hz to 1.2 kHz at the expense of some accuracy.

4.5.3 Off-line Operation

Setting the OUTPUT ON-LINE control bit HIGH (Table 4.2-1) connects the analog outputs to the P2 I/O connector for normal system operation. Clearing the bit LOW disconnects the analog outputs from P2 and is normally used for loopback testing because the output buffers can still monitor the outputs through the self-test multiplexers.

4.6 SELF-TESTING THE VMIVME-4514 BOARD

Built-in-Test (BIT) provisions include loopback testing and the measurement of analog input offset voltages. These capabilities permit self-contained, board level performance verification. Random polling mode is the only mode that can be used for self-testing. The control of the self-test modes is summarized in Table 4.6-1 below.

Table 4.6-1. Self-Test Control Modes

Random polling mode is the only mode that can be used for self-testing.

	CSR CONTROL BITS							
SELF-TEST MODE	D10	D9	D7	D4	D3	D2	D1	D0
Normal Operation *	0	0	X	X	X	X	X	X
(Reserved)	0	1	X	X	X	X	X	X
Test Input Offset	1	0	0	1	**	X	X	X
Test Analog Outputs	1	1	0	1	Selected Analog Output Channel			

* With D10 and D9 cleared, 07 and 04 select the mode of operation (see Section 4.4).

** Set this to a "zero" to test the input Channel 00 to 07 multiplexer, or a "one" to test the Channel 08 to15 multiplexer.

M4514/T4.6-1

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4.6.1 Loopback Testing of Inputs and Outputs

By routing the analog outputs through the input multiplexers, the operation of all the active components on the VMIVME-4514 Board can be verified. This loopback test is performed by selecting one of the 16 analog output channels. The selected output channel can then be exercised by the controlling processor, and monitored by the VMIVME-4514 ADC to verify that the signal path is operating correctly. This technique is illustrated in Figure 4.6.1-1.

4.7 CHANGING A/D OPERATING MODES

The board powers-up in the AUTO SCANNING MODE. To switch from AUTOSCAN to another mode, the sequencer **must** be stopped. This will synchronize the timing control logic. The sequence of events is (1) writing a control word that sets the SCAN HALT (D5) bit HIGH and the desired operating mode in the A/D Mode bits (D7 and D4), (2) writing a control word that clears the SCAN HALT (D5) bit LOW *(include the A/D Mode settings from step 1)*, and (3) rewrite the A/D Mode **and set** the START CONV H bit (D13) HIGH in the CSR to start the A/D conversion sequence. Table 4.7-1 shows the proper sequence and some example control words to switch to each of the A/D operating modes. No reset is needed to move between the SCANNING POLL MODE and the RANDOM POLL MODE. Also, no reset is needed to move from one of these modes to the AUTO SCANNING MODE.

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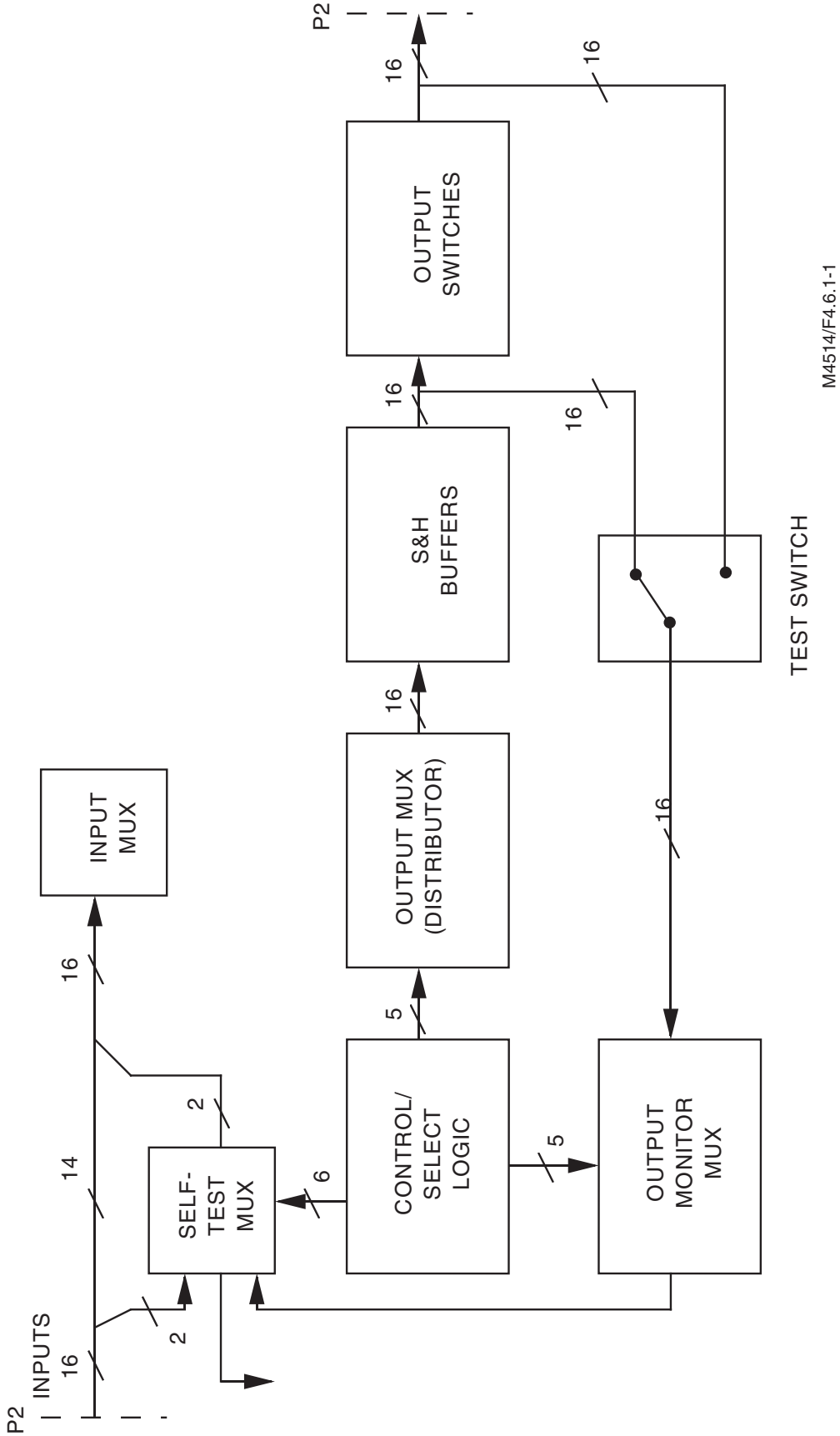


Figure 4.6.1-1. Block Diagram of Loopback Testing

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Table 4.7-1. How to Switch Among A/D Modes

SCANNING MODE CHANGE	EXAMPLE CONTROL WORD SEQUENCE
Old mode: AUTO SCANNING New mode: SCANNING POLL	1. Write $00A0 to the CSR. Set the mode and stop scanning. 2. Write $0080 to the CSR. Keep the mode and start scanning. 3. Write the number of channels to scan to the SSR (if not done previously).
Old mode: AUTO SCANNING New mode: RANDOM POLL	1. Write $0030 to the CSR. Set the mode and stop scanning. 2. Write $0010 to the CSR. Keep the mode and start scanning.
Old mode: SCANNING POLL New mode: AUTO SCANNING	1. Write $0000 to the CSR. Set the mode and begin conversions. 2. Write the number of channels to scan to the SSR (if a new scan size is desired).
Old mode: SCANNING POLL New mode: RANDOM POLL	1. No transition is necessary. Simply begin the RANDOM POLL process.
Old mode: RANDOM POLL New mode: AUTO SCANNING	1. Write $0000 to the CSR. Set the mode and begin conversions. 2. Write the number of channels to scan to the SSR (if a new scan size is desired).
Old mode: RANDOM POLL New mode: SCANNING POLL	1. No transition is necessary. Simply begin the SCANNING POLL process. 2. Write the number of channels to scan to the SSR (if not done previously).

M4514/T4.7-1

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

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SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

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DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items

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to ensure that the board is ready for the intended application.

a. Have the sections pertaining to theory and programming (Sections 3 and 4) been reviewed and applied to the system requirements?

b. Review Section 5.4.1 and Table 5.4-1 to verify that all factory installed jumpers are in place. To change the board address or address modifier response, refer to Section 5.4.2.

c. Have the I/O cables, with the proper mating connectors, been connected to the input/output connector P2? Refer to Section 5.6 for a description of the P2 connector.

d. Calibration has been performed at the factory. If recalibration should be required, refer to Section 5.5.

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*     CAUTION     *
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DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.4 OPERATIONAL CONFIGURATION

The VMIVME-4514 Board's base address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers. The locations and function of all the jumpers on the VMIVME-4514 are shown in Figure 5.4-1 and Table 5.4-1.

5.4.1 Factory-Installed Jumpers

Each VMIVME-4514 is configured at the factory with the specific jumper arrangement shown in Figure 5.4-1. The factory configuration establishes the following functional baseline for the board, and ensures that all essential jumpers are installed.

a. Short I/O base address is set to 0000 HEX.
b. I/O access mode is short nonprivileged.
c. Input and output ranges are set to ±10 V FSR.

5.4.2 Board Address and Address Modifier Selection

Jumper headers J8 and J10 permit the VMIVME-4514 Board to be located

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on any 128-byte boundary within the short I/O address space. The short I/O address space consists of all the addresses between XXXX 0000(HEX) and XXXX FFFF(HEX), where XXXX depends upon the make and model of CPU board used. This requires that 15 address lines be decoded in order to account for all possible base addresses (A01 through A15). Six lines are used for decoding

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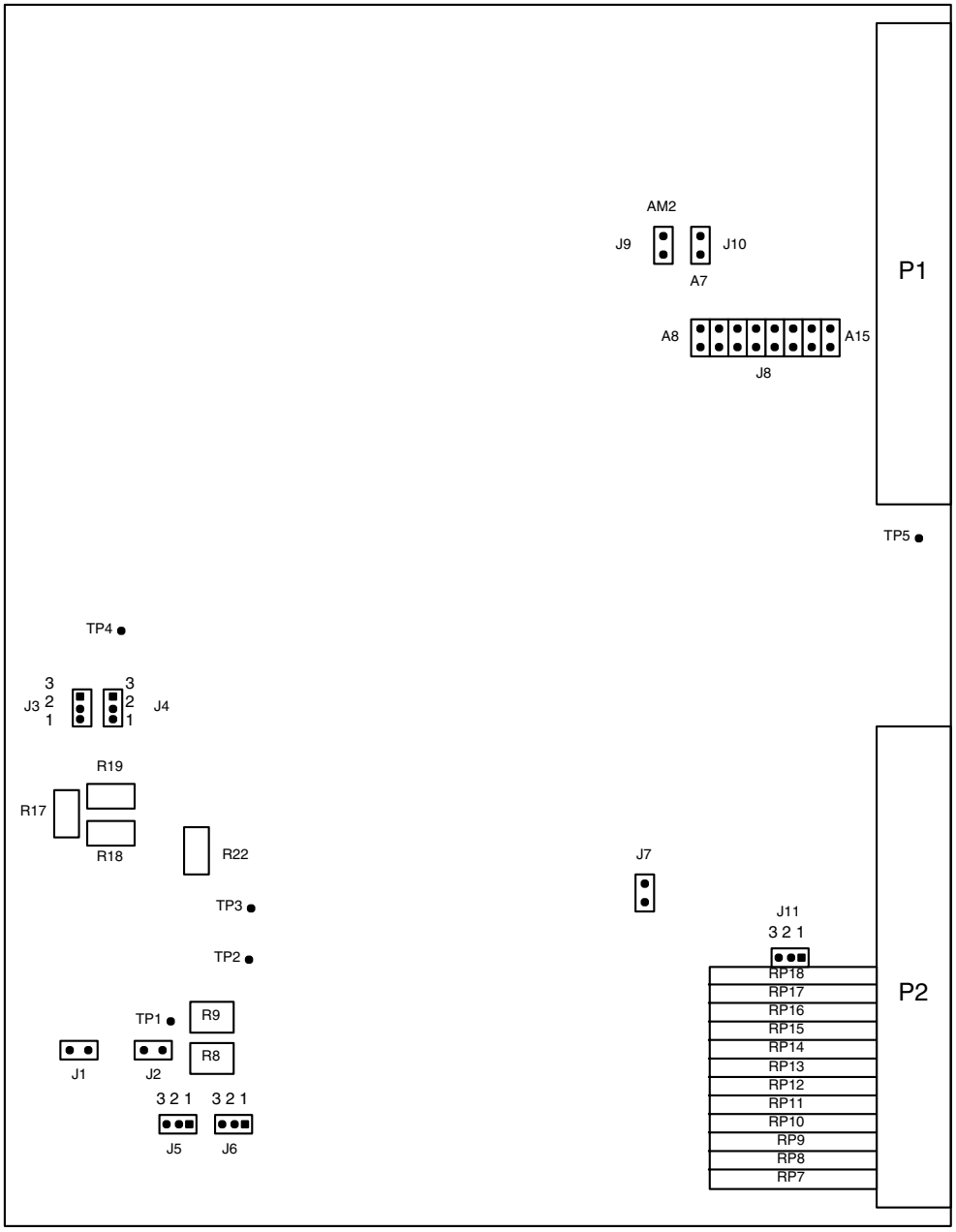


Figure 5.4-1. VMIVME-4514 Adjustment Map

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on-board functions (see Section 4). Therefore, the VMIVME-4514's base address is defined by the remaining nine lines (A07 through A15).

The board's base address is programmed by installing shunts across the jumper posts for each "zero" in the desired address code, and by removing the shunts for each "one" in the code. Address bit A06 has a weight of 64-byte locations. For example, a typical jumper arrangement shown in Figure 5.4.2-1. It would produce a base address of NNNN 8800(HEX), where NNNN depends upon the CPU board used. Also, the I/O access mode must be selected. This is done with jumper J9. Short supervisory access is selected by omitting the jumper. Short nonprivileged access is selected by installing the jumper. Table 5.4-2 and Figure 5.4-2 show the factory configuration of these jumpers.

Table 5.4-1. Jumper Functions

CONTROLS FOR THE VMIVME-4514 INPUTS:

J1	install for 0 to +5 V input range or for ±2.5 V range.
J2	install for 0 to +5 V input range or for ±2.5 V range.
J3	install on pins 1 and 2 for bipolar input (± 2.5, ±5, or ±10 V). Install on pins 2 and 3 for unipolar input (0 to +5 V or 0 to +10V)
J4	install on pins 1 and 2 for all input ranges except ± 10 V. Install on pins 2 and 3 for ±10 V input.
J7	install to use VME bus ground as the reference for single-ended inputs.
J11	install on pins 2 and 3 to use pin C16 of the P2 connector as the ground reference for single-ended inputs. It is normally on pins 1 and 2 to provide a ground return for output Channel 15.
R17	unipolar input offset ("zero") adjustment.
R18	input gain adjustment.
R19	bipolar input offset ("zero") adjustment.
TP1	reads input to A/D converter's track-and-hold amp.
TP4	reads analog ground near A/D Converter.
RP7	input SIP for Channels 12 to 15; always installed.
RP8	input SIP for Channels 12 to 15; install for differential operation.
RP9	input SIP for Channels 12 to 15; install for single-ended operation.
RP10	input SIP for Channels 8 to 11; install for single-ended operation.
RP11	input SIP for Channels 8 to 11; install for differential operation.
RP12	input SIP for Channels 8 to 11; always installed.
RP13	input SIP for Channels 4 to 7; always installed.

M4514/T5.4-1

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Table 5.4-1. Jumper Functions (Concluded)

RP14	input SIP for Channels 4 to 7; install for differential operation.
RP15	input SIP for Channels 4 to 7; install for single-ended operation.
RP16	input SIP for Channels 0 to 3; install for single-ended operation.
RP17	input SIP for Channels 0 to 3; install for differential operation.
RP18	input SIP for Channels 0 to 3; always installed.

CONTROLS FOR THE VMIVME-4514 OUTPUTS:

J5	install on pins 1 and 2 for 0 to +5 V or ±2.5 V output, install on pins 2 and 3 for 0 to +10 V or ±5 V output remove for ±10 V output.
J6	install on pins 1 and 2 for unipolar output (0 to +5 V or 0 to +10 V) install on pins 2 and 3 for bipolar output (± 2.5, ±5, or ±10 V).
R22	unipolar output offset ("zero") adjustment.
R9	output gain adjustment.
R8	bipolar output offset ("zero") adjustment.

CONTROLS FOR THE VMIVME-4514 VMEbus INTERFACE:

TP5	reads output Channel 0.
TP2	reads D/A Converter output.
TP3	reads analog ground near D/A Converter.
J9	controls VME address modifier to which VMIVME-4514 responds. Install for AM code 29 = short nonprivileged. Remove for AM code 2D = short supervisory.
J8	controls VME short I/O address of VMIVME-4514, bits A8 to A15. An installed jumper corresponds to a "zero" address bit.
J10	controls VME address bit A7. An installed jumper corresponds to a "zero" address bit.

M4514/T4.5-1

5.4.3 Analog Input Modes

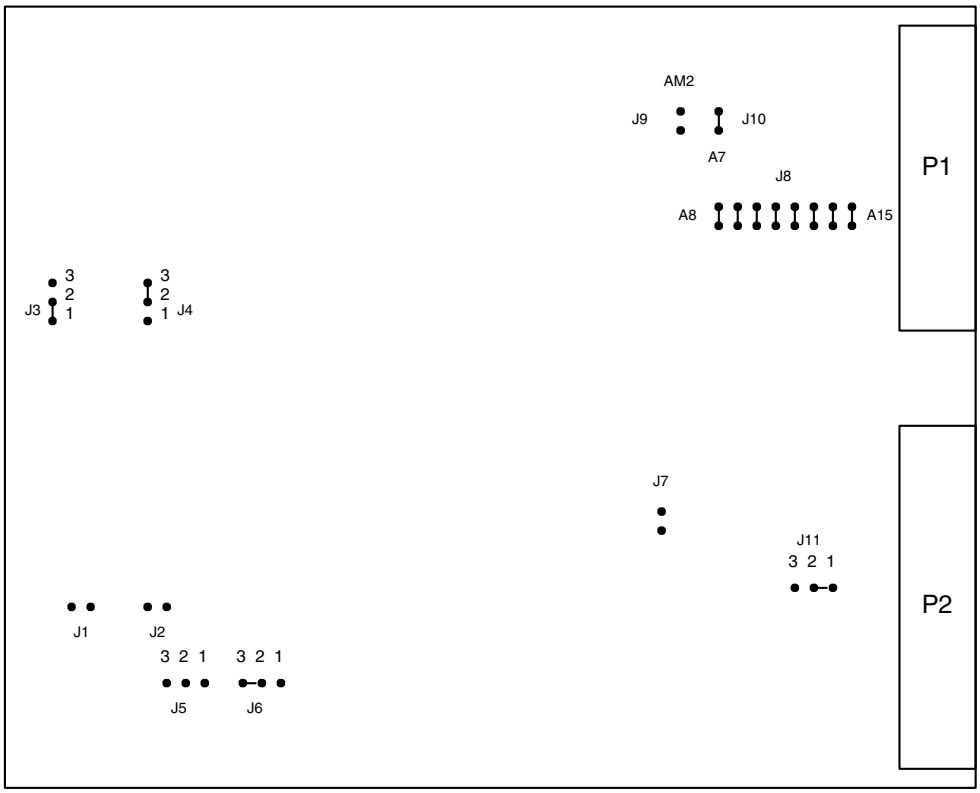
The VMIVME-4514 is factory configured for differential inputs with ±10 V input range. The VMIVME-4514 can be reconfigured in the field for single-ended inputs, and for input ranges of 0 to +5 V, 0 to +10 V, ±5 V, and ±2.5 V.

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Table 5.4-2. Factory Configuration

J1	OPEN
J2	OPEN
J3	Pins 1 and 2 Jumpered
J4	Pins 2 and 3 Jumpered
J5	OPEN
J6	Pins 2 and 3 Jumpered
J7	OPEN
J8	Jumpers on all positions
J9	OPEN
J10	Jumpered
J11	Pins 1 and 2 Jumpered

M4514/T5.4-2



M4514/F5.4-2

Figure 5.4-2. Factory Configuration of the Jumpers

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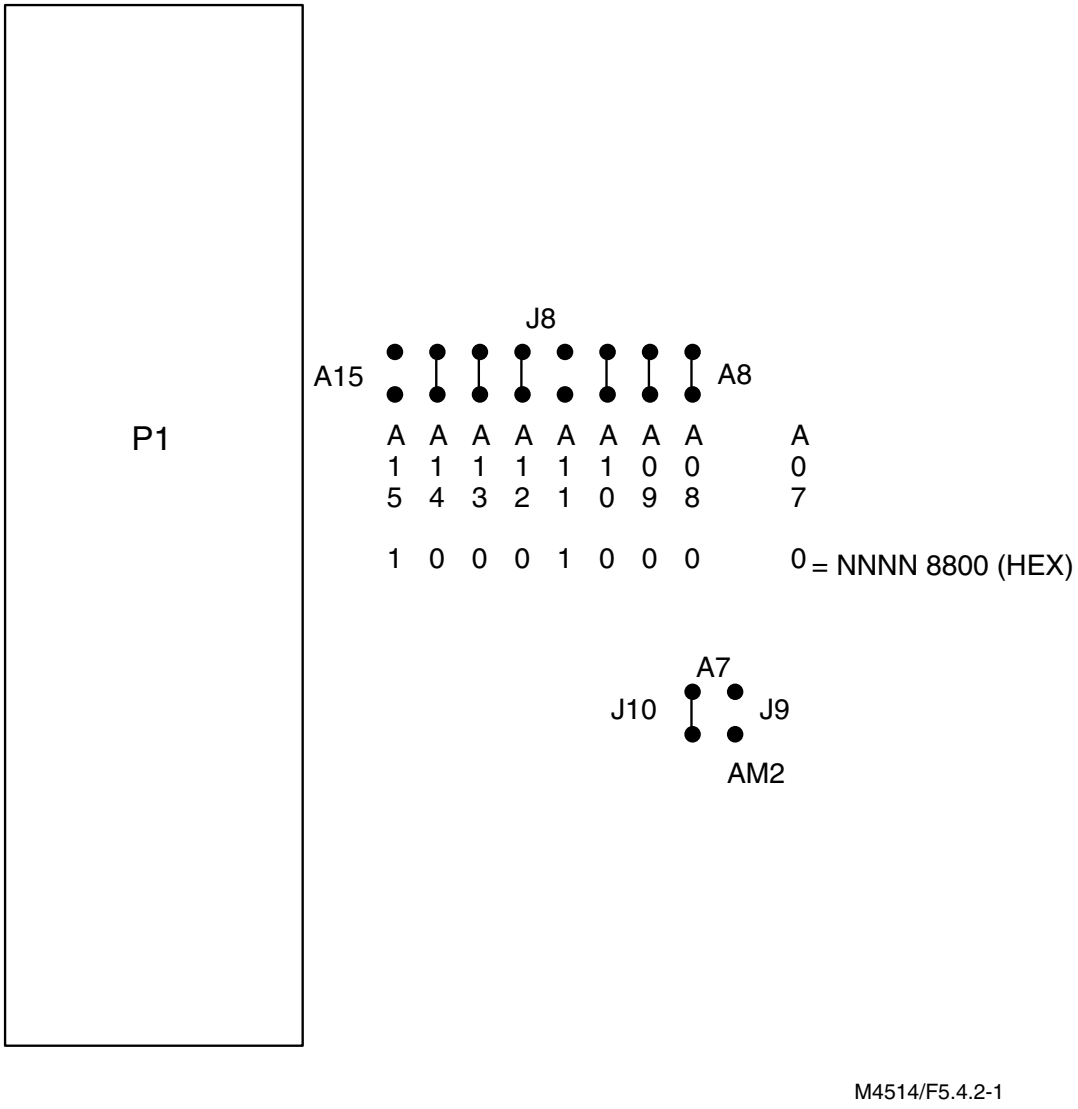


Figure 5.4.2-1. Address Jumpers

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5.4.3.1 Differential or Single-Ended Operation

The sixteen inputs can be configured for differential or single-ended operation in blocks of four. This is done by moving SIP resistor packages among sockets labelled RP7 through RP18. These sockets are near the P2 connector. Channels 0 to 3 are single-ended if RP16 is installed. They are differential if RP17 is installed. For Channels 4 to 7, RP15 allows single-ended operation and RP14 allows differential operation. On Channels 8 to 11, install RP10 for single-ended use or RP11 for differential use. On Channels 12 to 15, install RP9 for single-ended use or RP8 for differential use.

Any single-ended inputs will be referenced to the VMIVME-4514's analog ground (and to VMEbus ground) if J7 is installed. To reference these inputs to some other ground, remove J7 and put J11 in the [2-3] position. Pin C16 of the P2 connector is now the external ground sense. When J11 is in the [1-2] position, it provides the ground return for the last output channel.

5.4.3.2 Input Voltage Range

Jumpers J1, J2, J3, and J4 control the input voltage range. Table 5.4-1 shows the possible combinations. Note that self-testing depends on both the input voltage range and the output voltage range. If the ranges do not match, then the input code must be scaled and shifted in software to match the output code.

For 0 to +5 V, install J1 and J2; put J3 on position [2-3]; put J4 on [1-2]. For 0 to +10 V, omit J1 and J2; put J3 on [2-3]; put J4 on [1-2]. For ±2.5 V, install J1 and J2; put J3 on [1-2]; put J4 on [1-2]. For ±5 V, omit J1 and J2; put J3 on [1-2]; put J4 on [1-2]. For ±10 V, omit J1and J2; put J3 on [1-2]; put J4 on [2-3]. For both J3 and J4, pin 1 is nearest to the bottom of the board. It is marked by a square pad on the solder side.

5.4.4 Output Voltage Ranges

Jumpers J5 and J6 control the output voltage range. There are five possible ranges: 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V. For 0 to +5 V, put J5 on position [1-2]; put J6 on [1-2]. For 0 to +10 V, put J5 on [2-3]; put J6 on [1-2]. For ±2.5 V, put J5 on [1-2]; put J6 on [2-3]. For ±5 V, put J5 on [2-3]; put J6 on [2-3]. For ±10 V, remove J5; put J6 on [2-3].

5.5 CALIBRATION

Before shipment from the factory, the VMIVME-4514 is fully calibrated and

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conforms to all of the specifications listed in Section 2. Ultra-precise resistors have been used to make the calibration good for all voltage ranges, but the calibration for ±10 V is dominant. However, should recalibration be required, the recalibration procedures are not difficult. Perform the procedures in Sections 5.5.2 and 5.5.3 with the equipment listed in Section 5.5.1. The locations of all adjustments and test points are shown in Figure 5.4-1.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration. All adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

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DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.5.1 Equipment Required

a. Digital Voltmeter (DVM). With 1.0000 and 10.000 VDC ranges, 5 or more digits, 0.005 percent of the expected voltage measurement accuracy, with a minimum of 10 M• input impedance. This is used for calibrating the outputs.

b. Digital Voltage Source. With a 10.000 VDC range, resolution of 0.0005 VDC, accuracy of 0.005 percent of the expected value, and 0.10 • maximum output impedance. This is used for calibrating the inputs.

c. Chassis. VMEbus backplane or equivalent, with J1 and J2 connectors, a VMEbus master controller, a +5 VDC 0.1 VDC power supply, and one slot allocated for testing the VMIVME-4514 Board.

d. Extender board. One VMEbus extender board.

e. Test cables. Enough test cables for the equipment listed above.

f. CPU. A VMEbus computer that will be used to control the VMIVME-4514.

5.5.2 Analog Inputs Calibration Procedure

a. Install the VMIVME-4514 Board on an extender board in an open slot

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of the VMEbus backplane.

b. Configure the analog inputs for the desired input range (see Section 5.4.3).
c. Apply power to the backplane. Allow a minimum warmup time of ten minutes before proceeding.
d. Connect the digital voltage source between connector pins P2-A17 (+) and P2-C17 (-).
e. Write the 16-bit value 1000(HEX) to the Control and Status Register (CSR) at the board's base address +2.
f. If you are using a bipolar input range, set the voltage source for 0.0000 VDC. If you are using 0 to 5 V, set it for 2.5000 VDC. If you are using 0 to 10 V, set it for 5.0000 VDC.
g. If you are using a bipolar input range, adjust R19 (BIPOLAR INPUT OFFSET) for the next step. If you are using a unipolar input range, adjust R17 (UNIPOLAR INPUT OFFSET) for the next step.
h. Repeatedly read the 16-bit register at the board's base address +40 (HEX) and adjust R17 or R19 until the reading is 0800 (HEX).
i. Set the voltage source to produce a voltage of "full-scale" minus 1.5 bits. For 0 to 5 V, this is 4.9982 V. For 0 to 10 V, it is 9.9963 V. For ±2.5 V, this is 2.4982 V. For ±5 V, this is 4.9963 V. For ±10 V, it is 9.9927 V.
j. Repeatedly read the 16-bit register at the board's base address + 40 (HEX) and adjust R18 until the reading is alternating between 0FFE (HEX) and 0FFF (HEX).
k. Repeat steps f through j until no adjustment is necessary.
l. Calibration of the analog inputs is completed. Remove all test connections, and restore the board to its original configuration.
m. All unused inputs should be grounded.

5.5.3 Analog Outputs Calibration Procedure

a. Install the VMIVME-4514 Board on an extender board in an open slot of the VMEbus backplane.
b. Configure the analog inputs for the desired input range (see Section-5.4.3).
c. Apply power to the backplane. Allow a minimum warmup time of ten minutes before proceeding.
d. Connect the digital voltmeter across pins A1 (+) and C1 (-) of the P2 connector (or TP5(+) and TP3(-)).
e. Write the 16-bit word 1800 (HEX) to the CSR at offset address + 2.
f. Write the 16-bit value 0000 (HEX) to the analog output Channel 00 register at the offset address of 0020 (HEX).
g. If you are using a bipolar output range, adjust R8 to produce a minus full-scale reading on the DVM (read -2.5, -5, or -10 V). If you are

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using a unipolar output range, adjust R22 to produce a 0 VDC reading.

h. Write the 16-bit value 0FFF (HEX) to the output Channel 00 register at the board's offset address 0020 (HEX)
i. Adjust R9 to produce a reading of plus full-scale. For unipolar output, the reading should be 4.9988 or 9.9976 V. For bipolar output, the reading should be 2.4988, 4.9976, or 9.9951 V.
j. Repeat steps f through i until no adjustment is necessary.
k. This completes the calibration of the analog outputs. Remove power and all test connections. Restore the board to its original configuration.

5.6 CONNECTOR DESCRIPTION

Two 96-pin DIN connectors, P1 and P2 (Figure 2.1-1), provide all connections to the VMIVME-4514 Board. P1 contains the address, data and control lines, and all additional signals necessary to control the VMEbus functions of the board. P2 provides the connections for the 16 analog input and output channels.

Orientation of the P2 connector is shown in Figure 5.6-1, and the P2 signal assignments are listed in Table 5.6-1. The mating connector for P2 (Panduit Model 120-964-435E or equivalent) is designed to be used with a standard 64-wire ribbon-cable with conductor spacing of 0.050 inches. In environments where there is a high degree of electrical noise, a twisted-pair ribbon cable with an overall shield is recommended.

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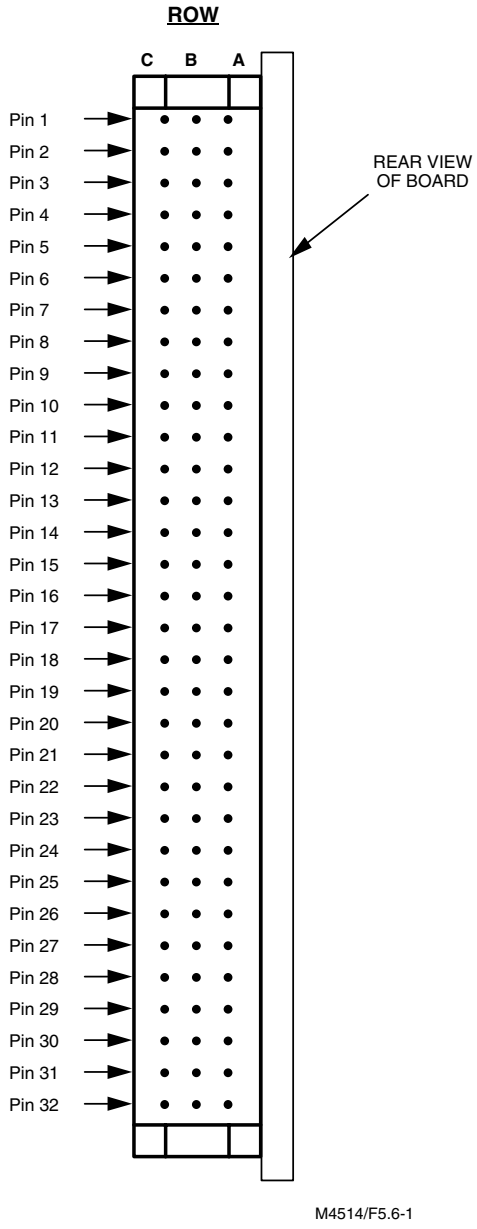


Figure 5.6-1. P2 Connector Pin Layout

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Table 5.6-1. P2 Connector - Pin Assignments

PIN NO.	ROW A	ROW B	ROW C
1	OUTPUT CH00	+5 V	AGND
2	OUTPUT CH01	GND	AGND
3	OUTPUT CH02		AGND
4	OUTPUT CH03		AGND
5	OUTPUT CH04		AGND
6	OUTPUT CH05		AGND
7	OUTPUT CH06		AGND
8	OUTPUT CH07		AGND
9	OUTPUT CH08		AGND
10	OUTPUT CH09		AGND
11	OUTPUT CH10		AGND
12	OUTPUT CH11	GND	AGND
13	OUTPUT CH12	+5 V	AGND
14	OUTPUT CH13		AGND
15	OUTPUT CH14		AGND
16	OUTPUT CH15		AGND
17	INPUT CH00 HIGH		INPUT CH00 LOW
18	INPUT CH01 HIGH		INPUT CH01 LOW
19	INPUT CH02 HIGH		INPUT CH02 LOW
20	INPUT CH03 HIGH		INPUT CH03 LOW
21	INPUT CH04 HIGH	GND	INPUT CH04 LOW
22	INPUT CH05 HIGH		INPUT CH05 LOW
23	INPUT CH06 HIGH		INPUT CH06 LOW
24	INPUT CH07 HIGH		INPUT CH07 LOW
25	INPUT CH08 HIGH		INPUT CH08 LOW
26	INPUT CH09 HIGH		INPUT CH09 LOW
27	INPUT CH10 HIGH		INPUT CH10 LOW
28	INPUT CH11 HIGH		INPUT CH11 LOW
29	INPUT CH12 HIGH		INPUT CH12 LOW
30	INPUT CH13 HIGH	GND	INPUT CH13 LOW
31	INPUT CH14 HIGH	+5 V	INPUT CH14 LOW
32	INPUT CH15 HIGH		INPUT CH15 LOW

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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