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# VMIVME-4514A
# 16-Channel Scanning Analog I/O Board with Built-in-Test and P2 I/O

## Product Manual

A GE Fanuc Company

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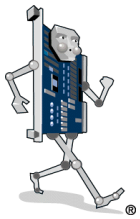
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(I/O man figure)



(IOWorks man figure)













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# Overview

## Contents

## Introduction

The VMIVME-4514A is a 16-Channel, 12-bit Analog Input / Output (AIO) Board. It provides both the stimulus and the response functions encountered in VMEbus based closed-loop analog systems. The analog signals are available at the P2 backplane connector. It is self-contained, with a resident 12-bit Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC). The board also supports a Built-in-Test feature that checks all of the active components on the board. The VMIVME-4514A provides a single board solution to the analog input / output requirements of such VMEbus applications as process control, simulators, trainers, and supervisory control.

The VMIVME-4514A provides the user with 16 analog outputs with 12 bits of resolution. The outputs are designed with individual Sample-and-Hold (S&H) amplifiers, one per channel. The outputs can be programmed (via on-board jumpers) to operate in a variety of voltage ranges. These ranges are 0 to +5 V, 0 to +10 V (unipolar), ±2.5, ±5.0, or ±10 V (bipolar). Each output can source or sink up to 10 mA at ±10 V. The outputs can be disconnected from the I / O connector for off-line testing.

The board also accepts 16 analog inputs. These inputs may be differential or pseudo-differential (single-ended). A 36 Hz single pole input filter may be ordered for the inputs. The input ADC can be programmed (via on-board jumpers) to operate in a variety of voltage ranges. These ranges are 0 to +5 V, 0 to +10 V (unipolar), ±2.5, ±5.0, or ±10 V (bipolar). The inputs have 12 bits of resolution. The inputs can be scanned by on-board multiplexers, and the data stored in a dual port memory.

The VMIVME-4514A has three ADC operating modes. They are Random Polling, Scanning Poll, and Auto Scanning. Auto Scanning Mode is entered when power is applied to the board, after a system reset, or under program control. In this mode, all 16 channels are continuously scanned. Their inputs are digitized and stored in sixteen 12-bit dual port registers. No programming is required other than reading the data from these registers. The Random Polling and Scanning Poll modes will be described later in this manual.



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A brief overview of the principal features of the VMIVME-4514A illustrates the flexibility and the performance that is available with this board:

- 16 differential or single-ended analog input channels
- 16 analog output channels with 10 mA drive capability
- On-board 12-bit ADC and DAC
- Three A / D operating modes:

— Auto Scanning Mode

— Scanning Poll Mode

— Random Polling Mode

- Powers up in Auto Scanning Mode requires no software initialization
- Input and output voltage ranges are jumper-selectable as 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, ±10 V
- Optional low pass filter is available for analog input noise elimination and anti-aliasing
- Program-controlled off-line operation of analog outputs
- A / D data coding is program-selectable as either binary, offset binary, or two's complement format
- Total acquisition and conversion time is 25 µsec resulting in 40 kHz maximum throughput
- All inputs and outputs are protected against line transients and short circuits
- Front panel Fail LED indicator
- Double Eurocard form factor
- P2 I / O connections



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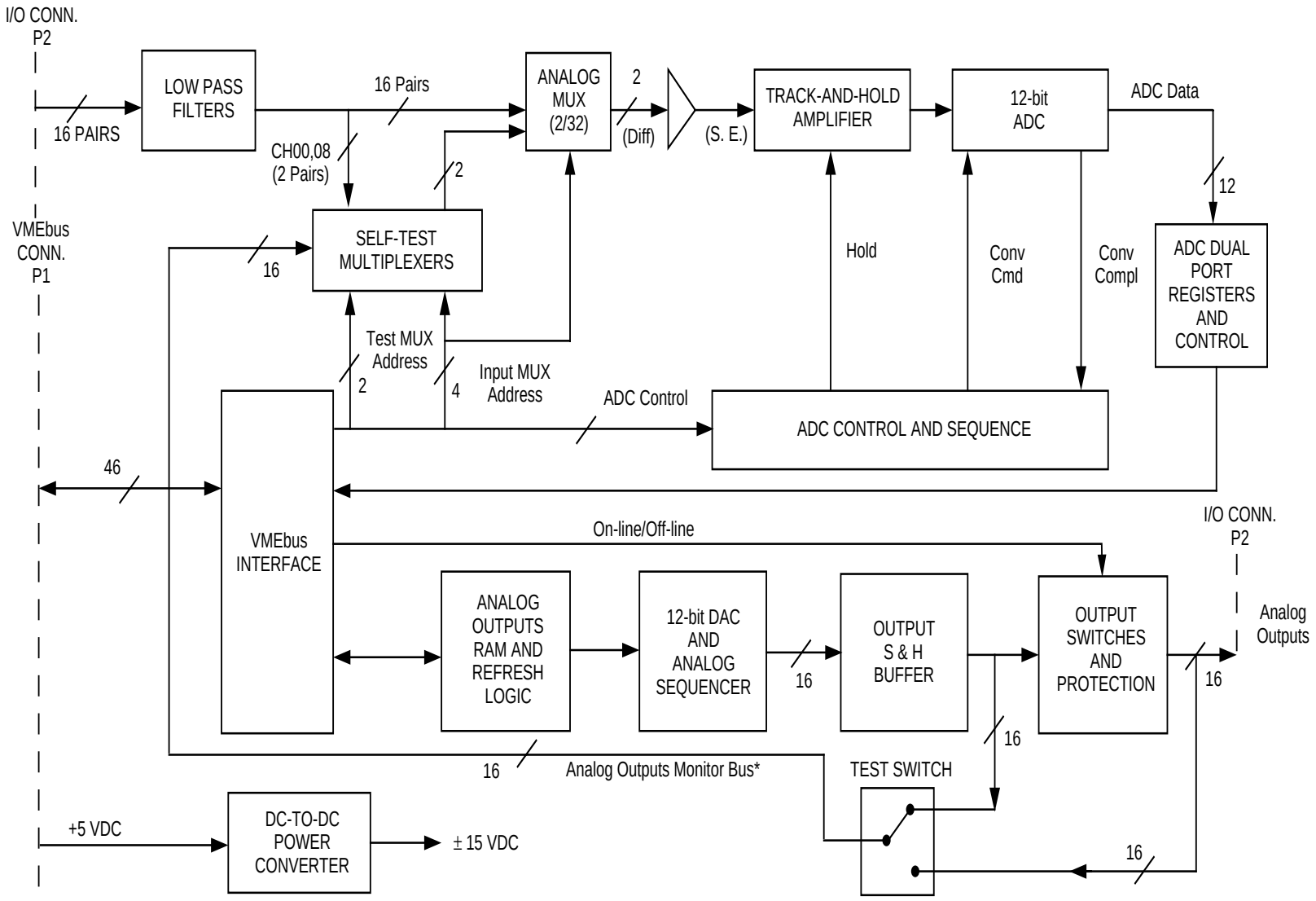
## Functional Description

The VMIVME-4514A is a self-contained, 16-channel, 12-bit Analog I/O Board. Figure 1 on page 17 is a block diagram of the board. The analog inputs are user-selectable either as single-ended (pseudo-differential) or as differential-pair channels. Each of the 16 analog outputs will supply up to 10 mA of drive current. The outputs can be operated off-line for both loopback self-testing and for single-point analog input/output applications. Built-in-test checks all of the active components on the board. It is done by looping back either the on-line or off-line analog outputs to the analog input's DAC via the input multiplexers.

An on-board ADC controller with a channel sequencer provides the highest throughput with minimal CPU intervention. This sequencer is used in the scanning modes. In these modes each channel is converted and stored in a dual port register which is accessible from the VMEbus. The block diagram of the VMIVME-4514A shown in Figure 1 on page 17 illustrates the board's components and their basic functions.



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*Monitors board outputs in "on-line" mode; buffer outputs in "off-line" mode.

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**Figure 1** VMIVME-4514A Functional Block Diagram



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## Reference Material List

For a detailed explanation of the VMEbus and its characteristics, refer to "The VMEbus Specification" available from:

VITA
VMEbus International Trade Association
7825 East Gelding Drive No.104
Scottsdale, AZ 85260
(602) 951-8866
FAX: (602) 951-0720
Internet: http://www.vita.com/
EMAIL: info@vita.com

For detailed information concerning the physical description and specifications of the VMIVME-4514A 16-Channel Scanning Analog I/O Board with Built-in-Test and P2 I/O, refer to *VMIC's Specification No. 800-104514-000*. This document is availble from:

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Huntsville, AL 35803-3308
(205) 880-0444
(800) 322-3616
Fax: (205) 882-0859

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

Table 2-1

| Title | Document No. |
|---|---|
| Digital Input Board Application Guide | 825-000000-000 |
| Change-of-State Application Guide | 825-000000-002 |
| Digital I/O (with Built-in-Test) Product Line Description | 825-000000-003 |
| Synchro/Resolver (Built-In-Test) Subsystem Configuration Guide | 825-000000-004 |
| Analog I/O Product (with Built-In-Test) Configuration Guide | 825-000000-005 |
| Connector and I/O Cable Application Guide | 825-000000-006 |



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# Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

## Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

## Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

## Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

## Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

## Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

## Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**WARNING:** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.



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## Warnings, Cautions and Notes

**STOP** informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

**WARNING** denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION** denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE** denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.



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CHAPTER

1

# *Theory of Operation*

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## Introduction

The VMIVME-4514A is a 16-channel, 12-bit Analog Input/Output (AIO) Board which is designed to operate in a standard VMEbus system. The board is self-contained with a resident 12-bit Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC), as well as, loopback circuitry to support the self-test feature. There is an on-board sequencer that allows the board to continuously scan the inputs. The scanning mode converts the input signal and stores it in on-board dual port memory. This simplifies the programming of the board. The user only has to read the register associated with the input in question to get the latest data.

The VMIVME-4514A does not require additional boards to provide high quality analog input and output functions. The VMIVME-4514A is a flexible element in an analog I/O system. It offers Built-In-Test and off-line operating features not found in many other products.



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## Intelligent I/O Controller

The VMIVME-4514A can be used in a VMIC Intelligent I/O Controller (IIOC). The IIOC consists of up to three 680XX Central Processing Units (CPUs) and their coprocessors, global memory, a host computer interface, VMIC firmware, and a variety of VMIC board level products. The IIOC is designed to give the user a total turnkey solution to a VMEbus system design.



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# Functional Organization

The VMIVME-4514A is divided into the following functional categories, as illustrated in Figure 1-1 on page 24. All of these functions are discussed in detail in this section.

- VMEbus interface
- ADC control
- A / D conversion and timing
- Analog input filters and multiplexer
- DAC and analog distributor
- Analog output buffers and switches
- Analog output refresh logic
- Self-test multiplexers
- Power converter



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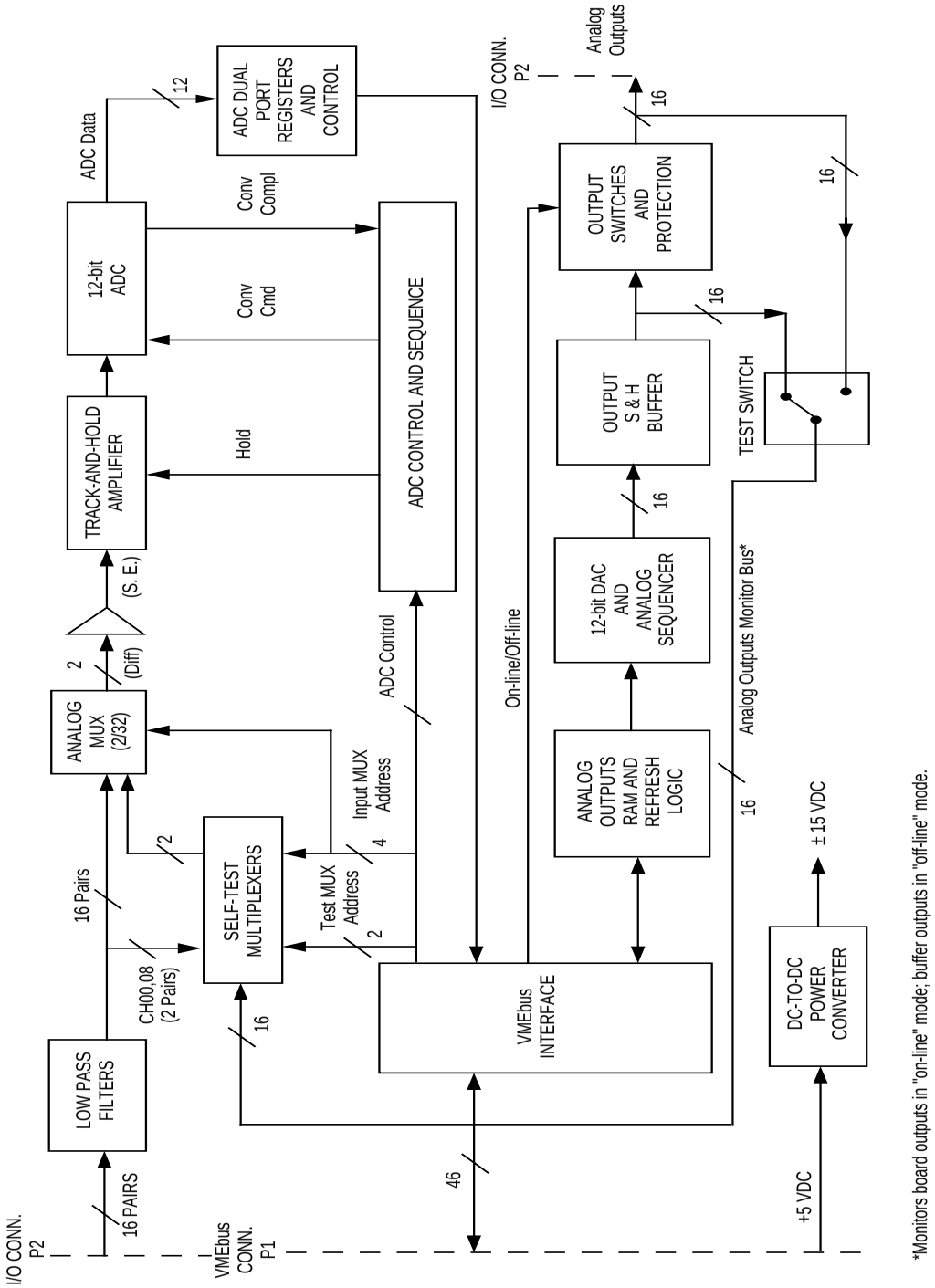



**Figure 1-1** VMIVME-4514A Functional Block Diagram

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# VMEbus Interface

The VMIVME-4514A communications registers are memory mapped as 64 (decimal) 16-bit words. The registers are contiguous, and may be user-located on any 128-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged.

During each read or write operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers (shown in Figure 2-2 on page 44) and the address and address modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK* interface signal is asserted (driven LOW). Subsequent removal of the Central Processing Unit (CPU) read or write command causes the board-generated DTACK* signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communications with the board, as follows:

- Data Bus lines D00 to D15.
- Address lines A01, A02, A03, A04, A05, A06.
- Bus Control Signals:
  - — WRITE*
  - — DS0,* DS1*
  - — SYS CLK
  - — SYSRESET*

The Data Bus lines are bidirectional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all of the data devices on the board.

Address lines A01 through A06 map the 64 communication registers into a 128-byte range within the VMEbus address space (Chapter 3). The control signals determine whether data is to be moved to the board (write) or from the board (read), provide the necessary data strobes (DS0*, DS1*), and supply a 16 MHz clock (SYSCLK) for use by on-board timers. A SYSRESET* input resets all timers and flags.

Static controls are latched into the Control Register and are used primarily to establish the operating mode of the board. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC, are read through the Status Register. The control and status registers are referred to collectively as the Control and Status Register (CSR), since they are at the same address. The WRITE* signal determines which one is accessed. Most of the Control Register outputs can be monitored directly through the Status Register.

Each of the 16 analog output channels is controlled by writing 12-bit right-justified data into a dedicated 16-bit read/write register. The 16 analog output control registers constitute the VMEbus port of a 16-word dual port memory. The other memory port is controlled by the analog output refresh logic.



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# ADC Control

Control commands and status flag's bit locations associated with controlling the ADC are described in more detail in Chapter 3 of this manual. There are two mode control bits in the CSR used by the ADC. They are called A/D Mode 1H and A/D Mode 0H. The state of these bits determines which one of the three possible operating modes the ADC will use. The following truth table shows these functions:

**Table 1-1** ADC Mode Control Bits

| A/D Mode (1H) | A/D Mode (0H) | ADC Operating Mode |
|---|---|---|
| 0 | 0 | Auto Scanning |
| 0 | 1 | Random Polling |
| 1 | 0 | Scanning Poll |
| 1 | 1 | Not Used |

The ADC operating mode basically determines if the ADC and the channel selection logic are controlled externally by a CPU or internally by the on-board channel sequencer. The programming associated with these operating modes will be described in *"Programming"* Chapter 3 of this manual. The following discussions are here to reveal the ADC controls and timing intervals.

## Auto Scanning Mode

The Auto Scanning Mode is the default mode of operation. It is entered after power is applied to the board, a hardware system reset, or when a program clears the A/D mode control bits (A/D Mode 1H and A/D Mode 0H) to "zeros" in the CSR. This mode performs a sequential scan of all the inputs, digitizing their values and storing this data in a dual port register. Any unused input should be grounded. Once all of the inputs have been digitized, the process starts all over at the first channel. The VMEbus has access to this data at any time.

Whenever a channel is read, the latest data is used. This mode frees the programmer from much of the overhead required to process analog conversions. This can allow the board to digitize the inputs at a faster rate; increasing throughput. If the Scan Size Register (SSR, located at offset 06) is loaded, then only the indicated number of channels will be scanned. If input filters are going to be used, then all 16 channels must be scanned. This prevents the filter caps from injecting a "pumpback" current error to the ADC. Any unused input should be grounded.



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## Random Polling Mode

To enter this mode, the CSR A/D Mode 1H and A/D Mode 0H bits must be set to "zero" and "one," respectively. In this mode, the CPU controls and monitors every aspect of a conversion. It must select the channel to convert and start the conversion. The CPU must wait for the conversion to finish, then check (or poll) a status bit in the CSR (end-of-conversion). When it is asserted, this tells the program that the conversion is complete. The host can now read the data. This mode is called "random" because the CPU can select the channel to use in any order (i.e., CH2, CH0, CH8, CH14, CH2, etc.). This is the only mode which can be used to self-test the outputs.

## Scanning Poll Mode

The Scanning Poll Mode is very similar to the Auto Scanning Mode. This mode does everything the Auto Scanning Mode does except it does only one (1) scan of the inputs. An "end-of-scan" status bit must be polled to determine when the scan is complete. To start this mode, the A/D Mode 1H and A/D Mode 0H control bits in the CSR must be set to "one" and "zero," respectively. The SSR must be loaded prior to starting the first scan.

## Scan Size Register

The Scanning Poll Mode and the Auto Scanning Mode do not necessarily convert all 16 inputs. If fewer than 16 inputs are used, higher throughput is possible by scanning only the lowest numbered input channels. For example, if the SSR is loaded with 8, only the Channels 0 through 7 will be scanned. The SSR is at offset address 06 from the VMIVME-4514A's base address. Its use is optional in the Auto Scanning Mode (16 channels will be assumed). It must be loaded prior to using Scanning Poll Mode.



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# A/D Conversion and Timing

Regardless of which ADC operating mode described in *ADC Control* on page 26 is used, the A / D conversion sequence is the same. All of the ADC timing intervals discussed in this section are performed automatically by the on-board controller. Program control consists basically of some handshake sequences (start something, wait for it to finish, and then poll a status bit to confirm it).

## Converter Controls and Status Flags

Once the conversion sequence has begun (initiated by one of the above A / D operating modes), it consists of the following *consecutive* time intervals:

- Settling delay
- Tracking interval
- A / D conversion

The settling delay occurs directly after a state change has occurred in the analog networks (such as selecting a new input channel). It represents the settling time of the networks. After the settling delay has been completed, the Track-and-Hold (T&H) amplifier (Figure 1-1 on page 24) enters the tracking mode, and the tracking interval begins. During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage. The Settling Busy flag is a handshake signal that tells the CPU when the input has settled to its input value. It is set HIGH at the beginning of the settling delay, and is cleared LOW at the end of the tracking interval. Any Start Settling commands issued when this flag is set will be ignored.

At the end of the tracking interval, the T&H amplifier enters the Hold Mode. The amplifier's output is held at a constant level. Now if the board is controlling the conversions, a CONV CMD from the timing decoder is issued. If the CPU is controlling the conversions, it must set the EN Start CONV control bit in the CSR. Either way this causes the A / D conversion to begin. The A / D conversion digitizes the output of the T&H amplifier into a 12-bit data word. It then terminates the conversion sequence. The CONV COMPL L flag from the ADC is HIGH during the conversion, and is Low otherwise. The EN Start CONV control bit sets the CONV Busy flag HIGH. It remains HIGH until the conversion sequence has been completed.

In the Random Polling Mode, completion of the A / D conversion causes the New Data RDY flag to be set HIGH, indicating that valid data is present in the Converter Data Register (CDR). This register is only used by the Random Polling Mode. The action of reading the CDR clears the New Data RDY and CONV Busy flags to the LOW ("zero") state.

In the Scanning Poll Mode, when the A / D conversion is completed on the last channel to be scanned, the REGD End Of Scan flag is set in the CSR. This flag can be polled to determine when all of the channels have been converted and their data is available to be read. The on-board ADC controller uses a microsecond timer. The microsecond timer uses the 16 MHz system clock to generate the Tracking and CONV CMD control signals for the converter. It also provides the settling time delay. The CSR contains a Short Settling control bit. Setting this bit High provides increased throughput by reducing the time allocated to both the settling delay and the tracking interval.



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# Analog Input

Sixteen differential or single-ended analog input channels are available at the rear panel through the P2 connector. By connecting the analog return in the remote device to the Input Ground Sense input on the P2 connector as shown in Figure 1-2 on page 30, the single-ended lines can be operated as pseudo-differential inputs. However, it is recommended that the differential mode be used for increased noise and common mode rejection. All VMIVME-4514A input channels are overvoltage protected by current-limiting input resistors. See document number 800-104514-000 for the input overvoltage specifications. All unused inputs should be grounded.

## Low Pass Filters and Input Multiplexer

The 16 analog input channels can be provided with individual, single pole, low pass filters as shown in Figure 1-2 on page 30, and can be user-configured to operate either as single-ended or differential. See document number 800-104514-000 for the input filter specifications.

To achieve maximum system accuracy with filtered analog inputs, the sample rate should be limited to 2,500 Hz or less per channel. Higher sample rates will produce reflected or "pumpback" currents at the inputs which can induce error voltages across the filter input resistors. Thus, when the filters are installed, all 16 channels must be used in the Auto Scanning Mode.

Each of the 16 analog inputs is selectable through one of two input multiplexer sections. Each input multiplexer accepts eight differential input pairs. A second tier of multiplexers receives the selected channel from one of the input multiplexers. Both multiplexer sections are controlled by the same set of four address lines (INP MUX Address) which are derived from control bits "MUX A00" through "MUX A03" in the Control Register.

## Single-Ended Operation

Differential or single-ended operation of the analog inputs is selected by the location of Single-In-line-Package (SIP) resistors as illustrated in Figure 1-2 on page 30. The input multiplexers are always operated in the differential mode. Single-ended (pseudo-differential) operation is obtained by positioning the "Low" input resistor so that it connects to the common Input Ground Sense input instead of to the individual "Low" signal inputs.



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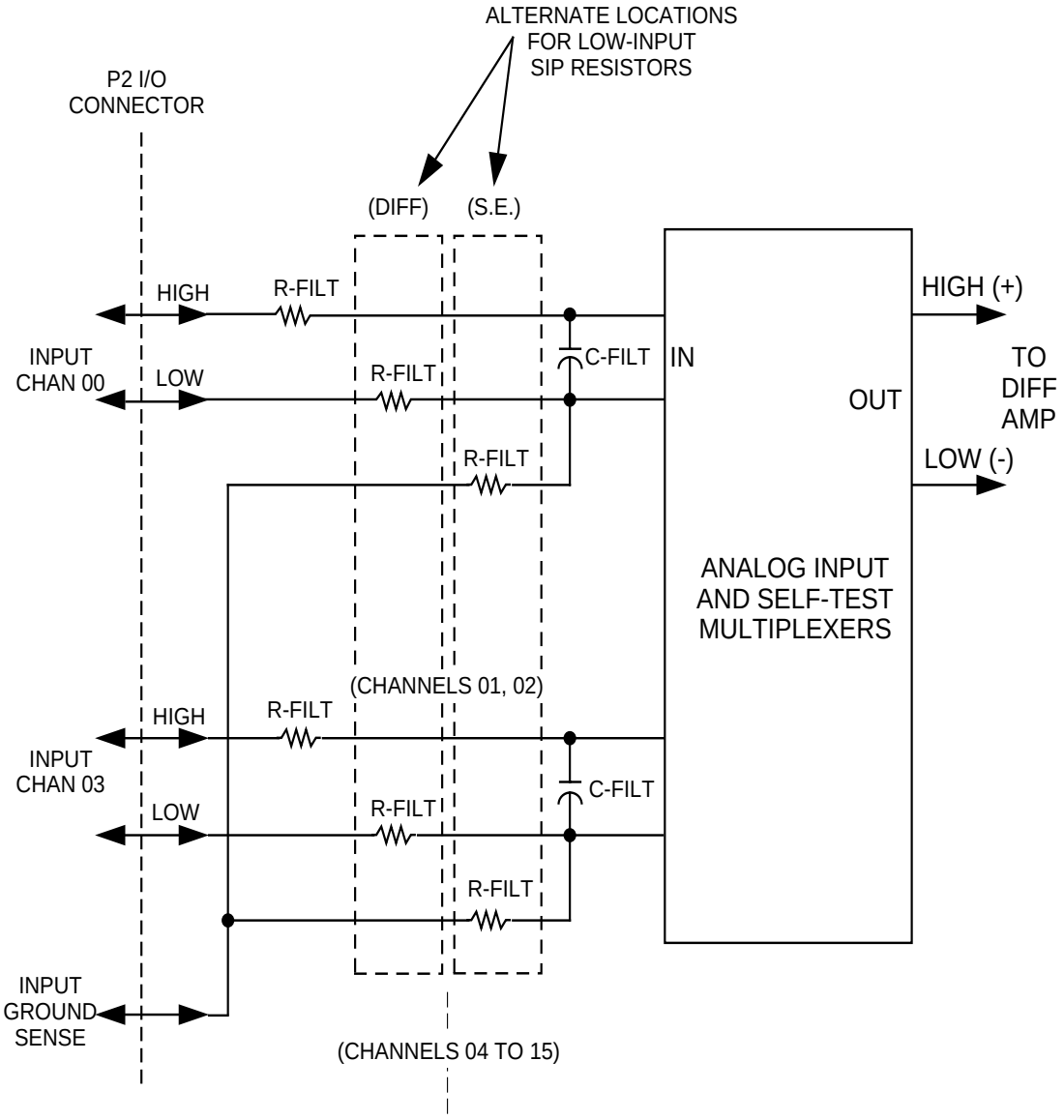



**Figure 1-2** Single-Ended and Differential Input Configurations



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# Analog Outputs

In addition to the analog inputs, there are 16 analog outputs available at the P2 connector. The analog outputs are updated (refreshed) periodically from the dual port memory by a refresh control logic, as illustrated in Figure 1-3 below. Each output receives an update once every 1.7 msec in the default refresh mode. A program controlled Fast Refresh flag can be used to reduce the refresh cycle time to approximately 0.4 msec, and thereby raising the maximum output sampling rate from 550 Hz to 1.6 kHz.

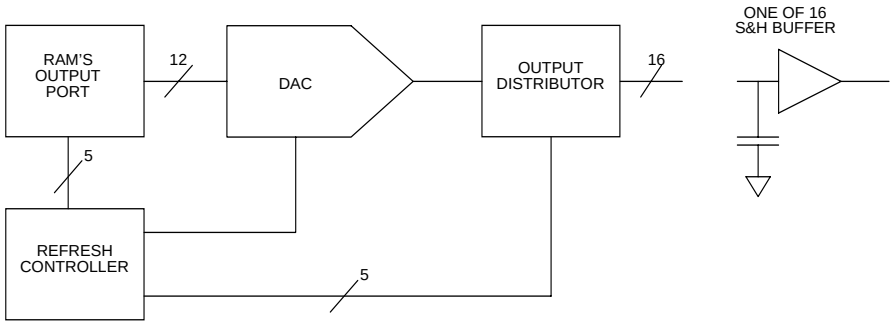



**Figure 1-3** Analog Outputs Block Diagram

## Digital-to-Analog Converter (DAC)

All 16 analog outputs are serviced by a single 12-bit DAC. The DAC is controlled by the refresh control logic. This logic periodically transfers data from the dual port memory's refresh port to the DAC. This logic simultaneously connects the DAC to the appropriate section of the analog distributor. The analog output data is placed in the dual port memory through the VMEbus port by the controlling processor.

## Analog Distributor

The analog distributor consists of the following elements:

- One of 16 decoders
- Low charge injection analog demultiplexer
- Sixteen capacitive storage elements

As the DAC is updated with data for each channel in the output refresh sequence, the decoder receives the same four address lines used by the dual port memory. In this manner, the converted analog level is always routed to the distributor section which corresponds to the dual port memory location for the same channel. After allowing the DAC to settle, the refresh logic enables (turns ON) the demultiplexer. Then the converted voltage level is transferred to the corresponding storage capacitor. After a settling interval of approximately 100 µsec is provided by the Refresh logic, the demultiplexer is disabled and the next channel in the Refresh sequence is processed.



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## Output Buffers and Switches

Voltage levels stored by the analog distributor are buffered and then switched to the P2 connector for routing through system I/O cables. The output buffers are low leakage, precision operational amplifiers which can supply 10 mA of drive current over the full available output voltage range (up to ±10 V). These buffers can withstand sustained short circuits-to-ground without damage.

Output switches permit the analog outputs to be disconnected from the P2 connector for "off-line" self-testing and for low impedance, single-point analog input/output system applications. To eliminate the effect of switch resistance on the output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operation. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ±15 V supply rails.

## Data RAM and Refresh Control

The dual port memory which services the analog outputs is organized as a 16-bit wide, 16-location array, in which each location can be accessed from either of the two ports. The VMEbus port is used by the VMEbus host to load the analog output data into the memory. These accesses may be made in any order. The digital codes are then transferred sequentially through the DAC port to the DAC. Then they are converted into voltage levels and subsequently distributed to the appropriate analog output channels. A flowchart of the Basic Refresh logic control sequence is shown in Figure 1-4 on page 33.

Operation of the dual port memory is controlled by the Refresh control logic. This circuitry derives its timing from the 16 MHz system clock. The Refresh control logic supervises all data transfers between the memory and the DAC, and controls the distribution of analog voltages to the analog outputs. (Refer to the preceding sections for specific functions of the Refresh logic.) Because the dual port memory must be accessed through both the VMEbus and DAC ports (and possibly by the ADC) arbitration logic is employed during the transfer of data to the DAC to ensure that only one port is active at any time.



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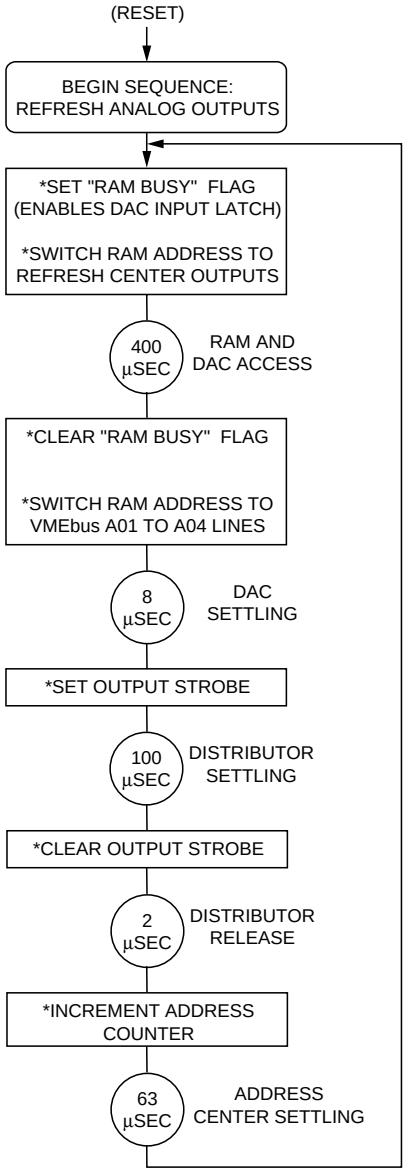



**Figure 1-4** Analog Outputs Refresh Logic; Flowchart



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# Built-in-Test (BIT)

Self-test provisions in the VMIVME-4514A design permit program-controlled verification of all active components on the board. The following paragraphs explain how this is done.

## Self-Test Multiplexers

The signal routing paths and multiplexers involved in board level self-test are shown in Figure 1-5 on page 35. The 16 analog outputs are decoded by the output monitor multiplexer onto a single line which is, in turn, connected by the self-test multiplexer to the input of an analog input multiplexer. This arrangement permits any one of the analog outputs to be sampled by the ADC. It also verifies the operation of the analog input multiplexers by exercising them with known signal levels.

In addition to accepting the selected analog output signal, the self-test multiplexer permits the High and Low inputs of the differential amplifier to be switched simultaneously to signal return. This feature provides a precision "zero" signal for software to use in correcting common "zero" offsets in the analog input channels. There will rarely be a need for this software adjustment. It is used when the input hardware is poorly or strangely calibrated.

Because the high input side of two input signals are used by the output monitor multiplexer (Channels 00 and 08), the low input side of these channels are also routed through this multiplexer. This will give both input lines of these channels the same path impedance and eliminate any offsets due to different input path impedances.

## Loopback Testing of Inputs and Outputs

By routing the analog outputs back through the analog input multiplexers, all of the active components on the board can be exercised in a "loopback" arrangement. The controlling processor can perform a loopback test in either the on-line or off-line mode by setting the output monitor switches appropriately. Then, by sending a specific code to a specific output channel and verifying that the ADC produces approximately the same code after sampling the same channel, the user can verify the operations of the board. Random Polling Mode is the only mode that can be used for loopback testing on the analog outputs. This technique is described in *Random Polling Mode* on page 27 and *Random Polling Mode* on page 57.



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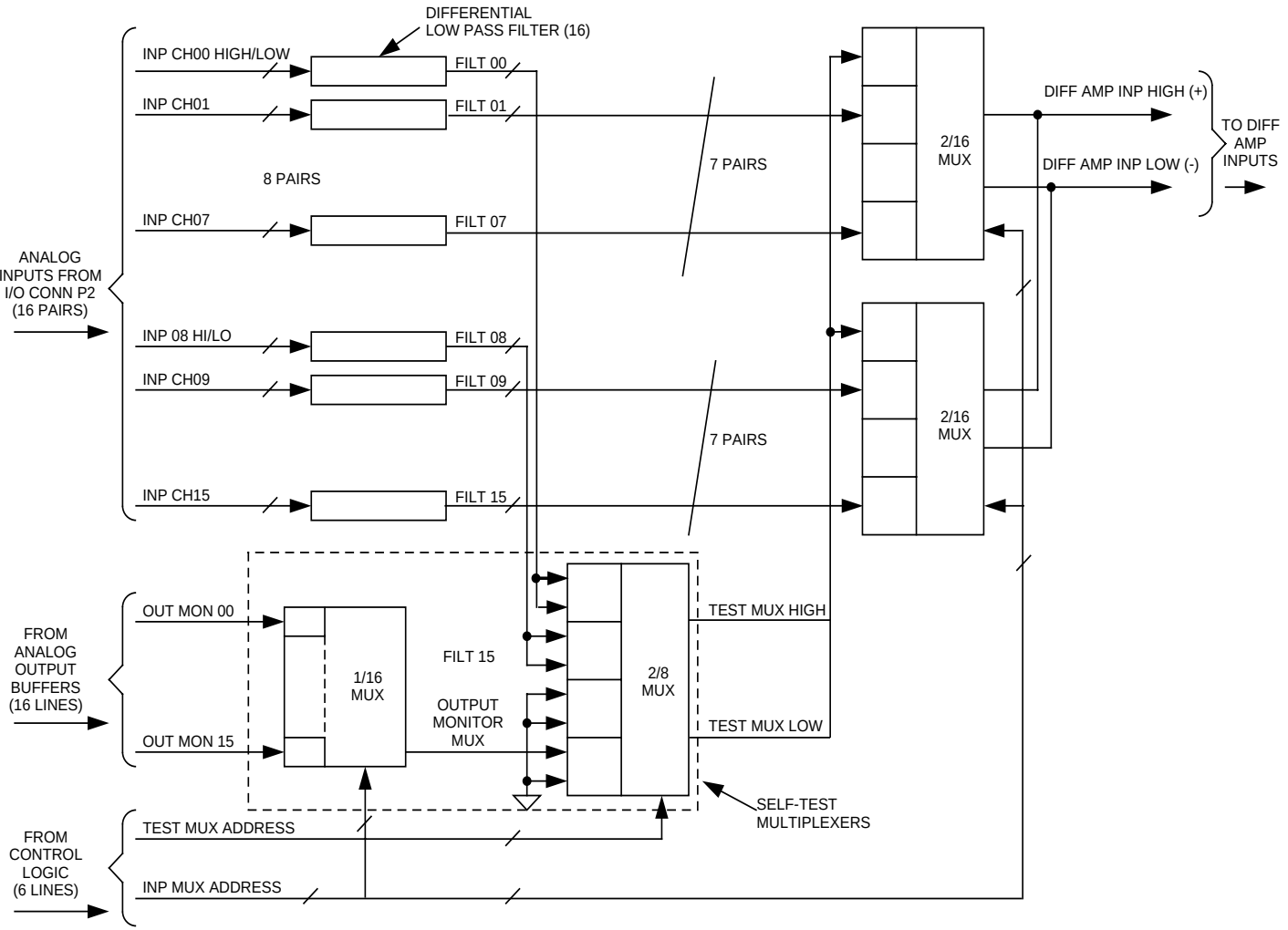



**Figure 1-5** Analog Inputs and Signal Routing



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## Built-In Power Converter

Electrical power for the VMIVME-4514A analog circuitry is supplied by the DC-to-DC converter shown in Figure 1-6 below. This converter transforms +5 V logic power into a regulated and isolated ±15 VDC power source for the analog circuitry, with a load capacity of approximately 300 mA on each 15 V bus.

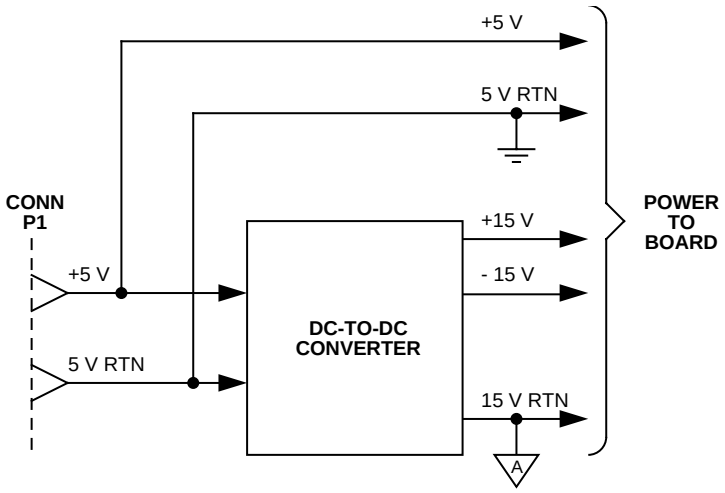



**Figure 1-6** Power Converter



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CHAPTER 2

# Configuration and Installation

## Contents


Unpacking Procedures . . . . . 38
Physical Installation. . . . . 39
Operational Configuration . . . . . 40
Calibration. . . . . 46
Connector Description . . . . . 49


## Introduction

This chapter describes the installation and configuration of the board. Cable configuration, jumper / switch configuration and board layout are illustrated in this chapter.



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## Unpacking Procedures

**CAUTION:** Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).



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# Physical Installation

**CAUTION:** Do not install or remove the boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

## Before applying power: checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming (Sections 3 and 4) been reviewed and applied to the system requirements?
2. Review *Factory-Installed Jumpers* on page 40 and Table 2-4 on page 42 to verify that all factory installed
   jumpers are in place. To change the board address or address modifier response, refer to *Board Address and Address Modifier Selection* on page 40.
3. Have the I/O cables, with the proper mating connectors, been connected to the input/output connector P2? Refer to *Connector Description* on page 49 for a description of the P2 connector.
4. Calibration has been performed at the factory. If recalibration should be required, refer to *Calibration* on page 46.



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# Operational Configuration

The VMIVME-4514A Board's base address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers. The locations and function of all the jumpers on the VMIVME-4514A are shown in Figure 2-1 on page 43 and Table 2-1 on page 41.

## Factory-Installed Jumpers

Each VMIVME-4514A is configured at the factory with the specific jumper arrangement shown in Figure 2-1 on page 43. The factory configuration establishes the following functional baseline for the board, and ensures that all essential jumpers are installed.

- Short I/O base address is set to 0000 HEX.
- I/O access mode is short nonprivileged.
- Input and output ranges are set to ±10 V FSR.

## Board Address and Address Modifier Selection

Jumper headers J8 and J10 permit the VMIVME-4514A Board to be located on any 128-byte boundary within the short I/O address space. The short I/O address space consists of all the addresses between XXXX 0000(HEX) and XXXX FFFF(HEX), where XXXX depends upon the make and model of CPU board used. This requires that 15 address lines be decoded in order to account for all possible base addresses (A01 through A15). Six lines are used for decoding on-board functions (see Section 4). Therefore, the VMIVME-4514A's base address is defined by the remaining nine lines (A07 through A15).

The board's base address is programmed by installing shunts across the jumper posts for each "zero" in the desired address code, and by removing the shunts for each "one" in the code. Address bit A06 has a weight of 64-byte locations. For example, a typical jumper arrangement shown in Figure 2-2 on page 44. It would produce a base address of NNNN 8800(HEX), where NNNN depends upon the CPU board used. Also, the I/O access mode must be selected. This is done with jumper J9. Short supervisory access is selected by omitting the jumper. Short nonprivileged access is selected by installing the jumper. Table 2-4 on page 42 and Figure 2-1 on page 43 show the factory configuration of these jumpers.



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**Table 2-1** Input Functions for Jumpers, Test Points, Potentiometers, and SIPs

| Controls For The VMIVME-4514A Inputs: | |
|---|---|
| **Comp** | **Function** |
| J1 | Omit jumper for 0 to +5 V input range or for ±2.5 V range. |
| J2 | Always Installed |
| J3 | Jumper pins 1 and 2 for bipolar input (±2.5, ±5, or ±10 V). Jumper pins 2 and 3 for unipolar input (0 to +5 V or 0 to +10 V). |
| J4 | Jumper pins 1 and 2 for all input ranges except ±10 V. Jumper pins 2 and 3 for ±10 V input. |
| J7 | To use VMEbus ground as the reference for single-ended inputs. If J7 is not installed, there will be a 40.2 kΩ impedance between the VMEbus ground and the single-ended input ground. |
| J11 | This jumper allows the user to reference an external ground in the input electronics. When the jumper is installed on pins 2 and 3, the user may connect the analog ground of the on-board input electronics to an external analog ground reference (via Pin C16 of Connector P2). This is required for single-ended inputs that are not already referenced to the analog ground of the VMIVME-4514. With the jumper installed on pins 1 and 2, a ground return is provided for output channel 15. |
| | |
| R17 | Unipolar input offset ("zero") adjustment. |
| R18 | Input gain adjustment |
| R19 | Bipolar input offset ("zero") adjustment. |
| | |
| TP1 | Reads input to A / D converter's track-and-hold amp |
| TP4 | Reads analog ground near A / D converter. |
| | |
| RP7 | Input SIP for channels 12 to 15; always installed |
| RP8 | Input SIP for channels 12 to 15; for differential operation |
| RP9 | Input SIP for channels 12 to 15; for single-ended operation |
| RP10 | Input SIP for channels 8 to 11; for single-ended operation |
| RP11 | Input SIP for channels 8 to 11; for differential operation |
| RP12 | Input SIP for channels 8 to 11; always installed |
| RP13 | Input SIP for channels 4 to 7; always installed |
| RP14 | Input SIP for channels 4 to 7; for differential operation |
| RP15 | Input SIP for channels 4 to 7; for single-ended operation |
| RP16 | Input SIP for channels 0 to 3; for single-ended operation |
| RP17 | Input SIP for channels 0 to 3; for differential operation |
| RP18 | Input SIP for channels 0 to 3; always installed |



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**Table 2-2** Output Functions for Jumpers, Test Points, Potentiometers, and SIPs

| Controls For The VMIVME-4514A Outputs: | |
|---|---|
| **Comp** | **Function** |
| J5 | Jumper pins 1 and 2 for 0 to +5 V or ±2.5 V output, Jumper pins 2 and 3 for 0 to +10 V or ±5ÊV output remove for ±10 V output. |
| J6 | Install on pins 1 and 2 for unipolar output (0 to +5 V or 0 to +10 V). Install on pins 2 and 3 for bipolar output (± 2.5, ±5, or ±10 V). |
| | |
| R22 | Unipolar output offset ("zero") adjustment. |
| R9 | Output gain adjustment. |
| R8 | Bipolar output offset ("zero") adjustment. |

**Table 2-3** VMEbus Interface for Jumpers and Test Points Functions

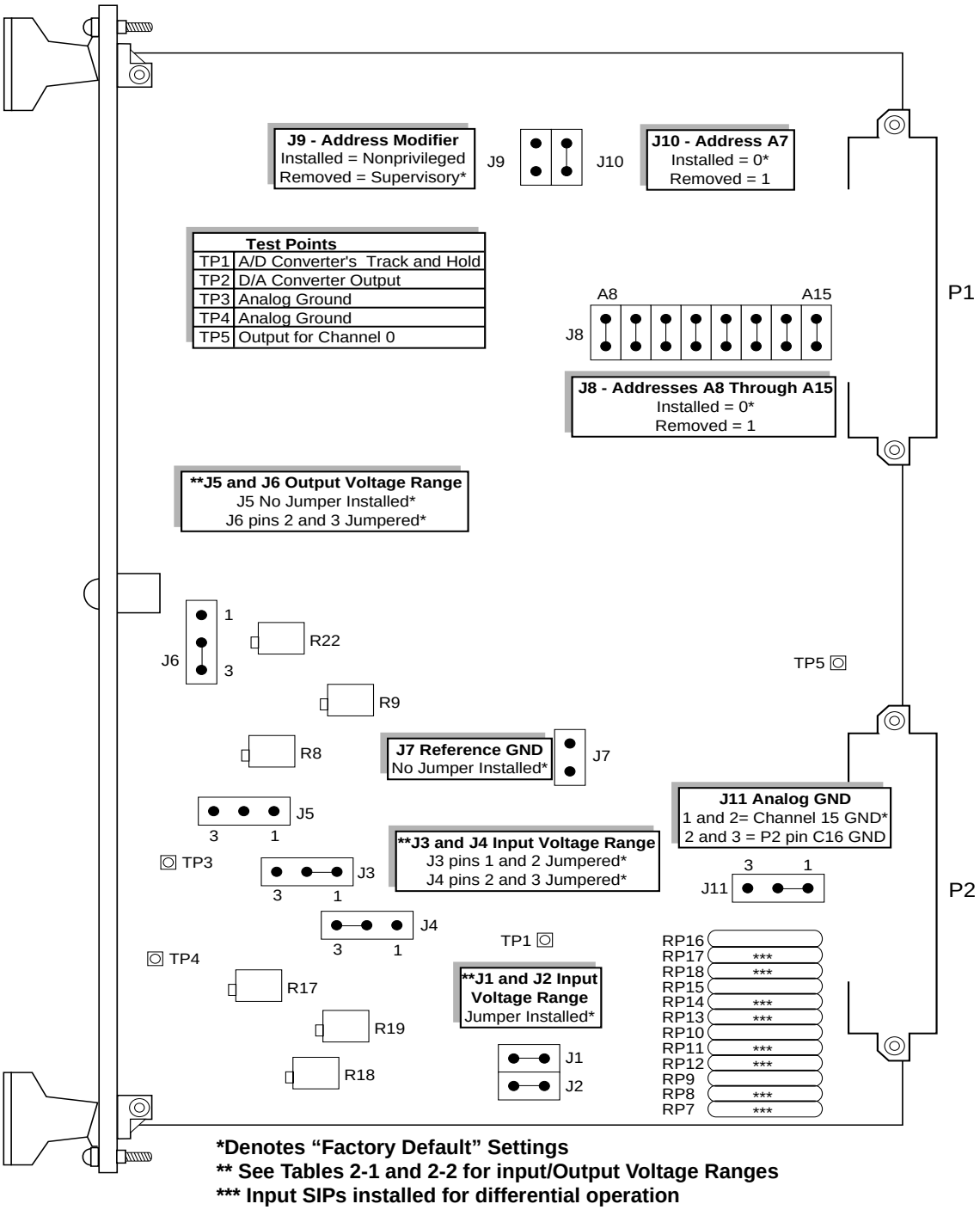
| Controls For The VMIVME-4514A VMEbus Interface: | |
|---|---|
| **Comp** | **Function** |
| TP2 | Reads D / A Converter output. |
| TP3 | Reads analog ground near D / A Converter. |
| TP5 | Reads output Channel 0. |
| | |
| J9 | Controls VMEbus address modifier to which VMIVME-4514A responds. Install for AM code 29 = short nonprivileged. Remove for AM code 2D = short supervisory. |
| J8 | Controls VMEbus short I / O address of VMIVME-4514A, bits A8 to A15. An installed jumper corresponds to a "zero" address bit. |
| J10 | Controls VMEbus address bit A7. An installed jumper corresponds to a "zero" address bit. |

**Table 2-4** Factory Default Jumper Configuration

| Jumper | Positions |
|---|---|
| J1 | Jumpered |
| J2 | Jumpered |
| J3 | Pins 1 and 2 Jumpered |
| J4 | Pins 2 and 3 Jumpered |
| J5 | Open |
| J6 | Pins 2 and 3 Jumpered |
| J7 | Open |
| J8 | Jumpered on all positions |
| J9 | Open |
| J10 | Jumpered |
| J11 | Pins 1 and 2 Jumpered |



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***Denotes "Factory Default" Settings**
**** See Tables 2-1 and 2-2 for input/Output Voltage Ranges**
***** Input SIPs installed for differential operation**

**Figure 2-1** Factory Default Jumpers, Test Points, and Potentiometer Adjustments



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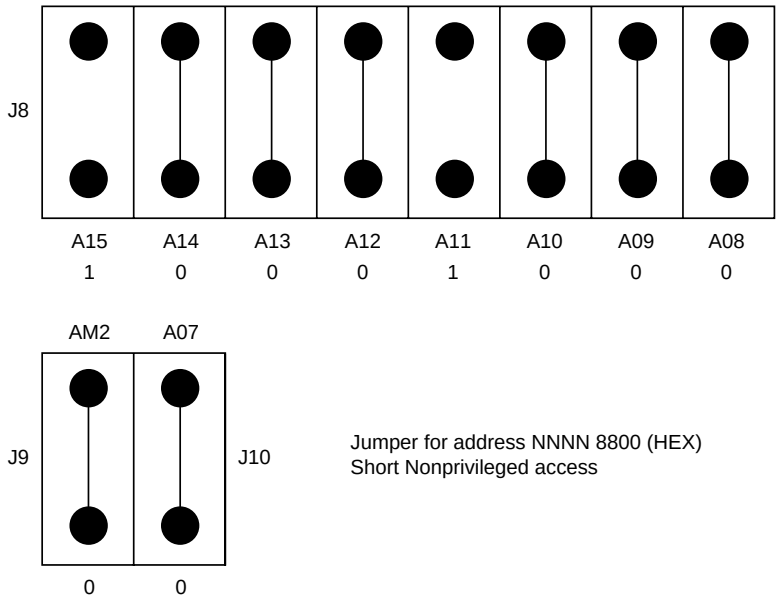



**Figure 2-2** Address Jumpers

## Analog Input Modes

The VMIVME-4514A is factory configured for differential inputs with ±10 V input range. The VMIVME-4514A can be reconfigured in the field for single-ended inputs, and for input ranges of 0 to +5 V, 0 to +10 V, ±5 V, and ±2.5 V.

### Differential or Single-Ended Operation

The sixteen inputs can be configured for differential or single-ended operation in blocks of four. This is done by moving SIP resistor packages among sockets labelled RP7 through RP18. These sockets are near the P2 connector. Channels 0 to 3 are single-ended if RP16 is installed. They are differential if RP17 is installed. For Channels 4 to 7, RP15 allows single-ended operation and RP14 allows differential operation. On Channels 8 to 11, install RP10 for single-ended use or RP11 for differential use. On Channels 12 to 15, install RP9 for single-ended use or RP8 for differential use. The socketed resistor packages, RP7, RP12, RP13, and RP18 must be installed for both single-ended and differential operation.

Any single-ended inputs will be referenced to the VMIVME-4514A's analog ground (and to VMEbus ground) if J7 is installed. To reference these inputs to some other ground, remove J7 and put J11 in the [2-3] position. Pin C16 of the P2 connector is now the external ground sense. When J11 is in the [1-2] position, it provides the ground return for the last output channel.



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## Input Voltage Range

Jumpers J1, J2, J3, and J4 control the input voltage range. Table 2-1 on page 41 shows the possible combinations. Note that self-testing depends on both the input voltage range and the output voltage range. If the ranges do not match, then the input code must be scaled and shifted in software to match the output code.

**Table 2-5** Input Voltage Ranges

| Voltage Range | J1 | J2 | J3 | J4 |
|---|---|---|---|---|
| 0 to +5 | Omitted | Installed | Pins 2 and 3 | Pins 1 and 2 |
| 0 to +10 | Installed | Installed | Pins 2 and 3 | Pins 1 and 2 |
| ±2.5 | Omitted | Installed | Pins 1 and 2 | Pins 1 and 2 |
| ±5 | Installed | Installed | Pins 1 and 2 | Pins 1 and 2 |
| ±10 | Installed | Installed | Pins 1 and 2 | Pins 2 and 3 |
| For both J3 and J4, pin 1 is marked by a square pad on the solder side. | | | | |

## Output Voltage Ranges

Jumpers J5 and J6 control the output voltage range. There are five possible ranges, Table 2-2 shows the ranges and the jumper pin positions.

**Table 2-6** Output Voltage Ranges

| Voltage Ranges | J5 | J6 |
|---|---|---|
| 0 to +5 | Pins 1 and 2 | Pins 1 and 2 |
| 0 to +10 | Pins 2 and 3 | Pins 1 and 2 |
| ±2.5 | Pins 1 and 2 | Pins 2 and 3 |
| ±5 | Pins 2 and 3 | Pins 2 and 3 |
| ±10 | Omitted | Pins 2 and 3 |



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# Calibration

Before shipment from the factory, the VMIVME-4514A is fully calibrated and conforms to all of the specifications listed in document number 800-104514-000. Ultra-precise resistors have been used to make the calibration good for all voltage ranges, but the calibration for ±10 V is dominant. However, should recalibration be required, the recalibration procedures are not difficult. Perform the procedures in *Analog Inputs Calibration Procedure* on page 47 and *Analog Outputs Calibration Procedure* on page 48 with the equipment listed below. The locations of all adjustments and test points are shown in Figure 2-1 on page 43. As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration. All adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

**CAUTION:** Do not install or remove this board with power applied to the system.

## Equipment Required

1. **Digital Voltmeter (DVM)**: With 1.0000 and 10.000 VDC ranges, 5 or more digits, 0.005 percent of the expected voltage measurement accuracy, with a minimum of 10 MΩ input impedance. **This is used for calibrating the outputs.**
2. **Digital Voltage Source:** With a 10.000 VDC range, resolution of 0.0005 VDC, accuracy of 0.005 percent of the expected value, and 0.10Ω maximum output impedance. **This is used for calibrating the inputs**.
3. **Chassis.** VMEbus backplane or equivalent, with J1 and J2 connectors, a VMEbus master controller, a +5 VDC 0.1 VDC power supply, and one slot allocated for testing the VMIVME-4514A Board.
4. **Extender board:** One VMEbus extender board.
5. **Test cables:** Enough test cables for the equipment listed above.
6. **CPU:** A VMEbus computer that will be used to control the VMIVME-4514A.



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## Analog Inputs Calibration Procedure

1. Install the VMIVME-4514A Board on an extender board in an open slot of the VMEbus backplane.
2. Configure the analog inputs for the desired input range. (See “Analog Input Modes” on page 44.)
3. Apply power to the backplane. Allow a minimum warmup time of ten minutes before proceeding.
4. Connect the digital voltage source between connector pins P2-A17 (+) and P2-C17 (-).
5. Write the 16-bit value 1000(HEX) to the Control and Status Register (CSR) at the board's base address +2.
6. If you are using a bipolar input range, set the voltage source for 0.0000 VDC. If you are using 0 to 5 V, set it for 2.5000 VDC. If you are using 0 to 10 V, set it for 5.0000 VDC.
7. If you are using a bipolar input range, adjust R19 (Bipolar Input Offset) for the next step. If you are using a unipolar input range, adjust R17 (Unipolar Input Offset) for the next step.
8. Repeatedly read the 16-bit register at the board's base address +40 (HEX) and adjust R17 or R19 until the reading is 0800 (HEX).
9. Set the voltage source to produce a voltage of "full-scale" minus 1.5 bits. For 0 to 5 V, this is 4.9982 V. For 0 to 10 V, it is 9.9963 V. For ±2.5 V, this is 2.4982 V. For ±5 V, this is 4.9963 V. For ±10 V, it is 9.9927 V.
10. Repeatedly read the 16-bit register at the board's base address + 40 (HEX) and adjust R18 until the reading is alternating between 0FFE (HEX) and 0FFF (HEX).
11. Repeat steps 6 through 10 until no adjustment is necessary.
12. Calibration of the analog inputs is completed. Remove all test connections, and restore the board to its original configuration.
13. All unused inputs should be grounded.



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## Analog Outputs Calibration Procedure

1. Install the VMIVME-4514A Board on an extender board in an open slot of the VMEbus backplane.
2. Configure the analog inputs for the desired input range. (See “Analog Input Modes” on page 44.)
3. Apply power to the backplane. Allow a minimum warmup time of ten minutes before proceeding.
4. Connect the digital voltmeter across pins A1 (+) and C1 (-) of the P2 connector (or TP5(+) and TP3(-)).
5. Write the 16-bit word 1800 (HEX) to the CSR at offset address + 2.
6. Write the 16-bit value 0000 (HEX) to the analog output Channel 00 register at the offset address of 0020 (HEX).
7. If you are using a bipolar output range, adjust R8 to produce a minus full-scale reading on the DVM (read -2.5, -5, or -10 V). If you are using a unipolar output range, adjust R22 to produce a 0 VDC reading.
8. Write the 16-bit value 0FFF (HEX) to the output Channel 00 register at the board's offset address 0020 (HEX).
9. Adjust R9 to produce a reading of plus full-scale. For unipolar output, the reading should be 4.9988 or 9.9976 V. For bipolar output, the reading should be 2.4988, 4.9976, or 9.9951 V.
10. Repeat steps 6 through 9 until no adjustment is necessary.
11. This completes the calibration of the analog outputs. Remove power and all test connections. Restore the board to its original configuration.



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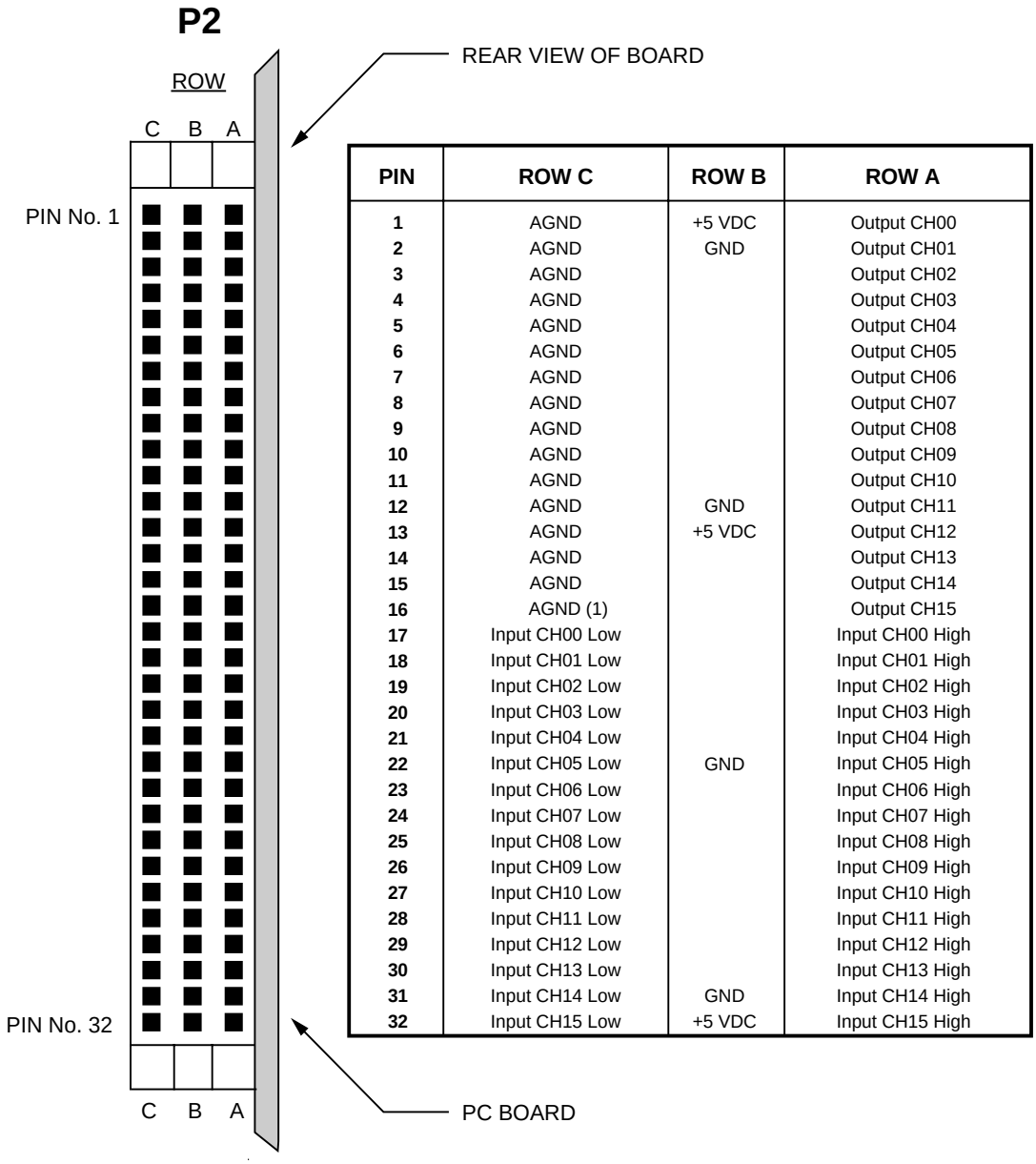
## Connector Description

Two 96-pin DIN connectors, P1 and P2, provide all connections to the VMIVME-4514A Board. P1 contains the address, data and control lines, and all additional signals necessary to control the VMEbus functions of the board. P2 provides the connections for the 16 analog input and output channels.

Orientation of the P2 connector and signal assignments are shown in Figure 2-3 on page 50. The mating connector for P2 (Panduit Model 120-964-435E or equivalent) is designed to be used with a standard 64-wire ribbon-cable with conductor spacing of 0.050 inches. In environments where there is a high degree of electrical noise, a twisted-pair ribbon cable with an overall shield is recommended.



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| PIN | ROW C | ROW B | ROW A |
|---|---|---|---|
| 1 | AGND | +5 VDC | Output CH00 |
| 2 | AGND | GND | Output CH01 |
| 3 | AGND | | Output CH02 |
| 4 | AGND | | Output CH03 |
| 5 | AGND | | Output CH04 |
| 6 | AGND | | Output CH05 |
| 7 | AGND | | Output CH06 |
| 8 | AGND | | Output CH07 |
| 9 | AGND | | Output CH08 |
| 10 | AGND | | Output CH09 |
| 11 | AGND | | Output CH10 |
| 12 | AGND | GND | Output CH11 |
| 13 | AGND | +5 VDC | Output CH12 |
| 14 | AGND | | Output CH13 |
| 15 | AGND | | Output CH14 |
| 16 | AGND (1) | | Output CH15 |
| 17 | Input CH00 Low | | Input CH00 High |
| 18 | Input CH01 Low | | Input CH01 High |
| 19 | Input CH02 Low | | Input CH02 High |
| 20 | Input CH03 Low | | Input CH03 High |
| 21 | Input CH04 Low | | Input CH04 High |
| 22 | Input CH05 Low | GND | Input CH05 High |
| 23 | Input CH06 Low | | Input CH06 High |
| 24 | Input CH07 Low | | Input CH07 High |
| 25 | Input CH08 Low | | Input CH08 High |
| 26 | Input CH09 Low | | Input CH09 High |
| 27 | Input CH10 Low | | Input CH10 High |
| 28 | Input CH11 Low | | Input CH11 High |
| 29 | Input CH12 Low | | Input CH12 High |
| 30 | Input CH13 Low | | Input CH13 High |
| 31 | Input CH14 Low | GND | Input CH14 High |
| 32 | Input CH15 Low | +5 VDC | Input CH15 High |

**Figure 2-3** P2 Connector and Pinout

(1) AGND when Jumper J11 is installed in the 1 to 2 position. When Jumper J11 is installed in the 2 to 3 position, Row C, Pin 16 can be used as an external ground sense for single-ended mode (See “Differential or Single-Ended Operation” on page 44.).



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CHAPTER

3

# Programming

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## Introduction

Communication with the VMIVME-4514A Analog I/O (AIO) Board takes place through 64 contiguous 16-bit register locations mapped into the VMEbus short I/O address space. The short I/O address space consists of all locations within the address range from XXXX0000 HEX to XXXXFFFF HEX*. The function of each communication register and its offset address is summarized in Table 3-1 on page 53. These registers will be discussed in more detail in this section of the manual.



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## Control and Status Register Description

The Control and Status Register (CSR) located at relative (or offset) address 02H contains all of the flags necessary to control and monitor the following board operations:

- Analog input channel selection
- Analog-to-Digital (A / D) conversion
- Built-in-Test (BIT)
- Analog outputs on-line / off-line
- Analog outputs refresh rate
- Front panel Fail indicator
- Board RESET

The CSR is 16 bits in length. The function of each control bit and status flag is described in Table 3-2 on page 54 and in more detail in the programming discussions that follow.



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## Initialization By Reset

When a SYSTEM RESET (the VMEbus signal) is applied to the board, all of the bits in the CSR are cleared to the LOW state or "zero". VMEbus systems automatically apply a SYSTEM RESET when they power-up. After SYSTEM RESET is removed, the VMIVME-4514A will Auto Scan its inputs, and its outputs will be off-line.

**NOTE:** *XXXX indicates "Don't Care" on the upper 16 address lines. The VMEbus modifiers indicate access to the short I/O (A16) address space. The CPU will access the short I/O address space via some 32-bit address range. Please refer to the CPU's manual for this information.

**Table 3-1** VMIVME-4514A Register Map

| Offset Address (Hex) | Offset Address (DEC) | Register Designation | Suggested Mnemonic | Access |
|---|---|---|---|---|
| 00 | 00 | Board Identification Register** | BD ID | Read |
| 02 | 02 | Control/Status Register | CSR | Read/Write |
| 04 | 04 | Convert Data Register (Random Polling Mode Only) | CDR | Read |
| 06 | 06 | Scan Size Register | SSR | Read/Write |
| 08-1E | 08-30 | Reserved* | | |
| 20 | 32 | Output data, Dual Port Register CH00 | ODPR00 | Read/Write |
| 22 | 34 | Output data, Dual Port Register CH01 | ODPR01 | Read/Write |
| 24 | 36 | Output data, Dual Port Register CH02 | ODPR02 | Read/Write |
| 26 | 38 | Output data, Dual Port Register CH03 | ODPR03 | Read/Write |
| 28 | 40 | Output data, Dual Port Register CH04 | ODPR04 | Read/Write |
| 2A | 42 | Output data, Dual Port Register CH05 | ODPR05 | Read/Write |
| 2C | 44 | Output data, Dual Port Register CH06 | ODPR06 | Read/Write |
| 2E | 46 | Output data, Dual Port Register CH07 | ODPR07 | Read/Write |
| 30 | 48 | Output data, Dual Port Register CH08 | ODPR08 | Read/Write |
| 32 | 50 | Output data, Dual Port Register CH09 | ODPR09 | Read/Write |
| 34 | 52 | Output data, Dual Port Register CH10 | ODPR10 | Read/Write |
| 36 | 54 | Output data, Dual Port Register CH11 | ODPR11 | Read/Write |
| 38 | 56 | Output data, Dual Port Register CH12 | ODPR12 | Read/Write |
| 3A | 58 | Output data, Dual Port Register CH13 | ODPR13 | Read/Write |
| 3C | 60 | Output data, Dual Port Register CH14 | ODPR14 | Read/Write |
| 3E | 62 | Output data, Dual Port Register CH15 | ODPR15 | Read/Write |
| 40 | 64 | Input data, Dual Port Register CH00 | INPR00 | Read/Write |
| 42 | 66 | Input data, Dual Port Register CH01 | INPR01 | Read/Write |
| 44 | 68 | Input data, Dual Port Register CH02 | INPR02 | Read/Write |
| 46 | 70 | Input data, Dual Port Register CH03 | INPR03 | Read/Write |
| 48 | 72 | Input data, Dual Port Register CH04 | INPR04 | Read/Write |
| 4A | 74 | Input data, Dual Port Register CH05 | INPR05 | Read/Write |
| 4C | 76 | Input data, Dual Port Register CH06 | INPR06 | Read/Write |
| 4E | 78 | Input data, Dual Port Register CH07 | INPR07 | Read/Write |
| 50 | 80 | Input data, Dual Port Register CH08 | INPR08 | Read/Write |



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**Table 3-1** VMIVME-4514A Register Map (Continued)

| Offset Address (Hex) | Offset Address (DEC) | Register Designation | Suggested Mnemonic | Access |
|---|---|---|---|---|
| 52 | 82 | Input data, Dual Port Register CH09 | INPR09 | Read / Write |
| 54 | 84 | Input data, Dual Port Register CH10 | INPR10 | Read / Write |
| 56 | 86 | Input data, Dual Port Register CH11 | INPR11 | Read / Write |
| 58 | 88 | Input data, Dual Port Register CH12 | INPR12 | Read / Write |
| 5A | 90 | Input data, Dual Port Register CH13 | INPR13 | Read / Write |
| 5C | 92 | Input data, Dual Port Register CH14 | INPR14 | Read / Write |
| 5E | 94 | Input data, Dual Port Register CH15 | INPR15 | Read / Write |
| 60-7E | 96-126 | Reserved* | | |

**NOTE:** *Reserved locations are generally duplicates of useful registers. For instance, offset 0A here currently has the same functionality as the formal CSR location. In future revisions, reserved locations may have different effects. It would be poor programming practice to use them. **Register contains a fixed value of 09XX HEX.

**Table 3-2** Control/Status Register Bit Map

| Control/Status Register (Offset 02) Read/Write, Byte | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| Short Settling / New Data Ready | Fail LED | Start Convert End of Scan | 2's Compl | Outputs on Line | Test Mode 1 | Test Mode 0 | Fast Refresh |

| Bit 07 | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
|---|---|---|---|---|---|---|---|
| Mode 1H | Start Settling | Scan Halt | Mode 0H | MUX A3 | MUX A2 | MUX A1 | MUX A0 |

## *Control/Status Register Bit Definitions*

**Bit 15:** **Short Settling/New Data Ready** - Writing a "one" here will decrease the refresh time and thus increase the input scan rate. When read, this bit shows the status of the CDR. If it is a "one", there is valid data in the CDR for the host to read.

**Bit 14:** **Fail LED** - This bit turns ON and OFF the front panel LED. Writing a "one" here will turn off the LED. A "zero" turns it ON.

**Bit 13:** **Start Convert/End-Of-Scan** - Writing a "one" to this bit location will begin a conversion sequence. Reading a "one" in this bit location indicates a scan has finished.



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**Bit 12:** **2's Compl** - When this bit is low, "a logic zero" the data format used is two's complement. Write a "one" to this bit location to change to offset binary data format.

**Bit 11:** **Outputs On-Line** - Write a "one" to this position when the outputs are to be connected to the external circuits.

**Bits 10-09:** **Test Mode [1..0]** - The Test Mode bits determine what the loop back registers will monitor.

**Bit 08:** **Fast Refresh** - Writing a "one" here will decrease the refresh time and thus increase the scan rate for the outputs.

**Bit 07:** **Mode 1H** - Bit 07 (Mode 1H) and bit 04 (Mode 0H) establish the operating mode of the board. See Table 3-3 for operating mode functions.

**Bit 06:** **Start Settling** - When a "one" is written to this bit, the switching multiplexers will change to the channel stated in the "MUX" address lines (D03 to D00). Always reads as a logic "zero".

**Bit 05:** **Scan Halt** - Writing a "one" at this location will stop the sequencer and set the SSR for 16 channels. This bit MUST be cleared before normal operations can commence.

**Bit 04:** **Mode 0H** - Bit 04 (Mode 0H) and D07 (Mode 1H) establish the operating mode of the board. See the following table for operating mode functions.

**Table 3-3** Operating Modes 1H and 0H Functions

| Mode 1 (Bit 7) | Mode 0 (Bit 4) | Function |
|---|---|---|
| 0 | 0 | Auto Scanning |
| 0 | 1 | Random Polling |
| 1 | 0 | Scanning Poll |
| 1 | 1 | Not Used |

**Bits 03 Through 00: MUX [A3...A0]** - These bits are used to select the input channel to convert.



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# Controlling and Reading the Analog-to-Digital Converter (ADC)

The VMIVME-4514A has a number of features which allow it to be used in a variety of applications. The simplest mode of operation is the Auto Scanning Mode. Activating the other control modes is discussed in *Changing A/D Operating Modes* on page 64.

## Auto Scanning Mode

This mode is entered when the board has power applied to it, after a hardware reset, or when the A/D mode control bits in the CSR are cleared to "zero." This mode allows the user to operate the board without setting any of the control bits in the CSR or selecting any channel for conversion. When Auto Scanning is activated, the board initiates a conversion on CH0. When that is finished, the board moves on to CH1 and so on. After CH15 has been digitized, the cycle begins again with CH0.

After each conversion, the data for that particular channel is stored in a dual port register assigned to that input. With every scan, new data is put in the register. This overwrites the old data. Thus, only the freshest data is in the register. This register is accessible by the VMEbus and may be *read* at any time. To enter the Auto Scanning Mode under program control, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be cleared (or set to "zero"). These bits are part of a data word that is written to the CSR. An example of how to enter this mode is shown in *Changing A/D Operating Modes* on page 64.

## Scanning Poll Mode

The Scanning Poll Mode performs a single scan of all the input channels and then stops. Data bit D13 in the CSR is used by the host CPU to monitor the completion of this scan. D13 is called REGD END OF SCAN H. When it goes high (a logic "one"), the scan is complete and data is ready for the host to read. To enter the Scanning Poll Mode under program control, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be set to "one" and "zero," respectively. These bits are part of a data word that is written to the CSR. An example of how to enter this mode is shown in *Changing A/D Operating Modes* on page 64.

## Scan Size Register

The Scan Size Register (SSR) is located at relative (or offset) address 06 Hex. This register is used during Auto Scan and Scan Poll modes. It can be loaded with a value of 0 through 10 Hex for scanning from 1 to 16 channels.Table 3-4 on page 57 shows which channels are scanned when writing to the SSR if utilizing Auto Scan or Scanning Poll modes.

At power up or after a system reset, Auto Scanning Mode is entered with all 16 channels scanned. If the user does not wish to Auto Scan all 16 inputs, a value smaller than 10 Hex can be written to the SSR. If the user is using Scan Polling mode, the SSR must be loaded with the desired number of channels to scan prior to starting the scan. To enable a write to the SSR, the Scan Halt bit (D05) in the CSR must be a logical "zero". A logical "one" in the Scan Halt bit will set the SSR for 16 channels and disable any writes to the SSR.



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**Table 3-4** Scan Size Register

| SSR Programming Value (HEX) | Number of Channels Scanned | Scanned Channels |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 1 | 0 |
| 2 | 2 | 0-1 |
| 3 | 3 | 0-2 |
| 4 | 4 | 0-3 |
| 5 | 5 | 0-4 |
| 6 | 6 | 0-5 |
| 7 | 7 | 0-6 |
| 8 | 8 | 0-7 |
| 9 | 9 | 0-8 |
| A | 10 | 0-9 |
| B | 11 | 0-10 |
| C | 12 | 0-11 |
| D | 13 | 0-12 |
| E | 14 | 0-13 |
| F | 15 | 0-14 |
| 10 | 16 | 0-15 |

## Random Polling Mode

The Random Polling Mode is the traditional method of controlling an A/D conversion. The CPU selects the channel to be converted. This is done by setting the MUX A3 through MUX A0 bits (D3 to D0) in the CSR to the value for the input in question. At the same time, D13 of the CSR (EN START CONV H) is set HIGH. This starts the multiplexer acquisition and the ADC timing sequence. *ADC Control* on page 26 has a detailed explanation of this. Now the CPU must poll the New Data RDY H bit (D15) in the CSR. If this is done by successively reading the CSR, digital noise may corrupt the reading. It is better to wait until the conversion time has expired, then read the CSR and test the bit. When this bit goes HIGH, the conversion is complete and the data is ready. Finally, the CPU reads the data. A new channel is selected and this process is repeated. Figure 3-1 on page 59 is a flowchart for such a process. This method is useful when the desired channels are not in sequence. Here any channel can be selected in any "random" order. It is also used when the same channel must be converted more often (or exclusively) than the others. This is the only mode which can test the outputs.

Each time a new channel is selected for conversion, the CSR bits A/D Mode 1H (D7) and A/D Mode 0H (D4) must be set to "zero" and "one," respectively. These bits are part of a data word that is written to the CSR. An example of how to enter this mode is show in *Changing A/D Operating Modes* on page 64.



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## Converter Data Register (CDR),-Random Polling Mode Only

A 16-bit *read only* register at offset address 04 (HEX) is used to store the data converted during the random poll mode. Data in this register is 12 bits, right-justified. D12 through D15 are always "zero" in the binary or offset binary data mode. In the two's complement data mode they are the sign extension of the data (see Table 3-5 below).

## Reading ADC Codes

The data format of the ADC is shown in Table 3-5 on page 58. This data can be straight binary, offset binary, or two's complement. This is controlled by the configuration of the ADC input range selection jumpers and the state of the 2's COMPL control bit in the CSR. Some converter output codes are summarized in Table 3-5 below. This table shows the values of data produced at major points within the full-scale ranges of the board.

For any offset binary converter code using the Bipolar Range, the associated input voltage is obtained from the following equation:

Output / Input (Volts) = $-E_{FSR} / 2 + E_{FSR}$ X [Channel Data In Decimal] / 4096,

where $E_{FSR}$ is the full-scale range voltage. (e.g., $E_{FSR}$ = 10 V for the ±5 V range.)

If the input voltage is for a straight binary code (Unipolar Range) or for a two's complement code (Bipolar Range), then use this equation:

Output / Input (Volts) = $+E_{FSR}$ X [Channel Data In Decimal] / 4096.

**NOTE:** Negative two's complement numbers must be translated to negative decimal output codes, e.g., FC00 (HEX) = -1024 (DECIMAL). If this code is for a +5 V input range, then the input voltage is +1.25 V (1.25 V = +5 V (1024 / 4096)).

**Table 3-5** Data Formats (in HEX)

| Unipolar Voltage | Bipolar Voltage | Offset Binary | Two's Complement |
|---|---|---|---|
| 0 V | -10 V | 000 | 800 |
| 2.5 V | -5 V | 400 | C00 |
| 5.0 V | 0 V | 800 | 000 |
| 7.5 V | 5 V | C00 | 400 |
| 9.9976 V | 9.9951 V | FFF | 7FF |



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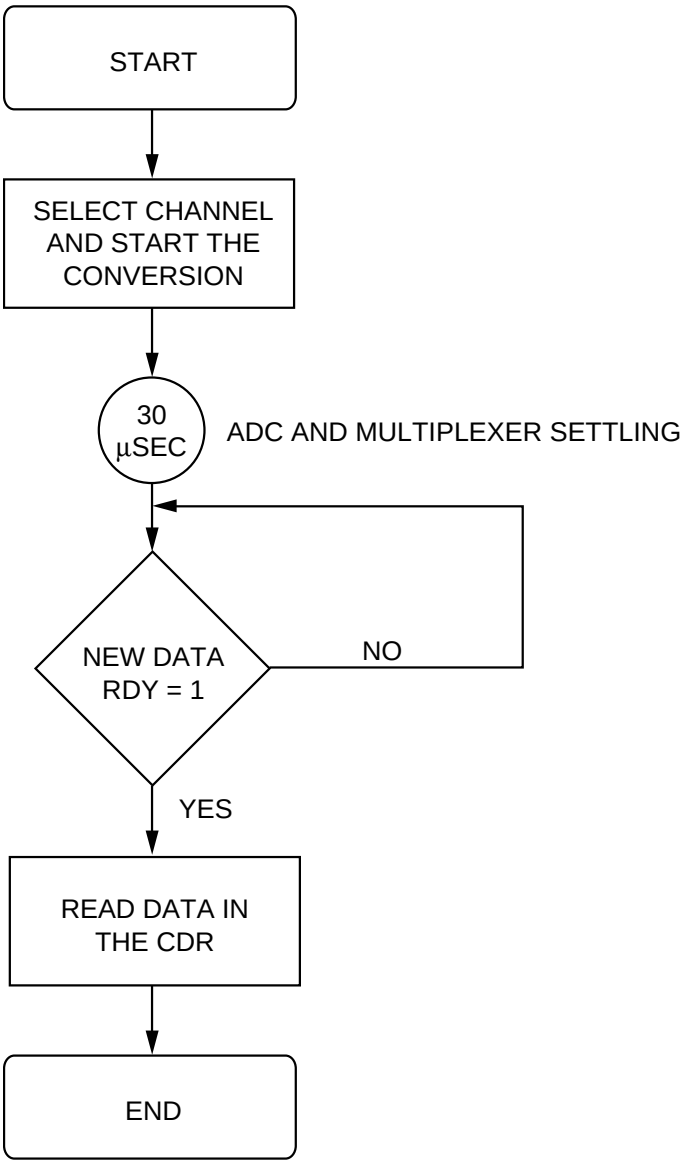



**Figure 3-1** Random Polling Flowchart



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## Operating Sequence Examples

Table 3-6 shows an example of each of the different operating sequences available with the VMIVME-4514A. Please note that these examples show only one variation of each possible control word. Other valid control words are formed by adding $8000, $4000, $1000, $800, and / or $100 ($ implies hexadecimal values) to the examples for any write to the CSR.

**Table 3-6** Operation Sequence Examples

| Mode | Example Sequence (All numbers are in hexadecimal) |
|---|---|
| Auto Scanning | 1. Read data from the IDPRs (offset addresses 40 thru 5E) |
| Scanning Poll | 1. Write the number of channels (e.g., 10) to the SSR (offset address 06). This must be done after the board is powered-up or whenever a change is desired.<br>2. Write 2080 to the CSR (offset 02).<br>3. Wait for the scan to finish. Bit 13 of the CSR will go HIGH (logic "1").<br>4. Read the data from the IDPRs. |
| Random Poll | 1. Write 201x to the CSR,(X : representing desired channel (0....F)).<br>2. Wait for the conversion to finish. Bit 15 of the CSR will go HIGH (logic "1").<br>3. Read the data from the CDR (offset address 04). |



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# Controlling the Analog Outputs

The 16 analog output channels appear to the controlling processor as 16 consecutive 16-bit words in the address space assigned to the VMIVME-4514A board starting at an offset address of 20 (HEX). The register map shown in Table 3-1 on page 53 lists the board's offset address for each output channel. Each analog output register supports both read and write operations, eliminating the need for corresponding "shadow" registers in the processor Random Access Memory (RAM) space.

## Writing to the Outputs

Digital voltage codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four bits (D12 to D15) will be ignored. The Digital-to-Analog (D/A) data format and coding conventions are shown in Table 3-5 on page 58. Each output will respond to a new code within 1.7 msec (0.4 msec in the Fast Refresh Mode) after the code is written to the Output Register.

## "Fast Refresh"

Setting the Fast Refresh control bit (Table 3-2 on page 54) HIGH will reduce the analog output Refresh time from the default value of 1.7 to 0.4 msec. The Fast Refresh Mode raises the output Nyquist frequency (maximum output signal frequency) from approximately 300 Hz to 1.2 kHz at the expense of some accuracy.

## Off-line Operation

Setting the Output On-Line control bit HIGH (Table 3-2 on page 54) connects the analog outputs to the P2 I/O connector for normal system operation. Clearing the bit LOW disconnects the analog outputs from P2 and is normally used for loopback testing because the output buffers can still monitor the outputs through the self-test multiplexers.



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# Self-Testing the VMIVME-4514A Board

Built-In-Test (BIT) provisions include loop back testing and the measurement of analog input offset voltages. These capabilities permit self-contained, board level performance verification. Random Polling Mode is the only mode that can be used for self-testing. The control of the self-test modes is summarized in Table 3-7 below.

**NOTE:** Random polling mode is the only mode that can be used for self-testing.

**Table 3-7** Self-Test Control Modes

| CSR Control Bits | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Self-Test Mode** | **D10** | **D9** | **D7** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Normal Operation* | 0 | 0 | X | X | X | X | X | X |
| Reserved | 0 | 1 | X | X | X | X | X | X |
| Test Input Offset | 1 | 0 | 0 | 1 | ** | X | X | X |
| Test Analog Outputs | 1 | 1 | 0 | 1 | Selected Analog Output Channel | | | |

**NOTES:** * With D10 and D9 cleared, 07 and 04 select the mode of operation. (See “Controlling and Reading the Analog-to-Digital Converter (ADC)” on page 56.) ** Set this to a "zero" to test the input Channel 00 to 07 multiplexer, or a "one" to test the Channel 08 to15 multiplexer.

## Loopback Testing of Inputs and Outputs

By routing the analog outputs through the input multiplexers, the operation of all the active components on the VMIVME-4514A Board can be verified. This Loopback Test is performed by selecting one of the 16 analog output channels. The selected output channel can then be exercised by the controlling processor, and monitored by the VMIVME-4514A ADC to verify that the signal path is operating correctly. This technique is illustrated in Figure 3-2 on page 63.



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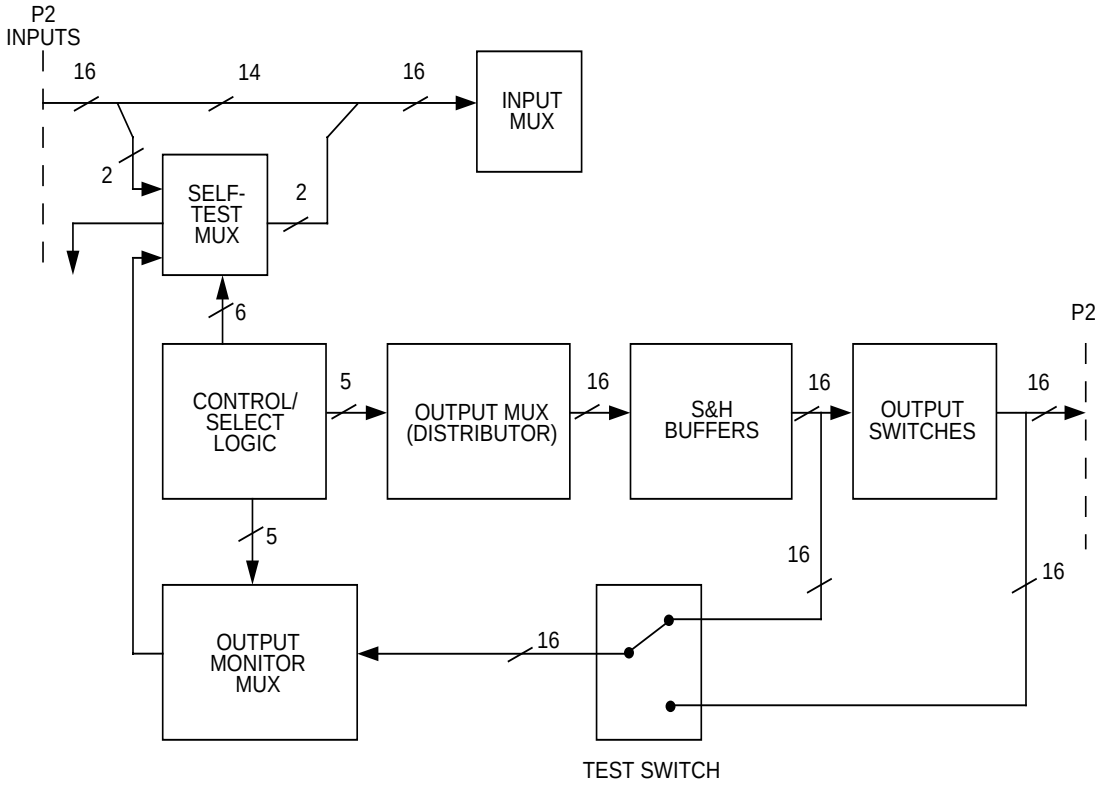



**Figure 3-2** Block Diagram of Loopback Testing



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## Changing A/D Operating Modes

The board powers-up in the Auto Scanning Mode. To switch from Auto Scanning to another mode, the sequencer **must** be stopped. This will synchronize the timing control logic. The sequence of events is (1) writing a control word that sets the Scan Halt (D5) bit HIGH and the desired operating mode in the A/D Mode bits (D7 and D4), (2) writing a control word that clears the Scan Halt (D5) bit LOW *(include the A/D Mode settings from step 1)*, and (3) rewrite the A/D Mode **and set** the Start Conv H bit (D13) HIGH in the CSR to start the A/D conversion sequence. Table 3-8 shows the proper sequence and some example control words to switch to each of the A/D operating modes. No reset is needed to move between the Scanning Poll Mode and the Random Poll Mode. Also, no reset is needed to move from one of these modes to the Auto Scanning Mode.

**Table 3-8** How to Switch Among A/D Modes

| Scanning Mode Change | Example Control Word Sequence |
|---|---|
| Old mode: Auto Scanning<br>New mode: Scanning Poll | 1. Write $00A0 to the CSR. Set the mode and stop scanning.<br>2. Write $0080 to the CSR. Keep the mode and start scanning.<br>3. Write the number of channels to scan to the SSR . |
| Old mode: Auto Scanning<br>New mode: Random Poll | 1. Write $0030 to the CSR. Set the mode and stop scanning.<br>2. Write $0010 to the CSR. Keep the mode and start scanning. |
| Old mode: Scanning Poll<br>New mode: Auto Scanning | 1. Write $0000 to the CSR. Set the mode and begin conversions.<br>2. Write the number of channels to scan to the SSR (if a new scan size is desired). |
| Old mode: Scanning Poll<br>New mode: Random Poll | 1. No transition is necessary. Simply begin the Random Poll process. |
| Old mode: Random Poll<br>New mode: Auto Scanning | 1. Write $0000 to the CSR. Set the mode and begin conversions.<br>2. Write the number of channels to scan to the SSR (if a new scan size is desired). |
| Old mode: Random Poll<br>New mode: Scanning Poll | 1. No transition is necessary. Simply begin the Scanning Poll process.<br>2. Write the number of channels to scan to the SSR . |



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# *Maintenance*

## Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com



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# Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.



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