VMIVME-4911
Quad Channel Synchro/Resolver-to-Digital Input Board with Built-in-Test

Product Manual

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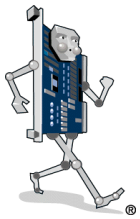

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Overview

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Introduction

The VMIVME-4911 is a VMEbus compatible quad channel synchro / resolver-to-digital converter input board which utilizes one synchro / resolver-to-digital module and a quad multiplexer to convert synchro / resolver data to a 14-bit digital word. Features of the VMIVME-4911 Synchro / Resolver-to-Digital Board include the following:

- Synchro or resolver inputs
- 14-bit accuracy
- Jumper programmed input selection receives synchro / resolver inputs from the field connector or from the Synchro / Resolver Test Bus Backplane (SRTbus™) for channel zero.
- 26 Vrms or 115 Vrms reference excitation level (option dependent).
- Jumper selection of ±15 VDC power and reference voltage input from test backplane or I / O field connector.
- Supports Built-in-Test on digital-to-synchro / resolver modules with channel zero jumper option.
- Supports expansion synchro / resolver multiplexer boards.

Functional Description

This paragraph describes the functional operation of the VMIVME-4911 Synchro / Resolver-to-Digital Input Board. The synchro / resolver-to-digital converter board consists of VMEbus compatibility logic, a synchro / resolver converter, a quad multiplexer, power input jumper selection, and jumper input selection to support Built-in-Test capabilities, as shown in Figure 1.1-1. The VMEbus compatibility logic contains address selection logic and data transfer logic providing for 8- or 16-bit data transfers. Jumper selection logic provides an option for channel 0 synchro / resolver signals to be sourced from the P3 I / O connector or from the P2 connector via the Synchro / Resolver Test Bus Backplane (SRTbus™). In addition, the ±15 VDC power supply can be jumpered to select P3 I / O connector input or the SRTbus™ input.

The synchro / resolver-to-digital input board converts the input of the user's synchro or resolver to a digital format. The board accepts synchro or resolver inputs of 11.8 volts rms line-to-line, 90 volts rms line-to-line, or resolver inputs of 26 volts rms line-to-line. Each of the three variations of the board are available with 14-bit resolution. The user options are given in document number 800-004911-000.

The VMIVME-4911 is also available without the converter module installed, in which case, the board is an expansion multiplexer. Up to (TBD) 4911 multiplexer expansion boards may be connected to one VMIVME-4911 Converter Board.

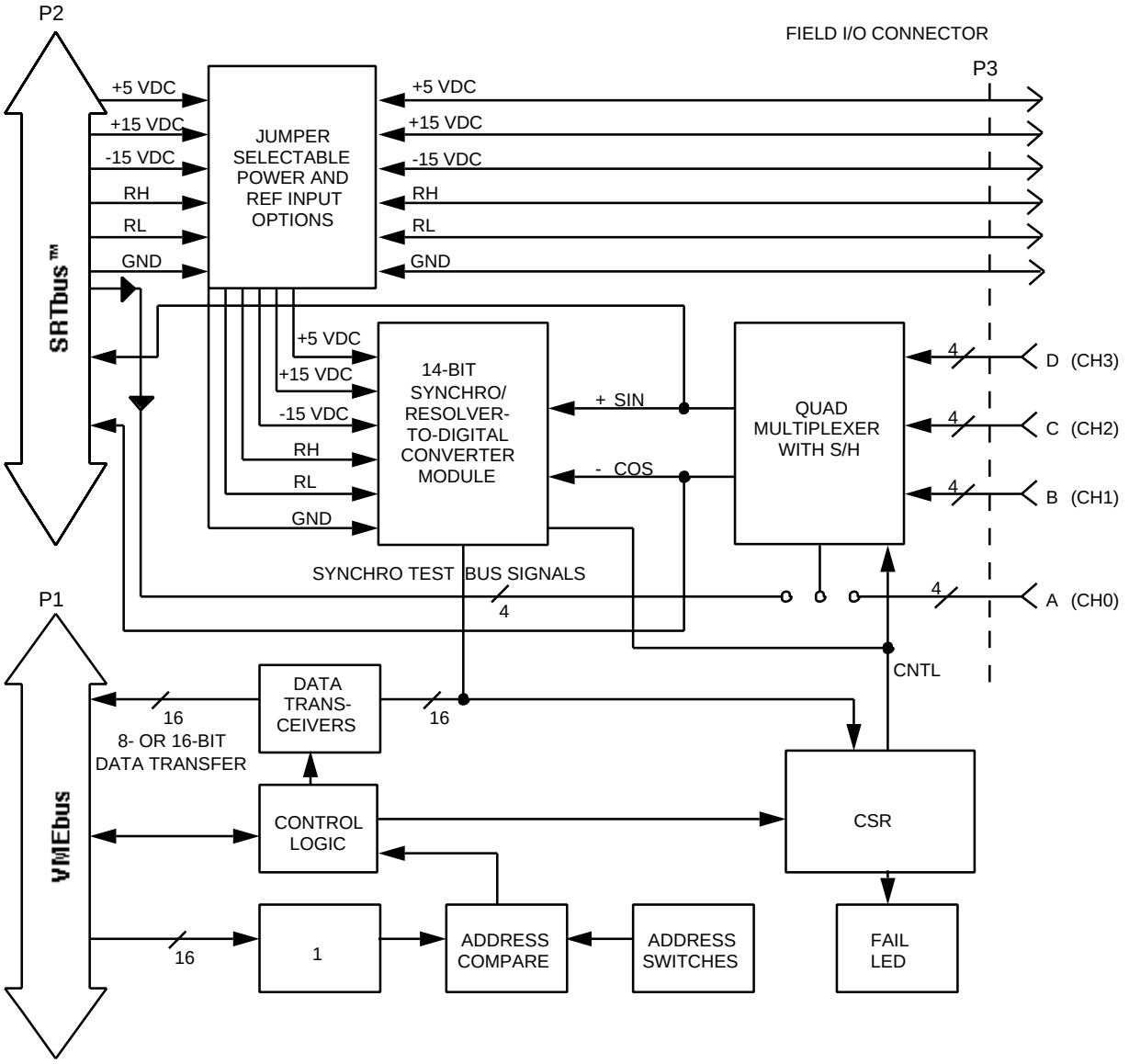

Figure 1 VMIVME-4911 Functional Block Diagram

Reference Material List

For a detailed description of the VMEbus, refer to *The VMEbus Specification and Handbook* available from:

VMEbus International Trade Association (VITA)
7825 Gelding Dr. Suite No. 104
Scottsdale, AZ 85620-3415
(602) 951-8866
Fax: (602) 951-0720
e-mail: info@vita.com
Internet: www.vita.com

Physical Description and Specifications, refer to *Product Specification, 800-004911-000* available from:

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www.vmic.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

Safety Symbols Used in This Manual

STOP: This symbol informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: This sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: This sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER

1

Theory of Operation

Contents

Introduction

The VMIVME-4911 quad channel board utilizes a multiplexed S / D or R / D converter that can be used when multiple synchro or resolver inputs are sampled for digital computation or display. Multiplexing is found in data logging systems, process monitors, ordnance aiming controls, navigation systems, numerical control, and range instrumentation. The synchro and resolver inputs often represent variables which are analyzed by a computer for monitoring or control.

VMEbus Compatibility Logic

Typical VMEbus drivers, receivers and control logic are shown in Figure 1-1 below.

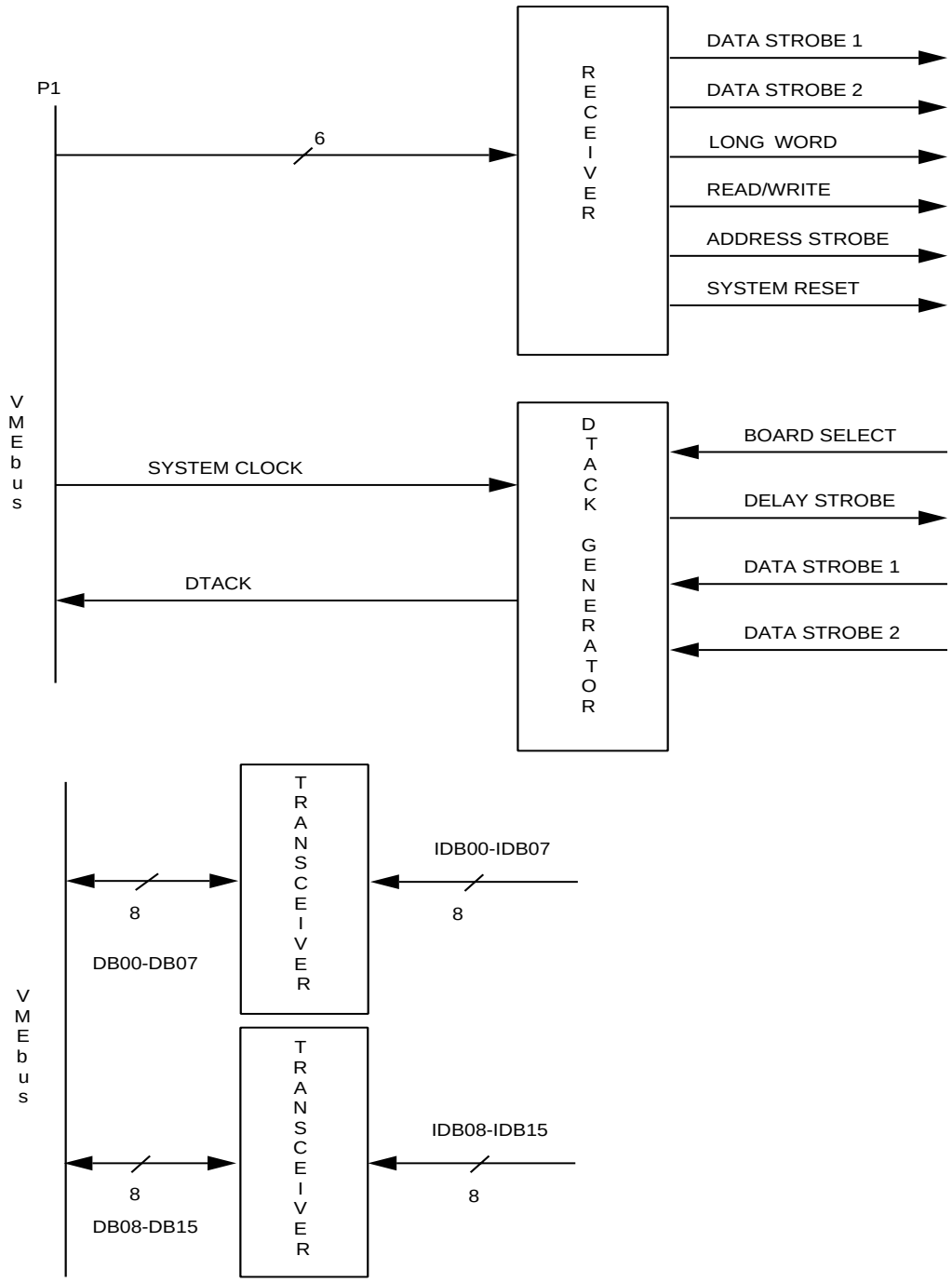


Figure 1-1 VMEbus Compatibility Logic

Data Transceivers

Data transfer transceivers are shown in Figure 1-2 on page 20. The transceivers provide the buffers necessary to support 16-bit data transfers.

Device Addressing

The VMIVME-4911 is designed to support data transfers in supervisory and/or non-privileged short I/O memory space. The board is factory configured via a programmed PAL to respond to either of two address modifier codes: Short Supervisory ($2D) and Short Non-Privileged access ($29).

The VMIVME-4911 is designed with board select switches and decode logic, as shown in Figure 1-2 below, to provide an efficient memory address map for CSR and I/O addresses.

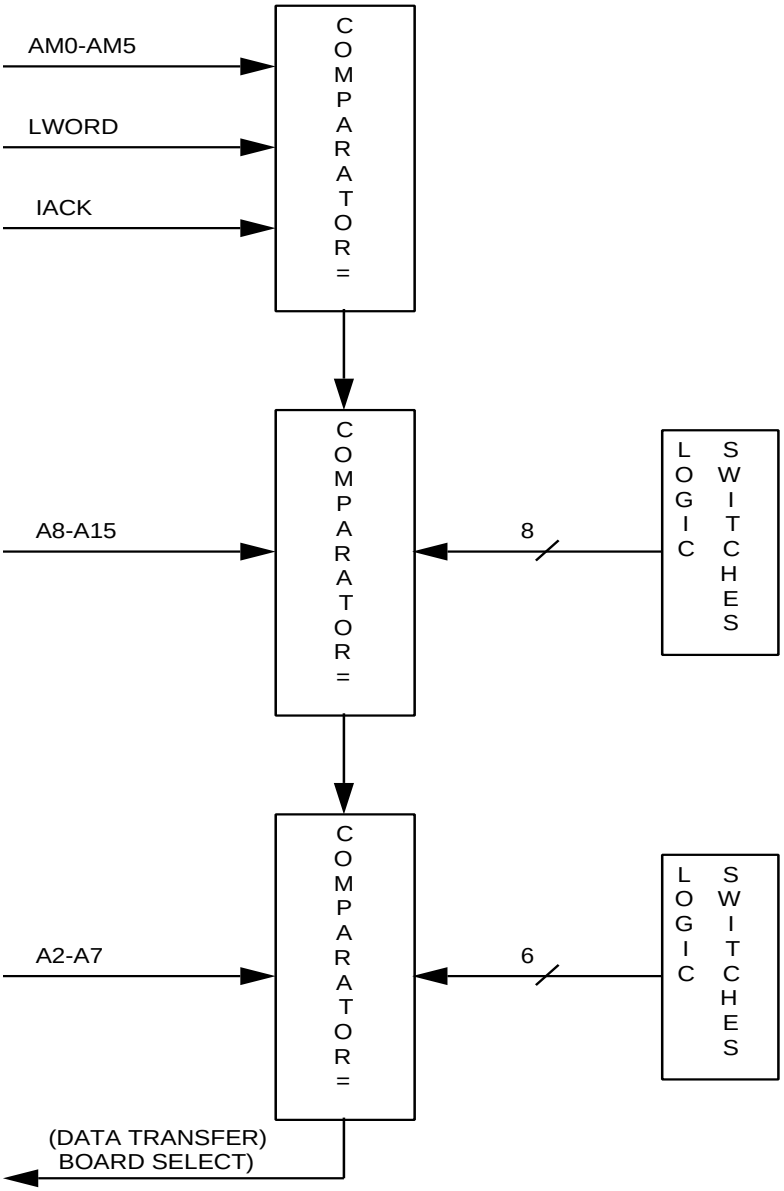


Figure 1-2 Address Compare Subsystem Detailed Block Diagram

Data Input

A data input operation is initiated when a CPU executes an instruction that sends the VMIVME-4911 board an address that selects the board. During the instruction execution, VMEbus control signals cause the board to place a data input word on the VMEbus backplane data lines to be read by the CPU.

Data input words are digital representations of the corresponding user input signal. User input signal changes will result in continuous variations of the input data which represents the user's synchro / resolver shaft position. The input data word is a bit pattern that represents the position of the user's transducer shaft. The associated weighting of each bit is listed in Table 1-1 below.

A simplified functional block diagram of the data input logic is shown in Figure 1-3 on page 22. A data buffer isolates the synchro / resolver data lines from the bidirectional internal data bus (DBXX) which is also used to load data in the control register. The outputs of the control register provide the control for the synchro / resolver module and the front panel Fail LED.

Table 1-1 Data Input Word: Bit Weight

BIT NO. (N)	2^{14-N}	BIT WEIGHT AS % OF FULL SCALE	RADIANS BIT	DEGREES BIT	MINUTES BIT	SECONDS BIT	MILS BIT
13	2.	50.	3.14159265	180	10,800.	648,000.	3,200.
12	4.	25.	1.57079633	90	5,400.	324,000.	1,600.
11	8.	12.5	.78539816	45	2,700.	162,000.	800.
10	16.	6.25	.39269908	22.5	1,350.	81,000.	400.
9	32.	3.125	.19634954	11.25	675.	40,500.	200.
8	64.	1.5625	.09817477	5.625	337.5	20,250.	100.
7	128.	.78125	.04908739	2.8125	168.75	10,125.	50.
6	256.	.390625	.02454369	1.40625	84.375	5,062.5	25.
5	512.	.1953125	.01227185	.703125	42.1875	2,531.25	12.5
4	1,024.	.09765625	.00613592	.3515625	21.09375	1,265.6250	6.25
3	2,048.	.04882813	.00306796	.1757813	10.54688	632.8125	3.125
2	4,096.	.02441406	.00153398	.0878906	5.27344	316.4063	1.5625
1	8,192.	.01220703	.00076699	.0439453	2.63672	158.2031	0.78125
0	16,384.	.00610352	.00038350	.0219727	1.31836	79.1016	0.390625

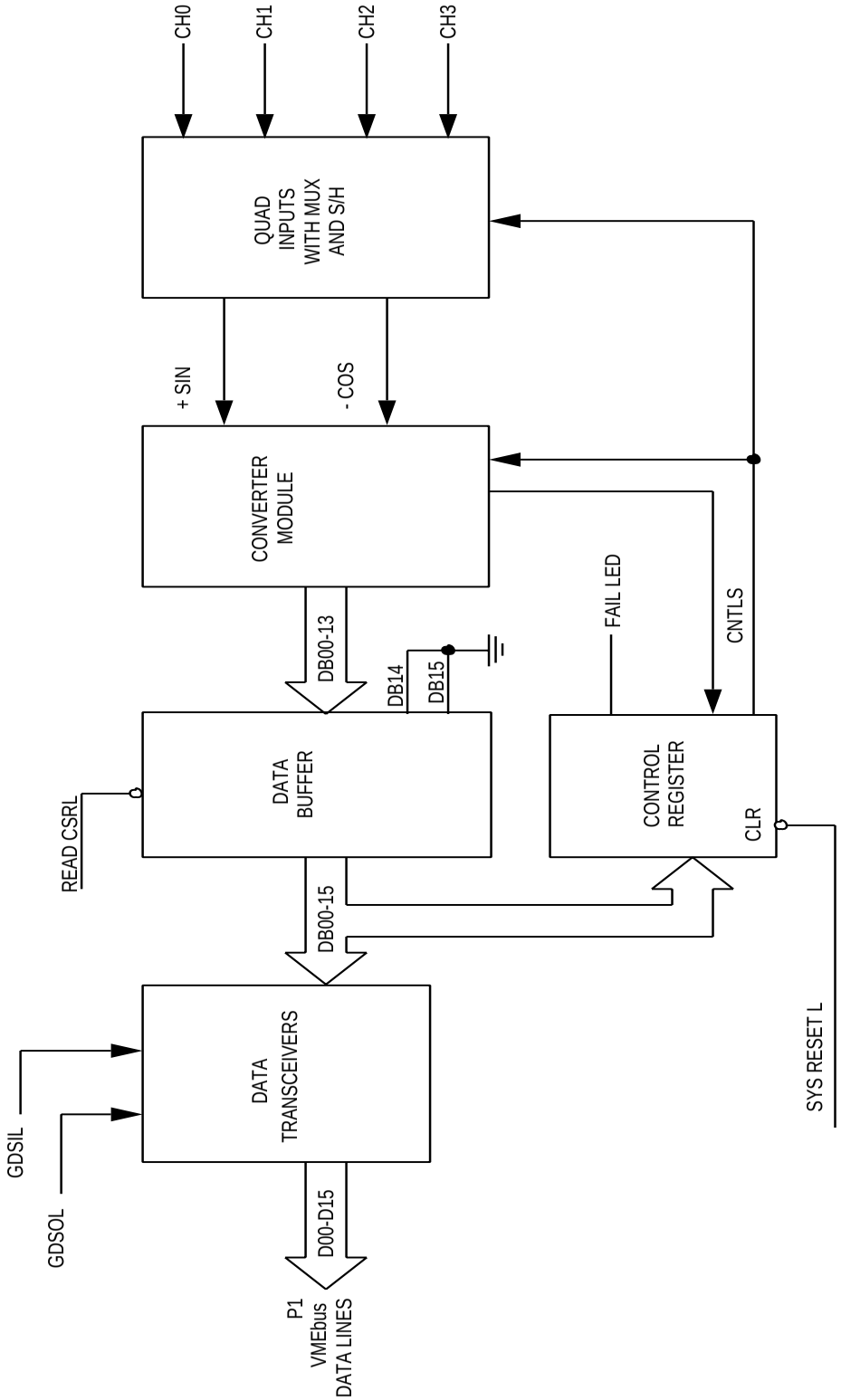


Figure 1-3 Simplified Data Input Block Diagram

Synchro/Resolver Board

Each multiplexed system, as shown in Figure 1-4 on page 24, consists of one converter module and one or more signal input modules. The block diagram shows one input module connected to one converter module. The input module contains four signal input channels A, B, C, D and one reference input channel.

Each synchro or resolver is connected to a separate input channel, and the reference to the reference channel. The input circuit is either a resolver isolation transformer or a Scott-T transformer.

If several synchro or resolvers share a reference, they will also share a reference input channel. The purpose of the reference input channel is to produce the sample time pulse $\overline{ST}$. Each $\overline{ST}$ pulse causes the dual sample/holds to which it is connected to sample the synchro or resolver input in that channel.

The sample enable, SE, inhibits the sample time generator. If the SE is at logic "one", the sample time generator automatically produces an $\overline{ST}$ pulse near each positive peak of the reference waveform. The synchro and resolver inputs connected to each reference are therefore sampled simultaneously once during each cycle, unless an SE pulse is applied The $\overline{ST}$ pulse is inhibited only if the SE is at logic "zero" at the moment the $\overline{ST}$ is initiated; once the $\overline{ST}$ begins, a subsequent SE drop to logic "zero" will not affect the $\overline{ST}$ pulse completion.

The outputs from each signal sample/hold circuit are nominally +4.1 sin Ø sin wt and -4.1 cos Ø sin wt. These signals are sampled by the dual sample/hold at a time close to the positive peaks of the reference waveform. The dual sample/hold outputs are nominally +4.1 sin Ø and -4.1 cos Ø. These outputs are MUXED together to the central converter input. The MUX select lines $\overline{MA}$, $\overline{MB}$, determine which of these outputs will be processed. The MUX shorting switches are operated automatically by the converter busy pulse to discharge the central converter MUXED input lines between conversions.

The SIN/COS (S/C) select was designed for situations in which the output from a signal module is processed not by a converter module, but by some other means such as a computer. By operating the S/C control, the sin Ø and cos Ø information can be MUXED into one output line.

The -85° nominal phase shifter and the zero crossing detector in the reference channel detect the peak of the reference waveform. The 5° shift away from 90° compensates for a lead of approximately this amount which normally occurs between the signal output and reference input of a synchro or resolver.

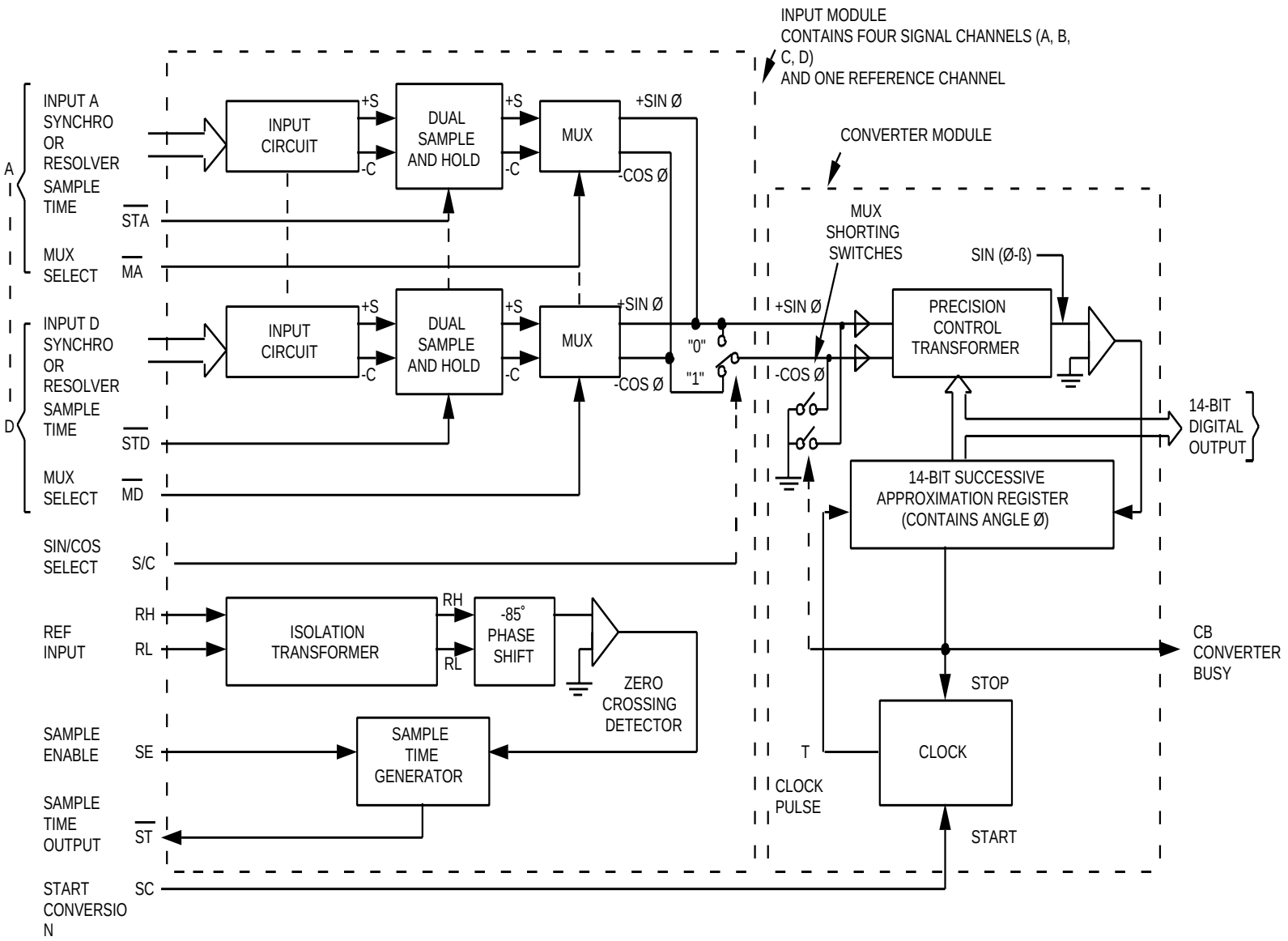


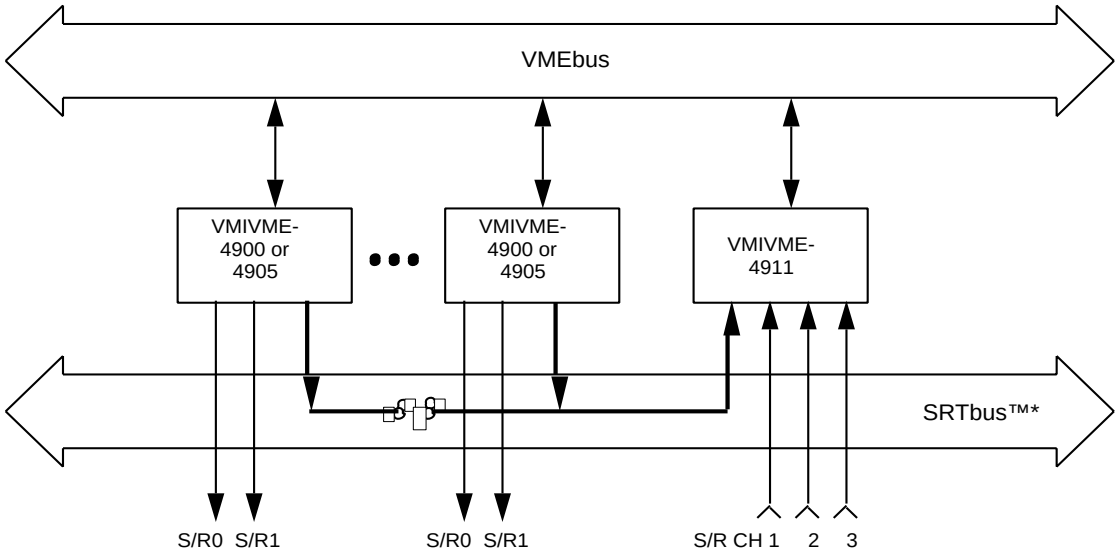
Figure 1-4 VMIVME-4911 Synchro/Resolver-to-Digital Converter Modules

Built-In-Test (BIT)

The VMIVME-4911 is designed such that Channel A may be jumpered to the P2 backplane such that the board can be loop-tested via VMIC's SRTbus™ and Digital-to-Synchro Converter Boards, as shown in Figure 1-5 below. This concept provides the user with the capability to design systems with off-line and on-line fault detection and isolation. The reader should refer to VMIC's Synchro / Resolver Subsystem Configuration Guide (Document No. 825-000000-004) for a thorough explanation of synchro / resolver Built-in-Test concepts.

The synchro / resolver input jumper option seen in Figure 1-6 on page 26 implements the two modes of operation for Channel A. With synchro / resolver input connected to the P3 I / O connector, the VMIVME-4911 lends itself to receive synchro / resolver inputs from the front panel of the board via a 25-pin AMP connector, No. 206584-1.

The user can also elect to receive Channel A synchro / resolver inputs from the VMIC synchro / resolver backplane via the P2 connector. This configuration lends itself for use with a Digital-to-Synchro / Resolver Converter Board, such as the VMIVME-4900, for test purposes or the user could supply field inputs directly to the P2 connector instead of using the P3 I / O connector (refer to Figure 1-5 below).



SRTbus™ is a trademark of VMIC.

Figure 1-5 Typical Subsystem Configuration for Testing VMIC's VMIVME-4900 and 4905 Synchro/Resolver Output Boards

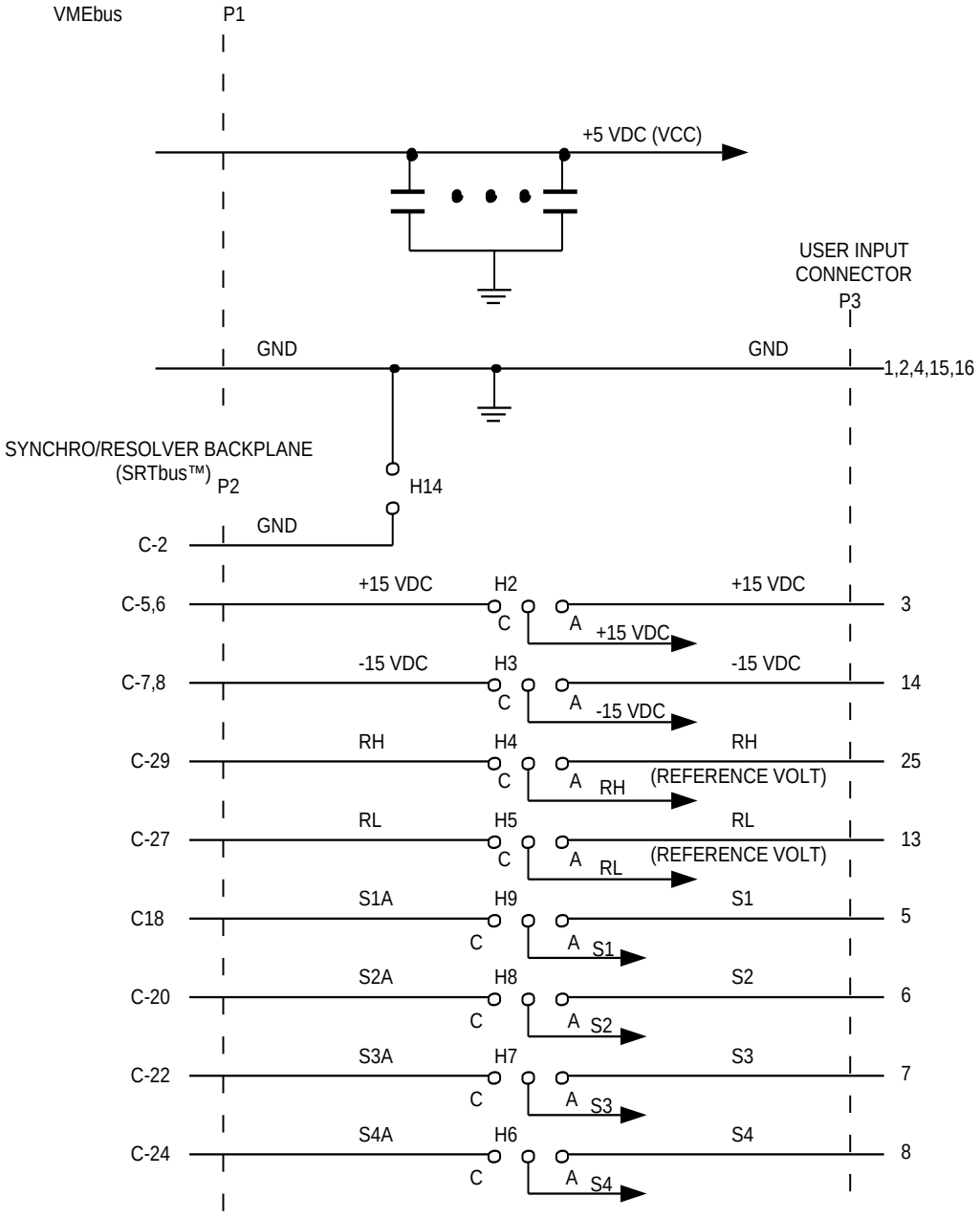


Figure 1-6 VMIVME-4911 Power Subsystem Block Diagram

Reference Input

This input is a user-supplied voltage that is chosen by the user. The available reference input voltage and the line-to-line voltage (V_{L-L}) for the reference input is listed in the product specification, document number 800-004911-000. For further information on the reference voltage input characteristics (voltage and impedance) refer to the Analog Input Characteristics section of the product specification.

CHAPTER
2

Configuration and Installation

Contents

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

CAUTION: Do not install or remove the board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated.

WARNING: Application of reverse polarity to any one of the three power supply inputs will cause catastrophic failure.

Jumper and Switch Locations

Refer to Figure 2-1 on page 32 for the locations of the jumper and switches described in this section.

Address Modifiers

The board is factory configured via a programmed PAL to respond to either of two address modifier codes: Short supervisory ($2D) and short non-privileged access ($29), or both, depending upon the option chosen.

Jumper Installation

Jumpers are provided to connect ± 15 V, RH, RL, and input channels from the front panel (P3) or the P2 connector (Jumpers H2 to H9). Jumpers are also provided for Multiplexer expansion cards (Jumpers H10 to H13 and H1). See Table 2-1 on page 36 for Jumper Configuration.

Address Selection Switches

The VMIVME-4911 uses four bytes of the VMEbus, short I/O address space. The upper 14 bits of the short address are Dual-in-Line Package (DIP) switch selectable. The addressing DIP switch and its use in the addressing scheme are shown in Figure 2-2 on page 33

X- Immaterial Switch Position

OFF = 1

ON = 0

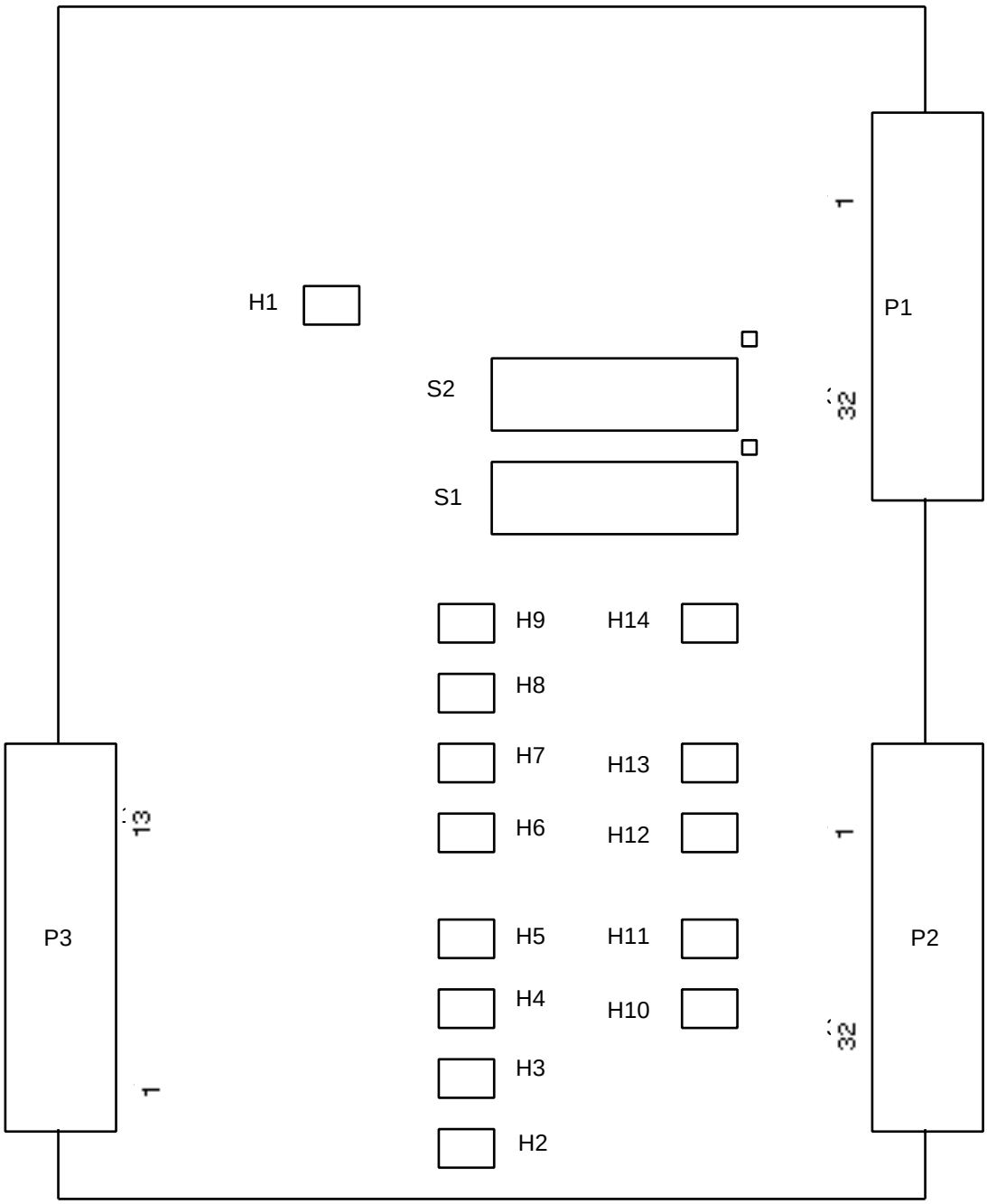


Figure 2-1 Location of Jumpers and Switches

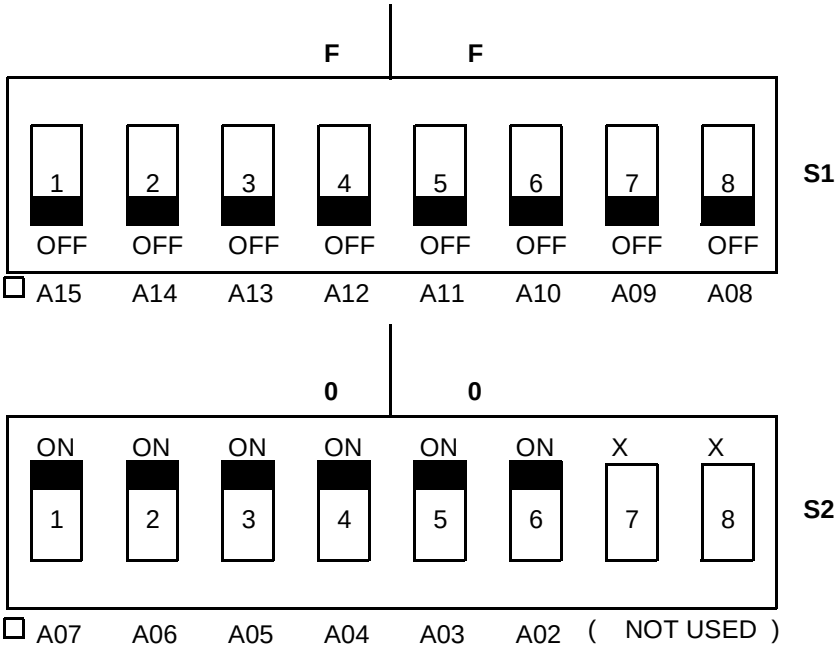


Figure 2-2 Address Select Switches

Example 1:

For the VMIVME-4911 to respond to an address base of $FF00_{16}$, the S1 and S2 switches would be set as shown in Figure 2-2 above.

Connectors

The VMIVME-4911 provides a choice of two sources of inputs on channel A, selectable by jumpers H6, H7, H8, and H9. One input selection uses the P2 connector and operates through the VMIC Synchro / Resolver Backplane. The other source uses the P3 front panel connector (AMP No. 206584-1). A compatible type D cable connector and strain relief kit is the AMP No. 747322-2. The reader should refer to Figure 2-3 on page 35, Table 2-1 and Table 2-2 on page 37 for signal input selection.

User Input Cables

VMIC recommends the use of shielded, insulated cable, triple-twisted (12 turns per foot) to avoid error inducing conditions at the data and reference inputs.

Front Panel Input Connector P3

The reader should refer to Table 2-3 on page 38 for pin assignments for the front panel user inputs.

VMEbus P2 Connector Pin Assignments

Connector P2, the VMEbus backplane connector may be used for power input, reference input and signal inputs. Connector P2 pin layout is shown in Figure 2-4 on page 39. P2 connector pin assignments are shown in Table 2-4 on page 40.

Reference Input

This input is user selected by option number and applied to the board via P2 and P3 (see Table 2-3 on page 38 and the Theory of Operation).

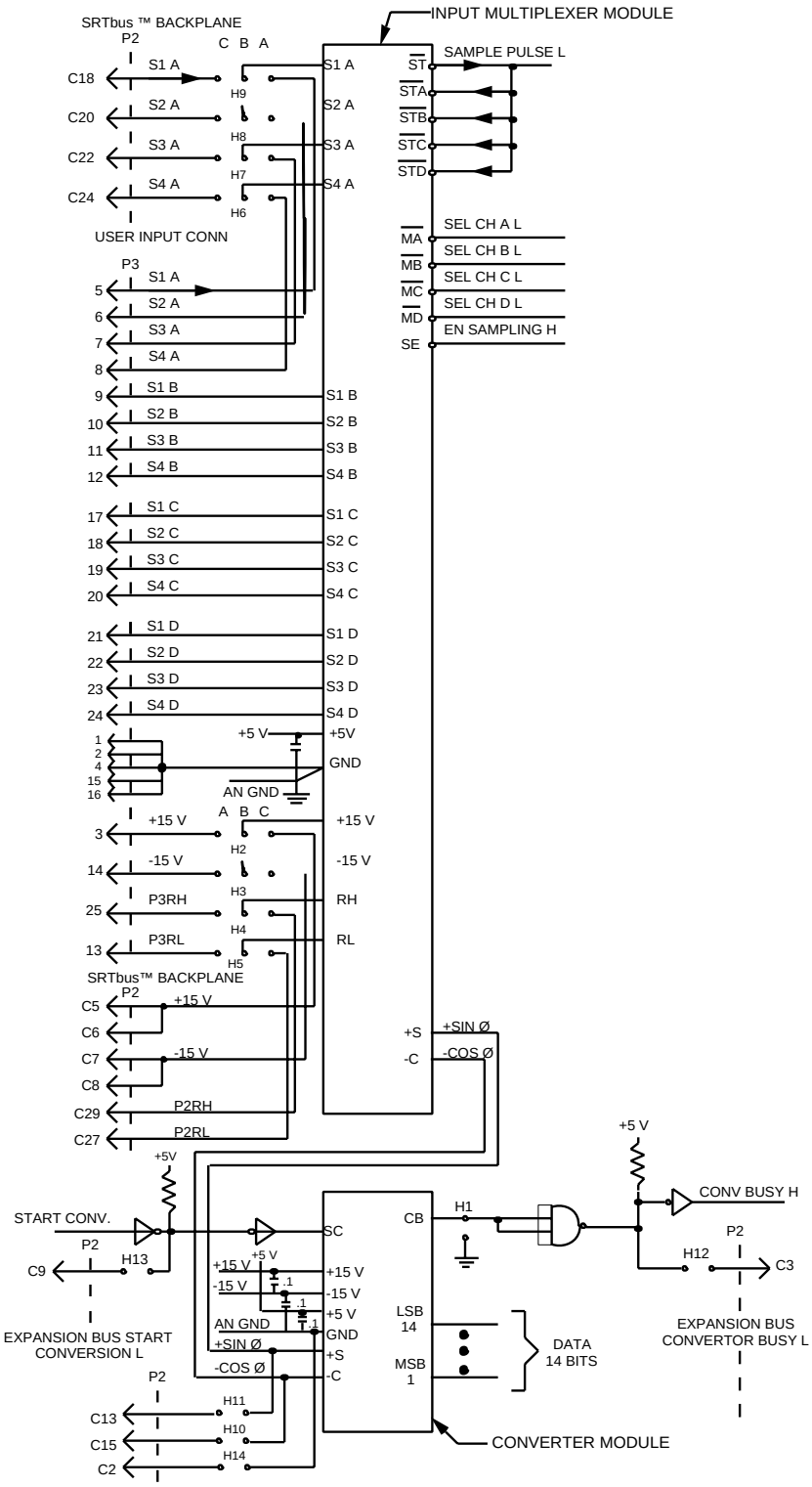


Figure 2-3 Typical Input Configuration

Table 2-1 Jumper Configuration

FUNCTION	JUMPER INSTALLATION
This jumper should be removed on all boards with converter modules installed. Factory configured.	H1
Disables Converter Busy Factory Configured for Board without converter modules.	 H1
+ 15 V from P3 connector	 H2
+ 15 V from P2 connector	 H2
- 15 V from P3 connector	 H3
- 15 V from P2 connector	 H3
RH from P3 connector	 H4
RH from P2 connector	 H4
RL from P3 connector	 H5
RL from P2 connector	 H5
Channel A input S4 from P3	 H6
Channel A input S4 from P2	 H6

Table 2-2 Jumper Configuration Continued

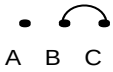
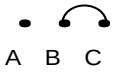
FUNCTION	JUMPER INSTALLATION
Channel A input S3 from P3 Channel A input S3 from P2	 H7  H7
Channel A input S2 from P3 Channel A input S2 from P2	 H8  H8
Channel A input S1 from P3 Channel A input S1 from P2	 H9  H9
Connects -cos 0 to P2 backplane for Multiplexer use	 H10
Disconnects -cos 0 from P2 backplane	H10
Connects +sin 0 to P2 backplane for Multiplexer use	 H11
Disconnects +sin 0 from P2 backplane	H11
Connects Converter Busy to P2 backplane	 H12
Disconnects Converter Busy from P2 backplane	H12
Connects Bus Start Convert to P2 backplane	 H13
Disconnects Bus Start Convert from P2 backplane	H13
Connects Analog GND to P2 backplane	 H14
Disconnects Analog GND to P2 backplane	H14

Table 2-3 P3 Connector Pin Assignments

CONNECTOR	PIN	SIGNAL	
P3	5	S1A	CHANNEL 0 INPUT (A)
P3	6	S2A	
P3	7	S3A	
P3	8	S4A	
P3	9	S1B	CHANNEL 1 INPUT (B)
P3	10	S2B	
P3	11	S3B	
P3	12	S4B	
P3	17	S1C	CHANNEL 2 INPUT (C)
P3	18	S2C	
P3	19	S3C	
P3	20	S4C	
P3	21	S1D	CHANNEL 3 INPUT (D)
P3	22	S2D	
P3	23	S3D	
P3	24	S4D	
P3	25	RH	REFERENCE INPUT
P3	13	RL	
P3	3	+15 V	
P3	14	-15 V	
P3	1	GND	
P3	2	GND	
P3	4	GND	
P3	15	GND	
P3	16	GND	

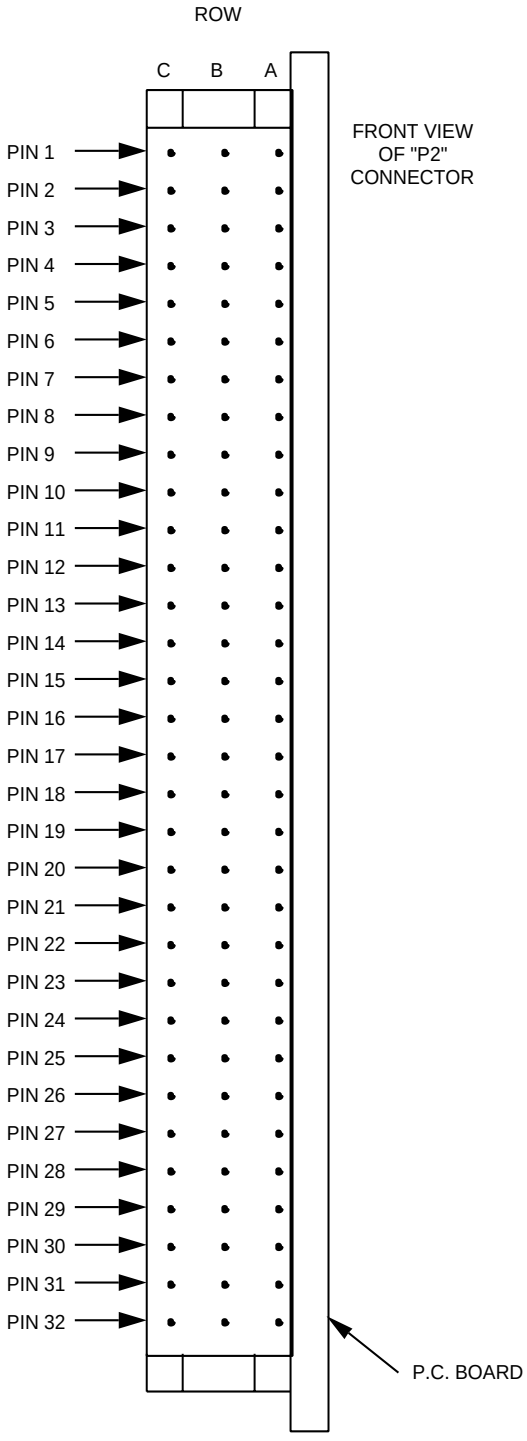


Figure 2-4 P2 Connector - Pin Layout

Table 2-4 P2 Connector Pin Assignments

ROW A	ROW B	PIN NO.	ROW C
	+5 V (B1)	1	
	GND (B2)	2	AN GND (C2)
		3	CONV BUSY L (C3)
		4	
		5	+15 V (C5)
		6	+15 V (C6)
		7	-15 V (C7)
		8	-15 V (C8)
		9	BUSY START CONV L (C11)
		10	
		11	
	GND (B12)	12	
	+5 V (B13)	13	+SIN Ø (C13)
		14	
		15	-COS Ø (C15)
		16	
		17	
		18	S1A (C18)
		19	
		20	S2A (C20)
		21	
	GND (B22)	22	S3A (C22)
		23	
		24	S4A (C24)
		25	
		26	
		27	RL (C27)
		28	
		29	RH (C29)
		30	
	GND (B31)	31	
	+5 V (B32)	32	

CHAPTER 3

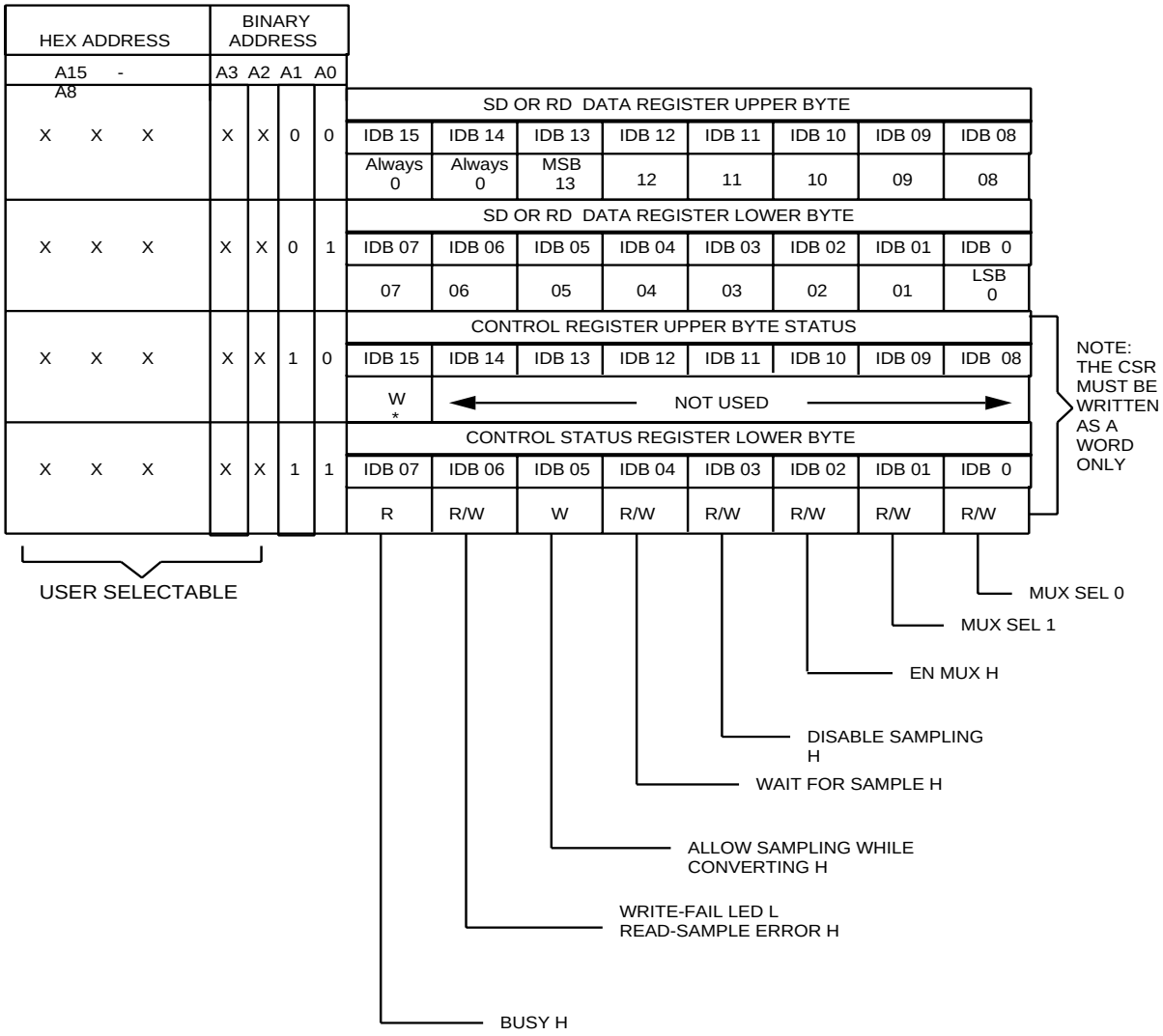
Programming

Contents

Introduction

The VMIVME-4911 accepts either 3-wire synchro or 4-wire resolver input data over a frequency range of 47 to 440 Hz. The VMIVME-4911 is a multiplexed sampling converter that continuously converts analog synchro (or resolver) input data into binary digital angle data. The binary digital data are digital representations of the corresponding position of the user's transducer shaft.

The VMIVME-4911 compares 14 of the 16 address bits (Bits A15 to A02) to the selected board address. The desired address of the board is selected with switches S1 and S2, as shown in Section 5. Address bit A01 is used to select between the Input Data Register (IDR) and the Control Status Register (CSR). The address map and register bit definitions are described in Figure 3-1 on page 42.



*Start conversion H.

Figure 3-1 Address Map and Register Bit Definitions

Control and Status Register (CSR)

The Control Status Register (CSR) is a *read/write* register that controls the input channel multiplexing, sampling, multiplexer enable, front panel Fail LED, and that provides status such as conversion complete (busy) and sample error. The format of the CSR is shown in Table 3-1 below. The CSR bit definitions are provided in Table 3-2 below. The front panel Fail LED is illuminated at power-up (system reset) and is extinguished under program control.

Table 3-1 CSR Format

15	14	13	12	11	10	09	08
START CONV H	← NOT USED →						
W	← N/A →						

NOTE: THE CSR MUST BE WRITTEN AS A WORD ONLY.

07	06	05	04	03	02	01	00
BUSY H	* FAIL LED L SAMPLE ERR H	ALLOW SAMPLING WHILE CONVERTING H	WAIT FOR SAMPLE H	DISABLE SAMPLING H	EN MUX H	MUX SEL 1	MUX SEL 0
R	R/W *	R/W	R/W	R/W	R/W	R/W	R/W

*Bit 06 is written as FAIL LED on LOW and read as SAMPLE ERR on HIGH.

Table 3-2 CSR Bit Definitions

Channel selected vs CSR bits 0 and 1.

BIT 1	BIT 0	CHANNEL SELECTED
0	0	A
0	1	B
1	0	C
1	1	D

BIT00 - MUX SEL 0. Bits 0 and 1 are used to select the synchro / resolver channel inputs.

BIT 01 - MUX SEL 1. Bits 0 and 1 are used to select the synchro / resolver channel inputs.

BIT 02 - EN MUX H. Enables the input multiplexer module on this board (when set to "one").

BIT 03 - DISABLE SAMPLING H. Disables further sampling of channel inputs. After the synchro / resolver inputs have been sampled, it may be desirable to suspend further sampling until all inputs have been converted. However, due to the gradual decay (droop) of the sample / hold circuits, all channels should be converted as soon as practical after sampling is completed (within one time period of the reference frequency). Set to logic "one" to disable sampling.

BIT 04 - WAIT FOR SAMPLE PULSE H. When set, this bit prevents conversion of synchro / resolver data until a new sample is taken. This bit should be set if the synchro / resolver inputs have changed and the new angle is to be read. The start bit can be set simultaneously with this bit.

BIT 05 - ALLOW SAMPLING WHILE CONVERTING H. When set, this bit causes the synchro / resolver inputs to be sampled continuously at every peak, even while conversion is taking place, resulting in a small error. It is recommended that this bit be cleared (to "zero") to inhibit sampling while the master converter is busy (150 µs per conversion).

BIT 06 - WRITTEN AS FAIL LED ON LOW. When cleared, this bit turns the Fail LED ON. This bit is cleared by the VMEbus SYSRESET L signal. After diagnostics are successfully completed, this bit should be set to "one" to turn the Fail LED OFF.

BIT 06 - READ AS SAMPLE ERR ON HIGH. This status bit is set if sampling of the synchro / resolver input occurs while a conversion is taking place. Sampling is inhibited during the conversion cycle unless the CONTINUOUS SAMPLING bit (bit 05) is set, therefore, this bit will never be set unless CONTINUOUS SAMPLING is enabled. This bit is automatically cleared at the start of each conversion.

BIT 07 - BUSY H (READ ONLY). This status bit indicates that a conversion sequence is in progress. This bit goes to "one" as soon as the START bit (bit 15) is set and it remains set until the conversion is complete and the synchro / resolver angle data is valid.

BITS 08 - 14 - NOT USED.

BIT 15 - START CONV H (WRITE ONLY). When set, this bit initiates a conversion cycle and immediately sets busy (Status Bit 07) to "one". If the synchro / resolver input is being sampled when this bit is set, conversion of the sampled signal will not start until the end of the sample pulse. This bit is automatically cleared when conversion is actually started.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.