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VMIVME-4941

QUAD-CHANNEL RESOLVER-TO-DIGITAL CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-004941-000 N

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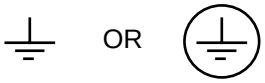
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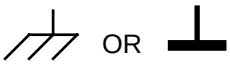
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



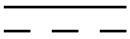
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



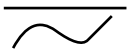
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

```
**************
*  CAUTION   *
**************
```

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

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VMIVME-4941
QUAD-CHANNEL RESOLVER TO DIGITAL CONVERTER BOARD

TABLE OF CONTENTS

Page

SECTION 1. INTRODUCTION

1.1 INTRODUCTION 1-1
1.2 FUNCTIONAL DESCRIPTION 1-1
1.3 REFERENCE MATERIAL....1-2

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. THEORY OF OPERATION

3.1 BLOCK DIAGRAMS 3-1
3.2 GENERAL DESCRIPTION....3-1
3.3 VMEbus FOUNDATION LOGIC 3-1
3.4 RESOLVER CONVERTER MODULES....3-4
3.4.1 Introduction....3-4
3.4.2 Digital Interface....3-6
3.4.3 Solid State Differential Input Option....3-6
3.4.4 Direct Input Option....3-6
3.4.5 Logic Input/Output 3-6
3.4.6 Dynamic Performance 3-7
3.4.7 Built-in-Test (Internal to the Converter)....3-7
3.5 BUILT-IN-TEST (ON-BOARD)....3-7
3.6 PITCH COUNTER OPERATION 3-8

SECTION 4. PROGRAMMING

4.1 REGISTER MAP....4-1
4.2 PITCH COUNTER(S)/REGISTER(S) 4-1
4.3 RESOLVER-TO-DIGITAL CONVERTER DATA REGISTER....4-1
4.4 CONTROL AND STATUS REGISTER (CSR) 4-7
4.4.1 Built-in-Test Programming 4-8
4.4.2 Fail LED Control 4-8
4.4.3 R/D Converter Resolution Control 4-8
4.4.4 R/D Converter Bandwidth Control 4-11

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TABLE OF CONTENTS (Continued)

Page

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 JUMPER AND SWITCH LOCATIONS.....5-1
5.4 ADDRESS MODIFIERS 5-3
5.5 ADDRESS SELECTION SWITCHES 5-3
5.6 EXTERNAL POWER SELECTION.....5-3
5.7 REFERENCE VOLTAGE INPUTS.....5-4
5.8 COUNTER DIRECTION JUMPERS 5-6
5.9 JUMPERING FOR DIRECT vs DIFFERENTIAL SIGNAL INPUTS....5-6
5.9.1 Direct Input Option.....5-6
5.9.2 Differential Input Option.....5-6
5.10 Cabling Requirements 5-9

SECTION 6. MAINTENANCE

6.1 MAINTENANCE.....6-1
6.2 MAINTENANCE PRINTS.....6-1

LIST OF FIGURES

Figure Page

3.1-1 Functional Block Diagram.....3-2
3.2-1 Input Configuration Software Control.....3-3
3.4.1-1 Resolver-to-Digital Converter Module Typical 1 of 4 3-5
3.6-1 Pitch Counter Logic Functional Block Diagram.....3-9
4.1-1 Register Map for Word Addressing.....4-5
4.1-2 Register Map for Longword Addressing 4-6
5.3-1 Location of Jumpers and Switches 5-2
5.5-1 Address Selection Switch Example (Address 0000) and Address Modifier Switch Example (Short Supervisory Access) 5-3
5.6-1 Jumper Installation to Select ±15 V Inputs via the P3 Connector.....5-4
5.6-2 Jumper Installation to Select ±15 V Inputs via the P2 (Backplane) Connector 5-4
5.7-1 Jumper Installation to Select the Reference Voltage Input at P3 for All Four Channels 5-5

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TABLE OF CONTENTS (Concluded)

LIST OF FIGURES (Concluded)

Figure		Page
5.7-2	Jumper Installation to Select a Single Reference Voltage Signal from P2 (Pins C29 and C27) for All Four Channels	5-5
5.7-3	Jumper Installation to Select a Separate Reference Voltage Signal for each Channel via the P2 Connector	5-6
5.9.1-1	Jumper Configuration for the Direct Signal Input Option (2 Volt), this Configuration Connects S1 to S4 on Each Resolver Input Channel	5-9
5.9.2-1	Jumper Installation to Select Single-Ended R/D Converter Inputs (11.8 V Option Only), These Jumpers Connect a Ground to the S1 and S4 Inputs for All Four Channels	5-9
5.10-1	Recommended Connection of Resolver Reference Voltage and Signals	5-10

LIST OF TABLES

Table		Page
4.1-1	Address Register Map	4-2
4.1-2	Address and Register Bit Definitions	4-3
4.3-1	Resolver-to-Digital Converter Data Register and Bit-Weight Table	4-7
4.4-1	CSR HI Byte Bit Map ($XX10)	4-9
4.4-2	CSR M-HI Byte Bit Map ($XX11)	4-9
4.4-3	CSR M-LO Byte Bit Map ($XX12)	4-9
4.4-4	CSR LO Byte Bit Map ($XX13)	4-9
4.4.1-1	CSR Relay Control Functions	4-10
5.8-1	Jumper Installations for Counting Up When R/D Data is Increasing	5-7
5.8-2	Jumper Installations for Counting Down When R/D is Increasing	5-8
5.10-1	P2 and P3 Connector Pinouts	5-11

APPENDIX

A Assembly Drawing, Parts List, and Schematics

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-4941 is a VMEbus compatible Quad Channel Resolver-to-Digital Converter Board. Its features include:

a. Quad R/D converters
b. Tracking rates up to 800 rps minimum (48,000 RPM)
c. Software programmable resolution (10-, 12-, 14- or 16-bit)
d. Software programmable bandwidth (530 Hz, 130 Hz)
e. 16 bit pitch counter per channel
f. 8, 16, or 32 bit data transfers
g. Reference frequency from 360 Hz (Lo Bandwidth) to 6 k Hz
h. Status indications for loss of signal and tracking error over 65 bits
i. Accuracy to ±2.3 ARC minutes available (optional)
j. Double Eurocard form factor
k. Built-in-test capability with loss of signal and level of error fail LEDs

1.2 FUNCTIONAL DESCRIPTION

The Quad Channel Resolver-to-Digital Converter Board consists of VMEbus compatibility logic, four resolver-to-digital converters, four 16-bit pitch counters, and logic to support fault isolation to the channel level using a resolver test signal that must be supplied via the P2 backplane user I/O pins.

VMEbus compatibility logic controls data transfers to the on-board registers allowing 8-, 16-, or 32-bit transfers. The compatibility logic also contains address decoding enabling the board to be addressed within the short I/O address space.

Four independent R/D converters provide the user with the capability to convert four resolver input channels. The R/D converters feature programmable resolution and bandwidth. The resolution selection provides the user with the capability of programming 10, 12, 14, or 16 bits.

The resolver board is designed for use in modern, high performance commercial and industrial control systems applications including motor control, radar, antenna position information, CNC machine tooling, robot axis control, and process control.

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1.3 REFERENCE MATERIAL

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004941-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

The Quad Resolver Input Board design may be partitioned into five primary functional blocks (refer to Figure 3.1-1):

a. VMEbus foundation logic
b. Register selection and control
c. Test control logic
d. Resolver converters
e. Pitch counters and control logic

3.2 GENERAL DESCRIPTION

The VMIVME-4941 is designed for use in modern high performance commercial and industrial control systems. Applications include motor control, radar antenna position information, CNC machine tooling, robot axis control, and process control.

The VMIVME-4941 utilizes four versatile state-of-the-art resolver to digital converters featuring programmable resolution and bandwidth. Resolution programming allows selection of 10, 12, 14 or 16 bit and options are available with accuracy to 2 minutes +1LSB (+4LSB Diff Lin.). Resolution programming combines the high tracking rate of 10 bit converters with the precision of 16 bit converters.

The Quad Resolver-To-Digital Converter Board is designed with test capability for operational verification of all resolver hybrid converter modules and the VMEbus control logic. The user may provide an input test signal via the P2 VMEbus expansion connector for board testing. A front panel fail LED is illuminated at power-up and may be extinguished via program control after diagnostics are successfully executed. Front panel status indicators are also provided to indicate a loss of signal and level of error faults.

3.3 VMEbus FOUNDATION LOGIC

The VMEbus foundation logic is designed to support the standard data, address, and control signal buffering. The data transfer logic supports long word transfers to provide the user with the capability of reading an R/D converter and its

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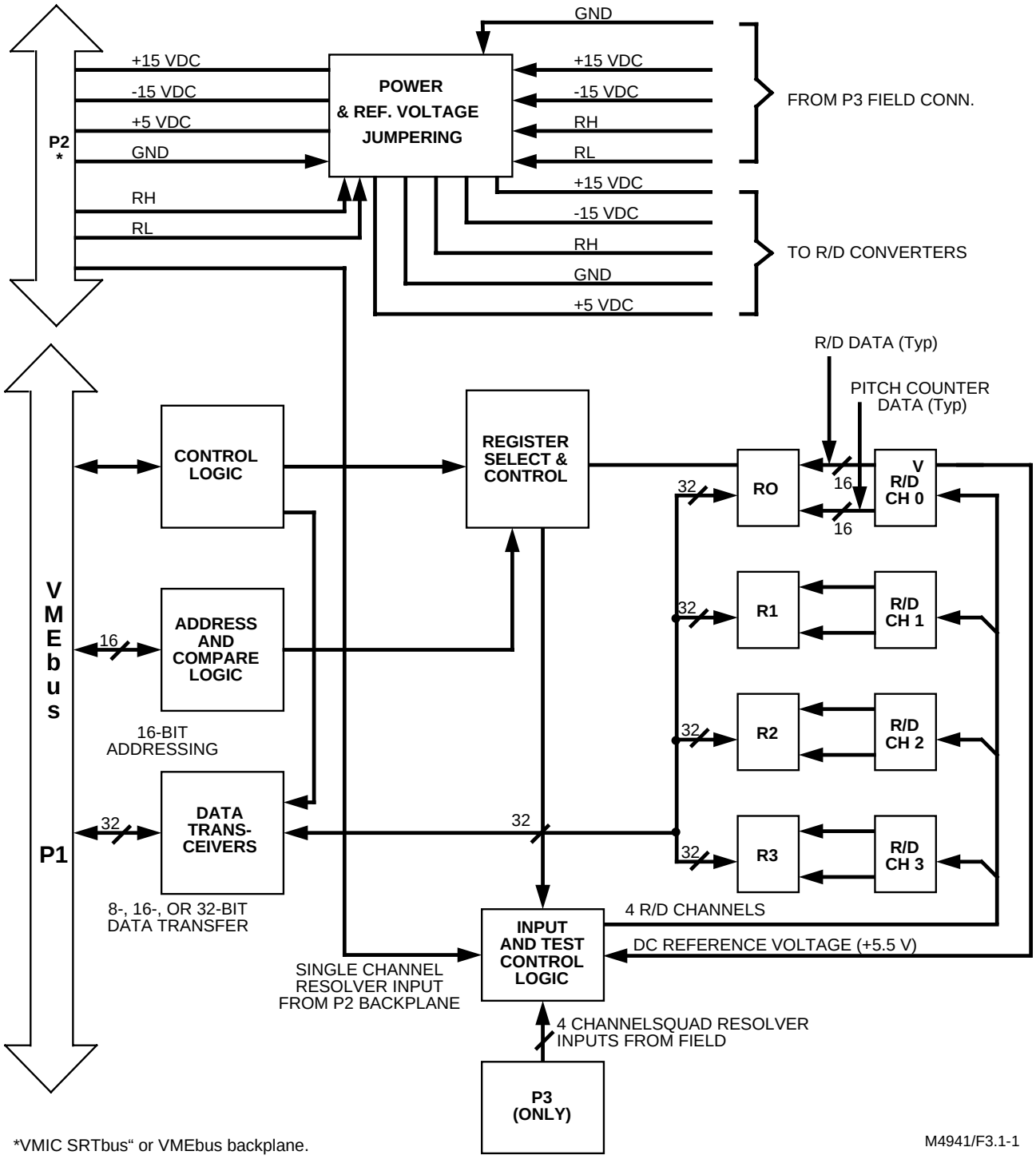


Figure 3.1-1. Functional Block Diagram

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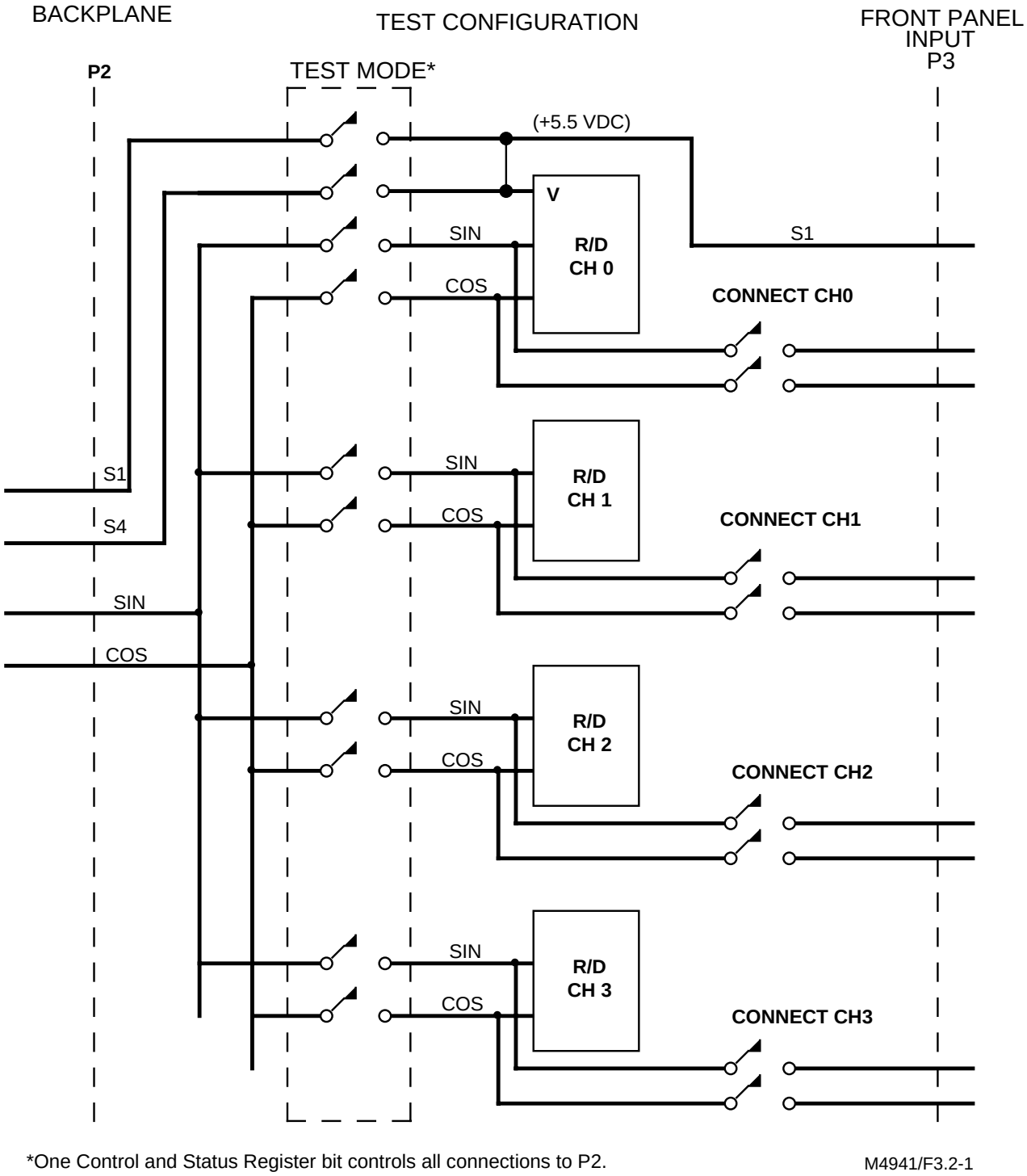


Figure 3.2-1. Input Configuration Software Control

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associated 16 bit pitch counter with one transfer cycle. The data transfer logic also supports 8 and 16 bit transfers.

3.4 RESOLVER CONVERTER MODULES

The four resolver-to-digital converter modules utilized are the ILC Data Device Corporation RDC-19200 MONOBRID Series modules. The RDC-19200 Series Converters are versatile state-of-the-art resolver to digital converters featuring programmable functions such as: resolution, bandwidth, and a scalable velocity output voltage. Resolution programming allows selection of 10-, 12-, 14-, or 16-bit. Models are available with accuracy to ±2 minute +1 LSB. Resolution programming combines the high tracking rate of a 10-bit converter with the precision of a 16-bit device in one module.

3.4.1 Introduction

The RDC-19200, includes three main parts: the signal input; a feedback loop whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and digital interface circuitry including various latches and buffers. Either 11.8 V or 2 V resolver inputs are offered with the RDC-19200 series. The 11.8 V input is differentially coupled and the 2 V input is direct coupled. The 2 V option eliminates the need for an input scaling network and allows operation with a lower reference voltage. Figure 3.4.1-1 shows a typical DDC-19200 used on the VMIVME-4941.

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, sin Ωcoswt and cosΩcoswt. The feedback loop produces a digital angle 0 which tracks the analog input angle • to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\Omega - 0) = \sin\Omega \cos 0 - \cos\Omega \sin 0$$

Where Ω is the angle representing the resolver shaft position, and 0 is the digital angle contained in the up/down counter. The tracking process consists of continually adjusting 0 to make (Ω-0) equal to zero, so that 0 will represent the shaft position •. The output of the demodulator is an analog DC level proportional to sin (Ω•-0). The error processor receives its input from the demodulator and integrates this sin(•-0) error signal which then drives a Voltage Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes d0/dt equal to

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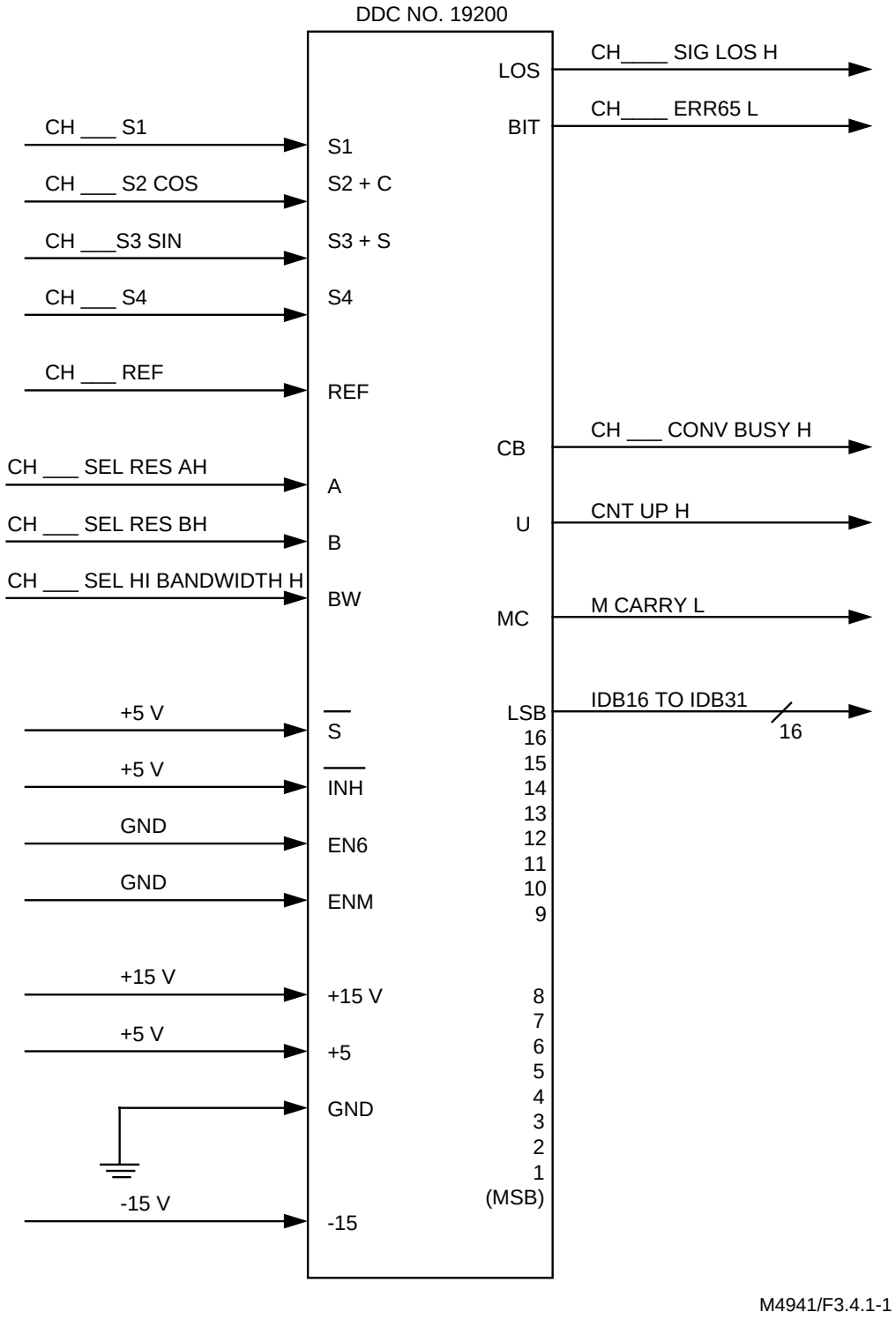


Figure 3.4.1-1. Resolver-to-Digital Converter Module Typical 1 of 4

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dΩ/dt without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The converter automatically zero-sets all of the internal op amps twice per carrier cycle near the zero crossings of the reference. This contributes to the converter's superior dynamic performance.

3.4.2 Digital Interface

The digital interface circuitry has three main functions: to latch the output bits so that stable data can be read out; to furnish parallel, three-state data formats; and to act as a buffer between the internal CMOS logic and the external TTL logic.

3.4.3 Solid State Differential Input Option

This option provides signal and reference inputs that are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off. The maximum transient peak voltage should not exceed 100 volts.

3.4.4 Direct Input Option

The direct input option provides for 2 Vrms resolver inputs. A 2 V input from a resolver means that the reference voltage can be less than that of an 11.8 V resolver, thus lowering the cost and power of the reference oscillator. However, operation at a lower level makes the input more noise sensitive.

3.4.5 Logic Input/Output

The digital angle output consists of 10, 12, 14, or 16 parallel data bits and a CONVERTER BUSY (CB) signal. All logic outputs are short-circuit proof to ground and +5 volts. The CB output is a positive, 0.4 to 0.7 µs pulse. Data changes about 50 ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB, and the angle is determined by the sum of the bits at logic "1". Digital outputs are three-state and provide two bytes; bits 1 through 8 (MSB) are enabled by the signal EM and bits 9 through 16 (LSB) are enabled by the signal EL.

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50 ns nominal. Valid data is available at the outputs 0.2 µs after the leading edge of CB.

As long as the converter maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when power is initially applied, the response will be critically damped. After initial slewing at the

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maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to final value is a function of the small signal settling time.

Resolution control is via two logic inputs, A and B. The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that no race conditions exist between counting and changing the resolution, inputs A and B are latched internally on the trailing edge of CB.

Direction Output (U) is a logic "1" to count up and logic "0" for down. The logic level at (U) is valid 0.5 µs before and 0.5 µs after the leading edge of CB.

Either low or high bandwidth can be selected by using the BW logic input. A logic "0" applied to BW will select low bandwidth (130 Hz nom.); a logic "1" selects high bandwidth (530 Hz nom.). Bandwidth can be changed during converter operation.

3.4.6 Dynamic Performance

A Type II servo loop (Kv = •) and very high acceleration constants give the RDC-19200 superior dynamic performance, as listed in the specifications. If the power supply voltages are not within the ±15 VDC nominal values (5%), the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage.

3.4.7 Built-in-Test (Internal to the Converter)

The RDC-19200 provides two useful logic outputs for systems self tests. The Built-In-Test output (BIT) monitors the level of error (D) and, if it exceeds approximately 65 bits, the logic level at BIT will change from logic "1" to logic "0". This condition will occur during a large step and reset after the converter settles out. BIT will also be set for an over-velocity condition because the converter loop cannot maintain input/output sync, and if the converter malfunctions where it cannot maintain the loop at a null. For system safety, the Loss Of Signal (LOS) output is useful. The LOS signal will change from logic "0" to "1" if both resolver inputs are disconnected, resulting in unpredictable converter performance.

3.5 BUILT-IN-TEST (ON-BOARD)

The Built-in-Test feature of the VMIVME-4941 requires a separate digital to resolver converter board. Built-in-Test is performed under software control in which the D/R output board is used as a resolver input for the VMIVME-4941. The VMIVME-4941's CSR is programmed to connect all four R/D modules to the P2 resolver input channel. Thus, a digital word is transferred to the D/R board and can

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be read back on all channels and a software compare performed on the digital data. Using this scheme all R/D converters can be tested in the same software test loop. The reader should refer to Section 4 for additional programming details. A front panel Fail LED is initialized on during power-up reset and may be extinguished via program control upon successful completion of diagnostics. Because this product is designed to utilize the DC reference voltage from channel 0 for the test signal input to all four modules, this functional test is accurate to within 20 counts (the user should expect a 20-count error).

3.6 PITCH COUNTER OPERATION

The 16-bit pitch counters utilize the direction and carry outputs from the R/D modules to count the number of revolutions. Control logic is provided (refer to Figure 3.6-1) to ensure synchronous writing/reading/counting.

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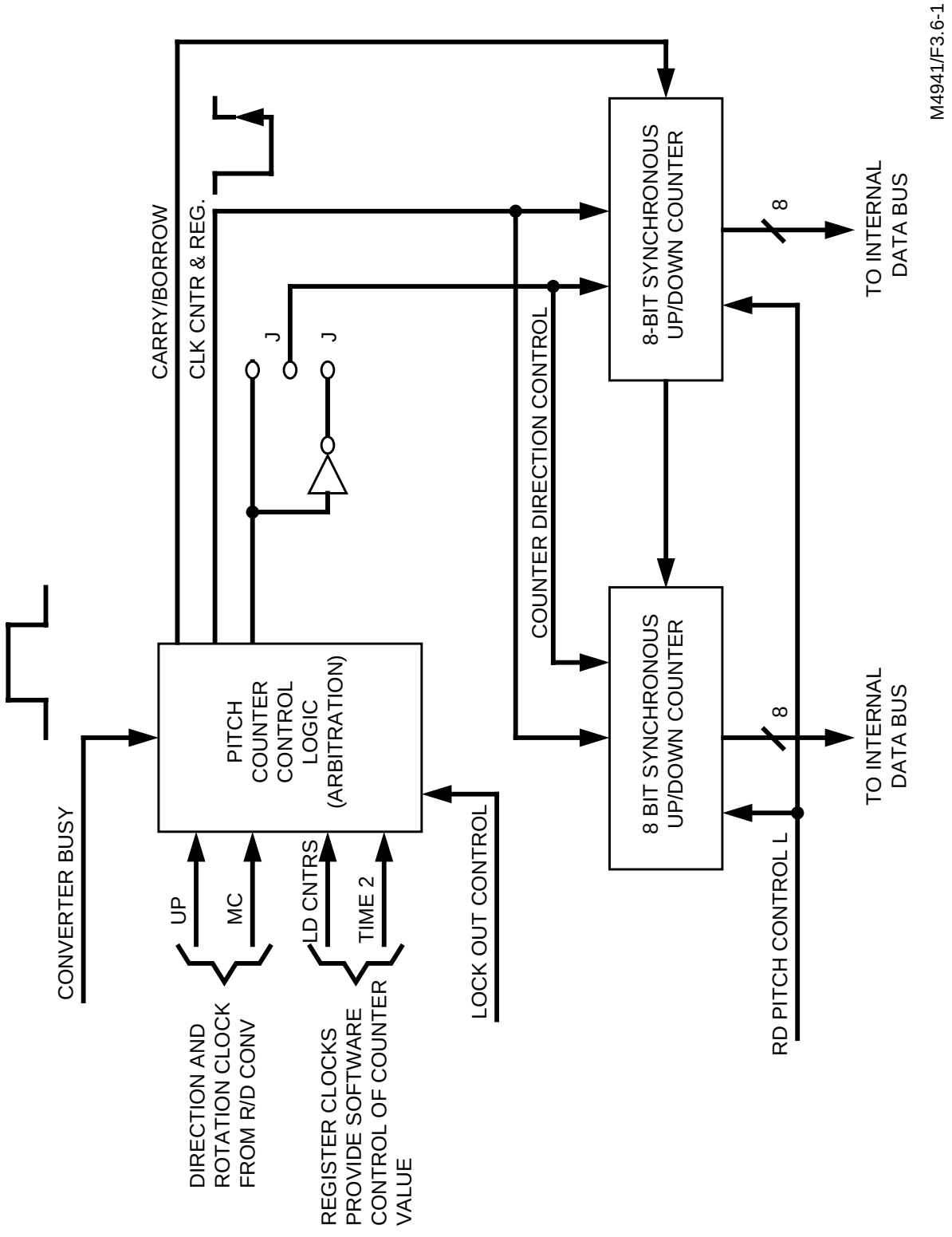


Figure 3.6-1. Pitch Counter Logic Functional Block Diagram

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SECTION 4

PROGRAMMING

4.1 REGISTER MAP

The VMIVME-4941 contains four 16-bit registers corresponding to four R/D converters, four 16 bit pitch counters, and a 32-bit Control and Status Register (CSR). All the registers are byte, word, and longword addressable. Furthermore, the pitch counter register and the R/D data register for a single channel can be read as a single longword. Table 4.1-1 contains the address and functions of each register. Table 4.1-2 gives a more detailed definition of each register.

The base address is determined by address selection switches. For more information concerning the address switch selection requirements, the reader should refer to Section 5.

The VMIVME-4941 registers are accessable as bytes, words, or longwords. The word and longword register maps are shown in Figures 4.1-1 and 4.1-2

4.2 PITCH COUNTER(S)/REGISTER(S)

The pitch counter function is to count the revolutions or pitches that the resolver goes through. The R/D converters generate carry/borrow and direction information each time a resolver passes through the 0° axis. The pitch counters count how many times the resolver has passed through the 0° axis.

Each pitch counter contains 16 bits of count information providing a total count of 65,535 before the counter overflows to all zeroes. The count direction is jumper programmable so that the user can define which rotation direction will produce an increment to the counter. The reader should refer to Section 5.8 for additional details concerning the pitch counter(s) operation. Pitch counters are read/write registers which may be accessed without limiting operational functions.

4.3 RESOLVER-TO-DIGITAL CONVERTER DATA REGISTER

The digital information contained in the D/R registers is the natural binary representation of the resolver input angle. Table 4.3-1 below shows the bit-weight and how the information is stored in the read only register.

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Table 4.1-1. Address Register Map

RELATIVE ADDRESS	MNEMONIC	ACCESS MODE	NAME/FUNCTION
00	PC0U	READ/WRITE	PITCH COUNTER NO. 0 UPPER BYTE
01	PC0L	READ/WRITE	PITCH COUNTER NO. 0 LOWER BYTE
02	RD0U	READ	R/D NO. 0 UPPER BYTE
03	RD0L	READ	R/D NO. 0 LOWER BYTE
04	PC1U	READ/WRITE	PITCH COUNTER NO. 1 UPPER BYTE
05	PC1L	READ/WRITE	PITCH COUNTER NO. 1 LOWER BYTE
06	RD1U	READ	R/D NO. 1 UPPER BYTE
07	RD1L	READ	R/D NO. 1 LOWER BYTE
08	PC2U	READ/WRITE	PITCH COUNTER NO. 2 UPPER BYTE
09	PC2L	READ/WRITE	PITCH COUNTER NO. 2 LOWER BYTE
0A	RD2U	READ	R/D NO. 2 UPPER BYTE
0B	RD2L	READ	R/D NO. 2 LOWER BYTE
0C	PC3U	READ/WRITE	PITCH COUNTER NO. 3 UPPER BYTE
0D	PC3L	READ/WRITE	PITCH COUNTER NO. 3 LOWER BYTE
0E	RD3U	READ	R/D NO. 3 UPPER BYTE
0F	RD3L	READ	R/D NO. 3 LOWER BYTE
10	CSRU	READ/WRITE	CONTROL AND STATUS REGISTER UPPER
11	CSRMU	READ	CONTROL AND STATUS REGISTER MED UPPER
12	CSRML	WRITE	CONTROL AND STATUS REGISTER MED LOWER
13	CSRL	WRITE	CONTROL AND STATUS REGISTER LOWER
$XX14-XX1F	NOT USED		

M4941/T4.1-1

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Table 4.1-2. Address and Register Bit Definitions

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	A0								
X X	X	X	X	0	0	0	0	0	**PITCH COUNTER 0 UPPER BYTE**							
									IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
X X	X	X	X	0	0	0	0	1	**PITCH COUNTER 0 LOWER BYTE**							
									IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 0
X X	X	X	X	0	0	0	1	0	**R/D REGISTER 0 UPPER BYTE***							
									IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									MSB 1	2	3	4	5	6	7	8
X X	X	X	X	0	0	0	1	1	**R/D REGISTER 0 LOWER BYTE***							
									IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									9	10	11	12	13	14	15	LSB 16
X X	X	X	X	0	0	1	0	0	**PITCH COUNTER 1 UPPER BYTE**							
									IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
X X	X	X	X	0	0	1	0	1	**PITCH COUNTER 1 LOWER BYTE***							
									IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 0
X X	X	X	X	0	0	1	1	0	**R/D REGISTER 1 UPPER BYTE***							
									IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									MSB 1	2	3	4	5	6	7	8
X X	X	X	X	0	0	1	1	1	**R/D REGISTER 1 LOWER BYTE***							
									IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									9	10	11	12	13	14	15	LSB 16

M4941/T4.1-2/1

(Base Address Determined by Address Selection Switches)

*See Table 4.3-1 and bit/weight table.

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Table 4.1-2. Address and Register Bit Definitions (Concluded)

HEX ADDRESS	BINARY ADDRESS															
A15 - A8	A7	A6	A5	A4	A3	A2	A1	A0								
									PITCH COUNTER 2 UPPER BYTE							
X X	X	X	X	0	1	0	0	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
									PITCH COUNTER 2 LOWER BYTE							
X X	X	X	X	0	1	0	0	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 0
									R/D REGISTER 2 UPPER BYTE*							
X X	X	X	X	0	1	0	1	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									MSB 1	2	3	4	5	6	7	8
									R/D REGISTER 2 LOWER BYTE*							
X X	X	X	X	0	1	0	1	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									9	10	11	12	13	14	15	LSB 16
									PITCH COUNTER 3 UPPER BYTE							
X X	X	X	X	0	1	1	0	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
									PITCH COUNTER 3 LOWER BYTE							
X X	X	X	X	0	1	1	0	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 0
									R/D REGISTER 3 UPPER BYTE*							
X X	X	X	X	0	1	1	1	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									MSB 1	2	3	4	5	6	7	8
									R/D REGISTER 3 LOWER BYTE*							
X X	X	X	X	0	1	1	1	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									9	10	11	12	13	14	15	LSB 16
									CONTROL/STATUS REGISTER							
X X	X	X	X	1	0	0	0	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									**	**	FAIL LED	TEST MODE	CONNECT CH3	CONNECT CH2	CONNECT CH1	CONNECT CH0
									CONTROL/STATUS REGISTER							
X X	X	X	X	1	0	0	0	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									CH3 0=ERR	CH3 1=SIG	CH2 0=ERR	CH2 1=SIG	CH1 0=ERR	CH1 1=SIG	CH0 0=ERR	CH0 1=SIG
									CONTROL/STATUS REGISTER							
X X	X	X	X	1	0	0	1	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
									N/C	CH3 HBW	CH3 B	CH3 A	N/C	CH2 HBW	CH2 B	CH2 A
									CONTROL/STATUS REGISTER							
X X	X	X	X	1	0	0	1	1	IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
									N/C	CH1 HBW	CH1 B	CH1 A	N/C	CH0 HBW	CH0 B	CH0 A

* Refer to Table 4.3-1 and bit/weight table.
** Not used - reserved.

M4941/T4.1-2/2

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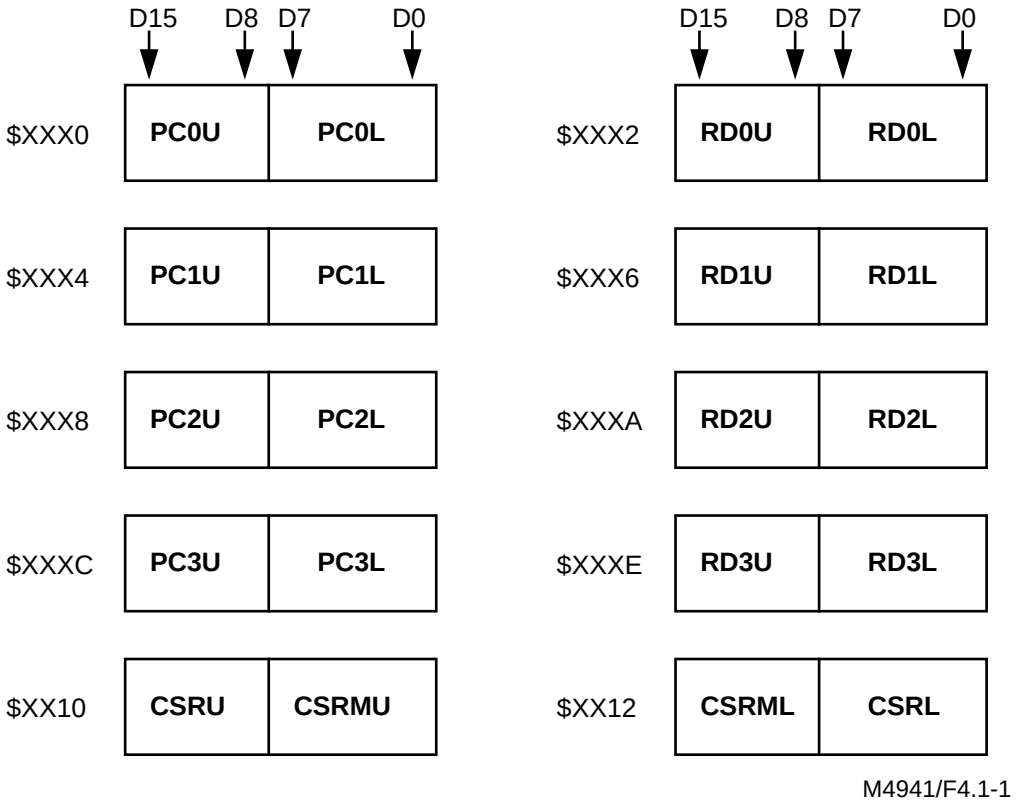


Figure 4.1-1. Register Map for Word Addressing

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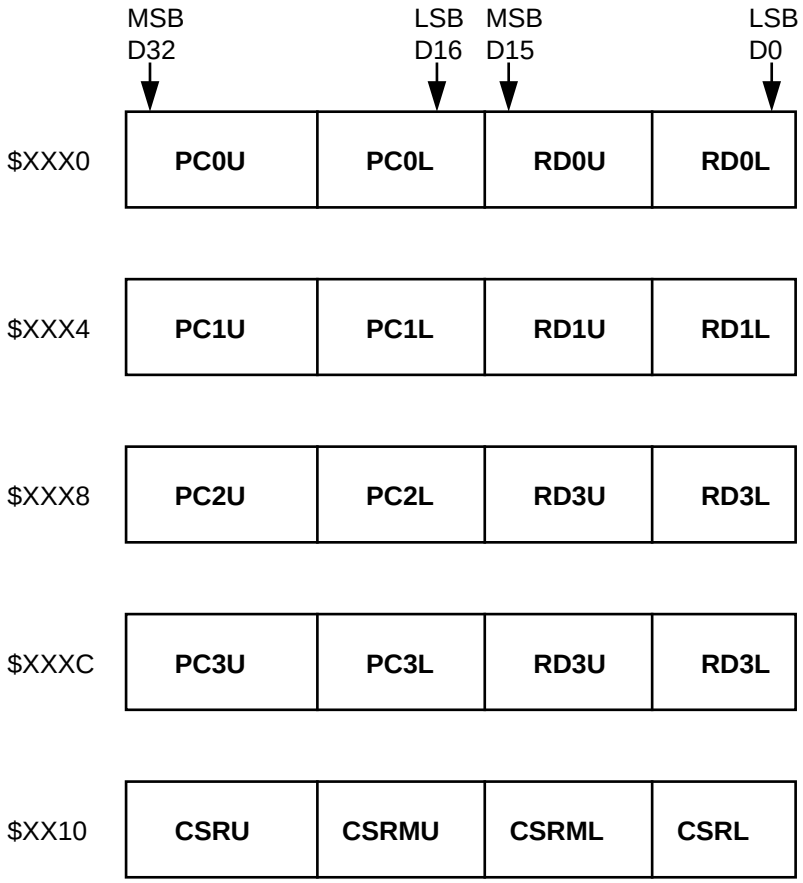


Figure 4.1-2. Register Map for Longword Addressing

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Table 4.3-1. Resolver-to-Digital Converter Data Register and Bit-Weight Table

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NO MSB	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16 LSB

BIT-WEIGHT TABLE

BIT NO.	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5.400
3	45	2.700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	169.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

M4941/T4.3-1

The D/R registers contain 10, 12, 14 or 16 bits, depending upon the user programming of the resolution. Unused bits are read as zero. The resolution can be changed during converter operation so the appropriate isolation and velocity dynamics can be changed as needed.

4.4 CONTROL AND STATUS REGISTER (CSR)

The CSR contains the Fail LED bit, five relay control bits, signal loss indication, error indication, resolution control bits, and bandwidth selection. The following sub-sections explain the function of each of the CSR bits. All bits are cleared upon power-up or upon a system reset, except the board Fail LED bit. The

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board Fail LED bit is initialized ON. Detailed bit maps of the CSR are shown in Tables 4.4-1, 4.4-2, 4.4-3, AND 4.4-4.

4.4.1 Built-in-Test Programming

The relay configuration shown in Figure 3.1-1 is designed for board testing. Activating the TEST MODE relay connects all R/D converter modules to the P2 connector so the user may apply a test signal for board level testing.

For normal R/D operation, CSR bits 24, 25, 26 and 27 are set to enable the resolver inputs, via the front panel connector, to be connected to their respective R/D converter modules. See Tables 4.4-4 and 4.4.1-1 for the function of each relay control bit in the CSR.

CAUTION

RELAY CONTROL BITS 24, 25, 26 AND 27 SHOULD *NEVER* BE SET WHEN THE TEST MODE BIT (BIT 28) IS SET. FAILURE TO HEED THIS PROGRAMMING NOTE MAY RESULT IN DAMAGE TO THE VMIVME-4941 BOARD. THE PROBLEM CAN BE CAUSED BY THE SIMULTANEOUS CONNECTION OF MORE THAN ONE VOLTAGE SOURCE TO THE CONVERTER INPUT. NOTE THAT THE RELAY DROPOUT TIME IS ONE MILLISECOND, MAXIMUM.

4.4.2 Fail LED Control

Controls front panel Fail LED. Setting the bit to a "zero" will turn the Fail LED ON. Setting the bit will turn the LED OFF.

4.4.3 R/D Converter Resolution Control

The CSR also allows the user to select each resolver-to-digital channel as specified in Tables 4.1-2, 4.4-3, and 4.4-4. Each converter may be programmed as shown in the following matrix to select the desired resolution:

CONTROL BIT*		RESOLUTION (BITS)
XB	XA	
0	0	10
0	1	12
1	0	14
1	1	16

*X = Channel number 0, 1, 2, or 3.

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Table 4.4-1. CSR HI Byte Bit Map ($XX10)

IDB 31	IDB 30	IDB 29	IDB 28	IDB 27	IDB 26	IDB 25	IDB 24
RESERVED		**FAIL LED**	**TEST MODE**	**CONNECT CH3**	**CONNECT CH2**	**CONNECT CH1**	**CONNECT CH0**
(0)	**(0)**	**0=ON 1=OFF**	**1=TEST 0=OPERATE**				

M4941/T4.4-1

Table 4.4-2. CSR M-HI Byte Bit Map ($XX11)

IDB 23	IDB 22	IDB 21	IDB 20	IDB 19	IDB 18	IDB 17	IDB 16
CHAN 3		**CHAN 2**		**CHAN 1**		**CHAN 0**	
0=ERR ≥65 BITS	**1=SIG LOSS**	**0=ERR ≥65 BITS**	**1=SIG LOSS**	**0=ERR ≥65 BITS**	**1=SIG LOSS**	**0=ERR ≥65 BITS**	**1=SIG LOSS**

M4941/T4.4-2

Table 4.4-3. CSR M-LO Byte Bit Map ($XX12)

IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8
RESERVED	**CHAN 3**			**RESERVED**	**CHAN 2**		
(0)	**1=SEL HIGH BANDWIDTH**	**RESOLUTION SEL**		**(0)**	**1=SEL HIGH BANDWIDTH**	**RESOLUTION SEL**	
		B	**A**			**B**	**A**

M4941/T4.4-3

Table 4.4-4. CSR LO Byte Bit Map ($XX13)

IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0
RESERVED	**CHAN 1**			**RESERVED**	**CHAN 0**		
(0)	**1=SEL HIGH BANDWIDTH**	**RESOLUTION SEL**		**(0)**	**1=SEL HIGH BANDWIDTH**	**RESOLUTION SEL**	
		B	**A**			**B**	**A**

M4941/T4.4-4

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Table 4.4.1-1. CSR Relay Control Functions

CSR BIT	RELAY CONTROL MNEMONIC	FUNCTION
24	CONNECT CH0	CONNECTS THE CH 0 INPUT FOR NORMAL OPERATION
25	CONNECT CH1	CONNECTS THE CH 1 INPUT FOR NORMAL OPERATION
26	CONNECT CH2	CONNECTS THE CH 2 INPUT FOR NORMAL OPERATION
27	CONNECT CH3	CONNECTS THE CH 3 INPUT FOR NORMAL OPERATION
28	TEST MODE	CONNECTS THE TEST CH INPUT TO ALL R/D CONVERTERS

M4941/T4.4.1-1

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4.4.4 R/D CONVERTER BANDWIDTH CONTROL

The CSR also contains bits that provide the user with the capability of selecting HI or LO bandwidth options as shown in the following matrix:

	RESOLUTION (Values in RPS/volts)			
BW (XHB)	10	12	14	16
HI	80	20	5	1.25
LO	20	5	1.25	0.32

The format of the CSR is shown in Table 4.1-2.

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

WARNING

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated.

5.3 JUMPER AND SWITCH LOCATIONS

Refer to Figure 5.3-1 for locations of all jumpers and switches.

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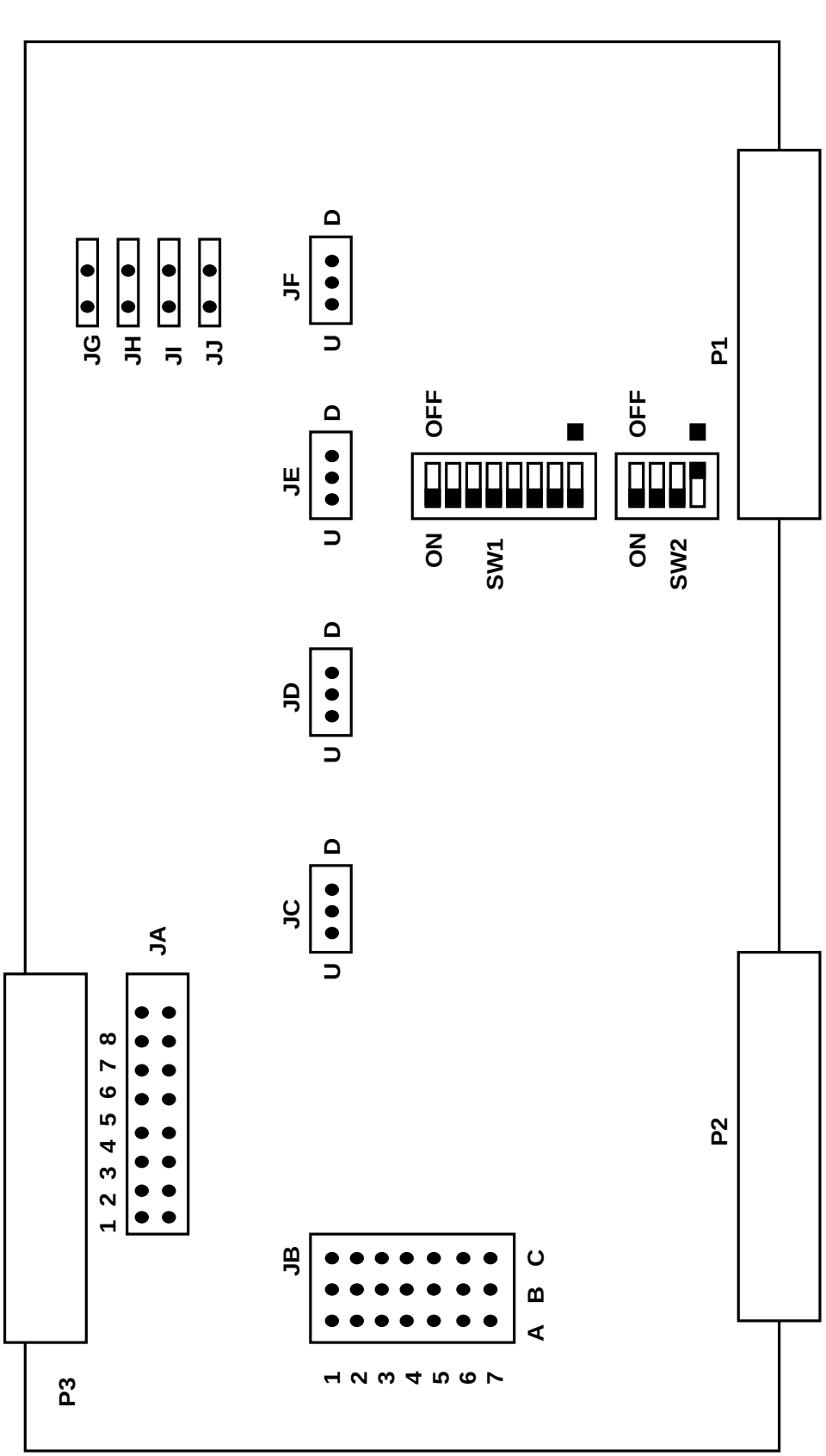


Figure 5.3-1. Location of Jumpers and Switches

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5.4 ADDRESS MODIFIERS

The VMIVME-4941 is designed to respond to short supervisory or non-privileged I/O access (switch selectable). Set the AM2 switch (refer to Figure 5.5-1) to OFF to select short supervisory access or to ON to select short non-privileged access.

5.5 ADDRESS SELECTION SWITCHES

The addressing DIP switches and their use in the board addressing scheme are depicted in Figure 5.5-1.

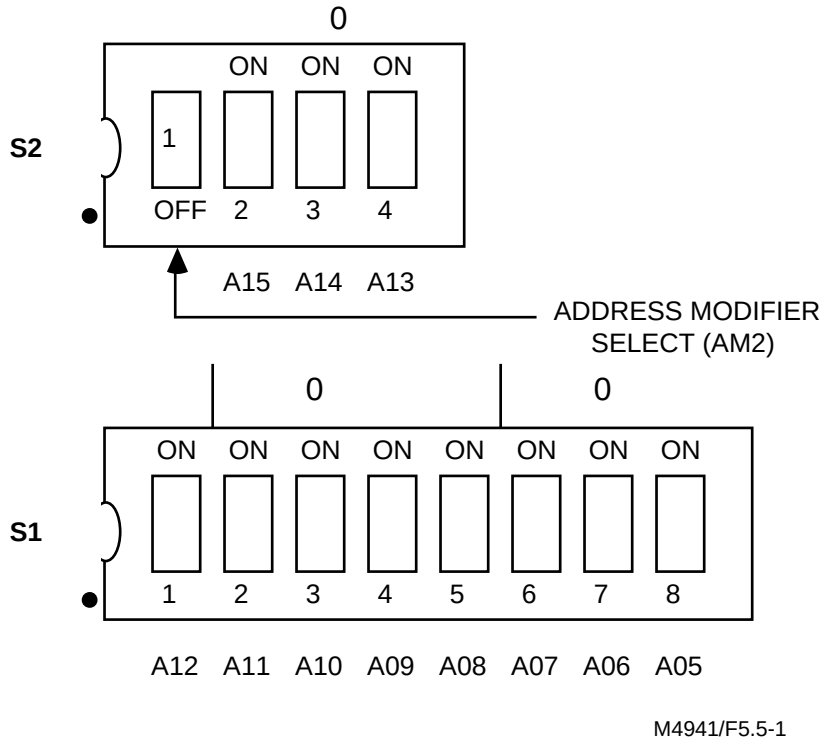


Figure 5.5-1. Address Selection Switch Example (Address 0000) and Address Modifier Switch Example (Short Supervisory Access)

5.6 EXTERNAL POWER SELECTION

Jumpers are provided to allow the user to connect ±15 V power inputs from either the P3 connector or from the P2 (backplane) connector. See Figures 5.6-1 and 5.6-2 to select ±15 V from the front panel or from the P2 connector, respectively.

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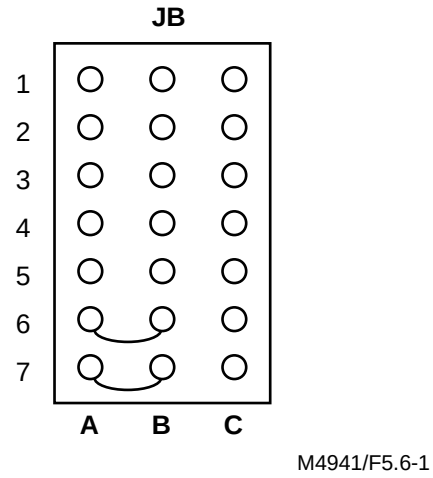


Figure 5.6-1. Jumper Installation to Select ±15 V Inputs via the P3 Connector

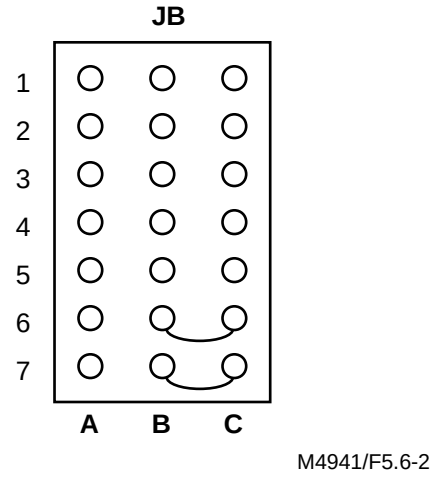
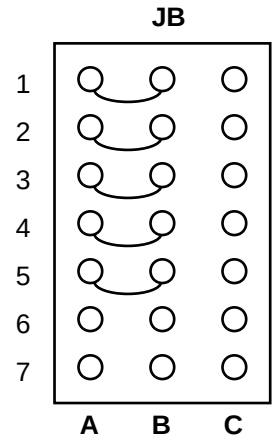


Figure 5.6-2. Jumper Installation to Select ±15 V Inputs via the P2 (Backplane) Connector

5.7 REFERENCE VOLTAGE INPUTS

The reference voltage input to the four R/D (or S/D) converter modules may be applied via the front panel (see Figure 5.7-1) or via the P2 connector (see Figure 5.7-2). Provision is also made to allow a separate reference input for each R/D (or S/D) converter (see Figure 5.7-3) via the P2 connector.

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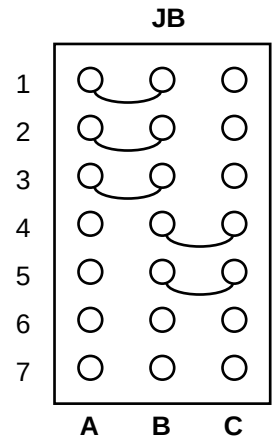


M4941/F5.7-1

Figure 5.7-1. Jumper Installation to Select the Reference Voltage Input at P3 for All Four Channels

```
*************
*  CAUTION  *
*************
```

THE FIELD INPUT FOR RL MUST BE ISOLATED FROM THE POWER SOURCE IF THE JB5 A-B JUMPER IS INSTALLED. OTHERWISE, FIELD SOURCE OR BOARD DAMAGE MAY RESULT SINCE THIS JUMPER CONNECTS P3/RL TO THE LOCAL ANALOG GROUND.



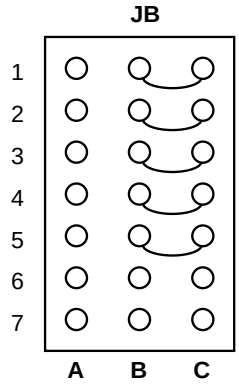
M4941/F5.7-2

Figure 5.7-2. Jumper Installation to Select a Single Reference Voltage Signal from P2 (Pins C29 and C27) for All Four Channels

```
*************
*  CAUTION  *
*************
```

THE FIELD INPUT FOR RL MUST BE ISOLATED FROM THE POWER SOURCE IF THE JB5 A-B JUMPER IS INSTALLED. OTHERWISE, FIELD SOURCE OR BOARD DAMAGE MAY RESULT SINCE THIS JUMPER CONNECTS P2/RL TO THE LOCAL ANALOG GROUND.

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M4941/F5.7-3

Figure 5.7-3. Jumper Installation to Select a Separate Reference Voltage Signal for Each Channel via the P2 Connector

```
*************
*  CAUTION  *
*************
```

THE FIELD INPUT FOR RL MUST BE ISOLATED FROM THE POWER SOURCE IF THE JB5 A-B JUMPER IS INSTALLED. OTHERWISE, FIELD SOURCE OR BOARD DAMAGE MAY RESULT SINCE THIS JUMPER CONNECTS P2/RL TO THE LOCAL ANALOG GROUND.

5.8 COUNTER DIRECTION JUMPERS

Each Resolver-to-Digital (or Synchro-to-Digital) Converter is designed with a dedicated 16-bit pitch counter or pitch count information associated with each R/D converter. The direction in which each counter counts is determined by counter direction control jumpers as shown in Tables 5.8-1 and 5.8-2.

5.9 JUMPERING FOR DIRECT vs DIFFERENTIAL SIGNAL INPUTS

5.9.1 Direct Input Option - Resolver

For the direct input option (2 volt signal), jumper field JA must always be configured as shown in Figure 5.9.1-1. Jumpers JG, JH, JI, and JJ must be removed.

5.9.2 Differential Input Option - Resolver

All jumpers must be removed from the JA jumper field to configure the VMIVME-4941 for differential signal inputs. Jumpers JG, JH, JI, and JJ must be installed.

If the differential (11.8 V) option was purchased and single-ended operation is desired, then all jumpers must be installed in the JA jumper field as shown in Figure 5.9.2-1. Jumpers JG, JH, JI, and JJ must be removed.

5.9.3 Synchro Inputs

All jumpers must be removed from the JA jumper for inputs S1, S2, and S3. Remove jumpers JG, JH, JI, and JJ.

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Table 5.8-1. Jumper Installations for Counting Up When R/D Data is Increasing

CHANNEL NUMBER	JUMPER
CH0	JC U ○—○ ○ D
CH1	JD U ○—○ ○ D
CH2	JE U ○—○ ○ D
CH3	JF U ○—○ ○ D

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Table 5.8-2. Jumper Installations for Counting Down When R/D Data is Increasing

CHANNEL NUMBER	JUMPER
CH0	JC U D
CH1	JD U D
CH2	JE U D
CH3	JF U D

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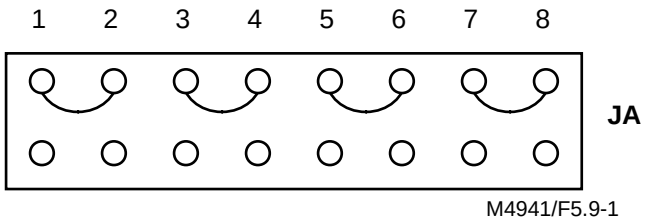


Figure 5.9.1-1. Jumper Configuration for the Direct Signal Input Option (2 Volt), this Configuration Connects S1 to S4 on Each Resolver Input Channel

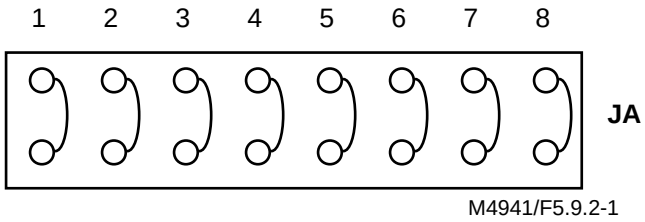


Figure 5.9.2-1. Jumper Installation to Select Single-Ended R/D Converter Inputs (11.8 V Option Only), These Jumpers Connect a Ground to the S1 and S4 Inputs for All Four Channels

5.10 CABLING REQUIREMENTS

The resolver inputs to the VMIVME-4941 should be connected as shown in Figure 5.10-1. Connector pin numbers are listed in Table 5.10-1. See Section 2.3 for connectior information.

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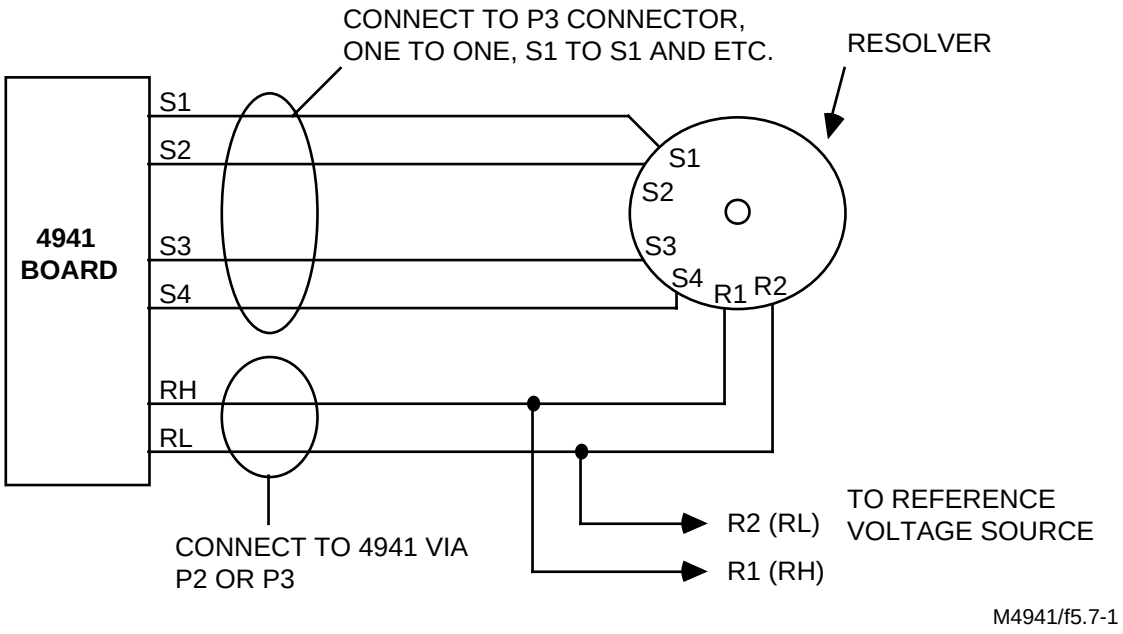


Figure 5.10-1. Recommended Connection of Resolver Reference Voltage and Signals

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Table 5.10-1. P2 and P3 Connector Pinouts

CONNECTOR	PIN	SIGNAL	
P2	C1	GND	
P2	C5, C6	P2 + 15 V	
P2	C7, C8	P2 - 15 V	
P2	C18	S1	TEST CHANNEL RESOLVER INPUT FOR BUILT-IN-TEST FEATURE
P2	C20	S2 COS	
P2	C22	S3 SIN	
P2	C24	S4	
P2	C29	P2RH	
P2	C27	P2RL	
P2	A27	P2RH1	SEPARATE REF. V. INPUTS FOR CHANNELS 1, 2, 3
P2	A28	P2RH2	
P2	A29	P2RH3	

CONNECTOR	PIN	SIGNAL	
P3	5	0S1	CHANNEL 0 RESOLVER INPUT
P3	6	0S2	
P3	7	0S3	
P3	8	0S4	
P3	9	1S1	CHANNEL 1 RESOLVER INPUT
P3	10	1S2	
P3	11	1S3	
P3	12	1S4	
P3	17	2S1	CHANNEL 2 RESOLVER INPUT
P3	18	2S2	
P3	19	2S3	
P3	20	2S4	
P3	21	3S1	CHANNEL 3 RESOLVER INPUT
P3	22	3S2	
P3	23	3S3	
P3	24	3S4	
P3	25	P3RH	
P3	13	P3RL	
P3	3	P3 + 15 V	
P3	14	P3 - 15 V	
P3	1, 2, 4, 15, 16	GND	

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

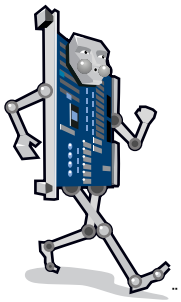
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