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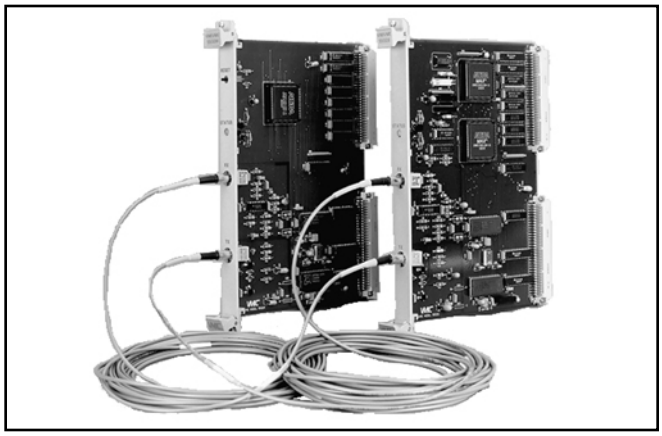
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Find the *Abaco Systems / VMIC VMIVME-5532M* at our website: *Click HERE*

VMIVME-5532L
VMEbus Fiber-Optic Repeater Link with Slave Chassis System Controller

- High-performance, easy-to-use method of linking two or more VMEbus systems together via fiber-optic cable
- Can provide system controller function in the slave chassis
- A local master is allowed in slave chassis
- Software transparent allows direct communication from master chassis to slave chassis with no software overhead (unidirectional link control with bidirectional data transfers). This mode allows plug-and-play operation.
- Register enable allows operation as described above, but includes registers in short I/O space dealing with slave chassis multimaster operation
- Supports 8-, 16-, and 32-bit data transfers
- Supports 16-, 24-, and 32-bit addressing
- Total electrical isolation between VMEbus systems
- Maximum 6,560 ft (2,000 m) fiber-optic cables
- Advantages over standard repeaters
  - — Small cables
  - — High-noise immunity
  - — High-voltage isolation
  - — No EMI generated by cables
- The VME-to-VME link consists of two boards and two fiber-optic cables



OVERVIEW — The VMIVME-5532 Link is a high-performance, yet easy-to-use method of linking two or more VMEbus systems together via fiber-optic cable. The Repeater Link is a two-board set which allows VMEbus slave I/O boards residing in one VMEbus chassis to be controlled by a VMEbus master residing in another chassis. In general, the VMEbus chassis in which VMEbus masters reside is referred to as a master chassis, while the VMEbus slave boards reside in a slave chassis. However, the VMIVME-5532 also allows a local VMEbus master to work in a slave chassis for local control, thus providing *multimaster* in the slave chassis. The two-board set is configured as shown in Figure 1 with one board designated for the master chassis while the other board is designated for the slave chassis. A master VMEbus chassis can communicate with several slave chassis by using multiple REPEATER Links in a star configuration as shown in Figure 2.

The link is software transparent. Any VMEbus master in the master chassis may access (read or write) to any slave board in the slave chassis. Only noninterrupter slave boards are allowed in the slave chassis.

The link between the master chassis and slave chassis is automatically established when a VMEbus master (typically a CPU board) addresses any board in the slave chassis.

Any time a master in the master chassis issues a VMEbus read/write cycle it will be repeated to the slave chassis. If a slave board in any slave chassis responds to that address, the data transfer (read or write) will occur between the chassis and a Data Transfer Acknowledge (DTACK) will be generated to the master (in master chassis) to complete the cycle.

The slave repeater includes a bus arbiter, bus requester, system controller, and Control/Status Registers for manipulating and monitoring the slave chassis when it is being used in a redundant repeater link or multimaster application as shown in Figure 3. The bus arbiter (SGL) and system controller are used when the slave board occupies slot 1 of the slave chassis. The bus requester (ROR) and Control/Status Registers allow the host CPU in the master VMEbus chassis to monitor and gain bus mastership of the slave chassis using bus request level 3 (BR3*). A control bit (burst mode) is included to allow the host CPU to request and hold bus mastership as long as desired. A key register is also included which requires the host CPU to load a matching code before the burst mode bit can be set.

A link consists of two boards (VMIVME-5532M and VMIVME-5532S) and two cables which enable a VMEbus system to be expanded beyond a single chassis. Refer to Figures 4 and 5 for a block diagram of each board.

VMEbus SPECIFICATIONS

VMEbus Compliance: Complies with VMEbus specification revision C.1A32, A24, A16: D32, D16, D08 (EO)

Arbiter: SGL

Requester: ROR, bus request level 3 only (BR3*)

BG3IN*-BG3OUT* Maximum Delay: 100 ns

BG3IN*-BBUSY* Maximum Delay: 200 ns

Link Registers (available when enabled):

- Board Identification
- Burst Mode
- Host Bus Grant
- VMEbus Activity (Slave Chassis)
- Burst Mode Key
- VMEbus Key
- Sysreset Enable Key
- Slave Chassis Reset Key

VMIVME-5532M is DTB slave (for use in Master Chassis)

VMIVME-5532S is DTB master (for use in Slave Chassis)

Form factor - double height, single slot

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Ordering Options								
July 15, 1997 800-005532-000 C		A	B	C	–	D	E	F
VMIVME-5532L	–				–			

A = Fiber-Optic Connector Type
- 0 = Ceramic Ferrule St Connector
- 1 = Stainless Steel Ferrule St Connector

BC = Cable Length

00 = No Cables	17 = 6,560 ft (2,000 m)
01 = 5 ft (1.5 m)	18 = 574 ft (174.9 m)
02 = 25 ft (7.6 m)	19 = 656 ft (199.9 m)
03 = 50 ft (15.2 m)	20 = 820 ft (249.9 m)
04 = 100 ft (30.4 m)	21 = 1,148 ft (349.9 m)
05 = 150 ft (45.7 m)	22 = 1,312 ft (399.9 m)
06 = 200 ft (60.9 m)	23 = 1,640 ft (499.9 m)
07 = 350 ft (106.7 m)	24 = 1,804 ft (549.8 m)
08 = 500 ft (152.4 m)	25 = 2,132 ft (649.8 m)
09 = 1,000 ft (304.8 m)	26 = 2,296 ft (699.8 m)
10 = 1,500 ft (457.3 m)	27 = 2,624 ft (799.8 m)
11 = 2,000 ft (609.7 m)	28 = 2,952 ft (899.8 m)
12 = 2,460 ft (750.0 m)	29 = 3,116 ft (949.7 m)
13 = 3,280 ft (1,000 m)	30 = 250 ft (76.2 m)
14 = 4,100 ft (1,250 m)	31 = 10 ft (3.0 m)
15 = 4,920 ft (1,500 m)	32 = 80 ft (24.4 m)
16 = 5,740 ft (1,750 m)	

BOARDS ONLY		A	B	C	–	D	E	F
VMIVME-5532M	–	0	0	0	–			

ABC = 000 (Options reserved for future use)

		A	B	C	–	D	E	F
VMIVME-5532S	–	0	0	0	–			

ABC = 000 (Options reserved for future use)

Note

Link: Includes one VMIVME-5532M (Master) Board, one VMIVME-5532S (Slave) Board, and two cable assemblies

Connector Data

Compatible Connector	*ST Connector*
PC Board Fiber-Optic Connector	Fiber-Optic Receiver HFBR-2416 (Hewlett-Packard) Fiber-Optic Transmitter HFBR-1414 (Hewlett Packard

For Ordering Information, Call:
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VMEbus Signals Repeated to Slave Chassis [1]:
A1 to A31, D0 to D31, DS0*, DS1*, WRITE*, SYSRESET*, SYSCLK, AM0, AM2, AM4, AM5, LWORD*, and IACK*

VMEbus Signals Returned to Master Chassis:
D0 to D31, DTACK*

VMEbus Signals Active in Slave Chassis But Not Repeated: BR0*-BR3*, BGIN0*-BGIN3*, BG0OUT*-BG3OUT*, BBSY*

Address Modifiers: 09, 0D, 29, 2D, 39, 3D

Read Cycle Overhead: 4.0 µs maximum

Write Cycle Overhead: 4.0 µs maximum

Transfer Rate (Maximum) (10-foot Cable Length): Assuming a slave board in the slave chassis responds in 250 ns:
1 Mbyte/s minimum (D32)

CABLE SPECIFICATIONS[2]

Mode: Multi

Length: 5 to 6,560 ft (1.5 to 2,000 m)

Fiber Size: 62.5 micron

Clad Size: 125 micron

Buffer Size: 900 micron

Maximum Attenuation at 1,300 nm: 9.0 dB (including connectors)

Bandwidth at 1,300 nm: 500 MHz-km

Boot Length: 20 to 60 mm

U.L./NEC Rating: OFNP

Connector Style: ST, 2.5 mm Bayonet, both ends

Quantity Required: 2 per link

PHYSICAL/ENVIRONMENTAL

Temperature: 0 to 65 °C, operating
-20 to 85 °C, storage

Humidity: 20 to 80 percent, relative noncondensing

Altitude: Operation to 10,000 ft (3,048 m)

Cooling: Forced air convection

1. The following signals are regenerated at the slave chassis instead of being sent over the fiber-optic cable: SYSCLK, AM0, AM1, AM3, and IACK*.

2. Cables conforming to this specification are supplied with VMIVME-5532L. To order cables separately, please refer to specification number VMICBL-000-F3-XXX.

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Dimensions: Double height (6U) board 160 x 233.35 mm

POWER REQUIREMENTS

VMIVME-5532S: 2 A typical at 5 VDC
2.5 A maximum

VMIVME-5532M: 2 A typical at 5 VDC
2.5 A maximum

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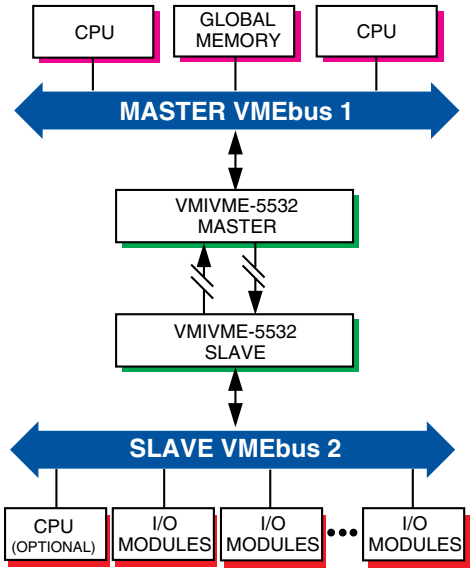


Figure 1. Single Link Application Diagram

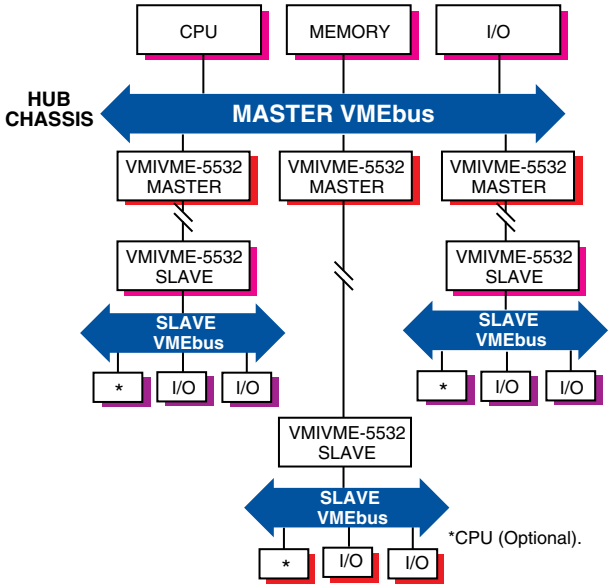
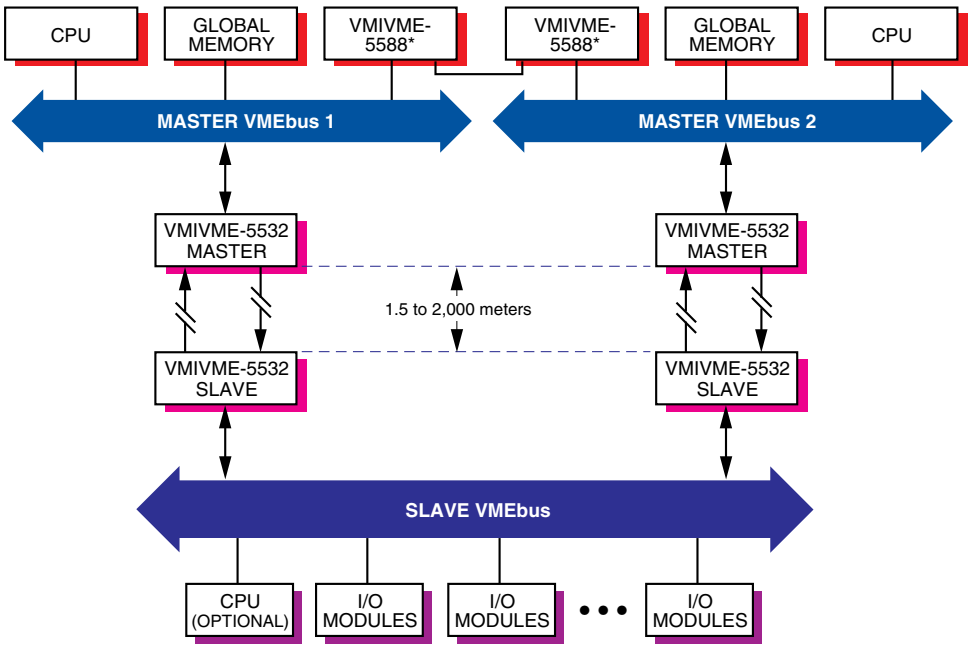


Figure 2. Star Configuration



*VMIVME-5588 Reflective Memory is an effective way to synchronize memory for multiple master CPUs.

Figure 3. Redundant Link Configuration

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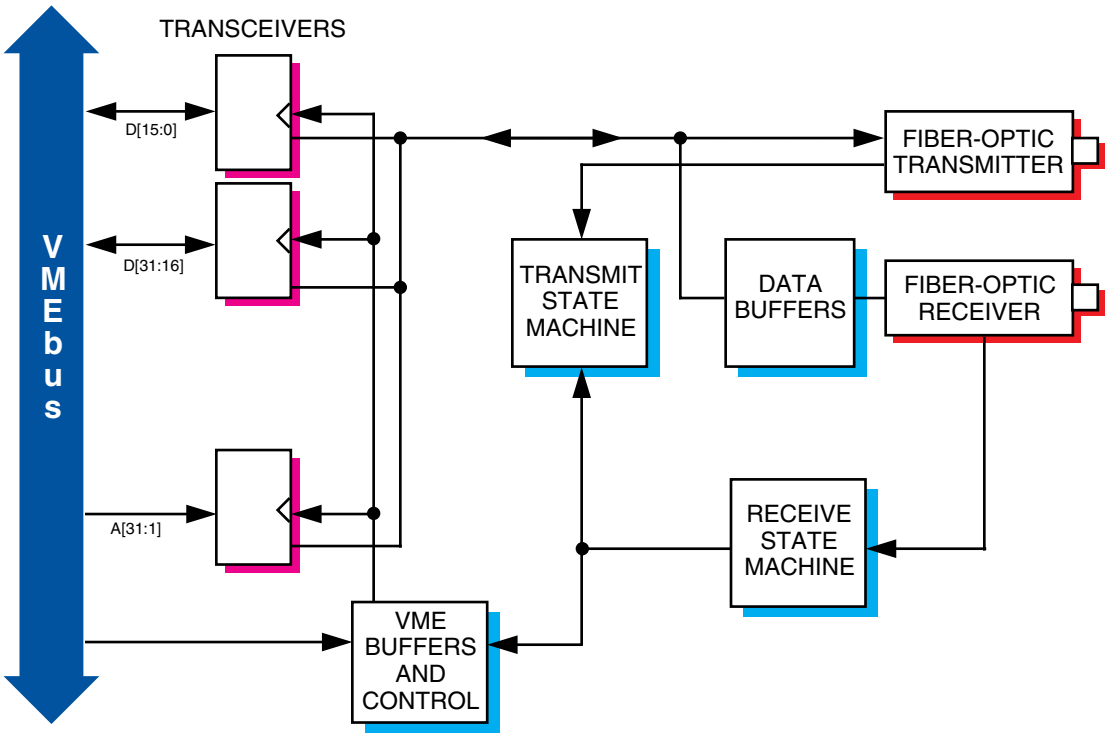


Figure 4. Block Diagram of VMIVME-5532M Master Chassis Repeater Link Board

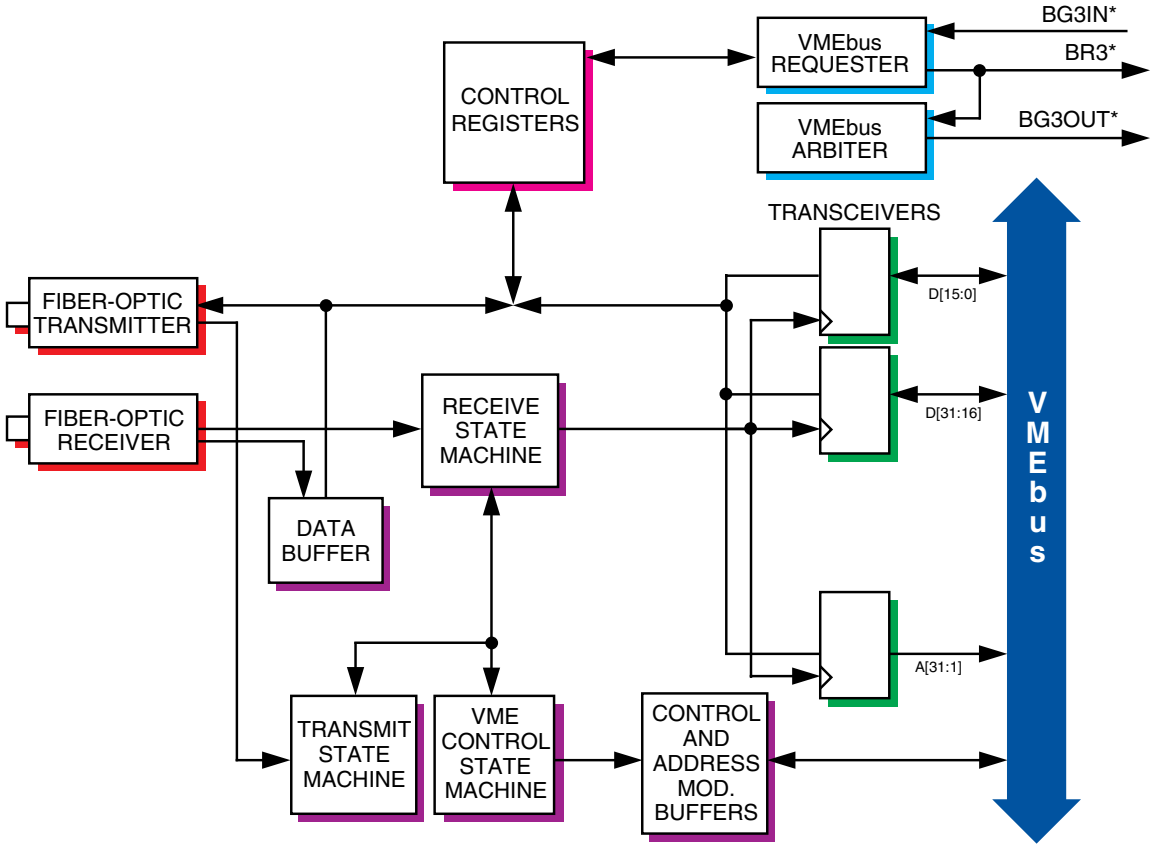


Figure 5. Block Diagram of VMIVME-5532S Slave Chassis Repeater Link Board

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