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Find the *Abaco Systems / VMIC VMIVME-5588DMA-210* at our website: ***Click HERE***

VMIVME-5588
High-Speed Reflective Memory with Interrupts

- High-speed, easy-to-use network (1.2 Gbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Up to 1,000 ft between nodes with multimode fiber, 10 km with single mode, 30 m with twinax
- Supports up to 256 nodes
- Data transferred at 29.5 Mbyte/s without redundant transfer
- Data transferred at 14.8 Mbyte/s with redundant transfer
- Any node on the network can generate an interrupt in any other node on the network or in all network nodes with a single command
- Error detection
- Redundant transmission mode for suppressing errors
- No processor overhead
- No processor involvement in the operation of the network
- Up to 16 Mbyte of Reflective Memory
- A24:A32:D32:D16:D8 memory access
- Two-slot 6U VMEbus board
- Any node may reset any or all other nodes
- Software compatible with VMIVME-5578
- Software-addressable digital output bit (available at front panel and P2 connector) for interfacing with the VMIVME-5599 optical switch board or any user-defined purpose
- Multimode or single-mode fiber-optic or twinax cable options

INTRODUCTION — VMIVME-5588 is a high-performance, daisy-chained VME-to-VME network. Data is transferred by writing to on-board global RAM. The data is automatically sent to the location in memory on all Reflective Memory boards on the network.

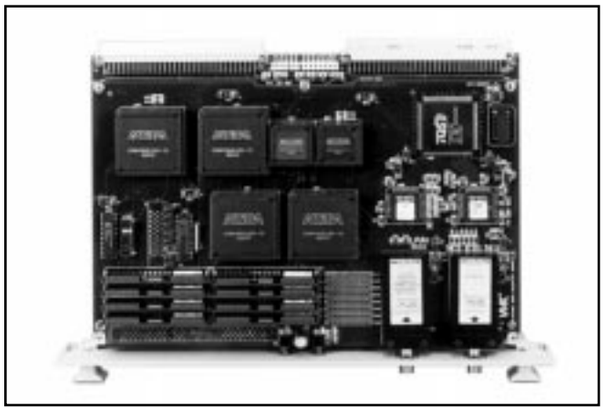
PRODUCT OVERVIEW — The Reflective Memory concept provides a very fast and efficient way of sharing data across distributed computer systems.

VMIC's VMIVME-5588 Reflective Memory interface allows data to be shared between up to 256 independent systems (nodes) at rates up to 29.5 Mbyte/s. Each Reflective Memory board may be configured with 256 Kbyte to 16 Mbyte of on-board SRAM. The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed data path to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize CPU and bus performance to maintain high data throughput.

The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. These interrupt (three levels, each user definable) signals may be used to synchronize a system process, or used to follow any data. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.

The VMIVME-5588 requires no initialization unless interrupts are being used. If interrupts are used, vectors and interrupt levels must be written to on-board registers and the interrupts enabled.

Each node on the system has a unique identification number between 0 and 255. The node number is established during hardware system integration by placement of jumpers on the board. This node number can be read by software by



accessing an on-board register. In some applications, this node number would be useful in establishing the function of the node.

In order to achieve an aggregate throughput of 29.5 Mbyte/s, nodes capable of writing to the Reflective Memory network at an aggregate rate of 29.5 Mbyte/s must be present. Note that workstation-to-VME adapters may limit the data transfer rate between the workstation and the Reflective Memory network.

LINK ARBITRATION — The VMIVME-5588 system is a daisy-chain ring as shown in Figure 1. Each transfer is passed from node-to-node until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives except those that it originated. Nodes are allowed to insert transfers between transfers passing through.

INTERRUPT TRANSFERS — In addition to transferring data between nodes, the VMIVME-5588 will allow any processor in any node to generate an interrupt on any other node. These interrupts would generally be used to indicate to the receiving node that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving node is ready for new data.

Three interrupts are available. The user may define the function, priority, and vector for each interrupt. Any processor can generate an interrupt on any other node on the network. In addition, any processor on the network can generate an interrupt on all nodes on the network. Interrupts are generated by simply writing to a VMIVME-5588 register.

All data and interrupt command transfers contain the node number of the node that originated the transfer. This information is used primarily so the originating node can remove the transfer from the network after the transfer has traversed the ring. The node identification is also used by nodes receiving interrupt commands. When a node receives an interrupt command for itself, it places the identification

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VME Microsystems Intl. Corp. 12090 South Memorial Parkway, Huntsville, AL 35803-3308 USA

Ordering Options								
June 16, 1999 800-005588-000 D		A	B	C	–	D	E	F
VMIVME-5588	–				–			

A = Memory Options
0 = 256 Kbyte
1 = 512 Kbyte
2 = 1 Mbyte
3 = 2 Mbyte
4 = 4 Mbyte
5 = 8 Mbyte
6 = 16 Mbyte

B = FIFO Option
0 = 512 Transfer FIFO
1 = 4 Kbyte Transfer FIFO

C = Transmission Mode

Transmit	Receive
0 = mm Fiber	mm Fiber
1 = Reserved	
2 = sm Fiber	sm Fiber
3 = mm Fiber	sm Fiber
4 = sm Fiber	mm Fiber
5 = Twinax	Twinax
6 = Twinax	mm Fiber
7 = Twinax	sm Fiber
8 = mm Fiber	Twinax
9 = sm Fiber	Twinax

Multimode Fiber-Optic Cable Assemblies

		A	B	C	–	D	E	F
VMICBL-000-F3	–		0		–			

A = Fiber-Optic Connector Type
0 = Ceramic Ferrule ST Connector
1 = Stainless Steel Ferrule ST Connector

BC = Cable Lengths
00 = Not Used
01 = 5 ft (1.5 m)
02 = 25 ft (7.6 m)
03 = 50 ft (15.2 m)
04 = 100 ft (30.4 m)
05 = 150 ft (45.7 m)
06 = 200 ft (60.9 m)
07 = 350 ft (106.7 m)
08 = 500 ft (152.4 m)
09 = 1,000 ft (304.8 m)

Twinax Cable Assemblies

		A	B	C	–	D	E	F
VMICBL-001-33	–	0			–			

A = 0 (Option reserved for future use)

BC = Cable Lengths
00 = Not Used
01 = 0.5 m
02 = 1 m
03 = 3 m
04 = 5 m
05 = 7 m
06 = 10 m
07 = 15 m
08 = 20 m
09 = 25 m
10 = 30 m

For Ordering Information, Call:
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number of the originating node in a FIFO. Up to 512 interrupts can be stacked in the FIFO. During the interrupt service routine, the identification of the interrupting node can be read from the FIFO.

ERROR MANAGEMENT — Errors are detected by the VMIVME-5588 with the use of the error detection facilities of the Fiber Channel encoder/decoder and additional interlaced parity encoding and checking. The error rate of the VMIVME-5588 is a function of the rate of errors produced in the cable portion of the system. This optical error rate depends on the length and type of fiber-optic cable. Assuming an optical error rate of 10^{-12}, the error rate of the VMIVME-5588 is 1.3 x 10^{-10} transfers/transfer.

However, the rate of undetectable errors is less than 1.64 x 10^{-20} transfers/transfer. When a node detects an error, the erroneous transfer is removed from the system and a VMEbus interrupt is generated, if enabled.

The VMIVME-5588 can be operated in a redundant transfer mode in which each transfer is transmitted twice. In this mode of operation, the first of the two transfers is used unless an error is detected in which case the second transfer is used. In the event that an error is detected in both transfers, the node removes the transfer from the system. The probability of both transfers containing an error is 1.64 x 10^{-20}, or about one error every 317,855 years at maximum data rate.

PROTECTION AGAINST LOST DATA — Data received by the node from the fiber-optic cable is error checked and placed in a receive FIFO. Arbitration with accesses from the VMEbus then takes place and the data is written to the node's SRAM and to the node's transmit FIFO. Data written to the board from the VMEbus is placed directly into SRAM and into the transmit FIFO. Data in the transmit FIFO is transmitted by the node over the cable to the next node. Data could be lost if either FIFO were allowed to become full.

The product is designed to prevent either FIFO from becoming full and overflowing. It is important to note the only way that data can start to accumulate in FIFOs is for data to enter the node at a rate greater than 29.5 Mbyte/s or 14.8 Mbyte/s in redundant mode. Since data can enter from the fiber and from the VMEbus, it is possible to exceed these rates. If the transmit FIFO becomes half-full, a bit in the Status Register is set and, if enabled, an interrupt is generated. This is an indication to the node's software that subsequent WRITEs to the Reflective Memory should be suspended until the FIFO is less than half-full. If the half-full indication is ignored and the transmit FIFO becomes full, then writes to the Reflective Memory will not be acknowledged until access is granted or the CPU times out with a Bus Error.

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If the transmit FIFO is allowed to become over half-full, there is a danger the receiver FIFO may overflow resulting in data loss. In order to prevent this situation, a VMEbus throttle mode will become active when the transmitter is over half-full. Instead of a 200 ns VMEbus response time, the VMEbus response time extends to 3.2 ms per access to allow the receiver time to move data from the receive FIFO to the transmit FIFO.

If the receive FIFO becomes over half-full, VME access is held off until the receive FIFO is less than half-full.

NETWORK MONITOR — There is a bit in a Status Register that can be used to verify that data is traversing the ring (that is, the ring is not broken). This can also be used to measure network latency.

VMIC offers multimode fiber-optic cables and twinax cables. VMIC does not offer single-mode fiber-optic cables.

SPECIFICATIONS

Memory Size: 256 Kbyte, 512 Kbyte, 1 Mbyte, 2 Mbyte, 4 Mbyte, 8 Mbyte, or 16 Mbyte

Access Time: 100 ns Write
400 ns Read (worst-case arbitration)
200 ns Read (best-case arbitration)

VME Cycle Time: 200 ns Write (20 Mbyte/s)
320 ns Read (12.5 Mbyte/s) (best-case arbitration)
520 ns Read (7.7 Mbyte/s) (worst-case arbitration)

TRANSFER SPECIFICATION

Transfer Rate: 29.5 Mbyte/s (longword accesses) without redundant transfer
14.8 Mbyte/s (longword accesses) with redundant transfer

COMPATIBILITY

VMEbus: This product complies with the VMEbus specification (ANSI/IEEE STD 1014-1987, IEC 821 and 297), with the following mnemonics:
A32:A24:D32/D16/D08 (EO): Slave: 39/3D:09/0D Form factor: 6U

Memory: Addressable on 256 Kbyte boundaries for 256 Kbyte memory option

Addressable on 512 Kbyte boundaries for 512 Kbyte memory option

Addressable on 1 Mbyte boundary for 1 Mbyte memory option

Addressable on 2 Mbyte boundaries for 2 Mbyte option

Addressable on 4 Mbyte boundaries for 4 Mbyte option

Addressable on 8 Mbyte boundaries for 8 Mbyte option

Addressable on 16 Mbyte boundaries for 16 Mbyte option

INTERCONNECTION

Cable Requirements: Two fiber-optic or twinax cables

Configuration: Daisy-chain ring up to 256 nodes

Power Requirements: 5.0 A maximum at +5 VDC

CABLES

VMIC offers the following cable assemblies that are compatible with the VMIVME-5588.

Multimode Fiber Cable:
ST connectors
1,000 feet maximum
62.5 micron core
10 dB maximum attenuation between nodes
Wavelength = 860 nm

Twinax Cable:
9-pin D-type connector
Equalized, 30 m maximum

The VMIVME-5588 is compatible with single-mode fiber with SC connectors and a maximum of 10 km. VMIC does not supply single-mode fiber cable.

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 65 °C, operating with forced air cooling. -40 to 85 °C, storage.

Relative Humidity: 20 to 80 percent, noncondensing

MTBF: 88,005 hours (217F)

DATA TRANSFERS

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the VMIVME-5588 is shown in Figure 2.

TRADEMARKS

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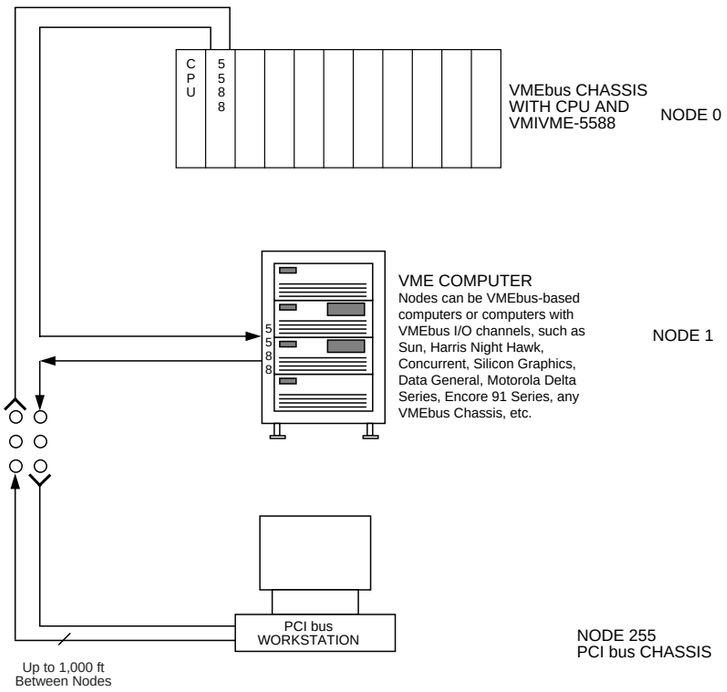


Figure 1. Network Example Using Reflective Memory System

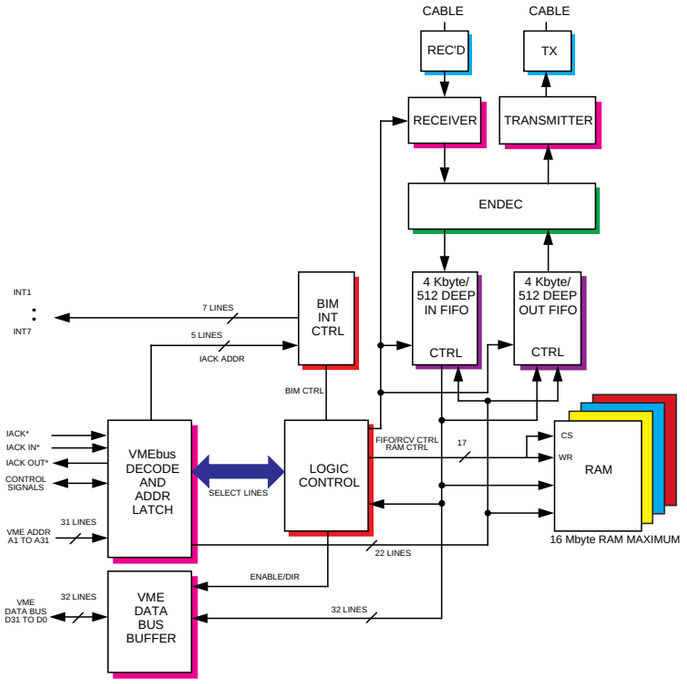


Figure 2. VMIVME-5588 Functional Block Diagram

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