ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Abaco Systems / VMIC VMIVME-5620-000* at our website: ***Click HERE***

VMIVME-5620

INTELLIGENT HSD EMULATOR

(HSDE)

PRODUCT MANUAL

DOCUMENT NO. 500-005620-000 D

Revised May 16, 1995

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
(205) 880-0444 FAX NO. (205) 882-0859
1-800-322-3616

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

Date: January 31, 1995

To: All VMIVME-5620 Users

From: VMIC Customer Service Engineering

Subject: Operation of the VMIVME-5620 BSP register

The intent of this notice is to inform and emphasize the use of the Board Status Pointer (BSP) register for applications which may require the Host Computer to poll the VMIVME-5620 for HSD status.

Recently it has come to our attention, that many VMIVME-5620 users who choose to poll the VMIVME-5620 for HSD status, are not using the Board Status Pointer (BSP) register, and instead are directly polling the HSD Status (BST) register.

The intent of the BSP register is to allow the VMIVME-5620 to run as freely as possible without interruption from the Host Computer. If the user chooses to poll the BST register directly, repeated accesses to the BST register, by the host, will interrupt and slow down theVMIVME-5620 internal processor. A description of how to use the BSP register is as follows:

- The user loads the BSP register with an address, which points to the same VMEbus memory space used to store the IOCL.
- The VMIVME-5620 stores and maintains an image of the BST register at this address.
- The user would then poll the VMEbus address, where the image of the BST register is stored and maintained, thus allowing the VMIVME-5620 to run free of interruption from the Host Computer.

NOTE: If the user has selected a VMEbus Block Transfer Mode (Hex AM code = $0B, $0F, $3B, or $3F) in either the IOCB Address Modifier (CAM) or the Data Address Modifier (DAM) registers, the Host Computer MUST use the BSP register, when polling for HSD status is necessary, or Data Corruption during DMA data transfers may occur. The Host Computer MUST NOT access any VMIVME-5620 register during VMEbus Block Transfers.

I hope this has cleared up any confusion as to correct software procedures when using the VMIVME-5620. If you should have any questions, please do not hesitate to contact VMIC's Customer Service Department at 1-800-240-7782 or FAX us at (205) 650-7245.

FILE 0131NOT1.WPS

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

To: Customers of VMIC

From: VMIC Customer Service

Subject: Field problems related to the IACK Daisy-chain

We have solved several integration problems by explaining the requirements for, and the proper installation or removal of, IACK Daisy-chain jumpers on the VMEbus backplane. In support of this we pass along the attached excerpt from "The VMEbus Specification" available from VITA, 10229 N. Scottsdale Road, Suite E, Scottsdale, AZ 85253 in the USA or VITA, P.O. Box 192, 5300 AD Zaltbommel, The Netherlands.

Please note that according to Rule 4.1, IACK Daisy-chain jumper must be installed at empty slots. These jumpers must be installed if boards with interrupt capability are present whether or not the interrupt function is being used. Caution should be taken to not install IACK jumpers at slots where interrupter boards are present.

CM/dj

Attachment

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Reference the VMEbus Specification, Section 4.2.2, Interrupt Acknowledge Line.

4.2.2 Interrupt Acknowledge Line. The IACK* line runs the full length of the backplane and is connected to the IACKIN* pin of slot 1 (see Fig 41). When driven low, the IACKIN* pin causes the IACK daisy-chain driver, located in slot 1, to propagate a falling edge down the interrupt acknowledge daisy-chain.

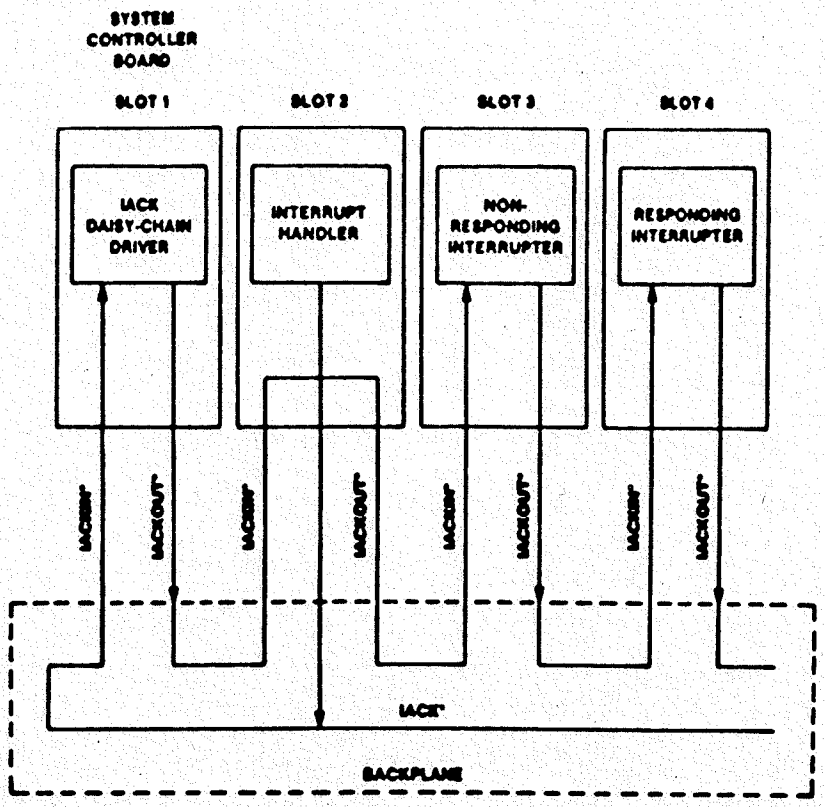
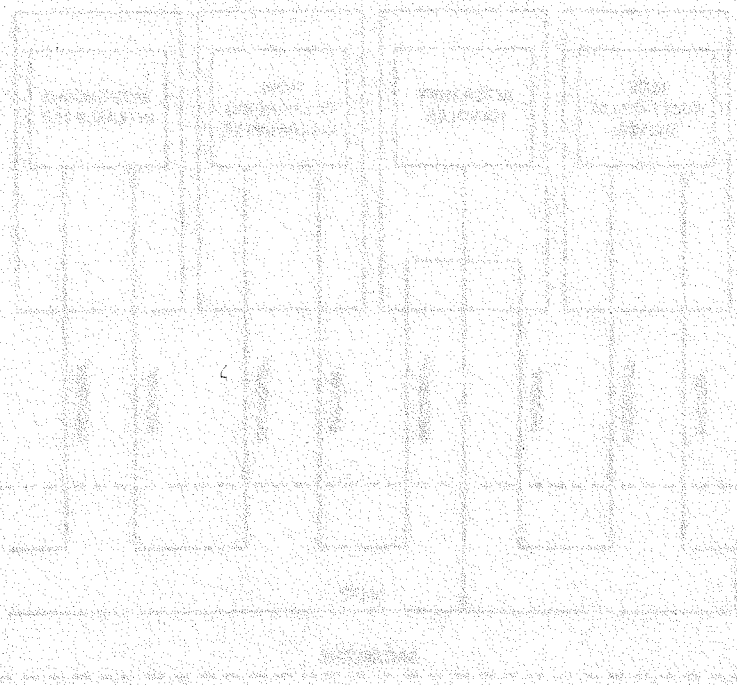


Fig 41
IACKIN* / IACKOUT* Daisy-Chain

4.2.3 Interrupt Acknowledge Daisy-Chain. Each of the seven interrupt request lines can be shared by two or more interrupter modules. The interrupt acknowledge daisy-chain ensures that only one interrupter responds to the system. Each interrupter that is driving an interrupt request line low waits for a falling edge to arrive at its IACKIN* daisy-chain input. Only upon receiving this falling edge does an interrupter respond to an interrupt acknowledge cycle. It does not pass the falling edge on down the daisy-chain, preventing other interrupters from responding to the interrupt acknowledge cycle.

Rule 4.1 If a backplane slot is not occupied by a board, and if there are boards farther down the interrupt acknowledge daisy-chain, then jumpers shall be installed at the empty slot to pass through the daisy-chain signal.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, VMIC assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

VMIC reserves the right to make any changes, without notice, to this or any of VMIC's products to improve reliability, performance, function, or design.

VMIC does not assume any liability arising out of the application or use of any product or circuit described herein; nor does VMIC convey any license under its patent rights or the rights of others.

For warranty and repair policies, refer to VMIC's Standard Conditions of Sale.

AMXbus, BITMODULE, DMAbus, MEGAMODULE, NETbus, SRTbus, TESTCAL, TURBOMODULE, UCLIO, UIOD, VMEmanager, VMEnet, VMEnet II, WARPNET, and WinUIOC are trademarks of VME Microsystems International Corporation. The VMIC logo and UIOC are registered trademarks of VME Microsystems International Corporation. Other registered trademarks are the property of their respective owners.

VME Microsystems International Corporation

All Rights Reserved

This document shall not be duplicated, nor its contents used for any purpose, unless granted express written permission from VMIC.

Copyright © April 1993 by
VME Microsystems International Corporation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	04/26/93	Release	93-0375
B	07/21/94	Cover, Pages ii, 5-2, and 5-3	94-0581
C	02/09/95	Cover, Pages ii, 4-3, and 4-14	95-0099
D	05/16/95	Cover, Notice, Pages ii, vi, vii, Deleted Section 4.24.8, and New Section 6	95-0372

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SAFETY SYMBOLS

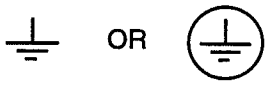
GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



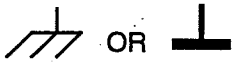
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



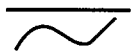
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-5620
INTELLIGENT HSD EMULATOR

TABLE OF CONTENTS

Page

SECTION 1 . INTRODUCTION

1.1 FEATURES 1-1
1.2 FUNCTIONAL DESCRIPTION 1-1

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATION

SECTION 3. THEORY OF OPERATION

3.1 OVERVIEW 3-1
3.2 MASTER/SLAVE, INTERBUS LINK, AND EXTERNAL MODES 3-1

SECTION 4. PROGRAMMING

4.1 REGISTER MAP 4-1
4.2 BOARD ID REGISTER (BID) 4-2
4.3 P.O.R. SELF-TEST STATUS REGISTER (STFLAG) 4-2
4.4 ROM VERSION REGISTER (ROM_VER) 4-3
4.5 HSD STATUS REGISTER (BST) 4-3
4.6 DEVICE STATUS REGISTER (DVS) 4-8
4.7 HSD MODE CONTROL REGISTER (MOD) 4-8
4.8 HSD ACTIVITY CONTROL REGISTER (ACT) 4-9
4.9 EXTENDED MODE REGISTER (EMOD) 4-11
4.10 IOCB ADDRESS MODIFIER REGISTER (CAM) 4-13
4.11 DATA ADDRESS MODIFIER REGISTER (DAM) 4-14
4.12 HSD INTERFACE TIME-OUT REGISTER (TIM) 4-14
4.13 VME ERROR INTERRUPT CONTROL REGISTER (VEIC) 4-15
4.14 HSD ERROR INTERRUPT CONTROL REGISTER (HEIC) 4-15
4.15 TRANSFER COMPLETE INTERRUPT CONTROL REGISTER(TCIC) 4-16
4.16 RESTART INTERRUPT CONTROL REGISTER (RSIC) 4-17
4.17 INTERRUPT VECTOR REGISTER (VEIV, HEIV, TCIC, RSIC) 4-18
4.18 RESIDUAL TRANSFER COUNT REGISTER (RXC) 4-18
4.19 IOCB POINTER REGISTER (CBP) 4-19
4-20 EXTERNAL FUNCTION WORD REGISTER (EFW) 4-19
4.21 DATA POINTER REGISTER (DBP) 4-19
4.22 BOARD STATUS POINTER REGISTER (BSP) 4-19
4.23 AUTOMATIC CLEARING OF STATUS BITS IN BST REGISTERS 4-20

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TABLE OF CONTENTS (Continued)

Page

SECTION 4. PROGRAMMABLE (Concluded)

4.24 PROGRAMMING DETAILS 4-21
4.24.1 General Programming for a Data Transfer, Master Mode 4-21
4.24.2 General Programming for a Data Transfer, Slave Mode 4-26
4.24.3 Interrupts 4-27
4.24.4 Inter-Bus Link Mode 4-29
4.24.4.1 Configuration and Interconnection 4-29
4.24.4.2 IBL Interface Signals 4-29
4.24.4.3 Link Acquisition and Data Transfer 4-30
4.24.5 External Mode 4-31
4.24.5.1 Entering or Exiting External Mode 4-31
4.24.5.2 External Mode Protocol 4-32
4.24.5.3 Execution 4-32
4.24.6 Self-Tests 4-33
4.24.7 Programming Examples 4-36

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 JUMPER CONFIGURATIONS 5-2
5.3.1 VMEbus Address Configuration 5-2
5.3.2 System Controller Configuration 5-2
5.4 SERIAL PORTS AND HARDWARE RESET 5-3

SECTION 6. MAINTENANCE

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMIVME-5620
INTELLIGENT HSD EMULATOR

TABLE OF CONTENTS (CONCLUDED)

LIST OF FIGURES

Figure		Page
3.1-1	HSD Master / Slave Interconnection	3-3
3.1-2	VMIVME-5620 External Function or Output Timing	3-4
3.1-3	VMIVME-5620 Input Data or Status Timing	3-4
3.1-4	VMIVME-5620 External Mode Timing	3-5
4.24.1-1	Input / Output Control Block	4-23
4.24.1-2	IOCB Status Word Format	4.25
4.24.2-1	Autoslave Control Block	4-27
4.24.4.2-1	IBL Mode Interconnection	4-31
5.3-1	VMIVME-5620 Jumper Locations	5-4

LIST OF TABLES

Table		Page
4.1-1	VMIVME-5620 Register Map	4-2
4.5-1	HSD Status Register Format	4-3
4.7-1	HSD Mode Control Register	4-8
4.8-1	HSD Activity Control Register Format	4-9
4.9-1	Extended Mode Register Format	4-11
4.9-2	SCON Time Codes	4-12
4.9-3	VMEbus Release Mode Code	4-13
4.10-1	IOCB Address Modifier Register	4-13
4.10-2	Common VMEbus Address Modifier Codes	4-14
4.13-1	VME Error Interrupt Control Register Format	4-15
4.14-1	HSD Error Interrupt Control Register	4-15
4.15-1	Transfer Complete Interrupt Control Register Format	4-16
4.16-1	Restart Interrupt Control Register Format	4-17
4.24.1-1	Valid Combinations of HSD Op Code Bits	4-24
4.24.4.2-1	IBL Functional Description of Control Signals	4-29

APPENDIX

A Assembly Drawing, Parts List, and Schematic

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-5620 is a DMA interface designed to be compatible with the VMEbus and the Encore HSD bus as defined by the Encore Model 9132 High-Speed-Data (HSD) interface, and the Encore Model 9136 Interbus Link (IBL).

The VMIVME-5620 is an Encore HSD-compatible HSD interface implemented on a double Eurocard. Two flat 50-conductor cables with socket connectors at both ends connect the VMIVME-5620 to the Encore HSD/IBL interface. The VMIVME-5620 includes these features:

32, 16, and 8-bit DMA transfers over HSD bus.
Executes commands from lists in memory by DMA.
HSD compatibility, as HSD Master or HSD Slave.
IBL compatibility, high or low priority.
VMEbus compatible (ANSI/IEEE STD 1014-1987 IEC 821 and 297).
A32:A24:A16:D32:D16:D8(EO) as VME Master.
A24:A16:D32:D16:D8(EO) as VME Slave.
VME-to-VME link using two boards.
250-foot maximum cable length.
Programmable interrupt vectors and level.
Programmable VMEbus address modifiers (data transfers).
Command Chaining.
Data Chaining.
Data Buffering (FIFOs).
4 Mbyte/sec transfer rate (VMIVME-5620 to VMIVME-5620).
Block Transfers.
Release on Request.
HSD External Mode support.
Front Panel Fail LED.
Jumper selectable slave address.

The data transfer rate is a strong function of cable length, and it depends on operating mode. Please refer to Encore Technical Manual Number 35-329-132-000 for details.

VMIC recommends that the cables be high-quality twisted-pair with overall shield, for lengths greater than 50 feet.

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-5620 is a high performance variable-width link between the VMEbus and the Encore HSD interface. The VMIVME-5620 uses an integrated VMEbus interface (Cypress VIC068), with an onboard local bus that includes a processor and

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

memory. In Master or Interbus Link (IBL) modes, the processor interprets an I/O Control List (IOCL), which is a list of host-based I/O Control Blocks (IOCB). The VMEbus interface provides variable-width host global memory access, and interrupts to the host interrupt handler.

The VMIVME-5620 can operate in the HSD Master mode. This is the mode used to drive HSD peripherals. It fully implements this mode, sending External Function Commands to the HSD peripheral device, receiving device status, and transferring data blocks to or from the device, all by interpreting an IOCL in VMEbus global memory. Further, it supports External Mode, which the HSD peripheral device controls addressing and data transfers to or from VMEbus global memory.

The VMIVME-5620 can operate in the Interbus Link (IBL) mode. This mode permits two HSD-compatible controllers, one of which may be an Encore HSD controller, to form a high speed link. The IBL mode reroutes some signals on the HSD interface so that a "crossed" cable is not necessary.

The VMIVME-5620 can operate in the HSD Slave mode, in which it behaves as if it were an HSD peripheral device. In the Slave mode, it receives External Function Commands and acts on them, subsequently receiving or transmitting data, and possibly providing device status. The Slave provides addresses to the Master, as well as determining data transfer timing and direction.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATION

REFER TO 800-005620-000 SPECIFICATION

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 3

THEORY OF OPERATION

3.1 OVERVIEW

The VMIVME-5620 is a D32:D16:D8(EO) VMEbus Slave for setup purposes. The VMEbus processor must set a number of items within the VMIVME-5620, such as interrupt vectors and masks. Most importantly, the processor must set up an address (pointer) to the first longword of an Input Output Control list (IOCL) of Input Output Control Blocks (IOCB). When the GO bit is set, the VMIVME-5620 autonomously executes commands from this list.

The VMIVME-5620 operates as a VMEbus Master while executing the IOCL. The address and data modes used as Master are under control of the user, during setup time.

The term "Command Chaining" refers to automatic execution of the next IOCB in the list, when the currently executing one finishes.

The term "Data Chaining" refers to a mode of command chaining wherein some of the opcode bits from the command field of the IOCB (HSD Op) are set only from the first IOCB in the data chain, rather than reloading from each IOCB.

As an HSD Slave, the VMIVME-5620 reacts to commands sent by a Master HSD, which could be another VMIVME-5620. There is an Autoslave mode, in which the VMIVME-5620 looks up address modes, buffer addresses, and word counts to use, based on the content of the DEVOP field in the External Function Word received from the Master HSD.

There are FIFO elements between the cable interface circuits and the VME circuits. These allow transfers on one end of a link to proceed (briefly) at full speed without waiting for bus access at the other end.

The cable interface is Encore HSD compatible. It supports transfers in both directions (FROM and INTO the VMIVME-5620), using Slave Mode, Encore/Gould External Mode, and IBL Mode. The Slave Configuration provides the necessary control line swapping that avoids the need to make a special cable to cross the lines to the HSD at the other end of the cable, and also alters the function of some of the control registers. The External Mode allows the device at the other end of the cable to control I/O address and direction. IBL mode provides a simple DMA link between two machines.

3.2 MASTER/SLAVE, INTERBUS LINK, AND EXTERNAL MODES

Figure 3.1-1 is a simplified diagram of the connection between an HSD Master and an HSD Slave (device). There are thirty-two (32) bi-directional data lines, seven (7) control lines driven by the Master, and eight (8) control lines driven by the Slave. The control lines are:

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Name	Driver	Description
IDTARDY	Slave	Input Data Ready. Negates on IDTAACK.
IDTAACK	Master	Input Acknowledge.
ODTARDY	Master	Output Data Ready. Negates on OUTACK.
OUTACK	Slave	Output Acknowledge.
EXTFCN	Master	External Function. Negates on EXTFACK.
EXTFACK	Slave	External Function Acknowledge.
STATRDY	Slave	Input Status Ready. Negates on STATACK.
STATACK	Master	Input Status Acknowledge.
LASTWFG	Master	Last Word Flag, with ODTARDY for last word.
DATAEOB	Slave	Device End of Block, with IDTAACK for last word.
DEVPRES	Slave	Device Present.
TERMDEV	Master	Terminate Device. Stops transfers.
EXTTERM	Slave	External Terminate. Stops transfers.
IORESET	Master	I/O Reset. Hardware reset sent to Slave.
EXTMODE	Slave	External Mode. Slave controls Master.

There are four handshake pairs in this list. From Master to Slave, EXTFACK answers EXTFCN, and OUTACK answers ODTARDY. From Slave to Master, STATACK answers STATRDY, and IDTAACK answers IDTARDY. Figures 3.1-2 and 3.1-3 show the timing relationships of these eight signals for data output and input, respectively. When the Master executes an IOCB that calls for a data transfer, an EXTFCN cycle occurs, followed by a number of IDTARDY or ODTARDY cycles. A Command Transfer IOCB causes two EXTFCN cycles, and a Device Status Request IOCB results in an EXTFCN cycle followed by a STATRDY cycle.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

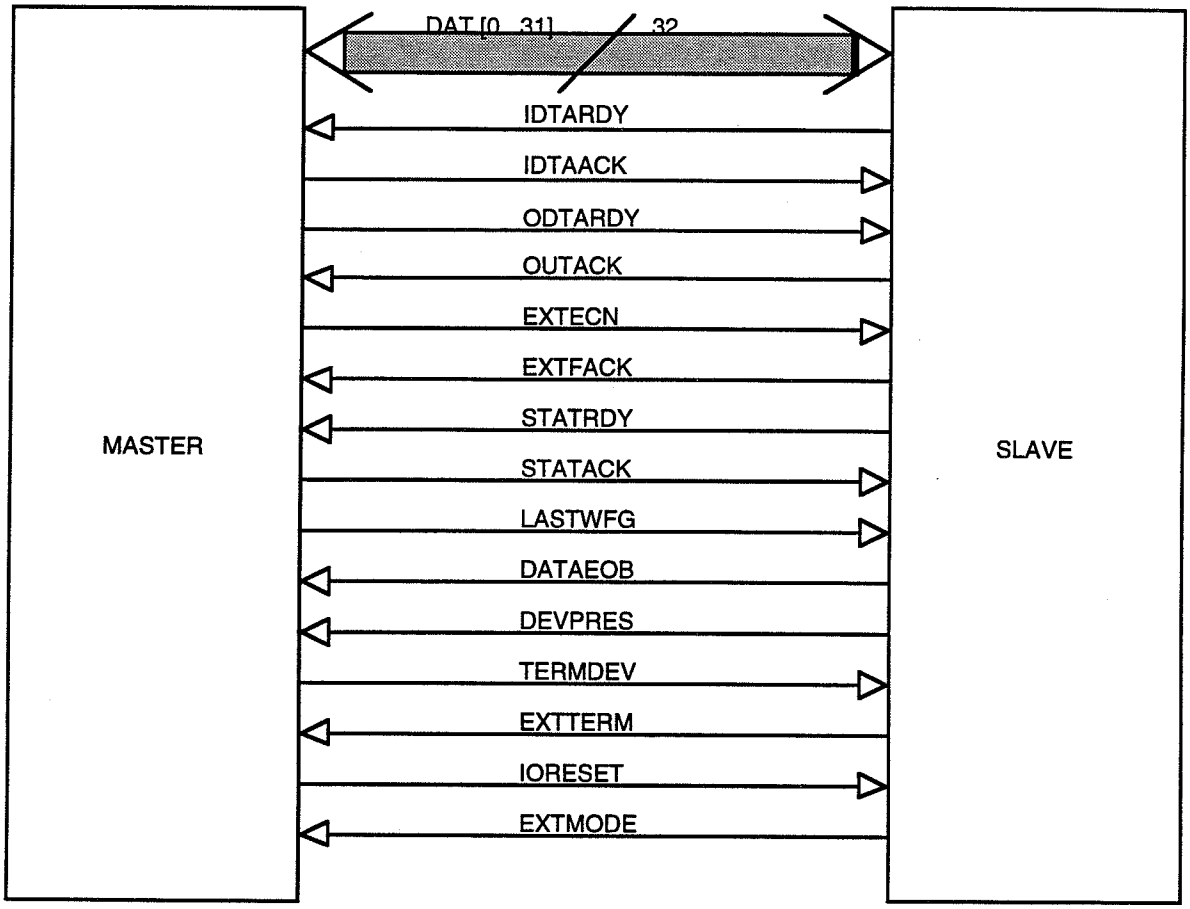


Figure 3.1-1 HSD Master / Slave Interconnection

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

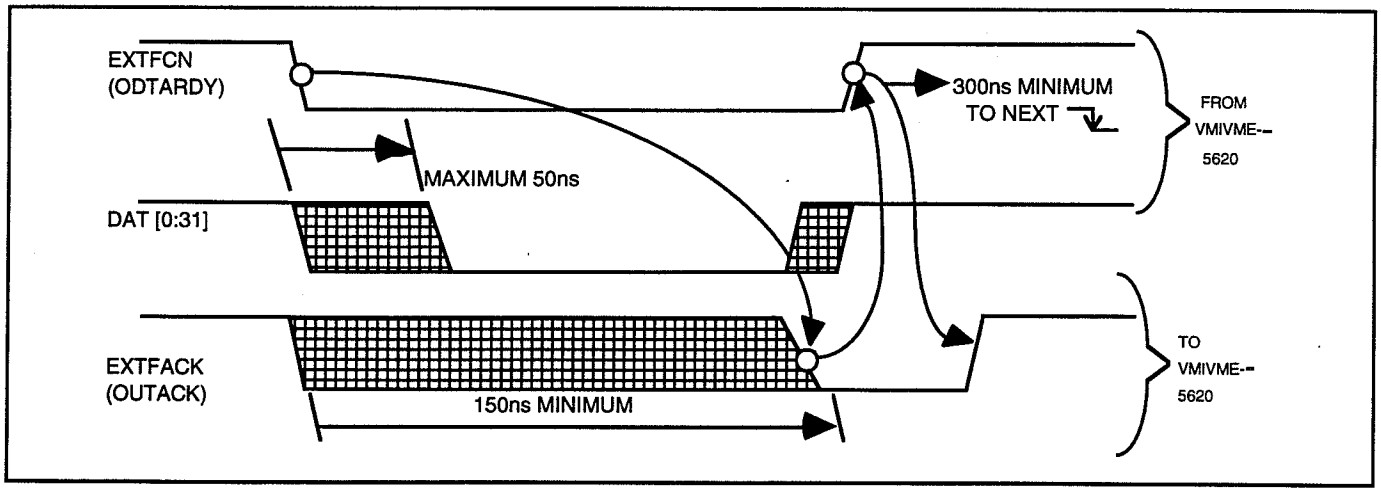


Figure 3.1-2 VMIVME-5620 External Function or Output Data Timing

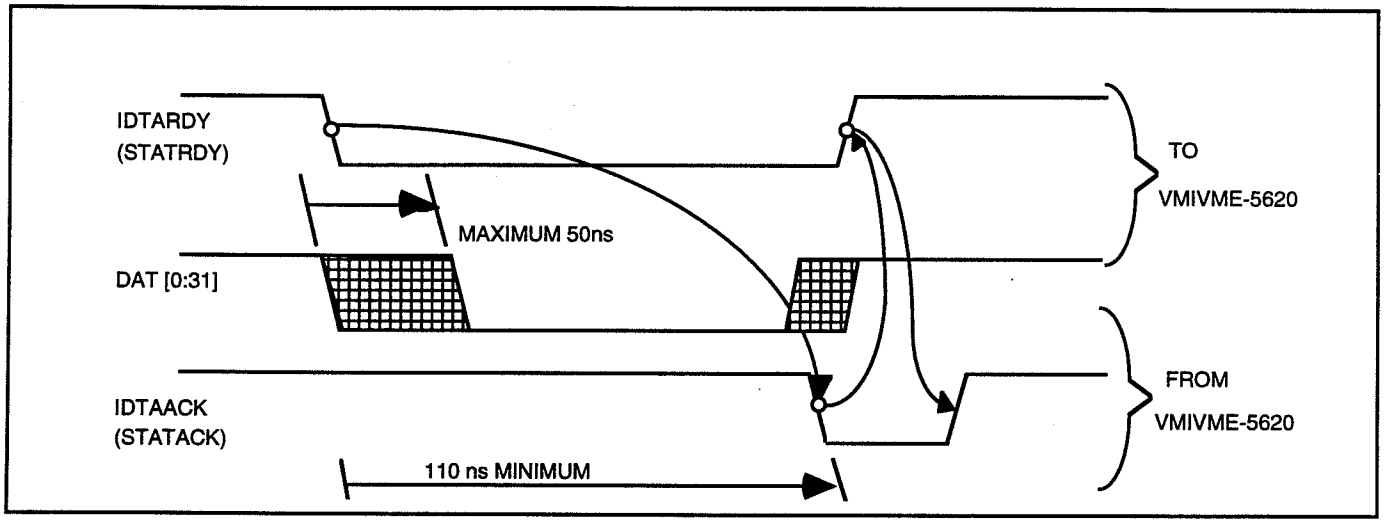


Figure 3.1-3 VMIVME-5620 Input Data or Status Timing

The LASTWFG may accompany an ODTARDY from the Master, or a DATAEOB may accompany an IDTARDY from the Slave. These conditions indicate that the current I/ODTARDY transfer is the last for this IOCB, regardless of the IOCB's transfer count.

DEVPRES is a level that informs the Master that the Slave is powered-up and functional. EXTMODE is a level that informs the Master that the Slave has received a Command Transfer that allows External Mode, and is acting in that capacity. Figure 3.1-4 shows the timing diagram for an External Mode transfer.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

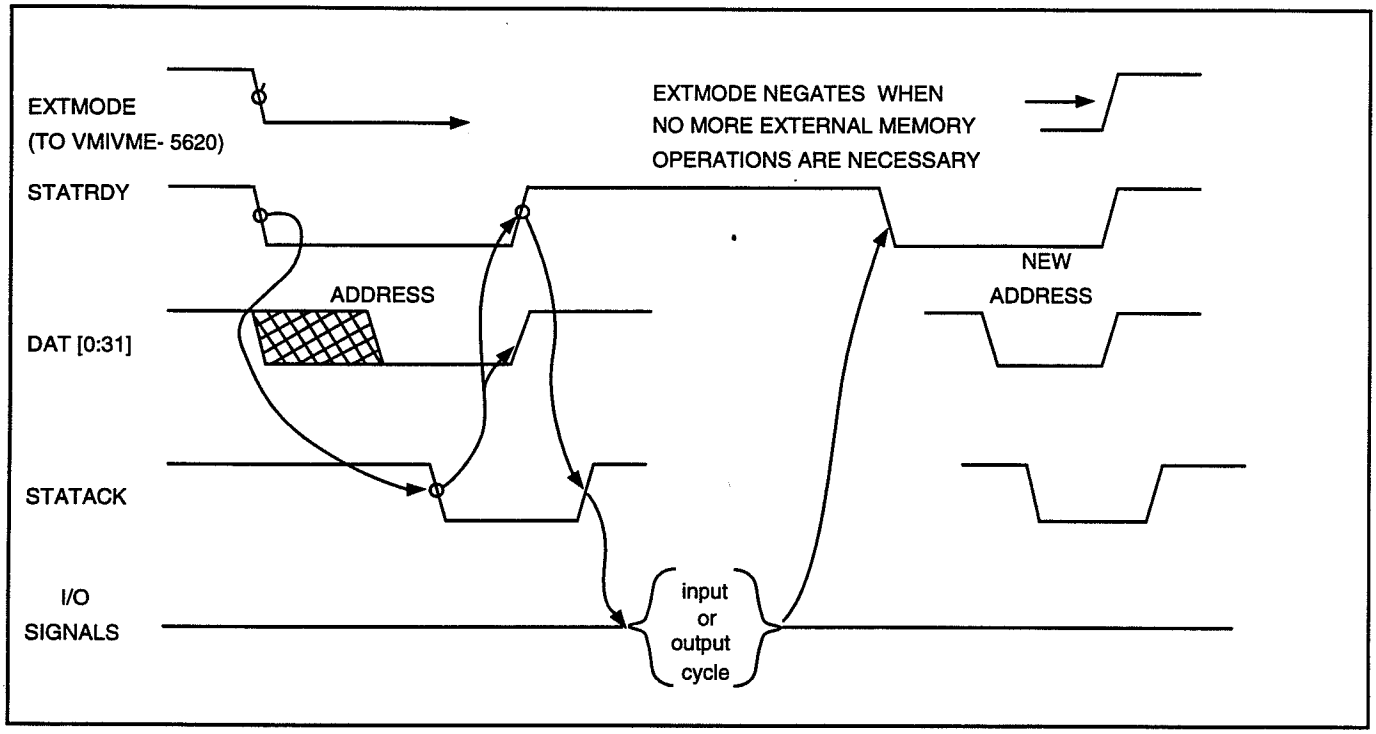


Figure 3.1-4 VMIVME-5620 External Mode Timing

EXTTERM, TERMDEV, and IORESET may occur asynchronously with respect to any other signal; they are pulses of between 300 nsec minimum and 600 nsec maximum.

Interbus Link (IBL) mode cable traffic consists entirely of Input Data or Output Data cycles. EXTTERM and TERMDEV serve a similar purpose as in Master/Slave mode. See Section 4.24.4 for details.

All the cable signals are handled with AM26S10 or equivalent open-collector transceivers. There is a 120 ohm pull-up resistor on each end of every signal line. Each signal has its own ground return line.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 4

PROGRAMMING

4.1 REGISTER MAP

The VMIVME-5620 has 24 registers of varying data widths as shown in the register map, Table 4.1-1, along with their recommended mnemonic names. These registers should generally be accessed according to the size indicated, but the registers will tolerate byte, word, longword, and unaligned access. Groups of smaller registers may be accessed as a larger data size: all four byte-wide Interrupt Vector Registers may be accessed together as a single longword, for example. Large registers such as the HSD Status Register may even be accessed as a sequence of bytes or words.

Software must initialize the IOCB Pointer Register, and it can read either address counter whenever the VMIVME-5620 is in the stopped state (not transferring data or commands over the HSD cables). Software must provide the command list that the VMIVME-5620 will execute, using the IOCB Pointer Register to access it directly. The width of commands and data transfers to and from memory is under control of on-board registers, and does not change while the VMIVME-5620 is executing commands from the list.

Table 4.1-1 is a partial map of the onboard registers. **Any bit or field shown as zero and/or reserved must be zero**. Figure 4.24.1-1 shows the format of the IOCB words used in Master Mode. Section 4.24.1 describes the VMIVME-5620 Master Mode activities directed by a list of IOCBs (IOCL), and Section 4.24.2 describes VMIVME-5620 Slave Mode functions, either semiautomatic or entirely managed by host software.

NOTE: For a short time after power-up, the VMIVME-5620 will not decode accesses from the VMEbus. This period is always less than twenty (20) milliseconds. After this time, on board self-diagnostic tests begin to run. These take approximately three (3) seconds, during which time the VMIVME-5620 decodes VMEbus accesses and shows hex $FF in the P.O.R self-test Status Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.1-1 VMIVME-5620 Register Map

OFFSET ADDRESS	DESCRIPTION	MNEMONIC	ACCESS	REF. SECTION
$00	Board ID Register	BID	Byte (R)	4.2
$01	P.O.R Self-Test Status Register	STFLAG	Byte (R)	4.3
$02	ROM Version Register	ROM_VER	Word (R)	4.4
$04	HSD Status Register	BST	Longword (R/W)	4.5
$08	Device Status Register	DVS	Longword (R/W)	4.6
$0C	HSD Mode Control Register	MOD	Byte (R/W)	4.7
$0D	HSD Activity Control Register	ACT	Byte (R/W)	4.8
$0E	Extended Mode Register	EMOD	Word (R/W)	4.9
$10	IOCB Address Modifier Register	CAM	Byte (R/W)	4.10
$11	Data Address Modifier Register	DAM	Byte (R/W)	4.11
$12	HSD Interface Time-out Register	TIM	Word (R/W)	4.12
$14	VME Error Interrupt Control Register	VEIC	Byte (R/W)	4.13
$15	HSD Error Interrupt Control Register	HEIC	Byte (R/W)	4.14
$16	Transfer Complete Interrupt Control Register	TCIC	Byte (R/W)	4.15
$17	Restart Interrupt Control Register	RSIC	Byte (R/W)	4.16
$18	VME Error Interrupt Vector Register	VEIV	Byte (R/W)	4.17
$19	HSD Error Interrupt Vector Register	HEIV	Byte (R/W)	4.17
$1A	Transfer Complete Interrupt Vector Register	TCIV	Byte (R/W)	4.17
$1B	Restart Interrupt Vector Register	RSIV	Byte (R/W)	4.17
$1C	Residual Transfer Count Register	RXC	Longword (R/W)	4.18
$20	IOCB Pointer Register	CBP	Longword (R/W)	4.19
$24	External Function Word Register	EFW	Longword (R/W)	4.20
$28	Data Pointer Register	DBP	Longword (R/W)	4.21
$2C	Board Status Pointer Register	BSP	Longword (R/W)	4.22

4.2 BOARD ID REGISTER (BID)

The Board ID Register is a read-only byte register at offset $00. It will always contain the value $1E, the VMIVME-5620 board identification code.

4.3 P.O.R. SELF-TEST STATUS REGISTER (STFLAG)

The P.O.R. Self-Test Status Register is a read-only byte register at offset $01. Upon power-up or VMEbus system reset, the VMIVME-5620 processor runs a self-diagnostic and reports the results to the BST Register. A value of $FF indicates the board is still busy with its self test, while a value of $00 indicates the test is complete. When the value is $FF, the board should be considered non-functional; the only registers containing valid data besides this one are the Board ID Register and the ROM Version Register. Once the register is clear, the board functions normally and all other registers are valid.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.4 ROM VERSION REGISTER (ROM_VER)

The ROM Version Register is a read-only word register at offset $02. The value in this register represents the revision number of the onboard firmware as four four-bit BCD digits.

4.5 HSD STATUS REGISTER (BST)

The HSD Status Register is a read/write longword at offset $04. The definition of this register is shown in Table 4.5-1. Note that nearly every bit in this register has a unique meaning and function as described below.

Table 4.5-1 HSD Status Register Format

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Any Error	External Terminate	Slave Reset	Time-out Error	VMEbus Error	Hardware Error	Reserved Field Non-Zero	Device Present

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
External Function Word Received	Autoslave Function Complete	Last Word Flag / Device End of Block	Transfer Count Complete	Self Test Failed	Self Test Busy	IBL Link Active	IBL Link Ready

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Illegal IOCB	Running	HSD Protocol Error	VME System Controller	IOCB Complete	Register Busy	Master in External Mode	0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receive FIFO Not Empty	Receive FIFO Full	Transmit FIFO Not Empty	Transmit FIFO Full	Port A Status Bit 1	Port A Status Bit 0	Port B Status Bit 1	Port B Status Bit 0

NOTE:

IF THE USER HAS SELECTED A VMEbus BLOCK TRANSFER MODE (HEX AM CODE = $0B, $0F, $3B, OR $3F) IN EITHER THE IOCB ADDRESS MODIFIER (CAM) OR THE DATA ADDRESS MODIFIER (DAM) REGISTERS, THE HOST MUST USE THE BSP REGISTER, WHEN POLLING FOR HSD STATUS IS NECESSARY, OR DATA CORRUPTION MAY OCCUR DURING DMA DATA TRANSFERS. THE HOST MUST NOT ACCESS ANY VMIVME-5620 REGISTER DURING VMEbus BLOCK TRANSFERS.

Bits 0-3: Port Status

These are the status bits for the two onboard RS-232 serial ports. Each port has an associated two-bit code, of which there are three valid states. A value of 11 indicates the port has failed testing and is unusable. A value of 01 indicates either that a terminal is connected properly or that the port is unconnected. A value of 00 indicates the port has been looped back on itself (default configuration).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 4: Transmit FIFO Full

This bit, if a one, indicates that the Transmit FIFO (the one that sends data from the VMIVME-5620 to the cable) is full. No more data can be sent until the device on the other end of the cable accepts some data. This bit is meaningful only when the VMIVME-5620 is stopped (GO, RUNNING, and Master-in-External-Mode bits are all zeros).

Bit 5: Transmit FIFO Not Empty

This bit, if a one, indicates that the Transmit FIFO (the one that sends data from the VMIVME-5620 to the cable) is not empty. This means that data is waiting for the device on the other end of the cable to accept it. This bit is meaningful only when the VMIVME-5620 is stopped (GO, RUNNING, and Master-in-External-Mode bits are all zeros).

Bit 6: Receive FIFO Full

This bit, if a one, indicates that the Receive FIFO (the one that accepts data from the cable into the VMIVME-5620) is full. No more data can be accepted until the VMIVME-5620 processes some incoming data. This bit is meaningful only when the VMIVME-5620 is stopped (GO, RUNNING, and Master-in-External-Mode bits are all zeros).

Bit 7: Receive FIFO Not Empty

This bit, if a one, indicates that the Receive FIFO (the one that accepts data from the cable into the VMIVME-5620) is not empty. This means that data that came from the device on the other end of the cable is waiting to be processed. This bit is meaningful only when the VMIVME-5620 is stopped (GO, RUNNING, and Master-in-External-Mode bits are all zeros).

Bit 8: Reserved

This bit is always clear.

Bit 9: Master in External Mode

This bit, if a one, indicates that the VMIVME-5620 is in Master Mode with External Mode enabled, and the device at the other end of the cable is asserting the EXTMODE signal.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 10: Register Busy

A write operation into the Activity Control Register (ACT) is serviced by a firmware interrupt on the VMIVME-5620. Until the VMIVME-5620 firmware interprets the new data, the contents of the ACT Register may not reflect the expected results. BST bit ten (Register Busy) provides a handshake method that allows the host computer software to ensure that the ACT contents have taken effect. The following code fragment illustrates the proper technique of altering the ACT registers.

```
/*
 * ....................................................
 *  Sample code fragment to set the GO bit.
 * ....................................................
 */

while((v5620->bst & REGBUSY) != 0);   /* let previous finish */
v5620-> bst |= REGBUSY;               /* Avoid races         */
v5620-> act |= 1;                     /* Set GO bit          */
```

The following code fragment may be used when reading the ACT register:

```
/*
 * ....................................................
 * Sample code fragment to read the ACT register and
 * print a message if the led is on
 * ....................................................
 */

while((v5620->bst & REGBUSY)!= 0);    /*let previous finish  */
if (v5620->bst & LED) puts ( "The LED is ON" );
```

NOTE: The above handshake applies only to the ACT register; the remaining VMIVME-5620 registers may be written and read at will. However, if other register contents are changed while RUNNING is a one, the effect is unpredictable.

Bit 11: IOCB Complete

This bit indicates that an IOCB has completed.

Bit 12: VME System Controller

This bit is set if the VMIVME-5620 board is configured as a VMEbus slot 1 controller. See section 5.3.2 for details.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 13: HSD Protocol Error

If set, this bit indicates an HSD Protocol Error (wrong HSD cable cycle). If this bit is set, the Any Error bit (bit 31) will be set also.

Bit 14: Running

If this bit is set, the VMIVME-5620 is busy performing HSD activities.

Bit 15: Illegal IOCB

This bit is set if an illegal IOCB is encountered during execution of an IOCL. If this bit is set, the Any Error bit (bit 31) will be set as well.

Bit 16: IBL Link Ready

This bit is set when the VMIVME-5620 has established an IBL link connected to another HSD and is ready for transfers. See Section 4.24.4 for IBL mode details.

Bit 17: IBL Link Active

This bit is set when another HSD connected to this VMIVME-5620 has established an IBL link and is ready for transfers. See Section 4.24.4 for IBL mode details.

Bit 18: Self Test Busy

This bit is set when the VMIVME-5620 is busy running one of the tests controlled by the Test Bit of the HSD Mode Control Register. After initializing these tests, the host program should wait for this bit to clear before testing the Self Test Failed bit in this register to determine the success of the self tests.

Bit 19: Self Test Failed

This bit is set if any of the self tests controlled by the Test Bit of the HSD Activity Control Register have failed. This bit is not valid if the Self Test Busy bit is set. If this bit is set, the Any Error bit (bit 31) will also be set.

Bit 20: Transfer Count Complete

This bit is set when the VMIVME-5620 completes a transfer due to the transfer count field of the IOCB decrementing to zero.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 21: Last Word Flag / Device End of Block

This bit is set when an HSD transfer is completed due to the Last Word Flag being received when receiving or the Device End of Block being received when transmitting.

Bit 22: Autoslave Function Complete

This bit is set when an autoslave table entry has been completed.

Bit 23: External Function Word Received

This bit is set when an External Function Word has been received from another HSD, when this HSD is in Slave Mode.

Bit 24: Device Present

This bit indicates the slave device is present when this unit is in Master Mode, or that the other HSD is present when this unit is in IBL mode.

Bit 25: Reserved Field Non-Zero

This bit is set if any reserved bits in any VMIVME-5620 registers are non-zero. If this bit is set, the Any Error bit (bit 31) will also be set. Note that the unused register space from offset $30 to offset $3F is also reserved and must be completely clear. All reserved bits are clear by default after power-up or reset.

Bit 26: Hardware Error

If this bit is set, some local hardware error other than a VMEbus Error (BERR) has occurred. If this bit is set, the Any Error bit (bit 31) will be set as well.

Bit 27: VMEbus Error

This bit is set if a VMEbus Error has occurred. Note that the VMIVME-5620 does not have a bus timer unless it is configured as the system controller (see Section 5.3.2 for details), and thus cannot trigger a bus error itself. The bus error signal (BERR*) must be asserted by some other VMEbus device. This bit will also be set, however, if a VMIVME-5620 DMA transfer points to the VMIVME-5620 board. If this bit is set, the Any Error bit (bit 31) will be set as well.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 28: Timeout Error

If this bit is set, an HSD interface Timeout error has occurred. The amount of time allowed is controlled by the value in the HSD Interface Timeout Register. Since this kind of error is generally caused by a problem at the other end of the cable, the Any Error bit is NOT set with this bit.

Bit 29: Slave Reset

This bit is set when the other master HSD device has sent an I/O reset.

Bit 30: External Terminate

This bit is set when the other HSD device has terminated early.

Bit 31: Any Error

This bit is set whenever one or more of the following bits are set: HSD Protocol Error, Illegal IOCB, Self Test Failed, Reserved Field Non-Zero, Hardware Error, or VMEbus Error. It is clear only if all the aforementioned bits are clear.

4.6 DEVICE STATUS REGISTER (DVS)

The Device Status Register is a read/write longword at offset $08. It contains the most recently requested device status.

4.7 HSD MODE CONTROL REGISTER (MOD)

The HSD Mode Control Register is a read/write byte at offset $0C. Every bit in this register has a unique function as shown in Table 4.7-1 below.

Table 4.7-1 HSD Mode Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IBLHI PRI	Master	IBL MODE	Last Word Flag Enable	External Function Word Hold	Autoslave	Bus Request Level Bit 1	Bus Request Level Bit 2

Bits 0 & 1: Bus Request Level

This bit pair controls the VMEbus bus request level for the VMEbus DMA accesses during transfers. The default value is binary 11, indicating a bus request level of 3, the highest value available.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 2: Autoslave

When set, this bit enables autoslave mode. See Section 4.24.2 for details.

Bit 3: External Function Word Hold

When set, this bit causes the master to wait for the slave to accept the next external function word before transmitting any further data.

Bit 4: Last Word Flag Enable

When set, this bit enables the HSD last word flag feature. When this feature is enabled, a Last Word Flag signal will accompany the Output Data Ready signal when the last word is sent.

Bit 5: IBLMODE

This bit should be a zero for normal operations and a one to enable IBL operations.

Bit 6: Master

When set, this bit causes the VMIVME-5620 to act as an HSD Master.

Bit 7: IBLHIPRI

This bit has meaning only if the MOD Register IBLMODE bit is set to a one. If IBLHIPRI is set to a one, IBL transfers are performed at a high priority.

4.8 HSD ACTIVITY CONTROL REGISTER (ACT)

The HSD Activity Control Register is a read/write byte at offset $0D. Every bit of this register has a unique function as shown in Table 4.8-1.

Table 4.8-1 HSD Activity Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Terminate Device / External Terminate	REQ IBL	Test	Reset I/O Device	Reset HSD Interface	Clear Status Register	LED Control	GO

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 0: GO

Normally, setting this bit causes the activity indicated by the HSD Mode Control Register to begin. When executing self-tests, this bit has a different function. See Section 4.24.6 for details concerning self-testing.

Bit 1: LED Control

When this bit is set, the LED on the front panel will be on. Clear this bit to turn the LED off. The LED is off after the power-up (or reset) self-tests complete successfully. (The LED flashes on and off during these self-tests).

Bit 2: Clear Status Register

Setting this bit causes the HSD Status Register to return to its default state of all clear (except possibly for the Reserved Field Non-Zero and Device Present bits). This bit will not remain set, but will be read as clear.

Bit 3: Reset HSD Interface

Setting this bit causes the VMIVME-5620 to reset the HSD interface. The bit will not remain set, but will read as clear. The HSD interface logic will revert to its idle (waiting) state, and the FIFOs will be cleared.

Bit 4: Reset I/O Device

Setting this bit causes the I/O device to be reset by sending it an IORESET signal. The bit will not remain set, but will read as clear.

Bit 5: Test

When the Test Bit is set to one, the VMIVME-5620 performs a self-test as detailed in Section 4.24.6 of this document.

Bit 6: REQIBL

The REQIBL bit has a function only if the MOD Register IBLMODE bit is set. If the REQIBL Bit is set to one, the VMIVME-5620 will request the IBL Link. See Section 4.24.4 for IBL mode details.

Bit 7: Terminate Device / External Terminate

In Slave mode, setting this bit causes an EXTTERM signal to be sent to the Master. If the VMIVME-5620 is the Master, setting this bit sends a TERMDEV to the Slave.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.9 EXTENDED MODE REGISTER (EMOD)

The Extended Mode Register is a read/write word at offset $0E. The bits in this register effectively function as extensions to the HSD Mode Control Register and are defined according to Table 4.9-1 below.

Table 4.9-1 Extended Mode Register Format

Bits 15 & 14	Bits 13-11	Bit 10-9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bits 3-0
VMEbus Release Mode	SCON Mode VMEbus Timeout	00	Input LWF	Arbiter Mode	External Mode	Fast Mode	Warp Mode	VMEbus Fairness Timeout

Bits 0-3: VMEbus Fairness Timeout

The value in this bit field determines how many 2 µsecond intervals, if any, the VMIVME-5620 will wait before asserting its VMEbus request, if another VME master is already using the bus. This fair-request scheme of bus arbitration avoids the bus starvation that can occur when multiple bus masters exist, especially multiple masters at the same priority level. A value of zero here will disable the fairness time-out and a value of binary 1111 will cause the VMIVME-5620 to wait indefinitely for the other bus master to relinquish control. Note that the actual time-out value may be up to 2 µseconds longer than programmed. The default value for this field is $2, indicating a 4 µsecond time-out.

Bit 4: Warp Mode

When this bit is set, the HSD transfer speed is set to Warp Mode. Note that Warp Mode is unique to the VMIVME-5620 and may only be used between two such VMIVME-5620 units. This provides a faster non-HSD cable protocol for either Master/Slave or IBL configurations.

Bit 5: Fast Mode

When this bit is set, the HSD transfer speed is set to Fast Mode, wherein the settling time for HSD transfers is slightly reduced, allowing a higher transfer rate. Fast Mode transfers should only be attempted with short HSD cables.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bit 6: External Mode

When this bit is set to a one, and the VMIVME-5620 is in Slave Mode, the VMIVME-5620 can perform External Mode cycles, which control all cable activity. If the VMIVME-5620 is in Master Mode, the unit will ignore External Mode cycles from the Slave unless this bit is set to a one. See Sections 3.2 and 4.24.5 for details concerning External Mode

Bit 7: Arbiter Mode

This bit has no effect unless the VMIVME-5620 is in the VMEbus slot one as the controller and the SCON jumper is installed (see section 5.3.2 for details). If the VMIVME-5620 is the system controller, a zero in this bit will cause the VMIVME-5620 to use a round robin arbitration scheme, while a one will cause it to use a prioritized arbitration scheme.

Bits 8: Input LWF

When this bit is set to a one (1), the VMIVME-5620 will send the Last Word Flag (LASTWFG) signal along with the Input Data Acknowledge (IDTAACK) signal for the last expected transfer cycle. This feature, when enabled, causes the VMIVME-5620 to accept data from the HSD cable much more slowly than otherwise; therefore, it should not be used unless the device on the other end of the cable requires it.

Bits 9-10: Reserved

Bits 11-13: SCON Mode VMEbus Time-out

When the VMIVME-5620 is system controller, the maximum allowed time before a BUS ERROR signal is issued before a DTACK occurs is set by this field. The maximum time is coded as shown in Table 4.9-2.

Table 4.9-2 SCON Time Codes

BIT 11-13	TIME (NOMINAL)
000	4 Microseconds
001	16 Microseconds
010	32 Microseconds
011	64 Microseconds
100	128 Microseconds
101	256 Microseconds
110	512 Microseconds
111	INFINITE

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bits 14 & 15: VMEbus Release Mode

This bit pair determines the VMEbus Release Mode when the VMIVME-5620 is the bus Master. The Release Mode may be chosen according to Table 4.9-3.

Table 4.9-3 VMEbus Release Mode Code

Bit 15	Bit 14	Release Mode
1	1	Bus Capture and Hold
1	0	Release on BCLR*
0	1	Release when Done
0	0	Release on Request

The default value for this field is binary 00, indicating Release on Request mode.

4.10 IOCB ADDRESS MODIFIER REGISTER (CAM)

The IOCB Address Modifier Register is a read/write byte at offset $10. This register contains the information needed to fetch IOCB contents directly from VMEbus memory during IOCB execution. The most significant two bits contain a two-bit code representing the data width of the VMEbus access according to Table 4.10-1. The least significant six bits directly correspond to the VMEbus address modifier (AM) bits AM5-AM0, bit 5 corresponding to AM5 through bit 0 corresponding to AM0. Typical VMEbus address modifier values are listed in Table 4.10-2.

Table 4.10-1 IOCB Address Modifier Register

Bit 7	Bit 6	Transfer Size	Bits 5-0
0	1	Byte (8 bits)	(See Table 4.10-2)
1	0	Word (16 bits)	
0	0	Longword (32 bits)	

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.10-2 Common VMEbus Address Modifier Codes

HEX AM Code	ACCESS TYPE AND MODE
$09	Extended (A32) non-privileged data
$0A	Extended (A32) non-privileged program
$0B	Extended (A32) non-privileged block transfer
$0D	Extended (A32) supervisory data
$0E	Extended (A32) supervisory program
$0F	Extended (A32) supervisory block transfer
$29	Short I/O (A16) non-privileged data
$2D	Short I/O (A16) supervisory data
$39	Standard (A24) non-privileged data
$3A	Standard (A24) non-privileged program
$3B	Standard (A24) non-privileged block transfer
$3D	Standard (A24) supervisory data
$3E	Standard (A24) supervisory program
$3F	Standard (A24) supervisory block transfer

The power-up/reset default value for the IOCB Address Modifier Register is $B9, indicating standard A24 non-privileged VMEbus addressing using 16-bit transfers.

NOTE:

IF THE USER HAS SELECTED A VMEbus BLOCK TRANSFER MODE (HEX AM CODE = $0B, $0F, $3B, OR $3F) IN EITHER THE IOCB ADDRESS MODIFIER (CAM) OR THE DATA ADDRESS MODIFIER (DAM) REGISTERS, THE HOST MUST USE THE BSP REGISTER, WHEN POLLING FOR HSD STATUS IS NECESSARY, OR DATA CORRUPTION MAY OCCUR DURING DMA DATA TRANSFERS. THE HOST MUST NOT ACCESS ANY VMIVME-5620 REGISTER DURING VMEbus BLOCK TRANSFERS.

4.11 DATA ADDRESS MODIFIER REGISTER (DAM)

The Data Address Modifier Register is a read/write byte at offset $11. This register has exactly the same format as the IOCB Address Modifier Register (see section 4.10). It functions similarly as well, the only difference being that this register's contents are used to access data buffers over the VMEbus, and not I/O Control Lists. This register defaults to a value of $39 (standard A24 non-privileged VMEbus addressing using 32-bit transfers). If the DAM contains one of the block transfer codes, the VMIVME-5620 will use VMEbus block transfers to transmit or receive data buffers, unless the Input LWF bit is set in the EMOD register and/or External Mode is active.

4.12 HSD INTERFACE TIMEOUT REGISTER (TIM)

The HSD Interface Timeout Register is a read/write word at offset $12. This register contains a value in milliseconds for which the VMIVME-5620 will wait for an HSD transfer to be completed. If this time limit is exceeded, a Timeout error will occur and the Timeout Error bit of the HSD Status Register will be set (see Section 4.5). If this register contains all zeros, the timeout value is infinite.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.13 VME ERROR INTERRUPT CONTROL REGISTER (VEIC)

The VME Error Interrupt Control Register is a read/write byte at offset $14. See Table 4.13-1 for the format of this register.

Table 4.13-1 VME Error Interrupt Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2-0
Interrupt Mask	0	0	Bus Error	Hardware Error	VMEbus Interrupt Level

Bits 0-2: VMEbus Interrupt Level

These three bits set the level of the error interrupt from 1-7. If all three bits are clear, the interrupt is effectively disabled since there is no VMEbus level 0 interrupt.

Bit 3: Hardware Error

If this bit is set, a hardware error can trigger this interrupt.

Bit 4: Bus Error

If this bit is set, a VMEbus error can trigger this interrupt.

Bits 5 & 6: Reserved

These bits must remain clear.

Bit 7: Interrupt Mask

Set this bit to disable any error interrupts. If this bit is clear, any errors whose corresponding bits in this register are set will cause an interrupt at the level indicated by the least significant bits of this register.

4.14 HSD ERROR INTERRUPT CONTROL REGISTER (HEIC)

The HSD Error Interrupt Control Register is a read/write byte at offset $15. See Table 4.14-1 for the formatting of this register.

Table 4.14-1 HSD Error Interrupt Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2-0
Interrupt Mask	Bad IOCB Error	Protocol Error	External Terminate	Timeout Error	VMEbus Interrupt Level

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bits 0-2: VMEbus Interrupt Level

These three bits that set the level of the HSD error interrupt from 1-7. If all three bits are clear, the interrupt is effectively disabled since there is no VMEbus level 0 interrupt.

Bit 3: Timeout Error

If this bit is set, an HSD Time-out Error will trigger this interrupt.

Bit 4: External Terminate

If this bit is set, an External Terminate from an HSD device will trigger this interrupt.

Bit 5: Protocol Error

If this bit is set, an HSD Protocol Error will trigger this interrupt.

Bit 6: Bad IOCB Error

If this bit is set, a Bad IOCB Error will trigger this interrupt.

Bit 7: Interrupt Mask

Set this bit to disable any error interrupts. If this bit is clear, any errors whose corresponding bits in this register are set will cause an interrupt at the level indicated by the least significant bits of this register.

4.15 TRANSFER COMPLETE INTERRUPT CONTROL REGISTER (TCIC)

The Transfer Complete Interrupt Control Register is a read/write byte at offset $16 as shown in Table 4.15-1.

Table 4.15-1 Transfer Complete Interrupt Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2-0
Interrupt Mask	External Function Word Received	Autoslave Complete	Last Word Flag / Device End of Block	Transfer Count Complete	VMEbus Interrupt Level

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bits 0-2: VMEbus Interrupt Level

These three bits that set the level of the transfer complete interrupt from 1-7. If all three bits are clear, the interrupt is effectively disabled since there is no VMEbus level 0 interrupt.

Bit 3: Transfer Count Complete

If this bit is set, the interrupt will be triggered when a transfer ends due to the Transfer Count completing.

Bit 4: Last Word Flag / Device End of Block

If this bit is set, the interrupt will be triggered when the Last Word Flag is sent (Master Mode) or a device end of block is received (Slave Mode).

Bit 5: Autoslave Complete

If this bit is set, the interrupt will be triggered when an Autoslave Table Entry has been completed.

Bit 6: External Function Word Received

If this bit is set, the interrupt will be triggered whenever an External Function Word is received.

Bit 7: Interrupt Mask

Set this bit to disable any Transfer Complete Interrupts. If this bit is clear, any conditions whose corresponding bits in this register are set will cause an interrupt at the level indicated by the least significant bits of this register.

4.16 RESTART INTERRUPT CONTROL REGISTER (RSIC)

The Restart Interrupt Control Register is a read/write byte at offset $17. See Table 4.16-1 for the format of this register.

Table 4.16-1 Restart Interrupt Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2-0
Interrupt Mask	Link Ready	Link Active	IOCB Done	Slave Reset	VMEbus Interrupt Level

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Bits 0-2: VMEbus Interrupt Level

These three bits set the level of the error interrupt from 1-7. If all three bits are clear, the interrupt is effectively disabled since there is no VMEbus level 0 interrupt.

Bit 3: Slave Reset

If this bit is set, a Slave Reset will trigger this interrupt.

Bit 4: IOCB Done

If this bit is set, this interrupt will be triggered whenever an IOCB Is completed.

Bit 5: Link Active

If this bit is set, and the unit is in IBL Mode, the interrupt will be triggered when the IBL arbitration logic assigns the link to the other unit.

Bit 6: Link Ready

If this bit is set, and the unit is in IBL Mode, the interrupt will be triggered when the IBL arbitration logic assigns the link to this unit.

Bit 7: Interrupt Mask

Set this bit to disable any restart interrupts. If this bit is clear, any errors whose corresponding bits in this register are set will cause an interrupt at the level indicated by the least significant bits of this register.

4.17 INTERRUPT VECTOR REGISTERS (VEIV, HEIV, TCIV, RSIV)

There are four byte-wide read/write interrupt vector registers at offsets $18, $19, $1A, and $1B for the VME Error Interrupt Vector, HSD Error Interrupt Vector, Transfer Complete Interrupt Vector, and the Restart Interrupt Vector, respectively. These registers should be initialized to hold standard VMEbus interrupt vectors for their corresponding interrupts.

4.18 RESIDUAL TRANSFER COUNT REGISTER (RXC)

The Residual Transfer Count Register is a read/write longword at offset $1C. This register contains a single integer representing the number of transfers remaining for an IOCB or autoslave table entry.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.19 IOCB POINTER REGISTER (CBP)

The IOCB Pointer Register is a read/write longword at offset $20. This pointer should be initialized to hold the address of the first IOCB in the first IOCL. The value will be incremented as the VMIVME-5620 executes the IOCL. The contents of the IOCB Address Modifier Register are also used to determine access type when addressing the IOCB, possibly causing some of the most significant bits of this register to be ignored. For example, during VMEbus standard A24 addressing, the most significant byte of this register is ignored.

4.20 EXTERNAL FUNCTION WORD REGISTER (EFW)

The External Function Word Register is a read/write longword at offset $24. This register contains the External Function Word last sent (Master Mode), or last received (Slave Mode).

4.21 DATA POINTER REGISTER (DBP)

The Data Pointer Register is a read/write longword at offset $28. This register contains the VMEbus address for the current data buffer. The contents of the Data Address Modifier Register are also used to determine access type when addressing the data buffers, possibly causing some of the most significant bits of this register to be ignored. For example, during VMEbus standard A24 addressing, the most significant byte of this register is ignored.

4.22 BOARD STATUS POINTER REGISTER (BSP)

The Board Status Pointer Register is a read/write longword at offset $2C. This register contains the address of the image of the HSD Status Register maintained by the VMIVME-5620 in the same VMEbus memory space used for the IOCL. If the BSP is non-zero, the image is updated along with the HSD Status Register, so its value is always current. The BSP should be used whenever host software needs to poll the HSD status repeatedly, since polling the image does not interrupt and slow down the VMIVME-5620 internal firmware.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.23 AUTOMATIC CLEARING of STATUS BITS IN BST REGISTERS

Whenever an IOCB begins to execute (Master or IBL modes), or when an EFW arrives in Slave mode, the following BST status bits clear automatically:

Protocol Error.
Illegal IOCB (Bad HSD Op).
IOCB Complete.
Any of Protocol Error, Illegal IOCB, Self test failure,
Reserved field Non-Zero, Hardware Error, or VMEbus Error.
Last Word Flag / Device End of Block.
External Terminate.
Transfer Count Complete.
Autoslave Function Complete.
Slave Reset (by signal from Master).
HSD Interface Time Out (time in TIM register exceeded).
VMEbus Error (no VMEbus DTACK* signal).
Hardware Error (FIFO overflow, for example).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.24 PROGRAMMING DETAILS

4.24.1 General Programming For A Data Transfer, Master Mode

The VMIVME-5620 can perform a number of data transfers in automatic sequence. These may be any mix of input and output transfers, but must all be for the same VME address space, and all be of the same width (byte, word, or longword). The program must set up a list of commands to do (an IOCL), and then load the VMIVME-5620 onboard registers with information about how to execute the list.

The IOCL consists of one or more IOCBs (see Figure 4.24.1-1 for the IOCB format). The eight most significant bits of Word 0 of any IOCB are the operational code (HSD Op) that the VMIVME-5620 interprets. Table 4.24.1-1 shows the valid combinations of bits in the VMIVME-5620 HSD Op. The bits in this code are as follows:

31 I/O Direction — A 1 means input (HSD cable to VMEbus); a 0 means output (VMEbus to HSD cable). Data are taken from or stored into a buffer pointed to by the second word of the IOCB(Word 1).

30 Command Xfer — If set to 1: The data to be transferred are the first two words of the IOCB itself (Words 0 and 1). External Function handshaking is used on the HSD interface, rather than normal data handshaking. There is no other data transfer, and the direction is always VMEbus-to-HSD-cable, regardless of the state of bit 31.

29 Device Status — If set to 1: The device asserts Input Status Ready (STATRDY), and the VMIVME-5620 stores the presented status in the data buffer (pointed at by Word 1). There is no other data transfer, and the direction is always HSD-cable-to-VMEbus, regardless of the state of bit 31.

28 Cont On Err — If set to 1: If either command or data chaining is in effect (bits 25 and 24), a VMEbus Error (BERR*) will cause status to be stored in the last word of the IOCB (Word 3), and the VMIVME-5620 will start working on the next IOCB in the list.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

27	Int on EOB	If set to 1: When the transfer specified by the IOCB is complete at the destination (FIFO empty and no words left to transfer), the VMIVME-5620 generates a VMEbus interrupt as specified by vector and level registers.
26	Xfer in Chan	If set to 1: The VMIVME-5620 uses the address in the second word of the IOCB (Word 1) to point to a new IOCB, and then proceeds to load and interpret that. No data transfer takes place.
25	Command Chain	If set to 1: When the other functions specified by the current IOCB are done, the VMIVME-5620 increments the IOCB address to point to the word immediately following the last word of the current IOCB, and loads and interprets a new IOCB from there.
24	Data Chain	If set to 1: The VMIVME-5620 acts as bit 25 does (command chain), except that the VMIVME-5620 loads only bits 27 through 24 of the HSD Op, and does not transfer the EFW through the HSD interface. Bits 31 through 28 of the HSD Op are kept from the current IOCB. The effect is to chain the data buffers pointed to by the second word of the IOCB's (Words 1) as if they were all one long buffer.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

WORD 0

HSD Op	DEVOP	Transfer Count
31 24	23 16	15 0

I/O DIRECT	CMD XFER	DEV STAT RQ	CONT ON ERR	INT ON EOB	XFER IN CHN	CMD CHAIN	DATA CHAIN
31	30	29	28	27	26	25	24

WORD 1

Memory Buffer Address or Device-Dependent Command
31 0

WORD 2

Not Used (but see External Mode, Section 4.24.5)
31 0

WORD 3

HSD Status
31 0

Figure 4.24.1-1 Input/Output Control Block

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4.24.1-1 Valid Combinations of HSD Op Code Bits

	Bits in HSD Op Code								Possible Op Codes (Hex)							
	IOD	CT	DSR	CE	IEB	TIC	CC	DC								
NO CHAINING	D	0	0	X	I	0	0	0	00	08	10	18	80	88	90	98
	X	0	0	X	I	1	0	0	04	0C	14	1C	84	8C	94	9C
	X	0	1	X	I	0	0	0	20	28	30	38	A0	A8	B0	B8
	X	1	0	X	I	0	0	0	40	48	50	58	C0	C8	D0	D8
COMMAND CHAIN	D	0	0	0	I	0	1	0	02	82	0A	8A				
	D	0	0	1	I	0	1	0	12	92	1A	9A				
	X	0	1	0	I	0	1	0	22	A2	2A	AA				
	X	1	0	0	I	0	1	0	42	C2	4A	CA				
DATA CHAIN	D	0	0	0	I	0	0	1	01	81	09	89				
	X	0	0	0	I	1	0	1	05	85	0D	8D				
	D	0	0	1	I	0	0	1	11	91	19	99				

X = Don't care.
D = I/O Direction (0 = VME-to-HSD).
I = Interrupt on End of Block.

There are 60 valid HSD opcodes out of a possible 256.

The last word of an IOCB is space for VMIVME-5620 error status. The VMIVME-5620 can store status here at the completion of any IOCB that transfers data or status. See Figure 4.24.1-2 for the status format. The most significant bit of the IOCB status word identifies the source of the status: 0 means no status is present, and 1 means the VMIVME-5620 has stored status. The fields of this word are:

Status ID	31	1: VMIVME-5620 status present 0: No status
I/O Reset	30	Transfer stopped by I/O RESET
Ext Term	29	Transfer stopped by external terminate
Buf Uflo	28	Input ended before Transfer Count (TC) went to zero
LWF or DEB	27	Transfer stopped by last word flag
BERR	26	VMEbus BERR during data transfer
Ill. IOCB	25	IOCB not valid due to bad HSD Op
Buf Oflo	24	Input data buffer full, TC not zero
Residual	23-0	TC left if transfer stopped before TC exhausted

The host computer should ensure that the IOCB status is zeroed before executing the IOCB, so the presence of VMIVME-5620 status can be determined.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

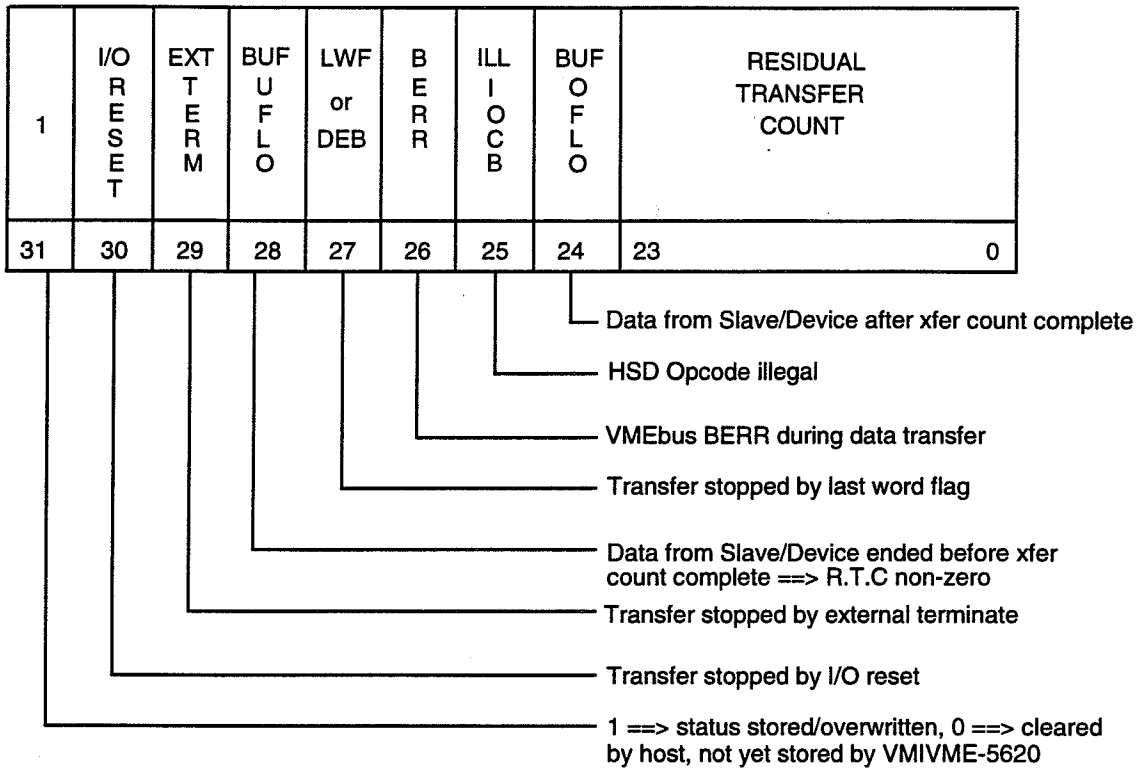


Figure 4.24.1-2 IOCB Status Word Format

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.24.2 General Programming For A Data Transfer, Slave Mode

When in Slave Mode, the VMIVME-5620 reacts to commands sent over the HSD cable from another HSD, which could be another VMIVME-5620 configured as Master.

When the Master interprets an IOCB, it sends the entire 32-bit first word of the IOCB to the Slave. This is called an External Function Word (EFW). Bits 16 through 23 of the EFW are called a DEVOP. Typically, the Slave interprets the DEVOP, and may set up a DMA transfer to/from its own VMEbus, using the Direction bit and the Transfer Count in the EFW.

The VMIVME-5620 provides an Autoslave mode that partly automates the DEVOP interpretation process. The user loads the IOCB Pointer (CBP) with the address of a table of entries each of which is two longwords (8 bytes) long. Figure 4.24.2-1 shows the format of these entries. Then, after the GO bit is set, the VMIVME-5620 uses the DEVOP as an index into this table and acts as follows:

```
If ENABLE is a one then                          (autoslave)
   {
      if Data-Chain in EFW is a one then (data chained)
         {
            Use Max Transfer Count from table
         }
      else                                       (not data chained)
         {
            Use Transfer Count from EF word or use
            transfer count from table, whichever is
            the smaller.
         }
      Start DMA using address and AM bits from table
      Wait for LWF from the master, or TC complete.
      If INT is a one, generate VMEbus interrupt.

   }
else                                             ("manual" slave)
   {
      Generate VMEbus Interrupt (if TCIC register
      contents allow) to let VME host handle the
      transfer.
   }
```

If the Autoslave Complete is NOT set in the Board Status (BST) register when the interrupt occurs, the host processor must take action. If a data transfer is necessary, it must load the address into the Data Pointer (DBP) and set the GO bit. The I/O direction will be taken from the EFW that caused the Autoslave failure.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

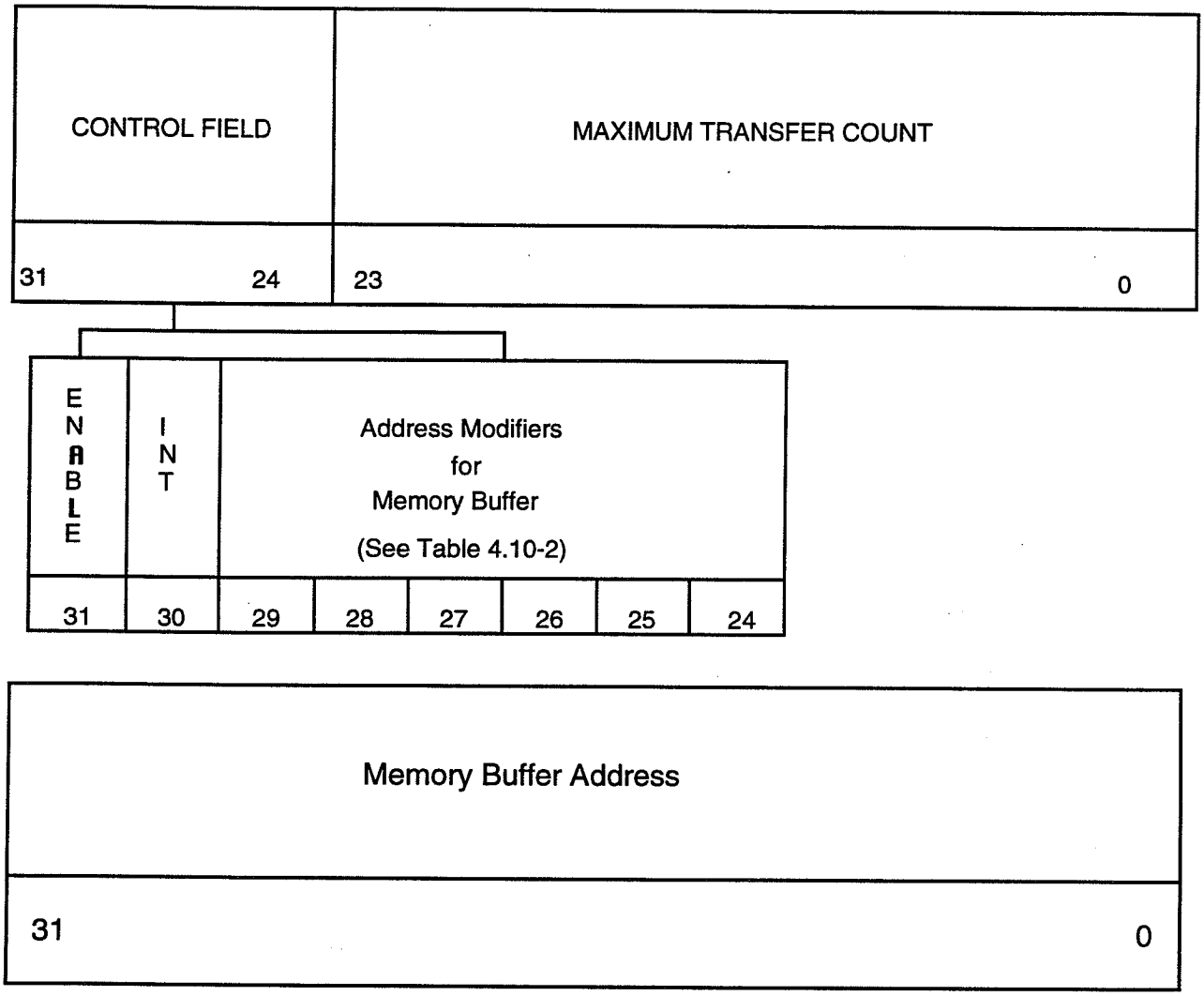


Figure 4.24.2-1 Autoslave Control Block

NOTE

When operating in the Slave mode with the Input LWF bit set to one in the EMOD register, the effective Transfer Count must be greater than one.

4.24.3 Interrupts

The VMIVME-5620 can generate VMEbus interrupts for a variety of reasons, under control of mask/level and vector registers, each programmable by the user. Whenever a VMEbus interrupt is generated, any activity caused by the GO bit stops, the GO bit resets, and then the RUNNING bit resets.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

There are four sets of interrupt registers. Each set has a vector register (8 bits), and a mask/level register (8 bits). The mask/level register has a master mask bit and one or more "reason" bits, and a three-bit level field. The master mask bit enables VMEbus interrupts on the level set by the level field. Non-zero reason bits control why the interrupt goes active. The interrupt register formats are shown in Section 4.13 through 4.17.

The VMIVME-5620 will generate an interrupt only if the associated interrupt mask bit is zero and the associated reason bit is a one. In addition, some of the reasons require an additional enable bit to be a one. Each IOCB has an Int On EOB bit in the HSD Op field, and each Autoslave table entry has an INT bit in the first longword.

In Master or IBL mode, the IOCB Int On EOB bit must be a one to permit the following interrupts. The CBP will, after the interrupt, be pointing to Word 0 of the IOCB that caused the interrupt (not to the next IOCB in the IOCL).

IOCB Done
External Terminate
Last Word Flag/Device End of Block
Transfer Count Complete

In Autoslave mode, when an entry is accessed, the INT bit in the table entry must be a one to permit the following interrupts.

Autoslave Done
Slave Reset (by I/O RESET from Master)
External Terminate
Last Word Flag/Device End of Block
Transfer Count Complete

The External Function Word Hold bit, if a one, will generate an External Function Word Received interrupt when an Autoslave table access occurs. The host will have to issue a GO before any further action happens. External Function Word Hold in Master or IBL modes has a different function: the VMIVME-5620 waits for outgoing FIFO storage to empty before transmitting anything else.

NOTE

It is important to realize that any interrupt that comes from the VMIVME-5620 means that VMIVME-5620 activity has stopped. The CPU must take action to allow HSD activity to go on.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.24.4 Inter-Bus Link Mode

A VMIVME-5620 can be connected to another VMIVME-5620, or to an HSD, in Inter-Bus Link (IBL) mode. The IBL mode is a symmetric DMA link between two computers, providing a request-grant protocol for control of the link.

4.24.4.1 Configuration and Interconnection

In IBL mode, one of the VMIVME-5620's has to be configured as Master, and the other as Slave, to get the proper signal interconnections.

If a VMIVME-5620 is connected to an Encore HSD, the VMIVME-5620 must be configured as a Slave. The Slave connotation in IBL mode does not mean that the Slave unit always has to react to the other unit, as it would in "normal" mode. Either board can initiate a transfer or a series of transfers. One, and only one, of the two boards in an IBL link must be configured as the high priority board. This resolves a simultaneous request for control of the link in favor of the high priority board.

4.24.4.2 IBL Interface Signals

Figure 4.24.4.2-1 is a simplified block diagram of the interconnection between VMIVME-5620's in IBL mode. The Master board could be an Encore HSD, with similar names as that of the Slave board. The functions of the IBL Interface control signals are shown in Table 4.24.4.2-1

Table 4.24.4.2-1. IBL Functional Description of Control Signals

VMIVME-5620	ENCORE NAME	I/O	MEANING
LKRQOUT	LRO	OUT	Request control of the link
EXTFACK	LAO	IN	Acknowledges link control by this unit
LKRQIN	LRI	IN	Other unit requests control of the link
STATACK	LAI	OUT	Acknowledges link control by other unit
IORESET	IOR	OUT	Level meaning connected and on-line
DEVPRES	DP	IN	Level meaning other unit is present
ODTARDY	ODR	OUT	Output data present
OUTACK	OA	IN	Output data taken
IDTARDY	IDR	IN	Input data present
IDTAACK	IA	OUT	Input data taken
LASTWFG	LWF	OUT	Last word: Sent with last ODR or IA
DATAEOB	DEB	IN	End Block: Comes with last IDR or OA
TERMDEV	TDV	OUT	Asynchronous stop signal to other unit
EXTTERM	EXT	IN	Asynchronous stop signal from other unit

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Of these, EXTFACK, STATACK, and IORESET have different functions than they do in "normal" (Master-Slave/Device) mode. LKRQOUT and LKRQIN are used only in IBL mode. The rest of the control signals shown above have the same function and relative timing as in "normal" mode. The "normal" mode signals EXTMODE, EXTFCN, and STATRDY are not used in IBL mode.

4.24.4.3 Link Acquisition and Data Transfer

Suppose that two VMIVME-5620's are connected in IBL mode. One of them is Master and the other is Slave. It does not matter which one requests the link, so let the requester be called A, and let the other unit be called B.

Unit A reacts to a REQIBL bit set in its ACT register by asserting LKRQOUT. Unit B will receive LKRQIN, whereupon it asserts its STATACK as acknowledgment. Unit A perceives this as EXTFACK, and negates its LKRQOUT. Unit B sees LKRQIN negate, and negates its STATACK, and unit A sees EXTFACK negate. This completes link acquisition by unit A. Unit A will set its IBL Link Ready Status bit, and unit B will set its IBL Link Active bit. Unit A resets its REQIBL bit when it sets Link Ready Status.

The hosts of the units can enable the Restart Interrupt of the VMIVME-5620's so they can react to the IBL Link Ready and IBL Link Active bits without having to poll them.

By convention, the unit that gets control of the link (that is the one that set IBL Link Ready as opposed to IBL Link Active) will transmit data to the other unit. The units could run a series of transfers over the link, provided the order and direction of the transfer are determined by which one is in control of the link.

Once the link is established as above, each unit must execute an IOCB to do data transfers. The IOCB format is the same as that for the Master in "normal" mode. The host sets up the registers of the VMIVME-5620's as in "normal" mode, and sets the GO bit in the ACT register. There is no transfer of External Function Words, but data proceeds across the link. Because there is no EFW transfer, the receiving unit's IOCB must either be set with the exact transfer count expected, or with a larger count. In the latter case, the transfer stops when the receiving unit detects the Last Word Flag (LASTWFG) signal. Therefore, the host should always set the Last Word Flag Enable bit in the MOD register.

When the IOCB (or chain of IOCBs) completes, the unit automatically resets the IBL Link Ready or IBL Link Active bits, and sets the Last Word Flag/Device End of Block or Transfer Count Complete bits. The host can enable interrupts to be notified of these, if desired.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

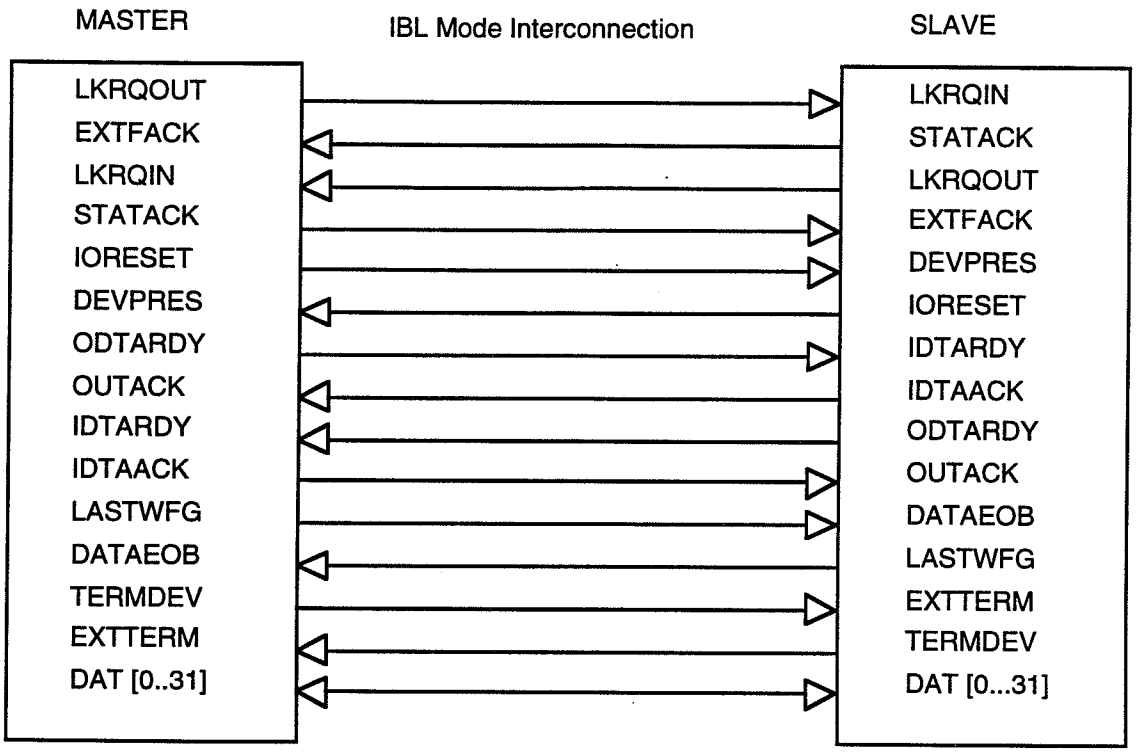


Figure 4.24.4.2-1. IBL Mode Interconnection

4.24.5 External Mode

The VMIVME-5620 can emulate an HSD connected to a Device that runs in External Mode, and can also emulate a Device that runs in External Mode. External Mode allows a Slave/Device to completely control data transfers to and from an HSD or VMIVME-5620 Master, by providing a memory address to the Master for each transfer cycle. Cable connections from the Master to the Slave are the same for a Slave that can run in External Mode as for any other Slave or Device.

4.24.5.1 Entering or Exiting External Mode

The Master VMIVME-5620 (or Encore HSD) ordinarily allows the Slave VMIVME-5620 or Device to use External Mode by executing a Command Transfer IOCB. At any time after all the control lines have negated, the Slave or Device can assert the EXTMODE signal. Once the Master perceives this, it reacts to signals from the Slave or Device until EXTMODE negates; during this time, the Master cannot service any ACT register requests, with the exception of the Terminate Device bit, because it is under the control of the Slave or Device.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.24.5.2 External Mode Protocol

Transfers in External Mode proceed as follows:

The Slave presents a 24-bit address (bits 0-23) and a direction bit (bit 31: 0 for from Master, 1 for to Master) on the data lines, and asserts STATRDY. The Master takes the address and direction, and asserts STATACK. The Slave negates STATRDY, and finally the Master negates STATACK.

If the direction bit was zero, the Slave waits for the Master to present data on the data lines and asserts ODTARDY. The Slave takes the data, asserts OUTACK, waits for the Master to negate ODTARDY, and negates OUTACK. This completes a transfer from the Master to the Slave.

If the direction bit was a one, the Slave presents data on the data lines and asserts IDTARDY. When the Master takes the data, it asserts IDTAACK. The Slave negates IDTARDY, and waits for the Master to negate IDTAACK. This completes a transfer from the Slave to the Master.

Transfers proceed as above, with address (Input Status) cycles interspersed with Input Data or Output Data cycles, until the Slave no longer wants control. The Slave returns control to the Master by negating EXTMODE.

4.24.5.3 Execution

Before executing the Command Transfer IOCB that allows the Slave to run in External Mode, the Master's host must load the Residual Transfer Count register with a bias to be algebraically added to all addresses that will come from the Slave. This bias allows for host mapping, and for possible 32-bit addressing.

The Slave's host runs the Slave by executing IOCB's that have the same format as for a Master in "normal" mode, except that the third word (IOCB Word 2) now must contain the address to be sent to the Master. This is a 24-bit address, right justified. If the IOCB calls for more than one transfer (IOCB Word 0 Transfer Count greater than one), this address will be internally incremented, by the size of the transfer, after each address/data cycle. IOCB's can be chained, just as in "normal" Master mode.

The CAM and DAM registers, interrupt vectors and controls, the IOCB Pointer Register, and so on must be set up by both hosts before action starts.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

If the Master encounters a BERR from the VMEbus while attempting DMA on behalf of the Slave, the Master will send a Terminate Device signal (TERMDEV) to the Slave, which will stop External Mode activity and negate EXTMODE. The Master's host can also stop activity by setting the Terminate Device bit in the ACT register. This is the only ACT bit that the Master will react to, while in External Mode.

4.24.6 Self Tests

The VMIVME-5620 can perform several diagnostic tests on parts of its hardware. The host CPU must set up each test and command it to run. The CPU uses the RUNNING and Self Test Failed (TSTFAIL) bits in the BST register, and the GO bit in the ACT register, to control the self tests. Some of the tests may return a code in the DVS register on failure. The first four steps in running a self test are the same for each test; they are shown as a through d below. From that point, the tests differ. The codes that can be returned in the DVS register are listed after the specific test steps.

The Timer Interrupt Test (TEST_TIMER) needs special consideration: the host computer must NOT access any of the VMIVME-5620 registers while this test is running. The RUNNING bit may be polled without disturbing the test by using the BSP register to force status to be stored in VMEbus address space, and then polling the stored copy. See section 4.22 for details.

a. Make sure GO and RUNNING are zeros.
b. Set desired tests in EFW register HSD Op field bits. See the diagram at the end of the DVS return code list.
c. Do not set any of TEST_BERR or TEST_LOOP or TEST_DMA simultaneously.
d. Set Test bit in ACT register.

TEST_DMA: VMEbus → VMEbus DMA loop test
- Load source pointer in CBP
- Load destination pointer in DBP
- Set CAM and DAM
- Set byte count in EFW TC field (mult. of 4)
- Set GO
- Wait for GO and RUNNING to go to zero
- Examine TSTFAIL bit and DVS register

TEST_FIFO: No-cable FIFO loop test
- Set GO
- Wait for GO and RUNNING to go to zero
- Examine TSTFAIL bit and DVS register
- RXC contains ones in error positions if test failed

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

TEST_VINT: VMEbus interrupt test
- Set vector in RSIV
- Set level (1-7) in RSIC, other bits zeros
- Set GO (causes the VMEbus interrupt)
- (VMIVME-5620 waits at most 10 milliseconds)
- Wait for GO and RUNNING to go to zero
- Examine TSTFAIL bit and DVS register

TEST_BERR: Self-access BERR test
- Set base address of board in CBP
- Set CAM
- Set GO
- Wait for GO and RUNNING to go to zero
- RXC contains longword read if did not BERR
- Examine TSTFAIL bit and DVS register

TEST_LOOP: Loopback no-cable test
- Load source pointer in CBP
- Load destination pointer in DBP
- Set CAM and DAM
- Set byte count in EFW (mult. of 4)
- Set GO
- Wait for GO and RUNNING to go to zero
- Examine TSTFAIL bit and DVS register

TEST_SERP: Serial port test
- Set GO
- Wait for GO and RUNNING to go to zero
- Examine TSTFAIL bit and DVS register

TEST_TIMER: Timer interrupt test
- Set GO
- Wait for GO and RUNNING to go to zero
  (See text above for how to wait)
- Examine TSTFAIL bit and DVS register

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DVS Register Self Test Failure Codes

Mnemonic	Value	Reason for Failure
DMA_GET_ERR	1	TEST_DMA data fetch error
DMA_PUT_ERR	2	TEST_DMA data store error
VINT_TIMEOUT	3	TEST_VINT timed out
VINT_ILLEGAL	4	TEST_VINT improperly set up
SERP_A_BAD	5	TEST_SERP found 2681 port A bad
SERP_B_BAD	6	TEST_SERP found 2681 port B bad
BERR_NO_BERR	7	TEST_BERR did not BERR
FIFO_NO_LOOP	8	TEST_FIFO loopback timed out
FIFO_DATA_ERR	9	TEST_FIFO data error, see RXC reg
FIFO_BAD_STAT	10	TEST_FIFO loopback status error
LOOP_GET_ERR	11	TEST_LOOP data fetch error
LOOP_PUT_ERR	12	TEST_LOOP data store error
TIMER_FAST	13	TEST_TIMER: timer speed high
TIMER_SLOW	14	TEST_TIMER: timer speed low
TEST_UNDEFINED	255	Undefined test bit in HSD Op

Test Codes in External Function Word HSD Op Field

	31	30	29	28	27	26	25	24
Selftest HSD OP:	Test DMA	Test FIFO	Test VINT	Test BERR	Test LOOP	Test SERP	Test TIMER	0

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.24.7 Programming Examples

Here are some simple examples of how to use the VMIVME-5620 as Master or Slave. Shown are a master "write" (transmit to cable from VME), a Slave "read" (receive from cable and DMA to VME), and an example of command chaining as master.

1. Master writes 1024 longwords to slave:

Host sets up an IOCB:

```
wr_io:  dc.l    0x00010400    ; HSD op = 00
                              ; Dev op = 01
                              ; TC = 1024
        dc.l    buf_addr
        dc.l    0             ; Unused
        dc.l    0             ; Place for status
```

Host sets the pointer to the IOCB into the VMIVME-5620, assuming BRD to be the base address of the board:

```
        move.l  #wr_io,BRD+0x20
```

Host sets the mode and sets GO:

```
        move.w  #0x4301,BRD+0x0C
```

Host waits for both GO and RUNNING to be zero.

```
w_stop: btst.b  #0,BRD+0x0D
        bne     w_stop+0x06
w_run:  btst.b  #6,brd+0x06
        bne     w_run
```

This is, of course, an extremely simple case. The host could have armed a TC complete interrupt, and set the interrupt bit in the HSD Op, in which case it would not have to poll the status to discover when the transfer completed. There also is no data or command chaining going on.

2. Slave set up to automatically read 1024 words from master:

Host sets up the autoslave table by clearing all 512 longwords of it, and setting the following:

```
as_tbl: dc.l    0             ;Entry for devop 0
        dc.l    0xB9000400    :Entry for devop 1
                              ;   Enabled, no INT
                              ;   Address mode 0x39
        dc.l    rcv_buf_addr ;Max. TC = 1024
        dc.l                  ;Entry for devop 2
                 ...          ;507 more zeros
```


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Host points out the table to the VMIVME-5620:

```
move.l  #as_tbl,BRD+0x20
```

Host turns on autoslave mode and waits:

```
move.w  #0x701,BRD+0x0C
```

Here, the only indication that a transfer happened is that the Autoslave Function Complete bit sets in the BST register. The table entry could have requested an interrupt on done, and armed LWF and Transfer Complete interrupts, to keep from having to poll BST. Furthermore, unless the master requested data chaining, the TC field in the entry is not used unless it is less than the count sent as part of the EF word.

3. Master writes 1024 words, then reads 256 words, then requests device status, and generates a Done interrupt at the end of the status request:

Host sets up an IOCL:

```
io_lst: dc.l    0x02010400    ; Write, cmd chain
        dc.l    wr_buf
        dc.l    0
        dc.l    0             ; VMIVME-5620 status
        dc.l    0x82020100    ; Read, cmd chain
        dc.l    rd_buf
        dc.l    0
        dc.l    0             ; VMIVME-5620 status
        dc.l    0x28000000    ; DSR, int on done
        dc.l    st_buf        ; Points to status
        dc.l    0
        dc.l    0             ; VMIVME-5620 status
```

The write will complete, then the read, and then the DSR. If some error happens during the read, for example, the residual word count and status will store in Word 3 of the read IOCB, and because the Continue On Error bit is not set, the Done interrupt will never happen (the DSR IOCB never executes).

On the following pages is a hardware definition header file recommended for programming the VMIVME-5620.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

```
/* File:           5620hdwe.h
 * Description:    VMIVME-5620 register definitions
 * Revision:       XO
 * Date:           06 Dec 92
 * Where used: Force-33 CPU test code for VMIVME-5620
 * Property of:    VMIC (VME Microsystems International Inc.)
 */

/* Register variables as offsets from ID register */

#define BID         *(Byte *)(regbase+0x00)       /* Board ID */
#define STFLGID     *(Byte *)(regbase+0x01)       /* Self test flag in ID register */
#define ROM_VER     *(Word *)(regbase+0x02)       /* ROM version code */
#define BST         *(Word *)(regbase+0x04)       /* Board Status */
#define BSTRH       *(Word *)(regbase+0x06)       /* Board Status, right half */
#define DVS         *(Long *)(regbase+0x08)       /* Device (HSD) status */
#define MOD         *(Byte *)(regbase+0x0C)       /* Mode control */
#define ACT         *(Byte *)(regbase+0x0D)       /* Activity control */
#define MOD_ACT     *(Word *)(regbase+0x0C)       /* MOD and ACT as a Word */
#define MOD_EXT     *(Word *)(regbase+0x0E)       /* Extended MODE register */
#define CAM         *(Byte *)(regbase+0x10)       /* Command address mode and size */
#define DAM         *(Byte *)(regbase+0x11)       /* Data address mode and size */
#define CAM_DAM     *(Word *)(regbase+0x10)       /* CAM and DAM as a Word */
#define TIMEMS *(Word *)(regbase+0x12)       /* Timeout for cable, in ms */
#define VEIC        *(Byte *)(regbase+0x14)       /* VMEbus error interrupt control
*/
#define HEIC        *(Byte *)(regbase+0x15)       /* HSD (Device) Error int control
*/
#define TCIC        *(Byte *)(regbase+0x16)       /* Transfer Complete int control */
#define RSIC        *(Byte *)(regbase+0x17)       /* Restart interrupt control */
#define VEIV        *(Byte *)(regbase+0x18)       /* VMEbus error interrupt vector */
#define HEIV        *(Byte *)(regbase+0x19)       /* HSD (Device) Error int vector */
#define TCIV        *(Byte *)(regbase+0x1A)       /* Transfer Complete int vector */
#define RSIV        *(Byte *)(regbase+0x1B)       /* Restart interrupt vector */
#define RXC         *(Long *)(regbase+0x1C)       /* Residual Transfer Count */
#define CBP         *(Long *)(regbase+0x20)       /* Command buffer ptr (--> IOCL) */
#define EFW         *(Long *)(regbase+0x24)       /* External Function Word (EFW)*/
#define HSDOp       *(Byte *)(regbase+0x24)       /* EFW HSD Opcode */
#define DevOp       *(Byte *)(regbase+0x25)       /* EFW Dev Opcode */
#define HSD_WC *(Word *)(regbase+0x26)       /* EFW Word Count */
#define DBP         *(Long *)(regbase+0x28)       /* Data buffer pointer */
#define BSP         *(Long *)(regbase+0x2C)       /* Board status buffer pointer */

/* BST (Board Status) bits */

#define ANYERR 0x8000            /* Any Error (OR of bits marked ERROR) */
#define EXTTERM    0x4000            /* External Terminate */
#define SLVRST 0x2000            /* Slave Reset */
#define TIMEOUT    0x1000            /* Time Out of HSD cable int'face (ERROR) */
#define VMEBERR    0x0800            /* BERR on VMEbus master cycle (ERROR) */
#define HDWEERR    0x0400            /* 5620 hardware error (ERROR) */
#define RFNZ       0x0200            /* Reserved Field set non-zero (ERROR) */
#define DEVPRES    0x0100            /* Device Present */
#define EFRCVD 0x0080            /* External Function Word received */
#define AUSDONE    0x0040            /* Autoslave function complete */
#define LWF_DEB    0x0020            /* Last Word Flag or Device End of Block */
#define WCDONE 0x0010            /* Word Count Complete */
#define TSTFAIL    0x0008            /* Self test function failure */
#define TSTBUSY    0x0004            /* Self test function busy */
```


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

```
#define LINKACT    0x0002              /* IBL link function is active */
#define LINKRDY    0x0001              /* IBL link established and ready */

/* BSTRH (Board Status Right Half) bits */

#define IL_IOCB    0x8000              /* Illegal IOCB */
#define RUNNING    0x4000              /* Running (Bunny) bit */
#define PROTERR    0x2000              /* HSD cable protocol error */
#define SCON       0x1000              /* 1 = SCON jumper is installed (slot 1) */
#define IOCBDN 0x0800              /* IOCB done */
#define REGBUSY    0x0400              /* Write-to-register process busy */
#define ST_PA      0x000C              /* 2681 serial port A test results */
#define ST_PB      0x0003              /* 2681 serial port B test results */

/* Mode control register and Activity control register */

#define HIPRIOR    0x8000              /* Priority level for REQIBL */
#define MASTMOD    0x4000              /* Master mode */
#define IBLMOD 0x2000              /* IBL (link) mode */
#define ENALWF 0x1000              /* Enable Last Word Flag function */
#define EFHOLD 0x0800              /* EF Word Hold function */
#define AUTOSLV    0x0400              /* Auto Slave function */
#define BRLEVEL    0x0300              /* VMEbus Bus Request Level to use */
#define TDVEXT 0x0080              /* Send TDV (master) or EXT (slave) */
#define REQIBL 0x0040              /* Request IBL link */
#define RUNTEST    0x0020              /* Run spec. test routine (spec. in EFW) */
#define RESETIO    0x0010              /* Send reset to device */
#define RSTIFAC    0x0008              /* Reset HSD interface hardware */
#define CLRSTAT    0x0004              /* Clear Board Status as much as possible */
#define LED        0x0002              /* Panel LED (1 = ON, 0 = OFF) */
#define GO     0x0001              /* Do specified HSD fn. (clears on done) */

/* Extended Mode control register */

#define ME_RELMOD      0xC000      /* Release Mode */
#define ME_RELROR      0x0000      /* Release on Request */
#define ME_RELRWD      0x4000      /* Release when Done */
#define ME_RELROC      0x8000      /* Release on BCLR* */
#define ME_RELBCAP     0xC000      /* Bus capture and hold */
#define ME_VMETOT      0x3800      /* VMEbus timeout if SCON */
#define ME_INPLWF      0x0100      /* Send LWF with last IDA */
#define ME_PRIRR           0x0080      /* Priority (1) or Round Robin (0) */
#define ME_EXTMOD      0x0040      /* External Mode (Only if Slave) */
#define ME_FAST            0x0020      /* FAST mode for cable */
#define ME_WARP            0x0010      /* WARP mode for cable */
#define ME_FAIRTO      0x000F      /* Fairness control and timeout */

/* Command address modifier or Data address modifier */

#define VMESIZE            0xC0        /* VMEbus size, 00 = L, 01 = B, 10 = W */
#define VME_SIZE_32        0x00        /* 32-bit size as VMEbus master */
#define VME_SIZE_16        0x80        /* 16-bit size as VMEbus master */
#define VME_SIZE_8     0x40        /*  8-bit size as VMEbus master */
#define ADDRMOD            0x3F        /* VMEbus Address Modifier */

/* Interrupt control registers */

#define INTMASK    0x80                /* Int mask (1 = enabled, 0 = disabled) */
```


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

```
#define INTLEVL    0x07              /* VMEbus level code */
#define BERRMSK    0x10              /* VMEbus BERR mask in VEIC */
#define HDWEMSK    0x08              /* Hardware Error mask in VEIC */
#define ILIOMSK    0x40              /* Illegal IOCB mask in VEIC */
#define PROTMSK    0x20              /* HSD cable protocol error mask in VEIC */
#define EXTTMSK    0x10              /* External Terminate mask in HEIC */
#define TMOTMSK    0x08              /* HSD Time Out mask in HEIC */
#define EFRVMSK    0x40              /* EF word received mask in TCIC */
#define AUSDMSK    0x20              /* AUS Done mask in TCIC */
#define LWEBMSK    0x10              /* Last Word Flag/Device EOB mask in TCIC */
#define WCDNMSK    0x08              /* WC Done mask in TCIC */
#define LKACMSK    0x20              /* IBL link active: other HSD acquired it */
#define CBDNMSK    0x10              /* IOCB Done mask in RSIC */
#define SLRSMSK    0x08              /* Slave Reset mask in RSIC */

/* External Function Word HSDOp (not DevOp) bits */

#define EF_IOD 0x80000000     /* IO Direction: 0 = to cable, 1 = to VME */
#define EF_CT      0x40000000     /* Command Transfer */
#define EF_DSR 0x20000000     /* Device Status Request */
#define EF_CE      0x10000000     /* Continue on Error */
#define EF_IEB 0x08000000     /* Interrupt on End of Block */
#define EF_TIC 0x04000000     /* Transfer In Channel */
#define EF_CC      0x02000000     /* Command Chain */
#define EF_DC      0x01000000     /* Data Chain */

/* Autoslave table definitions */

#define AS_EN      0x80000000     /* Enable this entry */
#define AS_INT 0x40000000     /* Interrupt on use of entry */
#define AS_AM      0x3F000000     /* VMEbus AM code for this entry */
#define AS_MXC 0xFFFFFF           /* Maximum transfer count */

/* IOCB word 3 status definitions */

#define IS_ID      0x80000000     /* IOCB status ID: 1 = resid/error, 0 = dev */
#define IS_IORS    0x40000000     /* Transfer stopped by I/O Reset */
#define IS_EXTT    0x20000000     /* Transfer stopped by External Terminate */
#define IS_UFLO    0x10000000     /* From-cable buffer underflow */
#define IS_LWEB    0x08000000     /* Transfer stopped by LWF or DEB */
#define IS_BERR    0x04000000     /* VMEbus BERR during data transfer */
#define IS_ILIO    0x02000000     /* Illegal IOCB because of HSD opcode */
#define IS_OFLO    0x01000000     /* From-cable buffer overflow */
#define IS_RESD    0x00FFFFFF     /* Residual transfer count */

/* Selftest control bits within HSDOp field of EFW */

#define TEST_DMA          0x80       /* VMEbus --> VMEbus DMA loop test */
#define TEST_FIFO     0x40       /* No-cable FIFO loop test */
#define TEST_VINT     0x20       /* VMEbus interrupt test */
#define TEST_BERR     0x10       /* Self-access BERR test */
#define TEST_LOOP     0x08       /* Loopback no-cable test */
#define TEST_SERP     0x04       /* Serial port test */
#define TEST_TIMER    0x02       /* Timer interrupt test */
```


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
**********
*  CAUTION  *
**********
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
**********
*  CAUTION  *
**********
```

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the boards are properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

5.3 JUMPER CONFIGURATIONS

The VMIVME-5620 has several jumper fields that are pre-configured for certain defaults at the factory but which may need to be changed according to the host system configuration. Figure 5.3-1 shows the locations of all jumpers on the VMIVME-5620 with factory default jumpers installed.

5.3.1 VMEbus Address Configuration

The VMIVME-5620 occupies 64 bytes of memory and may be addressed using jumper field JP3. Table 5.3.1-1 shows the jumper configuration of JP3 for the different modes and accesses available.

Table 5.3.1-1. JP3 Configurations

Function	Jumper ID	Pin Numbers	Configuration
A24 Mode	A16SPC	41, 42	Installed
A16 Mode	A16SPC	41, 42	Omitted
Supervisory Access	SUPSPC	37, 38	Omitted
	NPSPC	39, 40	Installed
Nonprivileged Access	SUPSPC	37, 38	Installed
	NPSPC	39, 40	Omitted
Both Supervisory and Nonprivileged Access	SUPSPC	37, 38	Omitted
	NPSPC	39, 40	Omitted

In configuring the board's address, A24 mode uses jumpers A6 through A23 of JP3. A16 mode only uses jumpers A6 through A15. An installed jumper equals zero (0); an omitted jumper equals one (1).

5.3.2 System Controller Configuration

If the VMIVME-5620 is installed as the system controller in slot one of the chassis, the board must have the SCON jumper (pins 43 and 44) of JP3 installed. If the SCON jumper is installed, the VMIVME-5620 performs the following system controller functions:

a. Full-function, four-level bus arbiter. The arbitration method used can be toggled between a round-robin and a prioritized scheme by changing the Arbiter Mode bit in the Extended Mode Register (see Section 4.9).
b. The 16 MHz SYSCLK VMEbus system clock.
c. The SYSRESET* system reset signal.
d. IACK* interrupt acknowledge daisy-chain driver.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

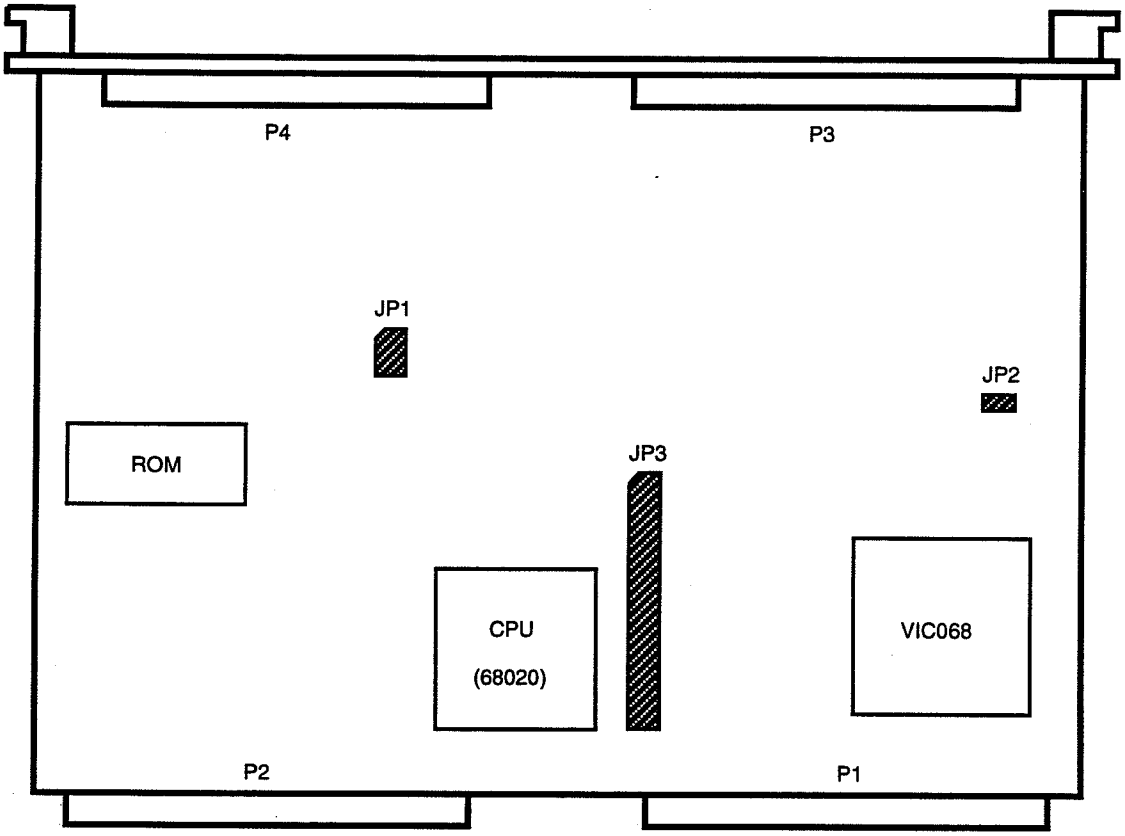
e. VMEbus BERR bus error timer. By default, the VMIVME-5620 activates the BERR* signal when any bus master fails to get a DTACK* acknowledge signal within 64 microseconds. This bus error timeout can be changed. See Section 4.6.

5.4 SERIAL PORTS AND HARDWARE RESET

The serial ports (JP1) support a basic 3-wire RS-232 protocol and allow communications to the 68020 for factory test and development purposes. The operating parameters are fixed at 9600 baud, 8 bits, 1 stop bit, no parity. GND is the ground pin. TX is the transmit pin. RX is the receive pin. Both serial ports are shipped with the transmit pins jumpered to the receive pins, disabling them. These jumpers should not be removed by the user.

JP2, if momentarily shorted, causes a hard reset just as if power had been removed and restored. JP2 should normally be left unconnected.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



SERIAL PORTS

JP1

GND
TX
RX

DEFAULT CONFIGURATION

A24 Address = 000000 Hex
Responds to Standard (A24) addressing in both supervisory and nonprivileged modes
System Controller functions disabled
Serial ports disabled

ADDRESSING *

JP3

1	2	A23
3	4	A22
5	6	A21
7	8	A20
9	10	A19
11	12	A18
13	14	A17
15	16	A16
17	18	A15
19	20	A14
21	22	A13
23	24	A12
25	26	A11
27	28	A10
29	30	A9
31	32	A8
33	34	A7
35	36	A6
37	38	SUPSPC
39	40	NPSPC
41	42	A16SPC
43	44	SCON

RESET

JP2

PUCAP
GND

* An installed jumper equals zero (0).
An omitted jumper equals one (1).

Figure 5.3-1. VMIVME-5620 Jumper Locations

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP