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VM1548

TTL I/O MODULE

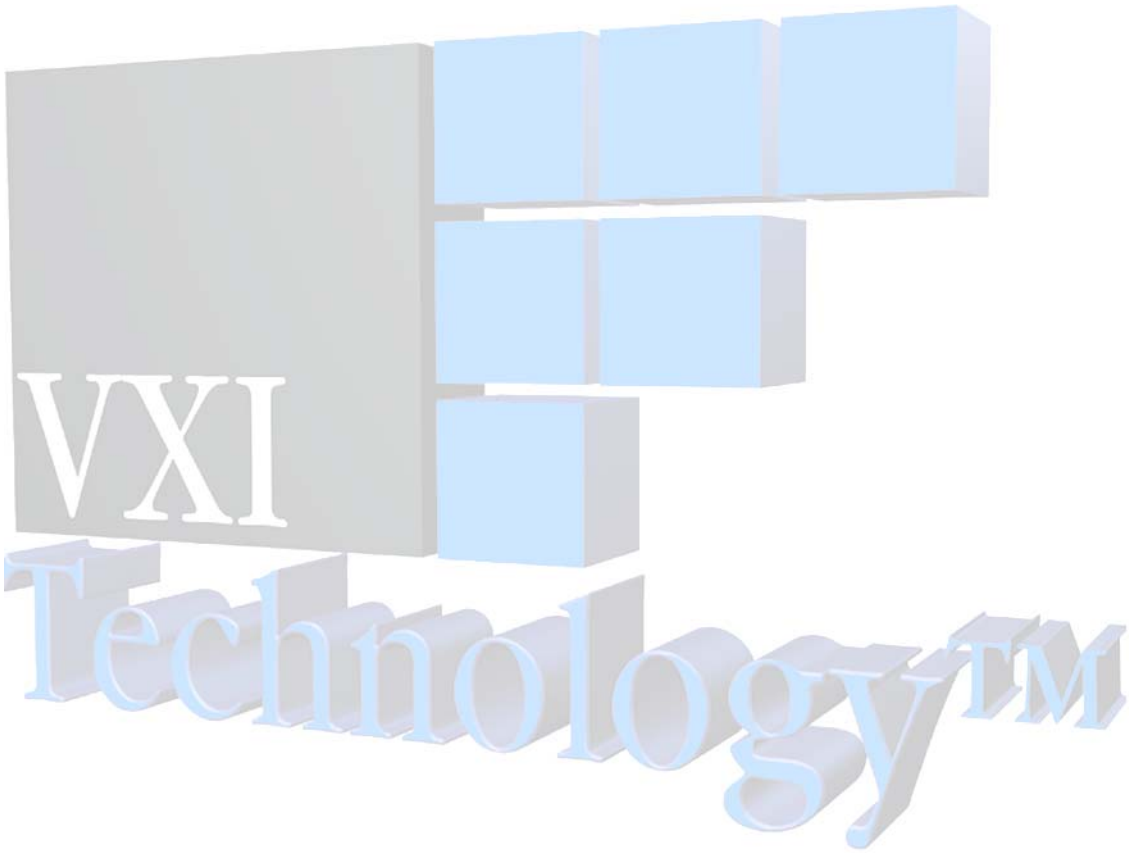
USER'S MANUAL

P/N: 82-0021-000
Released June 28, 2007

VXI Technology, Inc.

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Irvine, CA 92614-6509
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CERTIFICATION

VXI Technology, Inc. (VTI) certifies that this product met its published specifications at the time of shipment from the factory. VTI further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

The product referred to herein is warranted against defects in material and workmanship for a period of three years from the receipt date of the product at customer's facility. The sole and exclusive remedy for breach of any warranty concerning these goods shall be repair or replacement of defective parts, or a refund of the purchase price, to be determined at the option of VTI.

For warranty service or repair, this product must be returned to a VXI Technology authorized service center. The product shall be shipped prepaid to VTI and VTI shall prepay all returns of the product to the buyer. However, the buyer shall pay all shipping charges, duties, and taxes for products returned to VTI from another country.

VTI warrants that its software and firmware designated by VTI for use with a product will execute its programming when properly installed on that product. VTI does not however warrant that the operation of the product, or software or firmware will be uninterrupted or error free.

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The warranty shall not apply to defects resulting from improper or inadequate maintenance by the buyer, buyer-supplied products or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

VXI Technology, Inc. shall not be liable for injury to property other than the goods themselves. Other than the limited warranty stated above, VXI Technology, Inc. makes no other warranties, express or implied, with respect to the quality of product beyond the description of the goods on the face of the contract. VTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

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DECLARATION OF CONFORMITY

Declaration of Conformity According to ISO/IEC Guide 22 and EN 45014

MANUFACTURER'S NAME	VXI Technology, Inc.
MANUFACTURER'S ADDRESS	2031 Main Street Irvine, California 92614-6509
PRODUCT NAME	TTL I/O Module
MODEL NUMBER(S)	VM1548
PRODUCT OPTIONS	All
PRODUCT CONFIGURATIONS	All

VXI Technology, Inc. declares that the aforementioned product conforms to the requirements of the Low Voltage Directive 73/23/EEC *and the* EMC Directive 89/366/EEC *(inclusive* 93/68/EEC*) and carries the "CE" mark accordingly. The product has been designed and manufactured according to the following specifications:*

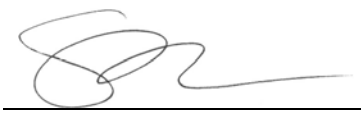
SAFETY	EN61010 (2001)
EMC	EN61326 (1997 w/A1:98) Class A CISPR 22 (1997) Class A VCCI (April 2000) Class A ICES-003 Class A (ANSI C63.4 1992) AS/NZS 3548 (w/A1 & A2:97) Class A FCC Part 15 Subpart B Class A EN 61010-1:2001

The product was installed into a C-size VXI mainframe chassis and tested in a typical configuration.

I hereby declare that the aforementioned product has been designed to be in compliance with the relevant sections of the specifications listed above as well as complying with all essential requirements of the Low Voltage Directive.

June 2007

CE



Steve Mauga, QA Manager

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GENERAL SAFETY INSTRUCTIONS

Review the following safety precautions to avoid bodily injury and/or damage to the product. These precautions must be observed during all phases of operation or service of this product. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture and intended use of the product.

Service should only be performed by qualified personnel.

TERMS AND SYMBOLS

These terms may appear in this manual:

WARNING Indicates that a procedure or condition may cause bodily injury or death.

CAUTION Indicates that a procedure or condition could possibly cause damage to equipment or loss of data.

These symbols may appear on the product:



ATTENTION - Important safety instructions



Frame or chassis ground



Indicates that the product was manufactured after August 13, 2005. This mark is placed in accordance with *EN 50419, Marking of electrical and electronic equipment in accordance with Article 11(2) of Directive 2002/96/EC (WEEE).* End-of-life product can be returned to VTI by obtaining an RMA number. Fees for take-back and recycling will apply if not prohibited by national law.

WARNINGS

Follow these precautions to avoid injury or damage to the product:

Use Proper Power Cord To avoid hazard, only use the power cord specified for this product.

Use Proper Power Source To avoid electrical overload, electric shock, or fire hazard, do not use a power source that applies other than the specified voltage.

Use Proper Fuse To avoid fire hazard, only use the type and rating fuse specified for this product.

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WARNINGS (CONT.)

Avoid Electric Shock

To avoid electric shock or fire hazard, do not operate this product with the covers removed. Do not connect or disconnect any cable, probes, test leads, etc. while they are connected to a voltage source. Remove all power and unplug unit before performing any service. ***Service should only be performed by qualified personnel.***

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground.

Operating Conditions

To avoid injury, electric shock or fire hazard:

- Do not operate in wet or damp conditions.
- Do not operate in an explosive atmosphere.
- Operate or store only in specified temperature range.
- Provide proper clearance for product ventilation to prevent overheating.
- DO NOT operate if any damage to this product is suspected. ***Product should be inspected or serviced only by qualified personnel.***



Improper Use

The operator of this instrument is advised that if the equipment is used in a manner not specified in this manual, the protection provided by the equipment may be impaired.
Conformity is checked by inspection.

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SUPPORT RESOURCES

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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VXI Technology, Inc.
2031 Main Street
Irvine, CA 92614-6509

Phone: (949) 955-1894
Fax: (949) 955-3041

VXI Technology
Cleveland Instrument Division

5425 Warner Road
Suite 13
Valley View, OH 44125

Phone: (216) 447-8950
Fax: (216) 447-8951

VXI Technology
Lake Stevens Instrument Division

VXI Technology, Inc.
1924 - 203 Bickford
Snohomish, WA 98290

Phone: (425) 212-2285
Fax: (425) 212-2289

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Phone: (949) 955-1894
Fax: (949) 955-3041
E-mail: support@vxitech.com



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SECTION 1

INTRODUCTION

INTRODUCTION

The VM1548 is a high-performance TTL I/O module which has been designed for high data throughput and flexibility of configuration. The instrument uses the message-based word serial interface for programming and data movement as well as allowing direct register access for very high-speed data input and retrieval. The VM1548 command set conforms with the SCPI standard for consistency and ease of programming.

The VM1548 is a member of the VXI Technology VMIP™ (*VXI Modular Instrumentation Platform*) family and is available as a 48-, 96- or 144-channel, single-wide VXIbus instrument. Figure 1-1 and Figure 1-2 show the 144-channel version of the VM1548. The 96-channel version would not have J200 and its associated LED's and nomenclature while the 48-channel version would eliminate J202 as well. In addition to these three standard configurations, the VM1548 may be combined with any of the other members of the VMIP family to form a customized and highly integrated instrument (see Figure 1-1). This allows the user to reduce system size and cost by combining the VM1548 with two other instrument functions in a single wide, C-size VXIbus module.

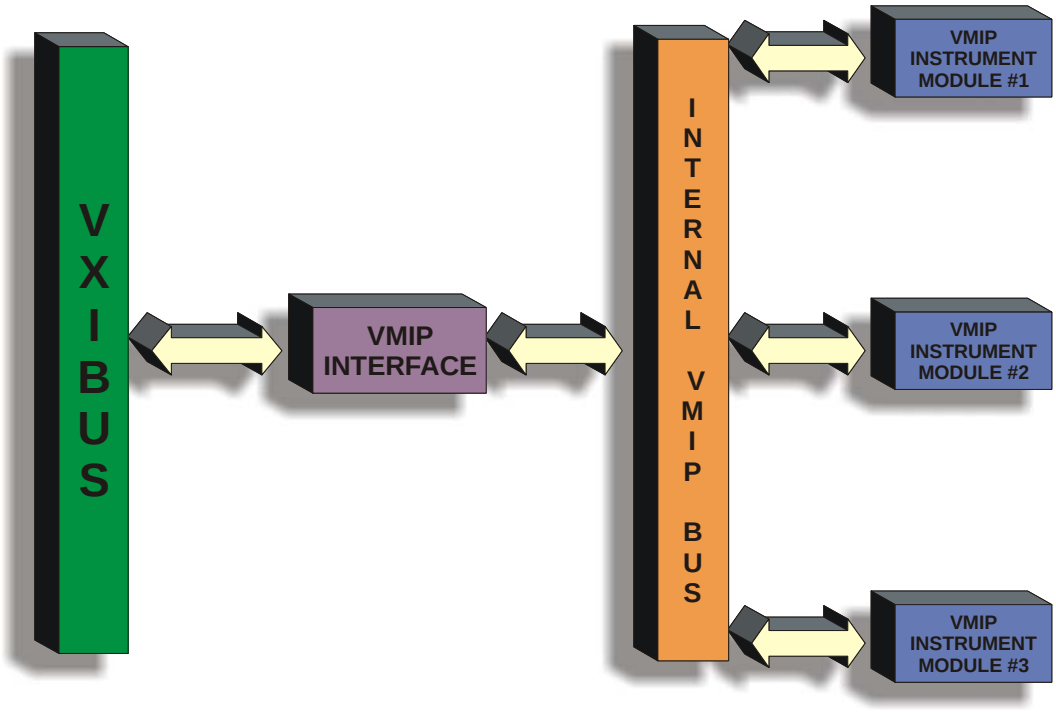
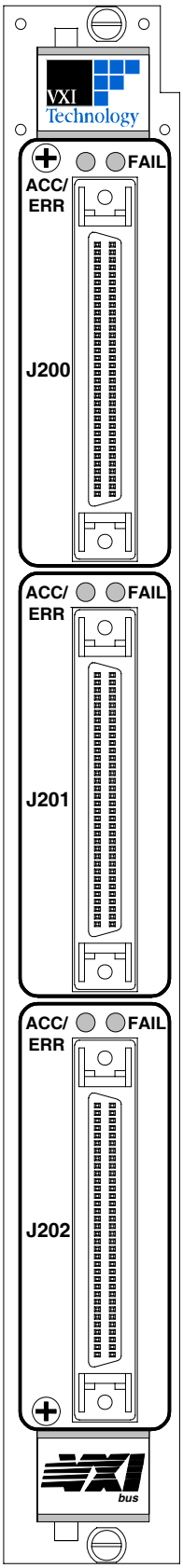


FIGURE 1-1: VMIP™ PLATFORM

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Regardless of whether the VM1548 is configured with other VM1548 modules or with other VMIP modules, each group of 48 channels is treated as an independent instrument in the VXIbus chassis and as such, each group has its own FAIL/POWER and ACCESS/ERROR indicators.

DESCRIPTION

The VM1548 is a high-performance TTL I/O module with six groups of eight bits per VMIP daughter module. Each group of eight bits may be configured as an input or output under program control or via front panel control lines. The inputs and outputs may be either single buffered to provide real time data access or may be double buffered to provide synchronized data input and/or output.

When an input group or output group is specified as single buffered (the register source is programmed as NONE), the front panel inputs are read at the time the access occurs or the front panel outputs are updated immediately. If an input group or output group is specified as double buffered (the register source is programmed other than NONE), then the inputs read the last clocked input and the front panel outputs will not reflect the new data until they are clocked.

The VM1548 has the flexibility to source the input and output clocks from either the front panel (one input per group of eight bits), the backplane TTL Trigger bus or via a word serial command. By using the appropriate clocking sources, very large numbers of channels may be synchronized to collect or present data to a UUT.

Each data I/O pin has a series damping resistor to reduce ringing of the data during a transition period. The VM1548 is shipped from the factory with 22 Ω networks. The damping resistor networks are socketed to allow the user to change the value to better reflect their own unique transmission line characteristics.

Each clock input is internally pulled to a logic high level and has a RC termination network to reduce multiple clocking due to clock line ringing. The RC network consists of a 120 Ω resistor in series with a 100 pF capacitor giving a time constant of 12 ns. These values are selected to terminate the clock lines during fast transitions only and will not load the driving source.

FIGURE 1-2: FRONT PANEL LAYOUT

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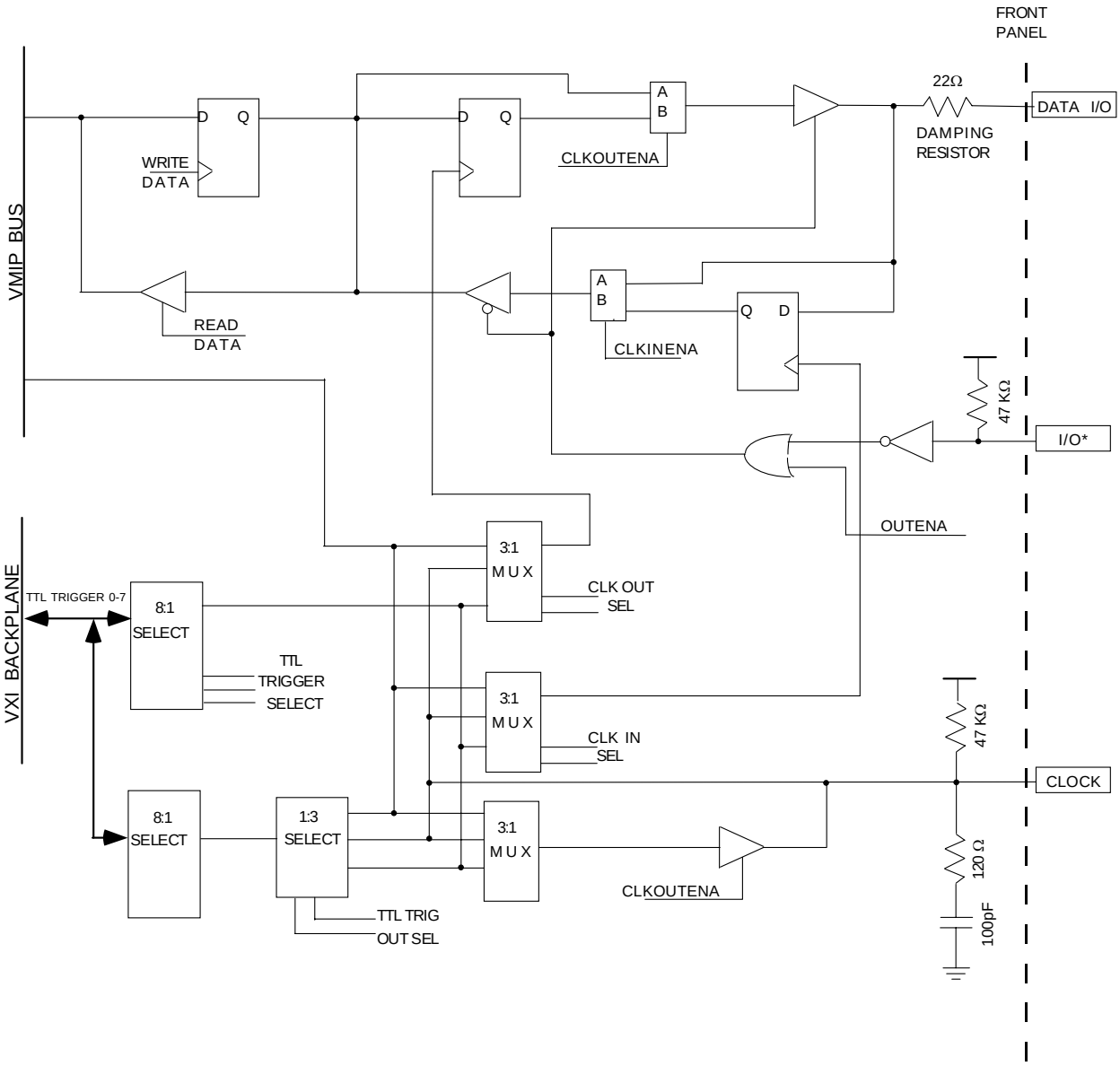


FIGURE 1-3: VM1548 MODULE BLOCK DIAGRAM

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VM1548 SPECIFICATIONS

GENERAL SPECIFICATIONS	
NUMBER OF CHANNELS	
VM1548-1	48, 6 Groups of 8 Bits
VM1548-2	96, 12 Groups of 8 Bits
VM1548-3	144, 18 Groups of 8 Bits
DATA ACCESS TYPES	
	Direct Register Access or Message-based Word Serial
REGISTER ACCESS	
	Registers located in the user area of the VXI register map
DATA THROUGHPUT	
	500 ns Typical, direct register access 2 MB/s (megabytes/second) using D8 access 4 MB/s using D16 access
PHYSICAL INTERFACE	
	Socketed 74BCT652N driver with series damping resistors
DAMPING RESISTOR	
	Socketed 22 Ω Network
DATA INPUT CHARACTERISTICS	
V_{IN} (High)	> 2.0 V
V_{IN} (Low)	< 0.8 V
I_{IN} (@ V_{IN} = 2.7 V)	< 70 µA
I_{IN} (@ V_{IN} = 5.0 V)	< 1 mA
I_{IN} (@ V_{IN} = 0.5 V)	< -1 mA
DATA OUTPUT CHARACTERISTICS	
V_{OUT} (High)	> 2.0 V @ -15 mA
V_{OUT} (Low)	< 0.55 V @ 64 mA
** Voltages are with the damping resistors removed and replaced with shorts.*	
CLOCK AND CONTROL INPUT CHARACTERISTICS	
V_{IN} (High)	> 2.0 V
V_{IN} (Low)	< 0.8 V
I_{IN} (@ V_{IN} = 5.0 V)	< 10 µA
I_{IN} (@ V_{IN} = 0.5 V)	< 100 µA
DATA INPUT CLOCK SOURCES	
	6 Front Panel, TTL Trigger bus (0 - 7), Word Serial Event (command) Rising or Falling Edge
TTL TRIGGER OUTPUT SOURCES	
	Front Panel Clock Inputs (0 - 5), Word Serial Event (command) Rising or Falling Edge
CLOCKED INPUT DATA SETUP	
	≥ 10 ns
CLOCKED INPUT DATA HOLD	
	≥ 5 ns
CLOCKED DATA OUTPUT SKEW	
	≤ 20 ns
POWER REQUIREMENTS	
VM1548-1	+5 V @ 1.18 A, -5.2 V @ 0.5 A
VM1548-2	+5 V @ 1.62 A, -5.2 V @ 0.5 A
VM1548-3	+5 V @ 2.06 A, -5.2 V @ 0.5 A

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GENERAL SPECIFICATIONS (CONTINUED.)	
COOLING REQUIREMENTS	
VM1548-1	0.4 liters
VM1548-2	0.8 liters
VM1548-3	1.2 liters
MANUFACTURER'S ID	
	3915
COOLING REQUIREMENTS	
	258

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SECTION 2

PREPARATION FOR USE

INSTALLATION

When the VM1548 is unpacked from its shipping carton, the contents should include the following items:

(1) VM1548 VXIbus module
(1) VM1548 TTL I/O Module Operator's Manual (this manual)

All components should be immediately inspected for damage upon receipt of the unit.

Once the VM1548 is assessed to be in good condition, it may be installed into an appropriate C size or D-size VXIbus chassis in any slot other than slot 0. The chassis should be checked to ensure that it is capable of providing adequate power and cooling for the VM1548. Once the chassis is found to be adequate, the VM1548's logical address and the chassis' backplane jumpers should be configured prior to the VM1548's installation.

CALCULATING SYSTEM POWER AND COOLING REQUIREMENTS

It is imperative that the chassis provide adequate power and cooling for this module. Referring to the chassis user's manual, confirm that the power budget for the system (the chassis and all modules installed therein) is not exceeded and that the cooling system can provide adequate airflow at the specified backpressure.



It should be noted that if the chassis cannot provide adequate power to the module, the instrument may not perform to specification or possibly not operate at all. In addition, if adequate cooling is not provided, the reliability of the instrument will be jeopardized and permanent damage may occur. Damage found to have occurred due to inadequate cooling would also void the warranty of the module.

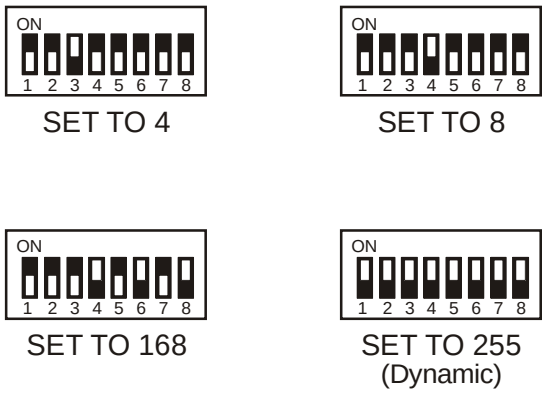
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SETTING THE CHASSIS BACKPLANE JUMPERS

Please refer to the chassis User's Manual for further details on setting the backplane jumpers.

SETTING THE LOGICAL ADDRESS

The logical address of the VM1548 is set by a single 8-position DIP switch located near the module's backplane connectors (this is the only switch on the module). The switch is labeled with positions 1 through 8 and with an ON position. A switch pushed toward the ON legend will signify a logic 1; switches pushed away from the ON legend will signify a logic 0. The switch located at position 1 is the least significant bit while the switch located at position 8 is the most significant bit. See Figure 2-1 for examples of setting the logical address switch.



Switch Position	Switch Value
1	1
2	2
3	4
4	8
5	16
6	32
7	64
8	128

FIGURE 2-1: LOGICAL ADDRESS SWITCH SETTING EXAMPLES

The VMIP may contain three separate instruments and will allocate logical addresses as required by the VXIbus specification (revisions 1.3 and higher). The logical address of the instrument is set on the VMIP carrier. The VMIP logical addresses must be set to an even multiple of 4 ***unless dynamic addressing is used***. Switch positions 1 and 2 must always be set to the OFF position. Therefore, only addresses of 4, 8, 12, 16, ... 252 are allowed. The address switch should be set for one of these legal addresses and the address for the second instrument (the instrument in the center position) will automatically be set to the switch set address plus one; while the third instrument (the instrument in the lowest position) will automatically be set to the switch set address plus two. If dynamic address configuration is desired, the address switch should be set for a value of 255 (All switches set to ON). Upon power-up, the slot 0 resource manager will assign the first available logical addresses to each instrument in the VMIP module.

If dynamic address configuration is desired, the address switch should be set for a value of 255. (All switches set to ON). Upon power-up, the slot 0 resource manager will assign the first available logical addresses to each instrument in the VMIP module.

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FRONT PANEL INTERFACE WIRING

The VM1548's module interface is made available on the front panel of the instrument. The 48-channel version (VM1548-1) will have J201 that contains all signals for this instrument. The 96-channel version (VM1548-2) will have J201 and J202 provided, while the 144-channel version (VM1548-3) will have J200, J201, and J202. The wiring for each of these connectors is identical and since each group of four channels is treated as a separate instrument, the module will have three channel 1s, three channel 2s, three channel 3s, etc.

The connector used in the VM1548 is a readily available 68-pin high-density type commonly known as a 68-pin version of the SCSI 2 connector. The mating connector is an IDC (Insulation Displacement Connector) component and is available from a variety of sources. The connector attaches to two 34-conductor 0.050 centers ribbon cable and the pin out has been selected to allow for using the twisted pair type of ribbon cable. Some manufacturers also allow the use of discrete 30 gauge stranded wires.

TABLE 2-1: J200, J201 AND J202 PIN OUT

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
GND	1	DATA1.5	18	GND	35	DATA4.5	52
DATA0.0	2	DATA1.6	19	DATA3.0	36	DATA4.6	53
DATA0.1	3	DATA1.7	20	DATA3.1	37	DATA4.7	54
DATA0.2	4	I/O*1	21	DATA3.2	38	I/O*4	55
DATA0.3	5	CLK1	22	DATA3.3	39	CLK4	56
DATA0.4	6	GND	23	DATA3.4	40	GND	57
DATA0.5	7	DATA2.0	24	DATA3.5	41	DATA5.0	58
DATA0.6	8	DATA2.1	25	DATA3.6	42	DATA5.1	59
DATA0.7	9	DATA2.2	26	DATA3.7	43	DATA5.2	60
I/O*0	10	DATA2.3	27	I/O*3	44	DATA5.3	61
CLK0	11	DATA2.4	28	CLK3	45	DATA5.4	62
GND	12	DATA2.5	29	GND	46	DATA5.5	63
DATA1.0	13	DATA2.6	30	DATA4.0	47	DATA5.6	64
DATA1.1	14	DATA2.7	31	DATA4.1	48	DATA5.7	65
DATA1.2	15	I/O*2	32	DATA4.2	49	I/O*5	66
DATA1.3	16	CLK2	33	DATA4.3	50	CLK5	67
DATA1.4	17	GND	34	DATA4.4	51	GND	68

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The mating connector to J200, J201 or J202 is available from the following companies:

AMP Inc.

P/N 749621-7	Connector
P/N 749195-2	Back Shell
P/N 82208	Catalog covering this series of connectors

Circuit Assembly

P/N CA-68NDP-12GT	Connector
P/N CA-68NDBS-1M	Back Shell
P/N DG01	Catalog covering this series of connectors

The pin locations for J200, J201, and J202 are shown in Figure 2-2.

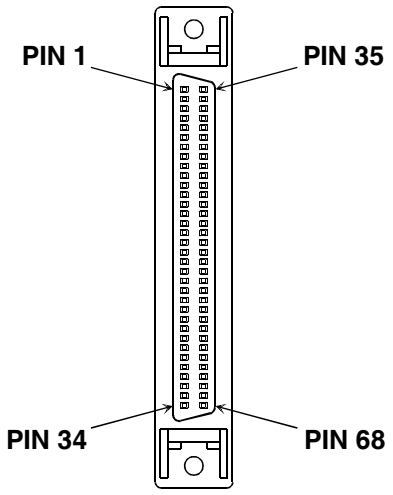


FIGURE 2-2: J200, J201, AND J202 PIN LOCATIONS

SECTION 3

PROGRAMMING

EXAMPLES OF SCPI COMMANDS

TTLTRIG Circuit

A multiplexer is used to select 1 of 8 different sources as TTLTRIG. The signal is selected using the following SCPI command:

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OUTPUT:TTLTRIG:SOURCE <source>	*Where <source> refers to one of the EXTERNAL CLK lines (CLK0-5), IMMEDIATE or NONE.*

The selected signal is called GLOBAL (TRIGOUT) and after a polarity control, it is called TTLTRIGGER, which is presented on the VXIbus as the selected TTLTRIG0-7. The specific TTLTRIG line is selected using the following SCPI command:

OUTPUT:TTLTRIG <n>	*Where <n> refers to one of the 8 TTLTRIG lines.*

The TTLTRIGGER is enabled or disabled using the following SCPI command:

OUTPUT:TTLTRIG:STATE ON	*Enables the Trigger*
OUTPUT:TTLTRIG:STATE OFF	*Disables the Trigger*

The following is an example of how to produce CLK2 as TTLTRIG4 to the backplane:

```
OUTPUT:TTLTRIG:STATE ON
OUTPUT:TTLTRIG:POLARITY NORMAL
OUTPUT:TTLTRIG 4
OUTPUT:TTLTRIG:SOURCE EXTERNAL2
```


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If CLK2 is a logic low level, then the following SCPI command would allow a logic high level on the backplane.

OUTPUT:TTLTRIG:POLARITY INVERT *TTLTRIG 4 will not pull the line low*

Likewise, continuing with this example, the following command would produce a logic low level on the backplane.

OUTPUT:TTLTRIG:POLARITY NORMAL *TTLTRIG 4 will pull the line low*

Interrupt Circuit

This section deals with the interrupt circuit. The VM1548 has the capability to interrupt the slot 0 controller via the VMIP with either a high going edge or with a low going edge of the IRQ* signal. The timing and control circuitry can select one of the six EXTERNAL clocks, GLOBAL (TRIGOUT) or NONE as the interrupt trigger. The interrupt is selected and enabled using the following SCPI command:

STATUS:INTERRUPT:ENABLE <source> *Where <source> is EXTERNAL0-5, GLOBAL or NONE*

The following SCPI command will trigger the status interrupt on a positive edge:

STATUS:INTERRUPT:PTRANSITION ON

The following SCPI command will trigger the status interrupt on a negative edge:

STATUS:INTERRUPT:NTRANSITION ON

EXAMPLES

To use GLOBAL (TRIGOUT) out as the status interrupt trigger, the following SCPI command would be issued:

STATUS:INTERRUPT:ENABLE GLOBAL

To trigger the status interrupt from a negative going edge external clock source from port 3, the following SCPI commands would be issued:

STATUS:INTERRUPT:ENABLE EXTERNAL3
STATUS:INTERRUPT:NTRANSITION ON

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To trigger the status interrupt from a negative edge going external clock source from port 1, the following SCPI commands would be issued:

```
STATUS:INTERRUPT:ENABLE EXTERNAL1
STATUS:INTERRUPT:NTRANSITION ON
```

Output Register Circuit

This section refers to the bi-directional port when configured as an output. The SCPI command used to configure a port as an output is:

```
SOURCE:DATA:ENABLE <port #> ON
```

The port is programmable to allow the data to be transparent or clocked. If the port is clocked, there are several choices for the clock source. The method for selecting clocked mode and the source of the clock is done with one SCPI command.

OUTPUT:REGISTER:SOURCE <port #> <source>	*Where <port> is 1 of 6 data registers and <source> is EXTERNAL, TTLTRIG, GLOBAL (TRIGOUT) or IMMEDIATE*

The method for selecting transparent mode is:

OUTPUT:REGISTER:SOURCE <port #> NONE	*Where <port> is 1 of 6 data registers and NONE means this data register is transparent*

EXAMPLES

The following SCPI commands will clock the number 205 out of port #5 using the IMMEDIATE pulse.

```
SOURCE:DATA:ENABLE 5 ON
OUTPUT:REGISTER:SOURCE 5 IMMEDIATE
SOURCE:DATA 5 205
TRIGGER:SEQUENCE:IMMEDIATE                    This provides a rising edge clock
```

The following is an example of writing to a port operating in transparent mode. This method requires no clock edge for the data to be presented on the external connector.

```
SOURCE:DATA:ENABLE 5 ON
OUTPUT:REGISTER:SOURCE 5 NONE
SOURCE:DATA 5 205                             205 Immediately appears on the
                                              External Connector
```

The following example selects the external CLK5 line to clock the data port. In this example, it is assumed the external CLK5 signal is a steady logic low and the clock edge is produced by toggling the clock polarity.

```
SOURCE:DATA:ENABLE 5 ON
OUTPUT:REGISTER:SOURCE 5 EXTERNAL
OUTPUT:REGISTER:POLARITY 5 NORMAL
SOURCE:DATA 5 205
OUTPUT:REGISTER:POLARITY 5 INVERT             This provides a rising edge clock
```


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Input Register Circuit

This section refers to the bi-directional port when configured as an input. The SCPI command used to configure a port as an input is:

SOURCE:DATA:ENABLE <port #> OFF

The port is programmable to allow the data to be transparent or clocked. If the port is clocked, there are several choices for the clock source. The method for selecting clocked mode and the source of the clock is done with one SCPI command.

INPUT:REGISTER:SOURCE <port #> <source>	Where <port> is 1 of 6 data registers and <source> is EXTERNAL, TTLTRIG, GLOBAL (TRIGOUT) or IMMEDIATE

Regardless of the port's input mode, note that data inputs to the module do not contain pull-up or down-biasing resistors. As such, if the user does not provide either active or passive biasing of the data inputs, a read of the port may result in either a "1" or a "0" being read from the data inputs.

The method for selecting transparent mode is:

INPUT:REGISTER:SOURCE <port #> NONE	Where <port> is 1 of 6 data registers and NONE means this data register is transparent

EXAMPLES

The following SCPI commands will clock the data in on port #3 using the IMMEDIATE pulse.

SOURCE:DATA:ENABLE 3 OFF	
INPUT:REGISTER:SOURCE 3 IMMEDIATE	
TRIGGER:SEQUENCE:IMMEDIATE	*This provides a rising edge clock*
FORMAT ASCII	
READ? 3	*Example of read value is 255*

The following is an example of reading from a port operating in transparent mode. This method requires no clock edge for the data to be available.

SOURCE:DATA:ENABLE 5 OFF	
INPUT:REGISTER:SOURCE 5 NONE	
FORMAT BINARY	*Example of read value is #B11111111*
READ? 5	*The data presented on the external connector is what will be read*

The following example selects the external CLK3 line to clock the data port. In this example, it is assumed the external CLK3 signal is a steady logic low and the clock edge is produced by toggling the clock polarity.

SOURCE:DATA:ENABLE 3 OFF	
INPUT:REGISTER:SOURCE 3 EXTERNAL	
INPUT:REGISTER:POLARITY 3 NORMAL	
INPUT:REGISTER:POLARITY 3 INVERT	*This provides a rising edge clock*
FORMAT HEX	
READ? 3	*Example of read value is #HFF*

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Bi-directional Clock Circuit

There are 6 independent bi-directional clock circuits connected to the 68-pin external connector. Each clock is associated with one of the 6 ports previously described. Therefore <port #> terminology is used to refer to a specific clock. When the circuit is configured as an output, the clock signal will be sourced by the module. When the circuit is configured as an input, the clock signal is sourced by the UUT. This clock (CLK0-5) may be used for many different purposes: a trigger source; selections for the interrupt trigger; a port's input clock; a port's output clock.

The following SCPI command configures the clock line as an output:

OUTPUT:CLOCK:ENABLE ON

The following SCPI command configures the clock line as an input:

OUTPUT:CLOCK:ENABLE OFF

When the circuit is operating as an output, the clock source is selectable using the following SCPI command.

OUTPUT:CLOCK:SOURCE <port #> <source>	Where <source> is TTLTRIG, IMMEDIATE, GLOBAL (TRIGOUT) or NONE

The polarity of the output clock signal is controlled with the following SCPI command.

OUTPUT:CLOCK:POLARITY <edge>	Where <edge> is NORMAL or INVERT

EXAMPLES

To drive TRIGIN out as CLK1 on the external connector, the following SCPI commands would be issued.

```
OUTPUT:CLOCK:ENABLE 1 ON
OUTPUT:CLOCK:SOURCE TTLTRIG
```

To drive TRIGOUT out as CLK3 on the external connector, the following SCPI commands would be issued:

```
OUTPUT:CLOCK:ENABLE 3 ON
OUTPUT:CLOCK:SOURCE GLOBAL
```

To drive IMMEDIATE out as CLK5 on the external connector, the following SCPI commands would be issued:

```
OUTPUT:CLOCK:ENABLE 5 ON
OUTPUT:CLOCK:SOURCE IMMEDIATE
```

To select no clock, the NONE parameter is used. This will always be a logic level low.

```
OUTPUT:CLOCK:ENABLE 5 ON
OUTPUT:CLOCK:SOURCE NONE
```


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APPLICATION EXAMPLES

This section contains examples of using SCPI command strings for programming the VM1548 module. The code is functional and will contain a brief description and block diagram of the operation.

WRITE MODE

In this example the VM1548 will be set up prior to receiving the UUT generated clock edge. The VM1548 will output one (1) 16-bit binary word to the UUT from ports 0 and 1.

COMMANDS	DESCRIPTION
OUT:CLOC:ENAB 0 0	Disables port 0 clock from driving front panel connector and enables this line as the clock input to port 0.
OUT:CLOC:ENAB 1 0	Same as previous command except for port 1.
OUT:REG:SOUR 0 EXT	Selects port 0 input clock (CLK0) as method of triggering.
OUT:REG:SOUR 1 EXT	Same as previous command except for port 1.
SOUR:DATA:ENAB 0 1	Selects and enables port 0 to write data to the UUT.
STAT:INT:ENAB EXT0	Set the interrupt trigger source as the port 0 clock.
STAT:INT:PTR ON	Set the interrupt trigger source to the positive edge.
SOUR:DATA 0 48	Writes “48” data to port 0 for subsequent transfer to the UUT.
SOUR:DATA:ENAB 1 1	Selects and enables port 1 to write data to the UUT.
SOUR:DATA 1 15	Writes “15” data to port 1 for subsequent transfer to the UUT.

Figure 3-1 takes a closer look at what each command above is accomplishing.

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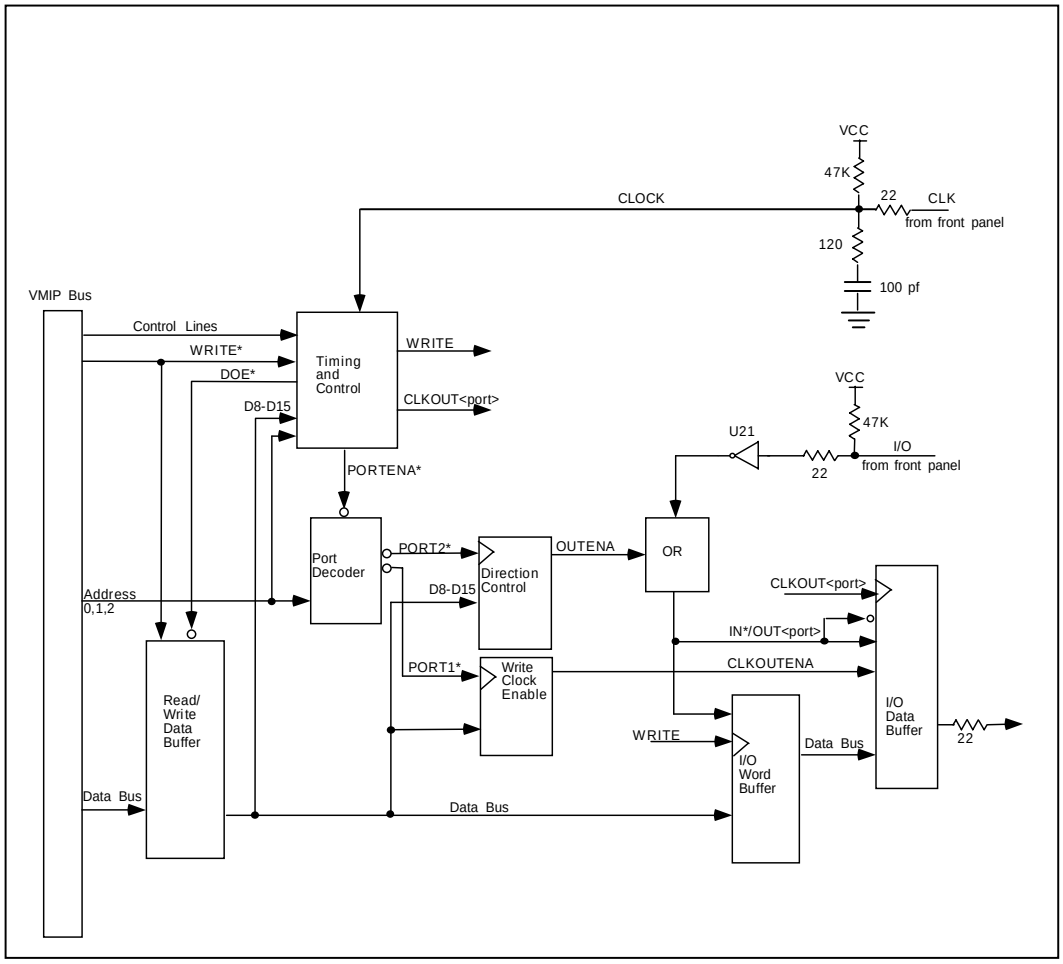


FIGURE 3-1: OUTPUT BLOCK DIAGRAM

OUT:CLOC:ENAB 0 0 and **OUT:CLOC:ENAB 1 0** commands inform the timing and control circuitry that the front panel clock lines are used as inputs. This allows the UUT to furnish the clock source when ready to receive data.

The **OUT:REG:SOUR 0 EXT** and the **OUT:REG:SOUR 1 EXT** commands select the external clock input as the trigger method to output data to the UUT. When these commands are received the VM1548 timing and control circuitry will generate the PORTENA* signal to the port decoder. The port decoder then clocks the write clock enable latch selecting the CLKOUTENA. The CLKOUTENA signals are applied to the I/O data and word buffers enabling the output clock line. The **SOUR:DATA:ENAB 0 1** and **SOUR:DATA 0 48** command enables port 0 for a write and latches the data into the I/O word buffer respectively.

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The VM1548 timing and control circuitry generates the PORTENA* signal to the port decoder. This decoder in turn clocks the direction latch selecting the OUTENA. This signal is OR'd with the external I/O direction signal from the UUT. The result is referred to as IN*/OUT and is applied to the I/O data and word buffers configuring them as outputs. The timing and control circuitry will generate a write pulse latching the data from the read/write data buffer into the I/O word buffer. Port 0 is now ready to transmit the data byte "48" to the UUT. The steps are repeated for the **SOUR:DATA:ENAB 1 1** and **SOUR:DATA 1 15** commands with port 1 being enabled and loaded with the data byte "15".

The VM1548 is now ready to transmit the data word "1548" to the UUT. When the CLK signals are received from the UUT, the I/O data buffers latch the data word from the I/O word buffer. The data on the I/O data buffer's outputs are now available to the UUT. The **STAT:INT:ENAB EXT 0** and **STAT:INT:PTR ON** commands enable the interrupt to occur when the CLK 0 signal is received and sets the polarity of this interrupt to the positive edge. The VM1548 module sends an Interrupt Request (IRQ*) informing the slot 0 controller that the transfer has occurred.

READ MODE

In this example the VM1548 will be configured to clock the UUT and read 24 bits of data, when the TTL Trigger line 1 is activated. The TTL Trigger is assumed to be pulled by another instrument used during this test. The UUT will output data on the rising edge of the received clock that is generated from the VM1548. The VM1548 will capture or read data on the falling edge of this same clock. When the VM1548 detects a TTL Trigger 1, the front panel clock lines to the UUT are activated. The clock is sent, the UUT transmits data on the rising edge and the data will be latched into the VM1548 on the falling edge. An Interrupt Request is generated informing the slot 0 controller via the VMIP that data is ready to be read.

COMMANDS	DESCRIPTION
OUT:CLOC:ENAB 3 ON	Enables port 3 clock to drive the front panel connector
OUT:CLOC:ENAB 4 ON	Same as previous command except for port 4
OUT:CLOC:ENAB 5 ON	Same as previous command except for port 5
SOUR:DATA:ENAB 3 OFF	Selects and enables port 3 to read data from the UUT
SOUR:DATA:ENAB 4 OFF	Selects and enables port 4 to read data from the UUT
SOUR:DATA:ENAB 5 OFF	Selects and enables port 5 to read data from the UUT
INP:REG:POL 3 INV	Selects the falling edge for clocking port 3
INP:REG:POL 4 INV	Selects the falling edge for clocking port 4
INP:REG:POL 4 INV	Selects the falling edge for clocking port 5
INP:REG:SOUR 3 TTLT	Selects VXI bus TRIGIN as the clock source for port 3
INP:REG:SOUR 4 TTLT	Same as previous command except for port 4
INP:REG:SOUR 5 TTLT	Same as previous command except for port 5
INP:TTLT:STATE ON	Enables the TTL trigger selection mux
INP:TTLT 1	Selects VXI bus TTL trigger line 1 to be used as TRIGIN
STAT:INT:ENAB	Set the interrupt trigger source as the default value
STAT:INT:NTR ON	Set the interrupt trigger source to the negative edge
	The controller waits for the interrupt and then proceeds
READ? 3	Data is transferred from port 3 to the VMIP bus
READ? 4	Data is transferred from port 4 to the VMIP bus
READ? 5	Data is transferred from port 5 to the VMIP bus

Figure 3-2 takes a closer look at what each command above is accomplishing.

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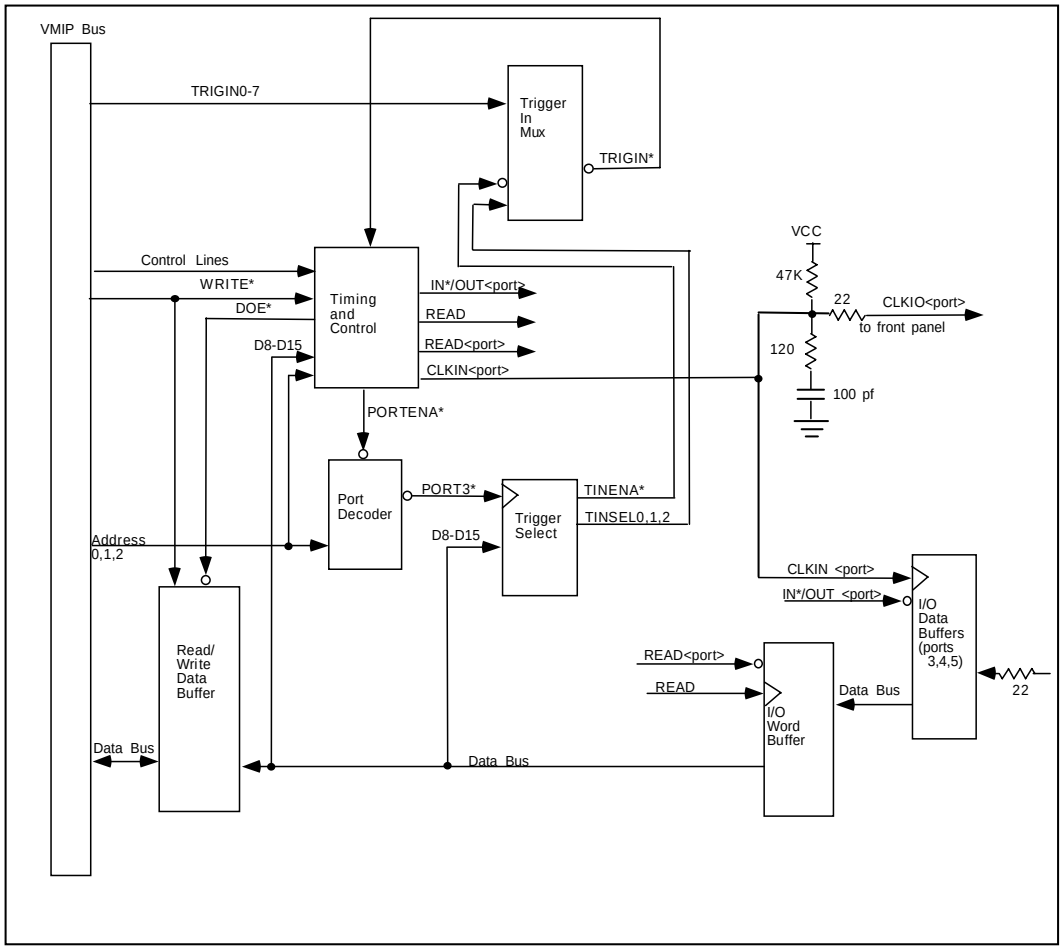


FIGURE 3-2: READ MODE USING TTL TRIGGER IN

The **OUT:CLOC:ENAB <port> ON** command configures the front panel clock connection to the output mode. This allows the VM1548 to drive these lines clocking the UUT. The timing and control circuitry generates the IN*/OUT <port> signal to the I/O data and word buffers configuring them as inputs when the **SOUR:DATA:ENAB <port> 1** commands are received. The **INP:REG:SOUR <port> TTLT** commands select the VXI TTL trigger in as the clock input for the trigger method to input data from the UUT. This clock is transmitted from the front panel connectors, clocking the data out of the UUT. When the commands are received the VM1548 timing and control circuitry will generate the PORTENA* signal to the port decoder. The port decoder then clocks the write clock enable latch selecting the CLKINENA. The CLKINENA signals are applied to the I/O data and word buffers enabling the input clock line.

The **INP:REG:POL <port> INV** command causes the timing and control circuitry to select the falling edge of the TTL trigger in as the CLKIN <port> for the I/O data buffers.

When **INP:TTLT:STATE ON** command is received, the VM1548 timing and control circuitry generates the PORTENA* signal to the port decoder. This clocks the trigger select latch selecting the TINENA line. The TINENA signal enables the trigger in mux. **INP:TTLT 1** notifies the timing and control circuitry to select TTL trigger 1 for the clock source. The port decoder is again enabled to clock the trigger select latch selecting the TINSEL signals. These signals are routed to the trigger in mux that enables TTL trigger 1 to be routed to the timing and control circuitry for clocking the UUT and the I/O data buffers. The normal polarity of the trigger is sent to the UUT and the inverted version is used for the I/O data buffers.

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The **STAT:INT:ENAB** command uses the default value of NONE (ground) to generate the status interrupt onto the VXI backplane and the **STAT:INT:PTR ON** command set the polarity of the interrupt. When the TTL trigger 1 occurs, the VM1548 will send a high going pulse to clock data out of the UUT. The falling edge of this pulse is used to latch the data into the VM1548's I/O data buffers. The VM1548 sends an Interrupt Request (IRQ*) informing the slot 0 controller via the VMIP that the transfer has occurred and that the data in the I/O data buffers is now available. The READ? <port> command causes the timing and control circuitry to generate two READ signals. The first READ signal is routed to the I/O word buffers thereby enabling them to output data to the read/write data buffer and onto the VMIP bus. The second signal READ (0,2,4) then clocks the I/O word buffer. The I/O word buffer will output one 16-bit word at a time.

Note that data inputs to the module do not contain pull-up or down-biasing resistors. If the user does not provide active or passive biasing of the data inputs, a read of the port may result in either a "1" or "0" being read from the data inputs.

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WRITE/READ MODE

In this example, data from port 0, port 1, and port 2 to port 3, port 4, and port 5 will be configured and transferred through a wrap-around cable. The wrap-around cable pin outs used are as defined in Table 3-1. The data to be sent is port 0 = 01, port 1 = 23, and port 2 = 45. The IRQ* signal will be generated from the external clock received from port 5.

COMMANDS	DESCRIPTION
INP:REG:SOUR 3 EXT	Selects External clock line as the clock source for port 3
INP:REG:POL 3 INV	Selects the inverted (falling) clock edge for port 3
INP:REG:SOUR 4 EXT	Selects External clock line as the clock source for port 4
INP:REG:POL 4 INV	Selects the inverted (falling) clock edge for port 4
INP:REG:SOUR 5 EXT	Selects External clock line as the clock source for port 5
INP:REG:POL 5 INV	Selects the inverted (falling) clock edge for port 5
OUT:CLOC:ENAB 0 ON	Enables the output clock for port 0
OUT:CLOC:SOUR 0 IMM	Selects the IMM (word serial event) to drive the external clock for port 0
OUT:REG:SOUR 0 IMM	Selects the IMM (word serial event) as the clock source for port 0 I/O data buffers
OUT:CLOC:ENAB 1 ON	Enables the output clock for port 1
OUT:CLOC:SOUR 1 IMM	Selects the IMM (word serial event) to drive the external clock for port 1
OUT:REG:SOUR 1 IMM	Selects the IMM (word serial event) as the clock source for port 1 I/O data buffers
OUT:CLOC:ENAB 2 ON	Enables the output clock for port 1
OUT:CLOC:SOUR 2 IMM	Selects the IMM (word serial event) to drive the external clock for port 1
OUT:REG:SOUR 2 IMM	Selects the IMM (word serial event) as the clock source for port 1 I/O data buffers
SOUR:DATA:ENAB 0 ON	Configures port 0 I/O data buffers for write mode
SOUR:DATA:ENAB 1 ON	Configures port 1 I/O data buffers for write mode
SOUR:DATA:ENAB 2 ON	Configures port 2 I/O data buffers for write mode
SOUR:DATA:ENAB 3 OFF	Configures port 3 I/O data buffers for read mode
SOUR:DATA:ENAB 4 OFF	Configures port 4 I/O data buffers for read mode
SOUR:DATA:ENAB 5 OFF	Configures port 5 I/O data buffers for read mode
SOUR:DATA 0 01	Writes data “01” to port 0’s I/O data buffer
SOUR:DATA 1 23	Writes data “23” to port 1’s I/O data buffer
SOUR:DATA 2 45	Writes data “45” to port 2’s I/O data buffer
STAT:INT:ENAB EXT 5	Set the interrupt trigger source as the port 5 clock
STAT:INT:PTR ON	Set the interrupt trigger source to the positive edge
TRIG:SEQ:IMM	Generates a word serial event to transfer data and clocks from ports 0, 1, and 2
READ? 3	Read data from port 3
READ? 4	Read data from port 4
READ? 5	Read data from port 5

See Figure 3-3 for the Write/read block diagram.

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The **INP:REG:SOUR <port> EXT** commands select the external clock for <port> as the clock input for the trigger method to input data from the UUT. When the commands are received, the VM1548 timing and control circuitry will generate the PORTENA* signal to the port decoder. The port decoder then clocks the write clock enable latch selecting the CLKINENA. The CLKINENA signals are applied to the I/O data and word buffers enabling the input clock line.

The **INP:REG:POL <port> INV** command causes the timing and control circuitry to select the falling edge of the external clock as the CLKIN <port> for the I/O data buffers.

OUT:CLOC:ENAB <port> ON commands inform the timing and control circuitry that the front panel clock lines are used as outputs. This allows the VM1548 to furnish the clock source. **OUT:CLOC:SOUR <port> IMM** commands inform the timing and control circuitry to drive the front panel clock lines using the immediate (word serial event) trigger.

The **OUT:REG:SOUR <port> IMM** commands select the immediate (word serial event) clock as the trigger method for the selected ports to output data to the UUT (VM1548 through wrap-around cable). When these commands are received, the VM1548 timing and control circuitry will generate the PORTENA* signal to the port decoder. The port decoder then clocks the write clock enable latch selecting the CLKOUTENA. The CLKOUTENA signals are applied to the I/O data and word buffers enabling the output clock line.

The **SOUR:DATA:ENAB <port> ON** enables the selected ports for a write, in this case ports 0, 1 and 2. The **SOUR:DATA:ENAB <port> OFF** enables the selected ports to read, in this case ports 3, 4 and 5. The **SOUR:DATA <port> <data>** commands writes the data into the specified ports as previously described.

The **STAT:INT:ENAB EXT 5** and **STAT:INT:PTR ON** commands enable the interrupt to occur when the CLK 5 signal is received and sets the polarity of this interrupt to the positive edge.

TRIG:SEQ:IMM command will generate a short pulse that will initiate the transfer of data from ports 0, 1 and 2 to ports 3, 4 and 5. When CLK 5 has been received, the VM1548 module sends an Interrupt Request (IRQ*) informing the slot 0 controller via the VMIP that the transfer has occurred. The **READ? <port>** will then fetch the data from the specified ports.

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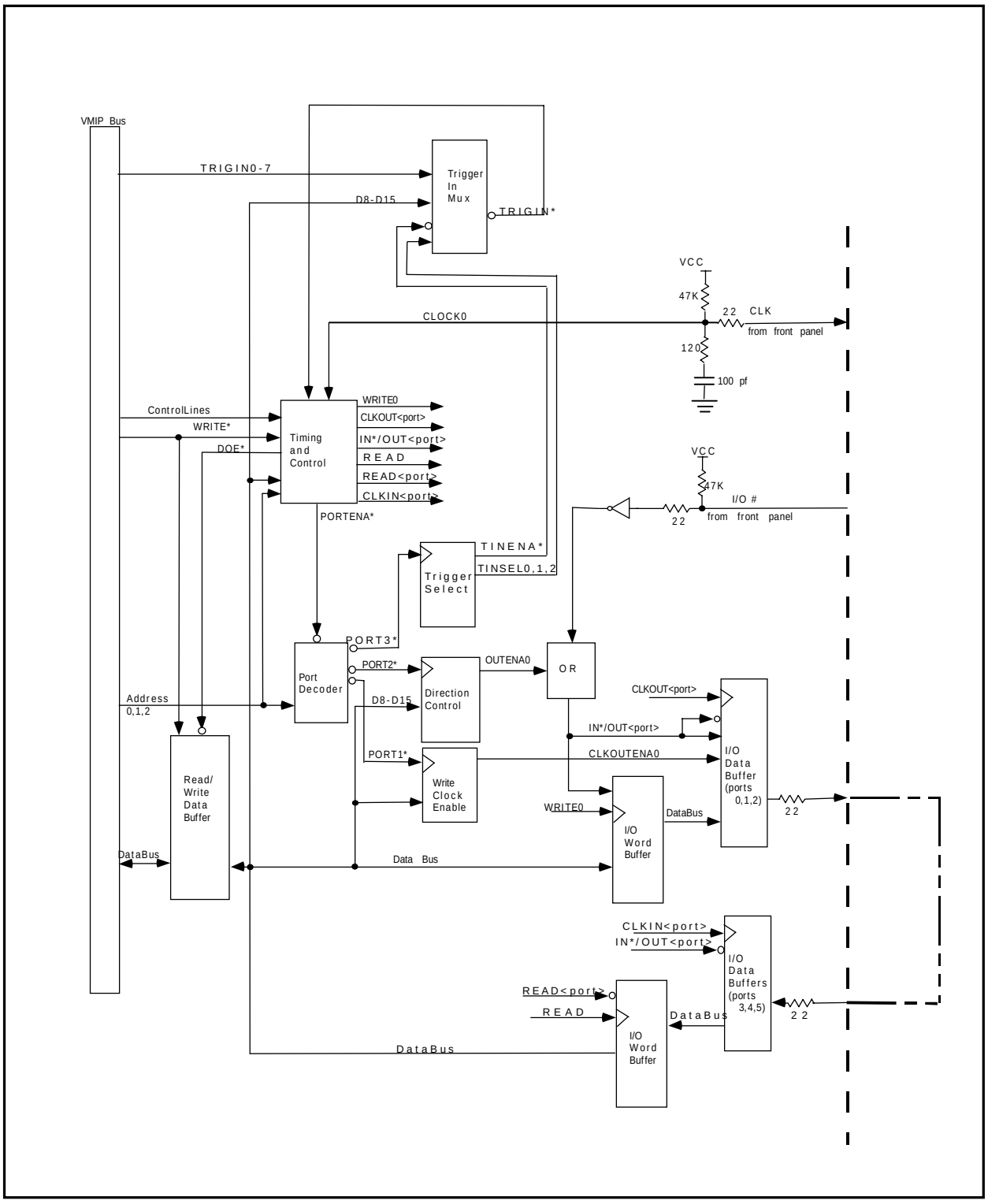


FIGURE 3-3: WRITE/READ

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TABLE 3-1: WRAP-AROUND TEST CABLE

FROM		TO	
Signal	**Pin**	**Signal**	**Pin**
DATA0.0	2	DATA3.0	36
DATA0.1	3	DATA3.1	37
DATA0.2	4	DATA3.2	38
DATA0.3	5	DATA3.3	39
DATA0.4	6	DATA3.4	40
DATA0.5	7	DATA3.5	41
DATA0.6	8	DATA3.6	42
DATA0.7	9	DATA3.7	43
I/O*0	10	I/O*3	44
CLK0	11	CLK3	45
DATA1.0	13	DATA4.0	47
DATA1.1	14	DATA4.1	48
DATA1.2	15	DATA4.2	49
DATA1.3	16	DATA4.3	50
DATA1.4	17	DATA4.4	51
DATA1.5	18	DATA4.5	52
DATA1.6	19	DATA4.6	53
DATA1.7	20	DATA4.7	54
I/O*1	21	I/O*4	55
CLK1	22	CLK4	56
DATA2.0	24	DATA5.0	58
DATA2.1	25	DATA5.1	59
DATA2.2	26	DATA5.2	60
DATA2.3	27	DATA5.3	61
DATA2.4	28	DATA5.4	62
DATA2.5	29	DATA5.5	63
DATA2.6	30	DATA5.6	64
DATA2.7	31	DATA5.7	65
I/O*2	32	I/O*5	66
CLK2	33	CLK5	67

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REGISTER ACCESS EXAMPLES

The VM1548 module supports direct register access for very high-speed data retrieval. The register map is as specified in Table 3-2.

As can be seen from the register map in Table 3-2, each 16-bit wide register is shared by two ports. Therefore, in order to program a particular port, it must be ensured that the value of the other port is untouched. This can be ensured by reading the value of the register and OR'ing the obtained value with the value to be programmed. This final value can then be written at the correct offset. This is true assuming that the function used to write to the register performs 16-bit writes.

Similarly, when a register is read, it provides the data values of two ports. Therefore, the unwanted value must be OR'd with a proper mask. This is again assuming that the function used to read the register performs 16-bit reads.

Example 1: For example in order program Port 1:

a) First, the register value at offset 0x20 is read. Assume that the value read is as given below:

`1111000010101010` (in binary format)

The lower 8 bits are the current value for Port 0. In order to maintain its value, an appropriate OR operation is required. A bit-shift operation may also be required depending on the port to be written to.

For example, if the new value to be written to Port 1 is 00001111, then the final value to be written to the register is

```
(1111000010101010 | (00001111 << 8))
```

Example 2: For example in order read Port 1:

Read the register at offset 0x20. This presents the values of Ports 0 and 1. However, since the value Port 1 is of interest, the following steps must be followed:

a) Read the register at offset 0x20. Assume that the value read is as shown below:

`1010000011110000` (in binary format)

b) Since the upper 8 bits are of interest, an appropriate mask has to be applied and the value right shifted.

The data value of port 1 is:

```
((1010000011110000 | 0xFF00) >> 8)
```


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The VM1548 digital I/O module supports direct access to the six 8-bit data ports via the Device Dependent Registers of VXIbus interface. The specific registers are located in A16 Memory at offsets 0x20 = Port1, 0x21 = Port0, 0x22 = Port3, 0x23 = Port2, 0x24 = Port5 and 0x25 = Port4. The following diagram shows A16 Memory and the VM1548 Data Port Map.

TABLE 3-2: A16 MEMORY MAP

3E		
3C		
3A		
38		
36		
34		
32		
30		
2E		
2C		
2A		
28		
26		
24	Port 5	Port 4
22	Port 3	Port 2
20	Port 1	Port 0
1E		
1C		
1A		
18		
16	[A32 Pointer Low]	
14	[A32 Pointer High]	
12	[A24 Pointer Low]	
10	[A24 Pointer High]	
E	Data Low	
C	Data High	
A	Response [/Data Extended]	
8	Protocol [/Signal] Register	
6	[Offset Register]	
4	Status / Control Register	
2	Device Type	

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VXI*PLUG&PLAY* EXAMPLES

```
/*=============================================================*/
/*
 *                          APPLICATION FUNCTION
 *                          --------------------
 */
/*=============================================================*/
Function:               vtvm1548_setupAndWriteData

Formal Parameters  ViSession instrHndl
                        - A valid session handle to the instrument.

                   ViInt16 portNumber
- This parameter is used to set the port and the clock associated with the
specified port to which the 8 bit data value is to be  written.

                        Valid Values:               Interpretation:
                        ------------            ---------------
                        vtvm1548_PORT_ZERO      Port Zero
                        vtvm1548_PORT_ONE       Port One
                        vtvm1548_PORT_TWO       Port Two
                        vtvm1548_PORT_THREE           Port Three
                        vtvm1548_PORT_FOUR      Port Four
                        vtvm1548_PORT_FIVE      Port Five

                   ViInt16 clkSource
- This parameter is used to set the source of the clock circuit associated with
the specified port.

                        Valid Values:               Interpretation:
                        ------------            --------------
                        vtvm1548_CLK_SOURCE_IMM  Word Serial Event
                        vtvm1548_CLK_SOURCE_TTLT VXIbus TRIGIN
                        vtvm1548_CLK_SOURCE_GLOB TRIGOUT
                        vtvm1548_CLK_SOURCE_NONE Ground

                   ViBoolean polarity
- This parameter is used to set the polarity of  the clock circuit associated with
the specified port. This parameter is considered only if the specified clock
source is either vtvm1548_CLK_SOURCE_TTLT or tvm1548_CLK_SOURCE_GLOB.
```


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```
                        Valid Values:                   Interpretation:
                        ------------                ---------------
                        vtvm1548_POL_NORM           Normal Polarity   (0)
                        vtvm1548_POL_INVERT               Inverted Polarity (1)

                    ViInt16 data
- This parameter is used to specify the 8 bit data value that is to be written to
the  output port.

                        Valid Range:
                        -----------
                        vtvm1548_DATA_MIN (0) to
                        vtvm1548_DATA_MAX (255).

Return Values:          Returns VI_SUCCESS if successful.
                              Else returns error value.

Description  This function is an application function that shows how the user can
use core functions to set up the specified port as output and write the specified
data value to it. It then triggers the port to output its data.
/*****************************************************************/
ViStatus _VI_FUNC vtvm1548_setupAndWriteData (ViSession instrHndl,
                              ViInt16 portNumber, ViInt16    clkSource,
                              ViBoolean polarity, ViInt16 data)
{
  /*
   * Variable used to store return status of the function.
   */
   ViStatus  status = VI_NULL;

  /*
   * Setup the specified port as output and configure the clock
   * associated with it.
   */
   status = vtvm1548_configPort (instrHndl,portNumber,vtvm1548_MODE_OUTPUT,
vtvm1548_CLK_MODE_OUT,clkSource,polarity);
if (status < VI_SUCCESS)
            return vtvm1548_ERROR_SETTING_PORT;

  /*
   * Set up the specified port's register source.
   */
   status = vtvm1548_configRegister(instrHndl,portNumber,
                        vtvm1548_CLK_SOURCE_IMM,VI_NULL);
if (status < VI_SUCCESS)
            return vtvm1548_ERROR_SETTING_REGISTER;

  /*
   * Write the input 8 bit data to the specified port.
   */
   status = vtvm1548_sourceData(instrHndl,portNumber,data);
if (status < VI_SUCCESS)
            return vtvm1548_DATA_OUT_OF_RANGE;

  /*
   * Trigger the output port using the IMMEDIATE pulse.
   */
   status = vtvm1548_triggerSeqImmediate(instrHndl);
if (status < VI_SUCCESS)
            return status;

            return VI_SUCCESS;
}
```


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```
/*****************************************************************/
Function:               vtvm1548_setupAndReadData

Formal Parameters  ViSession instrHndl
                        - A valid session handle to the instrument.

                   ViInt16 portNumber
                   - This parameter is used to specify the port
                   which is to be configured as input.

                        Valid Values:                Interpretation:
                        ------------                 ---------------
                        vtvm1548_PORT_ZERO       Port Zero
                        vtvm1548_PORT_ONE        Port One
                        vtvm1548_PORT_TWO        Port Two
                        vtvm1548_PORT_THREE            Port Three
                        vtvm1548_PORT_FOUR       Port Four
                        vtvm1548_PORT_FIVE       Port Five

                   ViInt16 clkSource
- This parameter is used to set the source of the clock circuit associated with
the specified port.

                        Valid Values:                Interpretation:
                        ------------                 --------------
                        vtvm1548_CLK_SOURCE_IMM  Word Serial Event
                        vtvm1548_CLK_SOURCE_TTLT VXIbus TRIGIN
                        vtvm1548_CLK_SOURCE_GLOB TRIGOUT
                        vtvm1548_CLK_SOURCE_NONE Ground
                   ViBoolean polarity
                   - This parameter is used to set the polarity of
                   the clock circuit associated with the specified port.
This parameter is considered only if the specified clock source is either
vtvm1548_CLK_SOURCE_TTLT or          vtvm1548_CLK_SOURCE_GLOB.

      Valid Values:                 Interpretation:
                        ------------                 --------------
                        vtvm1548_POL_NORM        Normal Polarity   (0)
                        vtvm1548_POL_INVERT            Inverted Polarity (1)

                   ViPInt16     data
-  This  parameter  returns  the  8  bit  data  value  that  has  been  read  from  the
specified input port.

Return Values:     Returns VI_SUCCESS if successful.
                             Else returns error value.

Description  This function is an application function that shows how the user can
use core functions to set up the specified port as input. It triggers the port to
input the data and reads the same.
*****************************************************************/
ViStatus _VI_FUNC vtvm1548_setupAndReadData (ViSession instrHndl,
                                             ViInt16      portNumber,
                                             ViInt16      clkSource,
                                             ViBoolean    polarity,
                                             ViPInt16     data)
{
  /*
   * Variable used to store return status of the function.
   */
   ViStatus  status= VI_NULL;

  /*
   * Setup the specified port as input and configure the clock
   * associated with it.
```


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```
   */
   status = vtvm1548_configPort (instrHnd,portNumber,
                                          vtvm1548_MODE_INPUT,
                                          vtvm1548_CLK_MODE_IN,
                                          clkSource,
                                          polarity);
if (status < VI_SUCCESS)
            return vtvm1548_ERROR_SETTING_PORT;

  /*
   * Setup the specified port's register source.
   */
   status = vtvm1548_configRegister(instrHndl,portNumber,
                                       vtvm1548_CLK_SOURCE_IMM,VI_NULL);
if (status < VI_SUCCESS)
            return vtvm1548_ERROR_SETTING_REGISTER;

  /*
   * Trigger the input port using the IMMEDIATE pulse.
   */
   status = vtvm1548_triggerSeqImmediate(instrHndl);
if (status < VI_SUCCESS)
            return status;

  /*
   * Read the 8 bit data from a specified input port.
   */
   status = vtvm1548_readInstrument(instrHndl,portNumber,data);
if (status < VI_SUCCESS)
            return status;

            return VI_SUCCESS;
}
```


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SECTION 4

COMMAND DICTIONARY

INTRODUCTION

This section presents the instrument command set. It begins with an alphabetical list of all the commands supported by the VM1548 divided into three sections: IEEE 488.2 commands, the instrument specific SCPI commands and the required SCPI commands. With each command is a brief description of its function, whether the command's value is affected by the *RST command and its reset value.

The remainder of this section is devoted to describing each command, one per page, in detail. The description is presented in a regular and orthogonal way assisting the user in the use of each command. Every command entry describes the exact command and query syntax, the use and range of parameters and a complete description of the command's purpose.

ALPHABETICAL COMMAND LISTING

The following tables provide an alphabetical listing of each command supported by the VM1548 along with a brief description. If an X is found in the column titled *RST, then the value or setting controlled by this command is possibly changed by the execution of the *RST command. If no X is found, then *RST has no effect. The Reset Value column gives the value of each command's setting when the unit is powered up or when a *RST command is executed.

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TERMINOLOGY

Port — One of six data registers accessible via the 68-pin external connector. These registers are 8 bits wide and are programmable to be bi-directional. Port is also sometimes referred to as just register.

CLK0-5 — The 6 input clocks coming from the external connector.

TRIGOUT — The selected signal from the SCPI command. This signal is referred to as GLOBAL throughout the command dictionary section. This is due to the capabilities of this signal to trigger all ports at one time. OUTPUT:TTLTRIG:SOURCE

TTLTRIGGER — The signal GLOBAL (TRIGOUT) after applying the polarity control OUTPUT:TTLTRIG:POLARITY

IMMEDIATE — This is an abbreviation for Word Serial Event. IMMEDIATE refers to the SCPI Command TRIGger[:SEQuence]:IMMediate, which will generate a very short pulse.

Clocked Mode — This refers to the method of operation of a port. The data will be latched out or in, with reference to a clock source.

Transparent Mode — This refers to the method of operation of a port. For example, if the port is being used as an output, then as soon as the data is written it will appear on the external connector. Likewise if the port is being used as an input, then the data appearing on the external connector is immediately available to be read.

Numbers — Numbers can be received by the module in decimal, hexadecimal, octal or binary. Numbers with no special leading characters are considered decimal.

Hexadecimal numbers are designated with a leading #H, i.e., #HFF is decimal 255. Octal numbers are designated with a leading #Q, i.e., #Q177 is decimal 255. Binary numbers are designated with a leading #B, i.e., #B 11111111 is decimal 255.

Queries — A query will return a value the specified register was set to. The query syntax is a command followed by a ?, i.e., INPut:TTLTrig is the set command and INPut:TTLTrig? is the query. Query only commands do not have a set command associated with it, i.e., READ?.

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TABLE 4-1: IEEE 488.2 COMMON COMMANDS

Command	Description	*RST	Reset Value
*CLS	Clears the Status Register.		
*ESE	Sets the Event Status Enable Register.		
*ESR?	Sets the Standard Event Status Register.		
*IDN?	Query the module Identification string.		
*OPC	Set the OPC bit in the Event Status Register.		
*RST	Resets the module to a known state.		
*STB?	Query the Status Byte Register.		
*TRG	Causes a trigger event to occur.		
*TST?	Starts and reports a self-test procedure.		
*WAI	Halts execution and queries.		

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TABLE 4-2: INSTRUMENT SPECIFIC SCPI COMMANDS

Command	Description	*RST	Reset Value
FORMat	Sets the output format for digital queries	X	ASCII (Decimal)
INPut:REGister:POLarity	Sets the active edge of the clock for an input port	X	Rising Edge
INPut:REGister:SOURce	Selects the source to clock input data port	X	Disabled
INPut:TTLTrig	Selects 1 of 8 VXI Trigger lines as the input trigger	X	0
INPut:TTLTrig:STATE	Enable/disable MUX that selects an input trigger	X	Disabled
OUTput:CLOCk:ENABle	Sets the Clock pin to be an output or an input	X	Input
OUTput:CLOCk:POLarity	Sets the active edge of a port's associated clock	X	Rising edge
OUTput:CLOCk:SOURce	Sets the source of a port's associated clock	X	NONE
OUTput:REGister:POLarity	Controls the polarity at which output data is latched to the specified port	X	Rising edge
OUTput:REGister:SOURce	Controls the source of the clock that will latch output data to the specified port	X	Disabled
OUTput:TTLTrig	Selects 1 of 8 VXI Trigger lines as the output trigger	X	0
OUTput: TTLTrig:POLarity	Sets the active edge of the TTL trigger	X	NORMal
OUTput: TTLTrig:SOURce	Selects the source for the internal signal TRIGOUT	X	NONE
OUTput: TTLTrig:STATE	Enable/disable MUX that selects an output trigger	X	Off
READ?	Queries an 8 bit input data port		
SOURce:DATA:ENABle	Sets an eight bit port for input or output	X	Input
SOURce:DATA	Sets the value driven by an output port	X	0
STATus:INTerrupt:ENABle	Enables or Disables Interrupts to the backplane	X	NONE
STATus:INTerrupt:PTRansition	Sets Interrupts to occur on a positive transition	X	1
STATus:INTerrupt:NTRansition	Sets Interrupts to occur on a negative transition	X	0
TRIGger:SEQuence:IMMediate	A word serial event which generates a short pulse		

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TABLE 4-3: SCPI REQUIRED COMMANDS

Command	Description	*RST	Reset Value
STATus:OPERation[:EVENt]?	Queries the Operation Status Event Register.		
STATus:OPERation:CONDition?	Queries the Operation Status Condition Register.		
STATus:OPERation:ENABle	Sets the Operation Status Enable Register.	X	0
STATus:QUEStionable[:EVENt]?	Queries the Questionable Status Event Register		
STATus:QUEStionable:CONDition?	Queries the Questionable Status Condition Register		
STATus:QUEStionable:ENABle	Sets the Questionable Status Enable Register.	X	
STATus:PRESet	Presets the Status Register.		
SYSTem:ERRor?	Queries the Error Queue		Clears queue
SYSTem:VERSion?	Queries which version of the SCPI standard the module complies with.		N/A

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COMMAND DICTIONARY

The remainder of this section is devoted to the actual command dictionary. Each command is fully described on its own page. In defining how each command is used, the following items are described:

Purpose	Describes the purpose of the command.
Type	Describes the type of command such as an event or setting.
Command Syntax	Details the exact command format.
Command Parameters	Describes the parameters sent with the command and their legal range.
Reset Value	Describes the values assumed when the *RST command is sent.
Query Syntax	Details the exact query form of the command.
Query Parameters	Describes the parameters sent with the command and their legal range. The default parameter values are assumed the same as in the command form unless described otherwise.
Query Response	Describes the format of the query response and the valid range of output.
Description	Describes in detail what the command does and refers to additional sources.
Examples	Present the proper use of each command and its query (when available).
Related Commands	Lists commands that affect the use of this command or commands that are affected by this command.

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COMMON SCPI COMMANDS

*CLS

Purpose	Clears all status and event registers	
Type	IEEE 488.2 Common Command	
Command Syntax	*CLS	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	N/A	
Query Parameters	N/A	
Query Response	N/A	
Description	This command clears the Status Event Register, Operation Status Register and the Questionable Data/Signal Register. It also clears the OPC flag and clears all queues (except the output queue).	
Examples	**Command / Query**	**Response / Descriptions**
	`*CLS`	*(Clears all status and event registers)*
Related Commands	N/A	

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*ESE

Purpose	Sets the bits of the Event Status Enable Register
Type	IEEE 488.2 Common Command
Command Syntax	*ESE <mask>
Command Parameters	<mask> = numeric ASCII value
***RST Value**	N/A, the parameter is required
Query Syntax	*ESE?
Query Parameters	N/A
Query Response	Numeric ASCII value from 0 to 255
Description	The Event Status Enable (ESE) command is used to set the bits of the Event Status Enable Register. See ANSI/IEEE 488.2-1987 section 11.5.1 for a complete description of the ESE register. A value of 1 in a bit position of the ESE register enables generation of the Event Status Bit (ESB) in the Status Byte by the corresponding bit in the Event Status Register (ESR). If the ESB is set in the Service Request Enable (SRE) register, then an interrupt will be generated. See the *ESR? command for details regarding the individual bits. The ESE register layout is: Bit 0 - Operation Complete Bit 1 - Request Control Bit 2 - Query Error Bit 3 - Device Dependent Error Bit 4 - Execution Error Bit 5 - Command Error Bit 6 - User Request Bit 7 - Power On The Event Status Enable query reports the current contents of the Event Status Enable Register.

Examples	**Command / Query**	**Response *(Description)***
	`*ESE 36` `*ESE?`	36 *(Returns the value of the event status enable register)*

Related Commands	*ESR?

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*ESR?

Purpose	Queries and clears the Standard Event Status Register
Type	IEEE 488.2 Common Command
Command Syntax	N/A
Command Parameters	N/A
***RST Value**	N/A
Query Syntax	ESR?
Query Parameters	N/A
Query Response	Numeric ASCII value from 0 to 255
Description	The Event Status Register (ESR) query queries and clears the contents of the Standard Event Status Register. This register is used in conjunction with the ESE register to generate the Event Status Bit (ESB) in the Status Byte. The layout of the ESR is: Bit 0 - Operation Complete Bit 1 - Request Control Bit 2 - Query Error Bit 3 - Device Dependent Error Bit 4 - Execution Error Bit 5 - Command Error Bit 6 - User Request Bit 7 - Power On The Operation Complete bit is set when it receives an *OPC command. The Query Error bit is set when data is over-written in the output queue. This could occur if one query is followed by another without reading the data from the first query. The Execution Error bit is set when an execution error is detected. Errors that range from -200 to -299 are execution errors. The Command Error bit is set when a command error is detected. Errors that range from -100 to -199 are command errors. The Power On bit is set when the module is first powered on or after it receives a reset via the VXI Control Register. Once the bit is cleared (by executing the *ESR? command) it will remain cleared.

Examples	**Command / Query**	**Response *(Description)***
	`*ESR?`	4

Related Commands	*ESE

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*IDN?

Purpose	Queries the module for its identification string	
Type	IEEE 488.2 Common Command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	*IDN?	
Query Parameters	N/A	
Query Response	ASCII character string	
Description	The Identification (IDN) query returns the identification string of the module. The response is divided into four fields separated by commas. The first field is the manufacturer's name, the second field is the model number, the third field is an optional serial number and the fourth field is the firmware revision number. If a serial number is not supplied, the third field is set to 0 (zero).	
Examples	**Command / Query**	**Response *(Description)***
	`*IDN`	VXI Technology, Inc.,VM1548,0,1.0 *(The revision listed here is for reference only; the response will always be the current revision of the instrument.)*
Related Commands	N/A	

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*OPC

Purpose	Sets the OPC bit in the Event Status Register	
Type	IEEE 488.2 Common Command	
Command Syntax	*OPC	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	*OPC?	
Query Parameters	N/A	
Query Response	1	
Description	The Operation Complete (OPC) command sets the OPC bit in the Event Status Register when all pending operations have completed. The OPC query will return a 1 to the output queue when all pending operations have completed.	
Examples	**Command / Query**	**Response *(Description)***
	`*OPC` `*OPC?`	*(Sets the OPC bit in the Event Status Register)* 1 *(Returns the value of the Event Status Register)*
Related Commands	*WAI	

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*RST

Purpose	Resets the module's hardware and software to a known state	
Type	IEEE 488.2 Common Command	
Command Syntax	*RST	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	N/A	
Query Parameters	N/A	
Query Response	N/A	
Description	The Reset (RST) command resets the module's hardware and software to a known state. See the command index at the beginning of this chapter for the default parameter values used with this command.	
Examples	**Command / Query**	**Response *(Description)***
	`*RST`	*(Resets the module)*
Related Commands	N/A	

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*SRE

Purpose	Sets the service request enable register
Type	IEEE 488.2 Common Command
Command Syntax	*SRE <mask>
Command Parameters	<mask> = Numeric ASCII value from 0 to 255
***RST Value**	None – Required Parameter
Query Syntax	*SRE?
Query Parameters	N/A
Query Response	Numeric ASCII value from 0 to 255
Description	The Service Request Enable (SRE) mask is used to control which bits in the status byte generate back plane interrupts. If a bit is set in the mask that newly enables a bit set in the status byte and interrupts are enabled, the module will generate a REQUEST TRUE event via an interrupt. See the *STB? Command for the layout of bits. **Note:** Bit 6 is always internally cleared to zero as required by IEEE 488.2 section 11.3.2.3. The layout of the Service Request Enable Register is: Bit 0 – Unused Bit 1 – Unused Bit 2 – Error Queue Has Data Bit 3 – Questionable Status Summary (Not Used) Bit 4 – Message Available Bit 5 – Event Status Summary Bit 6 – 0 (per IEEE 488.2 section 11.3.2.3) Bit 7 – Operation Status Summary

Examples	**Command / Query**	**Response *(Description)***
	`*SRE 4`	*(Sets the service request enable register)*
	`*SRE?`	4 *(Returns the value of the SRE register)*
Related Commands	N/A	

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*STB?

Purpose	Queries the Status Byte Register	
Type	IEEE 488.2 Common Command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	*STB?	
Query Parameters	N/A	
Query Response	Numeric ASCII value from 0 to 255	
Description	The Read Status Byte (STB) query fetches the current contents of the Status Byte Register. See the IEEE 488.2 specification for additional information regarding the Status byte Register and its use. The layout of the Status Register is: Bit 0 – Unused Bit 1 – Unused Bit 2 – Error Queue Has Data Bit 4 – Questionable Status Summary (not used) Bit 5 – Message Available Bit 6 – Master Summary Status Bit 7 – Operation Status Summary	
Examples	**Command / Query**	**Response *(Description)***
	`*STB?`	16 (*Queries the Status Byte Register)*
Related Commands	N/A	

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*TRG

Purpose	Causes a trigger event to occur	
Type	IEEE 488.2 Common Command	
Command Syntax	*TRG	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	N/A	
Query Parameters	N/A	
Query Response	N/A	
Description	The Trigger command causes a trigger event to occur.	
Examples	**Command / Query**	**Response *(Description)***
	`*TRG`	*(Triggers an event)*
Related Commands	N/A	

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*TST?

Purpose	Causes a self-test procedure to occur and queries the results	
Type	IEEE 488.2 Common Command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	*TST?	
Query Parameters	N/A	
Query Response	Numeric ASCII value from 0 to 143	
Description	The Self-Test query causes the VM1548 to run its self-test procedures and report on the results.	
Examples	**Command / Query**	**Response *(Description)***
	`*TST`	0 (*Begins the self-test procedure returns the result)*
Related Commands	N/A	

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*WAI

Purpose	Halts execution of additional commands and queries until the No Operation Pending message is true	
Type	IEEE 488.2 Common Command	
Command Syntax	*WAI	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	N/A	
Query Parameters	N/A	
Query Response	N/A	
Description	The Wait to Continue command halts the execution of commands and queries until the No Operation Pending message is true. This command makes sure that all previous commands have been executed before proceeding. It provides a way of synchronizing the module with its commander.	
Examples	**Command / Query**	**Response *(Description)***
	`*WAI`	*(Pauses the execution of additional commands until the No Operation Pending message is true.)*
Related Commands	*OPC	

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INSTRUMENT SPECIFIC SCPI COMMANDS

FORMat

Purpose	Sets the output format for digital queries	
Type	Setting	
Command Syntax	FORMat <type>	
Command Parameters	<type> = ASCii, HEXadecimal, OCTal, BINary	
***RST Value**	ASCii	
Query Syntax	FORMat?	
Query Parameters	None	
Query Response	ASC | HEX | OCT | BIN	
Description	The Format command sets the form of returned data from the instrument. This command applies only to SOURce:DATA? <port #> READ? <port #> ASCii specifies numbers expressed in decimal. Leading zeros are suppressed. HEXadecimal expresses numbers in a 2 digit leading 0 alphanumeric format. Numbers A-F are in capitals. OCTal expresses numbers in a 3 digit leading 0 format. BINary expressed numbers in an 8 digit leading 0 format.	
Examples	**Command / Query**	**Response *(Description)***
	`FORM ASC` `SOUR:DATA 0,58` `SOUR:DATA? 0` `FORM HEX` `SOUR:DATA? 0` `FORM OCT` `SOUR:DATA? 0` `FORM BIN` `SOUR:DATA? 0` `FORM?`	58 *(Returns the data value in decimal format)* *(Sets the data format to hexadecimal)* #H3A *(Returns the data value in hexadecimal format)* *(Sets the data value to an octal format)* #Q072 *(Returns the data value in octal format)* *(Returns the data value in decimal format)* #B00111010 *(Returns the data value in binary format)* BIN
Related Commands	SOURce:DATA? <port> READ? <port>	

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INPut:REGister:POLarity

Purpose	Selects the active clock edge of the input register.	
Type	Setting	
Command Syntax	INPut:REGister:POLarity <port #> <edge>	
Command Parameters	<port #> = 0,1,2,3,4,5 <edge> = NORMal | INVert	
***RST Value**	NORMal	
Query Syntax	INPut:REGister:POLarity? <port #>	
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5	
Query Response	NORM | INV	
Description	A Polarity of NORMal would cause the data to be latched in, on a rising edge of the clock. A Polarity of INVert would cause the data to be latched in, on a falling edge of the clock. Note, that it is important to remember that the input register must be operating in clocked mode in order for the polarity to affect the Input Register latching.	
Examples	**Command / Query**	**Response *(Description)***
	`INP:REG:POL 0 NORM` `INP:REG:POL? 0`	NORM
Related Commands	INPut:REGister:SOURce <port #> <source>	

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INPut:REGister:SOURce

Purpose	To control the selection of the signal to be used for the specified port's input clock source
Type	Setting
Command Syntax	INPut:REGister:SOURce <port #> <source>
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <source> = NONE | TTLTrig | EXTernal | IMMediate | GLOBal
***RST Value**	NONE
Query Syntax	INPut:REGister:SOURce? <port #>
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5
Query Response	NONE | TTLT | EXT | IMM | GLOB
Description	The Input Register Source command controls what signal will be used for the specified port's input clock. Source Parameter Description NONE: This disables the specified port's input clock. The data appearing on the specified port is read without any latching. TTLTrig: This selects the VXIbus TRIGIN as the clock source. TRIGIN can be 1 of 8 TTL trigger lines on the VXI bus. *See INPut:TTLTrig.* EXTernal: This selects the port's associated CLK line coming from the 68 pin external connector as the clock source. IMMediate: This selects the Word Serial Event as the clock source. *See: TRIGger:SEQuence:IMMediate*. GLOBal: This selects TRIGOUT as the clock source. *See: OUTPut:TTLTrig:SOURce.*

Examples	**Command / Query**	**Response *(Description)***
	`INP:REG:SOUR 0 TTLT` `INP:REG:SOUR? 0`	TTLT

Related Commands	INPut:REGister:POLarity <port #><edge>

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INPut:TTLTrig

Purpose	To select a specific VXIbus trigger line as TRIGIN	
Type	Setting	
Command Syntax	INPut:TTLTrig <n>	
Command Parameters	<n> = 0, 1, 2, 3, 4, 5, 6, 7	
***RST Value**	0	
Query Syntax	INPut:TTLTrig?	
Query Parameters	N/A	
Query Response	Numeric ASCII value between 0 and 7	
Description	The Input TTLTrig command controls which of the 8 VXI trigger lines will be selected as TRIGIN. The 8 VXI trigger lines feed into an 8 to 1 multiplexer. The selected signal is called TRIGIN.	
Examples	**Command / Query**	**Response *(Description)***
	`INP:TTLT 0` `INP:TTLT?`	0
Related Commands	INPut:TTLTrig:STATe <boolean>	

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INPut:TTLTrig:STATE

Purpose	To enable or disable the multiplexer that controls the selection of the VXI bus trigger line as TRIGIN.	
Type	Setting	
Command Syntax	INPut:TTLTrig:STATE <boolean>	
Command Parameters	<boolean> = 0 | 1 | OFF | ON	
***RST Value**	0	
Query Syntax	INPut:TTLTrig:STATE?	
Query Parameters	N/A	
Query Response	0 | 1	
Description	The Input TTLTrig state command enables or disables the multiplexer allowing the selection of a specific VXI trigger line as TRIGIN.	
Examples	**Command / Query**	**Response *(Description)***
	`INP:TTLT:STATE 0` `INP:TTLT:STATE?`	0
Related Commands	INPut:TTLTrig <n>	

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OUTput:CLOCk:ENABle

Purpose	Sets the direction in which the port's associated external clock line is driven
Type	Setting
Command Syntax	OUTput:CLOCk:ENABle <port #> <boolean>
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <boolean> = 0 | 1 | OFF | ON
***RST Value**	0
Query Syntax	OUTput:CLOCK:ENABle? <port #>
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5
Query Response	0 | 1
Description	The output clock enable command determines which direction the associated port's external clock line will be driven. This clock line is a pin on the 68-pin external connector. 0 or OFF - Means the associated port's external clock line will be an input. 1 or ON - Means the associated port's external clock line will be an output.

Examples	**Command / Query**	**Response *(Description)***
	`OUT:CLOC:ENAB 0 ON`	
	`OUT:CLOC:ENAB? 0`	1

Related Commands	OUTput:CLOCk:POLarity <port> <edge> OUTput:CLOCk:SOURce <port> <source>

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OUTput:CLOCk:POLarity

Purpose	To control the polarity of the specified port's external clock line.	
Type	Setting	
Command Syntax	OUTput:CLOCk:POLarity <port #> <edge>	
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <edge> = NORMal | INVert	
***RST Value**	NORMal	
Query Syntax	OUTput:CLOCk:POLarity? <port #>	
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5	
Query Response	NORM | INV	
Description	The output clock polarity command controls the polarity of the specified port's external clock line. There are six individual clock circuits (see clock circuit description). A polarity of NORMal will produce a rising edge clock on the 68-pin external connector. A polarity of INVert will produce a falling edge clock on the 68-pin external connector. Note: it is important to remember that the output clock source should be either GLOBAL or one of the eight TTLTrigger lines to control polarity.	
Examples	**Command / Query**	**Response *(Description)***
	`OUT:CLOC:POL 0 NORM` `OUT:CLOC:POL? 0`	NORM
Related Commands	OUTput:CLOCk:ENABle <port> <boolean> OUTput:CLOCk:SOURce <port> <source>	

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OUTput:CLOCk:SOURce

Purpose	To select a signal to be used as the source for the output clock appearing on the 68-pin external connector.
Type	Setting
Command Syntax	OUTput:CLOCk:SOURce <port #> <source>
Command Parameters	<port # > = 0, 1, 2, 3, 4, 5 <source> = NONE | TTLT | IMM | GLOB
***RST Value**	NONE
Query Syntax	OUTput:CLOCk:SOURce? <port #>
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5
Query Response	NONE | TTLT | IMM | GLOB
Description	The output clock source command selects a signal to be used as the source for the output clock, appearing on the 68-pin external connector. Source Parameter Description NONE: This parameter will select GROUND as the clock source. TTLTrig: This selects the VXIbus TRIGIN as the clock source. TRIGIN can be 1 of 8 trigger lines on the VXI bus. *See INPut:TTLTrig.* IMMediate: This selects the Word Serial Event as the clock source. *See TRIGger:SEQuence:IMMediate.* GLOBal: This selects TRIGOUT as the clock source. *See OUTPut:TTLTrig:SOURce.*

Examples	**Command / Query**	**Response *(Description)***
	`OUT:CLOC:SOUR 0 TTLT` `OUT:CLOC:SOUR? 0`	 TTLT

Related Commands	OUTput:CLOCk:ENABle <port> <boolean> OUTput:CLOCk:POLarity <port> <edge>

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OUTput:REGister:POLarity

Purpose	Controls the polarity at which output data is latched to the specified port	
Type	Setting	
Command Syntax	OUTput:REGister:POLarity <port #> <edge>	
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <edge> = NORMal | INVert	
***RST Value**	NORMal	
Query Syntax	OUTput:REGister:POLarity? <port #>	
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5	
Query Response	NORM | INV	
Description	The Output Register Polarity command controls the polarity at which output data is latched to the specified port. A polarity of NORMal would cause the data to be latched out on a rising edge of the clock. A Polarity of INVert would cause the data to be latched out on a falling edge of the clock. Note, that it is important to remember that the output register must be operating in clocked mode in order for the polarity to affect the Output Register latching.	
Examples	**Command / Query**	**Response *(Description)***
	`OUT:REG:POL 0 NORM` `OUT:REG:POL? 0`	NORM
Related Commands	OUTput:REGister:SOURce <port> <source>	

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OUTput:REGister:SOURce

Purpose	Controls the source of the clock that will latch output data to the specified port
Type	Setting
Command Syntax	OUTput:REGister:SOURce <port #> <source>
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <source> = NONE | TTLTrig | EXTernal | IMMediate | GLOBal
***RST Value**	NONE
Query Syntax	OUTput:REGister:SOURce? <port #>
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5
Query Response	NONE | TTLT | EXT | IMM | GLOB
Description	The Output Register Source command controls which clock source will be used to clock data to the output data port. Source Parameter Description NONE: This disables the specified port's output clock. The data appearing on the specified port will latch out immediately. TTLTrig: This selects the VXIbus TRIGIN as the clock source. TRIGIN can be 1 of 8 trigger lines on the VXI bus. *See INPut:TTLTrig.* EXTernal: This selects the port's associated CLK line coming from the 68 pin external connector as the clock source. IMMediate: This selects the Word Serial Event as the clock source. *See TRIGger:SEQuence:IMMediate.* GLOBal: This selects TRIGOUT as the clock source. *See OUTPut:TTLTrig:SOURce.* Note: The **NONE** selection is single buffered; all other selections are double buffered.
Examples	**Command / Query**: `OUT:REG:SOUR 0 IMM` `OUT:REG:SOUR? 0` **Response *(Description)***: IMM
Related Commands	OUTput:REGister:POLarity INPut:TTLTrigger INPut:TTLTrig:STATe *TRG TRIGger:SEQuence:IMMediate OUTput:TTLTrig:SOURce

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OUTput:TTLTrig

Purpose	To select a specific VXIbus trigger line as TRIGOUT	
Type	Setting	
Command Syntax	OUTput:TTLTrig <n>	
Command Parameters	<n> = 0,1,2,3,4,5,6,7	
***RST Value**	0	
Query Syntax	OUTput:TTLTrig?	
Query Parameters	N/A	
Query Response	0, 1, 2, 3, 4, 5,	
Description	The Output TTLTrig command controls which of the 8 VXI trigger lines will be configured as TRIGOUT	
Examples	**Command / Query**	**Response *(Description)***
	`OUT:TTLT 0` `OUT:TTLT?`	0
Related Commands	OUTput:TTLTrig:STATE <boolean> OUTput:TTLTrig:SOURce <source>	

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OUTput:TTLTrig:POLarity

Purpose	To control the polarity of the TTL TRIGGER signal	
Type	Setting	
Command Syntax	OUTput:TTLTrig:POLarity <edge>	
Command Parameters	<edge> = NORMal | INVert	
***RST Value**	NORMal	
Query Syntax	OUTput:TTLTrig:POLarity?	
Query Parameters	None	
Query Response	NORM | INV	
Description	The Output TTLTrig polarity command controls the polarity of the TTL TRIGGER signal driving the VXI trigger line. When polarity is NORMal the selected VXIbus trigger line will provide a rising edge trigger. When polarity is INVerted the selected VXIbus trigger line will provide a falling edge trigger. Note: It is important to remember that the output TILT Source should be one of the six external clocks.	
Examples	**Command / Query**	**Response *(Description)***
	`OUT:TTLT:POL NORM` `OUT:TTLT:POL?`	NORM
Related Commands	OUTput:TTLTrig <n> OUTput:TTLTrig:STATe <boolean> OUTput:TTLTrig:SOURce <source>	

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OUTput:TTLTrig:SOURce

Purpose	Selects the source for the internal signal TRIGOUT
Type	Setting
Command Syntax	OUTput:TTLTrig:SOURce <source>
Command Parameters	<source> = EXTernal0-5 | IMMediate | NONE
***RST Value**	NONE
Query Syntax	OUTput:TTLTrig:SOURce?
Query Parameters	N/A
Query Response	EXT0-5 | IMM | NONE
Description	The Output TTLTrig Source command selects which signal (EXTernal0-5, IMMediate or NONE) will be used as the TRIGOUT signal. The TRIGOUT signal is referred to throughout this manual as GLOBAL. Source Parameter Description EXTernal0-5: Selects one of the six external clocks as TRIGOUT. See the clock circuit description. IMMediate: This selects the Word Serial Trigger event as TRIGOUT. *See *TRG and TRIGger:SEQuence:IMMediate.* NONE: This parameter routes Ground to TRIGOUT thereby selecting no signal as TRIGOUT.

Examples	**Command / Query**	**Response *(Description)***
	`OUT:TTLT:SOUR IMM` `OUT:TTLT:SOUR?`	IMM

Related Commands	INPut:REGister:SOURce OUTput:CLOCk:SOURce OUTput:REGister:SOURce OUTput:TTLTrig OUTput:TTLTrig:STATe OUTput:TTLTrig:POLarity STATus:INTerrupt:ENABle

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OUTput:TTLTrig:STATE

Purpose	To enable or disable the TTL TRIGGER driving the VXIbus trigger lines	
Type	Setting	
Command Syntax	OUTput:TTLTrig:STATE <boolean>	
Command Parameters	<boolean> = 0 | 1 | OFF | ON	
***RST Value**	0	
Query Syntax	OUTput:TTLTrig:STATE?	
Query Parameters	N/A	
Query Response	0 | 1	
Description	The Output TTLTrig State command enables or disables the selected trigger line driven by the TTL TRIGGER onto the VXIbus.	
Examples	**Command / Query**	**Response *(Description)***
	`OUT:TTLT:STATE OFF` `OUT:TTLT:STATE?`	0
Related Commands	OUTput:TTLTrig <n> OUTput:TTLTrig:SOURce <source>	

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READ?

Purpose	To obtain an 8-bit value from one of the input ports.	
Type	Query	
Command Syntax	None - Query Only	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	READ? <port #>	
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5	
Query Response	Numeric ASCII value from 0 to 255	
Description	The Read command will fetch data from the specified input port. By definition this command is a query and will respond with the value read from the data register. The format of the returned data is set with the FORMat command. This command requires that the register be enabled as an input port. If the port is configured as an output the current value is returned. The operation mode of the register (clocked or transparent) can also affect what data is currently in the register.	
Examples	**Command / Query**	**Response *(Description)***
	`READ? 2`	*(Returns the data currently in the register)*
Related Commands	SOURce:DATA:ENABle <port> <boolean> INPut:REGister:SOURce <port> <source> FORMat <type>	

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SOURce:DATA:ENABle

Purpose	Sets the direction in which the module's ports will be driven	
Type	Setting	
Command Syntax	SOURce:DATA:ENABle <port #> <boolean>	
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <boolean> = 0 | 1 | OF | ON	
***RST Value**	0	
Query Syntax	SOURce:DATA:ENABle? <port #>	
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5	
Query Response	0 | 1	
Description	The Source Data Enable command controls the direction of the I/O data buffers as either read or write. ON or 1 sets the port as an output, OFF or 0 sets the port as an input.	
Examples	**Command / Query**	**Response *(Description)***
	`SOUR:DATA:ENAB 0 ON` `SOUR:DATA:ENAB? 0`	1
Related Commands	SOURce:DATA <n> READ? <port #>	

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SOURce:DATA

Purpose	Writes an 8-bit data value to the specified output port
Type	Event
Command Syntax	SOURce:DATA <port #> <n>
Command Parameters	<port #> = 0, 1, 2, 3, 4, 5 <n> = 0 - 255
***RST Value**	0 on all ports
Query Syntax	SOURce:DATA? <port #>
Query Parameters	<port #> = 0, 1, 2, 3, 4, 5
Query Response	0 – 255 The query returns the last value written to the data register, regardless of the direction the data register is currently being driven. The format of the returned information is determined by the FORMat command.
Description	The Source Data command will write an 8-bit value to the specified output port. This command requires that the register be enabled as an output port. The operation mode of the register (clocked or transparent) can also affect what data is actually presented to the external connector.
Examples	**Command / Query** / **Response *(Description)***
	`SOUR:DATA 0 87`
	`SOUR:DATA? 0` / 87
Related Commands	SOURce:DATA:ENABle <port> <boolean> OUTput:REGister:SOURce <port> <source> FORMat <type>

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STATus:INTerrupt:ENABle

Purpose	Enables and sets the interrupt trigger source, or disables the interrupt to the backplane.
Type	Setting
Command Syntax	STATus:INTerrupt:ENABle <source>
Command Parameters	<source> = EXTernal0-5, GLOBal, NONE
***RST Value**	NONE
Query Syntax	STATus:INTerrupt:ENABle?
Query Parameters	N/A
Query Response	EXT0-5, GLOB, NONE
Description	The Status Interrupt enable command selects a source for the interrupt trigger. Source Parameter Description EXT 0-5: This selects 1 of 6 external clocks. See the clock circuit description. GLOBal: This selects TRIGOUT as the interrupt trigger. See TTLTRIG diagram. NONE: This parameter will select GROUND as the interrupt trigger source, thus providing a logic level low.

Examples	**Command / Query**	**Response *(Description)***
	`STAT:INT:ENAB EXT3` `STAT:INT:ENAB?`	 EXT3

Related Commands	STATus:INTerrupt:PTRansition <boolean> STATus:INTerrupt:NTRansition <boolean>

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STATus:INTerrupt:NTRansition

Purpose	Sets the transition on which the interrupt trigger will occur
Type	Setting
Command Syntax	STATus:INTerrupt:NTRansition <boolean>
Command Parameters	<boolean> = 0 | 1 | OFF | ON
***RST Value**	OFF
Query Syntax	STATus:INTerrupt:NTRransition?
Query Parameters	N/A
Query Response	<boolean> = 0 | 1 | OFF | ON
Description	The Status Interrupt NTRansition sets the transition on which the interrupt trigger will occur. If the negative transition is set to on, then a falling edge trigger will generate an interrupt. If the negative transition is off then a rising edge trigger will generate an interrupt. Note: It is important to remember that the interrupt trigger source should be either GLOBAL or 1 of the 6 external clocks for setting the interrupt trigger source to occur on a negative transition.

Examples

Command / Query	**Response *(Description)***
`STAT:INT:NTR 1`	
`STAT:INT:NTR?`	1
`STAT:INT:NTR 0`	
`STAT:INT:NTR?`	0
`STAT:INT:PTR?`	1

Related Commands	STATus:INTerrupt:ENABle <source> STATus:INTerrupt:PTRansition <boolean>

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STATus:INTerrupt:PTRansition

Purpose	Sets the transition on which the Interrupt Trigger will occur
Type	Setting
Command Syntax	STATus:INTerrupt:PTRansition <boolean>
Command Parameters	<boolean> = 0 | 1 | OFF | ON
***RST Value**	ON
Query Syntax	STATus:INTerrupt:PTRransition?
Query Parameters	N/A
Query Response	<boolean> = 0 | 1 | OFF | ON
Description	The Status Interrupt PTRansition sets the transition on which the interrupt trigger will occur. If the positive transition is set to on, then a rising edge trigger will generate an interrupt. If the positive transition is off then a falling edge trigger will generate an interrupt. Note: It is important to remember that the interrupt trigger source should be either GLOBAL or 1 of 6 external clocks for setting the interrupt trigger source to occur on a positive transition.

Examples

Command / Query	**Response *(Description)***
`STAT:INT:PTR 1`	
`STAT:INT:PTR?`	1
`STAT:INT:PTR 0`	
`STAT:INT:PTR?`	0
`STAT:INT:NTR?`	1

Related Commands	STATus:INTerrupt:ENABle <source> STATus:INTerrupt:NTRansition <boolean>

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TRIGger:SEQuence:IMMediate

Purpose	A word serial event which generates a short pulse	
Type	Event	
Command Syntax	TRIGger:SEQuence:IMMediate	
Command Parameters	None	
***RST Value**	N/A	
Query Syntax	None	
Query Parameters	N/A	
Query Response	N/A	
Description	This command generates a short pulse or a word serial event for the trigger signal.	
Examples	**Command / Query**	**Response *(Description)***
	`TRIG:SEQ:IMM`	
Related Commands	*TRG	

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REQUIRED SCPI COMMANDS

STATus:OPERation?

Purpose	Queries the Operation Status Event Register	
Type	Required SCPI command	
Command Syntax	None - Query Only	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	STATus:OPERation[:EVENt]?	
Query Parameters	None	
Query Response	0	
Description	The Status Operation Event Register query is included for SCPI compliance. The VM1548 does not alter any of the bits in this register and always reports a 0.	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:OPER?`	0
Related Commands	None	

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STATus:OPERation:CONDition?

Purpose	Queries the Operation Status Register's condition register	
Type	Required SCPI command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	STATus:OPERation:CONDition?	
Query Parameters	N/A	
Query Response	0 | 32	
Description	The Operation Status Condition Register query is provided for SCPI compliance only. The VM1548 does not alter the state of any of the bits in this register and always reports a 0.	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:OPER:COND?`	0 *(Indicates that no bits are set in the Operation Status register)*
Related Commands	STATus:OPERation:ENABle STATus:OPERation[:EVENt]	

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STATus:OPERation:ENABle

Purpose	Sets the Operation Status Enable Register	
Type	Required SCPI command	
Command Syntax	STATus:OPERation:ENABle <NRf>	
Command Parameters	<NRf >= numeric ASCII value from 0 to 32767	
***RST Value**	0	
Query Syntax	STATus:OPERation:ENABle?	
Query Parameters	None	
Query Response	Numeric ASCII value from 0 to 32767	
Description	The Operation Status Enable Register is included for SCPI compatibility and the VM1548 does not alter any of the bits in this register. The register layout is as follows: Bit 0 - Calibrating Bit 1 - Setting Bit 2 - Ranging Bit 3 - Sweeping Bit 4 - Measuring Bit 5 - Waiting for trigger Bit 6 - Waiting for arm Bit 7 - Correcting	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:OPER:ENAB 0` `STAT:OPER:ENAB?`	 0
Related Commands	None	

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STATus:PRESet

Purpose	Presets the Status Registers	
Type	Required SCPI command	
Command Syntax	STATus:PRESet	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	N/A	
Query Parameters	N/A	
Query Response	N/A	
Description	The Status Preset command presets the Status Registers. The Operational Status Enable Register is set to 0 and the Questionable Status Enable Register is set to 0. This command is provided for SCPI compliance only.	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:PRES`	
Related Commands	N/A	

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STATus:QUEStionable:CONDition?

Purpose	Queries the Questionable Status Condition Register	
Type	Required SCPI command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	STATus:QUEStionable:CONDition?	
Query Parameters	N/A	
Query Response	0	
Description	The Questionable Status Condition Register query is provided for SCPI compliance only. The VM1548 does not alter any bits in this register and a query always reports a 0.	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:QUES:COND?`	0
Related Commands	N/A	

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STATus:QUEStionable:ENABle

Purpose	Sets the Questionable Status Enable Register	
Type	Required SCPI command	
Command Syntax	STATus:QUEStionable:ENABle <NRf>	
Command Parameters	<NRf> = numeric ASCII value from 0 to 32767	
***RST Value**	<NRf> must be supplied	
Query Syntax	STATus:QUEStionable:ENABle?	
Query Parameters	N/A	
Query Response	<NRf> = Numeric ASCII value from 0 to 32767	
Description	The command sets the bits in the Questionable Data/Signal Register's enable register to be reported to the summary bit (sets Status Byte Register bit 3 to true). The Status Questionable Enable query reports the contents of the Questionable Data/Signal Register's enable register, then clears the register contents and enters the value into the computer	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:QUES:ENAB 64` `STAT:QUES:ENAB?`	64
Related Commands	N/A	

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STATus:QUEStionable[:EVENt]?

Purpose	Queries the Questionable Status Event Register	
Type	Required SCPI command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	STATus:QUEStionable[:EVENt]?	
Query Parameters	N/A	
Query Response	Decimal number	
Description	The query reports the bits set in the event register of the Questionable Data/Signal register. This command reads the event register, then clears all bits in the event register and enters the value into the computer.	
Examples	**Command / Query**	**Response *(Description)***
	`STAT:QUES?`	0
Related Commands	N/A	

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SYSTem:ERRor?

Purpose	Queries the Error Queue	
Type	Required SCPI command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	Clears queue	
Query Syntax	SYSTem:ERRor?	
Query Parameters	N/A	
Query Response	ASCII string	
Description	The System Error query is used to retrieve error messages from the error queue. The error queue will maintain two error messages. If additional errors occur, the queue will overflow and the subsequent error messages will be lost. In the case of an overflow, an overflow message will replace the second error message. See the SCPI standard Volume 2: Command Reference for details on errors and reporting them.	
Examples	**Command / Query**	**Response *(Description)***
	`SYST:ERR?`	-350, “Queue overflow”
Related Commands	N/A	

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SYSTem:VERSion?

Purpose	Queries the SCPI version number with which the VM1548 complies	
Type	Required SCPI command	
Command Syntax	N/A	
Command Parameters	N/A	
***RST Value**	N/A	
Query Syntax	SYSTem:VERSion?	
Query Parameters	N/A	
Query Response	Numeric ASCII value	
Description	The System Version query reports version of the SCPI standard with which the VM1548 complies.	
Examples	**Command / Query**	**Response *(Description)***
	`SYST:VERS?`	1994.0
Related Commands	N/A	

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SECTION 5

THEORY OF OPERATION

INTRODUCTION

The VM1548 TTL I/O module is a VXI message-based device consisting of six channels of bi-directional I/O. The six channels or ports are configured as inputs or outputs in groups of eight bits that can be clocked from internal or external sources. The six channels can be remotely configured from the front panel connector I/O signal or from the VMIP module through SCPI commands. The clocking can be from one of eight VXI TTL trigger lines, a word serial event, or an externally supplied clock. This clocking method allows for large parallel data words to be transmitted or received. The VM1548 contains the capability to generate a TTL trigger onto the VXI backplane using a word serial event, one of six front panel clock inputs or from a TTL Trigger input. By utilizing the D16 access the VM1548 can achieve data throughput rates of 4 MB/s.

The VM1548 contains 22 Ω series damping resistors on all data lines to reduce ringing during a data transition period and a RC network of a 120 Ω resistor in series with a 100 pF capacitor for termination of clock lines.

All channels (0 through 5) on the VM1548 perform identically, that is all buffers are loaded the same way, all channels are accessed the same, etc. Because of this similarity, for clarity, the theory of operation will describe channel 0 for byte wide and channels 0 and 1 for word wide operations.

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VXI INTERFACE

DEVICE TRANSFERS (WRITE MODE)

When write transfers to the UUT are selected the VM1548 will select the direction of the transfer, enable the clocks for the selected channel(s), latch the data into the I/O word buffer and clock the I/O data buffer using the appropriate triggering method.

DIRECTION

Direction of transfer is controlled either from the front panel connector or from U10 the direction control latch (see Figure 5-1). Upon receipt of the SCPI command for setting the direction, U8 decodes the VMIP address and issues the DOE* signal to the read/write data buffer U2. This allows the transceiver U2 to be configured to write data when both signals are low. U8 then generates the PORTENA* signal that provides a low signal to U5 enabling the 1 of 8 port decoder. Address bits A0, A1 and A2 are decoded causing U5 to provide a low going edge clocking the direction latch, U10. This octal D latch provides the direction signal OUTENA0 that is OR'd with the corresponding I/O signal from the front panel connector.

The front panel I/O signal is active low and is pulled to VCC through a 47 KΩ resistor. The signal is then inverted by U21 and routed to the OR gate at U20. The results of OR'ing these two signals together provide a high on I/O buffer U14 direction enable lines GBA* and GAB (see section 6, schematics for pin name designations). This signal is also routed to the I/O word buffer U11 output write enable line OEAB1. This is done to avoid READ/WRITE contentions between the two buffers. The I/O buffers are now configured to drive the data to the UUT or the write mode.

CLOCK ENABLE

Output clock enabling is accomplished when the VMIP module receives the SCPI command for output clock enable. U8 then decodes the address and control bits from the VMIP bus and generates the DOE* signal to the read/write data buffer. U8 generates PORTENA* enabling U5 as detailed previously. This time the address bits decode to PORT1* clocking the write clock enable latch U4. The output of this latch, CLKOUTENA0, is routed to the I/O data buffer clock enable line SAB.

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DATA LOAD

Loading of data into the I/O word buffer occurs when the VMIP receives the SCPI command for writing data. U8 decodes the address and control bits from the VMIP bus and generates the DOE* signal to the read/write data buffer. U8 then issues the WRITE0* signal to the selected I/O word buffer thus latching the data. The I/O buffers are enabled and configured to transmit data from channel 0 to the UUT upon receipt of the proper clock or trigger.

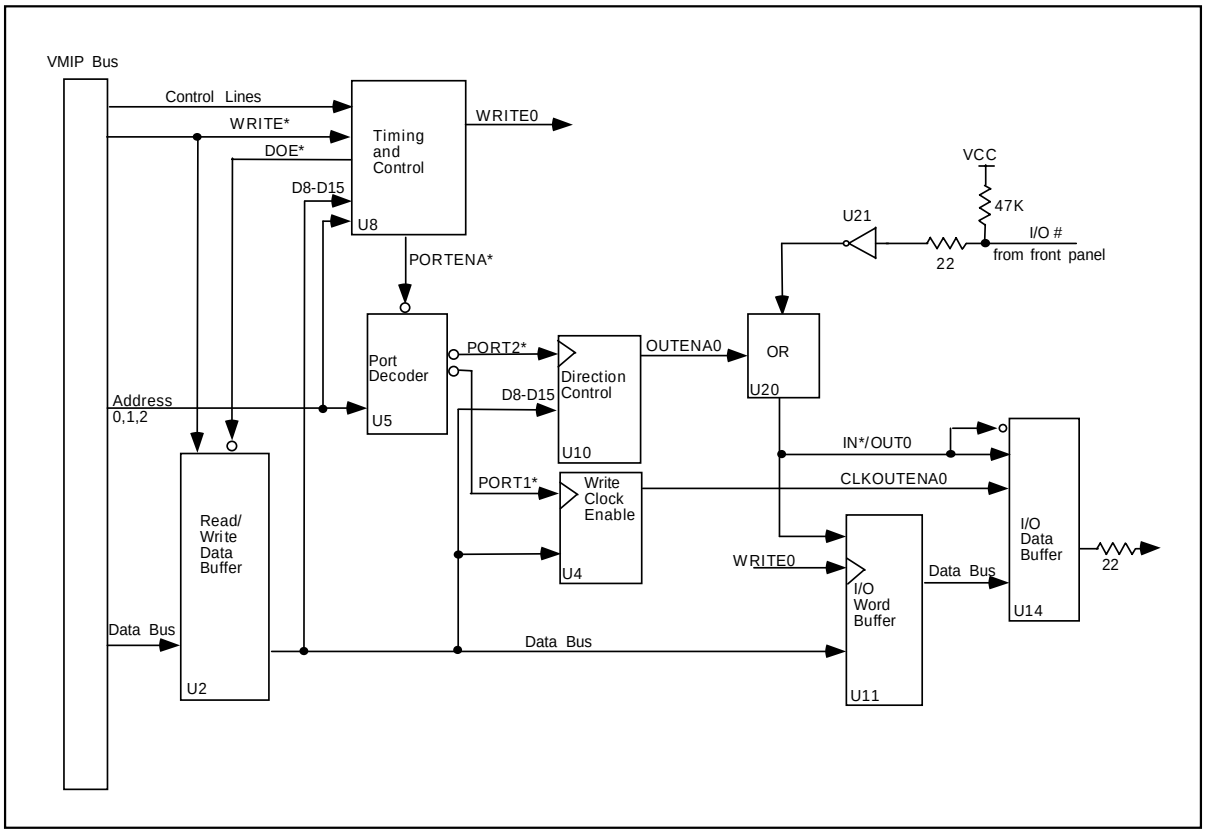


TABLE 5-1: WRITE MODE BUFFER CONFIGURATION

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DEVICE TRIGGERING (TTL INPUT TRIGGER)

The VM1548 is capable of both receiving and generating VXI TTL triggers. The generated TTL triggers may be used to signal another VXI instrument that a VM1548 event has occurred. The VM1548 can also receive any one of eight TTL triggers from the VXI backplane, TTL trigout, or a front panel connector clock line for use in triggering all six channels at once.

TRIGGER DECODE

Upon receipt of the command that informs the timing and control FPGA that the input trigger feature has been selected. U8 generates the PORTENA* signal that provides a low signal to U5 enabling the 1 of 8 port decoder (see Figure 5-2). Address bits A0, A1 and A2 are decoded causing U5 to provide a low going edge clocking the trigger select latch, U7. U7 then outputs the binary equivalent number that matches the desired trigger and the trigger input enable signal TINENA*.

TRIGGER SELECT

The select lines TINSEL0, TINSEL1, TINSEL2 and enable signal TINENA* are then routed to U1 the trigger input mux. This 8:1 mux will select the desired trigger. The output of U1 is the signal TRIGIN* and is routed to the timing and control FPGA. Once inside U8 the TRIGIN* signal may be inverted to produce a falling edge, if this feature has been selected, or remain in the normal default state of a rising edge. The signal is then muxed to the output clock circuitry in U8 and routed to the selected I/O data buffer (U14) as CLKOUT0. The rising edge of this signal then clocks the I/O data buffer to drive the I/O data outputs onto the UUT.

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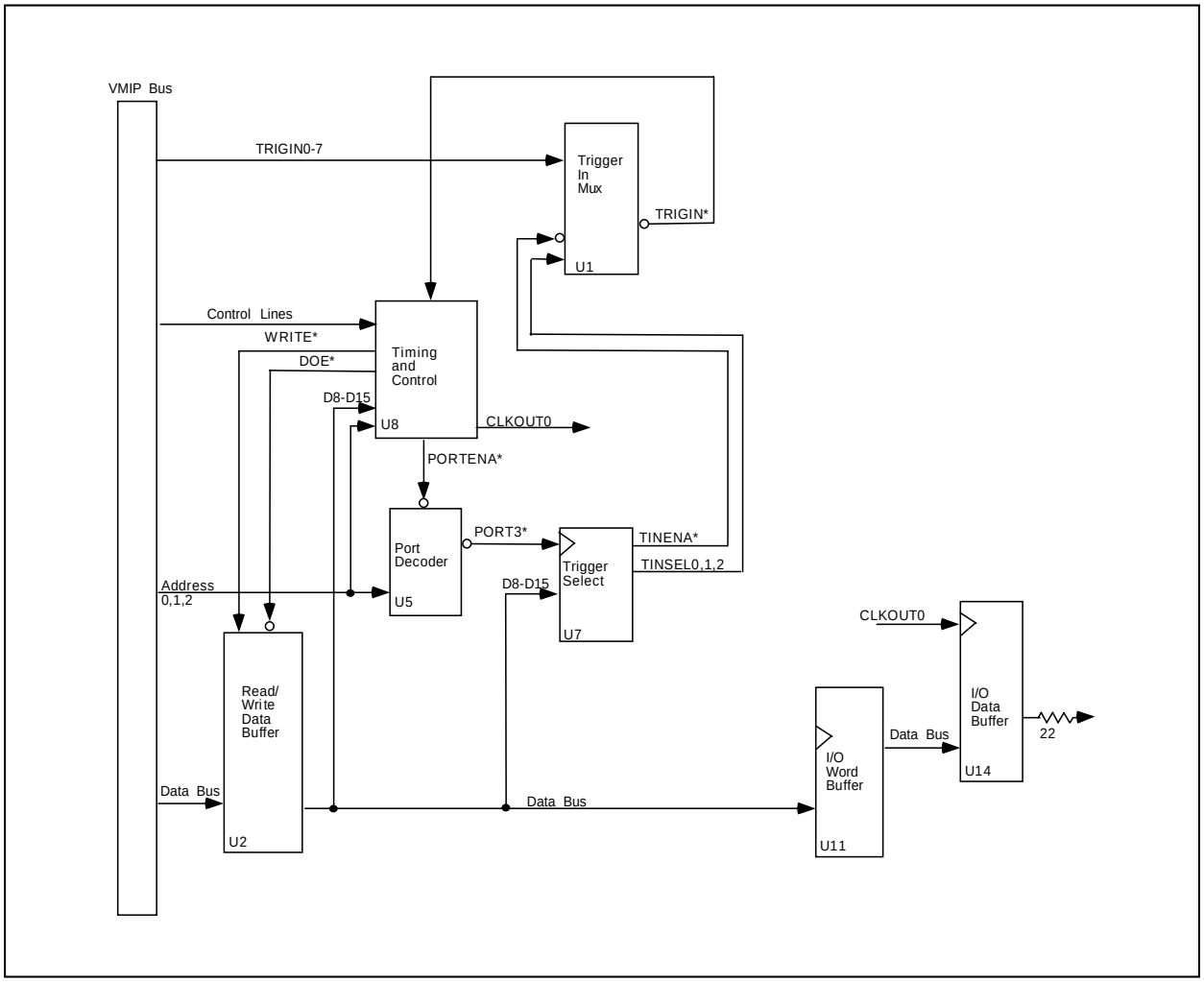


TABLE 5-2: TTL TRIGGER INPUT

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DEVICE TRANSFERS (READ MODE)

When read transfers from the UUT are selected the VM1548 will select the direction of the transfer, enable the clocks for the selected channel(s), latch the data into the I/O data buffer, if double buffering is selected, using the appropriate triggering method and clock the I/O word buffer.

This clock or trigger can be from either a TTL trigger input, the front panel connector CLK input, a word serial event or a TTL trigger out. The front panel connector CLK input will be used to trigger the latching of data into the I/O data buffer and then generate an Interrupt Request (IRQ) to the slot 0 controller.

DIRECTION

Direction of transfer is controlled either from the front panel connector or from U10 the direction control latch (see Figure 5-3). Upon receipt of the SCPI command, U8 decodes the VMIP address and issues the DOE* signal to the read/write data buffer U2 allowing the data on the inputs of U2 to be available on the outputs when both signals are low. U8 then generates the PORTENA* signal that provides a low signal to U5 enabling the 1 of 8 port decoder. Address bits A0, A1 and A2 are decoded causing U5 to provide a low going edge clocking the direction latch, U10. This octal D latch provides the direction signal OUTENA0, a low equates to read and a high equates to write, that is OR'd with the corresponding I/O signal from the front panel connector.

The front panel connector I/O signal is active low and is pulled to VCC through a 47 kΩ resistor. The signal is then inverted by U21 and routed to the OR gate at U20. The results of OR'ing these two signals together provide a low on I/O buffer U14 direction enable lines GBA* and GAB (see section 6, schematics for pin name designations). This signal is also routed to the I/O word buffer U11 output write enable line OEAB1. This is done to avoid READ/WRITE contentions between the two buffers. The I/O buffers are now configured to receive data from the UUT or the read mode.

CLOCK ENABLE

Input clock enabling is accomplished when the VMIP module receives the SCPI command for input clock enable. U8 then decodes the address and control bits from the VMIP bus and generates the DOE* signal to the read/write data buffer. U8 generates PORTENA* enabling U5 as detailed previously. This time the address bits decode to PORT0* clocking the read clock enable latch U9. The output of this latch CLKINENA0 is routed to the I/O data buffer clock enable line SBA. Loading of data into the I/O data buffer occurs when the VM1548 receives the appropriate input clock or trigger as specified by the SCPI command.

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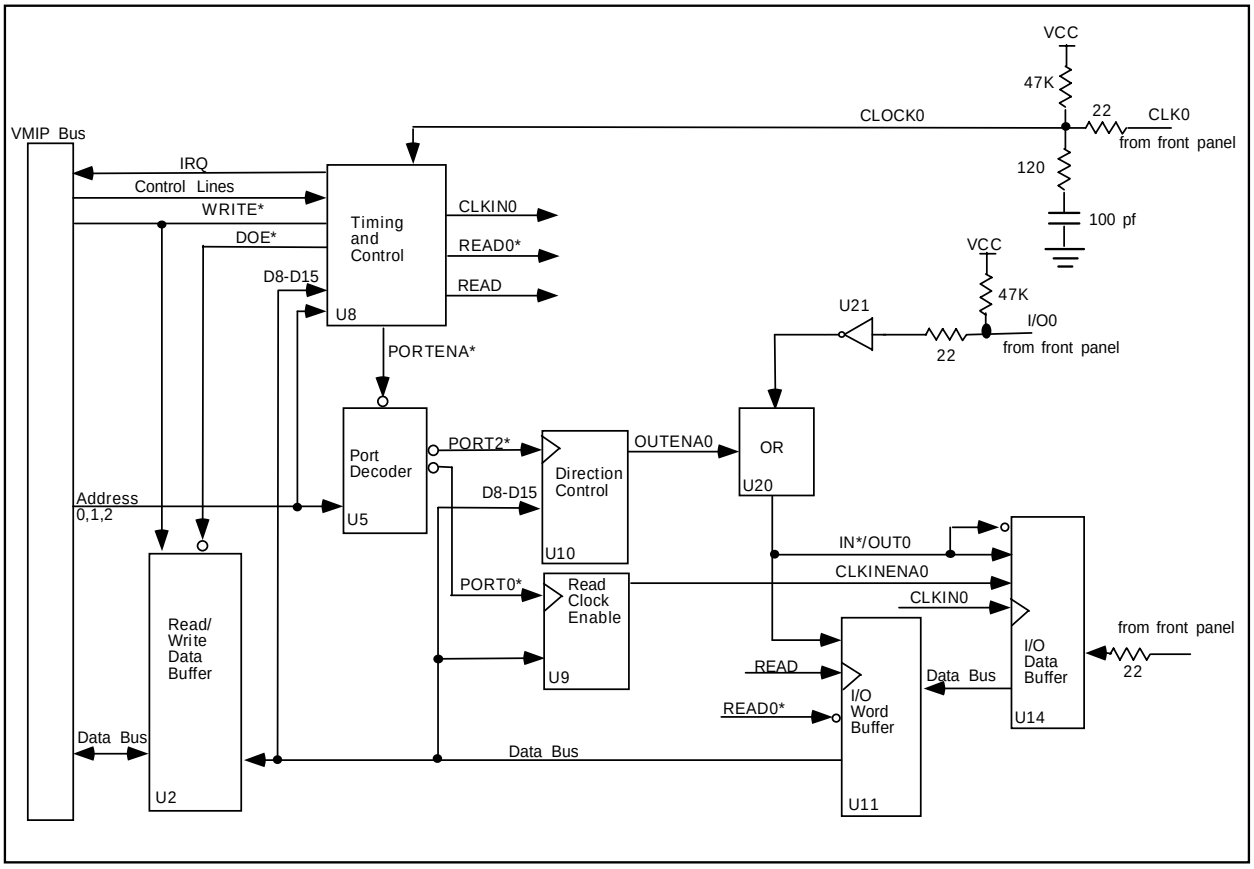


TABLE 5-3: READ MODE BUFFER CONFIGURATION

The CLK0 input from the UUT is terminated in the VM1548 by a RC network of 120 Ω to ground through a 100 pF capacitor and a 47 kΩ resistor to VCC. This termination value gives a time constant of 12 ns for fast rise times on input clocks and will not load the UUT driving source. The received clock now referred to as CLOCK0 is routed to timing and control FPGA U8. Once inside U8 the CLOCK0 signal may be inverted to produce a falling edge if this feature has been selected or remains in the normal default state of a rising edge. The signal is then muxed to the input clock circuitry in U8 and routed to the selected I/O data buffer (U14) as CLKIN0.

LATCH DATA

The rising edge of this signal then clocks the I/O data buffer to read data from the UUT. The CLOCK0 signal also causes the timing and control FPGA to generate an IRQ signal to the VXI backplane signaling incoming data from the UUT.

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READ DATA

Upon receipt of the SCPI command to read the data, the timing and control FPGA decodes the address and control bits from the VMIP bus and generates the READ0* signal to the OEBA1 input of U11. This enables the I/O word buffer to input data from the I/O data buffer.

U8 then issues the READ signal to the previously enabled I/O word buffer thus latching the data. U8 generates the DOE* signal to the read/write data buffer. This allows the input data from the UUT to be available on the VXI data bus.

Note that data inputs to the module do not contain pull-up or down-biasing resistors. If the user does not provide active or passive biasing of the data inputs, a read of the port may result in either a "1" or "0" being read from the data inputs.

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