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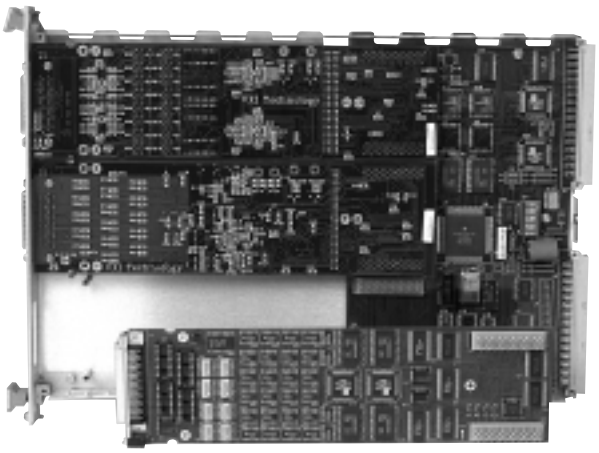
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Find the *Ametek / VTI Instruments / VXI Technology VM1602* at our website: *Click HERE*

VM1602

32-channel Time Stamp (VMIP™)

- 32-channel Event Monitor with Time Stamp Recording
- Up to 96 Channels per VXIbus C-size Slot
- Message-based Control with Pseudo-register Data Access
- 40-bit Counter for High Total Time Count
- 1µs Resolution for Precision Time Stamping
- SCPI Compatible
- VXI*plug&play* Drivers



Overview

The VM1602 is a high-performance event monitor with time stamp recording capability. The instrument monitors each of its 32 inputs for an event and records the time when the event occurred. The time is recorded by saving the value of a 40-bit time counter into memory, along with a 32-bit event source value corresponding to the channel or channels which caused the event to occur. An event occurs on a channel when the input has a rising or falling edge. Each channel is independently programmed for rising or falling edge detection. The instrument can collect a total of 128k events, or 512k events when the extended memory option is installed.

Each input can be configured for either differential or single-ended operation. In differential mode, a high input occurs when the positive input is at a higher potential than the negative input. In single-ended mode, a high input occurs when the positive input of a channel is at a higher potential than the programmed threshold voltage for the corresponding channel.

The time stamp which is recorded with each input event consists of a 40-bit time counter value. This counter increments at a rate of 1µs, 10µs, 100µs or 1ms. All time measurements are then made by finding the difference between time counter values multiplied by the increment rate of the counter.

Flexibility

In order to maximize flexibility, each pair of input channels can be connected to a common input. For example, channel 2 can be connected to channel 1's input, channel 4 can be connected to channel 3's input, etc. This allows the two channels to be combined to monitor and time stamp both the rising and falling edges of a given signal. In addition to the front panel inputs, the VM1602 can also monitor all of the VXIbus TTL trigger bus lines. Monitoring the VXIbus TTL trigger lines allows the VM1602 to add time stamp capability to any instrument which can drive the trigger lines.

The VM1602 allows each channel to be enabled or disabled. This prevents unused channels from detecting events and using the time stamp memory. If a channel is enabled and an event occurs, a bit corresponding to the channel is set in the event source memory along with the time stamp counter value. This bit is set high only when events occur, and more than one channel can have an event within the sample window.

When a channel is disabled, the logic level on that input is recorded every time an event occurs on an enabled channel. This allows the VM1602 to operate as a rudimentary logic analyzer.

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VM1602

32-channel Time Stamp (VMIP™)

Specifications

Input

Channels: 32. A single C-size module may be configured for 32, 64 or 96 channels

Type: Differential or single ended. Programmable internal threshold in single-ended mode

Impedance: 20k Ω single-ended, 40k Ω differential

Termination: User installed, 8-resistor, 16-pin DIP network

Voltage Range: -5 volts to +5 volts

Threshold Range: -5 volts to +5 volts, 39 mV resolution (8 bits)

Hysteresis: 100 mV nominal

Threshold Accuracy: ±2% of range

Threshold Source: Internally generated level, 8 DACs, one per four adjacent channels. (Channel 1 through 4 share a single threshold DAC.)

Sense: Rising or falling edge, programmed on a per-channel basis

Source: Odd-numbered channels may be routed to either the front panel or the TTL trigger bus. Even-numbered channels may be routed to either the front panel or to the same source as the adjacent channel. (Channel 2 connects to channel 1's input source.)

Time Stamp

Counter: 40 bits; 32-bit hardware counter feeding an 8-bit software counter

Resolution: Programmable to 1µS, 10µs, 100µs or 1ms

Accuracy: ± 0.01% derived from the VXIbus CLK10 signals. May be improved by supplying a superior source to the slot zero controller.

Event Recording Depth: 128k samples deep, 512k samples optional

User Connector: The user connector is a standard 68-pin SCSI-2 compatible IDC. A mating connector is provided with each unit.

Ordering Information

VM1602 32-channel Time Stamp
(must be configured with a VM9000 host module)

Option 3: 512k Word Upgrade

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