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WAVETEK

OPERATION AND
MAINTENANCE MANUAL

Model 1391

INCLUDING SCPI AND MATE/CIIL
LANGUAGE DESCRIPTIONS

50 MHz VXI Pulse Generator

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Manual Revision B, 4/93
Manual Part Number 1006-00-0694

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ERRATA
FOR
INSTRUCTION MANUAL
MODEL 1391
50MHz VXI PULSE GENERATOR

NOTE

This errata is only for the Model 1391 manual ***dated 4/93***

Make the following changes to the manual:

Page 1-4, Paragraph 1.3.7, Cooling Requirement:

Replace

"Minimum airflow requirement for 10°C rise is 0.381mm (.015 in) H_2O at 11.34 1/sec (24 CFM)."

with

"Minimum airflow requirement for 10°C rise is 0.381mm (.015 in) H_2O at 3.9 1/sec (24 CFM)."

Page 3-20, Paragraph 1.3.7, SUMBUS Operation

At the bottom of the second column, change from

```
Receiver:  INIT:CONT OFF
           TRIG:SOUR:ECLTO
```

to

```
Receiver:  INIT:CONT OFF
           TRIG:SOUR ECLTO
```

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SAFETY FIRST



PROTECT YOURSELF. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the VXI chassis' power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the VXI chassis power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't energize the VXI chassis until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

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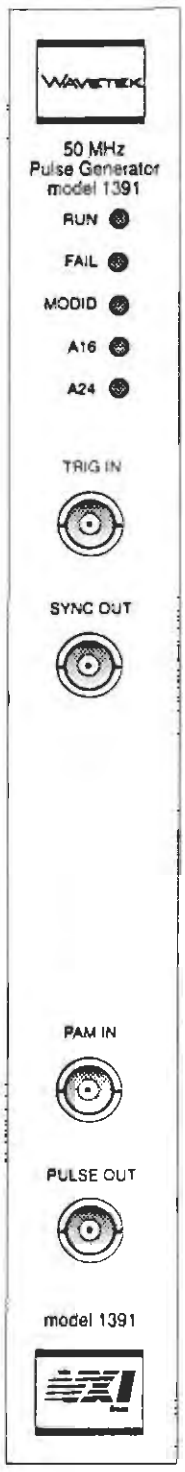


Figure 1-1. Model 1391 50 MHz VXI Pulse Generator

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1.1 The Model 1391

The Model 1391 is a 1 mHz to 50 MHz "C" size VXI Programmable Pulse Generator. It can generate single, double, and delayed pulses with programmable period, width, delay, rise/fall transitions, and output levels. The generator operates as a continuous, triggered, gated or burst pulse source up to 50 MHz. Additionally, the Model 1391 can be programmed for a square wave function (~50% time symmetry) up to 100 MHz. Pulse characteristics are programmable with 4 digit resolution, with width and delay up to 2000 seconds, and rise/fall transition times settable from 5 ns to 50 µs.

The pulse ouput amplitude may be specified as upper and lower levels, which can be programmed in a ±16 V window (±8V into 50Ω termination). Peak to peak amplitude, upper level value minus lower level value, is continuously variable in 10 mV steps from 150 mVp-p to 16 Vp-p (50Ω). The pulse amplitude (upper, lower, or both) may be modulated (PAM) with an external signal.

Control of the pulse generator adheres to the SCPI (Standard Commands for Programmable Instruments) format Version 1992.0, February 1992 (refer to the SCPI manual for further information). SCPI is an industry standard language for remote instrument programming. Using any manufacturer's VXI chassis, the Model 1391 can be controlled using the SCPI language and the appropriate controller.

Multiple pulse generators may be linked and operated together inside one VXIbus chassis. Series operation is provided by full support of the VXIbus SUMBUS. A signal programmed at the output may be sent to the SUMBUS, or signal present at the SUMBUS may be summed into the model 1391 output. In parallel operation, model 1391's may be slaved to a master clock/trigger bus on the VXIbus backplane to create a multichannel pulse generator.

The model 1391 has extensive self-adjustment utilities built in. Calibration constants are maintained in non-volatile memory.

1.2 Specifications

1.2.1 Functions

Programmable single, double or delayed pulse and fixed (~50%) duty cycle square wave.

1.2.2 Operating Modes

Continuous:
Pulse period generated continuously internal to the model 1391 at programmed frequency/period. Selected pulse waveform is continuously output at PULSE OUT with programmed pulse characteristics. Period timing signal appears at SYNC OUT (if enabled) and may be selected for output to the backplane. Pulse periods programmable up to 25 MHz in double pulse, 50 MHz in single or delayed pulse, and 100 MHz in square wave. Pulse Amplitude Modulation may be enabled for external signal at PAM IN.

Triggered:
As above for Continuous mode, except that pulse period generation is disabled. Output quiescent until triggered by an external signal at TRIG IN, a TTLTRG or ECLTRG signal, internal trigger frequency, or a VXIbus command, then generates one pulse period with the programmed pulse waveform and pulse characteristics. Triggered pulse periods operate to 25 MHz in double pulse, 50 MHz in single or delayed pulse and square wave.

Gated:
Similar to triggered mode except output continues for the duration of gate signal. The last pulse period started is completed.

Burst:
Similar to triggered mode except programmable number of pulse periods in a burst. Burst length, initiated by the trigger signal, is programmable between 2 and 10,000,000 cycles.

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1.2.3 Inputs

Trig In:
Front panel BNC input for external triggering signal. Variable trigger level control accepts TTL or variable amplitude bipolar signals. In addition, any of the trigger lines on the VXIbus backplane can be selected as the trigger input, see Trigger Input (from VXI Backplane). TRIG IN is protected over a ±20 V input range.

Variable Trigger Level:	
Range:	± 10 V
Resolution:	50 mV
Accuracy:	± 500 mV
Minimum input level:	750 mVpp
Maximum input level:	± 20 V
Minimum pulse width:	10 ns
Input impedance:	≥1kΩ shunted by ≤10 pF
Jitter:	±500 ps: for ≥750 mVpp square wave input with ≤50 ns transitions.

PAM In:
Front panel BNC connector, used to externally Pulse Amplitude Modulate the model 1391. PAM modulation scale factor is set so that a 1 volt input at this connector will result in a 2 volt change in upper/lower level amplitude at the PULSE OUT connector. Input is protected to ±50 V inputs.

Input impedance:	≥1 kΩ
Bandwidth:	dc to >20 kHz
Accuracy:	± 5%

SUMBUS Input (from VXI Backplane):
Analog signals on the VXIbus SUMBUS line may be summed into a model 1391 PULSE OUT with a fixed scale factor. A full-scale PULSE OUT signal of 16 Vpp requires a 2Vpp (80 mApp driving 25Ω) input signal at the SUMBUS line. SUMBUS receiver specifications are:

Scale factor:	8 V/V
Accuracy:	± (6% + 200 mV + 2.5 mA)
Input impedance:	>10 kΩ in parallel with <20 pF
Bandwidth:	> 50 MHz

Trigger Input (from VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected as the trigger input for the model 1391. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.4 Outputs

Pulse Output:
Front panel BNC output, supplies the 150 mVpp to 16 Vpp pulse waveform into a 50Ω termination, up to 50 MHz. Programmable on or off (Zoff > 500 kΩ). Output is protected against short circuits.

Source Impedance: 50Ω.

NOTE: When overload current is detected, the protection circuitry disables the Pulse Output. To recover from an overload, turn the power off, wait two minutes, and turn the power back on.

Sync Output:
TTL level pulse (active high) into 50Ω. Programmable as either the pulse period (MARKer:TYPE CLOCk) or as a copy of the external gating signal (MARKer:TYPE GATE). When in continuous mode, the Sync Output is an approximate 50% duty cycle square wave defining the timing of a pulse period up to 50 MHz. For frequencies >50 MHz and up to 100 MHz, the Sync Output operates as a clock source.

In triggered mode (INITiate:CONTinuous OFF), the Sync Output (MARKer:TYPE CLOCk) is a copy of the triggering signal. The Sync Output (MARKer:TYPE GATE) is valid only in burst mode (TRIGger:COUNt <value>, where "value" is greater than 1) or in gated mode (TRIGger:GATE ON). The SYNC OUT BNC is short circuit protected.

TTL Compatible:	<0.4 to >2.0 V into 50Ω
Timing:	50% point of rising edge defines the start of a pulse period. Configuration dependent delay (see Trigger Latency, Figure 1-2 and the table below) following trigger event.
Transition time:	<5ns with 3 feet RG-58 50Ω coax cable terminated into 50Ω.

Trigger Delays ($t_1 - t_0$, see Figure 1-2)

Configuration*	Trigger Latency
External Trigger Input**	
Trigger Mode	typically 58 ns
Burst Mode, Pulse	typically 83 ns
Burst Mode, Square	typically 63 ns
ECL Trigger**	typically 52 ns
TTL Trigger	typically 52 ns

* Trigger delays measured for a single pulse, 0 ns delay.

** Add 22 ns when unit is configured as the Master.

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SUMBUS Output (to VXI Backplane):
Pulse output signals from the model 1391 may be summed onto the VXIbus SUMBUS line with levels proportional to the pulse output. A full-scale PULSE OUT signal of 16 Vpp results in an 80 mApp signal driving the SUMBUS line. SUMBUS driver specifications are:

Scale factor:	5 mA/V
Accuracy:	± (6% + 2.5 mA)
Load Impedance:	25Ω ± 2% (VXI Specification)
Output impedance:	>10 kΩ in parallel with <20 pF
Compliance:	± 1.2 V minimum
Bandwidth:	> 50 MHz (limited by the backplane).

Trigger Output (to VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected to be driven by a signal from the model 1391. The internal trigger, the external trigger input, or the pulse waveform may be selected to be output. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.5 Pulse Characteristics

See Figure 1-2 for an illustration defining the various pulse characteristics. Pulse functions are programmable using operating mode, pulse period (frequency), width, delay, transition times, and amplitude levels.

NOTE: All pulse characteristics specifications require high-quality 50Ω cable (≤3 feet RG-59 or equivalent) and a high-frequency 50Ω (≥ 1W) termination at the far end of the cable from the PULSE OUT BNC.

Pulse Period:

Range:	
Pulse Out:	20 ns to 1000 s (1 mHz to 50 MHz)
Sync Out:	10 ns to 1000 s (1 mHz to 100 MHz)
Resolution:	4 digits, limited by 1 mHz
Accuracy:	Same as the VXIbus CLK10 reference in continuous mode (± 0.01% typical), ± 2% of setting in non-continuous modes.

Pulse Width:

Range:	10 ns to 1000 s (up to 2000 s with external trigger).
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 2 ns)
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by min. off-time of 10 ns.

Pulse Delay:

Range:	0 ns to 2000 s
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 5 ns); transition times set to minimum.
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by minimum off-time of 12 ns.

Rise and Fall Transitions:

Range:	5 ns to 50 µs
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (5% + 2 ns)
Aberrations (Vpp):	< (5% of Vpp + 20 mV)

NOTE: The ratio of rise time to fall time may not exceed 10:1. For Amplitudes > 12 Vpp the Aberrations specification applies for transitions ≥ 7 ns.

Upper and Lower Levels:

Range:	± 8 V
Resolution:	10 mV

Vpp Amplitude (Upper Level – Lower Level)

Accuracy:	
Vpp ≥ 0.5	± (2% of setting + 50 mV)
Vpp < 0.5	± (2% of setting + 25 mV)

Offset ((Upper Level + Lower Level)/2)

Accuracy:	± (2% of setting + 50 mV)

NOTE: The minimum amplitude (upper – lower) may not be less than 150 mVpp. Pulses less than 500 mVpp are restricted to a ± 2V window.

1.2.6 Multichannel Operation

Multiple 1391 modules may be operated together in series or in parallel to create a multichannel pulse generator.

Series (SUMBUS) Operation
A module may be selected to drive the SUMBUS, receive from the SUMBUS, or disconnect from the SUMBUS. Allows the signal from one module to be summed with the signal at the output of another. Allows for more complex waveform generation than provided with simple pulse generator features, such as multi-level pulses.

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Parallel (Master/Slave) Operation
Up to 10 model 1391 modules may be operated in Master/Slave configuration within a VXIbus chassis. This mode of operation uses the high bandwidth and tight timing of the ECL trigger lines to couple the start of triggered pulse periods of Slave modules to the trigger output of the Master module. Sets the "start of pulse period" (t_1) timing points of adjacent modules into close agreement. Modules further away will have a timing delay of approximately 0.5 ns per slot, dependent upon the VXIbus chassis backplane.

1.8 GENERAL

1.8.1 SCPI Programming
Conforms to SCPI Version 1992.0 (see Appendix E) and IEEE-488.2 standard mandated commands. Root level commands include:

DIAGnostic	**OUTP**ut	**SOUR**ce
STATus	**SYST**em	**TRIG**ger
INITiate	**CAL**ibrate	**RES**et
TEST		

1.8.2 VXIbus Interface
Message Based Device (MBD), 256 byte input buffer. Supports the following subsets/protocols:

A16/A24 D16/D24 Master, A16/A24 D16/D24 Slave;
VXIbus Instrument Protocol (I);
VXIbus IEEE-488.2 Instrument Protocol (I4);
Event Generator, Response Generator;
DC (Dynamically Configurable) Device.

The model 1391 supports all Word Serial Commands specified in the VXIbus System Specification (Rev. 1.4), Tables E.1 and E.2 for the above subset/protocol classification.

1.8.3 Environmental

Temperature Range:

Operating:	Specifications apply 0°C to 50°C, when calibrated at 23°C ± 3°C.
Storage:	-40°C to +71°C (RH not controlled).
Warm-up Time:	30 minutes for specified operation, except stability specifications require 60 minutes.
Altitude:	
Operating:	Sea level to 10,000 ft.
Storage:	Sea level to 15,000 ft.
Relative Humidity (non-condensing):	
0°C to +10°C:	not controlled.
+11°C to +30°C:	95 ± 5% RH max.
+31°C to +40°C:	75 ± 5% RH max.
+41°C to +50°C:	45 ± 5% RH max.
Vibration:	0.013 in., 5 to 55 Hz, 2g max.
Shock:	Non-operating, 40 g, 9 ms half-sine.
Bench Handling:	Non-operating, 4 inch or point of balance drop, any face, solid wooden surface.

1.8.4 Size

Dimensions:	Single slot, "C" size VXI module.
Weight:	1.65 kg (3.63 lb) net; 3.64 kg (8.00 lb) shipping.

1.8.5 Power

Total: < 47 Watts

Voltage	Peak Current	Dynamic Current
+24 Vdc	0.4 A	0.3 A
+12 Vdc	1.0 A	0.1 A
+5 Vdc	1.0 A	0.2 A
–2 Vdc	1.1 A	0.1 A
–5.2 Vdc	1.8 A	0.1 A
–12 Vdc	0.8 A	0.1 A
–24 Vdc	0.4 A	0.3 A

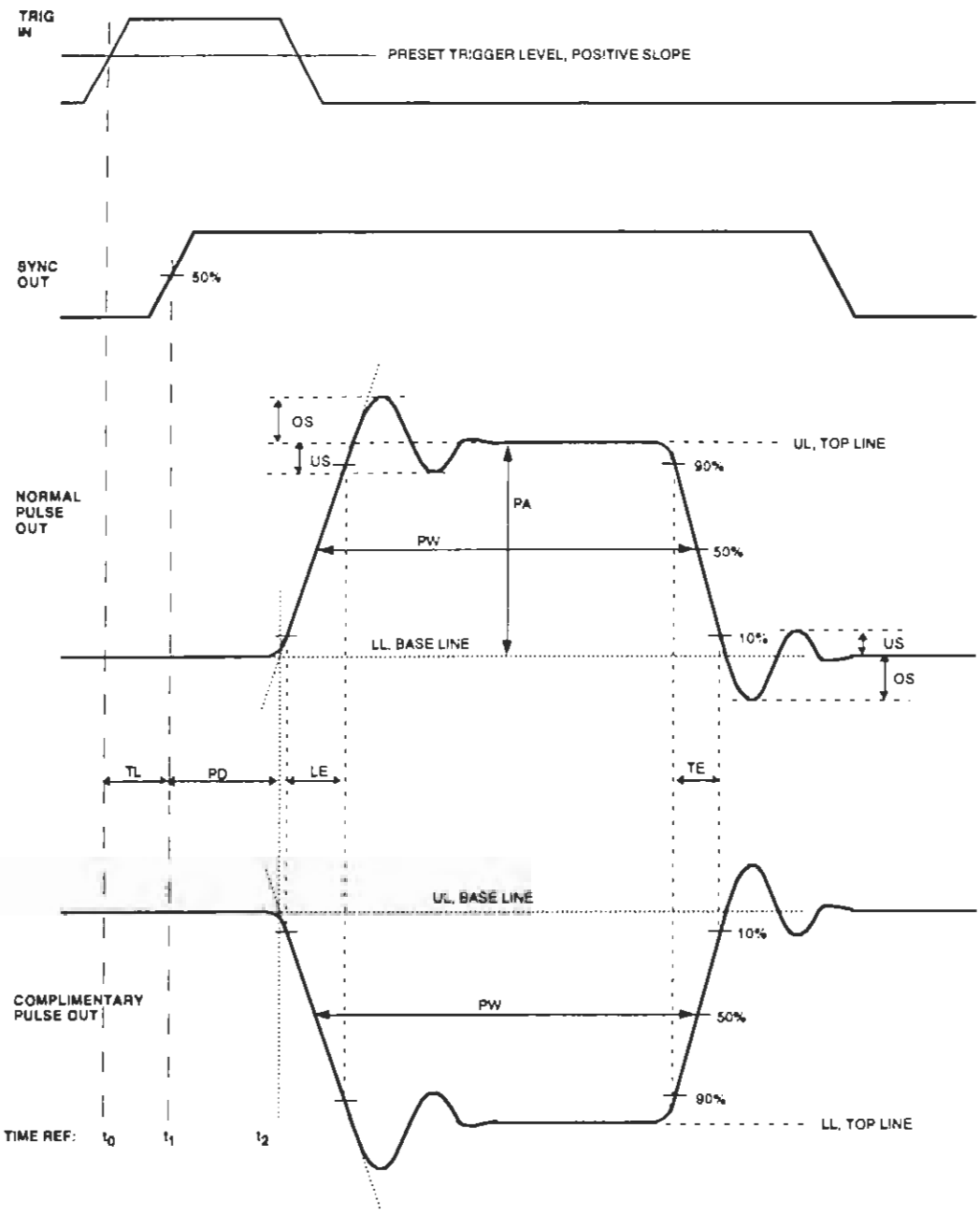
1.8.6 Reliability
>22,000 hours MTBF at 25°C, ground benign. MIL-HDBK-217 calculation at 50% component stress.

1.8.7 Cooling Requirement
Within a VXI mainframe with cooling air. Minimum airflow requirement for 10°C rise is 0.381mm (.015 in) H_2O at 11.34 l/sec (24 CFM).

1.8.8 Safety
Designed and tested to MIL-T-28800D, UL-1244, and the VXI System Specification, Revision 1.4.

1.8.9 EMC
Designed and tested to MIL-STD-461C, Part 7, RE-02, and VXI System Specification, Revision 1.4; RE, RS, CE, CS.

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t_0 — TIME AT TRIGGER EVENT
t_1 — START OF PULSE PERIOD
t_2 — START OF DELAYED PULSE
UL — UPPER LEVEL VOLTAGE
LL — LOWER LEVEL VOLTAGE
PA — PULSE AMPLITUDE = (UL - LL)
TL — TRIGGER LATENCY = $t_1 - t_0$
PD — PULSE DELAY = $t_2 - t_1$
PW — PULSE WIDTH
LE — LEADING EDGE TRANSITION TIME
TE — TRAILING EDGE TRANSITION TIME
OS — OVERSHOOT
US — UNDERSHOOT
ABS — ABERRATIONS (pk-pk) = (OS + US)/PA * 100%

Figure 1.2 Definitions of Pulse Characteristics

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1-6 SPECIFICATIONS

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2.1 RECEIVING INSPECTION

Check the shipment at the time of delivery and inspect each box for damage. Describe any box damage and list any shortages on the delivery invoice.

2.1.1 Unpacking Instructions

1. **Unpack the boxes.** Unpack the boxes in a clean and dry environment. Save all the packing material in case the instrument must be returned for repair.
2. **Inspect the shipment for damage.** Inspect the equipment carefully for any signs of mechanical damage regardless of the condition of the shipping boxes.
3. **If necessary, file a claim.** In the case of mechanical damage, call the shipper immediately and start the claim process.
4. **Call Wavetek.** Call Wavetek's Customer Service representative (619 279-2200) to inform them that the shipment arrived damaged. Please be prepared to provide a detailed damage report.

2.1.2 Returning Equipment

Follow these steps when you return equipment to Wavetek:

1. **Save the packing material.** Always return equipment in its original packing material and boxes. If you use inadequate material, you'll have to pay to repair any shipping damage as carriers won't pay claims on incorrectly packed equipment.
2. **Call Wavetek Customer Service and ask for a return authorization.** The Wavetek Customer Service representative (619 279-2200) will ask for your name, telephone number, company name, equipment type, model number, serial number, and a description of the problem.
3. **Pack and ship the equipment.**

2.2 PREPARATION FOR STORAGE OR SHIPMENT

2.2.1 Packaging

If at all possible, always use the original shipping container. However, when using packing materials other than the original, use the following guidelines:

1. Wrap the Model 1391 in ESD sensitive packing material.
2. Use a double-walled cardboard shipping container.

Protect all sides, including the top and bottom, with shock absorbing material (minimum of 2 inch thick material) to prevent movement of the Model 1391 within the container. Seal the shipping container with approved sealing tape. Mark "FRAGILE" on all sides, top, and bottom of the shipping container.

2.2.2 Storage

The Model 1391 should be stored in a clean, dry environment. In high humidity environments, protect the Model 1391 from temperature variations that could cause internal condensation. The following environmental conditions apply to both shipping and storage;

Temperature	–40°C to +71°C
Relative Humidity	not controlled, non-condensing.
Altitude	<15000 ft
Vibration	< 2g
Shock	< 40g

2.3 PREPARATION FOR USE

Paragraph 2.3 covers the following topics:

Logical Address Selection
Data Transfer Bus Arbitration
Installation

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2.3.1 Logical Address Selection

The VXI chassis Resource Manager identifies units in the system by the unit's logical address. The VXI logical address can range from 0 to 255. However, addresses 0 and 255 are reserved for special functions. Address 0 identifies the Resource Manager. Address 255 permits the Resource Manager to dynamically address the unit based on the unit's VXI chassis slot.

To change the Model 1391's logical address, use the eight position DIP switch (figure 2-1) accessible from the side panel. The Model 1391 uses binary values (2^0 to 2^7) to set the address using the active low address switch. This means the OFF position represents a logical 1. Conversely, an ON position represents a logical 0. Switch position number one is the least significant bit of the address. Insert A in figure 2-1 illustrates a switch set to a logical address of 3.

Wavetek ships the Model 1391 with a logical address of 255 for Dynamic Configuration. Refer to insert B in figure 2-1.

2.3.2 Data Transfer Bus Arbitration

The Model 1391 has VMEbus Mastership capability. This means the Pulse Generator, when enabled, sends Responses and Events as signals to its Commander. The Model 1391 cannot drive the interrupt lines.

The Model 1391 is configured as a level 3 requestor by the factory. The level 3 Bus Request and Bus Grant lines are used (BR3*, BG3IN*, and BG3OUT*). The other Bus Grant lines are daisy-chained by jumpers. The VMEbus specifications describe three priority schemes: Prioritized, Round-robin, and Single level. The Prioritized arbitration assigns the bus according to a fixed priority scheme where each of four bus lines has a priority from highest (BR3*) to lowest (BR0*). Round-robin arbitration assigns the bus on a rotating basis. Single level arbitration only accepts requests on BR3*.

If a different requestor level is required, the jumpers must be changed. The following instructions and figure 2-2 will aid in reconfiguring the Model 1391 to

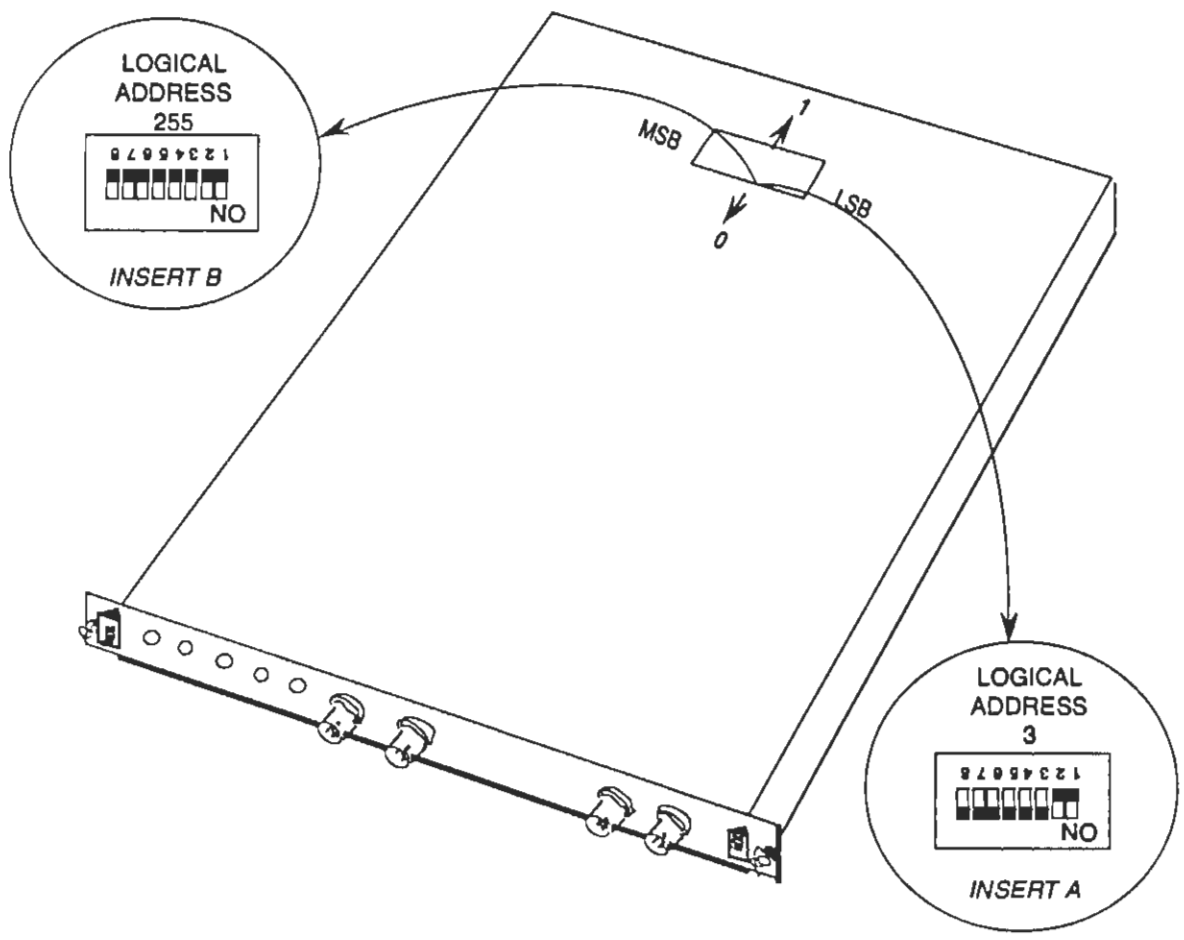


Figure 2-1. Set the Logical Address

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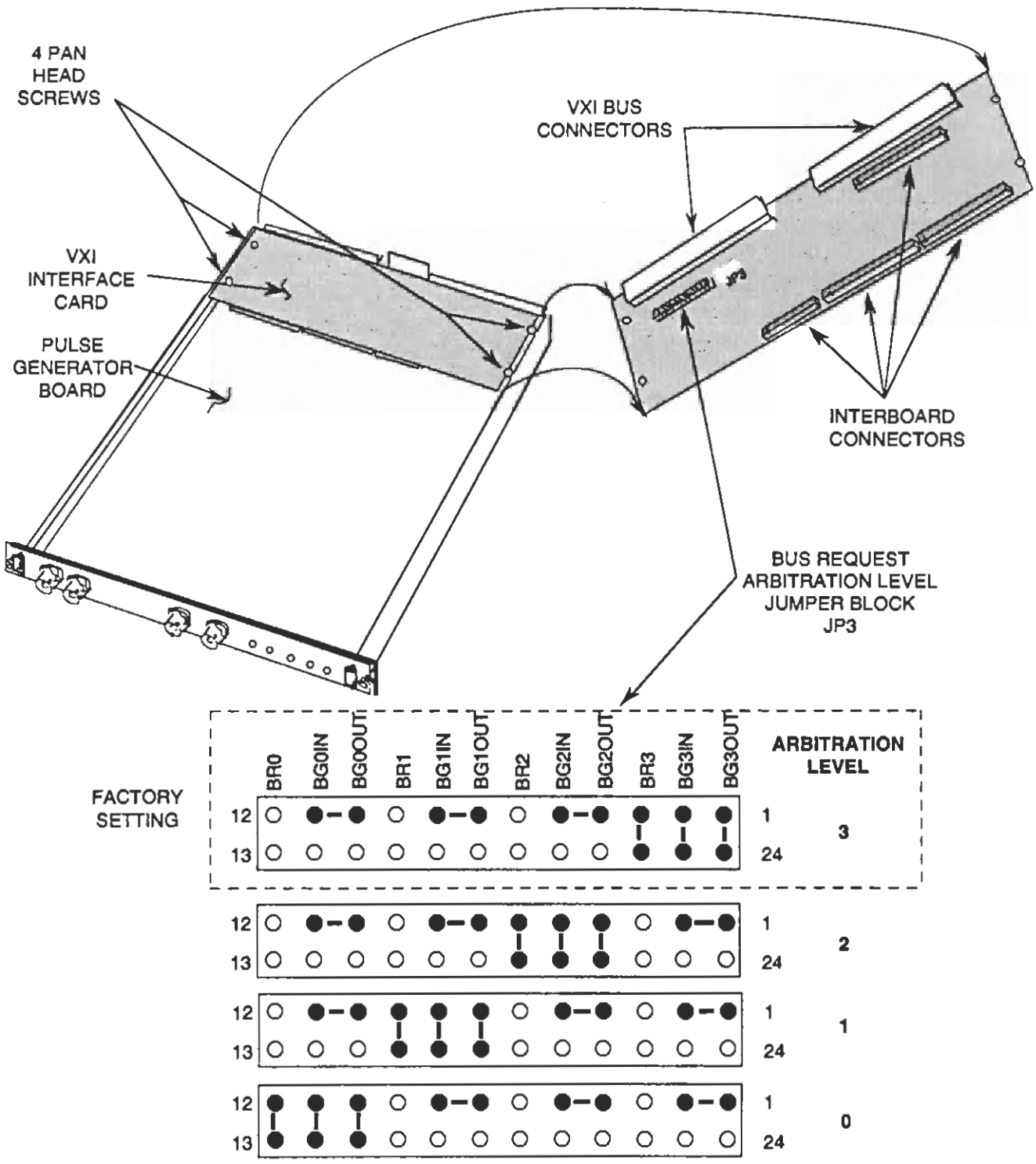


Figure 2-2. Bus Arbitration Level Jumpers

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a new level. Refer to the VMEbus specification for more information on '*data transfer bus arbitration*'.

CAUTION

The Pulse Generator contains CMOS devices which are sensitive to static electricity. When performing the bus arbitration level change, static electricity discharge straps should be worn.

1. Remove the four flat head screws on the Model 1391 left side panel, remove the panel.
2. Remove the four pan head screws holding the VXI Interface card to the main Pulse Generator board.
3. Slowly and gently lift the VXI Interface card up from the Pulse Generator board. Considerable force may be required as there are four connectors between the two boards with a total of 136 pins. Do not use a metallic prying tool.
4. Change the data transfer bus arbitration jumpers to the desired level. Refer to figure 2-2.
5. Carefully install the VXI Interface card onto the Pulse Generator board. Install the four pan head screws, the side panel and the four flat head screws.

2.4 INSTALLATION

The instrument will be installed in a VXI mainframe in any slot except slot 0 (zero). When inserting the instrument into the mainframe, it should be gently rocked back and forth to seat the connectors into the backplane receptacles. The ejectors will be at right angles to the front panel when the instrument is properly seated into the backplane. The two captive screws above and below the ejectors are used to secure the instrument into the chassis.

2.5 INITIAL CHECKOUT AND OPERATION VERIFICATION

This procedure provides the operator, service technician, receiving inspector, etc. with a quick method of verifying the functional operation of the Model 1391. This procedure does not test the unit's specifications. This procedure assumes the Model 1391 is properly installed in a "C" size VXI chassis with a VXI controller in slot 0. Required tools and test equipment are given in table 2-1.

Table 2-1. Test Equipment and Tools

Equipment	Comments
Oscilloscope	Bandwidth: ≥100 MHz
Signal Source	Frequency: 10 kHz
	Output: ±1V sine wave
BNC 50Ω Feed-through (2ea)	Accuracy: 0.5% Power: 2W
BNC Coax Cable (3ea)	RG58U, 3 ft. length

Because each step in the procedure is dependent on the preceding step, start with step 1 and continue through to the end. Do not send any command unless specifically instructed to do so within the procedure.

1) Verify proper LED operation during instrument power-up

LED	Normal Result
Run	On
Fail	Off
MODID	Flashes
A16	Flashes
A24	Off

2) Send: `*tst?`

   If response = 0, continue

   If response ≠ 0, decode error value (see Appendix D).

NOTE

If the test fails on a new or newly factory repaired unit, call Wavetek Customer Service at 619/279-2200 or FAX 619/565-9558.

3) Connect two coax cables between the Model 1391 PULSE OUT and SYNC OUT connectors and the

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oscilloscope. Use a 50Ω terminator on each cable. Connect the SYNC OUT to CH1 and the PULSE OUT to CH2, and synchronize the oscilloscope internally from CH1.

Send: `outp on;:mark on`

Verify the SYNC waveform on CH1 is a 1 MHz, TTL level square. Verify the pulse waveform on CH2 as follows:

NOTE

Numeric values should not be verified for accuracy in this operational check-out, but should be checked visually on the oscilloscope trace for approximate accuracy. Use the Performance Verification Procedure in Section 5 of this manual, if required, to test the unit to specification.

- single pulse; 1 µs period
- ±2.5 V upper and lower levels
- 250 ns pulse width
- ≤5 ns leading and trailing transition times

4) Verify the various pulse functions (waveforms) and pulse characteristics:

Send: `puls:del 600e-9`

Verify the single pulse is now delayed 600 ns relative to the rising edge of the SYNC.

Send: `puls:doub on`

Verify double pulses with the second pulse delayed 400 ns relative to the rising edge of the SYNC.

Send: `func squ`

Verify a 50% square wave output coincident with the SYNC.

Send: `func puls;freq 200e3`

Verify the waveform returns to double pulse, and that the waveform period (determined by the sync) has increased to 5 µs.

Send:
```
puls:doub:del 2e-6
puls:widt 8e-7
puls:tran:stat on;lead
              1e-7;tra 3e-7
```

Verify the double pulses now have a leading transition time of 100 ns, a pulse width (between the 50% points) of 800 ns, a trailing transition time of 300 ns, and that the second is delayed from the first by 2 µs.

5) Verify the output levels as follows:

Send: `volt:high 4;low -2`

Verify the output levels change from ±2.5 V to a low level of –2V and a high level of +4V.

6) Set the external generator up for a ±1V, 10 kHz sine wave. Connect the external signal to the Model 1391 TRIG IN connector.

Send:
```
init:cont off
trig:lev 0;sour ext
```

Verify a double pulse with all of the characteristics set up in steps 3 and 4, except that the pulse period is now triggered by the 10 kHz rate set by the external signal.

Send: `trig:coun 3`

Verify the double pulses are now triggered for 3 periods (six pulses in all) at the 10 kHz rate.

Send: `trig:gate on`

Verify the double pulse periods are gated on for approximately half the time by the 10 kHz external signal.

Send: `init:cont on`

Verify continuous operation.

7) Move the cable from the the TRIG IN connector to the the PAM IN connector.

Send: `pulm:stat on;ampl pos`

Verify the lower level is at zero volts and that the upper level is being amplitude modulated around its 4V median level with a ±2V sinusoidal envelope.

8) This completes the operational verification. Disconnect the test equipment.

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3.1 Introduction

This section provides the Operator/Programmer with the information needed to operate the Model 1391 Pulse Generator in a VXI system. The unit resides in a VXI chassis and is subject to all of the restrictions and benefits of that environment.

Paragraph 3.2 describes the Model 1391 connectors and LED indicators. Paragraph 3.3 defines the Model 1391 SCPI programming messages. Paragraph 3.4 demonstrates how to operate the Model 1391 using the defined messages.

3.2 Connectors and LED Indicators

This paragraph describes the Model 1391 front panel connectors and LED indicators. Figure 3-1 illustrates the front panel; bold numbers identify the indicators and connectors. Table 3-1 describes the function of each item shown in figure 3-1.

3.3 Model 1391 Programming

The Model 1391 communicates within the SCPI (Standard Commands for Programmable Instruments) and IEEE 488.2 standards. It may also communicate using the CIIL (Control Interface Intermediate Language) language described in the MATE specification as an option. When the CIIL language is included, the "Native" SCPI language is also retained, because it has a much broader set of features. For MATE/CIIL information, refer to Appendix A at the end of this manual.

The standard Model 1391 must respond to two types of commands: SCPI commands and IEEE 488.2 Common Commands. The IEEE 488.2 Common Commands support functions that are common to all instruments, such as reset, self test and status reporting. Common Commands are non-heirarchical (can be included within SCPI commands without disturbing their heirarchical relationships) and are easily identified by their leading asterisk (*).

SCPI commands support functions that are specific to the instrument. The SCPI language is heirarchical, requiring commands to be entered in a very specific fashion, and this manual contains tabular and graphical representations of the logic used by the SCPI *parser* (the 1391's firmware) to process commands.

This section provides the following information:

SCPI Command Table	Paragraph 3.3.1.
Command Message Format	Paragraph 3.3.2.
Model 1391 SCPI Commands	Paragraph 3.3.3.
Self Test Query Response	Paragraph 3.3.4.
System Trigger	Paragraph 3.3.5.
IEEE 488.2 Common Commands	Paragraph 3.3.6.

3.3.1 SCPI Command Table

Table 3-2 lists the SCPI commands used in the Model 1391 and indicates their hierarchical relationships. The IEEE 488.2 Common Commands are listed in a separate table (Table 3-4). The SCPI Command Table is organized as follows:

Keyword	Parameter Form	Notes
[SOURce]		
:FREQuency		
[:CW]	<numeric_value>	
:MODE	<list>	
STARt	<numeric_value>	
STOP	<numeric_value>	

The indentations of *keywords* indicates their hierarchical relationships according to a tree system. The left-most edge is called the *root node*. Keywords closer to the root node are higher in hierarchy; lower nodes are to the right of their parent node. To program or query a settable parameter, the full path must be defined to reach the keyword appended with the required parameter form. A SCPI programming string typically starts at the root node and proceeds to the right through branch nodes to the *leaf node*. This string of keywords separated by colons and completely defining a single path is defined as a Program Header, and is commonly referred to as a "command" (see paragraph 3.3.2) or as a "query" (see paragraph 3.3.2.6). A Program Header followed by Program Data is defined as a Program Message Unit (paragraph 3.3.2.1).

In the example above, the left-most keyword, [SOURce], is directly off the root node. Nodes in this position are called *Subsystems*, and all keywords

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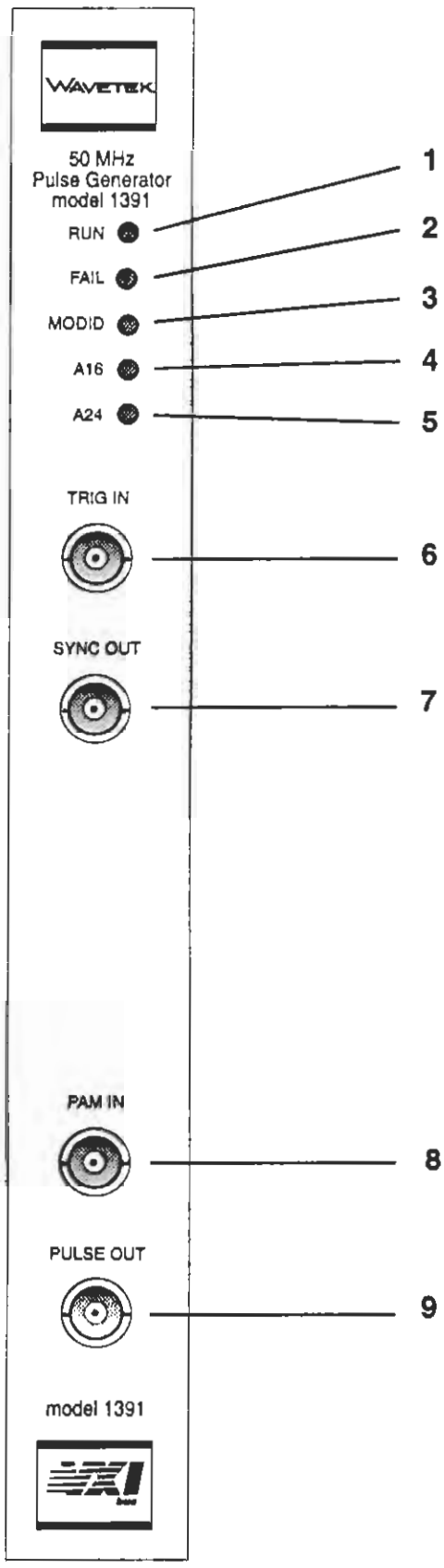


Figure 3-1. Model 1391 Front Panel

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Table 3-1. Model 1391 Front Panel

Item	Item Name	Function
1	RUN LED Indicator	When lit, indicates the VXIbus Interface Module microprocessor is running.
2	FAIL LED Indicator	When lit, indicates the VXIbus Interface Module registers are not initialized.
3	MODID LED Indicator	This indicator turns on momentarily indicating the Resource Manager has detected the presence of the model 1391.
4	A16 LED Indicator	When lit, indicates that devices on the VXIbus are accessing the generator's A16 registers.
5	A24 LED Indicator	This indicator illuminates during a VMEbus access to the A24 shared memory. This LED will not function in a Model 1391.
6	TRIG IN Connector	This connector receives the external trigger signal for the Model 1391's triggered, gated, and burst modes.
7	SYNC OUT Connector	This connector outputs TTL pulses for waveform synchronization.
8	PAM IN Connector	This connector is the input for external signals to Pulse Amplitude Modulate the PULSE OUT levels.
9	PULSE OUT Connector	This connector supplies the generator's waveform output. Output level is 150 mVpp to 16 Vpp into 50Ω.

indented under [SOURce] are part of the Source Subsystem. FREQuency is one of the main parameters under the Source Subsystem. The third level keywords under FREQuency set or query the various frequency related parameters. The brackets around the SOURce and CW keywords indicate that they are *implied nodes*, and they may be included in or omitted from the message at the programmer's option. When included, do not use the brackets in the command. Referring to Table 3-2, [SOURce] is the only Model 1391 Subsystem which is in brackets. This is the default Subsystem, and is assumed unless another Subsystem is specified at the start of a command.

The root node itself is an implied node and is not directly programmed. A colon at the start of a command resets the SCPI parser (included in instrument firmware) to the root node. A leading colon at the root node location is unnecessary (see paragraph 3.3.2.3).

3.3.1.1 Long and Short Form Keywords

The Model 1391 recognizes specific keywords that must be in the accepted long or short format. No other form of the keyword is accepted. For example, to send 'frequency' as part of a message, the short form keyword, shown in the table as upper case letters 'FREQ', or the long form of the same keyword containing both upper and lower case characters 'FREQuency' may be sent. Equal weight is given to upper and lower case characters when sending messages to the Model 1391.

3.3.2 Command Message Format

The following paragraphs provide the programmer/ operator with an introduction to the general rules that must be followed when sending messages to the Model 1391. For an understanding beyond what is covered in this paragraph, refer to the appropriate SCPI and IEEE 488.2 documents.

Operating the Model 1391 is easy, provided the programmer/operator pays strict attention to the message format, as shown in this manual. Each character, including spaces, must be properly placed or the Model 1391 will record any unrecognized parts of the command string as an error.

Table 3-2 shows the Model 1391 message structure and message relationships. Refer to this while working within this paragraph.

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Note

The Model 1391 records programming errors in its memory. The programmer/operator must use the 'SYSTEM:ERROR?' query to review these errors.

3.3.2.1 Program Message Unit

The Program Header (command or query) has been previously defined as a complete single path to a leaf node. It consists of one or more keywords separated by colons. It may also have a leading colon used to explicitly select the root node as the starting point. A Program Message Unit, <pmu>, consists of a Program Header followed (optionally) by Program Data.

3.3.2.2 Program Message

The Program Message (message) consists of one or more <pmu>'s deliminated by semicolons and followed by a Program Message Terminator, <pmt>.

3.3.2.3 Program Message Delimiters

To piece together the Program Message, the Model 1391 expects commands and parameters in the correct order (per Table 3-2), separated by defined delimiters: colons (:), semicolons (;), and spaces ( ).

Use the colon to separate keywords (nodes) within a Program Message Unit, for example,

```
VOLT:LEV:IMM:AMPL 5
```

Do not insert spaces between keywords and colons. Placing the optional colon at the beginning of a Program Message Unit ensures the parser starts from the "root" or top level. For example, a complete message with the leading colon is as follows:

```
:OUTP ON
```

The leading colon at the beginning of any new message is optional because the Program Message Terminator (<pmt>) at the end of the previous message sets the parser to the "root" level. The leading colon is not shown for most messages in this section.

The semicolon is used as a Program Message Unit Separator (<pms>). It permits the message units to be linked together in a single message. The colon may follow the semicolon to start the next message unit at the "root". For example,

```
SOUR:FREQ:CW 1E4;:OUTP ON
```

Without the colon following the semicolon, the message must start within the same subsystem as the previous message. For example:

```
SOUR:FUNC SQU;FREQ:CW 1E4
```

A space separates the Program Header from its data, as shown in the previous example.

3.3.2.4 Parameter Forms

For the Model 1391, parameters may be in the form of a decimal numeric value (numeric_data), alpha characters (character_data), or Boolean data. Examples of all three are:

```
FREQ 1000 (numeric_data)

FUNC SQU (character_data)

OUTP ON (Boolean_data)
```

Notice that in all cases, a space separates the header from data.

Numeric data values for most parameters may be in the form of an integer, a fixed or floating point value, or a special keyword as shown in the following:

integer;

```
FREQ 1000
```

fixed point;

```
FREQ 10.1
```

floating point;

```
FREQ 10E3
```

special form character;

```
FREQ MIN
```

When any of the three special form decimal numeric value keywords, 'MINimum', 'MAXimum', or 'DEFault', are sent, the parameter being addressed is set to a predetermined numeric value. The 'MAXimum' and 'MINimum' numeric values are the upper and lower limit values of the parameter. The 'DEFault' numeric value is within the limits of the parameter selected. Defaults values are listed in paragraph 3.4.3.

The Model 1391 uses several character data keywords. These are shown in Table 3-2.

Boolean data expresses an enabled ('on' or '1') or disabled ('off' or '0') state.

3.3.2.5 Program Message Terminators

The Model 1391 accepts New Line (NL, <LF>), END, or NL with END as the Program Message Terminator (<pmt>). However, the END (<EOI>) is the preferred <pmt> because it initiates an immediate transfer from the command/data buffer to the Language Processor for parsing. The other terminators may be delayed until the buffer fills.

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Table 3-2. Model 1391 Command Summary

KEYWORD	PARAMETER FORM	NOTES
CALibration		
[:ALL]?		
INITiate		
[:IMMediate]		
:CONTinuous	<Boolean_data> (ON)	
OUTPut		
:ECLTrg<n>		<n>=0 to 1 VXIbus ECLTrigger lines
[:STATe]	<Boolean_data> (OFF)	
:SOURce	<TRIP | PULSe>	
[:STATe]	<Boolean_data> (OFF)	
:SUMBus		
[:STATe]	<Boolean_data> (OFF)	
:TTLTrg<n>		<n>=0 to 7 VXIbus TTLTrigger lines
[:STATe]	<Boolean_data> (OFF)	
:SOURce	<TRIP | PULSe>	
RESet		
[SOURce]		
:FREQuency		
[:CW | FIXed]	<numeric_value>	
:FUNCtion		
[:SHAPe]	(<PULSe | SQUare>)	
:MARKer		
:TYPE	<CLOCk | GATE>	
[:STATe]	<Boolean_data> (OFF)	
:PULSe		
:WIDTh	<numeric_value>	
:DELay	<numeric_value>	
:DOUBle		
:DELay	<numeric_value>	
[:STATe]	<Boolean_data> (OFF)	
:POLarity	<NORMal | COMPlement | INVerted>	
:PERiod	<numeric_value>	
:TRANsition		
:STATe	<Boolean_data> (OFF)	
[:LEADing]	<numeric_value>	
:TRAiling	<numeric_value>	
:AUTO	<Boolean_data> (ON)	
:SUMBus		
[:STATe]	<Boolean_data> (OFF)	
:VOLTage		
[:LEVel]		
[:IMMediate]		
:HIGH	<numeric_value>	
:LOW	<numeric_value>	
[:AMPLitude]	<numeric_value>	
:OFFSet	<numeric_value>	

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Table 3-2. Model 1391 Command Summary (Continued)

KEYWORD	PARAMETER FORM	NOTES
[SOURce] (Continued) :PULM [:STATe] :AMPLitude	<Boolean_data> (OFF) <BIPolar | POSitive | NEGative>	
STATus :OPERation :CONDition? :ENABle [:EVENt]? :QUEStionable :CONDition? :ENABle [:EVENt]? :PRESet	<numeric_value> <numeric_value>	
SYSTem :ERRor? :DATE :TIME :VERSion? :LANGuage :CIIL	<year>, <month>, <day> <hour>, <minute>, <second>	1391 MATE only
TRIGger :COUNt :LEVel :GATE [:STATe] :MODE :MODE :SLOPe :SOURce :TIMer	<numeric_value> <numeric_value> <Boolean_data> (OFF) <SYNChronous | EXTWidth> <MASTer | SLAVe> <POSitive | NEGative> <INTernal | BUS | EXTernal | TTLTrg<n>| ECLTrg<n> | TOFF> <numeric_value>	<n> = 0 to 7 VXIbus TTLTrigger lines or 0 to 1 ECLTrigger lines.
DIAGnostic :CALibrate? :CALibrate :MEASure :MEASure? :SAVE :INIT	<step> <step>,<numeric_value> <step>	
TEST [:ALL]?		

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3.3.2.6 Queries

Unless otherwise indicated, each header with a parameter form also has a query form so that the current setting may be reported back. A query is programmed by following the leaf node keyword with a question mark (?), no space. For example, send:

```
SOUR:FREQ:CW?
```

or the reduced form:

```
FREQ?
```

to query the frequency setting. The response for this query is a floating point numerical value representing the frequency in Hertz. For example, if the response is 1 kHz, the returned value is:

```
1.000000E+03
```

For queries that include parameters, the question mark and a space are inserted prior to the parameter:

```
FREQ? MAX
```

Some commands may exist in query form only:

```
SYSTEM:ERROR?
```

Some queries are mandated such as `*ESE?`, `*SRE?`, and `*TST?`; see paragraph 3.3.4.

3.3.3 Model 1391 SCPI Commands

This paragraph introduces the operator to the Model 1391 SCPI command set. Paragraph 3.4 covers the relationship between these units. For a description of message format, refer to paragraph 3.3.2. This paragraph uses only the short form keyword recognized by the Model 1391 (refer to Table 3-2). Program Message Terminators are assumed, and therefore not shown in the examples. However, most optional keywords are shown to document the program flow.

3.3.3.1 CALibration Subsystem

The IEEE-488.2 calibration query (see paragraph 3.3.2.6) causes an internal Self Calibration to be performed and a response to be placed in the Output Queue. The value of 0 is returned if the self calibration passed. The interpretation of the value returned in the event of a failed self calibration is listed in Appendix C.

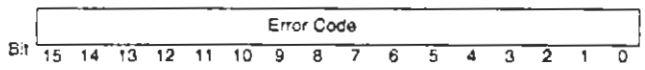
The `*CAL?` query invokes the same internal Self Calibration functions and returns the same reponse as the SCPI `CALibration[:ALL]?` query. Following is the CALibrate Substem excerpted from the SCPI Command Table:

```
CALibration
  [:ALL]?
```

```
CALibration[:ALL]?
```

Performs a Self Calibration and stores the calibration data in non-volatile memory. If the calibration is successful, use of the data is enabled. If the calibration is unsuccessful for any reason, use of the data is disabled and default correction factors are used. The response value will indicate the nature of the failure.

The value of a 16-bit Self Calibration Status Word is returned in response to the calibration query. The format of the Status Word is shown below:



Self Calibration Status Word

The Error Code field contains a bit weighted code that is unique to the failed step. Refer to Appendix C for more information.

3.3.3.2 TEST Subsystem

The IEEE-488.2 self test query causes an internal Self Test to be performed and a response to be placed in the Output Queue. The value of 0 is returned if the self test passed. The interpretation of the value returned in the event of a failed self test is listed in Appendix D.

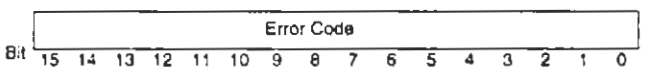
The `*TST?` query invokes the same internal Self Test functions and returns the same reponse as the SCPI `TEST[:ALL]?` query. Following is the TEST Subsystem excerpted from the SCPI Command Table:

```
TEST
  [:ALL]?
```

```
TEST[:ALL]?
```

Performs a Self Test and sends the results to the Output Queue. The response value will indicate the nature of the failure.

The value of a 16-bit Self Test Status Word is returned in response to the calibration query. The format of the Status Word is shown below:



Self Test Status Word

The Error Code field contains a bit weighted code that is unique to the failed step. Refer to Appendix D for more information.

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3.3.3.3 INITiate Subsystem

```
INITiate
  [:IMMediate]
  :CONTinuous     <Boolean>
```

```
INITiate[:IMMediate]
```

This command is included to support the SCPI specification, but it does not alter the setup of the model 1391.

```
INITiate:CONTinuous <ON|1|OFF|0>
```

This command selects between continuous mode of operation and a non-continuous (triggered, gated, or burst) mode of operation.

3.3.3.4 OUTPut Subsystem

```
OUTPut
  :ECLTrg<n>
     [:STATe]     <Boolean_data>
     :SOURce      <TRIP | PULSe>
  [:STATe]        <Boolean_data>
  :SUMBus
    [:STATe]      <Boolean_data>
  :TTLTrg<n>
     [:STATe]     <Boolean_data>
     :SOURce      <TRIP | PULSe>
```

```
OUTPut:ECLTrg<n>[:STATe]
                <ON|1|OFF|0>
```

Enables the selected model 1391 SOURce signal to drive one of the VXIbus backplane ECL Trigger Lines. Each ECL Trigger Line output can be separately enabled, one at a time. Valid numeric suffixes (<n>) are in the range 0 through 1. Default selection is "OFF" (0), enabled with "ON" or "1".

```
OUTPut:ECLTrg<n>:SOURce
                <TRIP|PULSe>
```

Selects the signal (internal to the 1391) which is to be enabled to drive one of the backplane ECL Trigger Lines. The default selection is the "trigger pulse", TRIP, which exists at the circuit node between a signal selector and the inputs to the width and delay *one-shot generators*. The selector chooses one signal among several, dependant upon operating mode, to trigger the one-shots. The PULSe signal is the output of the one-shots before it is applied to the analog output conditioning circuit blocks.

```
OUTPut[:STATe] <Boolean>
```

Controls the state of the function output relay, turning the signal to the PULSE OUT on or off. Default selection is "OFF" (0), enabled with "ON" or "1".

```
OUTPut:SUMBus[:STATe] <ON|1|OFF|0>
```

Connects or disconnects the Model 1391 to the VXIbus backplane SUMBUS line. Default selection is "OFF" (0); enabled with "ON" or "1". When ON, the Model 1391 drives the SUMBUS with a current proportional to the voltage waveform at PULSE OUT.

```
OUTPut:TTLTrg<n>[:STATe]
                <ON|1|OFF|0>
```

Enables the selected model 1391 SOURce signal to drive one of the VXIbus backplane TTL Trigger Lines. Each TTL Trigger Line output can be separately enabled, one at a time. Valid numeric suffixes (<n>) are in the range 0 through 7. Default selection is "OFF" (0), enabled with "ON" or "1".

```
OUTPut:TTLTrg<n>:SOURce
                <TRIP|PULSe>
```

Selects the signal (internal to the 1391) which is to be enabled to drive one of the backplane TTL Trigger Lines. The default selection is the "trigger pulse", TRIP, which exists at the circuit node between a signal selector and the inputs to the width and delay *one-shot generators*. The selector chooses one signal among several, dependent upon operating mode, to trigger the one-shots. The PULSe signal is the output of the one-shots before it is applied to the analog output conditioning circuit blocks.

3.3.3.5 RESet Subsystem

```
RESet
```

Resets all parameters to their default state (see paragraph 3.4.3).

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3.3.3.6 SOURce Subsystem

```
[SOURce]
  :FREQuency
    [:CW | FIXed] <numeric_value>
  :FUNCtion
    [:SHAPe]      <PULSe | SQUare>
  :MARKer
    :TYPE         <CLOCk | GATE>
    [:STATe]      <Boolean>
  :PULSe
    :WIDTh        <numeric_value>
    :DELay        <numeric_value>
    :DOUBle
      :DELay      <numeric_value>
      [:STATe]    <Boolean>
    :POLarity     <NORMal|COMPlement|
                  INVerted>
    :PERiod       <numeric_value>
    :TRANsition
      :STATe      <Boolean>
      [:LEADing]  <numeric_value>
      :TRAiling   <numeric_value>
        :AUTO     <Boolean>
  :SUMBus
    [:STATe]      <Boolean>
  :VOLTage
    [:LEVel]
      [:IMMediate]
        :HIGH     <numeric_value>
        :LOW      <numeric_value>
        [:AMPLitude] <numeric_value>
        :OFFSet   <numeric_value>
```

`[SOURce:]FREQuency`
`[:CW | FIXed] <numeric_value>`

Sets pulse generator "frequency" as an alternate to setting `SOUR:PULS:PER <value>` to control the pulse period. FREQuency and PERiod are "coupled" parameters, so that programming one updates the value of the other. "CW" and "FIXed" are interchangable. Parameter values range from a MINimum of 0.001 Hz to a MAXimum of 100 MHz. DEFault value is 1 MHz.

`[SOURce:]FUNCtion`
`[:SHAPe] <PULSe|SQUare>`

Selects the shape of the output signal. For the Model 1391, the Functions available at the PULSE OUT are the PULSe and the SQUare. Additionally, with the PULSe selected, other PULSe parameters in this Subsystem are used to select single, delayed, or double pulses within each period. Default selection is PULSe.

`[SOURce:]MARKer[:STATe] <ON|1|OFF|0>`

Enables or disables the SYNC output. Default selection is "OFF" (0); enabled with "ON" or "1".

`[SOURce:]MARKer:TYPE <CLOCk|GATE>`

Selects the method used to generate the SYNC output.

- CLOCk — A signal derived from the repetition rate (period) generator.
- GATE — A signal derived from the triggering circuitry. The GATE signal goes true when a trigger/gate/burst cycle is initiated, and goes false when the trigger/gate signal goes false.

`[SOURce:]PULSe:WIDTh <numeric_value>`

Sets the width of the pulse waveform in seconds. Defined as the time between the 50% points of leading and trailing transitions. Each pulse period can have single or double pulses. Width parameter values range from a MINimum of 10 ns to a MAXimum of 2000 s. DEFault value is 250 ns.

`[SOURce:]PULSe:DELay <numeric_value>`

Sets the delay of a single pulse waveform in seconds. Defined as the time between the start of a pulse period (50% point of SYNC OUT) and the 0% point of the leading transition of a single pulse. Delay parameter values range from a MINimum of 0 ns to a MAXimum of 2000 s. DEFault value is 0 ns.

`[SOURce:]PULSe:DOUBle:DELay`
`<numeric_value>`

Sets the delay of a double pulse waveform in seconds. Defined as the time between the start of a pulse period (50% point of SYNC OUT) and the 0% point of the leading transition of the second pulse. Delay parameter values range from a MINimum of 20 ns to a MAXimum of 2000 s. DEFault value is 400 ns.

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`[SOURce:]PULSe:DOUBle[:STATe] <ON|1|OFF|0>`

Enables or disables the double pulse function. Default selection is "OFF" (0); enabled with "ON" or "1". Enabling the double pulse selects the `PULSe:DOUBle:DELay` parameter in place of the `PULSe:DELay` parameter.

`[SOURce:]PULSe:POLarity <NORMal|COMPlement|INVerted>`

Allows the internal signal at the *one-shot generator* output to be inverted (complemented) before being applied to the output circuits and to the PULSE OUT. Default selection is NORMal.

- NORMal — Pulse leading transitions are rising transitions. Pulse width is active high.
- COMPlement — Pulse leading transitions are falling transitions. Pulse width is active low.
- INVerted — Alias for COMPlement.

`[SOURce:]PULSe:PERiod <numeric_value>`

Sets the period of the pulse waveform in seconds. Defined as the time between the 50% points of the rising transitions of two adjacent SYNC OUT waveforms (MARKer:TYPE CLOCk). This is the same as the time between two adjacent, *identical* transitions at the PULSE OUT. Each pulse period can have single or double pulses. Period parameter values range from a MINimum of 10 ns to a MAXimum of 1000 s. DEFault value is 1 µs. PERiod is "coupled" to the FREQuency parameter such that changing one parameter updates the other.

`[SOURce:]PULSe:TRANsition:STATe <ON|1|OFF|0>`

Sets the pulse transition time generators ON or OFF. Default is OFF. If the state is off, then the transitions are set to the minimum values of 5 ns. If the state is on, the transitions are determined by the values for LEADing and TRAiling.

`[SOURce:]PULSe:TRANsition[:LEADing] <numeric_value>`

Sets the width of the pulse waveform transitions in seconds when TRANsition state is ON. Defined as the time between the 10% point and 90% point of a leading transition. LEADing parameter values range from a MINimum of 5 ns to a MAXimum of 50 µs. DEFault value is 5 ns.

`[SOURce:]PULSe:TRANsition:TRAiling <numeric_value>`

Sets the width of the pulse waveform transitions in seconds when TRANsition state is ON. Programming this value sets "auto-trailing" OFF if it is ON. Defined as the time between the 10% point and 90% point of a trailing transition. TRAiling parameter values range from a MINimum of 5 ns to a MAXimum of 50 µs. DEFault value is 5 ns.

`[SOURce:]PULSe:TRANsition:TRAiling:AUTO <ON|1|OFF|0>`

When enabled, causes the parameter values for the TRAiling transition time to be set along with the LEADing transition time. When disabled, the TRAiling transition has its own parameter values, and LEADing and TRAiling transitions are independent, restricted only by the maximum 10:1 ratio. Default selection is "ON" (1); disabled with "OFF" or "0".

`[SOURce:]SUMBus[:STATe] <ON|1|OFF|0>`

Connects or disconnects the Model 1391 to the VXIbus backplane SUMBUS line. Default selection is "OFF" (0); enabled with "ON" or "1". When set to ON, the Model 1391 sums the waveform on the SUMBUS with the PULSE OUT waveform.

`[SOURce:]VOLTage[:LEVel][:IMMediate]:HIGH <numeric_value>`

Sets the amplitude in volts peak (50Ω) of the upper level of the pulse waveform at the PULSE OUT. Should be programmed along with the LOW LEVel parameter (see the NOTE below). HIGH level parameter values range from a MINimum of –7.850 V (50Ω) to a MAXimum of +8V (50Ω). DEFault value is +2.50 V (50Ω).

NOTE

The AMPLitude and OFFSet parameters, and the HIGH and LOW level parameters, are two ways of setting the output levels. Use HIGH and LOW together, or use AMPLitude and OFFSet together. These are "coupled" functions – setting up one pair causes the other pair to update to equivalent values.

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`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`:LOW <numeric_value>`

Sets the amplitude in volts peak (50Ω) of the lower level of the pulse waveform at the PULSE OUT. Should be programmed along with the HIGH LEVel parameter (see the NOTE above). LOW level parameter values range from a MINimum of –8V (50Ω) to a MAXimum of +7.850 V (50Ω). DEFault value is –2.50 V (50Ω).

`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`:OFFSet <numeric_value>`

Sets the offset in volts dc (50Ω) of the pulse waveform at the PULSE OUT. Should be programmed along with the AMPLitude LEVel parameter (see the NOTE above). OFFSet parameter values range from a MINimum of –7.925 Vdc (50Ω) to a MAXimum of +7.925 Vdc (50Ω). DEFault value is 0.

`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`[:AMPLitude] <numeric_value>`

Sets the amplitude in volts peak-to-peak (50Ω) of the pulse waveform at the PULSE OUT. Should be programmed along with the OFFSet LEVel parameter (see the NOTE above). AMPLitude parameter values range from a MINimum of 0.150 Vpp (50Ω) to a MAXimum of 16 Vpp (50Ω). DEFault value is 5 Vpp (50Ω).

NOTE

Restrictions on output levels: The sum of Vpk amplitude (half the programmed Vpp value) and the absolute offset value cannot exceed 8V. Additionally, for pulses less than 0.5 Vpp, this restriction is reduced to 2 V.

When setting the output in terms of HIGH and LOW levels, the HIGH level must be at least 0.15 V more positive than the LOW level. HIGH and LOW levels are programmed within a ±8 V window, reduced to a ±2 V window when (upper – lower) is less than 0.5 V.

`[SOURce:]PULM[:STATe] <ON|1|OFF|0>`

Connects or disconnects the PAM IN connector to the Model 1391. This enables or disables Pulse Amplitude Modulation. Default selection is "OFF" (0); enabled with "ON" or "1".

`[SOURce:]PULM:AMPLitude`
`<BIPolar|POSitive|NEGative>`

Determines how the Model 1391 pulse amplitude modulates the PULSE OUT signal using the PAM input. Default selection is BIPolar.

- BIPolar — The PULSE OUT waveform's lower level is a mirror image of its upper level. The instantaneous amplitude of the levels is a linear function of the signal at the PAM input.
- POSitive — The PULSE OUT waveform's lower level is fixed at the programmed `OFFSet` setting. The instantaneous amplitude of the upper level is a linear function of the signal at the PAM input.
- NEGative — The PULSE OUT waveform's upper-level is fixed at the programmed `OFFSet` setting. The instantaneous amplitude of the lower level is an inverted linear function of the signal at the PAM input.

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3.3.3.7 SYSTem Subsystem

```
SYSTem
  :ERRor?
  :DATE     <year>,<month>,<day>
  :TIME     <hour>,<minute>,<second>
  :VERSion?
  :LANGuage
   :CIIL
```

`SYSTem:DATE <year>,<month>,<day>`

Sets the system date using the following format: yyyy,mm,dd.

`SYSTem:ERRor?`

Returns the next message from the system error queue. With each query, the unit returns a number followed by a brief description. The error queue holds up to eight errors, with one returned for each query sent, until the queue is empty. Table 3-3 describes the system error messages.

`SYSTem:TIME <hour>,<minute>,<second>`

Sets the system time using the following 24 hour format: hh,mm,ss.

`SYSTem:TIME?`

Returns the system's idea of the time in the following format:

`<hour>,<minute>,<second>`

`SYSTem:VERSion?`

Returns the system's firmware version number in the following format:

`<manufacturer>,<model>,<serial_number | 0>,<firmware_level | 0>`

`SYSTem:LANGuage:CIIL`

Used only with the MATE/CIIL option. A unit with the option installed uses CIIL as its default command language and SCPI as its alternate or "native" command language. Many of the more complex features in the SCPI command set are not implemented in CIIL. When in CIIL, the operator can use the CIIL GAL command to go to SCPI to accomplish a task needing the additional features. This command is used to return to CIIL from SCPI.

3.3.3.8 TRIGger Subsystem

```
TRIGger
  :COUNt          <numeric_value>
  :LEVel          <numeric_value>
  :GATE
    :MODE       <SYNchronous|EXTWidth>
    [:STATe]      <Boolean>
  :MODE           <MASTer|SLAVe>
  :SLOPe          <POSitive|NEGative>
  :SOURce       <INTernal|BUS|EXTernal
                  |TTLTrg<n>|ECLTrg<n>|TOFF>
  :TIMer          <numeric_value>
```

NOTE

When INITiate:CONTinuous is ON, the pulse generator mode is continuous, regardless of the settings in this Subsystem. When INITiate:CONTinuous is OFF, the mode is non-continuous and determined by these settings. When GATE[:STATe] is OFF, the pulse generator is in a triggered mode if the COUNt parameter is 1, or in a burst mode if the COUNt is set higher than 1. When the GATE[:STATe] is ON, the pulse generator is in a gated mode, using either the SYNChronous or EXTWidth sub-modes.

`TRIGger:COUNt <numeric_value>`

This command sets the number of pulse periods generated after a trigger is received. MINimum and DEFault value is 1. MAXimum value is 10,000,000.

`TRIGger:GATE[:STATe] <ON|1|OFF|0>`

This enables or disables gated mode of operation. See the above note. Default selection is "OFF" (0); enabled with "ON" or "1".

`TRIGger:GATE:MODE <SYNChronous|EXTWidth>`

Selects the GATE sub-mode. Default is SYNChronous.

- **SYNChronous** The pulse generator is quiescent at the lower level value. When a trigger is received, the generator outputs pulse periods (with selected pulse parameters) as long as the gating signal is true. When the gating

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signal goes false before the 50% point of the current period, the generator completes its current period, and then returns to the quiescent state. When the gating signal goes false beyond the 50% point of the current period, the generator completes its current period and the next full period, and then returns to the quiescent state.

- EXTWidth — When the triggering signal is false, the pulse generator outputs its lower level. When the triggering signal is true, the pulse generator outputs its upper level. Transition times can be programmed.

`TRIGger:LEVel <numeric_value>`

This command selects the voltage threshold level for the trigger comparator. This determines the triggering point on an external signal applied to the TRIG IN connector. Determine TRIGger SLOPe at the same time. MINimum value is –10 V and MAXimum value is +10V. DEFault value is 1V.

`TRIGger:MODE <MASTer|SLAVe>`

This command selects whether a 1391 module is independent, a master or a slave. A master supplies a trigger to other modules. A slave picks up the trigger from a master. Master/Slave triggering operation allows multiple modules in a VXIbus chassis to operate as a multiple channel pulse generator system. Timing between channels is very tightly controlled. When set to SLAVe, but not making use of a trigger from a master, then the module is "independent". Default is SLAVe.

- MASTer — The module supplies its SYNC OUT signal to an ECLTrg line for slave modules to use.
- **SLAVe** — Can pick up the master trigger from an ECLTrg line.

`TRIGger:SLOPe <POSitive|NEGative>`

This command selects whether a trigger is initiated as the selected trigger signal passes through the threshold set by trigger LEVel in a positive-going or a negative-going direction. Default is POSitive.

`TRIGger:SOURce <INTernal|BUS|EXTernal|TTLTrg<n>|ECLTrg<n>|TOFF>`

Selects the source of the trigger signal. The trigger signal is used to initiate activity when the instrument is in a non-continuous mode of operation. Default is INTernal.

- EXTernal — Selects an external signal at the TRIG IN connector as the trigger source.
- **INTernal** — Selects the Model 1391 internal signal programmed by the trigger TIMer as the trigger source.
- BUS — Selects the IEEE-488 bus (488.1 GET command or 488.2 *TRG command) or the VXIbus (Word Serial Trigger command) as the triggering source.
- TTLTrg<n> — Selects one of the VXIbus TTL Trigger Lines from the backplane. Valid numeric suffixes are in the range 0 through 7.
- ECLTrg<n> — Selects one of the VXIbus ECL Trigger Lines from the backplane. Valid numeric suffixes are 0 and 1.
- TOFF — Disables all trigger sources.

`TRIGger:TIMer <numeric_value>`

Sets the period of an internal periodic signal source. The timer signal acts as a trigger when it is the selected trigger source. MINimum value is 20 ns and MAXimum value is 1000 s. DEFault value is 10 ms.

3.3.3.8 DIAGnostic Subsystem

```
DIAGnostic
  :CALibrate?    <step>
  :CALibrate
    :MEASure  <step>,<numeric_value>
    :MEASure?  <step>
    :SAVE
    :INIT
```

`DIAGnostic:CALibrate? <step>`

Initiates the manual calibration system. The <step> entered is the manual calibration step number that is to be set up for and performed. Some steps in the manual calibration procedure are handled automatically by the Model 1391, and this will be indicated by the return message. Manual steps requiring measurements with external test equipment and/or adjustments will return a message giving the appropriate instructions.

`DIAGnostic:CALibrate:MEASure <step>,<numeric_value>`

When the particular step requires an external measurement (see above), this command allows the operator to

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enter the value measured into the Model 1391's volatile memory. These values may be entered step-by-step as the data is taken, or all at once at the end of a successful manual calibration. See the SAVe command for making the new data non-volatile.

`DIAGnostic:CALibrate:MEASure? <step>`

Query form of the above command. Allows operator to query the currently stored Calibration Data for the given step number.

`DIAGnostic:CALibrate:SAVe`

Transfers the block of calibration data values from volatile to non-volatile memory. After the manual calibration has been successfully completed, the operator should send this command so that the new values are used to optimize the unit's accuracy.

`DIAGnostic:CALibrate:INIT`

Replaces the current calibration data values in non-volatile memory with a set of "default" values in ROM. The default values are nominal values which should aid in troubleshooting whether a unit's malfunction is due to miscalibration or to hardware failure.

3.3.3.10 STATus Subsystem

```
STATus
  :OPERation
    :CONDition?
    :ENABle        <NRf>
    [:EVENt]?
  :PRESet
  :QUEStionable
    :CONDition?
    :ENABle        <NRf>
    [:EVENt]?
```

`STATus:OPERation:CONDition?`

Returns the contents of the Operation Condition Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:OPERation:ENABle <NRf>`

Sets the enable mask of the Operation Event Register, which allows true conditions to be reported in the summary bit. The Model 1391 supports the command by saving the mask value and by not generating an error, although the Status registers do not exist.

The <NRf> notation indicates that SCPI's <numeric_value> format is not used in this case. Refer to the IEE488.2 <DECIMAL NUMERIC PROGRAM DATA>, flexible Numeric Representation for more information.

The "STATus:OPERation:ENABle?" query returns the enable mask of the Operation Event Register. The Model 1391 returns the value sent previously with the command above using the <NR1> format.

`STATus:OPERation[:EVENt?]`

Returns the contents of the Operation Event Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:PRESet`

Sets the enable registers to all 1's. The Model 1391 accepts the command without performing any action.

`STATus:OPERation:CONDition?`

Returns the contents of the Operation Condition Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:OPERation:ENABle <NRf>`

Sets the enable mask of the Operation Event Register, which allows true conditions to be reported in the summary bit. The Model 1391 supports the command by saving the mask value and by not generating an error, although the Status registers do not exist.

The <NRf> notation indicates that SCPI's <numeric_value> format is not used in this case. Refer to the IEE488.2 <DECIMAL NUMERIC PROGRAM DATA>, flexible Numeric Representation for more information.

The "STATus:OPERation:ENABle?" query returns the enable mask of the Operation Event Register. The Model 1391 returns the value sent previously with the command above using the <NR1> format.

`STATus:OPERation[:EVENt?]`

Returns the contents of the Operation Event Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

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Table 3-3. Error Messages

Error Number	Message	Error Number	Message
0	"No error"	-222	"Data out of range"
-100	"Command error"	-223	"Too much data"
-101	"Invalid character"	-224	"Illegal parameter value"
-102	"Syntax error"	-230	"Data corrupt or stale"
-103	"Invalid separator"	-231	"Data questionable"
-104	"Data type error"	-240	"Hardware error"
-105	"GET not allowed"	-241	"Hardware missing"
-108	"Parameter not allowed"	-250	"Mass storage error"
-110	"Command header error"	-251	"Missing mass storage"
-111	"Header separator error"	-252	"Missing media"
-112	"Program mnemonic too long"	-253	"Corrupt media"
-113	"Undefined header"	-254	"Media full"
-114	"Header suffix out of range"	-255	"Directory full"
-120	"Numeric data error"	-257	"File name error"
-121	"Invalid character in number"	-258	"Media protected"
-123	"Exponent too large"	-260	"Expression error"
-124	"Too many digits"	-261	"Math error in expression"
-128	"Numeric data not allowed"	-270	"Macro error"
-130	"Suffix error"	-271	"Macro syntax error"
-131	"Invalid suffix"	-272	"Macro execution error"
-134	"Suffix too long"	-273	"Illegal macro label"
-140	"Character data error"	-274	"Macro parameter error"
-144	"Character data too long"	-275	"Macro definition too long"
-148	"Character data not allowed"	-276	"Macro recursion error"
-150	"String data error"	-277	"Macro redefinition not allowed"
-151	"Invalid string data"	-278	"Macro header not found"
-158	"String data not allowed"	-280	"Program error"
-160	"Block data error"	-281	"Cannot create program"
-161	"Invalid block data"	-282	"Illegal program name"
-168	"Block data not allowed"	-283	"Illegal variable name"
-170	"Expression error"	-284	"Program currently running"
-171	"Invalid expression"	-285	"Program syntax error"
-178	"Expression data not allowed"	-286	"Program run time error"
-180	"Macro error"	-300	"Device specific error"
-181	"Invalid outside macro definition"	-310	"System error"
-183	"Invalid inside macro definition"	-311	"Memory error"
-184	"Macro parameter error"	-312	"PUD Memory lost"
-200	"Execution error"	-314	"Save/recall memory lost"
-201	"Invalid while in local"	-315	"Configuration memory lost"
-202	"Settings lost due to rtl"	-330	"Self test failed"
-210	"Trigger error"		

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3.3.4 IEEE-488.2 Common Commands

The *CAL? self calibrate query, the *TST? self test query, and the *TRG command are discussed elsewhere in this manual (along with their equivalent SCPI query or command).

The *CAL? query is equivalent to the SCPI CALibrate[:ALL]? query. The self calibration query is discussed in Appendix C of this operator's manual.

The *TST? query is equivalent to the SCPI TEST[:ALL]? query. The self test query is discussed in Appendix D of this operator's manual.

The *TRG is an IEEE Common Command used to provide a properly sequenced trigger and execute to an addressed 488.2 device. It triggers the Model 1391 via the VXI data bus ('BUS' must be selected as the trigger source in the Trigger subsystem).

The previous paragraphs describe in detail the three most commonly used IEEE Common Commands. Table 3-4 briefly describes the messages mandated by the 488.2 standards, plus optional commands supported by the model 1391.

3.4 Model 1391 Operation

The following paragraphs describe the SCPI language commands for various modes of operation for the Model 1391.

Continuous Operation	Paragraph 3.4.4
Marker Operation	Paragraph 3.4.5
SUMBUS Operation	Paragraph 3.4.6
PAM Operation	Paragraph 3.4.7
Triggered Operation	Paragraph 3.4.8
Gated Operation	Paragraph 3.4.9
Burst Operation	Paragraph 3.4.10
Internal Frequency Sweep	Paragraph 3.4.11

Before beginning, review the data in paragraphs 3.4.1, 3.4.2, and 3.4.3.

3.4.1 Output Terminations

Each output connector must be properly terminated during its use to minimize signal reflection or power loss due to an impedance mismatch. High quality 50Ω coax cable and terminations should be used for pulse waveform fidelity. Terminators should be placed at the end of the coax cable at the point of signal delivery. Figure 3-2 shows proper 50Ω termination for the PULSE OUT connector, with R_s representing the Model 1391 source impedance, R_L representing the termination or load resistance, and R_{IN} representing the receiving instrument input impedance. Table 3-5 lists all the input and output impedances of the Model 1391.

Table 3-5 Input and Output Impedances

Connector	Impedance
PULSE OUT	50Ω
SYNC OUT	50Ω, TTL (0 to >2.0 V terminated)
TRIG IN	≥1 kΩ, ≤10 pF
PAM IN	≥1 kΩ

Table 3-4 IEEE 488.2 Common Commands

Command	Function	Description
*CAL?	Calibration Query	Starts self-cal, places pass/fail response in output queue
*CLS	Clear Status Command	Clears Status Data Registers, forces OCIS/OQIS
*ESE	Standard Event Status Enable	Sets Event Status Enable Register bits
*ESE?	Standard Event Status Enable Query	Returns contents of Event Status Enable Register
*ESR?	Standard Event Status Register Query	Returns contents of Event Status Register
*IDN?	Identification Query	Identifies devices over the system interface
*OPC	Operation Complete Command	Requires oper. comp. message in Event Status Reg.
*OPC?	Operation Complete Query	ASCII '1' in dev. out. queue when operations complete
*RST	Reset Command	Resets the device
*SRE	Service Request Enable Command	Sets Service Request Enable Register bits
*SRE?	Service Request Enable Query	Returns contents of Service Request Enable Register
*STB?	Read Status Byte Query	Returns status and master summary status bytes
*TRG	Trigger Command	Initiates a properly sequenced trigger and execute
*TST?	Self Test Query	Starts self-test, places pass/fail response in output queue
*WAI	Wait - to - Continue Command	Blocks device commands until 'No-Op-Pend' flag is true

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3.4.2 Input/Output Protection

The Model 1391 provides protection for internal circuitry connected to input and output connectors. Refer to the Specifications in Section 1 of this manual to determine the level of protection associated with each input or output connector.

3.4.3 Power On/Reset Defaults

At power on, or as the result of sending `*RST` or `RESet`, the Model 1391 defaults to the following conditions:

Subsystem	SOURce
Operational Mode	CONTinuous
Function Shape	PULSe
Frequency value	1 MHz
Upper Level value	+2.5 V into 50Ω
Lower Level value	–2.5 V into 50Ω
Amplitude value	5 Vpp
Offset value	0 Vdc
Pulse Output	OFF
Pulse Period value	1 µs
Pulse Width value	250 ns
Pulse Delay value	0 ns
Double Pulse state	OFF
Double Pulse Delay	400 ns
Pulse Transition state	OFF (5 ns)
Leading Transition	5 ns
Trailing Transition	5 ns
Auto-Trailing state	ON
Pulse Polarity	NORMal
Sync Marker Output	OFF
Sync Marker Type	CLOCk
PAM Input	Disabled (Off)
PAM Mode	BIPolar
Sumbus	Off (not input or output)
Sumbus Mode	DRIVe
Trigger Mode	SLAVe
TTL Trigger Lines	Off (not input or output)
ECL Trigger Lines	Off (not input or output)
Trigger Slope	Positive
Trigger Level value	+1.0 V
Trigger Source	Internal
Trigger Timer	10 ms (100 Hz)
Trigger Count	1
Gate State	OFF
Gate Sub-Mode	SYNChronous

3.4.4 Continuous Operation

This paragraph shows how to set up the Model 1391 for a pulse waveform output using the default settings provided at power-on. The subsequent paragraphs under this heading will then demonstrate the continuous mode pulse period, pulse waveforms and characteristics, and the output levels. All of the parameters shown here are detailed in earlier paragraphs. Much of the information given here directly transfers to other modes.

Connect the Model 1391's PULSE OUT connector (terminated) to the device under test, as shown in figure 3-3. Use the SYNC OUT signal as a synchronizing source. Figure 3-4 illustrates the SYNC OUT and PULSE OUT relationships.

At power on, the Model 1391's PULSE OUT is always turned OFF. To enable the PULSE OUT connector, send the command:

```
OUTP:STAT ON
```

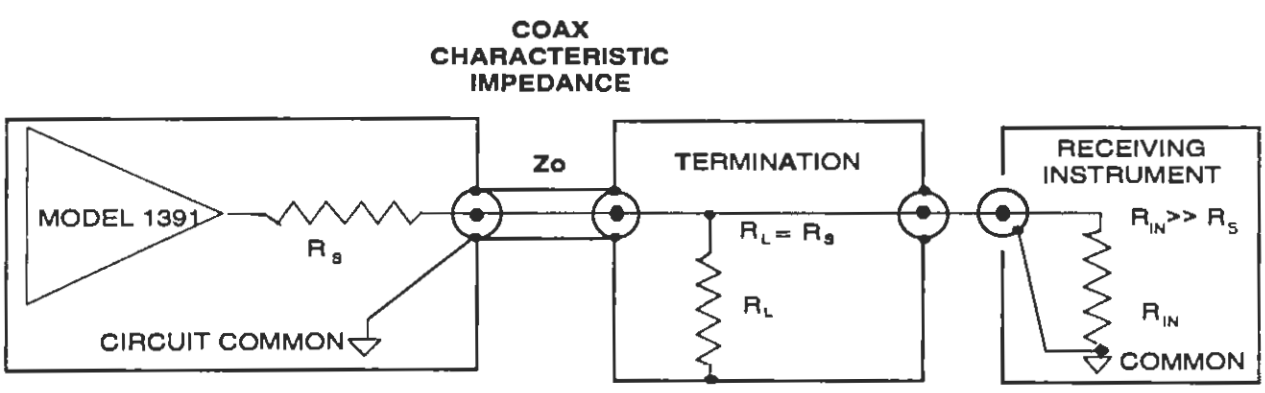


Figure 3-2. Output Termination

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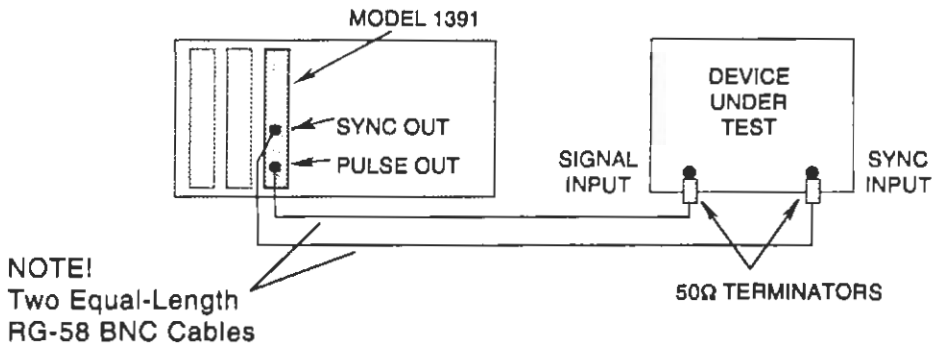


Figure 3-3. Model 1391 Basic Operation Setup

At power on, the Model 1391's SYNC OUT is always turned OFF. To enable the SYNC OUT connector, send the command:

```
SOUR:MARK:STAT ON
```

The two previous commands could be shortened and combined as follows:

```
OUTP ON;:MARK ON
```

Set up a 2 channel, high bandwidth oscilloscope as the DUT in Figure 3-3. Connect the SYNC to CH 1 and the PULSE to CH 2. Trigger the scope internally from CH 1. Compare the pulse waveform to Figure 3-4 below. The default pulse waveform should be a Single Pulse with its 0% point coincident with the 50% point of the rising edge of the SYNC, as shown in the diagram. The pulse period is 1 µs and the Leading Transition (t_r) and Trailing Transition (t_f) should both be no more than 5 ns. Verify 250 ns Pulse Width.

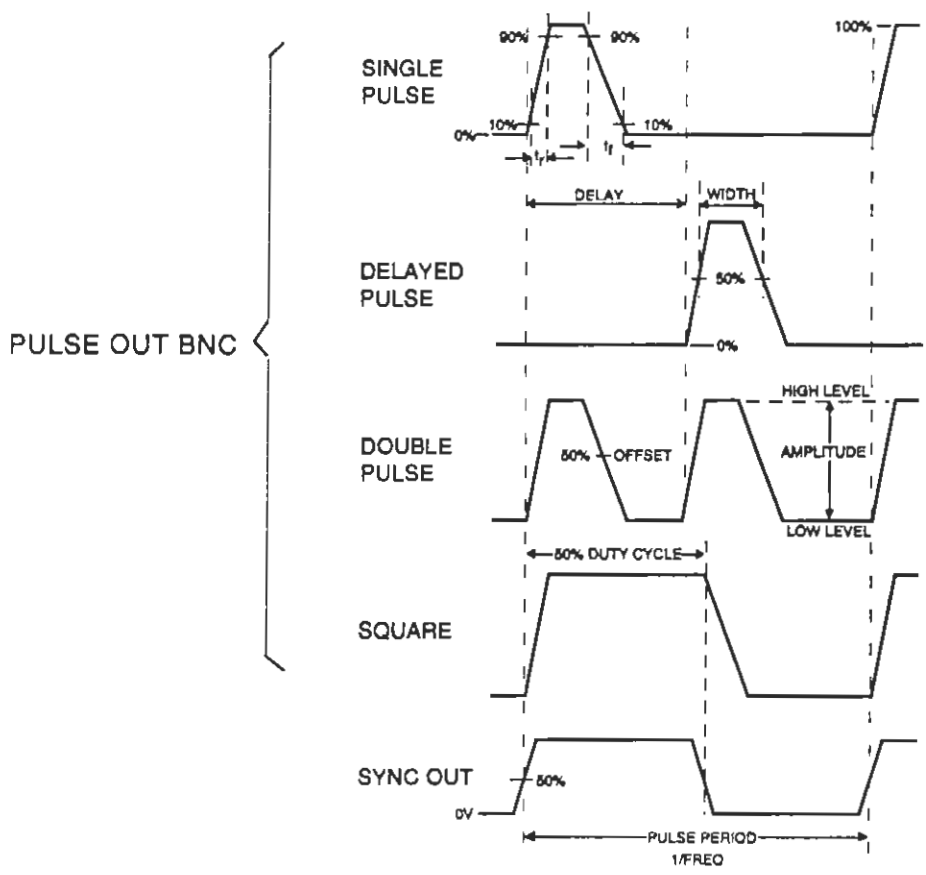


Figure 3-4. Continuous Waveform Characteristics

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3.4.4.1 Frequency/Period Parameters

The FREQuency and PERiod parameters are "coupled", meaning that setting one updates the other appropriately. The current default settings from the previous setup are 1 µs period and 1 MHz frequency. Change the period from 1 µs to 10 µs by sending:

```
PULS:PER 1E-5
```

Verify the frequency value has been updated by sending the query:

```
FREQ?
```

The returned response should be 'FREQ 1E5' (100 kHz). The display on the oscilloscope should now have a pulse period of 10 µs, with the other pulse parameters remaining the same.

3.4.4.2 Pulse Parameters

Programmable pulse parameters included in this paragraph are the WIDTh, LEADing TRANsition, TRAiling TRANsition, DELAY, and DOUBle DELay. Paragraphs 3.4.4 and 3.4.4.1 above have the Model 1391 set up in its default values except that the PULSE and SYNC outputs are ON and the period has been changed to 10 µs. There should be a 250 ns single pulse with 5 ns transitions on the oscilloscope. Change the single pulse width and transition times as follows:

```
PULS:TRAN:STAT ON
PULS:TRAN:TRA:AUTO ON
PULS:WIDT 2E-6
PULS:TRAN 200E-9
```

The first command enables the transition times for programming to values other than the default minimum of 5 ns. The second command causes the trailing transition to be programmed along with the leading transition. The next changes the single pulse width to 2 µs, and the final command command sets the leading (and thus both) transition to 200 ns. The oscilloscope display should now show a 2 µs wide single pulse with 200 ns transitions. Decouple the trailing transition from the leading transition as follows:

```
PULS:TRAN:TRA:AUTO OFF
PULS:TRAN:TRA 600E-9
```

The trailing transition should increase to 600 ns. Change from a single to a delayed pulse as follows:

```
PULS:DEL 2E-6
```

The pulse should now start 2 µs after the SYNC rather than coincident with the SYNC. Set up a double pulse as follows:

```
PULS:DOUB:DEL 4E-6
PULS:DOUB ON
```

The double pulse should appear much like the one in Figure 3-4. Note that the delay values for the delayed pulse and the double pulse are two independent parameters.

3.4.4.3 Output Levels

Leave the unit set up per the previous paragraph. Note that the default settings for output amplitudes of the pulse waveform result in levels of ±2.5 V into a 50Ω termination.

The output levels can be set up using the AMPLitude and OFFSet parameters, or by using the HIGH and LOW level parameters. Use HIGH and LOW together, or use AMPLitude and OFFSet together. These are "coupled" functions – setting up one pair causes the other pair to update to equivalent values.

Setting up the output is not as simple as many of the other parameters. Because the output amplifier is only capable of generating an output within a fixed "window" without limiting, there are interactions between the settings. This window is ±8V with the attenuator off and ±2V with the attenuator on.

When using the AMPLitude and OFFSet parameters, the sum of Vpk amplitude (half the programmed Vpp value) and the absolute value of the offset parameter cannot exceed 8V. Additionally, for pulses less than 0.5 Vpp, this restriction is reduced to 2 V.

When setting the output in terms of HIGH and LOW levels, the HIGH level must be at least 0.15 V more positive than the LOW level. HIGH and LOW levels are programmed within a ±8 V window, reduced to a ±2 V window when (upper – lower) is less than 0.5 V.

Set up the pulse waveform for negative supply ECL levels using AMPLitude and OFFSet parameters as follows:

```
VOLT 8E-1
VOLT:OFFS -1.3
```

Observe normal ECL levels on the oscilloscope waveform. The upper level should be –0.9V and the lower level should be –1.7V.

Set up the pulse waveform for CMOS levels using HIGH and LOW LEVel parameters as follows:

```
VOLT:HIGH 5
VOLT:LOW 0
```

The waveform should change to CMOS levels.

Note that the pulse waveform is "false" at the lower level and pulses "true" to the upper level. This is NORMal PULSe POLarity. Reverse the levels by programming the following:

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```
PULS:POL COMP (or INV)
```

Note the change in the waveform from positive to negative logic. This feature can be used to increase duty cycle to >95% by programming the complement of the desired waveform.

3.4.4.4 Pulse/Square Functions

Paragraph 3.4.4.2 demonstrates how to set up single, delayed and double pulses. These three waveforms are available under the default setting:

```
[SOUR:]FUNC[:SHAP] PULS
```

The Model 1391's default settings are designed to provide a "generic" starting point for common operations. Reset the unit (RESet or *RST) and then turn the PULSE and SYNC outputs back on (see paragraph 3.4.4). This is the single pulse. Observe a delayed pulse by sending:

```
PULS:DEL 100E-9
```

Observe a double pulse by sending:

```
PULS:DOUB ON
```

And finally, observe the SQUare function by sending:

```
FUNC SQU
```

The square has the same timing characteristics as a CLOCk SYNC, and its transitions and levels are settable like the PULSe waveforms. Additionally, the square's upper frequency is extended to 100 MHz.

3.4.5 Marker Operation

The pulse waveform Marker is the SYNC OUT waveform. The SYNC waveform can be set up as a pulse *period* marker, or as a non-continuous mode timing marker. The continuous mode default setting is as a period marker. This can be programmed as follows:

```
MARK:TYPE CLOC
```

For the non-continuous modes, GATE and BURSt, the marker type can be changed as follows:

```
MARK:TYPE GATE
```

The GATE SYNC will be described in paragraphs 3.4.9 and 3.4.10 and in the related figures.

3.4.6 SUMBUS Operation

SUMBUS operation requires the use of at least two Model 1391s or one 1391 and a VXIbus module supporting the SUMBUS. This discussion assumes two Model 1391s. The modules may be located anywhere in the VXIbus chassis (except slot 0).

Note that the scale factors (see Section 1) for outputting to the SUMBUS (5 mA/V) and inputting from the SUMBUS (0.2 V/mA) are reciprocals. This means that there is an end-to-end scale factor of 1 Vin/Vout for two Model 1391s.

NOTE

This simple 1 Vin/Vout scale factor applies to unattenuated amplitudes. Use 1 V/V if both the driving and the receiving units are unattenuated (both have their amplitudes ≥0.5 Vpp). This 1 V/V factor is also valid if both have their amplitudes set <0.5 Vpp. If the unit driving the SUMBUS is below and the receiving unit is above 0.5 Vpp, use a 0.25 Vin/Vout scale factor. If the unit driving the SUMBUS is above and the receiving unit is below 0.5 Vpp, use a 4 Vin/Vout scale factor.

Designate one of the units as the Driver. Its amplitude setting is Vin. Designate the other as the Receiver. Its amplitude setting is Vout. The Receiver unit will have its PULSE OUT and SYNC OUT connected to the oscilloscope as in Figure 3-4. First, set up the pulse waveforms of both units to match Figure 3-5, as follows:

Driver:

```
RES
OUTP ON;:MARK ON
PULS:PER 1E-3
PULS:WIDT 500E-6
PULS:DEL 200E-6
```

Receiver:

```
RES
OUTP ON;:MARK ON
PULS:PER 1E-3
PULS:WIDT 200E-6
PULS:DOUB ON
PULS:DOUB:DEL 600E-6
```

Now, set up the Driver as the Master and the Receiver as the Slave (Master/Slave Operation is explained in paragraph 3.4.11), as follows:

Driver:

```
TRIG:MODE MAST
OUTP:ECLTO ON
```

Receiver:

```
INIT:CONT OFF
TRIG:SOUR:ECLTO
```


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This slaves the Receiver's period to the Driver's. Finally, enable the SUMBUS, as follows:

Driver:

```
OUTP:SUMB ON
```

Receiver:

```
[SOUR:]SUMB ON
```

The oscilloscope waveform should look like the "RECEIVER W/SUMBUS" waveform in the figure. Note that the Driver and Receiver waveforms were at their default amplitudes of 5 Vpp. The summed waveform should be 10 Vpp because of the 1 V/V scale factor.

3.4.7 PAM Operation

PAM operation requires a Model 1391 and an external signal source to drive the PAM IN connector. Setting the Pulse Modulation (PULM) STATe ON enables signals at the PAM IN input to amplitude modulate the pulse level(s) around the value set by the programmed VOLTage setting. PAM is accomplished with four-quadrant multiplication of the 1391's pulse signal and the external PAM IN signal. Pulse Modulation has three sub-modes of operation. "POSitive AMPLitude" modulation causes the *lower level* to be fixed at the currently programmed OFFSet value and the median value upper level to be at its programmed value. The signal at PAM IN will amplitude modulate the instantaneous value of the upper level around this median value. The *envelope* of the modulated upper level will have the same shape as the external signal, limited by the >20 kHz bandwidth of the PAM input. The scale factor between the amplitude of the external signal and the amplitude of the modulation envelope is 2V of change in the output level per 1V of change in the external signal. This scale factor is reduced to 0.5 V of change in the output per 1V of change in the external signal when the programmed amplitude is set below 0.5 Vpp.

"NEGative AMPLitude" PAM is the mirror image of the POSitive case. The *upper level* is fixed at the currently programmed OFFSet value and the lower level is amplitude modulated. Note that the modulation envelope is also the mirror image of the external signal.

"BIPolar AMPLitude" modulation is essentially the sum of the POSitive and NEGative sub-modes.

The programmer/operator needs to be aware of two things when setting up PULseModulation. First, the output swing is limited to a window of ±8V (±2V for Vpp amplitudes less than 0.5 Vpp). Since the 1391's firmware has no knowledge of the external signal's amplitude and offset, the unit cannot issue an output stage clipping warning as it does with an AMPLitude/OFFSet setting conflict. Second, the multiplier can be overdriven resulting in overmodulation (including a polarity reversal of the pulses because of four-quadrant

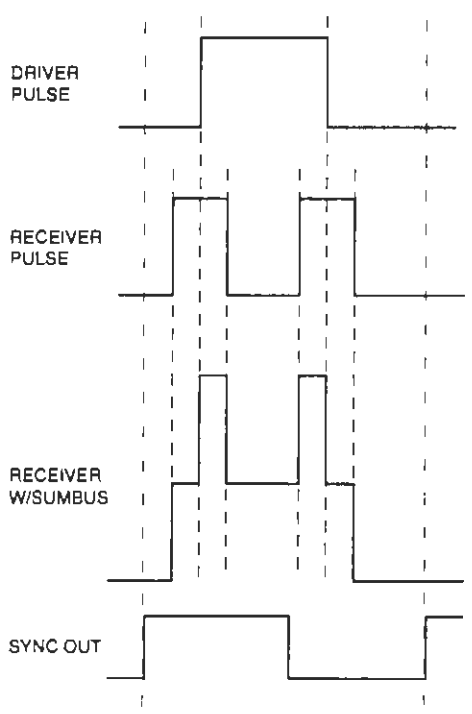


Figure 3-5 SUMBUS Waveforms

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operation). To avoid these problems, the desired PAM waveform should be designed using the following steps:

1) Sketch the desired PAM output waveform. From the sketch, select the required pulse characteristics (paragraph 3.4.4), PULM sub-mode, and the median pulse output level(s). Ensure that the required waveform can be produced within the 1391's output window capability.

2) Program the Model 1391 for pulse period, function, transitions, width and delay for the required pulse characteristics as discussed in the previous paragraphs. Turn on the pulse output.

3) Based on the PULM sub-mode selected from the sketch, set up the pulse upper and lower levels to the desired median level(s). Note that for POSitive or NEGative sub-modes, the programmed value of the level which is to be set to zero by the sub-mode is not important.

4) Enable the PAM IN and select a sub-mode, for example:

```
PULM ON
PULM:AMPL POS
```

   Verify the PULSE OUT waveform to ensure it matches the sketch.

5) Set up the external signal waveshape and amplitude. From the Vpp amplitude of the envelope in the sketch and the known scale factor, set the external signal's Vpp amplitude. Connect the external signal to the PAM IN connector. The ≥1 kΩ input impedance should not reduce the signal amplitude unless its source impedance is very high.

6) Compare the result to the sketch and fine adjust the external signal as necessary. In general, the oscilloscope should be synchronized to the lowest frequency component in the waveform, the external signal.

3.4.8 Triggered Operation

In the triggered mode, the Model 1391's output remains quiescent until triggered by the trigger source. All Model 1391 functions may be triggered. When triggered, the Model 1391 produces one complete waveform period, then returns to the quiescent state. The quiescent state for POSitive POLarity is the lower level. The quiescent state for NEGative POLarity is the upper level. The unit may be triggered by using

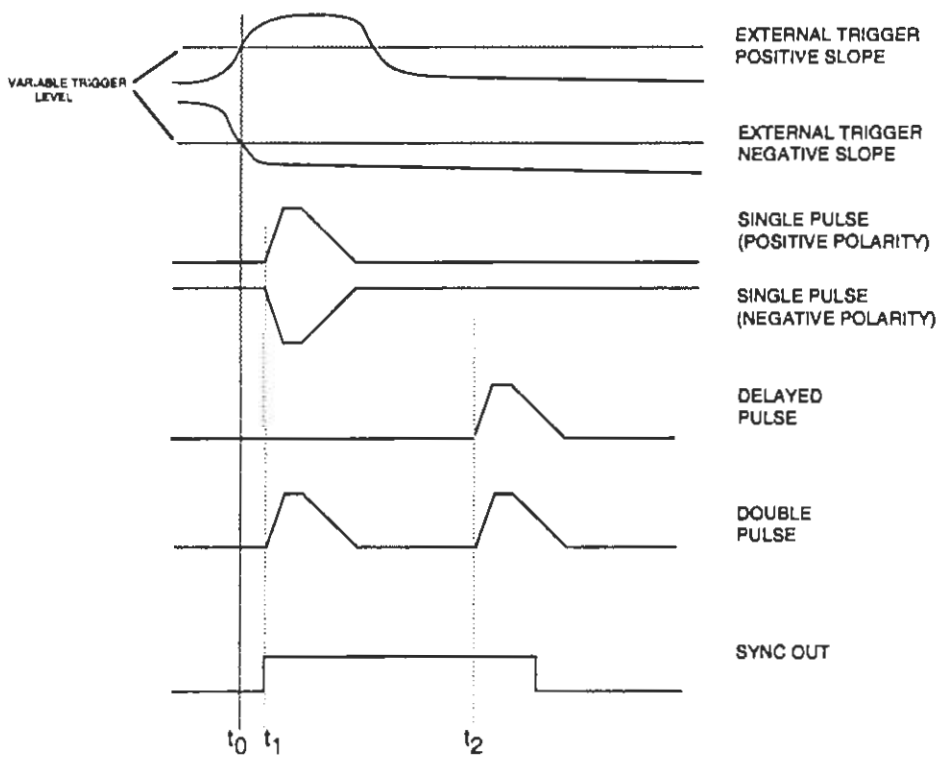


Figure 3-6. Triggered Waveform Characteristics

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the internal trigger TIMer, the external TRIG IN, the trigger command, or the VXI trigger bus input.

To set the Model 1391 for the triggered mode, follow the instructions in paragraph 3.4.4, then change the mode to triggered by sending:

```
INIT:CONT OFF
```

The default settings select triggered modes rather than one of the other non-continuous modes. These default settings are:

```
TRIG:GATE OFF
TRIG:COUN 1
```

In order to properly trigger the 1391, the TRIGger SOURce, MODE, TIMer, SLOPe and LEVel may also need to be set up.

3.4.8.1 Level and Slope Parameters

The TRIger LEVel and SLOPe parameters are used to tailor the response of the trigger input comparator to external triggering signals applied to the TRIG IN connector. This is only applicable when the triggering SOURce is selected as EXTernal. The LEVel should be set to a voltage level which corresponds to a point on the external signal where the dV/dt value of the signal's transitions is maximum. This minimizes triggering uncertainty (jitter). The SLOPe selection determines whether the 1391 is triggered on a positive-going or a negative-going transition through the selected voltage level. See Figure 3-6.

3.4.8.2 External Trigger Input

First set up the desired pulse characteristics per paragraph 3.4.4. Each trigger input will initiate one pulse period with these selected characteristics. Then determine the level and slope requirements (see the previous paragraph) for the external signal to be applied to the TRIG IN connector, and program the unit for triggered mode, external source. For example, for an external TTL triggering input:

```
RES
(PULSE CHARACTERISTICS)
TRIG:SLOP POS;LEV 1;SOUR EXT
INIT:CONT OFF
```

The result will be one period of the selected pulse waveform each time the external TTL signal makes a low-to-high transition. Note that the period of the external signal must be greater than the pulse period. Figure 3-6 illustrates triggering of each of the pulse functions. The SQUare may also be triggered, with timing coincident with the SYNC.

The pulse waveform could be complemented by sending the command:

```
PULS:POL COMP
```

Referring to Figure 3-6, the time t_0 is shown to be the point where the selected external signal transition, positive-going or negative-going, crosses the programmed trigger level voltage. The time t_1 is the 50% point of the rising edge of the SYNC OUT (MARKer:TYPE CLOCk). The time t_2 is the 0% point on the leading edge of a delayed pulse. The time $(t_1 - t_0)$ is a fixed eircuit delay between the triggering event and the start of a waveform period. Both the syne output (50% point) and the non-delayed pulse (0% point) occur at t_1, regardless of the operating mode. The time $(t_2 - t_1)$ is the programmable DELay parameter.

3.4.8.3 Internal Trigger

The trigger slope and level parameters have no effect on an internal trigger source. To trigger the generator internally, set up the internal trigger TIMer to a value greater than the pulse period. Using the previous example as a starting point, select the internal triggering source and program the TIMer as follows:

```
TRIG:SOUR INT;TIM <value>
```

Where <value> is the desired triggering period. Triggered periods operate to 25 MHz in double pulse, 50 MHz in single or delayed pulse, and 100 MHz in square.

3.4.8.4 BUS Trigger Commands

To trigger the generator using the IEEE 488 bus (external host) or the VXIbus, set up the generator in a triggered mode as described above, then select the bus trigger command by sending:

```
TRIG:SOUR BUS
```

Trigger the generator by sending either the 488.2 *TRG or 488.1 GET command over the 488 bus, or the word serial `Trigger` over the VXIbus. The *TRG command is mandated to be recognized by the Commander and by the Model 1391. Thc GET command causes the Commander to send the VXIbus word Serial `Trigger` command to addressed devices which support `Trigger` and do not have their DIR bit cleared to 0 (seee VXIbus System Specification). Trigger level or slope do not apply when using the `BUS` as the trigger source, and the bus commands only have effect when the Model 1391 is in a triggered mode of operation and the selected trigger source is `BUS`.

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3.4.8.5 VXI TTL/ECL Trigger Bus Input

The Model 1391 may also be triggered from the VXIbus TTL or ECL trigger lines on the backplane. The signal must be placed on the bus from another source within the VXI chassis.

To use the trigger bus as a trigger source, first set up the Model 1391 per the previous examples. Next, select one of the eight TTL trigger lines by sending the message:

```
TRIG:SOUR TTLT<n>
```

Where <n> represents one of the eight TTL Trigger lines, 0 through 7. Alternatively, select one of the two ECL trigger lines by sending the message:

```
TRIG:SOUR ECLT<n>
```

Where <n> represents one of the two ECL Trigger lines, 0 or 1. The ECL trigger lines will have higher bandwidth and tighter timing coupling between modules. Note that a TTL trigger line has a maximum bandwidth of 12.5 MHz per the VXIbus specification.

The selected signal will trigger the Model 1391 on the leading edge. Trigger level or slope does not apply when using one of the TTL Trigger lines as the trigger source.

The Model 1391 also offers a special operation mode optimized for triggering a 1391 from a 1391 using the ECL trigger lines (see paragraph 3.4.11).

3.4.9 Gated Operation

The synchronous gated mode is identical to the triggered mode, except the output from the Model 1391 starts from the quiescent state, produces continuous pulse periods for the duration of the trigger signal, then returns to the quiescent state. All waveforms may be gated (see figure 3-7).

To view synchronous gated mode, set up the Model 1391 pulse characteristics per the previous examples, and set the unit up for trigger mode using an EXTernal SOURce at the TRIG IN input. To observe gate mode properly, set the oscilloscope to both display and sync to the external triggering signal on CH1, and to display the 1391 PULSE OUT on CH2. Then switch from triggered to gated mode:

```
TRIG:GATE ON
```

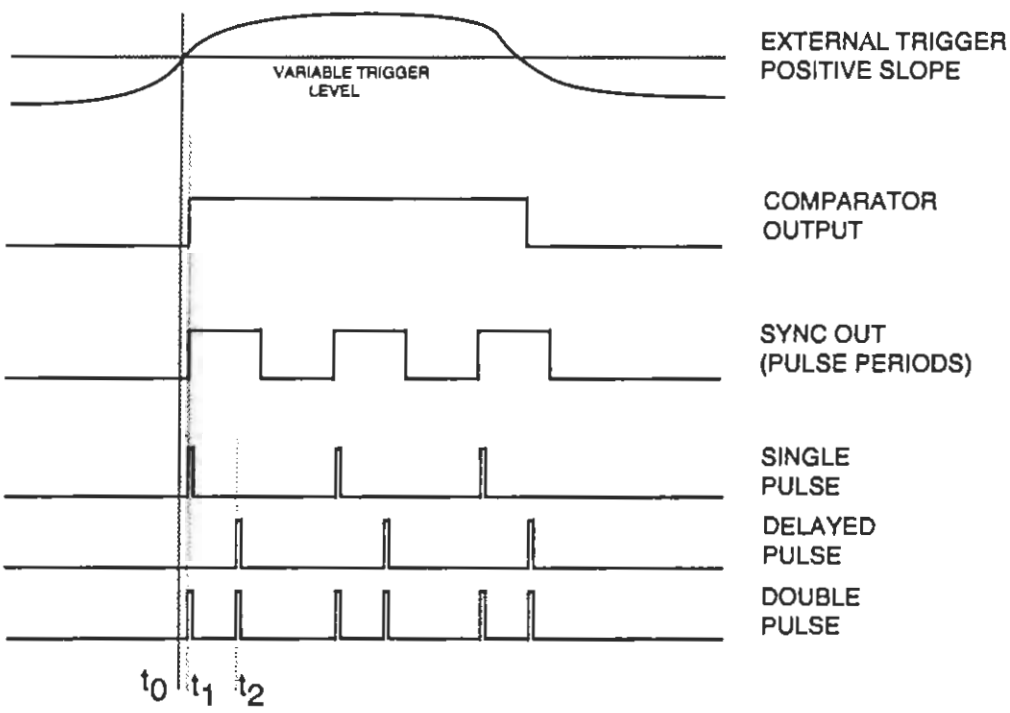


Figure 3-7. Synchronous Gate Waveform Characteristics

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The default setting is "synchronous" rather than "external width" gate mode, which can be programmed with the command:

```
TRIG:GATE:MODE SYNC
```

The SYNC OUT should appear as in Figure 3-7. Change the Sync waveform to be similar to the "COMPARATOR OUTPUT" waveform in the figure by sending:

```
MARK:TYPE GATE
```

Gate mode may also use various trigger sources. The unit may be triggered by the external TRIG IN as described above, the internal source as described in paragraph 3.4.8.3, or the VXI trigger bus input as described in paragraph 3.4.8.5. The BUS trigger commands as defined in paragraph 3.4.8.4 do not provide a trigger duration and are not valid in gated mode.

3.4.9.1 External Width Operation

In external width, the Model 1391 produces an output pulse whose period and width are determined by the selected triggering signal and the trigger level and slope settings, as shown in figure 3-8. To select external width, set up the 1391 in gated mode as described above and then send the command:

```
TRIG:GATE:MODE EXTW
```

Frequency or period commands are not required for external width. All other pulse characteristics are as described in paragraph 3.4.4. The external width accepts trigger inputs from all four trigger sources: external TRIG IN, internal trigger generator, VXI Trigger Bus, and the Trigger command. However, the most useful trigger source for external width is the external TRIG IN connector. This is because an externally defined signal is used and the trigger level and slope are adjustable as described in paragraph 3.4.8.1. To select the TRIG IN connector as the trigger source, send the command:

```
TRIG:SOUR EXT
```

To select the internal signal source (the frequency synthesizer) for the External Width function, send the following:

```
TRIG:TIM <value>;SOUR INT
```

The internal TIMer value is defined in paragraph 3.4.8.3. It is not recommended that this setup be used, since the identical result may be obtained by simply using a continuous square function.

A third trigger source for external width is the VXI backplane, described in paragraph 3.4.8.4. The period and width of the instrument output is dependent on the characteristics of the selected signal. A backplane signal is selected by programming one of the eight TTL trigger lines by sending the message:

```
TRIG:SOUR TTLT<n>
```

Where <n> represents one of the eight TTL Trigger lines, 0 through 7. Alternatively, select one of the two ECL trigger lines by sending the message:

```
TRIG:SOUR ECLT<n>
```

Where <n> represents one of the two ECL Trigger lines, 0 or 1. The ECL trigger lines will have higher bandwidth and tighter timing coupling between modules. Note that a TTL trigger line has a maximum bandwidth of 12.5 MHz per the VXIbus specification.

The remaining trigger source available to the Model 1391 in external width is the trigger command '*TRG',

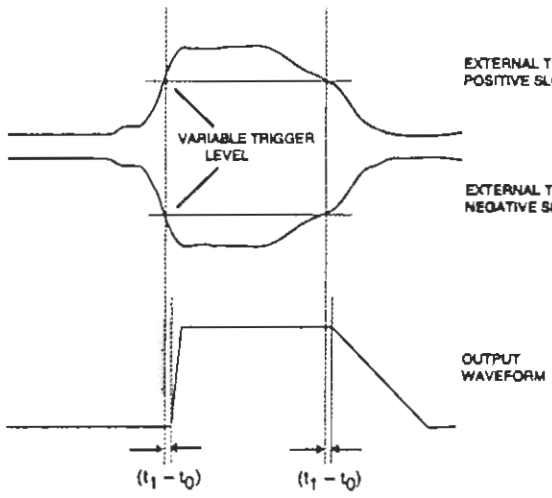


Figure 3-8. External Width Waveform Characteristics

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described in paragraph 3.4.8.3. When using the trigger command, the period and width of the output signal is determined by the *TRG bit. To select the trigger command, send:

```
TRIG:SOUR BUS
```

A pulse will be generated, whose width will be a function of the commander's *TRG write cycle time.

3.4.10 Burst Operation

The burst mode is identical to the triggered mode, except when a trigger is received, the Model 1391 leaves its quiescent state, produces a predefined number of pulse periods, then returns to its quiescent state. Burst waveforms (with COUNt set to "3") will be identical to the gate waveforms illustrated in Figure 3-7.

To observe the burst mode, set up the Model 1391 for triggered mode as described in paragraph 3.4.8, then send the burst mode command:

```
TRIG:COUN <n>
```

Where the value <n> is a number greater than 1 and up to 10 million. Numeric values are explained in paragraph 3.3.1.4. For burst count messages, numeric values may be in the form of an integer or floating point value, or one of the special case character keywords, 'MAXimum', 'MINimum', or 'DEFault'. Burst duration depends on the period or frequency programmed.

Both types of Sync waveform (see Gate Mode) are valid and programmable in Burst Mode.

A burst is initiated when the unit is triggered by the selected trigger source. The trigger source may be the external TRIG IN, as described in paragraph 3.4.8.2, the internal trigger source as defined in paragraph 3.4.8.3, the BUS trigger command as described in paragraph 3.4.8.4, or the VXI trigger bus input as described in paragraph 3.4.8.5.

3.4.11 Master/Slave Operation

Master/Slave triggering allows a VXIbus chassis with more than one Model 1391 module installed to operate as a multichannel pulse generator system. An ECL Trigger line is used to distribute the Master's trigger signal to the Slaves to ensure tight coupling. Additionally, signal timing is optimized to closely match the t_1 points (start of a pulse period, see Figure 3-7 and paragraph 3.4.8.2) of the Master module to an adjacent Slave module. Slave modules further away from the Master will have a backplane delay of approximately 0.5 ns per slot. Therefore, for best timing performance, the 1391 modules in the Master/Slave group should be adjacent to one another and the Master should be the one in the middle of the group.

The default setting for a 1391 module is "Slave", which allows it to be a Slave module in a Master/Slave group or an independent module. Once the Master module is chosen, send it the command:

```
TRIG:MODE MAST
```

There can only be one Master connected to a group of Slaves using one particular ECL Trigger line. Program the ECL Trigger line to be used by the group by sending the following command to the Master:

```
OUTP:ECLT<n> ON
```

Set up the Slaves to receive the Master's trigger on this particular ECL Trigger line by sending the following command to *each* Slave:

```
TRIG:SOUR:ECLT<n>
```

The Master is operated in continuous mode or a non-continuous mode with its trigger source set to anything other than the particular ECL Trigger line being used to trigger the Slaves. The Slaves must be set to a non-continuous mode with the trigger source set up as above. Each module, Master or Slave, can have all pulse characteristics (see paragraph 3.4.4) set up independently. The only restriction is that the master repetition period determined by the signal placed on the ECL Trigger line by the Master (essentially the signal that drives its SYNC OUT) is the longest period produced by any module. Each time a Slave is triggered by the Master, it must complete its output sequence, taking into consideration its period and COUNt value, and return to a quiescent state before the next Master trigger.

3.4.12 Status Commands

This subsystem contains the Status reporting registers. Neither the Operation, nor the Questionable registers are implemented in the Model 1391. All queries will return a "0" (zero). The Enable subcommands for each register will be accepted, but will not perform any function. Preset may be exercised, but will perform no function.

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4.1 INTRODUCTION

Figure 4-1 shows the Wavetek Model 1391 VXIbus Pulse Generator overall block diagram. The VXIbus connects to the module at backplane connectors P1 and P2, which supply the module with a digital interface, power supplies, trigger lines and a master clock. The module contains three printed circuit boards: the VXIbus Interface Board, pulse generator Main Board, and the pulse generator Amplifier Board. The VXIbus Interface Board contains the VXIbus P1 and P2 connectors and provides an interface between the VXIbus and the Pulse Generator Main Board. The Pulse Generator Main Board receives control signals and data from the interface and generates pulse waveforms. The Amplifier Board plugs into the Main Board and provides the high voltage, 50Ω source impedance pulse output signal to the PULSE OUT connector.

Under the direction of its VXIbus Commander (and more directly, the VXIbus Interface Board), the Wavetek Model 1391 Pulse Generator module produces pulse waveforms at the PULSE OUT BNC connector, and a TTL level pulse at the SYNC OUT BNC connector for pulse waveform synchronization. It also receives external triggering inputs at the TRIG IN BNC and external modulating signals at the PAM IN BNC.

The Model 1391 can also drive or receive triggering signals on the TTLTRIG or ECLTRIG lines on the VXIbus chassis backplane. This allows intermodule triggering and Master/Slave operation. In this manner, each Model 1391 module can be one channel in a multichannel pulse generator system.

The VXIbus chassis backplane also provides an analog SUMBUS, which is utilized by the Model 1391.

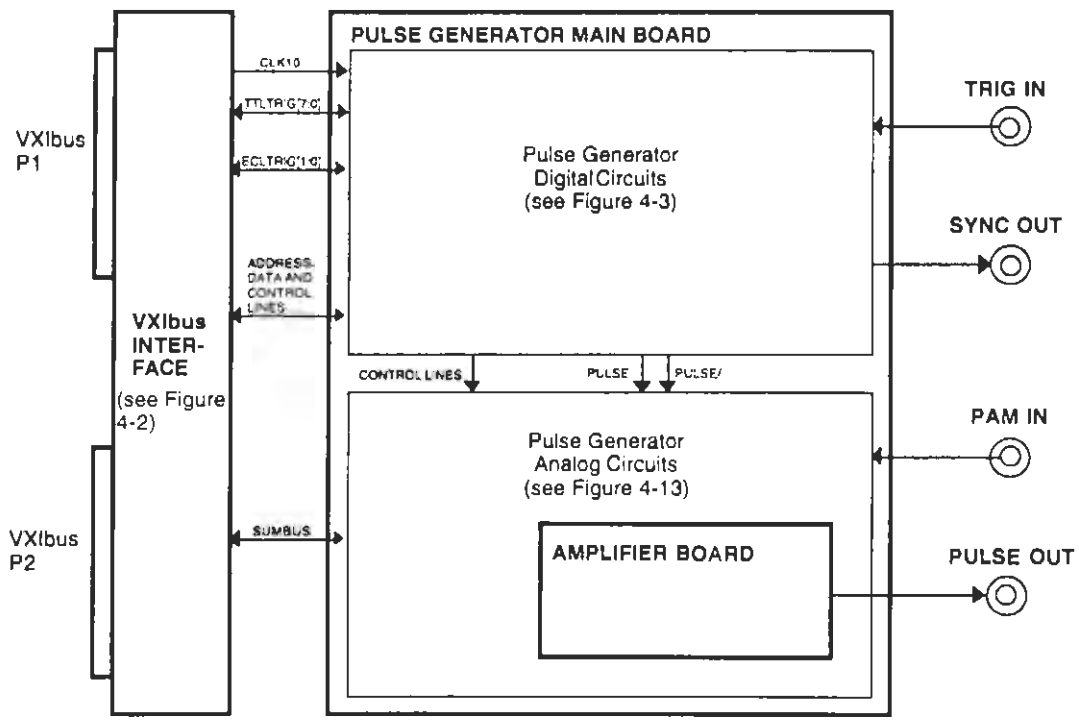


Figure 4-1. Model 1391 Pulse Generator Overall Block Diagram

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4.2 VXIBUS INTERFACE BOARD

All operating instructions and data for the Model 1391 module originate from its Commander, located within the VXI chassis. The VXIbus Interface Board, mounted within the Model 1391 module, transfers signals between the Pulse Generator and the VXIbus. An eight-position rocker switch, located on the interface board, determines the module's logical address.

Because of its high density, multilayer printed circuit card utilizing LSI and custom ASIC surface mount parts, the Interface Board is documented in this manual only as necessary to support factory repair. Maintenance information is provided to aid in fault isolation to the board level.

4.2.1 VXIbus Overview

A block diagram of the VXIBUS Interface Board is shown in figure 4-2. The VXIbus is contained in the chassis' backplane, and interconnects to the Model 1391 module P1 and P2 connectors. Refer to the VXIbus System Specifications for electrical specifications of the P1 and P2 connectors, the CLK10 line, the MODID line, the TTLTRG*/ECLTRIG* lines, and the TTLTRG*/ECLTRIG* protocols if detailed information is needed on the inputs to the VXI Interface Board.

The VXIbus System Specifications will also provide system architecture information that will be of help to understand the various tasks that the interface board performs. For Wavetek's implementation, the following sections should be understood: Device Overview, Message Based Devices, Message Based Device Communication Protocols, VXIbus and IEEE-488.2 Instrument Protocols, Shared Memory (present, but not used in the Model 1391), and Dynamic Configuration. The Wavetek VXIbus chip is an ASIC device which implements these protocols under direction of the interface 68HC000 CPU and system firmware.

4.2.2 Interface Board

The block diagram (figure 4-2) segments the Interface Board into a VXI INTERFACE block, a CPU & MEMORY block and an INSTRUMENT INTERFACE block. The VXI INTERFACE block contains the P1 and P2 connectors, the VXI ASIC device, the Shared Memory, module addressing, and various drivers and transceivers. The VXI ASIC device implements the complete VXIbus Message Based Device interface. It generates control signals that regulate the transfer of data between the interface CPU and the VXIbus. The VXIbus A16 registers are located within the ASIC. It also controls the RUN, FAIL, MODID, A16 and A24

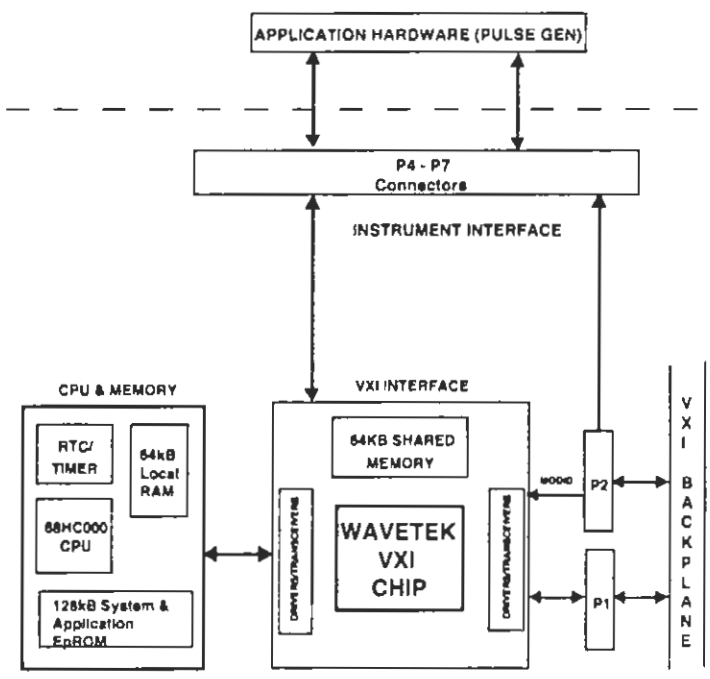


Figure 4-2. VXIbus Interface Board Block Diagram

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LEDs on the module's front panel. The VXIBUS interface contains 32K x 16 RAM as 64K bytes of A24/D16 Shared Memory which may be used to efficiently move large quantities of data. The Logical Address Switch and Bus Arbitration jumpers are explained in Section 2 of this manual.

The CPU & MEMORY block contains the microprocessor, local RAM and ROM, decoders, a real time clock/timer, an interrupt controller, a bus error timer and various drivers and transceivers. The local ROM consists of 128K of EPROM containing VXIbus System and Application (the Model 1391 Pulse Generator) code. There is also 64K bytes of local static RAM for variable data, stack and heap. The real-time clock provides timer and event capability. Up to seven interrupt inputs may be priority encoded; three from the application (not used in the 1391), three from the VXI ASIC, and one from the real time clock. The bus error timer generates a local BERR\ signal if data transfer acknowledgment (local DTACK\) is not given before time-out occurs. BERR\ is generated if a microprocessor access cycle exceeds 16 µs.

The INSTRUMENT INTERFACE block consists of connectors P4 through P7. The pin-outs and signal names of the interface between the VXI Interface Board and the Main Board are shown in sheet 1 of the Model 1391 Pulse Board schematic, 1104-00-3612, in Section 7 of this manual. These address, data, and control signals are described in paragraph 4.3.2 and are illustrated in figure 4-4.

4.3 PULSE GENERATOR BOARD – DIGITAL CIRCUITS

Refer to figures 4-1 and 4-3, other indicated figures, and the Main Board schematic 1104-00-3612 in Section 7 of this manual for the paragraphs under this heading. The Main Board is divided into "digital" and "analog" circuits, as indicated in figure 4-1. These paragraphs describe the theory of operation for the "digital" circuit blocks. Paragraphs under the 4.4 heading cover the "analog" circuit blocks of the Main Board and the Amplifier Board.

The interconnection of the digital circuits of the pulse generator is illustrated in figure 4-3. The main signal path is indicated by the heavier signal lines. This signal path is for normal operation in Continuous Mode. The signal path will be different for each mode. The following paragraphs give a quick overview of the purpose of each digital circuit block shown in figure 4-3. These descriptions will be followed by detailed circuit descriptions concentrating on each block.

Frequency Synthesizer

The synthesizer's output is a square wave with a programmable frequency range of 1mHz to 100 MHz. The synthesizer produces the basic timing signal for the continuous modes. The synthesizer also provides the internal trigger source for non-continuous modes. The synthesizer's output is routed to the SYNC output to provide clock outputs from 50 MHz to 100 MHz.

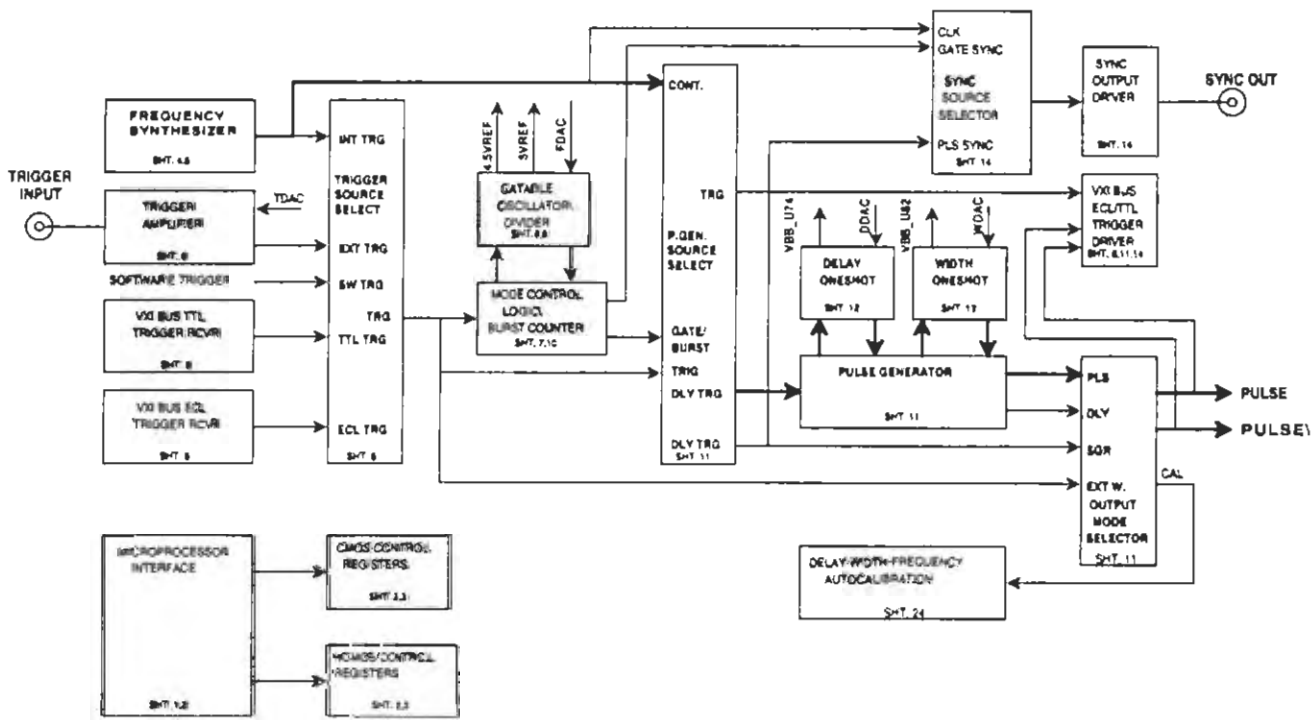


Figure 4-3. Pulse Generator Digital Circuits Block Diagram

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Trigger Amplifier

The trigger amplifier conditions the external triggering signal applied to the TRIG IN BNC connector. The trigger level is controlled by the TDAC signal from the analog section.

VXIbus TTL Trigger Receiver

The trigger receiver selects one of the eight VXIbus TTL Trigger Lines to trigger the Model 1391 when non-continuous modes are selected.

VXIbus ECL Trigger Receiver

The trigger receiver selects one of the two VXIbus ECL Trigger Lines to trigger the Model 1391 when non-continuous modes are selected.

Trigger Source Selector

The trigger source selector selects one of five triggering sources to trigger the Model 1391 when non-continuous modes are selected.

Mode Control Logic/Burst Counter

The mode control logic provides the gating signal to the gatable oscillator/divider upon receiving a trigger when gated or burst modes are selected. In gated mode, the oscillator runs for the duration of the triggering signal. When burst mode is selected, the gatable oscillator runs until the programmed number of cycles have been produced. The mode logic also provides an output GATE SYNC, routed to the sync output driver, coincident with the oscillator's gating signal.

Gatable Oscillator/Divider

The oscillator's output is a square wave with a programmable frequency range of 25 to 50 MHz when gated "on" by the mode control logic. The oscillator's frequency is controlled by the FDAC signal from the analog section. The oscillator also provides two reference voltages, 4.5VREF and 5VREF used by the analog section. The divider produces frequencies from 1mHZ to 50 MHz from the oscillator's output.

PGEN Source Selector

The source selector selects the pulse generator's triggering source. The selector produces three outputs, TRG, DLY TRG, and DLY TRG G, from the selected triggering source. The TRG output is the triggering source. This output can be routed to the VXIbus ECL Trigger Lines to drive other Model 1391's configured as slaves. The DLY TRG output is the triggering source delayed by about 20 ns. This output is routed to the sync output driver to produce a synchronizing output coincident with the pulse output. The DLY TRG G signal is a narrow glitch coincident with the leading edge of the DLY TRG signal. This signal clocks the pulse generator. The 20 ns delay between the TRG signal and the DLY TRG and DLY TRG G signals accounts for the time delays incurred driving and receiving the VXIbus ECL Trigger Lines so that master and slave Model 1391's are time synchronized.

Delay and Width One-Shots

The delay and width one-shots produce narrow output glitches at a programmed time delay after they are triggered. The one-shots have two sections; a coarse resolution digital section and a fine resolution analog section. The digital sections provide 10 ns steps, while the analog sections provide 100 ps steps. The analog delay sections are controlled by the DDAC and WDAC signals from the analog section. The VBB_U74 and VBB_U82 signals are used to generate the control voltages.

Pulse Generator

The pulse generator circuitry routes the DLY TRG G signal to the delay and width one-shots. The delay one-shot is always triggered by the DLY TRG G signal. The delay one-shot's output triggers the width one-shot. The signal routing for normal and delayed pulses are the same. A normal pulse is a delayed pulse with zero programmed delay. When the width one-shot is triggered, a flip-flop is set. The flip-flop is reset by the width one-shot's output. The flip-flop's output is a pulse whose width is determined by the width one-shot's programmed time delay.

When double pulses are selected, the DLY TRG G signal triggers both the width and delay one-shots. The width one-shot is immediately triggered, producing a pulse, and then triggered by the delay one-shot, producing a second pulse. When the delay one-shot is triggered, a second flip-flop is set. The output of the delay one-shot resets the flip-flop. This flip-flop produces a pulse whose width is equal to the programmed delay. This pulse, DLY, is used to calibrate the delay one-shot.

Output Mode Selector

The output mode selector selects the signals to drive the differential ECL signals PULSE and PULSE\. These signals drive the analog section, the VXIbus ECL/TTL trigger lines, and the autocalibration circuitry. For normal, delayed, and double pulses, the pulse generator's output is selected. For square wave outputs, the DLY TRG signal is selected. The TRG signal is selected for external width mode. The DLY signal is selected during an autocalibration of pulse delay. The CAL signal is a TTL version of the PULSE and PULSE\ signals.

Sync Source Selector

The sync source selector selects one of three signals to drive the sync output driver. The selector also has several programmable time delays to account for the Model 1391's many operating modes.

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Two types of sync are available from the Model 1391; *pulse sync* is coincident with the rising edge of the pulse output, *gate sync* is high when bursts of pulses are generated or the pulse generator is gated.

When square waves over 50 MHz are programmed, the frequency synthesizer's output is routed to the sync driver.

Sync Output Driver

The sync output driver level shifts the sync source selector's ECL output to drive TTL levels into a 50Ω load.

VXIbus ECL/TTL Trigger Driver

The trigger driver routes the PULSE or the TRG signal to any one of the eight VXIbus TTL trigger lines. The PULSE and TRG signals can also be routed to either of the two VXIbus ECL trigger lines as well.

Delay - Width - Frequency Autocalibration

The autocalibration circuitry is used to characterize the gated oscillator frequeney and the delay and width one-shots digital section's periods.

Microprocessor Interface

The interface allows the microprocessor's parallel data bus to talk to the serial data CMOS and NCMOS control registers.

CMOS and NCMOS Control Registers

The registers control the analog and digital sections of the Model 1391. The CMOS control registers have 0 to +5 volt output levels, and control analog section and the VXIbus TTL trigger driver and receiver sections. The NCMOS control registers have -5.2 to -0.6 volts output levels that are compatible with the ECL logic used throughout the Model 1391.

4.3.1 Interconnect and Power Distribution

Sheet 1 of the Model 1391 Pulse Board schematic shows all of the connections between the pulse generator and the VXIbus Interface Board. All power supplies and instrument control originates from the VXI Interface Board. Coded lines are identified as follows: 'A' for address; 'D' for data, 'L' for a VXIbus Interface Board origin, and 'B' for a buffered line. Each front panel LED is independently enabled (logic low) or disabled (logic high) by the VXIBUS Interface Board through control lines VA16 LD\, MID_LD\, FAIL_LD\ and RUN_LD\.

4.3.2 Digital Interface and Data Registers

Refer to figure 4-4 and Pulse Board schematic sheets 2 and 3. Three types of digital control signals direct the Model 1391 operations: dynamic control, strobed control, and static control. Dynamic control lines originate from programmable logic devices U2 and U3. These lines are synchronized to Interface Board microprocessor system timing and are controlled by LR/W (Read/Write) and LUDS\ (data strobe) to insure proper timing. LUDS\ is enabled after the 16 data bus lines have stabilized following a data change. Address lines (LA[01:05 and 14:20]) are always controlled by the Interface Board microprocessor. Parallel Data lines (LD[00:15]) are bidirectional between the Interface and Pulse Boards. Parallel Data is restricted to the devices on sheet 24 of the Pulse Board schematic. The Pulse Board data interface on sheets 2 and 3 of the schematic uses serial data on the bidirectional LD00 data line.

U2 acknowledges successful data transfer between the Pulse Board and VXIbus Interface Board (DTACK\). Absence of this important signal results in a Bus Error (BERR\) at the Interface microprocessor. U2 also generates three strobes for the data register decoders. REGSA strobes U1, REGSB strobes U8, and REGSC strobes U9. U1, U8, and U9 generate all of the strobed control signals. The RLYEN\ dynamic control signal generated by U2 determines when the attenuator relays can be energized (sheets 21 and 22 of the Pulse Board schematic). U2 also generates the DAC1_LD and DAC2_LD dynamic control signals which load data to the DACs on sheet 15 of the schematic.

U3 buffers the bidirectional LD00 serial data line as LDATA00, which is the source of data to all of the serial data registers, which produce all of the static control lines for the pulse generator circuitry. U3 controls the reading and writing of serial data to and from U4, the serial Calibration Data Memory. U4 is a 4096 bit EEPROM, organized as 256 sixteen bit words. CS_SMEM\ and SMEM_CLK are dynamic controls lines to U4, LDATA00 is the input data, and SMEMDOUT is the output data. This allows the microprocessor to read from and write to the Calibration Data Memory, U4, using U3 and LD00. CS_ADC\ and CS_901\ are dynamic control signals used to select the ADC (U109, Analog-to-Digital Converter) and the Counter/Timer (U112) on sheet 24 of the schematic. ADC_SCLK is the ADC clock.

When both REGSA (from U2) and LUDS\ (from the VXIbus Interface Board) are low, three to eight-line decoder U1 briefly enables (pulses low) one of eight control lines (Y0 through Y7), as determined by the status of address lines LA[14:16]. Four of these eight strobed control lines operate the three serial data registers U7, U11, and U15, which produce the static control lines for the pulse generator circuits that operate at normal TTL or CMOS levels. S_CLK\ clocks all serial data. R_EN1\, R_EN3\, and R_EN2\ strobe registers U7, U11, and U15. U7 controls the output attenuator relays (sheet 21) and the frequency refer-

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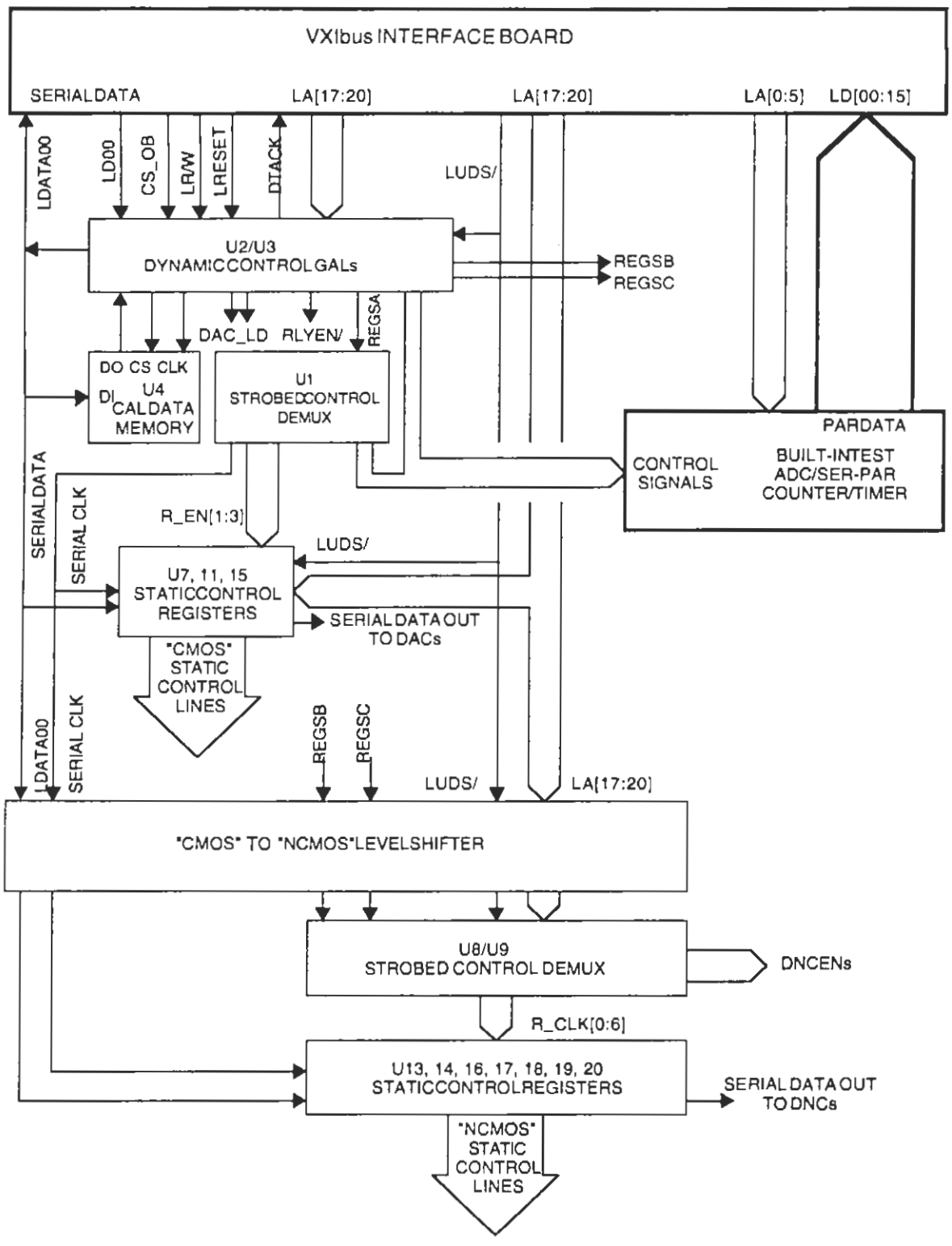


Figure 4-4. Digital Interface and Data Registers

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ence (sheet 24). U11 controls transition time range selection (TR1\, TR2\, TR3\ lines to sheet 19 and the LE<10NS and TE<10NS lines to sheet 17) and PAM enable and modes (PAMEN\, NPSEL\, and PPSEL\ lines to sheet 16). The serial data outputs of U7 and U11 are also used to supply data for the quad DACs, U87 and U89 on sheet 15. R_EN3\ is sent to enable serial data register U15 (sheet 3), which controls the selection of TTLTRIG* outputs to and inputs from the VXIbus backplane (sheet 6).

The remaining U1 generated signals control the ADC (U109, U110, and U11 on sheet 24) and the BUS trigger. SWTRIG\ is the software generated trigger signal. ADCL_EN\, ADCL_CLK\, and ADCR_CLK\ select and enable serial data registers U110 and U111. The serial data output of U109 connects to the serial data input of U110, cascading them to transform the serial ADC data into 16 bit words [LD00:16] for the microprocessor.

U5 and U6, level shifters, translate the normal CMOS levels of the LA[14:16], REGSB, REGSC, LUDS\, LDATA00, S_CLK\, and LRESET\ signal lines to NCMOS. These signals, now with a "T" prefix, control the data decoders, U8 and U9. These decoders operate as described for U1, except that their outputs (strobed control lines) are at NCMOS levels.

TDATA00, TS_CLK\, and TRESET\, buffered by U10, are sent as inputs to the NCMOS data registers (U13 through U20, except U15, on sheet 3).

U8 generates the strobes, R_CLK[0:6]\, for the NCMOS data registers. U9's outputs, buffered by U12, are sent as strobed control signals to various pulse generator circuits. DDNCEN and WDNCEN are sent to the Delay and the Width one-shots (sheets 12 and 13) to enable the DNC2016 counters. Likewise, CDNCEN, SDNCEN, and BDNCEN are sent to DNC2016 enable pins in the clock divider (sheet 9), frequency divider (sheet 5), and the burst counter (sheet 10). PLLEN enables the single-chip PLL, U21, on sheet 4. BRSTCNT (buffered reset to counters) initializes and clears the Mode Control logic (sheet 7), the Burst Counter (sheet 10), the Pulse Generator (sheet 11), the Delay one-shot (sheet 12), and the Width one-shot (sheet 13).

The NCMOS data registers, strobed by U8, are on sheet 3 of the Pulse Board schematic. These are U13 through U20, excluding U15. NCMOS levels are created by running CMOS devices with –5.2 volts at their ground pins and –0.6 volts (a diode drop from ground) at their supply pins. The resulting NCMOS logic levels can be used as static control lines to ECL logic without further logic level translation.

4.8.3 Frequency Synthesizer

The frequency synthesizer consists of two sections; a phase locked loop (Pulse Board schematic, sheet 4) and a frequency divider\selector (sheet 5). The phase locked loop produces an ECL level square wave between 50 and 100 MHz with 10 kHz resolution. A basic phase locked loop consists of a phase comparator, a loop filter, a VCO, and a programmable (÷ N) counter. The phase comparator drives the VCO via the loop filter until the ÷ N counter's output is the same frequency and phase as the reference frequency. For output frequencies between 50.01 and 100.00 MHz, "N" ranges between 5001 and 10000, with a reference frequency (1 LSB step) of 10 kHz. The loop filter determines the loop dynamics as well as suppresses reference frequency sidebands. The Model 1391 employs a slightly different loop, called Dual Modulus prescaling. This technique produces an additional digit of resolution at the same time as it scales down the 100 MHz VCO frequency to a value that the ÷ N counter can manage. A simplified dual modulus phase locked loop is shown in figure 4-5. The VCO's output is applied to the dual modulus prescaler. The prescaler divides F_{out} by "P" or "(P+1)" under control of the MC signal. The prescaler's output drives two low speed counters; ÷ A and ÷ N. The ÷ A counter controls the prescaler's division ratio.

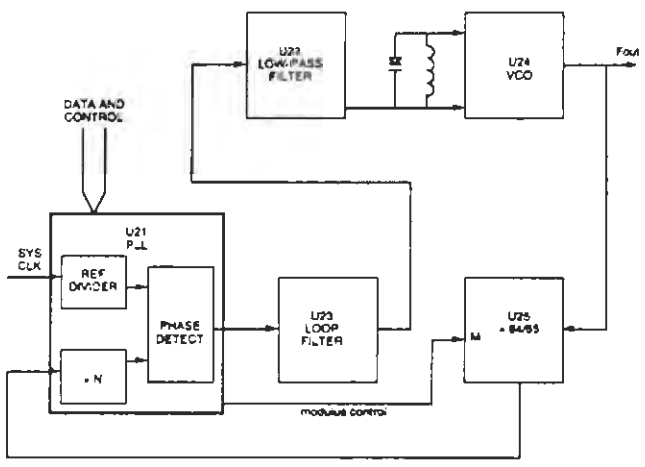


Figure 4-5. Dual Modulus PLL

The counter system operates as follows. The overall division ratio, N total, is factored into two parts; "A" and "N". Values for A and N are calculated from the equation: $N_{total} = (N*P)+A$. The counter system divides F_{out} by the value "(P+1)" A times and then divides F_{out} by the value "P" (N-A) times. In the Model

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1391, "P" equals 64. For example, to produce a 100.00 MHz output, N_{total} = 10000. Therefore A = 16 and N = 156 (10000 = 16 * 65 + 140 * 64).

Refer to the schematic, sheet 2. The phase locked loop's reference is provided by the 10 MHz VXIbus CLK10 signals, BCLK10+ and BCLK10–. U29 buffers the reference and drives U21's reference input. U21 contains a reference divider programmed to divide by 1000 to provide the 10 kHz reference for the phase locked loop. U21 also contains the divide by A and N counters along with the phase comparator. U21's dividers are programmed serially by the microprocessor. Serial data, PLLDATA, is clocked into U21 by the S_CLKA\ signal. The data latches into U21 by the PLLEN line. The phase detector's output is applied to the loop filter comprised of U23 and its associated components. The phase detector's output contains 10 kHz reference frequency components that would modulate the VCO's output. The sideband suppression filter, comprised of U22 and its associated components filter out the reference frequency components. The R-C filter, R14-C23, provide additional high frequency filtering. U24 and its associated components form the VCO. The VCO's frequency is determined by the LC tank circuit comprised of L1 and varactor diodes CR14 through CR17. As the voltage on the varactor diodes cathodes rises, the diodes capacitance decreases, increasing the VCO's frequency. CR13, CR18, and R15 limit the range of the VCO's control voltage to ensure start-up when power is applied. U24's 50.01 to 100.00 MHz output is buffered by U30. U25 divides the buffered VCO output by 64 or 65 as selected by U21's MC output. The phase locked loop is powered by isolated supplies provided by U26 thru U28. The VCO's 50.01 to 100.00 MHz output is successively divided by two providing the lower output frequencies. The buffered VCO output is applied to multiplexer U33 and to the divide-by-two stage U32\A. U32\A's output drives the multiplexer, U33, and the second divide-by-two stage U32\B. U32\B's output drives the multiplexer and the ECL to NTTL translator comprised of Q2, Q3, R23, and R24. The translated 12.5 to 25 MHz signal drives programmable divider U31. Serial data, SDNCDATA, is clocked into U31 by the S_CLKA\ signal. The data is latched into U31 by the SDNCEN signal. U31's NCMOS level output is level shifted by CR19 and R22 to ECL levels and applied to the multiplexer, U33. U33's output provides an ECL level square wave, ranging from 500 uHz to 100 MHz. When frequencies between 50 and 100 MHz are programmed, dividers U32\A and B are disabled by the VCO/2_OF and VCO/4_OF signals to remove sub-harmonic jitter caused by coupling within the ECL logic devices. Divider, U32\B is disabled when frequencies between 25 and 50 MHz are programmed. U33's output, buffered by one section of U30, produces the SYNTH signal, which is again buffered by U36/B producing the BSYNTH signal.

4.8.4 Trigger Amplifier

The external triggering signal is compared to the triggering level signal by high speed comparator, U34; see schematic 1104-00-3612 sheet 6. The output of the trigger level DAC, TDAC, swings between 0 volts and 4.5 volts. An offsetting current is added via R27 and R28 to allow setting the triggering level down to -10 volts. The input of U34 is restrained to about ±0.6 volts by CR20 and CR21 to preserve speed. Positive feedback around U34, provided by R29 and R30, produces about 40 mV of hysteresis. One section of U36 buffers U34's output.

4.8.5 VXIbus TTL Trigger Receiver

Data selector U38 selects one of eight VXIbus TTL trigger lines to drive TTL to ECL translator U35; see schematic 1104-00-3612 sheet 6. The desired trigger input is selected via the IN_TTLTRGA, IN_TTLTRGB, and IN_TTLTRGC signals.

4.8.6 VXIbus ECL Trigger Receiver

The differential ECL trigger signals, ETRGIN0+, ETRGIN0-, ETRGIN1+, and ETRGIN1-, are buffered by two sections of U29; see schematic 1104-00-3612 sheet 6.

4.8.7 Trigger Source Selector

Data selector U37, controlled by the TRG_SRCA, TRG_SRCB, and TRG_SRCC signals, selects the unit's triggering source; see schematic 1104-00-3612 sheet 6. The TTL level software triggering signal, SWTRG\ signal is translated to ECL levels by one section of U35 to drive U37. U37's output inverted by exclusive-OR gate U41 provides trigger slope selection. The SLP_CMP signal selects the slope.

4.8.8 Mode Control Logic\Burst Counter

The mode control logic controls the operation of the 25 to 50 MHz gatable oscillator; see schematic 1104-00-3612 sheets 7 and 10. When the gated mode is selected, the gatable oscillator runs for the duration of the external triggering signal, and always produces an integer number of cycles. When burst mode is selected, the gatable oscillator runs until the programmed number of cycles have been produced. Simplified mode control logic for the gated mode is shown in figure 4-6. When the triggering signal goes high, flip-flop U46\A, is set driving its Q\ output low, starting the gatable oscillator. The triggering signal also clears flip-flop U46\B, holding its Q output low. When the triggering signal returns low, the DIV_CLK\ signal from the gatable oscillator clocks U46\B's Q output

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high, which clocks a low into U46\A stopping the gatable oscillator. The RES_CLK signal, produced by U46\B, resets the gatable oscillator to a known state, ready for its next operating cycle. Figure 4-7 shows the mode control logic configured for burst mode. The glitcher produces a narrow ~5ns wide pulse on the leading edge of the triggering signal. The glitcher sets flip-flop U46\A starting the gated oscillator. The glitcher's output also arms the burst counter. The burst counter counts the gated oscillator's output, DIV_CLK, driving the B_END signal high after the programmed burst count has been reached. Flip-flop U46\B's Q output is then clocked high which clocks U46\A stopping the gatable oscillator. The RES_CLK signal, produced by U46\B, resets the gatable oscillator to a known state, ready for its next operating cycle.

The glitcher circuit, as shown on the schematic diagrams, comprised of U43 sections A and B along with R31 and C32 produce a narrow pulse coincident with the leading edge of the TRIG signal. U43 section C along with U44 sections A and B form a multiplexer that routes the glitcher output or the TRIG signal to the D input of U46\A under control of the G_MODE\, B_MODE\, and OSCONOFF signals. U45\A applies the B_END signal or a logic high to the D input of flip-flop U46\B under control of the B_MODE\ signal. The burst counter is a high speed counter that counts down from its programmed count to zero after it has been armed by the B_START signal, producing the B_END signal. The burst counter is comprised of two sections, a short count high speed ECL section, and a long count low speed NCMOS section. Flip-flop U58 sections A and B along with gates U57 A thru D form a two bit Johnson counter, clocked from the gatable oscillator's output DIV_CLK. NOR gates U57 preset the Johnson counter to any one of its four states when flip-flop U59\B is cleared by the B_START signal. The states are selected by the BH14\, BH23\, BH12\, and BH34\ signals.

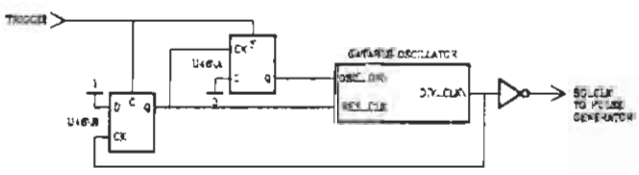


Figure 4-6. Model Control Logic - Gated

The Johnson counter's output, translated to NTTL levels by Q16, Q17, R51, and R52, clocks the programmable CMOS counter U60. The Johnson counter divides the 50 MHz maximum frequency DIV_CLK signal by four, producing a 12.5 MHz maximum clock compatible with U60. U59\B's output is translated to NTTL levels by Q18, Q19, R53, and R54 to load the programmed count into U60. When U60 counts down to zero, its CYDA output goes high. CR25 and R55 level shift the CYDA output to ECL compatible levels to drive the D input of U59/B high. The high level is clocked thru U59\B producing the B_END signal, and reloading programmable counter U60. Serial data, BDNCDATA, is clocked into U60 by the S_CLKB\ signal. The serial data is latched into U60 by the BDNCEN signal.

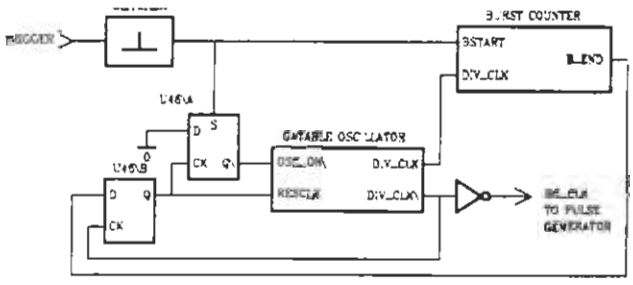


Figure 4-7. Mode Control Logic - Burst

4.3.8 Gatable Oscillator / Divider

When gated, the gatable oscillator (schematic 1104-00-3612 sheets 8 and 9) produces a 25 to 50 MHz square wave output by charging and discharging a timing capacitor with a constant current. The frequency of oscillation is controlled by varying the charging / discharging current. The magnitude of the current is controlled by the FDAC signal. A simplified gatable oscillator is shown in figure 4-8. The timing capacitor is always charged with a current of +I. A current of -2I is switched in to discharge the timing capacitor. When the oscillator is disabled, the timing node is biased to maintain the first oscillator period the same length as the following oscillator periods.

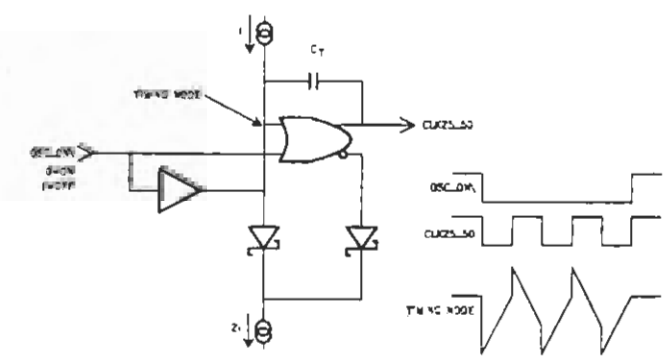


Figure 4-8. Gatable Oscillator

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Voltage divider, R35 - R37, divides the 0 to 4.5 volt FDAC signal down to 0 to about 3.5 volts. U48/B and Q5 force the voltage on the bottom of R38 equal to the divided down FDAC signal; refer to schematic 1104-00-3612 sheets 8 and 9. U47 provides a precise 10 volts reference voltage to the voltage divider formed by R32 thru R34. The voltage divider produces reference outputs of about 4.5 volts and 5 volts that are used throughout the Model 1391. U48/A and Q4 force the top of R38 to +5 volts. As the FDAC signal swings between 0 and 4.5 volts, the voltage across R38 swings between 5 and 1.5 volts, producing a current of 2.11 mA to 0.55 mA thru RN19/D, Q4, R38, Q5, and RN19/C. The end result is variable voltages referenced to the ±12 volts power supply rails. The voltages drive two complementary current sources, U49 - Q6, and U50 - Q9. U49 and Q6 force the variable voltage to appear across RN19/E, producing a collector current of 2.11 to 0.55 mA in Q6. U50 and Q9 operate in a similar manner. Q9's collector current swings between 1.1 and 4.22 mA as RN19 sections A and B are in parallel. The discharging current is switched into the timing capacitor, C36 by diode switch CR22 - CR23. When the oscillator is disabled, an amplifier comprised of Q10 - Q11 and their associated components biases the timing node so that the oscillator's first period is the same length as the following periods. R42 provides adjustment of the first period. Current source Q7 - R40 biases emitter follower Q11 with a current equal to the discharging current to compensate for Q10's Vbe shift with current. The frequency of the oscillator is dependent on the value of the timing capacitor, the charging current, and the threshold voltage of U51. The oscillation frequency versus control voltage is also slightly non-linear. To account for these errors, the frequency autocalibration system measures the oscillator's output frequency at several programmed values and applies a correction factor to the FDAC signal.

The gated oscillator's 25 to 50 MHz output is successively divided by two to obtain lower frequencies. Refer to figure 4-9 for a simplified diagram of the divider. The gated oscillator's output is applied to a divide by 2 stage and to one input of a multiplexer.

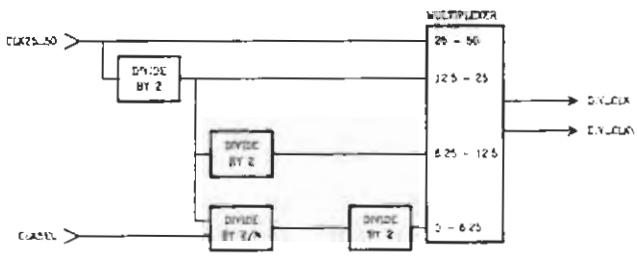


Figure 4-9. Divider

The divide by two stages output drives another input of the multiplexer, a second divide by two stage and a 2/N stage. The 2/N stage output is divided by 2 before being applied to the multiplexer.

The multiplexer's output is a square wave from 1mHz to 50 MHz, refer again to the schematic diagrams. Three sections of U53 add time delay to the CLK25_50 signal to match the delays of the other divider paths before driving the multiplexer U55 to provide the 25 to 50 MHz frequency range. The CLK25_50 signal is divided by 2 by U52/B. U53 adds time delay before driving the multiplexer U55 to provide the 12.5 to 25 MHz frequency range. The RNG2_OFF signal disables U52/B when frequencies between 25 and 50 MHz are programmed to remove sub-harmonic jitter caused by coupling within the ECL logic devices. The RES_CLK signal sets flip-flop U52/B to a known state. U115/A, configured as a divide by 2 stage further divides U52/B's output providing the 6.25 to 12.5 MHz frequency range. Flip-flop U52/A is configured as a divide by two when the CLK_SEL signal is low which routes U52/A's Q\ output to its D input via one section of U51 and U54. The RES_CLK signal sets flip-flop U52/A to a known state. When the CLK_SEL signal is high, programmable divider U56 is included in the feedback loop to the D input of U52/A. U52/A's output is translated to NTTL levels by Q12, Q13, R46, and R47 to drive the load input of U56. The 12.5 to 25 MHz output of U52/B, buffered by U45, is translated to NTTL levels by Q14, Q15, R48, and R49 to clock U56. CR24 and R50 translate U56's NCMOS level output to ECL levels. The programmable divider operates as follows. The RES_CLK signal sets U52/A's Q output low which loads the down counter U56. U56's CYDA output is low which is inverted by U54 providing a high to the D input of U52/A. When U52/A is clocked, its Q output goes high allowing U56 to count down from its programmed value. When U56 counts down to zero, its CYDA output goes high placing a low on U52/A's D input. The next clock reloads the down counter U56 and the cycle is repeated. U52/A's unsymmetrical output is turned into a square wave by divide by two stage U115/B. The RES_CLK signal sets flip-flop U115/B's output to a known state. The divide by N stage is configured as described above so that the placement of the leading edge of the divided output is accurately defined. Serial data, CDNCDATA, is clocked into U56 by the S_CLKB\ signal. The serial data is latched into U56 by the CDNCEN signal.

4.3.10 PGEN Source Selector

Multiplexer U61 selects one of three triggering sources (schematic 1104-00-3612 sheet 11). The BSYNTH signal is selected by the C_MODE\ signal for the con-

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tinuous mode. The TRIG signal is selected via the T_MODE\ signal for the triggered mode. The BG_MODE\ signal selects the BGCLK signal for gated and burst modes. The multiplexer's output is applied to delay line DL1 and to a second multiplexer, U63, along with the VXIbus ECL trigger drivers. The delay line's output is applied to the second multiplexer U63, controlled by the 0DL_SEL\ and 5DL_SEL\ signals selects a fixed delay when the unit is configured as a master in a multiple unit system. The fixed delay accounts for the time delays incurred driving and receiving the VXIbus ECL trigger lines. Multiplexer, U63's output clocks the pulse generator and sync output circuitry.

4.3.11 Delay and Width One-shots

The width and delay one-shots (schematic 1104-00-3612 sheets 12 and 13) are identical; only the delay one-shot will be described. After triggering, the one-shots produce a narrow pulse, ~5ns wide, at the programmed time delay. The one-shots consist of a digital section providing 10 ns resolution and an analog section providing 100 ps resolution. When delays of less than 10 ns are programmed, the analog section is triggered directly. For longer delays the digital section is triggered, which in turn triggers the analog section. A simplified analog one-shot is shown in figure 4-10. Quiescently, the Q\ output of the flip-flop sits at logic high, and the timing capacitor Ct is charged to about -0.9 volts. When triggered, the flip-flop's output is released, and the current source discharges the capacitor producing a linear ramp. The comparator monitors the ramp voltage, and clears the flip-flop when the threshold voltage is exceeded.

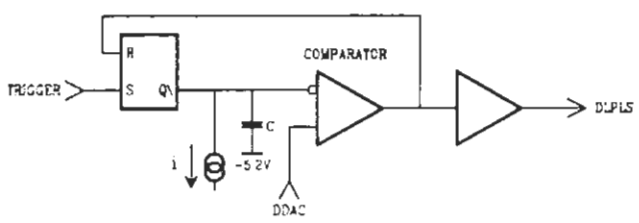


Figure 4-10. Analog One-Shot

When the flip-flop is cleared, its Q\ output rapidly charges the timing capacitor back to -0.9 volts. A narrow pulse is generated during the time it takes to charge the capacitor. The time delay between this pulse and the triggering pulse is proportional to the threshold voltage and the value of the timing capacitor and inversely proportional to the discharging current. With the timing capacitor's value and the discharge current fixed, the time delay is determined by the threshold voltage only, which is controlled by the DDAC signal.

A simplified digital one-shot is shown in figure 4-11. The digital one-shot produces precise delays with 10 ns resolution by counting periods of a 100 MHz gated oscillator. To generate very long time delays, i.e. 2000 seconds, a large counter is required (about 38 bits). A 38-bit counter that clocks at 100 MHz is very expensive, complex, and power hungry, so the counter is split into two sections, a 2-bit high speed ECL counter, and a 36-bit low speed CMOS counter.

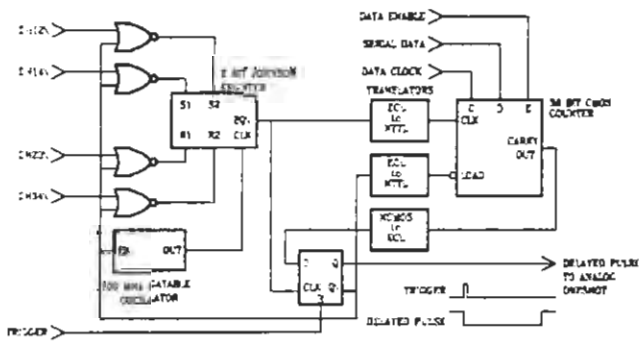


Figure 4-11. Digital One-Shot

The 2-bit counter provides 10 ns resolution steps, while the 36-bit counter provides 40 ns resolution steps. The desired time delay is factored into X * 40 ns steps + Y * 10 ns steps + analog delay. The triggering signal resets the flip-flop, enabling the 100 MHz gatable oscillator and the Johnson counter, and releases the load input of the CMOS counter. After Y 10 ns steps the Johnson counter clocks the CMOS counter. After the CMOS counter clocks X 40 ns steps, its carry output sets the flip-flop's D input high. On the next clock, the Q output returns high, and the counters are reloaded awaiting their next trigger. The rising edge of the delayed pulse then clocks the analog one-shot.

Refer to the schematic diagrams in section 7. NOR gates U71\A and B, route the DLYIN\ signal to the analog or digital one-shots, under control of the DLALSEL\ and DLDSEL\ signals. When long delays are selected, the DLYIN\ signal clears flip-flop U70\B. U70\B's output is translated to NTTL levels by Q22, Q23, R67, and R68 to drive the load input of CMOS counter U75. U70\B's output also enables the gatable oscillator and releases the preset inputs of the Johnson counter. NOR gate U72\C and delay line DL3 form a 100 MHz gatable oscillator. The oscillation frequency is determined by the propagation delay of the gate and the length of the delay line. U72\A, configured as a

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Vbb generator, biases the input of the delay line to ensure that the first period of the oscillator is the same length as later cycles. Gates, U71\B, U71\D, and U72\B delay the oscillator's output to eliminate a race condition in the one-shot. Gate, U72\D performs a similar function.

The gated oscillator runs at about 100 MHz. The exact frequency is unimportant, as the frequency is measured during autocalibration to determine the exact period of the "10 ns" steps. Both sections of U69 form a Johnson or twisted ring counter. The counter has four states each with equal duty cycle, at one fourth of the clock frequency. NOR gates U68\A to D allow presetting the counter to any of its four states. U69\B's output is translated to NTTL levels by Q20, Q21, R65, and R66 to clock CMOS counter U75. CR26 and R64 level shift the counter's NCMOS output to ECL compatible levels. Serial data, DDNCDATA, is clocked into U75 by the S_CLKA\ signal, and latched into U75 by the DDNCEN signal. At the end of the long delay period, U70\B's Q output clocks a logic high into flip-flop U70\A to start the analog one-shot.

When short delays are selected, the DLYIN\ signal is routed to the set input of U70\A to start the analog one-shot. U73 and its associated components form a constant current source to discharge timing capacitor C46. Common base stage Q24 buffers the current source output and limits the voltage swing of U70\A's output. U73 and Q25 force the reference voltage provided by U86 to appear across R71, producing a constant discharging current. The voltage ramp on the timing capacitor is compared against the DDAC signal by comparator, U74\B. RC network R72-C44,5 remove high frequency noise on the DDAC signal to reduce timing jitter. U74\C buffers the comparator's output producing the DLPLS signal to drive the pulse generator.

4.3.12 Pulse Generator

The pulse generator (schematic 1104-00-3612 sheet 11) routes the triggering signal to the width and delay one-shots. The triggering pulse is always routed thru the delay one-shot, as a normal pulse is a delayed pulse with zero delay. A simplified pulse generator is shown in figure 4-12. The glitcher produces a narrow pulse, ~5 ns wide, on the rising edge of the triggering signal. This pulse triggers the delay one-shot, and resets the delay flip-flop. When double pulse is selected, this pulse is also routed to the width one-shot. The delay one-shot produces a narrow pulse after its programmed delay. This pulse triggers the width one-shot as well as clocking a logic high into the delay flip-flop. The pulse resets the width flip-flop 3.5 ns later. The width one-shot produces a narrow pulse after its programmed delay. This pulse clocks a logic high into the width flip-flop. The outputs of the flip-flops are pulses whose widths are equal to the programmed pulse width and delay. The 3.5 ns delay line allows generating a pulse width less than the minimum programmable delay of the width one-shot. Refer to the schematics. U64 sections A and C along with R56 and C65 produce a narrow pulse or glitch on the rising edge of the triggering signal.

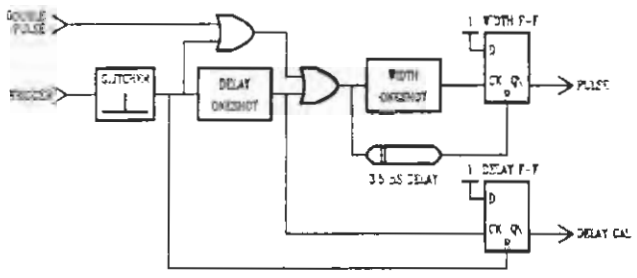


Figure 4-12. Simplified Pulse Generator

This pulse is routed to the delay one-shot. U65 sections A and C route the pulse to the width one-shot under control of the DP_SEL signal. R59 and R60 terminate DL2's output into its characteristic impedance.

4.3.13 Output Mode Selector

The output mode selector (schematic 1104-00-3612 Sheet 11) routes the delay and width outputs from the pulse generator and the pulse generator triggering signal to the analog pulse shaping circuitry and to the autocalibration system. Multiplexer, U67, under control of the PLS_SEL\, SQR_SEL\, TRG_SEL, and DLY_CAL signals, selects the signal applied to exclusive OR gates U41\B and C. The exclusive OR gate inverts the multiplexer's output when pulse complement is selected, via the PLS_COMP signal. U41\B's differential outputs drive the analog pulse shaping circuitry. U41\C's outputs drive ECL to TTL translator U42 to interface with the autocalibration system.

4.3.14 Sync Source Selector

The sync source selector (schematic 1104-00-3612 sheet 14) selects the type of sync signal, pulse or gate, and selectable time delays to account for the various delays of the different pulse modes. U64\B, along with U117 sections A and B, select the GATE_SIG or PLS_SRC signals under control of the SYNCTYPE signal. The GATE_SIG signal is delayed 20 ns by DL7. R248 and R249 terminate the output of DL7. Delay lines DL5, 6, and 8 add additional delay to the selected sync signal. Data selector, U84 under control of the SYNC_SEL1, SYNC_SEL2, and SYNC_SEL3

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signals select either the delayed sync signal or the SYNTH signal when square waves greater than 50 MHz are selected.

4.8.15 Sync Output Driver

The single-ended output from the sync source selector U84 (schematic 1104-00-3612 sheet 14) is converted to differential signals by U36 to drive differential amplifier Q32 - Q33. R90, R91, and R153 provide a constant current to Q32 - Q33. When the sync signal changes state, transistors Q32 and Q33 divert the current to ground or to the R88 - R89 combination and the sync output. When Q33 is turned off, the sync output is pulled up to +5 volts by R88 and R89. When Q33 is turned on, the constant current thru R88 and R89 drops the voltage at the sync output to about zero volts. When an external 50Ω load is connected, a voltage divider is formed with R88 and R89 producing an upper sync level of about +2.5 volts. The lower level remains at about 0 volts.

4.8.16 VXIbus ECL/TTL Trigger Drivers

The VXIbus ECLTRG and TTLTRG lines can be driven by either the pulse signal, with controlled width and delay, or the pulse generator's triggering signal; see schematic 1104-00-3612 sheets 6, 11, and 14. U92 sections A thru D, configured as a data selector, under control of the TTLT_SEL signal, selects which signal drives the VXIbus TTLTRG lines. One section of U42 translates the ECL signal to TTL levels.

Data selector U39, controlled by the OT_TTLTA, OT_TTLTB, OT_TTLTC, and TTRG_EN\ signals, selects which VXIbus TTLTRG line will be driven.

Only one of the VXIbus TTLTRG lines may be driven at a time. Buffer U40 provides the output drive current necessary to drive the VXIbus backplane. The single-ended PULSE\ and P_START signals are buffered and converted to differential signals by U98 sections A and C. The differential signals are received and converted back to single-ended signals by U113 sections A and C. NOR gates U62 and U91, configured as multiplexers, controlled by the EPLSSL0\, EP_SEL0\, EPLSSL1\, and EP_SEL1\ signals, select which signal drives the VXIbus ECLTRIG lines. Each of the two ECL trigger lines may be independently controlled.

4.8.17 Delay - Width - Frequency Autocalibration

The autocalibration circuitry (schematic 1104-00-3612 sheet 24) compares the frequencies of the 25 to 50 MHz gatable oscillator and the delay and width one-shot 100 MHz gated oscillators to the 10 MHz VXIbus Clock10 frequency reference.

The BCLK10+ reference signal is buffered by U113\B. Common base stage Q500 and its associated components disable the reference via the REFON\ signal during normal unit operation. U113's differential ECL level outputs are translated to TTL levels by U42. U114 section A divides the reference by 5 producing a 2MHz reference for timer-counter U112. The timer/counter can directly measure low frequencies up to about 10 kHz. The 25 to 50 MHz gatable oscillator is characterized by programming a burst of 50 cycles at programmed frequency of about 1kHz. The period of the 50 cycles is measured and the actual oscillator frequency is calculated, knowing the programmed divider ratio. This is repeated eight times for frequencies between 1 and 2kHz to determine the oscillator frequency verses control voltage. The delay and width one-shots are characterized by programming a burst of fifty 1ms pulses. The periods of the pulses are averaged and the actual gated oscillator frequency is calculated knowing the programmed divider ratio.

4.8.18 Microprocessor Interface Schematic Diagram

The analog and digital circuitry of the Model 1391 is controlled by the microprocessor located on the VXI Interface board (schematic 1104-00-3612 sheets 1,2, and 3). Signals to and from the interface board are routed thru connectors J4 thru J7. The microprocessor's address space is divided into blocks by decoder U1 and PLD's U2 and U3. Calibration constants are stored in EEROM, U4.

The analog and digital circuitry is controlled by serial input parallel output shift registers that are spread around the main PCB. Serial communication is used to reduce the number of signals on the board. Shift registers U7, U11, and U15 control the analog circuitry and the VXIbus TTL trigger circuitry. The ECL logic used throughout the Model 1391 is powered from the -5.2 volts supply. These devices have a logic high level of -0.9 volts, and a logic low level of -1.8 volts. The logic low level can be as low as -5.2 volts but the logic high level cannot swing above about -0.6 volts without effecting the device speed. CMOS shift registers, U13, U14, and U16 thru U20 are powered between -5.2 and about -0.6 volts via diodes CR6 thru CR11 to control the ECL logic. The CMOS logic levels (0 to +5 volts) of the microprocessor circuitry are translated to negative CMOS levels (-5.2 to -0.6 volts) by translators U5 and U6, powered thru diode CR2. Decoders U8 and U9 further decode the address space providing enabling signals to latch the data into the shift registers.

4.4 PULSE GENERATOR BOARD – ANALOG CIRCUITS

Refer to the Model 1391 Analog Block Diagram (figure 4-13). The sheet numbers shown inside the circuit blocks correspond to the schematic diagram sheet numbers of the Model 1391 main board (1104-00-3612).

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4.4.1 Main High Speed Analog Signal Path

The differential ECL level pulse from the pulse generator circuitry is applied to the level shifter. The level shifter converts the ECL (-0.9 to -1.8 volts) levels to a pulse of about 3Vpp centered around ground to drive the current switch. The current switch alternately switches the REI1 and FEI1 currents from the transition control current sources into the timing capacitors. As the timing capacitors charge, a linear voltage ramp is produced. The larger the REI1 or FEI1 current, the faster the timing capacitor will charge, providing faster edge transitions. Four ranges of timing capacitors can be selected to allow programming slower edge transitions. A larger timing capacitor produces a slower edge speed.

The limiter restrains the voltage on the timing capacitor to 1.2 Vpp. The resulting trapezoidal waveform has smooth leading and trailing edges but large amounts of overshoot that is dependent on the programmed edge speed. The trapezoid shaper clips off the top and the bottom parts of the trapezoidal waveform. The shaper also allows selective clipping of the top or bottom portions of the waveform to produce positive- or negative-going pulses. The multiplier provides gain control to adjust the peak-to-peak output amplitude of the pulse. The pulse amplitude can be modulated via the PAM IN BNC connector. The output amplifier provides voltage and current gain to produce 16 Vpp pulses into a 50Ω load. The output amplifier includes three attenuators to produce low level pulses. The signal on the VXI SUMBUS can also be added to the pulse output using the SUMBUS driver.

The SUMBUS driver contains circuitry to drive and receive the signal on the VXI SUMBUS. The SUMBUS driver produces a current output to the SUMBUS proportional to the amplitude of the pulse output.

Support Circuitry

The support circuitry provides the control voltages and currents required by the high speed analog signal path, and other sections of the Model 1391.

Control Voltage D to A Convertors

The Digital to Analog Convertors (DAC) provide control voltages to adjust the pulse output transitions, amplitude, and offset, the analog width and delay one-shots, the trigger level, and the gated oscillator frequency.

Transition Control Current Sources

The current sources produce current outputs proportional to the control voltage DAC LEDAC and TEDAC outputs to control the leading and trailing edge speeds.

Amplitude Control / PAM

This circuitry processes the control voltage DAC output ADAC, and the PAM IN signal to produce the control voltage for the multiplier, AMPCNTL, to vary the output amplitude.

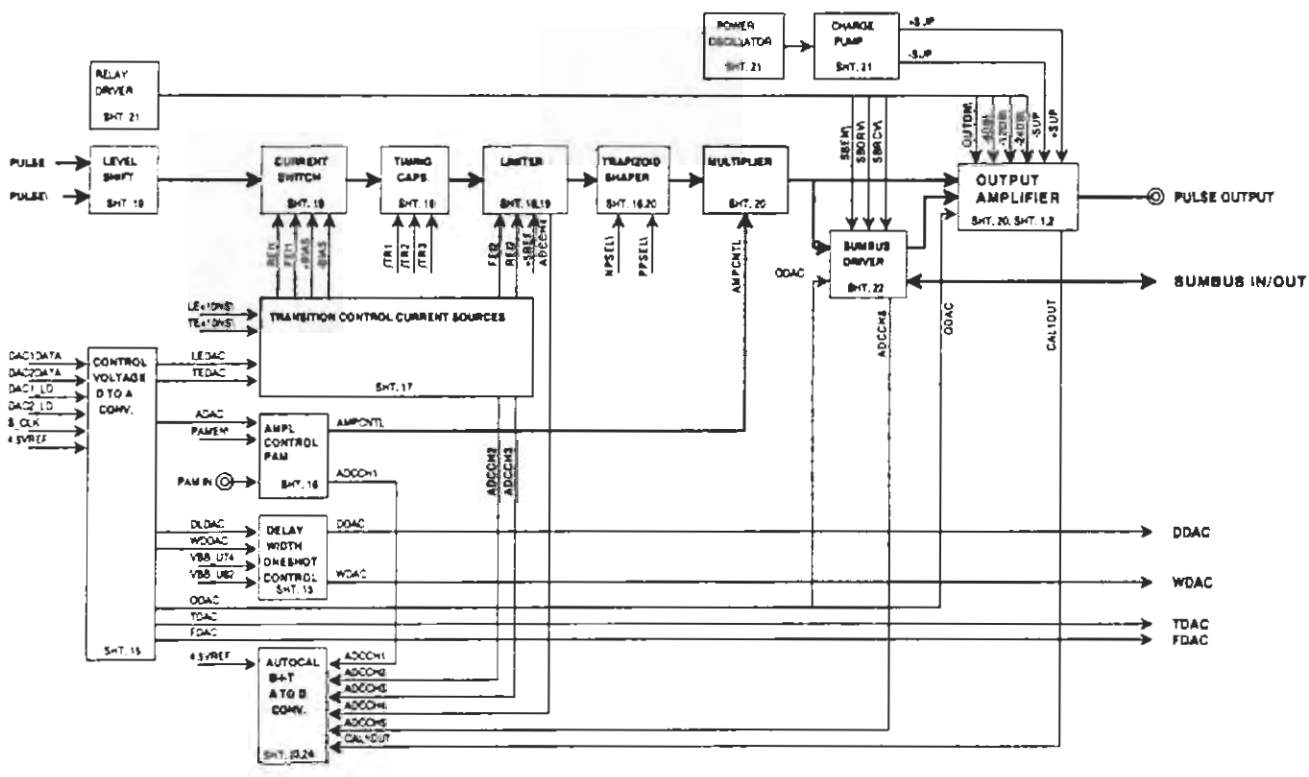


Figure 4-13. Pulse Generator Analog Circuits Block Diagram.

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Delay/Width One-shot Control

This circuitry processes the control voltage DAC outputs DLDAC and WDDAC to produce the control voltages for the width and delay analog one-shots, DDAC and WDAC.

Relay Driver

This circuitry buffers the control lines to drive the relays in the output amplifier and SUMBUS driver.

Power Oscillator

The power oscillator provides a 12 Vpp, 100 kHz square wave to drive the charge pump voltage convertor.

Charge Pump

The charge pump produces approximate ±30 volts power supply rails, +SUP and -SUP, from the ±24 volts VXIbus supplies and the power oscillator output. These high voltage supplies are required for the output amplifier.

Autocal-BIT A to D Convertor

The Analog to Digital Converter (ADC) measures the output amplifier output to calibrate the pulse amplitude and offset. The ADC also monitors several control voltages throughout the analog circuitry for the "Built-In-Test" function.

4.4.2 Level Shift

See Schematic Diagram Sheet 19 (1100-04-3612). U98 receives the differential pulse signal from the pulse generator. Dual diodes CR45 and CR46 biased by R125 thru R128 level shift U98's output about 1.2 volts negative. The bases of Q41 and Q42 swing thru about -2.1 to -3 volts. Q41 and Q42 are configured as a differential amplifier biased from a constant current source via diodes CR47 and CR48. Q43 and its associated components form a constant current source.

The voltage across CR50 is impressed across R132 producing a collector current in Q43 of about 28 mA. CR49 offsets the Vbe of Q43 providing first order temperature compensation of current. When pin 6 of U98 is high (pin 7 is low), Q41 is turned on and current flows from ground thru Q41 and CR47 into Q43. Q42 is off and its collector sits at about +1.5 volts as set by the voltage divider R133 and R134. With pin 6 low, Q41 turns off and Q42 turns on and Q42's collector sits at about -1.5 volts. To increase the speed of the level shifter, Q41 and Q42 are not allowed to turn completely off. R129 and R130 provide a small (about 1mA) current bleed to keep the stage biased.

4.4.3 Current Switch

See Schematic Diagram Sheet 19 (1104-00-3612). Complementary emitter followers Q44 and Q45 buffer the level shifter output to drive the diode switching bridge. CR51, biased by R135-R138, compensates for the Vbe's of Q44 and Q45. C96 and C97 provide AC bypass around CR51 to preserve the edge speeds.

The diode bridge comprised of CR52 thru CR54 alternately switches the FEI1 and the REI1 currents into the timing capacitors. Common base stages Q46 and Q47 buffer the diode bridge from the output capacitance of the current sources, and stray PCB capacitances. The bases of Q46 and Q47 are biased at about ±5 volts by a resistive divider located in the transition control current sources. When the level shifter's output is high (about +1.5 volts), CR53 is forward biased and Q44 sources current into the REI1 current source and reverse biases the lower section of CR54. CR52 is reverse biased and the FEI1 current flows thru the upper section of CR54 and into the timing capacitor. When the level shifter's output is low (about -1.5 volts), CR52 is forward biased and Q45 sinks the current from the FEI1 current source and reverse biases the upper section of CR54. CR53 is reverse biased and the REI1 current flows out of the timing capacitor thru the lower section of CR54.

4.4.4 Timing Capacitors

See Schematic Diagram Sheet 19 (1104-00-3612). Four ranges of transition time are provided by timing capacitors C106 thru C109. The fastest transition range is set by C106 and stray capacitances. Timing capacitors C107 thru C109 are switched in one at a time by diode switches CR56 thru CR58 driven by level shifter Q48.

The operation of the three diode switches are the same. Only the C107 switch will be explained. C107 is selected by driving the TR1/ line to a CMOS logic low (0 volts) which turns on Q48/A. Current flows thru Q48/A and R147 and forward biases both sections of CR56. The bottom end of C107 then see's a low impedance to ground and is effectively put in parallel with C106 slowing down the edge speed.

With the TR1/ signal at a CMOS logic high (+5 volts), Q48/A is turned off and its collector is pulled to –12 volts via R148 reverse biasing the upper section of CR56. The lower section of CR56 is reverse biased to about -7.2 volts, set by voltage divider R145 and R146, via R142.

4.4.5 Limiter

See Schematic Diagram Sheets 18,19 (1104-00-3612). The voltage across the timing capacitor is limited to about ± 0.75 volts by the limiting circuit. U48/D buffers the 5 volt reference applied to inverting amplifier U97/D. RN26/A and R124 set the gain to -0.15 producing the lower limit level of -0.75 volts. U97/B, arranged as a unity gain inverter, produces the upper

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limit level of 0.75 volts. A simplified upper level limiter circuit is shown in figure 4-14. Feedback around U97/C maintains the voltage on the inverting input at +0.75 volts. As the voltage across the timing capacitor rises, CR55 conducts and the FEI1 current flows into U97. With FEI2 equal to FEI1, the voltage drop across CR43 is equal to the voltage drop across CR55, the voltage across the timing capacitor will limit at +0.75 volts.

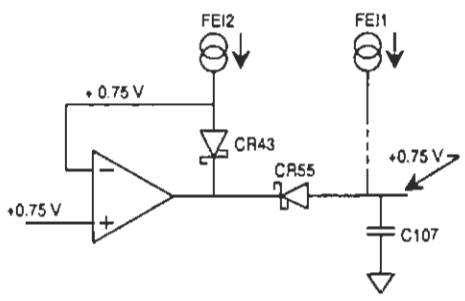


Figure 4-14. Simplified Upper Level Limiter

Refer to the schematic. Q40 buffers the output of U97/C to sink the FEI1 and FEI2 currents. CR35 reduces the power dissipation in Q40. RN26/E bleeds a small current (about 1 mA) into Q40 to stabilize its operating point. R221 and C77 provide U97/C with loop compensation. R256 limits Q40's base current on turn on, as well as damping high frequency oscillations. The lower level limiter operates in the same manner but with reversed polarities. R223 and R224 are part of the built in test circuitry. The midpoint of these resistors will sit very near 0 volts when the limiter circuitry is operating correctly.

4.4.8 Trapezoid Shaper

See Schematic Diagram Sheets 16 and 20 (1104-00-3612). U99, configured as a non-inverting amplifier with a gain of 1.67, buffers the voltage on the timing capacitors to drive the diode shaper. R162 shapes the transient response of U99. U99 is powered from about ±6.9 volts via CR61 and CR62. The output of U99, BUTT, is a waveform of about 2.5 Vpp with smooth leading and trailing edges, but rough top and bottom edges. The distortion is caused by the turn-off time of the limiter diodes. The diode shaper clips off the top and bottom portions of the waveform.

Figure 4-15 shows a simplified shaper. The bridge is fed constant currents via R157 and R158. When the BUTT signal is high, current flows thru R157 and the upper section of CR60 into R163, producing a voltage of about 0.5 volts. At the same time the lower section of CR59 is forward biased and current flows from the BUTT signal into R158. When the BUTT signal swings low, current flows thru R163 and the lower section of CR60 into R158, producing a voltage drop of about -0.5 volts across R163. At the same time, the upper section of CR59 is forward biased and current flows thru R157 and into the BUTT signal.

The end result is a clean 1Vpp waveform across R163. If either of the constant currents is turned off, the waveform will be clipped at ground, producing monopolar pulses. Q34 sections C and B are configured as switches that turn off the current sources. Q34 sections A and D level shift the control signals NPSEL/ and PPSEL/ to drive the switches.

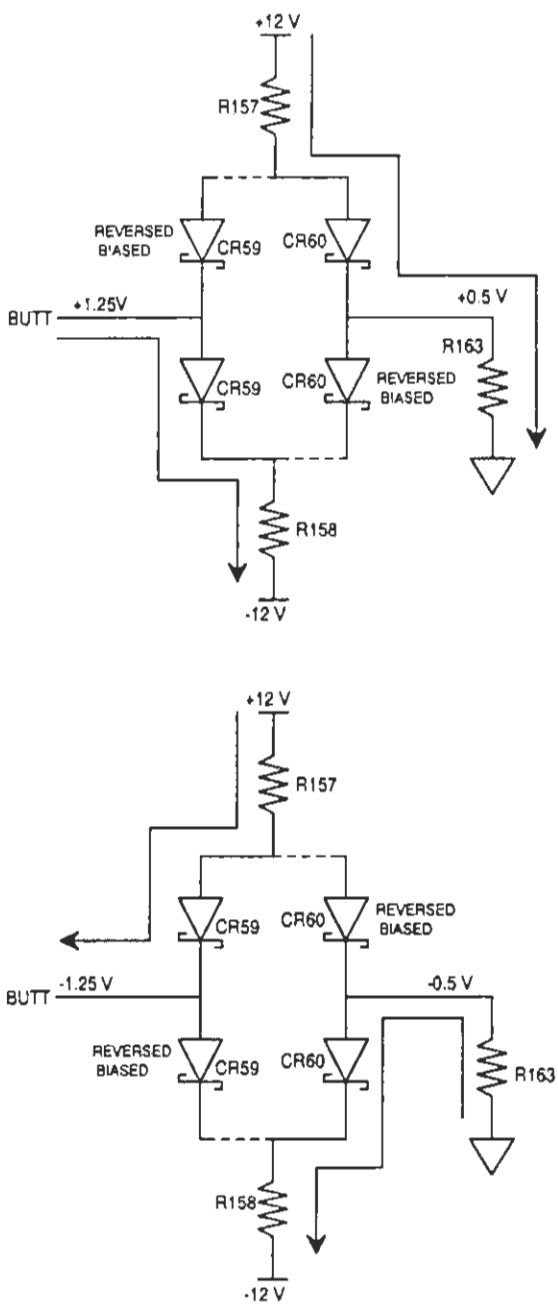


Figure 4-15. Simplified Trapezoid Shaper

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4.4.7 Multiplier

See Schematic Diagram Sheet 20 (1104-00-3612). The output of the trapezoid shaper is applied to the four quadrant multiplier, U101. Resistors R226 and R227 terminate the unused differential inputs of U101. R170 and R171 decouple the multiplier's negative power supply. R169 biases U101's positive power supply. U101 produces a differential current output, proportional to the product of the trapezoidal waveform and the AMPCNTL signal, into R172 and R231. Resistors R228, R232, R230, and R233 level shift the output to within the input common mode range of U102. U102 converts the multiplier's differential output into a single ended signal of about 2Vpp maximum when the output is 16 Vpp into 50Ω.

U102 is powered from the ±5.2 volt rails via CR33 and CR34. Additional voltage gain is provided by non-inverting amplifier U100 and its associated components. R166 and R167 set the voltage gain to about 2.6. R165 is used to shape U100's transient response. R168 isolates U100's output from the stray capacitance of the track leading to the SUMBUS driver.

4.4.8 Output Amplifier

See the Schematic Diagram Sheet 21 (1104-00-3612) and Schematic Diagram Sheets 1,2 (1104-00-3605). The multiplier's output signal, OADRV, drives the output amplifier board. The output amplifier is a discrete inverting stage that provides both voltage and current gain. The amplifier's output is the sum of the AMPDRV, SUMIN, and ODAC signals. The amplifier's gain for the AMPDRV and SUMIN signals is about -6.2 set by the ratios of the feedback resistors, R34, R35, and R38 to the input resistors R5 and R9. The gain for the ODAC signal is about -1.1 set by the ratio of the feedback resistors, R34, R35, and R38 to the input resistor R10. The output amplifier has two signal paths. There is a high speed AC path and a low speed DC correction path. The AC path is divided into two complementary sections, one for each polarity. Only the positive path will be described. C11 AC couples the virtual earth of the amplifier into the common base amplifier Q2. CR5 biases Q2's base to +15 volts, while R20 sets the stage's operating current to about 8mA. Emitter follower stage Q4 buffers Q2's collector to drive the gain stage Q6. Dual diode CR1 temperature compensates the Vbe's of Q2 and Q4. R22 bleeds a small current into CR5 to ensure start-up when power is applied. Q6 operates as a constant current source that is modulated by the AC signal. Q6's voltage gain is very high as its collector load is the high impedance seen looking into the current source Q7. RC network C15 - R32 adjusts the overshoot of the stage. Local feedback around the AC path via C17 and C19 adjusts the waveform quality. Complementary emitter followers Q8 and Q9 buffer the gain stage's output. Diodes CR7 thru CR9 set the quiescent current in Q8 and Q9. R42 thru R45 prevent thermal runaway in Q8 and Q9. Protection diodes CR10 and CR11 limit the amplifier's output to the power supply voltages.

The amplifier's DC path is comprised of U3 and its associated components, Q1, and CR14. U3 maintains the amplifier's virtual earth at zero volts by stealing current from Q6 via Q1. CR14 reduces the power dissipation in Q1. The operating current of Q6 is larger than that of Q7 so that Q1 always has to pull current from Q6. U3 is powered from voltage regulators U1 and U2. Zener diodes CR12 and CR13 reduce the power dissipation in the regulators.

The amplifier's 50Ω output impedance is set by the parallel combination of R46 and R47. R11 allows for measuring the amplifier's output directly during an autocalibration. The amplifier's 50Ω output is applied to three relay selected "pi" section attenuators. Relay K4 is used to disable the output of the amplifier.

4.4.9 SUMBUS Driver

See Schematic Diagram Sheet 22 (1104-00-3612). The SUMBUS driver is a wideband current output amplifier. A simplified schematic is shown in figure 4-16.

U105/B maintains the emitter of Q55 at about -3 volts, forcing a current of about 100 mA thru R191. This current is the sum of Q55's collector current and the current flowing in R189 and R187-R188. U104, configured as a unity gain differential amplifier, forces the voltage across R189 to be equal to the input signal SUMBDRV. Q54 buffers the output of U104. R189 is selected so that a 1Vpp input signal causes a 0 to 80 mA current in R189. Resistors R178 and R179 bias U104's inputs to zero volts forcing a constant 10 mA to flow in R187-R188. Q55's collector current will then swing between 10 and 90 mA. The 50 mA constant current source offsets Q55's collector current, producing an 80 mApp current into the VXI SUMBUS.

Referring to the schematics, CR65 provides a reference voltage referred to the +12 volt rail. A portion of the reference is impressed across R192 by U105/A and Q56, producing a collector current in Q56 of 50 mA, independent of power supply variations. R196 allows for adjusting the nominal current to set the zero offset of the driver. Relay K1 decouples the SUMBUS circuitry from the VXIBUS backplane. R500 and R501 provide an internal 25 ohm load to allow testing of the SUMBUS circuitry. U106 configured as a non-inverting gain of two receives the SUMBUS signal. R200 adjusts the transient response of U106. U107, with an inverting gain of about 1.5, provides an overall gain of -3 between the VXI SUMBUS and the output amplifier. R204 adjusts the transient response of U107. U106 and U107 are powered from about ±6.9 volts via zener diodes CR67 and CR68.

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4.4.10 Control Voltage D to A Convertors

See Schematic Diagram Sheet 15 (1104-00-3612). U48/B buffers the 4.5 volts reference voltage applied to quad 12 bit D to A convertors U87 and U89. Serial data, DAC1DATA and DAC2DATA, is clocked into the DAC's by the serial data clock signal S_CLK\. The data is latched with the DAC1_LD and DAC2_LD signals. Quad DAC U87 provides control voltages to the delay and width one-shot controls, the gatable oscillator, and the trigger amplifier. Voltage follower U90/B buffers the trigger level control voltage. Quad DAC U89 provides control voltages to the transition control current sources, the amplitude control/PAM circuitry, and the output amplifier. U90/A and its associated components offset the DAC output and provide voltage gain to produce a bipolar output control voltage to set the output amplifier offset. R109 and the series/parallel combination of R110, R107-R108 provide a gain of about 7.26 to the DAC output and a gain of about -3.72 to the 4.5 volt reference. The net result is an output voltage swing of about ±15.9 volts. Zener diodes CR30 and CR31 reduce the ±24 volt rails to about ±17.2 volts to power U90.

4.4.11 Amplitude Control/PAM Circuitry

See Schematic Diagram Sheet 16. The 0 to 4.5 volts control signal ADAC is inverted by unity gain amplifier U93/C before being applied to the summing amplifier U93/D. The summing amp has a gain of about -0.232, providing a zero to 1 volt output control voltage to the multiplier AMPCNTL. The PAM_IN signal is inverted by unity gain amplifier U93/B and applied to the summing amplifier via analog switch U94/C. R113 adjusts the PAM scale factor to account for component tolerances. The summing amplifier's output can be monitored for testing via R213.

4.4.12 Transition Control Current Sources

See Schematic Diagram Sheet 17 (1104-00-3612). The trailing edge of the waveform is controlled by the TEDAC signal from the control voltage D to A convertors. U93/A buffers the DAC output to drive the two voltage dividers R214-R215 and R116-R117. Analog switches U94/A and B select which divider drives the current source. When a trailing edge speed of 10 ns or greater is programmed, the TE<10NS\ signal is high enabling U94/A via Q40, which selects the R214-R215 divider. The divider provides about a 0.28 volt input to the current source for a full scale TEDAC output. For trailing edges faster than 10 ns, the R116-R117 divider provides about a 3.5 volt input to the trailing edge current source.

U96/A drives the bases of Q38 sections D, B, and C via level shift zener CR39. Varying the base voltage of Q38 varies the collector currents. Q38/D's collector current produces a voltage drop across RN25/E. Common base stage Q38/A provides a constant collector load for Q38 section D. Q38/A's base is biased to about +5 volts by voltage divider RN24/D-R217. Negative feedback around the loop drives the voltage across RN25/E equal to the input control voltage at TP30. Because Q38 sections B and C are similar to

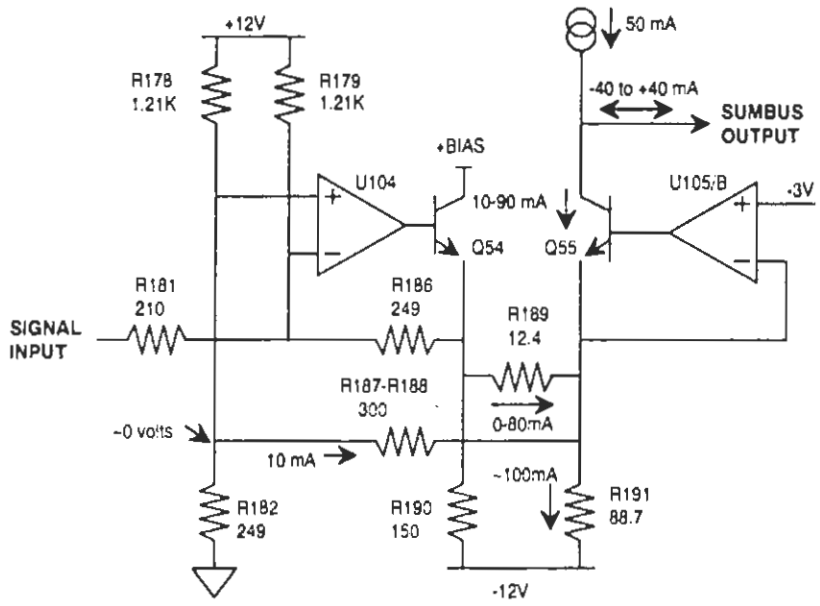


Figure 4-16. Simplified SUMBUS Driver.

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section D, and their emitter resistors are equal, the collector currents will be equal to that of section D. Resistors R120 and R122 stop parasitic oscillations in Q38.

The leading edge of the waveform is controlled by the LEDAC signal from the control voltage D to A convertors. U96/C, an inverting amplifier with selectable gain, inverts and scales the LEDAC signal. When leading edges of 10 ns or greater are programmed, U96/C provides an input to the leading edge current source of about -0.28 volts for a full scale LEDAC output. When edges faster than 10 ns are programmed, the LE<10NS\ signal enables analog switch U94/D placing R118 in parallel with R216. U96/C then provides an input of about -3.5 volts to the leading edge current source.

The operation of the leading edge current source is the same as that of the trailing edge. The voltages across RN25 sections E and A can be monitored by R219 and R220 for testing.

4.4.13 Delay - Width One-shot Control

See Schematic Diagram sheet 15 (1104-00-3612). U85 section A, buffers the DAC output to drive inverting amplifier U85/D. The amplifier has an inverting gain of about 0.83 producing a swing of about 0.37 volts for a zero to full scale swing of the DAC. The amplifier adds an offset to the signal that tracks the threshold of the ECL comparator in the one-shot. The amplifier has a non-inverting gain of about 0.8 to the offset voltage. The amplifier's overall output is a swing from about -1 volts to about -1.37 volts to control the delay analog one-shot.

The operation of the width analog one-shot circuitry is identical to that of the delay one-shot.

4.4.14 Relay Drivar

See Schematic Diagram Sheet 21 (1104-00-3612). U103 buffers the control lines to drive the relays in the output amplifier and SUMBUS driver circuits. Q53 and associated components switch the power supply to the relay coils. A flip-flop in the microprocessor interface section is set upon power up, which turns off Q53. Once the microprocessor is alive and in a known state, the flip-flop is reset, driving the RLYEN\ low, turning on the power to the relays.

4.4.15 Power Oscillator

See Schematic Diagram Sheet 21 (1104-00-3612). U118 a universal timer, running in the astable mode, oscillates at about 100 kHz. Its output at pin 3 is a 0 to 12 volt square wave. Complementary MOSFET's Q51 and Q52 buffer U118's output to drive the charge pump circuitry. C213 provides transient current to the MOSFET's. L2 decouples the switching spikes from the +12 volt supply. F1, a self-resetting circuit protector, shuts down the oscillator if excessive current is drawn.

4.4.16 Charge Pump

See Schematic Diagram Sheet 21 (1104-00-3612). The dual charge pump generates about ±36 volt rails (unloaded) for the output amplifier. When loaded the rails drop to about ±32 volts. The charge pump operates by stacking the ±24 volt supplies on top of the power oscillator's 12 Vpp output. Simplified charge pumps are shown in figure 4-17.

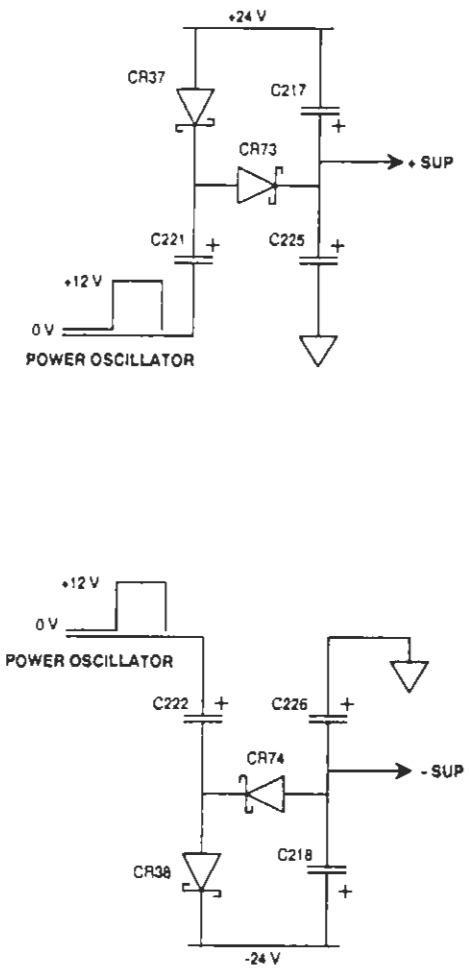


Figure 4-17. Simplified Charge Pump Circuits

Positive pump: When the power oscillator's output is low, C221 is charged to +24 volts thru CR37. When the oscillator's output swings up to +12 volts, CR37 is reverse biased and the top of C221 sits at +36 volts. C221's charge is dumped into C217 and C225 thru CR73. When the oscillator's output swings low again, CR73 is reverse biased preventing the discharge of C217 and C225. This cycle is repeated at about a 100 kHz rate.

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For the negative pump: When the power oscillator's output is high, C222 is charged to 36 volts thru CR38. When the oscillator's output swings down to zero volts, CR38 is reverse biased and the bottom of C222 sits at -36 volts. C222's charge is dumped into C218 and C226 thru CR74. When the oscillator output swings high again, CR74 is reverse biased preventing the discharge of C218 and C226. This cycle is repeated at about a 100 kHz rate.
Going back to the schematic diagrams, multiple capacitors are used in parallel to reduce the ESR to improve the output voltage regulation. Self resetting circuit protectors, F2 and F3, disconnect the ±24 volt supplies from the charge pumps if excessive current is drawn from the output amplifier.

4.4.17 Autocal/ Built - In - Test Circuitry

See Schematic Diagram Sheets 23,24 91104-00-3612). Unity gain followers U108 and U120 buffer the inputs of the A to D convertor U109. The outputs of the buffers are restrained to ±5 volts by the dual diodes to protect the ADC from over-voltage. Resistor R209 is part of a voltage divider used to calibrate the output amplifier. U109 is a 12 bit successive approximation convertor with a serial data output. Shift registers U110 and U111 convert the serial data to parallel data to simplify interfacing with the microprocessor. The A to D is clocked by a 4 MHz signal generated by dividing down the 16 MHz system clock.

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5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize the turn-around time.

5.2 CALIBRATION

Calibration is the process of *Scheduled Maintenance* as described in this section of the Model 1391 manual. Through Calibration, the unit is certified to be operational and within the specifications listed in Section 1 of this manual. The Calibration is valid over a specified *Calibration Interval*. After the interval (typically 1 year), the operator returns the unit to the metrology laboratory for Calibration. Units returned at the scheduled interval, without a failure description, may be calibrated and returned to the operator using the procedures in this section of the manual.

Start the Calibration with the *Performance Verification Procedure* following immediately in this section. Performance Verification tests the unit vigorously to the specifications in Section 1, using external test equipment and signals at the unit's input and output connectors. There are Performance Verification Data sheets at the end of this section which are intended to be copied and used to record the data values from the verification test. Completed Performance Verification Data sheets with no out-of-tolerance readings is sufficient for certification of Calibration and return to the operator.

If there are out-of-tolerance readings, perform the Alignment Procedure later in this section. After successful completion of alignment, complete the Performance Verification Procedure.

If the Alignment Procedure cannot be run successfully, or if the Performance Verification Data still has out-of-tolerance readings after alignment, then refer to Section 6 of this manual for *Fault Isolation*.

The Performance Verification Procedure may also be run before and after *Unscheduled Maintenance* (Troubleshooting) to locate problems and to ensure that all failures have been repaired.

5.3 REQUIRED TEST EQUIPMENT

The test equipment required to perform the Performance Verification Procedure and the Alignment Procedure is listed in table 5-1.

Table 5-1. List of Test Equipment

Equipment	Quantity	Specifications
VXI Requirements	1	VXI chassis.
	1	VXI slot-0 controller.
	1	VXI "C" size extender board. (Optional-see text)
Multimeter	1	HP 3478A or equivalent.
Oscilloscope	1	Tektronix 2465 or equivalent.
Frequency Counter	1	HP 5334A Universal Counter.
Signal Generator	1	Wavetek model 1391 or equivalent VXIbus generator, triggerable, ≤5% accuracy from 25 Hz to 50 MHz.
Voltage Source	1	-10 Vdc to +10 Vdc.
Adaptors	1 ea.	BNC female to banana jacks, BNC "tee".
Coaxial cable	3	BNC male connectors, RG58U cable.
Probe	2	10 MΩ.
50Ω Termination	2	Feedthrough, 0.1% accuracy, 2W.

5.4 PERFORMANCE VERIFICATION PROCEDURE

The Performance Verification Procedure is given in the following paragraphs. These step-by-step procedures outline the equipment setup and interconnect. Once set up for a reading, the various parameter settings and limits are given in the specified data table in the Performance Verification Data sheets at the end of this section.

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5.4.1 Preliminary Tests

a) After noting the serial number from the label between the P1 and P2 connectors, install the Model 1391 Unit Under Test (UUT) in a VXIbus chassis (no extender). Send the following command in order to ensure proper addressing and communication with the Commander:

```
*IDN?
```

Verify the following query response message returned from the UUT:

```
"Wavetek Instruments, 1391, 0,
X.X"
```

b) Allow the UUT 30 minutes of warm-up time. Obtain a copy of the Performance Verification Data sheets and fill in the preliminary data including the serial number and the UUT's software version number "X.X".

c) Perform the "automatic" steps of the Alignment Procedure by sending the command:

```
CAL?
```

Verify the following query response message returned from the UUT is the value "00", indicating AutoCal passed. If a non-zero value is returned, refer to the Troubleshooting data in section 6 of this manual.

5.4.2 Quick Functional Check

Purpose: Functional test to verify that the UUT is functioning correctly with power-on defaults. Also verifies that the pulse output can be turned off and on.

a) Perform the Self Test by sending the command:.

```
*TST?
```

Verify error code response string is "00", and record this value for step 1 under paragraph 5.4.2 of the Data Sheets. If the value is not "00", refer to Appendix D.

b) Send the UUT the `RES` command to set all parameters to their default values (paragraph 3.4.3). Connect PULSE OUT to the oscilloscope using 3 feet 50Ω BNC cable and 50Ω termination at the oscilloscope. Verify PULSE OUT output is off.

c) Send the `OUTP ON;:MARK ON` command to turn on the PULSE OUT and SYNC OUT outputs. Verify PULSE OUT is on with default values, as follows (do not measure at this time, just verify approximate values on oscilloscope):

- single pulse, 1 µs period
- ±2.5 V upper and lower levels
- 250 ns pulse width
- ≤5 ns transitions

d) Connect SYNC OUT to the frequency counter (the use of a 3 foot RG-58 BNC cable and a 50Ω termination will be assumed unless otherwise specified). Record the 1 MHz ± 0.01% frequency in step 2 of the Data Sheet

e) If the UUT is functional, continue with the remaining test paragraphs.

5.4.3 Sync Waveform Characteristics Test

Purpose: Verify pulse characteristics of sync waveform.

Specifications: See the following table:

Step #	Parameter	Specification
1,2	Sync rise/fall time	< 5 ns
3	Hi level (into 50Ω)	>2.0 V
4	Lo level (into 50Ω)	<0.4 V
5,6	Sync Pulse Width	N/A

a) Send the following commands to the UUT:

```
RES
MARK ON
```

b) Connect SYNC OUT to the oscilloscope. Measure the rise time, fall time, upper level, and lower level of the SYNC OUT waveform. Record these values in steps 1 through 4 under paragraph 5.4.3 of the Data Sheet.

c) Send the following commands to the UUT:

```
INIT:CONT OFF
TRIG:COUN 3;TIM 10E-6
PULSE:WIDT 100E-9
```

Measure the pulse width of the SYNC OUT waveform and record the value in step 5 of the Data Sheet.

c) Send the following command to the UUT:

```
MARK:TYPE GATE
```

Measure the pulse width of the SYNC OUT waveform and record the value in step 6 of the Data Sheet.

5.4.4 Gated Mode Test.

Purpose: Verify the functionality of the gated mode.

a) Select an external pulse or square wave signal generator to provide a gating signal for this test. This external signal must cover the range of

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200 ns (2.5 MHz square wave) to 200 ms (25 Hz square wave) with 5% or better accuracy. The generator must be capable of being manually triggered for a single cycle. Note the output voltage range of the external generator and set it to a typical value, for example "TTL" or "±1 volt bipolar".

b) Send the following commands to set the UUT to Gated Mode, external gating source:

```
RES
OUTP ON;:FREQ 5E7;PULS:WIDT 1E-8
INIT:CONT OFF;:TRIG:GATE ON
TRIG:SOUR EXT;LEV <value>
```

where <value> is a dc voltage threshold appropriate for gating on the external signal, for example +1.5 volts for "TTL" or 0 volts for "bipolar".

c) Connect the PULSE OUT to a counter/timer set up to trigger on the ±2.5 volt pulse output of the UUT. Set the counter/timer to count "events".

d) Set the external generator for 200 ns and single cycle it. The counter/timer should indicate that the UUT was gated on for approximately 10 cycles. Record the value in step 1 of paragraph 5.4.4 of the Data Sheets. Reset the counter/timer to "0 events" between readings.

h) Change the UUT to 1 MHz, the external generator to 200 ms, trigger it, and record the counter/timer value in step 2. Remove the external generator.

5.4.5 Burst Mode Test.

Purpose: Verify the functionality of the triggered and burst modes, and of the burst counter.

Comment: Burst count is programmable from 1 to 10,000,000. The observed count must be equal to the programmed value.

a) Send the following commands to set the UUT to Trigger/Burst Mode, "manual" trigger:

```
RES
OUTP ON;:INIT:CONT OFF
TRIG:SOUR BUS
```

b) Connect the PULSE OUT to a counter/timer set up to trigger on the ±2.5 volt pulse output of the UUT. Set the counter/timer to count "events".

c) Send the UUT the `*TRG` command. The counter/timer should indicate that the UUT generated a single cycle. Record the value in step 1 of paragraph 5.4.5 of the Data Sheets. Reset the counter/timer to "0 events" between readings.

d) Send the UUT the `TRIG:COUN 2` command and then the `*TRG` command. Record the counter/timer value in step 2.

e) Send the UUT the `TRIG:COUN 4` command and then the `*TRG` command. Record the counter/timer value in step 3.

f) Send the UUT the `TRIG:COUN 1E3` command and then the `*TRG` command. Record the counter/timer value in step 4. Disconnect the counter/timer.

5.4.6 Pulse Amplitude Accuracy Test

Purpose: Verify the accuracy of the pulse amplitude levels.

Comment: Setting the UUT to the External Width function (no trigger input) causes it to output a dc voltage at the lower level value. Then setting the pulse logic to complement causes it to output a dc voltage at the upper level value.

Specifications: ±((1% of Vpp + 35 mV) + (2% of offset + 50 mV)).

a) Program the UUT as follows to set up in External Width, dc level output:

```
RES
INIT:CONT OFF;:TRIG:GATE ON;SOUR
TOFF:GATE:MODE EXTW;:OUTP ON
VOLT:HIGH 8;LOW -8
```

b) Connect the PULSE OUT to the multimeter (DCV function), using an accurate 50Ω termination. Set `PULS:POL COMP` and measure the upper level value. Record the upper level value in step 1a of paragraph 5.4.6 of the Data Sheets. Set `PULS:POL NORM` and measure the lower level value and record it in step 1b.

c) Program the UUT as follows:

```
VOLT:HIGH 0.5;LOW -0.5
PULS:POL COMP
```

Measure the upper level value and record it in step 2a. Set `PULS:POL NORM` and measure the lower level value and record it in step 2b.

d) Program the UUT as follows:

```
VOLT:HIGH 0.2;LOW -0.2
PULS:POL COMP
```

Measure the upper level value and record it in step 3a. Set `PULS:POL NORM` and measure the lower level value and record it in step 3b.

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e) Program the UUT as follows:

```
VOLT:HIGH 8;LOW 7
PULS:POL COMP
```

Measure the upper level value and record it in step 4a. Set `PULS:POL NORM` and measure the lower level value and record it in step 4b.

f) Program the UUT as follows:

```
VOLT:HIGH -7;LOW -8
PULS:POL COMP
```

Measure the upper level value and record it in step 5a. Set `PULS:POL NORM` and measure the lower level value and record it in step 5b.

5.4.7 Pulse Width Accuracy Test

Purpose: Verify pulse width accuracy.

Comment: Pulse width is measured from the 50% voltage level on the leading edge of the pulse to the 50% voltage level of the trailing edge of the pulse.

Specifications: ± (1.0 % of setting + 2 ns).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON
VOLT:HIGH 5;LOW -5
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Set `PULS:WIDT 10E-9` and measure the pulse width. Record the pulse width value in step 1 of paragraph 5.4.7 of the Data Sheets.

c) Set `PULS:WIDT 13E-9` and measure the pulse width, and record the value in step 2.

d) Set `PULS:WIDT <value>` to the values in the data sheet for steps 3 through 10. Measure the pulse width, and record the values in steps 3 through 10.

e) Set `FREQ 1E5;PULS:WIDT 999E-9` and measure the pulse width, and record the value in step 11.

f) Set `PULS:WIDT 1.999E-6` and measure the pulse width, and record the value in step 12.

5.4.8 Pulse Delay Accuracy Test

Purpose: Verify single pulse delay accuracy of the PULSE OUT.

Comment: The definition for single pulse delay is the time interval from 50% voltage point of rising edge of the SYNC OUT to the 0% voltage point on leading edge of the single pulse (see Figure 1.2).

Specifications: ± (1.0 % of setting + 5 nsec).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON
VOLT:HIGH 5;LOW -5
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Measure the pulse delay. Record the pulse delay value in step 1 of paragraph 5.4.8 of the Data Sheets.

c) Set `PULS:DEL 8E-9` and measure the pulse delay, and record the value in step 2.

d) Set `PULS:DEL <value>` to the values in the data sheet for steps 3 through 10. Measure the pulse delay, and record the values in steps 3 through 10.

e) Set `FREQ 1E4;PULS:WIDT 1E-6;DEL 9.999E-6` and measure the pulse delay, and record the value in step 11.

f) Set `FREQ 1E3;PULS:DEL 99.999E-6` and measure the pulse delay, and record the value in step 12.

5.4.9 Double Pulse Delay Accuracy Test

Purpose: Verify double pulse delay accuracy of the PULSE OUT.

Comment: The definition for double pulse delay is the time interval from 50% voltage point of rising edge of the SYNC OUT to the 0% voltage point on leading edge of the second pulse of a double pulse train.

Specifications: ± (1.0 % of setting + 5 nsec).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON
PULS:DOUB ON
PULS:DOUB:DEL 20E-9
VOLT:HIGH 5;LOW -5
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Measure the double pulse delay. Record the double pulse delay value in step 1 of paragraph 5.4.9 of the Data Sheets.

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c) Set FREQ 10;PULS:WIDT 1E-3; DOUB:DEL 10E-3 and measure the double pulse delay (use Counter/Timer in start/stop mode to make this measurement), and record the value in step 2.

5.4.10 Function Delay Test

Purpose: Verify delay accuracy of the various functions at the PULSE OUT.

Comment: The definition for function delay is the time interval from 50% voltage point of rising edge of the SYNC OUT to the 0% voltage point on the first leading edge of the selected function (single, double or square).

Specifications: ± (1.0 % of setting + 5 nsec).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON
VOLT:HIGH 5;LOW -5
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Measure the single pulse delay and record the value in step 1 of paragraph 5.4.10 of the Data Sheets.

c) Set PULS:DOUB ON and measure the delay to the first pulse, and record the value in step 2.

e) Set FUNC:SQU and measure the delay to the square function, and record the value in step 3.

5.4.11 Pulse Output Transition Times Accuracy Test

Purpose: Verify pulse transition times accuracy for the four different ranges.

Comment: The leading edge transition time (rise time) is measured from the 10% voltage level to the 90% voltage level of the leading edge of the normal pulse. The trailing edge transition time (fall time) is measured from the 90% voltage level to the 10% voltage level of the trailing edge of the normal pulse.

Specifications: ± (5.0 % of setting + 2 ns).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON
VOLT:HIGH 5;LOW -5
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Measure the pulse rise and fall times (5 ns). Record the pulse transition time values in step 1a (rise time) and 1b (fall time) of paragraph 5.4.11 of the Data Sheets.

e) Set PULS:TRAN 45E-9;TRAN:STAT ON and measure the pulse transitions, and record the values in step 2a and 2b.

d) Set FREQ 1E5;PULS WIDT 2.5E-6.

e) Set PULS:TRAN <value> to the values in the data sheet for steps 3 through 5. Measure the pulse transitions, and record the values in steps 3 through 5.

f) Set FREQ 1E4;PULS WIDT 25E-6.

g) Set PULS:TRAN <value> to the values in the data sheet for steps 6 through 7. Measure the pulse transitions, and record the values in steps 6 through 7.

h) Set FREQ 1E3;PULS:WIDT 250E-6; TRAN 50E-6. Measure the pulse transitions, and record the values in step 8.

i) Set FREQ 1E6;PULS:WIDT 250E-9.

j) Set PULS:TRAN <value>;TRAN:TRA <value> to the values in the data sheet (note different LEADing and TRAiling values) for steps 9 through 10. Measure the pulse transitions, and record the values in steps 9 through 10.

k) Set FREQ 1E5;PULS WIDT 2.5E-6.

l) Set PULS:TRAN <value>;TRAN:TRA <value> to the values in the data sheet for steps 11 through 12. Measure the pulse transitions, and record the values in steps 11 through 12.

m) Set FREQ 1E3;PULS:WIDT 250E-6.

n) Set PULS:TRAN <value>;TRAN:TRA <value> to the values in the data sheet for steps 13 through 14. Measure the pulse transitions, and record the values in steps 13 through 14.

5.4.12 Pulse Output Aberrations Test

Purpose: Verify pulse output waveform quality.

Specifications: Peak-to-peak aberrations <(5% of Vpp amplitude + 20 mV).

a) Program the UUT as follows:

```
RES
OUTP ON;:MARK ON;FUNC SQU
VOLT:HIGH 6;LOW -6
```

b) Connect the PULSE OUT to CH1 and the SYNC OUT to CH2 of the oscilloscope. Trigger the oscilloscope from the SYNC OUT (CH2, Internal). Measure the peak-to-peak aberrations. Record the aberration values in step 1a (leading edge) and 1b (trailing edge) of paragraph 5.4.12 of the Data Sheets.

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5.4.13 Trigger Level Test

Purpose: Perform functional test of the trigger slope control and verify triggerlevel accuracy.

Comment: Trigger level is defined as the midpoint of the trigger circuit hysteresis. Therefore, the accuracy of the trigger level setting will be determined by applying a DC level to the TRIG IN connector. The DC level will be incremented, starting from below the "Trig off" level, with respect to the slope setting, while monitoring the generator's PULSE OUT to determine when the unit triggers "on". The DC level is then decremented (with respect to the slope setting) to determine the UUT's "Trig off" level.

The Pulse Generator will be set to the External Width function so that the oscilloscope can be used to monitor the PULSE OUT and determine the trigger 'on' and 'off' points by noting a level change.

Specifications: ± 500 mV.

a) Program the UUT as follows:

```
RES
OUTP ON;:INIT:CONT OFF
TRIG:SOUR EXT;LEV -9
TRIG:GATE:STAT ON;MODE EXTW
```

b) Connect the PULSE OUT to CH1 of the oscilloscope. Trigger the oscilloscope from CH1, Internal. Connect the Signal Generator output to both the TRIG IN connector and the DVM input. Set the Signal Generator to output approximately 1 volt below the programmed level setting. Verify that the UUT PULSE OUT is at the lower level (–2.5 Vdc) on the oscilloscope.

c) Increment the Signal Generator dc output in the positive direction until the PULSE OUT switches to the upper level (+2.5 Vdc), indicating passing through the trigger threshold. Note the value of the dc level at the DVM. Then decrement the Signal Generator dc output in the negative direction until the PULSE OUT switches back to the lower level. Note this value on the DVM. Calculate the Trigger Level as follows:

Trigger level = ("Trig on" level + "Trig off" level) / 2

Record the Trigger Level under paragraph 5.4.13, step 1 in the Data Sheets.

d) Send the UUT `TRIG:LEV <value>`, where <value> is the Trigger Level setting for steps 2 through 3. Repeat the procedure of steps b) and c) above to calculate and record the Trigger Level values under steps 2 through 3.

e) Send the UUT `TRIG:SLOP NEG;LEV -5`. Set the Signal Generator to output approximately 1 volt above the programmed level setting. Verify that the UUT PULSE OUT is at the lower level (–2.5 Vdc) on the oscilloscope. Decrement the Signal Generator dc output in the negative direction until the PULSE OUT switches to the upper level (+2.5 Vdc), indicating passing through the trigger threshold. Note the value of the dc level at the DVM. Then increment the Signal Generator dc output in the positive direction until the PULSE OUT switches back to the lower level. Note this value on the DVM. Calculate the Trigger Level and record the value for step 4.

5.4.14 Synthesizer Frequency Test (>1Hz)

Purpose: To verify functionality and accuracy of synthesizer up to 100 MHz (1 MHz synthesizer accuracy has been tested in paragraph 5.4.1).

Specifications: ± 100 ppm.

a) Program the UUT as follows:

```
RES
MARK ON;:FUNC SQU;FREQ 12.5E6
```

b) Connect the SYNC OUT to the counter/timer (set up to measure frequency). Record the 12.5 MHz value in step 1 of paragraph 5.4.14 of the Data Sheets.

c) Set `FREQ <value>` to the values in the data sheet for steps 2 through 5. Measure the frequency, and record the values in steps 2 through 5.

5.4.15 Burst Gateable Oscillator Frequency Test

Purpose: To verify accuracy and functionality of burst gateable oscillator up to 50 MHz.

Specifications: ± 2%.

a) Program the UUT as follows:

```
RES
INIT:CONT OFF
TRIG:SOUR EXT;GATE ON
MARK ON;:FUNC SQU;FREQ 100
```

b) Connect the SYNC OUT to the counter/timer (set up to measure frequency). Set the Signal Generator to output approximately +5 Vdc and apply it to the TRIG IN connector of the UUT. Record the 100 Hz value in step 1 of paragraph 5.4.15 of the Data Sheets.

c) Set `FREQ <value>` to the values in the data sheet for steps 2 through 9. Measure the frequency, and record the values in steps 2 through 9.

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5.4.16 External Trigger Frequencies Test

Purpose: To verify functionality of external trigger input up to 50 MHz at minimum specified amplitude.

Setup: Single Pulse function. Pulse width 10ns. Mode triggered.

Specifications: Frequency accuracy equal to that of the external Signal Generator; ± 100 ppm if a second model 1391 is used.

a) Program the UUT as follows:

```
RES
MARK ON;:INIT:CONT OFF
PULS:WIDT 10E-9
TRIG:SOUR EXT;LEV 0
```

b) Connect the SYNC OUT to the counter/timer (set up to measure frequency). Verify that the UUT is not generating a frequency. Set up the Signal Generator for a 100 Hz, ±1 volt square (when properly terminated) and connect its output to the TRIG IN connector. Record the 100 Hz value in step 1 of paragraph 5.4.16 of the Data Sheets.

c) Set the Signal Generator to 50 MHz. Measure the UUT frequency and record the value in step 2.

5.4.17 Trigger Source Test

Purpose: Perform functional test to verify that all thirteen trigger sources are selectable and operational.

Comment: The thirteen trigger sources are; External, Internal, BUS, VXIbus eight TTLTRG lines, and the two VXIbus ECLTRG lines. "External" and "BUS" trigger have been verified in a previous test. "Internal" selects the internal trigger generator. A second model 1391 or equivalent VXIbus module will be required to output triggering signals to the VXIbus ECL and TTL trigger lines. The commands given in this test for the external Signal Generator will assume that a model 1391 is used.

Specifications: Internal: ±100 ppm. For ECLTRG and TTLTRG, frequency accuracy equal to that of the external Signal Generator; ± 100 ppm if a second model 1391 is used.

a) Program the UUT as follows:

```
RES
MARK ON;:INIT:CONT OFF
PULS:WIDT 10E-9
TRIG:SOUR INT:TIM 20E-9
```

b) Connect the SYNC OUT to the counter/timer (set up to measure frequency). Record the 50 MHz value in step 1 of paragraph 5.4.17 of the Data Sheets.

c) Set `TRIG:TIM 1E-6` and record the 1 MHz internal trigger frequency in step 2.

d) Program the UUT as follows:

```
TRIG:SOUR TTLT0
```

Program the external Signal Generator as follows:

```
RES
FREQ 2E3
OUTPUT:TTLT0 ON
```

Record the 2 kHz frequency in step 3.

e) Program the UUT as follows:

```
TRIG:SOUR <source>
```

Program the external Signal Generator as follows:

```
FREQ <frequency>
OUTP:<source> ON
```

Where the parameters <source> and <frequency> are taken from the Data Sheet step as the test step advances from step 4 through step 12. Record the UUT frequency value for each step in the Data Sheet.

5.4.18 Trigger Output Mode Test

Purpose: Perform functional test to verify that the Pulse Generator can serve as a trigger source for one of eight of the VXIbus TTLTRG lines, and one of two of the VXIbus ECLTRG lines. There are two possible sources for this signal, TRIP and PULSE.

Specifications: Trigger frequency generated by the 1391 UUT accuracy is ±100 ppm.

a) Program the UUT as follows:

```
RES
FUNC SQU:FREQ 12E3
OUTP:TTLT0 ON
```

Program the external Signal Generator as follows:

```
RES
MARK ON;:INIT:CONT OFF
PULS:WIDT 10E-9
TRIG:SOUR TTLT0
```

b) Connect the external Signal Generator's SYNC OUT to the counter/timer (set up to measure frequency). Record the 12 kHz value in step 1 of paragraph 5.4.18 of the Data Sheets.

c) Set the UUT `OUTP:TTLT0:SOUR PULS;:FREQ 11E3` and record the 11 kHz trigger frequency in step 2.

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d) Set the UUT `OUTP:TTLT0:SOUR TRIP`.

e) Program the external Signal Generator as follows:

`TRIG:SOUR <source>`

Program the UUT as follows:

`FREQ <frequency>`

`OUTP:<trig line> ON`

Where the parameters <source>, <frequency>, and <trig line> are taken from the Data Sheet step as the test step advances from step 3 through step 10. Record the Signal Generator's triggered frequency value for the listed steps in the Data Sheet.

f) Set the UUT `OUTP:ECLT0:SOUR PULS;:FREQ 11E3` and record the 11 kHz trigger frequency in step 11.

g) Set the UUT `OUTP:ECLT1:STAT ON;SOUR TRIP;:FREQ 10E6`, set the Signal Generator `TRIG:SOUR ECLT1`, and record the 10 MHz trigger frequency in step 12.

f) Set the UUT `OUTP:ECLT1:SOUR PULS;:FREQ 21E3` and record the 21 kHz trigger frequency in step 13.

5.4.18 Master/Slave Test

Purpose: Perform functional test of the MASTer/SLAVe control, and verify intermodule time skew accuracy.

Comment: This test can only be run if the external Signal Generator is a Wavetek model 1391. The UUT is designated the MASTer. The model 1391 used as the external generator is designated as the SLAVe. The MASTer and SLAVe units must be in adjacent slots in the VXIbus chassis to test close coupling of signal delays.

a) Program the UUT as follows:

`RES`

`OUTP ON;ECLT0 ON;:MARK ON`

`TRIG:MODE MAST`

Program the external Signal Generator as follows:

`RES`

`MARK ON;:OUTP ON;:INIT:CONT OFF`

`TRIG:SOUR ECLT0`

b) Connect the UUT'S SYNC OUT to the oscilloscope CH1 and the external Signal Generator's SYNC OUT to CH2. Trigger the oscilloscope internally from CH1. Record the time skew value between the two rising edge 50% points in step 1 of paragraph 5.4.19 of the Data Sheets.

c) Connect the UUT'S PULSE OUT to the oscilloscope CH1 and the external Signal Generator's PULSE OUT to CH2. Record the time skew value between the two rising edge 50% points in step 2.

5.4.20 SUMBUS Test

Purpose: Perform functional test of the SUMBUS driver and receiver section, and verify voltage scaling accuracies.

Comment: This test can only be run if the external signal generator is a VXIbus module supporting the SUMBUS per the VXIbus System Specifications. This procedure will use SCPI commands which assume that the external generator is another Wavetek model 1391.

Specification: The 1391's SUMBUS driver outputs 5 mA per volt (at the Pulse Output) to the 25Ω ± 2% SUMBUS with an accuracy of ±(6% + 2.5mA). The 1391's SUMBUS receiver generates 8 volts at the Pulse Output per volt SUMBUS signal with an acuracy of ±(6% + 200 mV + 2.5 mA). End-to-end specification (one 1391 driving the SUMBUS, one 1391 receiving) is the sum of the percentage and offset voltage terms, and the current offset terms multiplied by 25Ω and the receiver gain of eight. This results in ±(14% + 1.2 V) end-to-end.

a) Program the UUT as follows:

`RES`

`OUTP ON;:INIT:CONT OFF`

`TRIG:SOUR TOFF;:VOLT 4`

Connect the UUT's PULSE OUT to the DVM. Record the lower level value in step 1 of paragraph 5.4.20 of the Data Sheets.

b) Program the UUT as follows:

`SOUR:SUMB ON`

Program the external Signal Generator as follows:

`RES`

`INIT:CONT OFF;:OUTP:SUMB ON`

`TRIG:SOUR TOFF;:VOLT 4`

`PULS:POL COMP`

c) Record the lower level in step 2.

d) Set the external Signal Generator `VOLT 16`. Record the lower level in step 3.

e) Perform steps a) through d) above, except reverse the roles of the "UUT" and the "external Signal Generator". Record the data values in steps 4 through 6.

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5.4.21 PAM Input Test

Purpose: Perform functional test of the PAM IN circuitry, and verify voltage scaling accuracies.

a) Program the UUT as follows:

```
RES;:OUTP ON;:INIT:CONT OFF
TRIG:SOUR TOFF;:VOLT 10
PULS:POL COMP
```

Connect the UUT's PULSE OUT to the DVM. Record the upper level valuc in step 1 of paragraph 5.4.21 of the Data Sheets.

b) Set the UUT `PULS:POL NORM` and record the lower level in step 2.

c) Apply +1.00 Vdc to the UUT's PAM IN connector. Verify accuracy with the DVM.

d) Set the UUT to `PULM ON;PULS:POL COMP` and record the upper level in step 3. Set the UUT `PULS:POL NORM` and record the lower level in step 4.

e) Set the UUT to `PULM:AMPL NEG;:PULS:POL COMP` and record the upper level in step 5. Set the UUT `PULS:POL NORM` and record the lower level in step 6.

f) Set the UUT to `PULM:AMPL POS;:PULS:POL COMP` and record the upper level in step 7. Set the UUT `PULS:POL NORM` and record the lower level in step 8.

This completes the Performance Verification-Procedure.

5.5 ALIGNMENT PROCEDURE

The procedure given in paragraph 5.5.5 requires that the model 1391 be part of a VXI system as described in table 5-1. The model 1391 will be installed on a C-size VXI extender card and controlled by the Resource Manager. The computer/display device can be the Resource Manager (internal host in a Stand-Alone system) or an external host connected to the Resource Manager via the IEEE-488 (GPIB) programming bus.

WARNING

With the covers removed, low voltage dc power supplies are exposed. Do not be misled by the term "low voltage". Under adverse conditions, potentials as low as 50 volts can cause serious injury or death.

WARNING

With the module on an extender card and the covers removed, no chassis cooling air is moving across the components. The Pulse Generator has many high-speed digital logic devices and discrete analog circuits which require some cooling air for continuous operation. Do not operate the module in this configuration for more than a few minutes without directing some cooling air across the face of the Main Pulse Board and the Amplifier Board using an external utility fan. Avoid burns - do not touch components in the module.

5.5.1 Self Calibration

The model 1391 performs a Self Calibration in response to the SCPI `CAL[:ALL]?` command or to the IEEE-488.2 `*CAL?` command. The Self Calibration performs only those steps in the "full" Calibration procedure of paragraph 5.5.5 which are marked "automatic". Self Calibration steps are performed by the instrument firmware at any time the operator/programmer sends the appropriate commands following the 30 minute warm-up. Self Calibration sets up various internal interconnections and uses internal time and voltage standards to store "fresh" Alignment Data which is used to optimize the unit's performance accuracy. During the Self Calibration, the unit disconnects all inputs and outputs, and at the end of Self Calibration it restores its current setup.

A Self Calibration is performed just prior to running the Performance Verification Procedure. Therefore, if there is an out-of-tolerance reading, the Self Calibration is not likely to correct it, and the "full" Alignment Procedure in paragraph 5.5.5 should be run.

5.5.2 Semi-Automated Procedure

When the alignment procedure is initiated, the Model 1391 firmware returns an abbreviated description of the current alignment step to the system console, and instructs the Pulse Generator to modify its settings in preparation for making that adjustment. The abbreviated description identifies the parameter, alignment tolerance, and adjustment component. The procedure is initiated by sending 'DIAG:CAL?', followed by the alignment step number, and a program message terminator.

NOTE

The completion of the alignment procedure returns the instrument to correct alignment.

Alignment limits and tolerances are not instrument specifications.

Instrument specifications are given in Section 1 of this Manual.

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5.5.3 Preparation

Obtain access to adjustable components by removing the side panel *without* the address switch cutout. Mount the module on an extender card, or plug it into a VXI chassis connector that will allow access during calibration. Provide cooling air across the face of the module using the VXIbus chassis or an external utility fan. Allow at least a 30 minute warm-up.

5.5.4 Connactor Termination

When used as test points, the SYNC OUT and PULSE OUT connectors must be terminated with 50Ω.

5.5.5 Alignment Procedure

To prepare the instrument for each step, send 'DIAG:CAL?', followed by the calibration step number and the END program message terminator (see paragraph 3.3.2.5). For steps that are identified as interacting with another step, all interacting steps must be within calibration tolerance before advancing to the next step. Figure 5-1 shows test point and adjustment locations.

NOTE

An automated version of this procedure is available to reduce the set-up time and operator programming. The program is written using WaveTest™ and there are operator panels which prompts the calibrator with instructions on which components/ parameters to adjust. For customers with the WaveTest™ programming environment, this program can be obtained from the Wavetek Customer Service department (see paragraph 6.1).

If the calibration program is not available, then perform the procedure below to calibrate the unit. The pulse width, pulse delay and the rise/fall time calibration section requires measured data to be entered into the Model 1391 database.

1) Instrument set-up and database initialization

   a) Send the command to force instrument power-up state;

   ```
   *RST
   ```

   b) If the unit being calibrated has been repaired or is known to be operating outside of specified limits, then send the command to initialize intrument database;

   ```
   :diag:cal:init
   ```

2) Automatic linearity adjustment of burst gateable oscillator frequency.

   a) Send the command:

   ```
   :diag:cal? 1
   ```

   b) Successful completion of this step is indicated by the response message;

   ```
   <response message>. Passed
   ```

3) Automatic measure of width gateable oscillator frequency.

   a) Send the command:

   ```
   :diag:cal? 2
   ```

   b) Successful completion of this step is indicated by the response message;

   ```
   <response message>. Passed
   ```

4) Automatic measure of delay gateable oscillator frequency.

   a) Send the command:

   ```
   :diag:cal? 3
   ```

   b) Successful completion of this step is indicated by the response message;

   ```
   <response message>. Passed
   ```

5) Manual calibration of amplitude limiter offset.

   a) Send the command:

   ```
   :diag:cal? 4
   ```

   b) Connect DMM HI to Output Amplifier P1 pin 5, and DMM LO to Output Amplifier TP1.

   c) Apply a 500 mVpp, 0V offset, 0.05 Hz square wave from the function generator to PAM input BNC of the pulse generator. Use the 50 Ω feed-thru terminator.

   d) Adjust **R158** for a DC voltage shift of <1mV. The absolute value of the offset voltage is unimportant.

   e) Disconnect the cable to the pulse generator PAM input BNC.

6) Manual calibration of pre-amplifier offset.

   a) Send the command:

   ```
   :diag:cal? 5
   ```

   b) Connect DMM HI to Output Amplifier P1 pin 5, and DMM LO to Output Amplifier TP1.

   c) Adjust **R520** for a DC offset of < 2 mV.

   d) Disconnect DMM leads.

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7) Automatic amplitude and offset calibration.

a) Send the command:

```
:diag:cal? 6
```

b) Successful completion of this step is indicated by the response message;

```
<response message>. Passed
```

8) Manual pulse amplitude modulation gain calibration.

a) Send the command:

```
:diag:cal? 7
```

b) Apply a 0.500 VDC signal from the function generator to PAM input BNC of the pulse generator. Use the 50 Ω feedthru terminator.

c) Adjust **R113** for a change of 0.5 Vdc ± 10 mV measured by the DMM at PULSE OUT of the pulse generator. Use the 50 Ω feedthru terminator at PULSE OUT BNC.

d) Disconnect the cable to the pulse generator PAM input BNC.

9) Gateable Oscillator First Period Adjustment.

a) Connect PULSE OUT of the pulse generator to the scope CH 1, 2V/div, 50 Ω internal load. Connect the pulse generator's SYNC OUT to CH2, 500 mV/div, 50 Ω internal load of the scope. Sync the scope on CH2. Set a sweep rate of 5 ns/div, X10 magnifier on, Δt cursors on.

b) Send the command:

```
:diag:cal? 8
```

c) Using the cursor and the horizontal position controls, measure the period of the third cycle of the burst. The period should be approximately 40 ns. Measure the period of the first cycle of the burst and adjust **R42** to the same period as the third cycle.

d) Send the command:

```
:diag:cal? 9
```

e) The period should be approximately 20 ns at this step. Repeat the measurements of the periods of cycles 1 and 3 as in step 9.c.

Ajust **R42** to split the error difference between the adjustment in step 9.c and this step.

f) Repeat steps 9.b through 9.e as necessary to minimize the errors.

10) Waveform Quality adjustment.

a) Connect PULSE OUT of the pulse generator to the scope CH1, 2 V/div, 50 Ω internal load. Connect the pulse generator's SYNC OUT to CH2, 500 mV/div, 50 Ω internal load of the scope. Sync the scope on CH2. Set a sweep rate of 10 ns/div.

b) Send the command:

```
:diag:cal? 10
```

c) Adjust **R76**, **R32**, **R33** and **C19** on the Output Amp and **R165** on mainboard for minimum aberrations (< 4% of peak-to-peak amplitude). Verify that rise and fall times are < 5 ns.

NOTE

If satisfactory results are not obtained (i.e., cannot get both rise/fall times and aberrations into specification at the same time), reset the four adjustments of step c) as indicated in Figure 5-1 and repeat the step.

11) SUMBUS offset adjustment.

a) Connect the DMM HI to P7-A18 on the VXI Interface board. Connect the DMM LO to TP38 on the 1391 pulse generator board. Measure and record the SUMBUS DC offset and make sure it is < 1mV before continuing.

b) Send the command:

```
:diag:cal? 11
```

c) Adjust **R196** for the same SUMBUS dc offset as measured in 11a above ± 1 mV.

12) Width one-shot analog calibration.

a) Connect PULSE OUT of the pulse generator to the scope CH1, 2 V/div, 50 Ω internal load. Connect the pulse generator's SYNC OUT to CH2, 500 mV/div, 50 Ω internal load of the scope. Sync the scope on CH2. Set up the scope for pulse width measurement.

b) Send the command:

```
:diag:cal? 12
```

c) Measure the pulse width from the 50% point of the rising edge to the 50% point of the falling edge of the signal at PULSE OUT. This value should be around 17.0 ns.

d) Send the command:

```
:diag:cal:meas 12,<pulse width>
```

where pulse width is the measurement made in step 12.c above. This stores the measurement made into the Model 1391 database.

e) Send the command:

```
:diag:cal? 13
```

f) Measure the pulse width from the 50% point of the rising edge to the 50% point of the falling edge

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of the signal at PULSE OUT. This value is approximately 29.0 ns.

g) Send the command:

```
:diag:cal:meas 13,<pulse width>
```

where pulse width is the measurement made in step 12.f above.

13) Delay one-shot analog calibration.

a) Connect PULSE OUT of the pulse generator to the scope CH1, 2 V/div, 50 Ω internal load. Connect the pulse generator's SYNC OUT to CH2, 500 mV/div, 50 Ω internal load of the scope. Sync the scope on CH2. Set up the scope for pulse delay measurement.

b) Send the command:

```
:diag:cal? 14
```

c) Measure the delay from the 50% point of the SYNC OUT signal to the 0% point of the PULSE OUT signal. This value is approximately 10.0 ns.

NOTE

The delay at the 0% point of the PULSE OUT signal can be easily found by following the steps below.

1) Measure the delay from the 50% point of the SYNC OUT signal to the 50% point of the PULSE OUT signal.
2) Measure the rise time of the PULSE OUT signal at the 10% to 90% points. Multiply this number by 5/8.
3) The 0% delay is found by subtracting the number found in step 2) from the number found in step 1).

d) Send the command:

```
:diag:cal:meas 14,<pulse delay>
```

where pulse delay is the measurement made in step 13.c above.

e) Send the command:

```
:diag:cal? 15
```

f) Measure the delay from the 50% point of the SYNC OUT signal to the 0% point of the PULSE OUT signal. This value is approximately 22.0 ns.

g) Send the command:

```
:diag:cal:meas 15,<pulse delay>
```

where pulse delay is the measurement made in step 13.f above.

14) Leading edge transition times measurement.

a) Connect PULSE OUT of the pulse generator to the scope CH1, 2 V/div, 50 Ω internal load. Connect the pulse generator's SYNC OUT to CH2, 500 mV/div, 50 Ω internal load of the scope. Sync the scope on CH2.

b) Send the command:

```
:diag:cal? <step number>
```

where <step number> goes from 16 through 45.

c) Measure the rise time at the 10% to 90% points of the pulse on the PULSE OUT BNC.

d) Send the command:

```
:diag:cal:meas <step_number>,
<measured value>
```

where <measured value> is the measurement made in step 14.c above.

e) Repeat steps 14.b through 14.d for the remaining step numbers.

15) Trailing edge transition times measurement.

a) Send the command:

```
:diag:cal? <step number>
```

where <step number> goes from 46 through 75.

b) Measure the fall time at the 90% to 10% points of the pulse on the PULSE OUT BNC.

c) Send the command:

```
:diag:cal:meas
<step_number>,<measured value>
```

where <measured value> is the measurement made in step 15.b above.

d) Repeat steps 15.a through 15.c for the remaining step numbers.

16) Database storage

a) Send the command:

```
:diag:cal:save
```

to store the measured constants into non-volatile memory.

NOTE

To verify the accuracy of Alignment Data in storage, send the command `DIAG:MEAS?` *<n> to query the values for a given step <n>. These values may have been entered either automatically or manually.*

An out-of-tolerance Performance Verification step may have a faulty data entry relating to that parameter.

This completes the Alignment Procedure.

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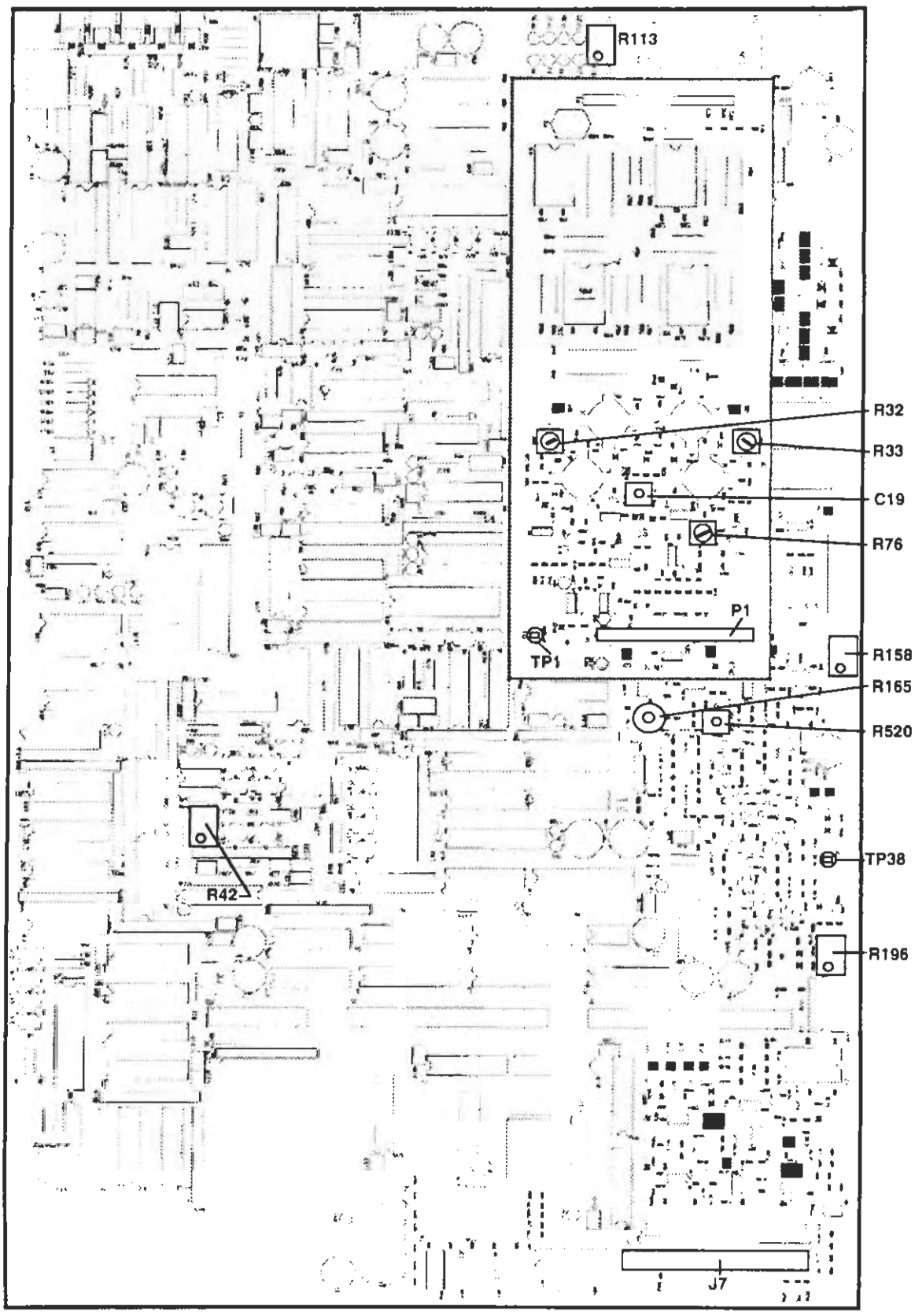


Figure 5-1. Test Points and Adjustments.

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PERFORMANCE VERIFICATION DATA SHEETS

Wavetek Model 1391 VXIbus Pulse Generator

Serial Number _____ **Test Conductor** _____

Firmware Version _____ **Date** _____

History:

- ❑ **Scheduled Maintainance (Calibration)**
- ❑ **Post-Alignment Verification**
- ❑ **Post-Repair Verification**

Comments: _____

_____

_____

_____

_____

5.4.2 Quick Functional Check

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1	*TST Error Response	00	_____	00	N/A
2	1 MHz Frequency	999,900	_____	1,000,100	Hz

5.4.3 Sync Waveform Characteristics Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1	Sync Rise time	N/A	_____	5.0	ns
2	Sync Fall time	N/A	_____	5.0	ns
3	Hi level(into 50Ω)	2.0	_____	N/A	V
4	Lo level(into 50Ω)	N/A	_____	0.4	V
5	CLOCk Type Sync Width	400	_____	600	ns
6	GATE Type Sync Width	2	_____	3	µs

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5.4.4 Gated Mode Test.

Step #	Gate Signal Width	Lo limit	Reading	Hi limit	Unit
1	200ns	9	_____	11	Events
2	200ms	180,000	_____	220,000	Events

5.4.5 Burst Mode Test.

Step #	Burst Count	Lo limit	Reading	Hi limit	Unit
1	1	1	_____	1	Events
2	2	2	_____	2	Events
3	4	4	_____	4	Events
4	1,000	1,000	_____	1,000	Events

5.4.B Pulse Amplitude Accuracy Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1a	8V upper level	7.755	_____	8.245	V
1b	-8V lower level	-8.245	_____	-7.755	V
2a	0.5V upper level	0.405	_____	0.595	V
2b	-0.5V lower level	-0.595	_____	-0.405	V
3a	0.2V upper level	0.111	_____	0.289	V
3b	-0.2V lower level	-0.289	_____	-0.111	V
4a	8V upper level	7.755	_____	8.245	V
4b	7V lower level	6.755	_____	7.245	V
5a	-7V upper level	-7.245	_____	-6.755	V
5b	-8V lower level	-8.245	_____	-7.755	V

5.4.7 Pulse Width Accuracy Test

Step #	Parameter	Lo limit	Reading	Hi limit	Units
1	10 ns Pulse width	7.90	_____	12.10	ns
2	13 ns Pulse width	10.87	_____	15.13	ns
3	14 ns Pulse width	11.86	_____	16.14	ns
4	15 ns Pulse width	12.85	_____	17.15	ns
5	16 ns Pulse width	13.84	_____	18.16	ns
6	28 ns Pulse width	25.72	_____	30.28	ns

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Step #	Parameter	Lo limit	Reading	Hi limit	Units
7	38 ns Pulse width	35.62		40.38	ns
8	48 ns Pulse width	45.52		50.48	ns
9	58 ns Pulse width	55.42		60.58	ns
10	68 ns Pulse width	65.32		70.68	ns
11	999 ns Pulse width	987		1011	ns
12	1.999 µs Pulse width	1.977		2.021	µs

5.4.8 Pulse Delay Accuracy Test

Step #	Parameter	Lo limit	Reading	Hi limit	Units
1	0 ns Pulse Delay	-5.00		5.00	ns
2	8 ns Pulse Delay	2.92		13.08	ns
3	9 ns Pulse Delay	3.91		14.09	ns
4	10 ns Pulse Delay	4.90		15.10	ns
5	11 ns Pulse Delay	5.89		16.11	ns
6	23 ns Pulse Delay	17.77		28.23	ns
7	33 ns Pulse Delay	27.67		38.33	ns
8	43 ns Pulse Delay	37.57		48.43	ns
9	53 ns Pulse Delay	47.47		58.53	ns
10	63 ns Pulse Delay	57.37		68.63	ns
11	9.999 µs Pulse Delay	9.894		10.104	µs
12	99.999 µs Pulse Delay	98.994		101.004	µs

5.4.8 Double Pulse Delay Accuracy Test

Step #	Parameter	Lo limit	Reading	Hi limit	Units
1	20 ns Double Delay	14.8		25.2	ns
2	10 ms Double Delay	9.90		10.10	ms

5.4.10 Function Delay Test

Step #	Parameter	Lo limit	Reading	Hi limit	Units
1	Single Pulse	-5.00		5.00	ns
2	Double Pulse	-5.00		5.00	ns
3	Square	-5.00		5.00	ns

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5.4.11 Pulse Output Transition Times Accuracy Test

Step #	Parameter/Transition time	Lo limit	Reading	Hi limit	Units
1a	Rise time/5 ns	2.75	_____	7.25	ns
1b	Fall time/5 ns	2.75	_____	7.25	ns
2a	Rise time/45 ns	40.75	_____	49.25	ns
2b	Fall time/45 ns	40.75	_____	49.25	ns
3a	Rise time/55 ns	50.25	_____	59.75	ns
3b	Fall time/55 ns	50.25	_____	59.75	ns
4a	Rise time/450 ns	425.5	_____	474.5	ns
4b	Fall time/450 ns	425.5	_____	474.5	ns
5a	Rise time/550 ns	520.5	_____	579.5	ns
5b	Fall time/550 ns	520.5	_____	579.5	ns
6a	Rise time/4.5 µs	4.273	_____	4.727	µs
6b	Fall time/4.5 µs	4.273	_____	4.727	µs
7a	Rise time/5.5 µs	5.223	_____	5.777	µs
7b	Fall time/5.5 µs	5.223	_____	5.777	µs
8a	Rise time/50 µs	47.50	_____	52.50	µs
8b	Fall time/50 µs	47.50	_____	52.50	µs
9a	Rise time/25 ns	21.75	_____	28.25	ns
9b	Fall time/250 ns	235.5	_____	264.5	ns
10a	Rise time/250 ns	235.5	_____	264.5	ns
10b	Fall time/25 ns	21.75	_____	28.25	ns
11a	Rise time/250 ns	235.5	_____	264.5	ns
11b	Fall time/2.5 µs	2.373	_____	2.627	µs
12a	Rise time/2.5 µs	2.373	_____	2.627	µs
12b	Fall time/250 ns	235.5	_____	264.5	ns
13a	Rise time/2.5 µs	2.373	_____	2.627	µs
13b	Fall time/25 µs	23.75	_____	26.25	µs
14a	Rise time/25 µs	23.75	_____	26.25	µs
14b	Fall time/2.5 µs	2.373	_____	2.627	µs

5.4.12 Pulse Output Aberrations Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1a	+ Aberrations	N/A	_____	0.620	Vpp
1b	- Aberrations	N/A	_____	0.620	Vpp

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5.4.13 Trigger Level Test

Step #	Slope/Trigger level	Lo limit	Reading	Hi limit	Units
1	Positive/trig level @ -9.0	-9.50	_____	-8.50	V
2	Positive/trig level @ 0.0	-0.50	_____	0.50	V
3	Positive/trig level @ +9.0	8.50	_____	9.50	V
4	Negative/trig level @ -5.0	-5.50	_____	-4.50	V

5.4.14 Synthesizer Frequency Test

Step #	Frequency Set	Lo limit	Reading	Hi limit	Units
1	12.50 MHz	12,498,750	_____	12,501,250	Hz
2	25.0 MHz	24,997,500	_____	25,002,500	Hz
3	50.00 MHz	49,995,000	_____	50,005,000	Hz
4	50.01 MHz	49,994,999	_____	50,015,001	Hz
5	100 MHz	99,990,000	_____	100,010,000	Hz

5.4.15 Burst Gateable Oscillator Frequency Test

Step #	Frequency Set	Lo limit	Reading	Hi limit	Units
1	100 Hz	98	_____	102	Hz
2	1 MHz	980,000	_____	1,020,000	Hz
3	9.375 MHz	9,187,500	_____	9,562,500	Hz
4	18.75 MHz	18,375,000	_____	19,125,000	Hz
5	25.1 MHz	24,598,000	_____	25,602,000	Hz
6	31.0 MHz	30,380,000	_____	31,620,000	Hz
7	37.5 MHz	36,750,000	_____	38,250,000	Hz
8	43.0 MHz	42,140,000	_____	43,860,000	Hz
9	50.00 MHz	49,000,000	_____	51,000,000	Hz

5.4.16 External Trigger Frequencies Test

Step #	External trigger freq	Lo limit*	Reading	Hi limit*	Units
1	100	99.99	_____	100.01	Hz
2	50	49.995	_____	50.005	MHz

*±100 ppm limits apply when the external generator is another model 1391, otherwise apply the specified frequency accuracy limits of the external generator.

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5.4.17 Trigger Source Test

Step #	Source/Frequency	Lo limit	Reading	Hi limit	Unit
1	Internal/50 MHz	49.995	_____	50.005	MHz
2	Internal/1 MHz	0.9999	_____	1.0001	MHz
3	TTLTRG0/2 kHz	1.9998	_____	2.0002	kHz
4	TTLTRG1/3 kHz	2.9997	_____	3.0003	kHz
5	TTLTRG2/4 kHz	3.9996	_____	4.0004	kHz
6	TTLTRG3/5 kHz	4.9995	_____	5.0005	kHz
7	TTLTRG4/2 kHz	1.9998	_____	2.0002	kHz
8	TTLTRG5/3 kHz	2.9997	_____	3.0003	kHz
9	TTLTRG6/4 kHz	3.9996	_____	4.0004	kHz
10	TTLTRG7/5 kHz	4.9995	_____	5.0005	kHz
11	ECLTRG0/30 MHz	29.997	_____	30.003	MHz
12	ECLTRG1/50 MHz	49.995	_____	50.005	MHz

5.4.18 Trigger Output Mode Test

Step #	Trig line/source/Frequency	Lo limit	Reading	Hi limit	Unit
1	TTLTRG0/TRIP/12 kHz	11.9988	_____	12.0012	kHz
2	TTLTRG0/PULS/11 kHz	10.9989	_____	11.0011	kHz
3	TTLTRG1/TRIP/22 kHz	21.9978	_____	22.0022	kHz
4	TTLTRG2/TRIP/32 kHz	31.9968	_____	32.0032	kHz
5	TTLTRG3/TRIP/42 kHz	41.9958	_____	42.0042	kHz
6	TTLTRG4/TRIP/52 kHz	51.9948	_____	52.0052	kHz
7	TTLTRG5/TRIP/62 kHz	61.9938	_____	62.0062	kHz
8	TTLTRG6/TRIP/72 kHz	71.9928	_____	72.0072	kHz
9	TTLTRG7/TRIP/82 kHz	81.9918	_____	82.0082	kHz
10	ECLTRG0/TRIP/25 MHz	24.9975	_____	25.0025	MHz
11	ECLTRG0/PULSE/11 kHz	10.9989	_____	11.0011	kHz
12	ECLTRG1/TRIP/10 MHz	9.9990	_____	10.0010	MHz
13	ECLTRG1/PULSE/21 kHz	20.9979	_____	21.0021	kHz

5.4.18 Master/Slave Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1	UUT Sync to SLAVe Sync	-2.0	_____	2.0	ns
2	UUT Pulse to SLAVe Pulse	-2.0	_____	2.0	ns

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5.4.20 SUMBUS Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1	UUT lower level @ -2V	-2.10	_____	-1.90	V
2	SUMBUS 4V; UUT lower level	-1.58	_____	1.58	V
3	SUMBUS 16 V; UUT lower level	3.58	_____	8.42	V
4	Sig Gen lower level @ -2V	-2.10	_____	-1.90	V
5	SUMBUS 4V; SG lower level	-1.58	_____	1.58	V
6	SUMBUS 16 V; SG lower level	3.58	_____	8.42	V

5.4.21 PAM Input Test

Step #	Parameter	Lo limit	Reading	Hi limit	Unit
1	UUT upper level @ 5V	4.815	_____	5.185	V
2	UUT lower level @ -5V	-5.185	_____	-4.815	V
3	Bipolar 1V; UUT upper level	5.765	_____	6.235	V
4	Bipolar 1V; UUT lower level	-6.235	_____	-5.765	V
5	Negative 1V; UUT upper level	-0.085	_____	0.085	V
6	Negative 1V; UUT lower level	-6.235	_____	-5.765	V
7	Negative 1V; UUT upper level	5.765	_____	6.235	V
8	Negative 1V; UUT lower level	-0.085	_____	0.085	V

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6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned for calibration or repair, a detailed description of the specific problem and any related symptoms should be attached to the instrument. Before returning a unit to the factory, authorization from Customer Service must be obtained by calling or writing to:

Customer Service
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
FAX: (619) 565-9558

6.2 BEFORE YOU START

A list of recommended spare parts is included in the drawings section of this manual (section 7). These parts should be ordered prior to an instrument failure to minimize repair turn-around time.

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the circuit description (section 4) in conjunction with the schematics (section 7). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

The intent of this section is to provide the information required to return the instrument to proper operation. Before beginning the troubleshooting process, verify the instrument's subsystems are set correctly. For more information about instrument operation, refer to section 3 of this manual. Also, try to rule out calibration as a possible problem. Finally, inspect the instrument's wiring, and circuit boards for heat damage.

6.3 REQUIRED TEST EQUIPMENT

Table 6-1 lists required tools and test equipment for troubleshooting.

Table 6-1. List of Test Equipment and Tools

Equipment	Quantity	Specifications
VXI Requirements	1	VXI chassis
	1	VXI slot-0 controller
	1	VXI "C" size extender board (Optional-see text)
Multimeter	1	HP 3478A or equivalent
Oscilloscope	1	Tektronix 2465 or equivalent
Frequency Counter	1	HP 5334A Universal Counter
Adaptor	1	BNC female to double banana jacks
Coaxial cable	1	BNC male connectors, RG58U cable
Probe	2	10 MΩ
50Ω Termination	1	Feedthrough, 0.1% accuracy, 2W

6.4 ISOLATING A PROBLEM

Begin the troubleshooting procedure by sending `*TST?` now. In many cases, running this test will help to isolate the faulty block. Refer to Appendix D of this manual to identify the failed test. If a number other than zero is returned after running `*TST?`, refer to Table 6-2 to identify the paragraph containing the information needed to isolate the faulty circuit block and related components.

If the `*TST?` query response returns no fault even though a problem does exist, refer to Table 6-3. This table lists problems that the Self Test cannot identify.

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Table 6-2. Problems Identified By *TST?

Error Bit	Test Name	Paragraph
0	Amplitude/Offset DAC	6.5.1
1	Trailing Edge DAC	6.5.2
2	Leading Edge DAC	6.5.3
3	Limit Amplifier	6.5.4
4	SUMBUS	6.5.5
5	Delay Gatable Oscillator	6.5.6
6	Width Gatable Oscillator	6.5.7
7	25-50 MHz Gatable Oscillator	6.5.8
8	–	–
14	Bus Error	6.5.9

Table 6-3. Problems Not Identified By *TST?

Problem	Paragraph
Abnormal LED State	6.5.10
Pulse Board Digital Interface	6.5.11
AutoCal/Built-In-Test	6.5.12
Frequency Reference	6.5.13
Frequency Synthesizer	6.5.14
TRIG IN	6.5.15
Trigger Source Selector	6.5.16
TTL/ECL Triggers to Backplane	6.5.17
TTL/ECL Triggers from Backplane	6.5.18
Mode Control Logic/Burst Counter	6.5.19
SYNC OUT Selector and Driver	6.5.20
Amplitude Control and Multiplier	6.5.21
PAM IN	6.5.22
Transition Time Generator	6.5.23
Trapezoid Shaper	6.5.24
Output Power Supplies	6.5.25
Output Amplifier/PULSE OUT	6.5.26

6.5 TROUBLESHOOTING

The following procedures require that the Model 1391 be part of a VXI system as described in table 6-1. The Model 1391 will be installed on a C-size VXI extender card and controlled by the Resource Manager. The computer/display device can be the Resource Manager or an external host connected to the Resource Manager via the IEEE-488 (GPIB) programming bus.

WARNING

With the covers removed, low voltage dc power supplies are exposed. Do not be misled by the term "low voltage". Under adverse conditions, potentials as low as 50 volts can cause serious injury or death.

WARNING

With the module on an extender card and the covers removed, no chassis cooling air is moving across the components. The Pulse Generator has many high-speed digital logic devices and discrete analog circuits which require some cooling air for continuous operation. Do not operate the module in this configuration for more than a few minutes without directing some cooling air across the face of the Main Pulse Board and the Amplifier Board using an external utility fan. Avoid burns - do not come into direct contact with components in the module.

CAUTION

Do not disconnect or remove any board assemblies unless the module is removed from chassis power. Some board assemblies contain devices that can be damaged if the board is removed or replaced with the power on. Several components, including MOS devices, can be damaged by electrostatic discharge. Use conductive foam and grounding straps when servicing is required around sensitive components. Use care when unplugging ICs from high-grip sockets.

NOTE

If possible, take all measurements with only the controller and Model 1391 Pulse Generator in the chassis. Unless otherwise stated, terminate PULSE OUT (and SYNC OUT connector if that circuit is being tested) into 50Ω.

When taking waveform readings within the instrument, always use a X10 probe with short ground lead to prevent loading and reduce the amount of waveform ringing.

6.5.1 Amplitude DAC Error Bit 0

Instrument Setup: RESET

This test verifies the amplitude control voltage to the multiplier circuitry. The test sets the amplitude DAC to minimum and measures control voltage. A failure will occur when the measured voltage is outside of ±0.1 volts. The test then sets the amplitude control

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DAC to maximum and again measures the control voltage. A failure will occur if the control voltage is less than 0.798 volts or greater than 1.298 volts. A failure may be caused by U93, U94, or U89, and their associated circuitry.

8.5.2 Trailing Edge DAC Error Bit 1

Instrument Setup: RESET

This test verifies the trailing edge current source circuitry. The test sets the trailing edge DAC to minimum and measures the current source feedback voltage. A failure will occur when the measured voltage is greater than 0.25 volts. The test then sets the trailing edge DAC to maximum, and the TE<10ns line to 0 and measures the feedback voltage. A failure will occur if the voltage is less than 3.371 volts or greater than 4.071 volts. The test then sets the TE<10ns line to 1, and remeasures the feedback voltage. A failure will occur if the voltage is less than 2.761 volts or greater than 3.361 volts. A failure may be caused by U89, U96, U94, Q38, and their associated circuitry.

8.5.3 Leading Edge DAC Error Bit 2

Instrument Setup:

```
RESET
```

This test verifies the leading edge current source circuitry. The test sets the leading edge DAC to minimum and measures the current source feedback voltage. A failure will occur when the measured voltage is greater than ±0.25 volts. The test then sets the leading edge DAC to maximum, and the LE<10ns line to 0 and measures the feedback voltage. A failure will occur if the voltage is less than -4.089 volts or greater than -3.389 volts. The test then sets the LE<10ns line to 1, and remeasures the feedback voltage. A failure will occur if the voltage is less than -3.3006 volts or greater than -2.706 volts. A failure may be caused by U89, U96, U94, Q39, and their associated circuitry.

8.5.4 Limit Amplifier Error Bit 3

Instrument Setup:

```
RESET
```

This test monitors the limiter clamp voltages. The midpoint of the two voltages is nominally zero volts. A failure will occur if the voltage is outside of ±0.150 volts. A failure may be caused by U97 and its associated circuitry.

8.5.5 SUMBUS Error Bit 4

Instrument Setup:

```
RESET
```

This test measures the SUMBUS driver output. This voltage is nominally zero volts. A failure will occur if the voltage is greater than ±0.05 volts. A failure may be caused by R196 or R232 being misadjusted. Verify that the voltage on pin 5 of output amplifier connector P1 is 0 ± 0.002 volts, if not follow the calibration procedure adjusting the amplitude limiter offset and the preamplifier offset.

These adjustments are described in the alignment procedure steps 5 and 6. The procedure for adjusting R196 is described in the alignment procedure step 11. This adjustment should be made only after the adjustment of steps 5 and 6 have been made. If the adjustment of R196 cannot be made, the problem can be isolated by measuring the voltage of the ODAC signal. This signal should be approximately 0 volts ± 0.1 volts. If not, the output amplifier, or offset control circuitry should be suspected. The next step is to measure the voltage across R191. It should be about 9.1 volts. If not CR66, Q55, and U105 and associated components should be suspected. The voltage across R192 should then be checked. It should be about 6 volts. If not, Q56, CR65, and U105 and associated components should be suspected.

8.5.6 Delay Gatable Oscillator Error Bit 5

Instrument Setup:

```
FREQ 1e3;VOLT 5;PULS:WIDT
250e-6;:DEL 125e-6;:FUNC
PULSE;:TRIG:SOUR BUS;COUN
50;:INIT:CONT OFF;:DIAG:REG
<value>
```

This test routes the delay one-shot output flip-flop to the Autocal measurement system. The DIAGnostic SCPI Subsystem routes signals and data to the Autocal system, and is used in factory level diagnostics. A failure will occur if the measured delay is less than 100 µs, or greater than 150 µs. A fault may be isolated by referring to Figure 6-1 Delay One-Shot Troubleshooting Flowchart.

8.5.7 Width Gatable Oscillator Error Bit 6

Instrument Setup:

```
FREQ 1e3;VOLT 5;PULS:WIDT
250e-6;DEL 125e-6;:FUNC
PULSE;:TRIG:SOUR BUS;COUN
50:INIT:CONT OFF
```

This test routes the width one-shot output flip-flop to the autocal measurement system. A failure will occur if the measured width is less than 200 µs, or greater than 350 µs. A fault may be isolated by referring to Figure 6-2 Width One-Shot Troubleshooting Flowchart.

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6.5.8 25-50 MHz Gatable Oscillator Error Bit 7

Instrument Setup:

```
FREQ 666.7:VOLT 5;FUNC
SQUARE;:TRIG:SOUR BUS;COUN
50;:INIT:CONT OFF
```

This test routes the output of the gatable oscillator to the autocal measurement system. The gatable oscillator produces a pulse with a width of 749.9625 µs (0.5 * 1 / 666.7 Hz). The average width of 50 cycles is measured. A failure will occur if the average width is less than 700 µs or greater than 800 µs. A fault may be isolated by referring to Figure 6-3 Gatable Oscillator Troubleshooting Flowchart.

6.5.8 Bus Error Error Bit 14

The Bus Error bit will be set if the main board fails to assert the DTACK\ signal after writing to the main board. If this failure occurs, U2 or U112 should be suspected.

6.5.10 Abnormal LED State

The VXI Interface board controls each front panel LED. The LED states may be used to isolate faults in the VXI interface and the main board.

RUN LED

The RUN LED should be illuminated continuously, indicating that the Interface board CPU is operational.

FAIL LED

The FAIL LED should be extinguished, except during the first 5 seconds after power up. If the LED is on after system power on, the interface board was either not able to initialize it's configuration registers or it failed it's own self test. This should not be confused with the Self Test of the main board. If the FAIL LED is illuminated, the interface board is not operational.

MODID LED

The MODID LED flashes on momentarily during power up. This may be too short in duration to be seen.

A16 LED

The A16 LED flashes on while the VXI Interface Board is being addressed by the VXIbus.

A24 LED

The A24 LED is illuminated during a VMEbus access to the A24 shared memory.

Troubleshoot the LEDs as follows.

1. Verify that the 1391 module is in fact non-operational in the chassis. If the 1391 module is operational, but the RUN LED is extinguished, troubleshoot the LED and the RUN_LED\ signal (refer to sheet 1 of the main board schematic).
2. If the 1391 module is non-operational, the fault may be in the interface board or the main board. To isolate the problem power down the system, remove the 1391 module, remove the left side panel and then the VXI interface board. Plug the Interface board directly on to the P1 and P2 connectors of the VXI chassis and reboot the system. Check the module status using the host computer. If the interface board is operational, it will identify itself normally in it's slot as a Wavetek Model 1391. A SYSTem:ERRor? query will return an error message, but this is because the interface board does not receive a DTAC\ response with the main board removed. If the interface board is still non-operational, call Wavetek customer service at (619) 279-2200 to arrange repair.
3. If the interface board is operational, reinstall it in the module and troubleshoot the interconnect signals on the P4 through P7 connectors on the main board (refer to main board schematic diagram sheet 1).
4. If the RUN and FAIL LEDs are operating normally, troubleshoot the remaining LEDs (refer to main board schematic sheet 1).

6.5.11 Pulse Board Digital Interface

Problems in the digital interface may be isolated by checking the functionality of the various circuit blocks of the unit. As it is very difficult to document the states of all of the control lines for all functions frequencies and modes, the best way to troubleshoot the digital interface is to look at the logic levels of the signals.

Do they wiggle between logic low and high?
Are they stuck low or high?
Are they someplace between low and high?

6.5.12 AutoCal/Built-In-Test

Problems in the voltage measuring portion of the Autocal/built in test circuitry may be isolated by measuring the voltages at the inputs of the ADC buffers and comparing these voltages to those on the outputs of the buffers. The voltages should be within about 10 mV of each other. The 4 MHz clock signal 4MHZCLK should be measured. If everything is correct, U109 should be suspected.

Problems in the period measuring portion of the Autocal/built in test circuitry may be isolated by measuring the 2 MHz reference signal, 2MHZREF. If this signal is bad or missing, the CLK10 signals from the VXIbus backplane should be traced out to U112. If everything is correct, U112 should be suspected.

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6.5.13 Frequency Reference

The frequency reference for the Model 1391 is provided by the VXI controller. The controller provides a precise 10 MHz differential ECL signal to the backplane. The backplane distributes the signal to each slot, via individual buffers. If the frequency reference is suspected, the module should first be tried in another slot to determine if the problem is due to the backplane. If the fault follows the module position, the CLK10+ and CLK10- signals from the P2 connector should be traced through the interface board to the main board and up to U21.

6.5.14 Frequency Synthesizer

Problems in the basic operation of the frequency synthesizer can be determined by observing the UNLOCK LED (DS5) on the main board. The LED is visible through the hole in the top of the synthesizer shield.

The UNLOCK LED is normally extinguished, indicating the loop is locked. The LED will momentarily flash when a large step change in frequency is programmed. Refer to Figure 6-4 Frequency Synthesizer Troubleshooting Flowchart to isolate a synthesizer fault.

6.5.15 TRIG IN

Problems in the trigger input circuitry can easily be isolated by applying a triggering signal to the TRIG IN BNC connector and monitoring TP11 on the main board. The duty cycle of the waveform at TP11 should change with the programmed trigger level. The trigger level control voltage TDAC should swing from about zero to about 4.5 volts as the trigger level, is programmed from +10 volts to -10 volts. If the TDAC signal is not present or incorrect, U87 and U90 should be suspected. If no waveform is present at TP11, U34 and U36 should be suspected.

6.5.16 Trigger Source Selector

Problems in the trigger source selector circuitry can be isolated by applying an external triggering signal to the TRIG IN BNC connector, selecting external trigger and monitoring TP12. Changing the trigger slope will invert the signal at TP12. The trigger source is selected by the TRG_SRCA, TRG_SRCB, and TRG_SRCC signals. The states of these signals for each trigger source is shown in table 6-4. If the control data is corrupted, U18 should be suspected.

Table 6-4. Trigger Source Selector Control Lines.

Trigger Source	TRG_SRCC	TRG_SRCB	TRG_SRCA
VXI ECL TRG0	0	1	0
VXI ECL TRG1	0	1	1
VXI TTL TRGn	1	0	1
Software Trigger	1	0	0
Internal Trigger	0	0	0
External Trigger	0	0	1

6.5.17 TTL/ECL Triggers to Backplane

A second Model 1391 is useful to troubleshoot the TTL/ECL triggering signals to the backplane. The unit under test should be programmed to drive each trigger line in turn while the second Model 1391 is programmed to receive the trigger from the backplane. If only one or two TTL trigger lines are inoperable, U15, U39, and U40 should be suspected. If all of the TTL trigger lines are inoperable, U18, U42, and U92 should be suspected in addition to U15, U39, and U40. If ECL-TRG0 is inoperable, U17, U62, U98, and U113 along with U44 on the interface board should be suspected. If ECLTRG1 is inoperable, U17, U91, U98, and U113 along with U44 on the interface board should be suspected.

6.5.18 TTL/ECL Triggers from Backplane

A second Model 1391 is useful to troubleshoot the TTL/ECL triggering signals from the backplane. The second 1391 should be programmed to drive each trigger line in turn while the unit under test is programmed to receive the trigger from the backplane. If only one or two TTL trigger lines are inoperable, U15 and U38 should be suspected. If all TTL trigger lines are inoperable, U35 and U37 should also be suspected. If either of the ECL trigger lines are inoperable, U29 and U37 along with U43 on the interface board should be suspected.

6.5.19 Mode Control Logic/Burst Counter

Problems in the mode control logic for burst mode may be isolated by programming the unit under test as follows, and then following Figure 6-5 Burst Mode Troubleshooting Flowchart:

```
FREQ 2e4;FUNC SQU;:INIT:CONT
OFF;:TRIG:GATE OFF;TIM 1e-3;
COUN 40
```


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6.5.20 SYNC OUT Selector and Driver

Problems in the Sync selector and driver can be isolated by programming the unit under test as follows, and then following Figure 6-6 Sync Selector Troubleshooting Flowchart:

```
FREQ 1e3;FUNC SQU;MARK ON;
VOLT 10
```

The states of the sync selector control lines are shown in table 6-6.

The signal path for the Gate Type of sync can be troubleshot by programming the unit under test as follows, and then following Figure 6-6 Sync Selector Troubleshooting Flow Chart:

```
FREQ 2e4;MARK ON;MARK:TYPE
GATE;:TRIG:COUN 10;TIM 1e-3;
SOUR INT;:INIT:CONT OFF
```

Table 6-5. Sync Selector Control Lines.

Sync Function	SYNC_SEL3	SYNC_SEL2	SYNC_SEL1
Off	0	0	0
Single Pulse	0	1	0
Double Pulse	0	1	1
Square	0	0	1
> 50 MHz	1	0	0

Sync Type	SYNCTYPE
Clock	0
Gate	1

6.5.21 Amplitude Control and Multiplier

Problems in the amplitude control and multiplier circuitry can be isolated by programming the unit under test as follows:

```
FREQ 1e3;VOLT 16;FUNC SQU
```

TP26 should measure about + 1 volt. If not, U89 and U93 should be suspected. The input of the multiplier, pin 8 of U101, should be a 1 Vpp square wave. If not the trapezoid shaper circuitry should be suspected. Pin 6 of U102 should be monitored for about a 2Vpp square wave. If not U101 and U102 should be suspected. Pin 6 of U100 should be monitored for about a 5.2 Vpp square wave. If not, U100 should be suspected.

6.5.22 PAM IN

Problems in the PAM IN circuitry can be isolated by removing the output amplifier and programming the unit under test as follows:

```
VOLT 10;FREQ 1e3;FUNC SQU;
PULM ON
```

A 1 Vpp square wave should be applied to the PAM IN BNC connector. Pin 7 of U93 should be monitored for a 1Vpp square wave. If not, U93 should be suspected. Pin 10 of U94 should then be monitored for a 1 Vpp square wave. If not U11 and U94 should be suspected. TP26 should be monitored for a 1Vpp square wave with a positive DC offset. If not, U93 should be suspected.

6.5.23 Transition Time Generator

Problems in the transition time generator may be isolated by programming the unit under test for:

```
VOLT 10;FREQ 1e3;FUNC SQU;
PULS:TRAN:STAT ON;TRA:AUTO ON
```

U98 pins 9 and 10 should be monitored for a 1kHz ECL level square wave. If no square wave is present, the width one-shot circuitry should be suspected. U98 pins 6 and 7 should then be monitored for ECL level square waves. If no square wave is present U98 should be suspected. The bases of Q41 and Q42 should be monitored for square waves that swing between about -2.3 and -3.2 volts.

If the square waves are not present, CR45 and CR46 should be suspected. The collector of Q42 should be monitored for about a 3Vpp square wave symmetrical about ground. If no square wave is present, Q41-Q43 should be suspected. The top of C106 should then be monitored for a 1.5 Vpp square wave, symmetrical about ground. If no square wave is present Q44 - Q47 and associated components should be suspected. The selection of timing capacitor for each range of transition times is shown in table 6-6.

Table 6-6 Transition Timing Range Capacitor Selection

Transition Range	Timing Capacitors
4.5 ns - 17 ns	C106
10 ns - 1.27 µs	C106 + C107
88 ns - 12 µs	C106 + C108
800 ns - 120 µs	C106 + C109
900 ns - 130 µs	C106 + C107 + C108 + C109

Note: Range changes are approximate and depend on calibration.

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8.5.24 Trapezoid Shaper

Problems in the trapezoid shaper may be isolated by programming the unit under test as follows:

```
FREQ 1e3;VOLT 10;FUNC SQU
```

Pin 3 of U99 should be monitored for a 1.5 Vpp square wave. If not, the transition generator should be suspected. TP37 should be monitored for a 3.2 Vpp square wave. If not U99 should be suspected. Pin 8 of U101 should be monitored for a 1 Vpp square wave. If not, the unit should be powered down and the output amplifier removed. Power should then be reapplied and the unit reprogrammed to the above state. The voltages on Q34 pins 6 and 4 should be monitored for +18 volts and -18 volts respectively. If not Q34 and U11 should be suspected.

8.5.25 Output Power Supplies

Problems in the output amplifier power supplies may be isolated by removing the output amplifier board and powering up the unit. The voltages at J12 pins 2 and 14 should be about ±36 volts. These voltages will drop to about ±30 volts with the output amplifier installed. If the voltages are correct without the output amplifier installed, the problem is probably in the output amplifier. If the unloaded voltages are incorrect, the voltage on L2 should be measured.

If the voltage is not about 12 volts, Q51 or Q52 may be shorted. The drains of Q51 and Q52 should swing between zero and about 12 volts at about 50 KHz with a symmetry of about 60/40, if not U118, Q51, and Q52 should be suspected. If the voltage at J12 pin 2 is about +24 volts CR37 should be suspected. Similarly if the voltage at J12 pin14 is about -24 volts CR38 should be suspected.

8.5.26 Output Amplifier/PULSE OUT

Problems in the output amplifier can be isolated by first programming the unit under test as follows:

```
FREQ 1e3;VOLT 10;FUNC
SQU;VOLT:OFFS 0;:OUTP ON
```

The voltages on output amplifier connector J1 should be as shown in Table 6-7. If the voltages are not correct, the associated main board circuitry should first be troubleshot and the problems corrected before proceeding. The voltages on output amplifier TP2 and TP3 should be about +12 and -12 volts respectively. If not U1, U2, and U3 should be suspected. If the amplifier's output is stuck high, TP4 should be about +10 volts, if not U3 should be suspected. The voltages on the collectors of Q8 and Q9 should be measured. They should be about ±28 volts. If not, circuit protector CB1 or CB2 may have tripped. Transistors Q8 and Q9 should then be checked for shorts.

Table 6-7 Output Amplifier Voltages

J1 Pin No.	Voltage
1,4,6,8,9,10,12,15	0 volts
2,3	~+30 volts
5	~ 3.24 Vpp Square wave
11	0 ±0.050 volts
13,14	~-30 volts

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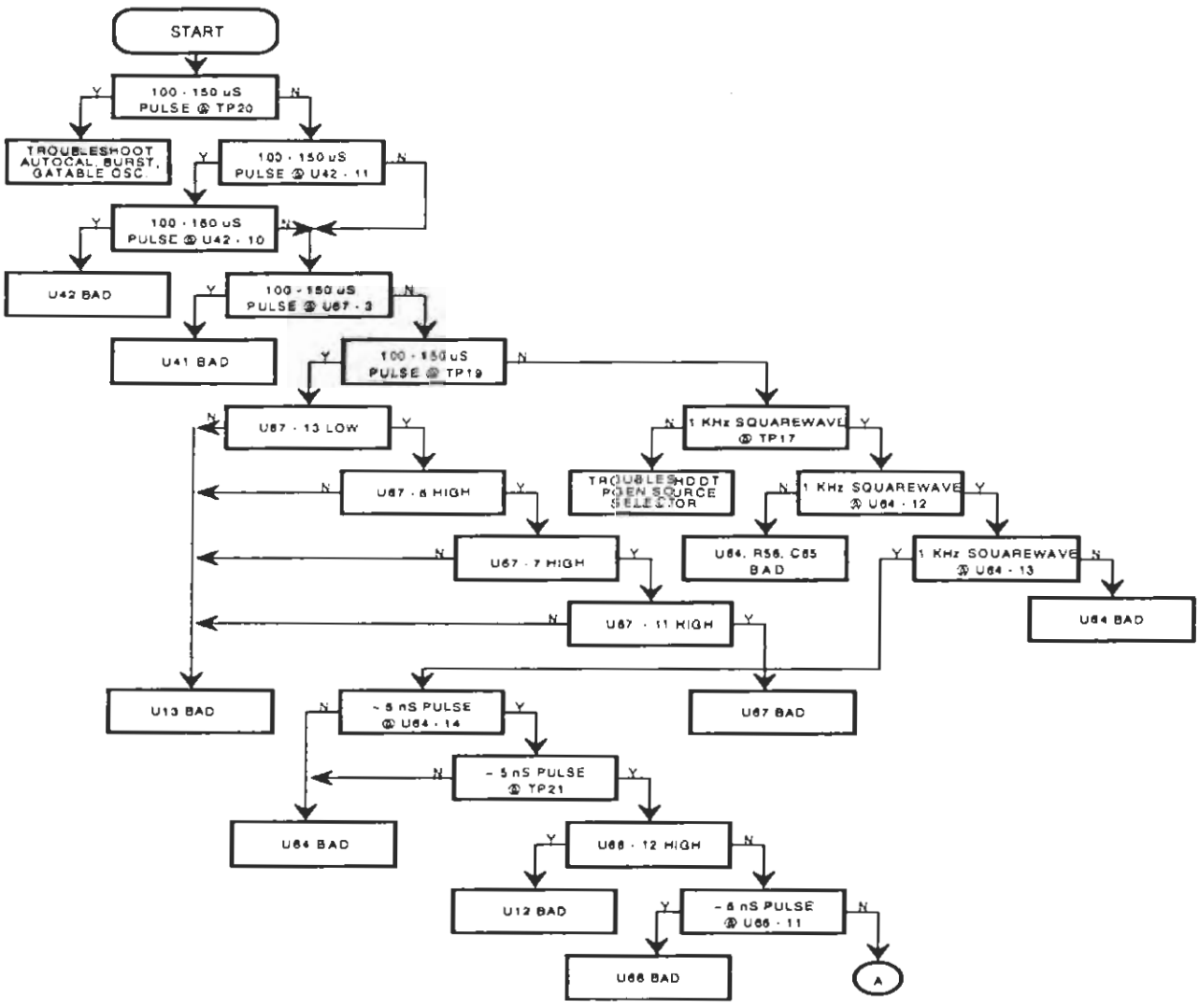


Figure 6-1. Delay One-Shot Troubleshooting Flow Chart

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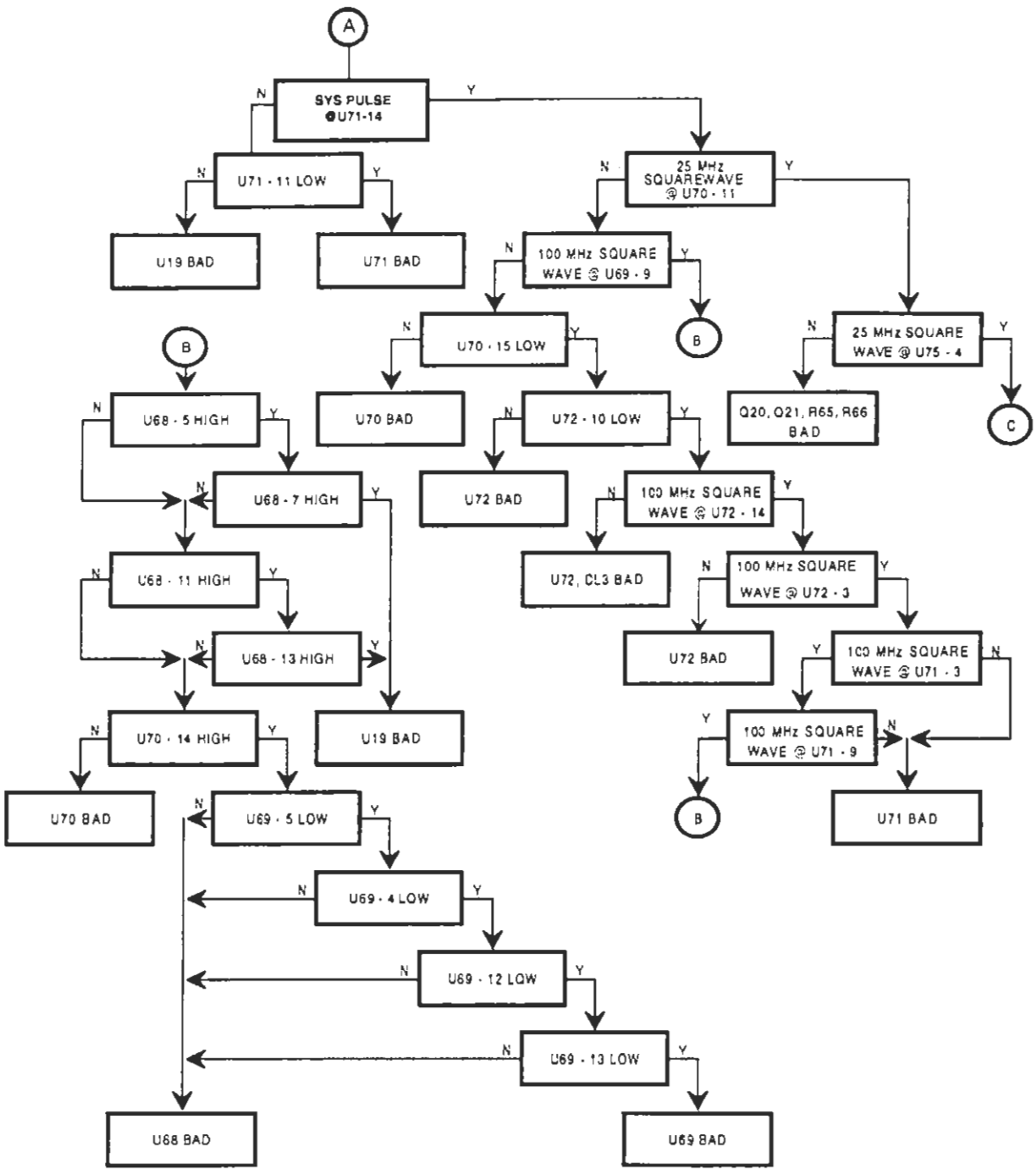


Figure 6-1 (Cont'd). Delay One-Shot Troubleshooting Flow Chart

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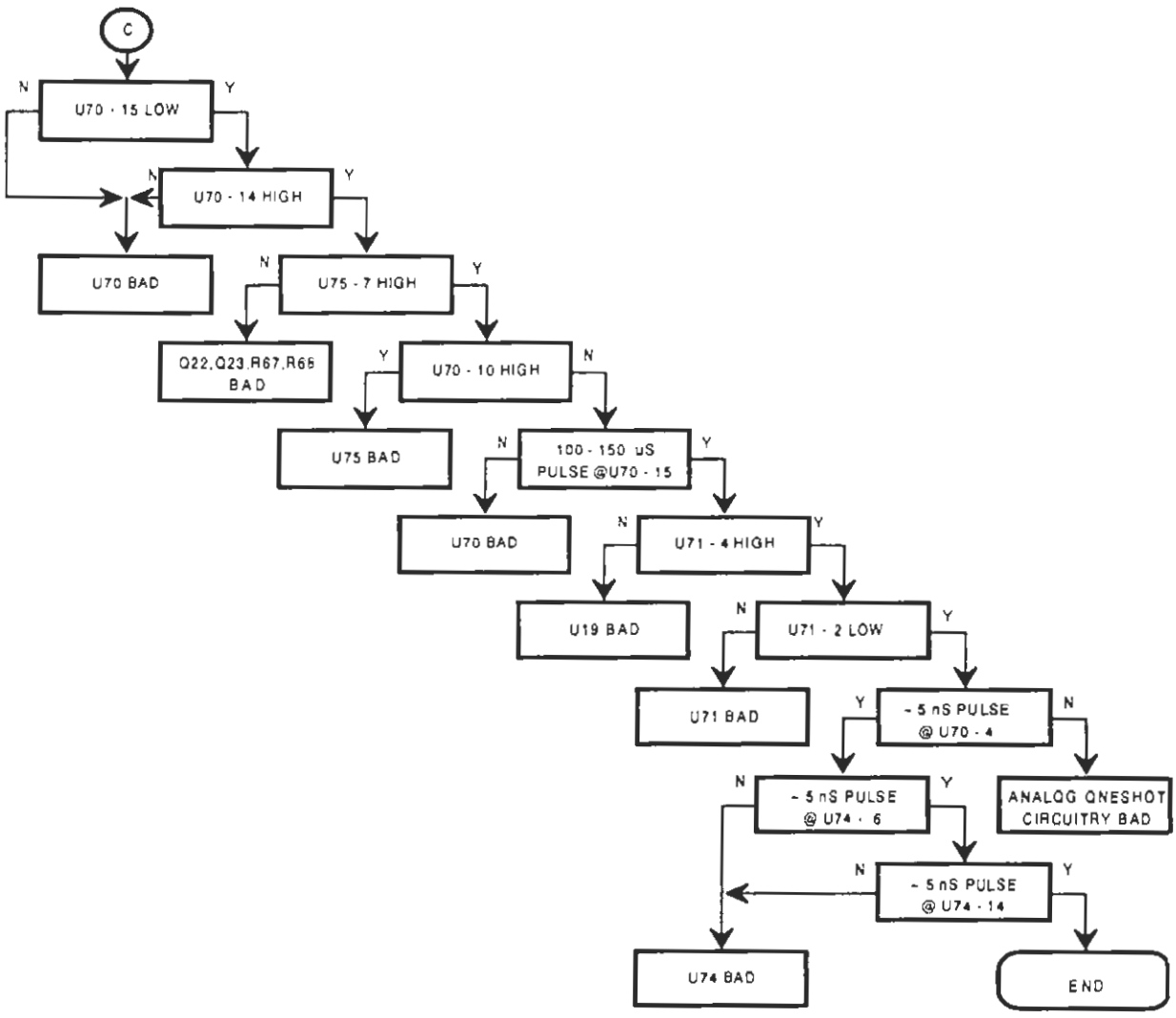


Figure 6-1 (Cont'd). Delay One-Shot Troubleshooting Flow Chart

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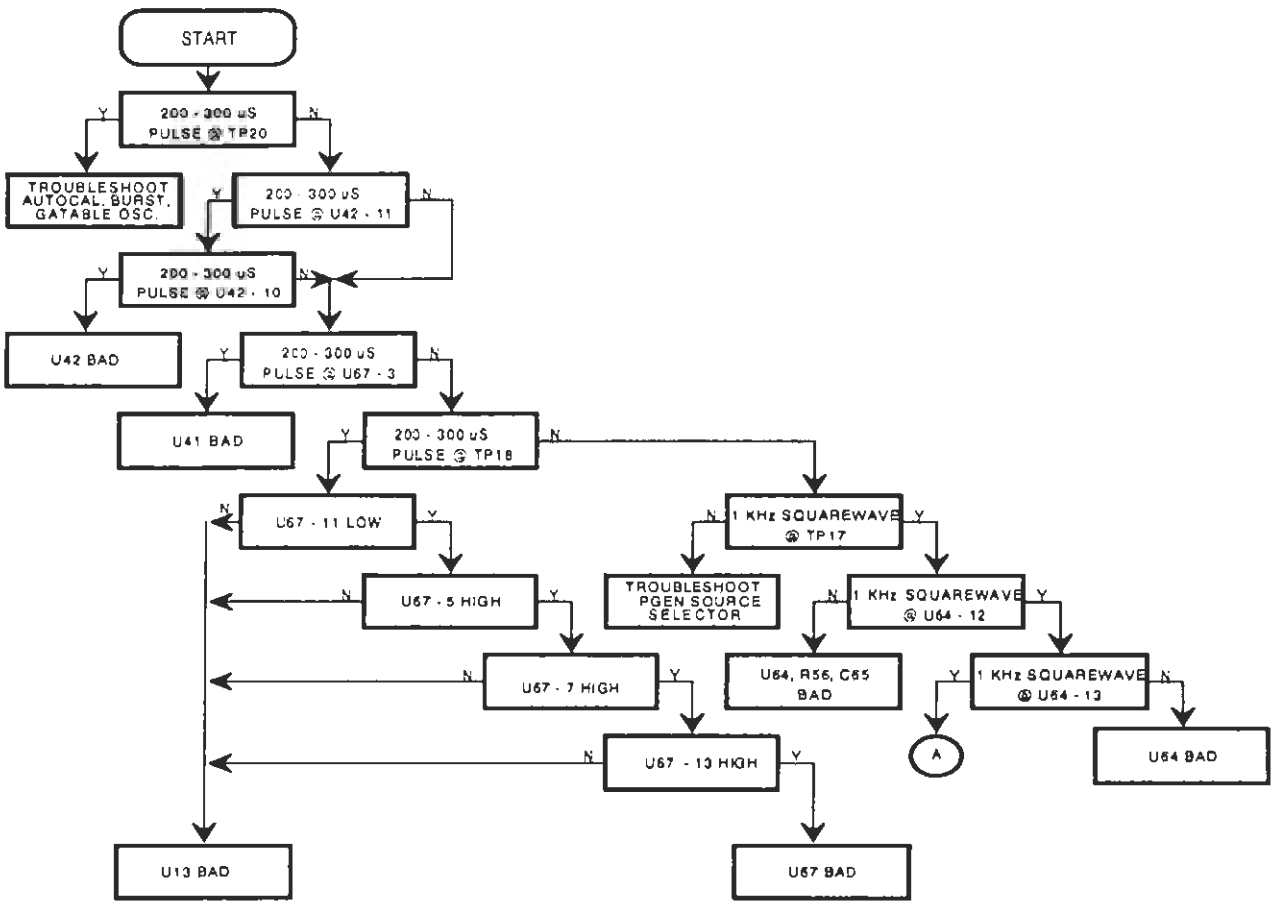


Figure 6-2. Width One-Shot Troubleshooting Flow Chart

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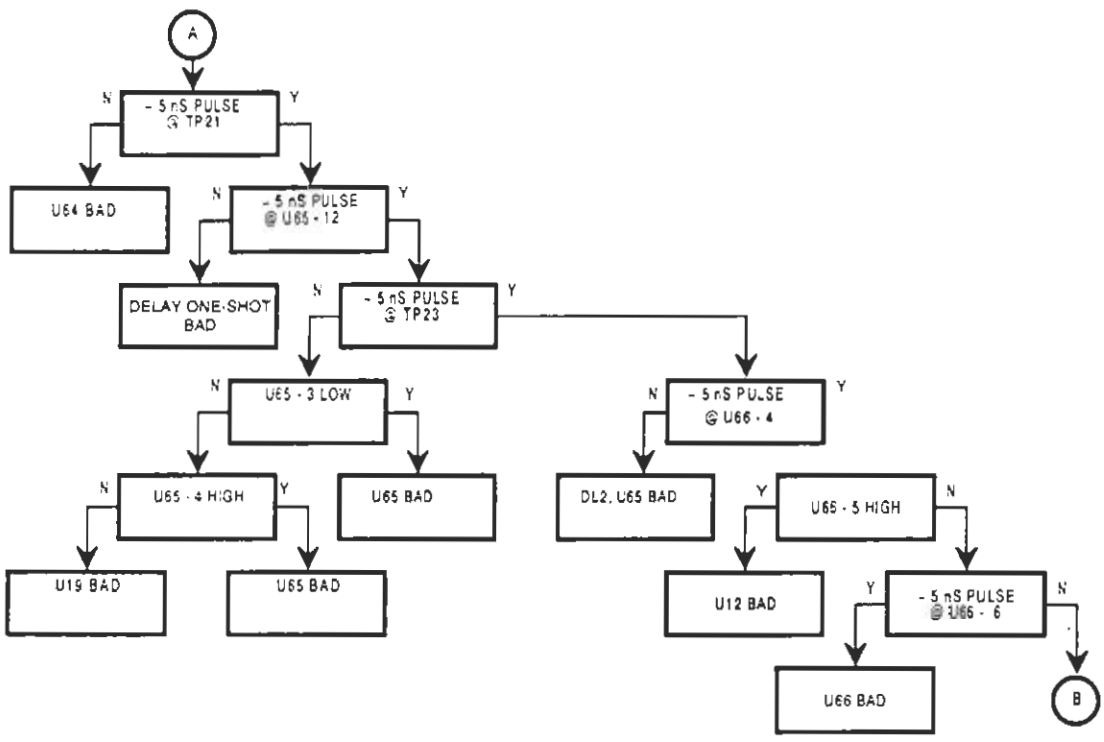


Figure 6-2 (Cont'd). Width One-Shot Troubleshooting Flow Chart

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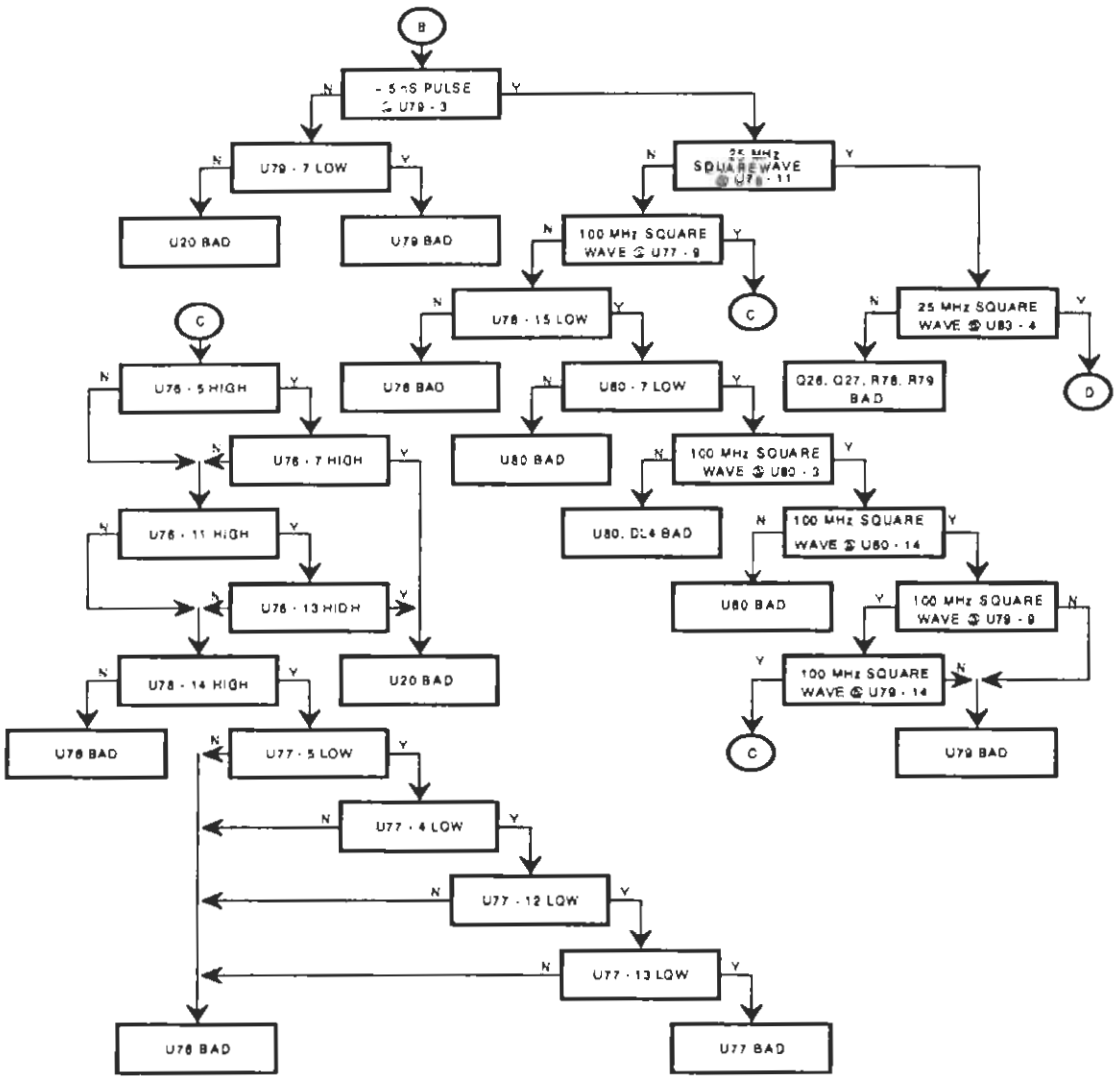


Figure 6-2 (Cont'd). Width One-Shot Troubleshooting Flow Chart

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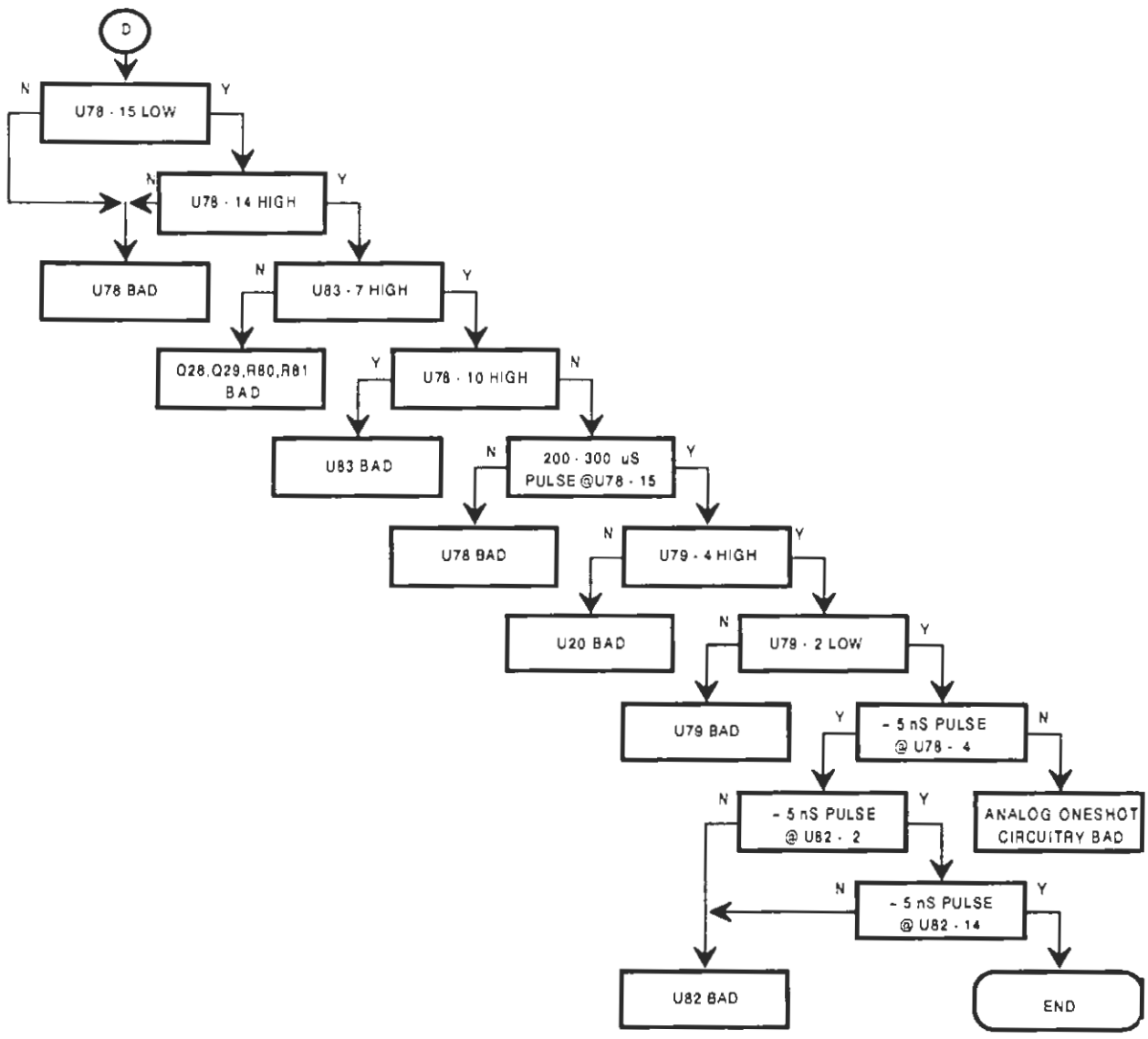


Figure 6-2 (Cont'd). Width One-Shot Troubleshooting Flow Chart

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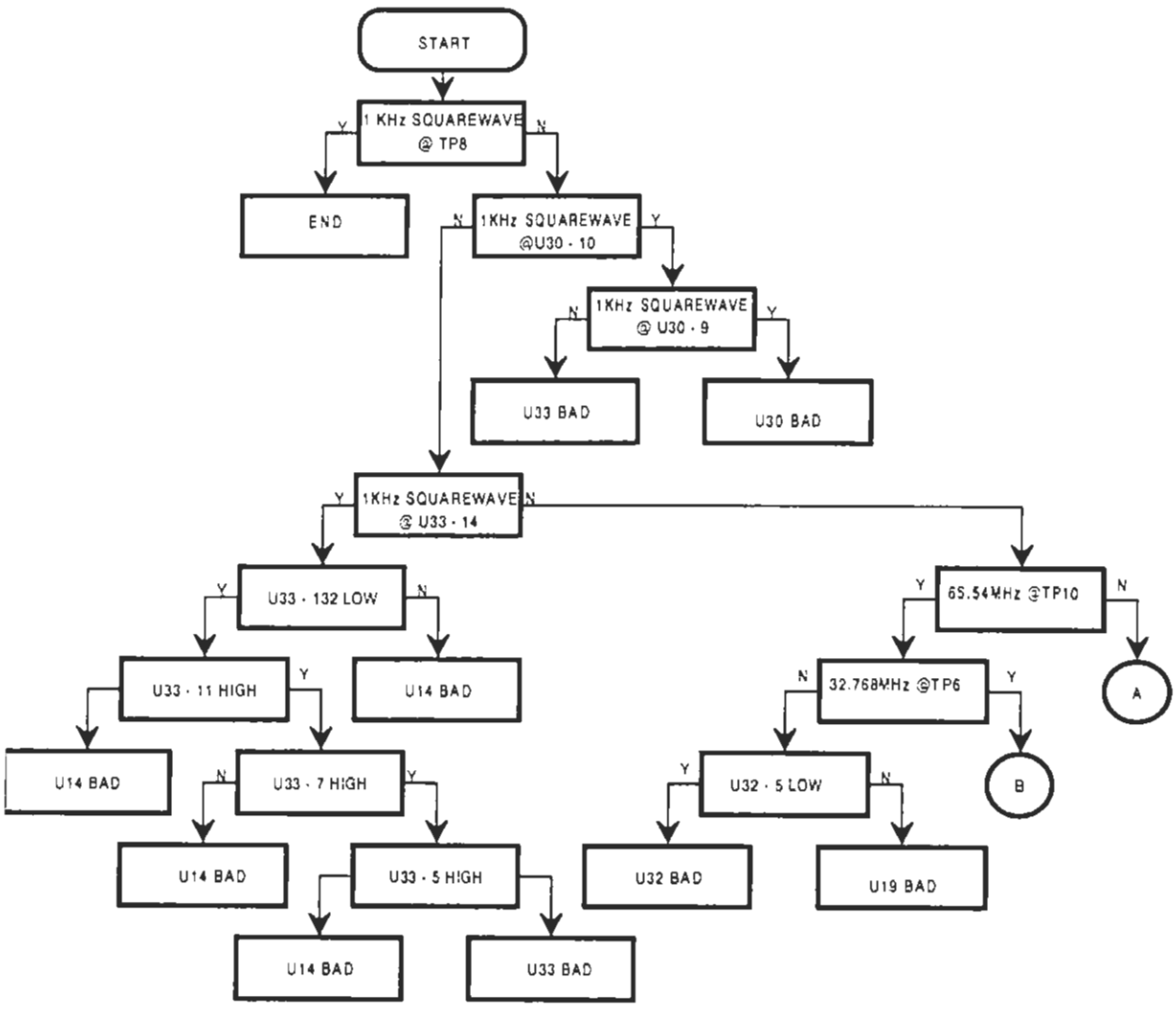


Figure 6-3. Gatable Oscillator Troubleshooting Flow Chart

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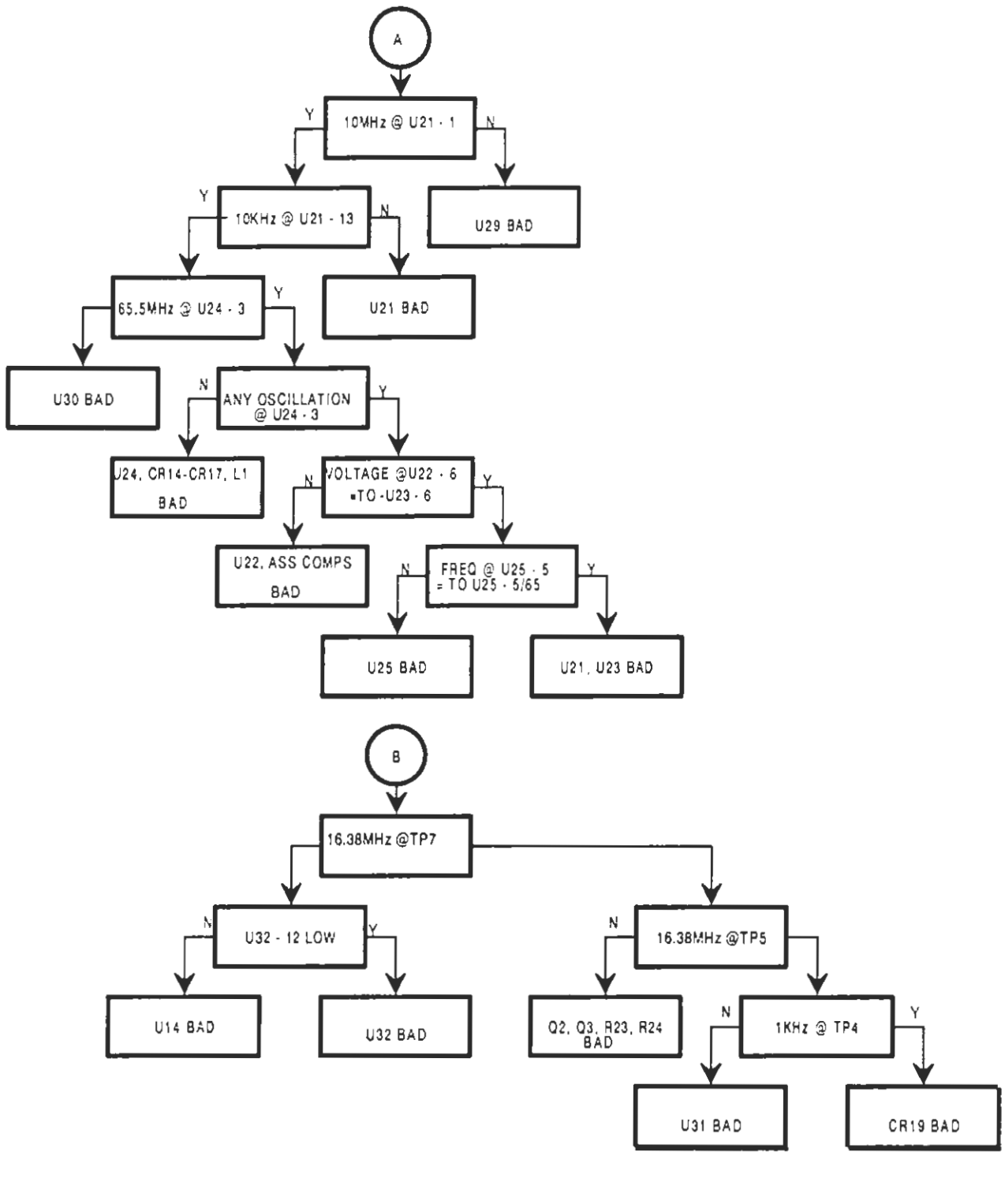


Figure 6-3 (Cont'd). Gatable Oscillator Troubleshooting Flow Chart

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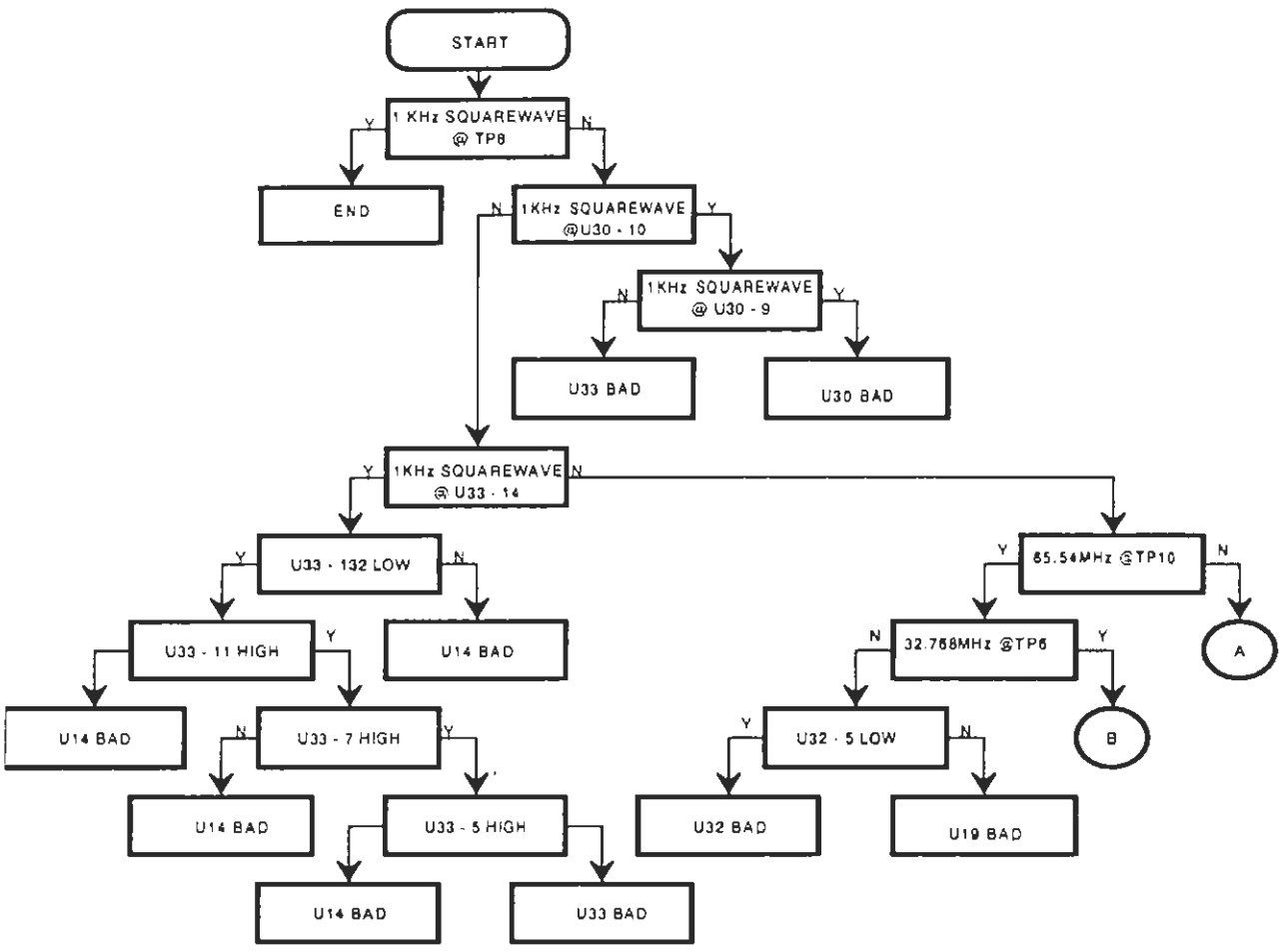


Figure 6-4. Frequency Synthesizer Troubleshooting Flow Chart

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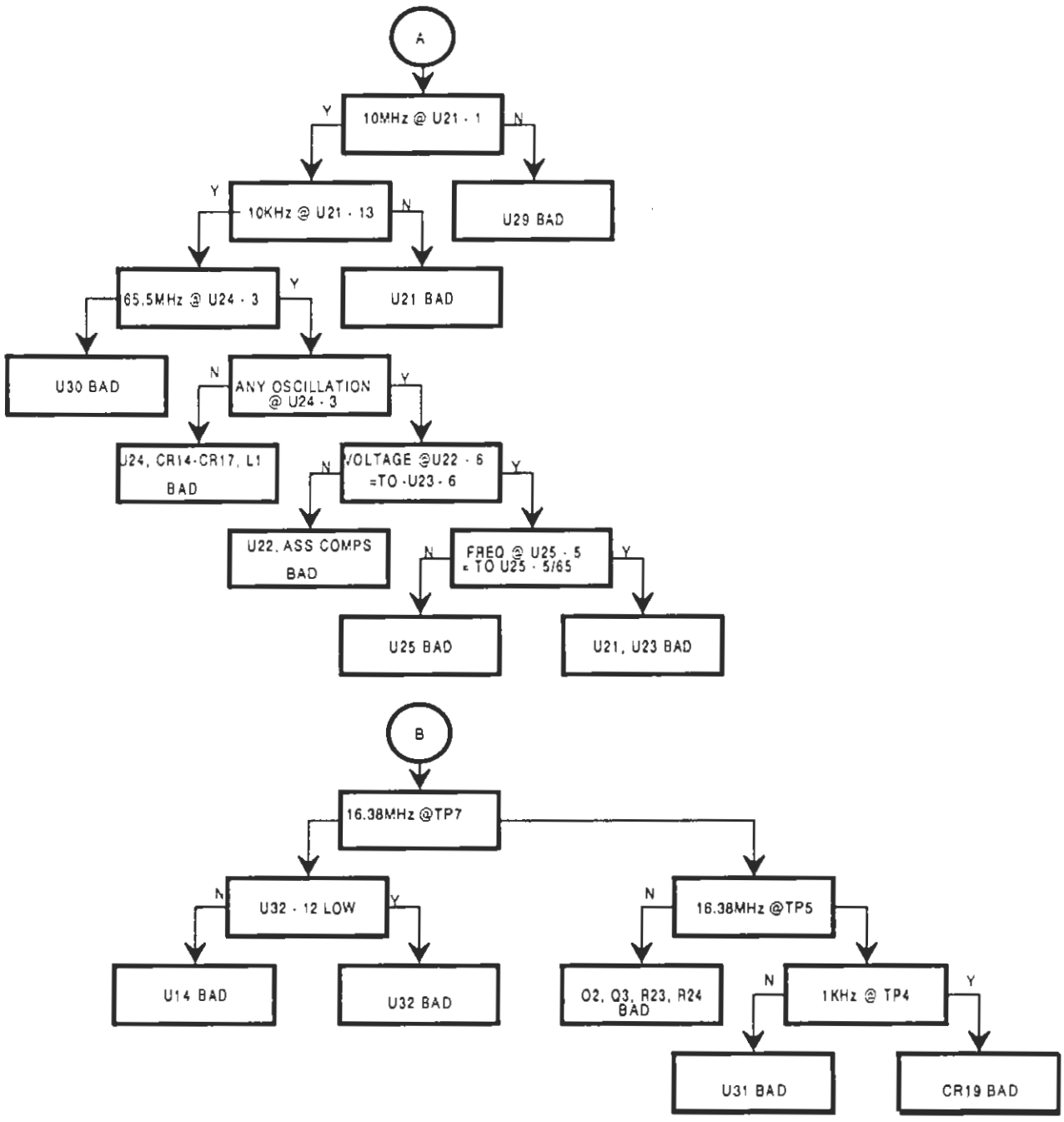


Figure 6-4 (Cont'd). Frequency Synthesizer Troubleshooting Flow Chart

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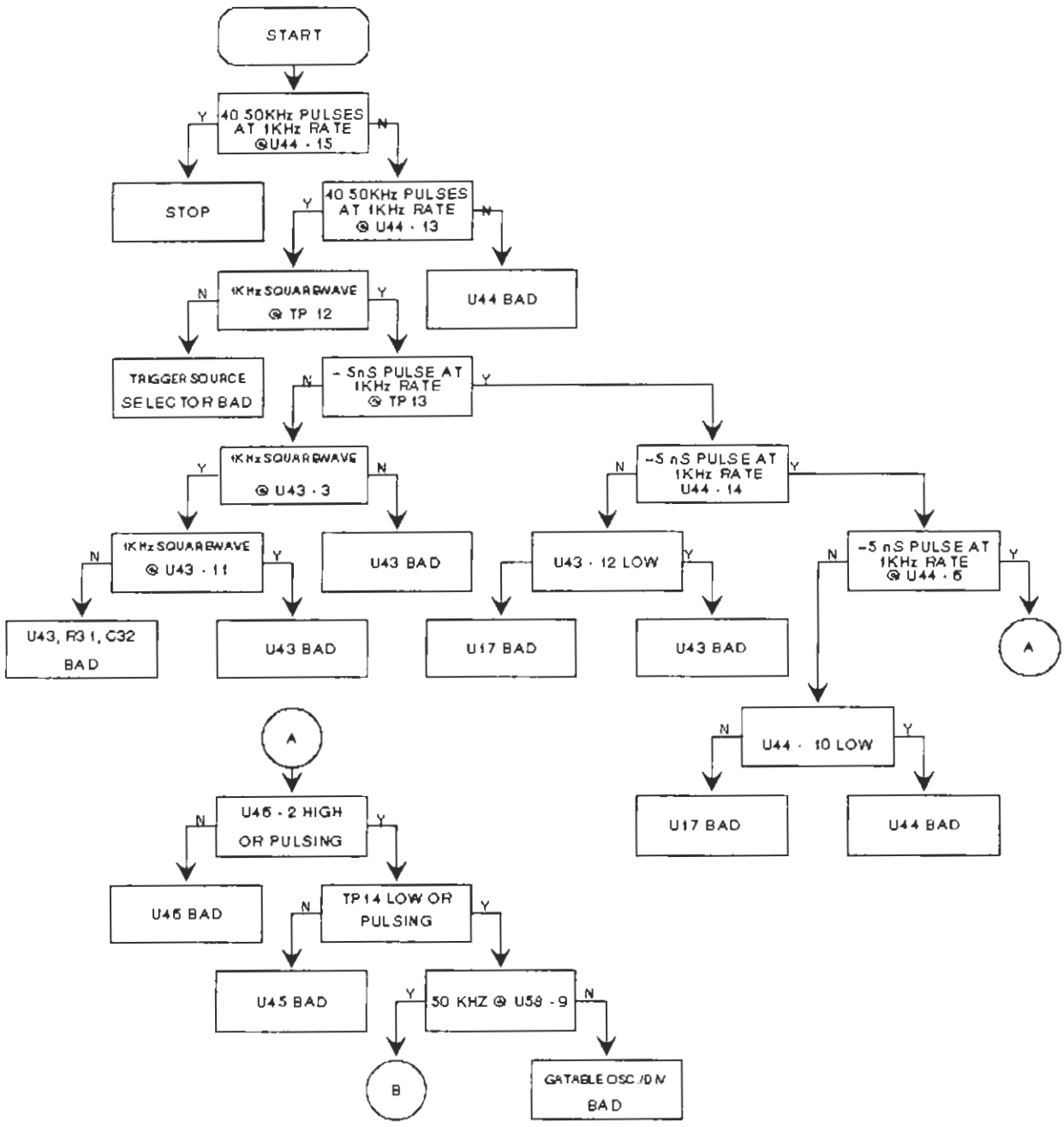


Figure 6-5. Burst Mode Troubleshooting Flow Chart

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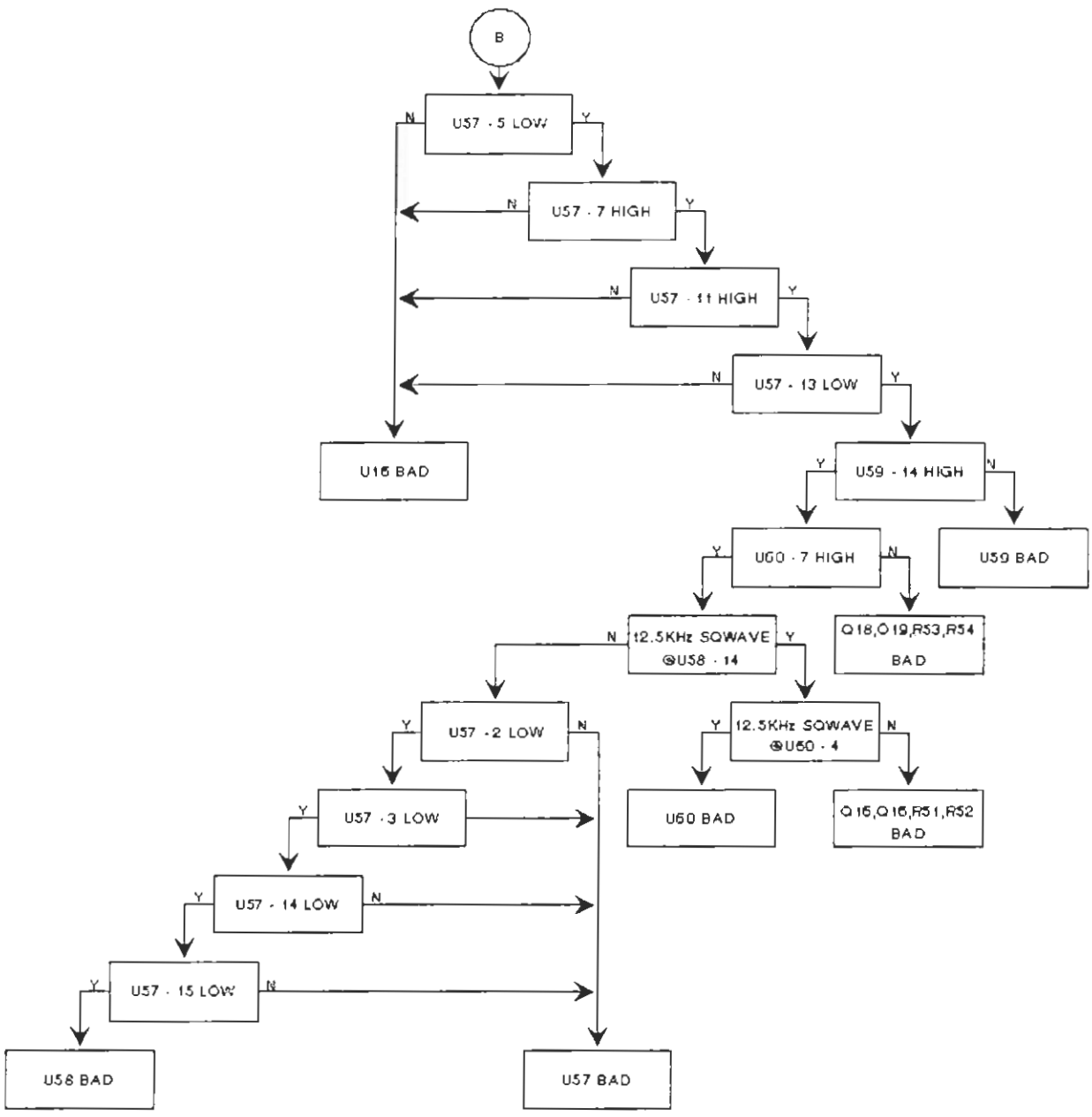


Figure 6-5 (Cont'd). Burst Mode Troubleshooting Flow Chart

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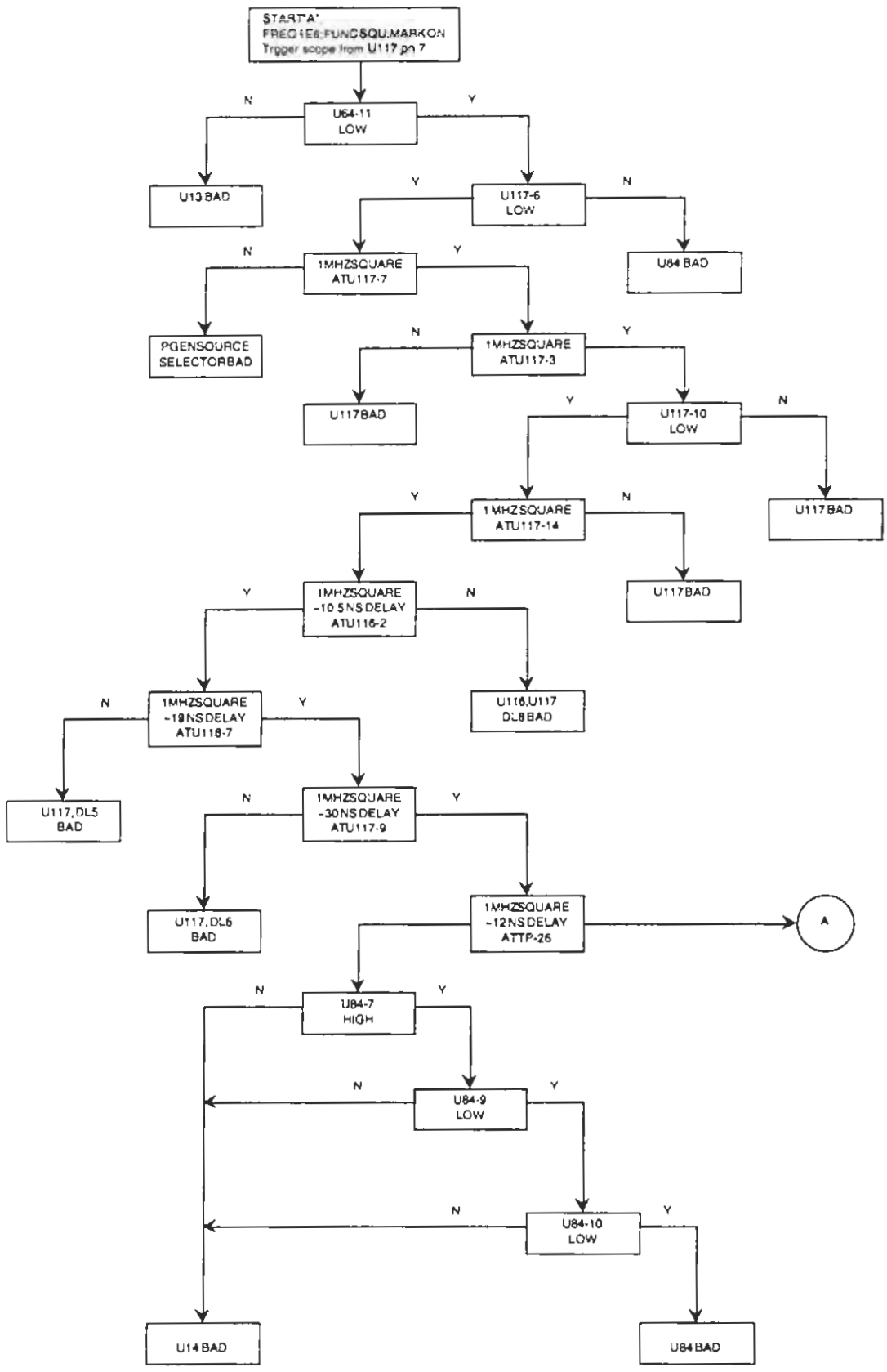


Figure 6-6. Sync Selector Troubleshooting Flow Chart

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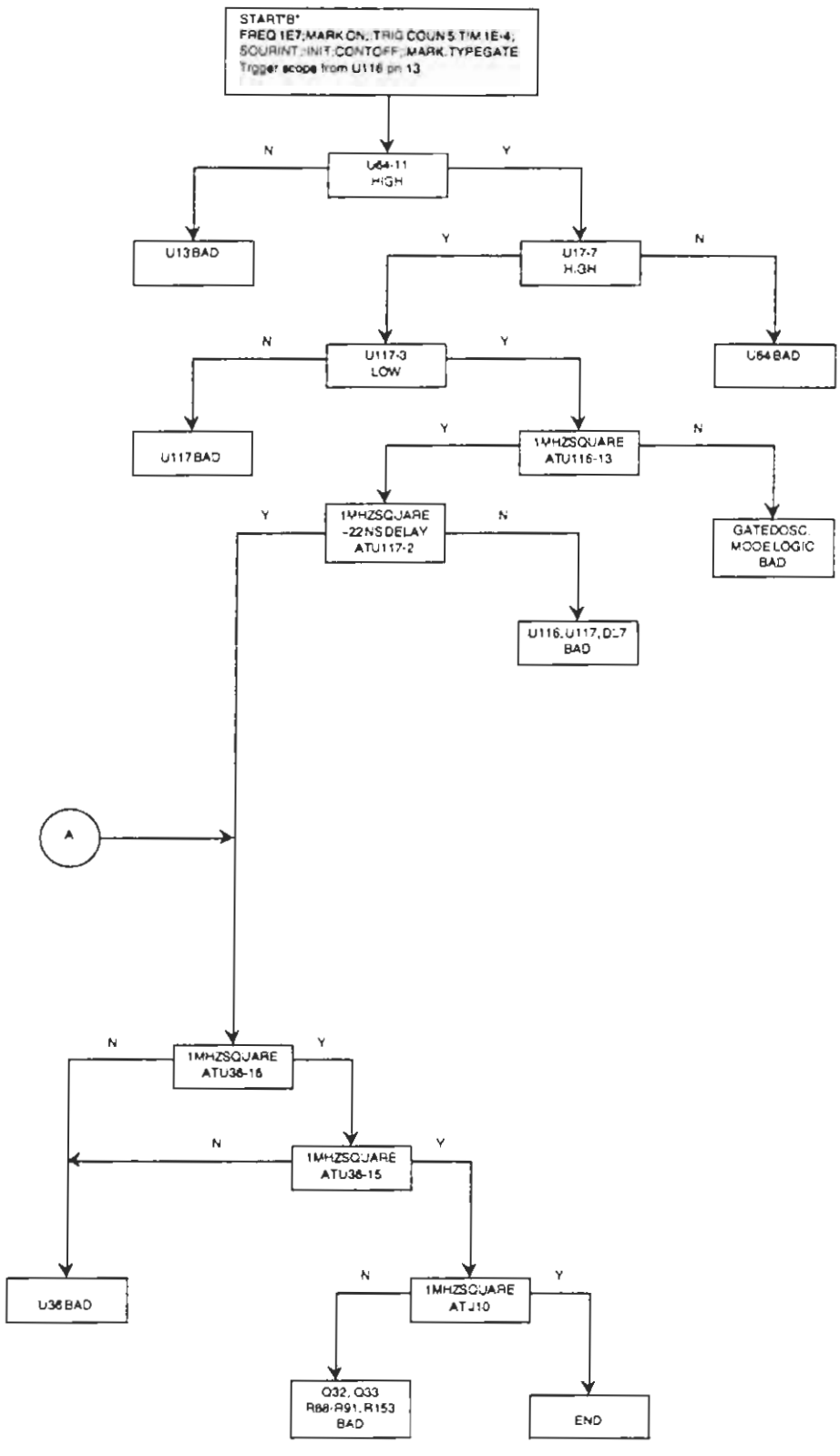


Figure 6-6 (Cont'd). Sync Selector Troubleshooting Flow Chart

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7.1 DRAWINGS

The following schematics and assembly drawings are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Outline Drawing	0002-00-0694
Instrument Schematic	1004-00-0694
Instrument Assembly Drawing	1001-00-0694
Instrument Parts List (Standard)	1000-00-0694-01
Instrument Parts List (MATE)	1000-00-0694-11
Main Board Schematic	1104-00-3612
Main Board Assembly	1101-00-3612
Main Board Parts List	1100-00-3612-01
Amplifier Board Schematic	1104-00-3605
Amplifier Board Assembly Drawing	1101-00-3605
Amplifier Board Parts List	1100-00-3605-01
Spares Kit Parts List	1200-00-3613

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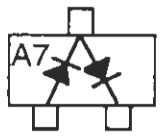
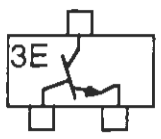
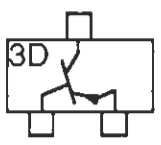
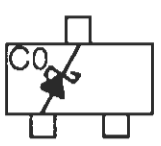
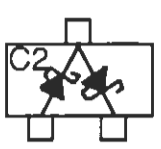
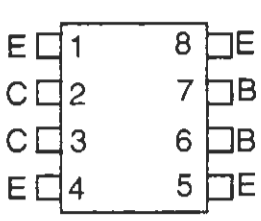
PART	MARKING	PIN-OUT
BAV99	A7	
MMBTH10	3E	
MMBTH81	3D	
HSM2820	C0	
HSMS2822	C2	
MRF3866 3866 NPN MRF5160 5160 PNP MRF5583 5583 PNP MRF5943 5943 NPN		

Figure 7-1. Surface Mount Parts Pin-Outs

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	A/D MODEL 1391 50 MHz VXI PG	1001-00-0694	WVTK	1001-00-0694	1
REF	ATS MODEL 1391	1002-00-0694	WVTK	1002-00-0694	1
REF	INSTR SCHEMATIC MODEL 1391	1004-00-0694	WVTK	1004-00-0694	1
REF	MANUAL MODEL 1391	1006-00-0694	WVTK	1006-00-0694	1
REF	CALIB PROCEDURE MODEL 1391	1008-00-0694	WVTK	1008-00-0694	1
16	INSTRUMENT LABEL MODEL 1391	1009-00-0694	WVTK	1009-00-0694	1
25	LABEL/INFO DRWG,MODULE PARAMETERS	1009-00-0694-01	WVTK	1009-00-0694-01	1
23	AMPLIFIER BD	1100-00-3605-01	WVTK	1100-00-3605-01	1
17	PCA 50MHz VXI MAIN BD	1100-00-3612-01	WVTK	1100-00-3612-01	1
NONE	PCA, VXI INTERFACE BOARD MODEL 1391	1100-00-3677-21	WVTK	1100-00-3677-21	1
14	CHASSIS RAIL, TOP	1400-02-5080	WVTK	1400-02-5080	1
19	CHASSIS RAIL,BOTTOM	1400-02-5081	WVTK	1400-02-5081	1
9	COVER,SIDE PANEL,LEFT	1400-02-8052	WVTK	1400-02-5082	1
15	REAR PANEL VXI	1400-02-5083	WVTK	1400-02-5083	1
18	COVER,SIDE PANEL,RIGHT	1400-02-5096	WVTK	1400-02-5096	1
6	WVTK LOGO NAMEPLATE	1400-02-5100	WVTK	1400-02-5100	1
2	VXI LOGO NAMEPLATE	1400-02-5114	WVTK	1400-02-5114	1
4	FRONT PANEL 1391	1400-02-5230	WVTK	1400-02-5230	1
5	HANOLE,EXTRACTOR,TOP, BLACK	20817-330	SCHRF	2800-07-0040	1
1	HANDLE,EXTRACTOR,BOTTOM,BLACK	20817-329	SCHRF	2800-07-0041	1
11	SCREW,4-40X1/4,PHP,NY LOCK PATCH,2 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	14
21	WASHER REF:21100-721, BAG OF 100 PCS	21100-721	SCHRF	2800-28-0030	2
10	SCREW,PLPS,FH,100 DEG,S/S,2-56NCx3/16" NYLK PATCH	2C18FXHSH	CMRCL	2800-54-0209	8
24	SCREW,FH,82DEG,'TYPE B',4x1/2",ZNC PLT	4N150FXSZ/B	CMRCL	2800-54-0210	6
8	SCREW,COLLAR,M2.5x11, NICKEL PLATE REF:21100-379, BAG OF 100 PCS	2800-54-0212	SCHRF	2800-54-0212	2
22	SCREW,CHEESE HEAD,M2.5x10,ZINC REF:21100-138, BAG OF 100 PCS	2800-54-0213	SCHRF	2800-54-0213	2

WAVETEK PARTS LIST	TITLE MODEL 1391 50 MHz VXI PULSE GENERATOR	ASSEMBLY NO. 1000-00-0694-01	REV C
		PAGE 1	

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
20	SCREW,RAISED C/SK,M2.5x8 REF:21100-429, BAG OF 100 PCS	2800-54-0214	SCHRF	2800-54-0214	2
7	SLEEVE,BLK PLASTIC,5.9x3.3 REF:21100-591, BAG OF 100 PCS	21100-591	SCHRF	3000-00-0203	2
NONE	CARTN,18x12x3 1/2,225#,DBLSLDE PACK,SNGL WALL	3300-01-0030	WVTK	3300-01-0030	1

WAVETEK PARTS LIST	TITLE MODEL 1391 50 MHz VXI PULSE GENERATOR	ASSEMBLY NO. 1000-00-0694-01 PAGE 2	REV C

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	A/D MODEL 1391 50 MHz VXI PG	1001-00-0694	WVTK	1001-00-0694	1
REF	ATS MODEL 1391	1002-00-0694	WVTK	1002-00-0694	1
REF	INSTR SCHEMATIC MODEL 1391	1004-00-0694	WVTK	1004-00-0694	1
REF	MANUAL MODEL 1391	1006-00-0694	WVTK	1006-00-0694	1
REF	CALIB PROCEDURE MODEL 1391	1008-00-0694	WVTK	1008-00-0694	1
25	LABEL/INFO DRWG,MODULE PARAMETERS	1009-00-0694-01	WVTK	1009-00-0694-01	1
16	INSTRUMENT LABEL MODEL 1391 MATE	1009-00-0694-11	WVTK	1009-00-0694-11	1
23	AMPLIFIER BD	1100-00-3605-01	WVTK	1100-00-3605-01	1
17	PCA 50MHz VXI MAIN BD	1100-00-3612-01	WVTK	1100-00-3612-01	1
13	PCA, VXI INTERFACE BD MODEL 1391 MATE	1100-00-3677-32	WVTK	1100-00-3677-32	1
14	CHASSIS RAIL, TOP	1400-02-5080	WVTK	1400-02-5080	1
19	CHASSIS RAIL,BOTTOM	1400-02-5081	WVTK	1400-02-5081	1
9	COVER,SIDE PANEL,LEFT	1400-02-8052	WVTK	1400-02-5082	1
15	REAR PANEL VXI	1400-02-5083	WVTK	1400-02-5083	1
18	COVER,SIDE PANEL,RIGHT	1400-02-5096	WVTK	1400-02-5096	1
6	WVTK LOGO NAMEPLATE	1400-02-5100	WVTK	1400-02-5100	1
2	VXI LOGO NAMEPLATE	1400-02-5114	WVTK	1400-02-5114	1
4	FRONT PANEL 1391	1400-02-5230	WVTK	1400-02-5230	1
5	HANDLE,EXTRACTOR,TOP, BLACK	20817-330	SCHRF	2800-07-0040	1
1	HANOLE,EXTRACTOR,BOTTOM,BLACK	20817-329	SCHRF	2800-07-0041	1
11	SCREW,4-40X1/4,PHP,NY LOCK PATCH,2 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	14
21	WASHER REF:21100-721, BAG OF 100 PCS	21100-721	SCHRF	2800-28-0030	2
10	SCREW,PLPS,FH,100 DEG,S/S,2-S6NCx3/16" NYLK PATCH	2C18FXHSH	CMRCL	2800-54-0209	8
24	SCREW,FH,82DEG,'TYPE B',4x1/2",ZNC PLT	4N150FXS2/B	CMRCL	2800-54-0210	6
8	SCREW,COLLAR,M2.5x11, NICKEL PLATE REF:21100-379, BAG OF 100 PCS	2800-54-0212	SCHRF	2800-54-0212	2
22	SCREW,CHEESE HEAD,M2.5x10,ZINC REF:21100-138, BAG OF 100 PCS	2800-54-0213	SCHRF	2800-54-0213	2

WAVETEK PARTS LIST	TITLE MODEL 1391 MATE 50 MHz PULSE GENERATOR	ASSEMBLY NO. 1000-00-0694-11 PAGE 1	REV B

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
20	SCREW,RAISED C/SK,M2.5x8 REF:21100-429, BAG OF 100 PCS	2800-54-0214	SCHRF	2800-54-0214	2
7	SLEEVE,BLK PLASTIC,5.9x3.3 REF:21100-591, BAG OF 100 PCS	21100-591	SCHRF	3000-00-0203	2
NONE	CARTN,18x12x3 1/2,225#,D8LSLDE PACK,SNGL WALL	3300-01-0030	WVTK	3300-01-0030	1

WAVETEK PARTS LIST	TITLE MODEL 1391 MATE 50 MHz PULSE GENERATOR	ASSEMBLY NO. 1000-00-0694-11	REV 8
		PAGE 2	

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D 50 MHz VXI MAIN BD	1101-00-3612	WVTK	1101-00-3612	1
NONE	SCHEMATIC 50 MHz VXI MAIN BD	1104-00-3612	WVTK	1104-00-3612	1
R34	RES,MFLM 4.530K .1% 1/8W T0	HA55 100PPM	HYMEG	111.4539	1
NONE	SUB ASSEMBLY FOR SURFACE MOUNT COMPONENTS	1200-00-3612-01	WVTK	1200-00-3612-01	1
2	CAN,M/B SYNTHESIZER	1400-02-5139	WVTK	1400-02-5139	1
C32 C46 C55 C65	CAP, CER, DISC, 10PF,1KV, COG,5%, RAD LD .25	10TCCQ10	SPRAG	1500-01-0031	4
C23	CAP,CER,100PF,100V,AXIAL	CAC02COG101J100A(OBS)	CORNG	1500-01-0106	1
C29 C30 C37 C42 C47 C51	CAP,CER,.001 MF,+-10%,50V,X7R,.1" LS	SR15SC102KAA	AVX	1500-01-0207	6
C128 C24 C25 C26 C76	CAP,CER,.01MF,+-10%,50V,X7R,.1"LS	SR15SC103KAA	AVX	1500-01-0307	5
C12 C13 C15 C153 C154 C155 C156 C157 C158 C159 C16 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C17 C170 C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C185 C186 C187 C188 C189 C190 C191 C192 C193 C198 C199 C200 C201 C202 C203 C204 C205 C233 C234 C27 C31 C33 C34 C39 C40 C41 C43 C44 C49 C50 C506 C507 C508 C52 C53 C550 C552 C57 C58 C59	CAP,CER,.1 MF,50V,X7R,+-10%,.1" LS	SR20SC104KAA	AVX	1500-01-0415	77
C35 C36	CAP CER MON 22PF 50V COG 5% RADIAL LD SP .2	5028E050RD220J	KYCRA	1500-02-2016	2
C195 C196	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	NRE101M35V10X12.5(OBS)	NIC	1500-31-0102	2
C1 C2 C3 C4 C5	CAP,ELECT,100MF,25V,RADIAL LEAD-SP SIZE	NRE101M25V6.3X11	NIC	1500-31-0122	5
C18 C20	CAP,MET POLYS,.1MF,10%,63V,.1"LS	MKS02-0.1MF-10%-63V	WIMA	1500-41-0418	2
C22	CAP,MET POLYS,0.01MF,+-20%,63V,.1"LS	MKS02-0.01MF,20%-63V	WIMA	1500-41-0422	1
C19	CAP, MET. POLYS, 0.015MF, 20%, 63V, 0.1LS	MKS02-0.015MF-20%-63V	WIMA	1500-41-0425	1
C11 C197 C237 C238 C45 C54 C551 C6 C8 C9	CAP, TANT, 1MF, 35V	196D105003SHA1(OBS)	SPRAG	1500-71-0512	10
C10 C152 C28 C56 C7	CAP,TANT,22MF,15V	196D226X9015KA1(OBS)	SPRAG	1500-72-2601	5
L1	INDUCTOR,99 NH,5%,Q66	132-07	COILC	1800-00-0050	1

WAVETEK PARTS LIST	TITLE PCA 50 MHz VXI MAIN BOARD	ASSEMBLY NO. 1100-00-3612-01	REV L
		PAGE 1	

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
DL2 DL3 DL4	DELAY LINE,PASSIVE, 3.5 NS, 100 OHM,SIP	EP123108	PCA	1800-00-0058	3
L2	INDUCTOR, 100 uH, 1S%, 1.1A,DCR 0.208	IHD1-100MH-15%	DALE	1800-00-0059	1
DL1 DL7	DELAY LINE, 20 NS, 100 OHM,PASSIVE,SIP	EP123141	PCA	1800-00-0060	2
DL6	DLY LINE,PASSIVE, 10 NS, 100 OHM,SIP	EP123121	PCA	1800-00-0063	1
DL5 DL8	DELAY LINE,PASSIVE, 7.5 NS, 100 OHM,SIP	EP123116	PCA	1800-00-0064	2
J10 J11 J14 J9	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	4
J12 J13	CONN,SIP, 15 PIN,LOW PROFILE	CES-115-01-S-S	SAM	2100-02-0312	2
J4 JS	SOCKET,40 PIN,ST,LOW INSERT	SSW-120-02-G-D	SAM	2100-03-0000	2
J6	SOCKET,20 PIN,ST,LOW INSERT	SSW-110-02-G-D	SAM	2100-03-0001	1
J7	SOCKET,36 PIN,ST,LOW INSERT	SSW-118-02-G-D	SAM	2100-03-0006	1
XU2 XU3	SOCKET,20 PIN	DILB20P-108T	BURND	2100-03-0051	2
TP1 TP2 TP22 TP24 TP29 TP3 TP34 TP38 TP9	TEST POINT,BLK,PC	TP-104-01-00	COMPO	2100-04-0054	9
TP10 TP11 TP12 TP13 TP14 TP1S TP17 TP18 TP19 TP20 TP21 TP23 TP25 TP26 TP30 TP31 TP32 TP33 TP35 TP36 TP4 TP41 TP42 TP5 TP6 TP7 TP8	TEST POINT,RED,PC	TP-104-01-02	COMPO	2100-04-0055	27
TP37	TEST POINT, SCOPE PROBE, COAXIAL	131-2766-01 W/131-0352	TEKTX	2100-04-0057	1
3	STANDOFF, 3/8 LG, 3/16 DIA, 4-40 THRD,ALUM	9395E	SMITH	2800-02-0040	4
4	TRANSIPAD	503-075	BIVAR	2800-11-0003	3
5	HEATSINK,TO-5 PKG	7-1208A	IERC	2800-11-0042	2
6	SCREW,4-40X1/4,PHP,NY LOCK PATCH,Z 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	4
7	HOLE PLUG,BINDER HEAD,NTRAL NYLON	207-120241-03-0101	FASTX	2800-35-0009	4
8	RIVET PLASTIC	231-080551-05-0101	FASTX	2800-60-0008	3
FB1 FB2	BALUN CORE	2873000902	FARIT	3100-00-0002	2
K1 K2 K3	RELAY, 2 FORM C, 5V, LOW PROFILE	TQ2E-5V	AROMT	4500-00-0038	3
R196	POT,TOP TRIM,20T,1K	68WR1K	BECK	4609-90-0005	1
R113	POT,TOP TRIM,20T,5K	68WR5K	BECK	4609-90-0013	1
R158 R42	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	2
R526 R527	RES,C,1/2W,5%,4.7	RC-1/2-4R7J	STKPL	4700-25-0479	2

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R209	RES,MFLM, 1/8W, 0.1%, 100 PPM/C, 24.9K OHM	RN55D2492B	BUYOP	4701-02-2492	1
R33	RES, MF,1/8W,.1% T2 499	CMF-1/10B(T-9)499	DALE	4701-02-4990	1
R32	RES, MF,1/8W,.1% T2 4.99K	RN55E4991B	DALE	4701-02-4991	1
R243 R246 R249 R255 R29 R58 R60	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	7
R14 R16 R211 R25 R72 R73 R84 R85	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	8
R19 R20 R37 R5 R6 R69 R71 R83	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	8
R26 R70 R82 R92	RES,MF,1/8W,1%,10	5043ED10R100F	MEPCO	4701-03-1009	4
R40	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	1
R30	RES,MF,1/8W,1%,1.62K	RN55D-1621F	TRW	4701-03-1621	1
R24 R47 R49 R52 R54 R66 R68 R79 R81	RES,MF,1/8W,1%,165	RN55D-1650F	TRW	4701-03-1650	9
R210	RES,MF,1/8W,1%,221	RN55D-2210F	TRW	4701-03-2210	1
R11 R9	RES,MF,1/8W,1%,2.37K	RN55D-2371F	TRW	4701-03-2371	2
R15 R31 R43 R56	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	4
R35 R532	RES,MF,1/8W,1%,2.74K	RN55D-2741F	TRW	4701-03-2741	2
R38	RES,MF,1/8W,1%,3.01K	RN55D-3011F	TRW	4701-03-3011	1
R27	RES,MF,1/8W,1%,3.16K	RN55D-3161F	TRW	4701-03-3161	1
R28	RES,MF,1/8W,1%,3.83K	RN55D-3831F	TRW	4701-03-3831	1
R23 R46 R48 R51 R53 R65 R67 R78 R80	RES,MF,1/8W,1%,39.2	RN55D-39R2F	TRW	4701-03-3929	9
R22 R50 R55 R64 R77	RES,MF,1/8W,1%,4.02K	RN55D-4021F	TRW	4701-03-4021	5
R10	RES,MF,1/8W,1%,432	RN55D-4320F	TRW	4701-03-4320	1
R8	RES,MF,1/8W,1%,464	RN55D-4640F	TRW	4701-03-4640	1
R41	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	1
R17 R7	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	2
R252 R253 R61 R74	RES,MF,1/8W,1%,49.9	RN55D-49R9F	CORNG	4701-03-4999	4
R533	RES,MF,1/8W,1%,511	RN55D-5110F	TRW	4701-03-5110	1
R63 R76 R91	RES,MF,1/8W,1%,523	RN55D-5230F	TRW	4701-03-5230	3
R21	RES,MF,1/8W,1%,7.5K	RN55D-7501F	TRW	4701-03-7501	1
R239 R240 R44 R45 R508	RES,MFLM,1/8W,1%,75	5033RD75ROF	MEPCO	4701-03-7509	5
R153 R90	RES, ZW, 1%, 100 PPM/C, 240 OHM	RN55D2400F	BUYOP	4701-06-2400	2
R88 R89	RES,MF,1W,1%,100	RN70D-1000F	TRW	4701-33-1000	2
RN29	RES NETWORK 470 2% 10PIN SIP ISOL	4310R102-471	BOURN	4770-00-0027	1
RN19	RES,NTWK, 2K OHM x 5, 2%,SIP,ISOLATED	4610X-102-202	BOURN	4770-00-0074	1

WAVETEK PARTS LIST	TITLE PCA 50 MHz VXI MAIN BOARD	ASSEMBLY NO. 1100-00-3612-01	REV L

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RN1 RN10 RN11 RN12 RN13 RN14 RN15 RN16 RN17 RN18 RN2 RN22 RN3 RN30 RN31 RN4 RN5 RN6 RN7 RN8 RN9	RES,NTWK, 82 OHM x 9, 2%, SIP,BUSS	4610X-101-820	BOURN	4770-00-0075	21
CR18	DIODE, ZENER, 3.9V, IN748	1N748A	FAIR	4801-01-0748	1
CR10 CR11 CR13 CR19 CR2 CR24 CR25 CR26 CR27 CR28 CR29 CR3 CR32 CR6 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	17
CR20 CR21	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	2
CR22 CR23 CR600	DIODE 5082-2811 SCHOTTKY,15V,20MA	5082-2811	HP	4809-02-2811	3
CR14 CR15 CR16 CR17	DIODE,BB909B	BB909B	PHLIP	4899-00-0040	4
DS5	LED,AMBER,RECT BAR	LTL-3251A	LITE	4899-00-0056	1
DS2 DS3	LED,GREEN,PC MT.,INT HOLDER	550-0206	DIALT	4899-00-0066	2
DS4 DS6	LED,YELLOW,PC MOUNT,INT. HOLDER	550-0306	DIALT	4899-00-0067	2
DS1	LED,RED, PC MT., INT. HOLDER	550-0406	DIALT	4899-00-0068	1
CB1	CIRCUIT PROT.,SELF RESETING, 0.65 AMP	RXE065	RAYCM	4899-00-0069	1
Q53	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	1
Q10 Q24 Q30 Q9	TRANS, NPN, TO-92	PN3563	NSC	4901-03-5630	4
Q32 Q33	TRANS	2N3866	MOT	4901-03-8660	2
Q25 Q31	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	2
Q1 Q11 Q500 Q7	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	4
Q5	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	1
Q4	TRANS,N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	1
Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q2 Q20 Q21 Q22 Q23 Q26 Q27 Q28 Q29 Q3 Q6	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	19
Q51	TRANSISTOR	RFP6P10	RCA	4902-00-0610	1
Q52	TRANSISTOR	RFP8N18L	HARIS	4902-00-0818	1
U22 U23 U49 U50	OP AMP,JFET,SINGLE	TL051CP	TI	7000-00-5100	4
U48	OP AMP,ENHANCED JFET,PRECISION QUAD	TL054CN	TI	7000-00-5400	1
U73	OP AMP,DUAL FET INPUT	CA082E(OBS)	RCA	7000-00-8200	1
U86	MIC POWER VOLT REF	LM385BZ-2.5	LINTE	7000-03-8500	1
U47	VOLTAGE REFERENCE, 10V, 8 PIN DIP	LT1021CCN8-10	LINTE	7000-10-2101	1
U109	ADC, 12 BIT,W/ 8 CHAN MUX	LTC1290DCN	LINTE	7000-12-9000	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U28	REG,POSITIVE,, 18 VOLT, 100MA, TO-92	MC78L18ACP	MOT	7000-78-1801	1
U27	VOLT REGULATOR, NEGATIVE	MC7905CP	MOT	7000-79-0500	1
U26	REG, NEG, 18 VOLTS, 100MA, TO-92	MC79L18ACP	MOT	7000-79-1801	1
U34	COMPARATOR,HIGH SPEED,ECL	AD96685BQ	AD	7000-96-6850	1
U5 U6	XLATOR, PROG, HEX	LTC1045CN	LINTE	8000-10-4500	2
U11 U110 U111 U13 U14 U15 U16 U17 U18 U19 U20 U7	SHFT REG,8-BIT,CMOS,OUTPUT CLR	SN74HC595N	TI	8000-74-5950	12
U117 U53 U57 U62 U68 U71 U72 U76 U79 U80 U91 U92	MECL 10KH HIGH-SPEED ECL	MC10H102P	MOT	8001-01-0201	12
U54	GATE, AND QUAD, ECL	MC10H104P	MOT	8001-01-0401	1
U116 U43 U44 U45 U51 U64 U65	GATE, OR/NOR, TRIPLE 2-3-2 IN	MC10H105P	MOT	8001-01-0501	7
U41	XOR/XNOR,MECL,2-INPUT ,TRIPLE	MC10H107P	MOT	8001-01-0701	1
U113 U29 U30 U36 U74 U82 U98	RECEIVER-TRIP LN ECL	MC10H116P	MOT	8001-01-1601	7
U33 U55 U61 U63 U67	GATE,OR AND/OR AND INVER DUAL WIDE, ECL	MC10H121P	MOT	8001-01-2100	5
U35	TRANSLATOR,QUAD TTL-TO-MECL	MC10H124P	MOT	8001-01-2401	1
U42	TRANSLATOR,QUAD TTL-TO-MECL	MC10H125P	MOT	8001-01-2501	1
U115 U32 U46 U52 U58 U59 U66 U69 U70 U77 U78	FLIP-FLOP, DUAL D, MAS/SL, ECL	MC10H131P	MOT	8001-01-3101	11
U37 U84	MUXMECL, 10KH	MC10H164-P	MOT	8001-01-6400	2
U39	DECODER/DEMUX,3 TO 8,TTL	SN74F138N	TI	8007-41-3820	1
U1 U8 U9	1 OF 8 DECODER/DEMULTIPLEXER	MC74HC138AN	MOT	8007-41-3840	3
U38	MUX 8-INPUT	74F151PC	FAIR	8007-41-5120	1
U114	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1
U12	BUFFER,OCTAL,INVERTIN G, TS,HCMOS	SN74HC540N	TI	8007-45-4040	1
U10	BUFFER,OCTAL,TS,HCMOS	SN74HC541N	TI	8007-45-4140	1
U4	EEPROM,SERIAL, 4096 BIT	XL93C66P	EXEL	8009-36-6000	1
U25	PRESCALER,DUAL MODULUS,DIVIDE-BY-64/ 65,ECL	MC12017P	MOT	8012-01-1700	1
U21	PLL SERIES INPUT FREQ SYNTHESIZER	MC145158P(OBS)	MOT	8014-51-5800	1
U40	BUFFER,OCTAL,OPEN COLTR,64MA	N74F760N	SIG	8074-76-0001	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U24	OSC EMT CUPLD, ECL	MC1648P	MOT	8100-16-4810	1
U3	GAL,PROG,USES 8000-16-8002 FOR MOD 1391, REF U3	8600-00-0745	WVTK	8600-00-0745	1
U2	GAL,ADDRESS DECODER,USES 8000-16-8002 FOR MOD 1391,REF U2	8600-00-0746	WVTK	8600-00-0746	1
U31 U56 U60 U75 U83	GATE ARRAY,COUNTER,SYNCH,MULTI-MODE,32-BIT	CLA53047/BW/DP	PLESS	8700-00-0005	5
Enter Alt-F1 to name your file REF	A/D 50 MHz VXI MAIN BD	1101-00-3612	WVTK	1101-00-3612	1
C217 C218 C219 C220 C221 C222 C223 C224 C225 C226	TANT, 4.7MF, 50V,SMD,EIA 7343 CASE	PCT4.7/50DM	NEMCO	1500-74-7512	10
C118 C121 C124 C125 C133 C135 C144 C147 C213 C235 C236	CAP,TANT, 6.8MF, 20V, 20%, SMD EIA 6032 CASE	PCT6.8/20CM	NEMCO	1500-76-8512	11
C215 C216	CAP,TANT, 6.8MF, 20%, 35V,SMD	TAJ-D-685-M-035	AVX	1500-76-8513	2
C141	CAP, SMD CER NPO 100PF/50V	C1206C101J2GAC	KEMET	1500-80-0001	1
C100 C101	CAP,SMD,CER,X7R,+/-15%,1000PF,50V	C1206C102K5RAC	KEMET	1500-81-0200	2
C103 C104 C105 C110 C111 C112 C113 C114 C115 C116 C117 C119 C120 C122 C123 C126 C127 C129 C130 C131 C132 C134 C136 C138 C139 C140 C142 C145 C146 C148 C149 C150 C151 C194 C207 C208 C209 C210 C211 C214 C227 C228 C229 C230 C231 C500 C501 C502 C504 C505 C560 C60 C61 C62 C63 C64 C68 C69 C70 C71 C72 C73 C74 C79 C80 C81 C82 C83 C84 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99	CAP,CER, 0.1MF, 50V,25U, +80-20%,SMD 1206	C1206C104Z5UAC	KEMET	1500-81-0401	80
C106 C137	CAP,SMD 5% 100V 15PF	11C1206C0G150J100NB	SPRAG	1500-81-5001	2
C77 C78	CAP,CERAMIC, 1500PF, 5%, 50V,NPO,SMD 1206 CASE	C152J1206CFLB OR T	PHLIP	1500-81-5201	2
C75	CAP,CER, 15000PF, 5%/10%, 50V,X7R,SMD 1206 CASE	C153J1206XFLB OR T	PHLIP	1500-81-5300	1
C107 C503	CAP,CER, 180 PF, 5%,NPO,SMD 1206 CASE	12061A181JAT050R OR B	AVX	1500-81-8101	2
C108	CAP,CER, 2000PF, 5%, 50V,X7R,SMD,1206	C202J1206XFLB OR T	PHLIP	1500-82-0201	1
C109	CAP,CER, 0.020MF, 5%, 50V,X7R,SMD, 1206	C203J1206XFLB OR T	PHLIP	1500-82-0301	1
C212 C67 C87 C88	CAP,CER, 2200PF, 5%/10%, 50V,X7R,SMD 1206 CASE	C222J1206XFLB OR T	PHLIP	1500-82-2200	4

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C85 C86	CAP,CER, 470PF, 5%/10%, 50V,NPO,SMD	C471J1206CFLB OR T	PHLIP	1500-84-7101	2
C143	CAP,CER, 8.2PF, 5%, 50V,NPO,SMD 1206 CASE	C8R2J1206CFLB OR T	PHLIP	1500-88-2901	1
1	PCB 50 MHz VXI MAIN BD REF: SPEC 0008-00-0455 REV E	1700-00-3612	WVTK	1700-00-3612	1
R520	POT,SMD,TRIM,MULTI-TURN, 1/4" SQ.	84WR10K	BECK	4600-03-0000	1
R165	POT, SMD, 500 OHM,SINGL TURN, 4 MM	3314J-1-501	BOURN	4600-04-0001	1
R125 R126 R139 R172 R194 R228 R231 R232 R256 R257 R504	RES, 100 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A1000FLR	PHLIP	4703-13-1000	11
R103 R135 R136 R215 R96	RES, 200PPM, 1%, 1/8W, 1K, 1206,SMD 1206 CASE	9C12063A1001FLR	MEPCO	4703-13-1001	5
R193 R198 R213 R219 R220 R223 R224 R502	1/8W, 1%, 200 PPM, 100 KOHM,SMD 1206 CASE	9C12063A1003FLR	PHCOM	4703-13-1003	8
R115 R120 R121 R122 R123 R159 R164 R170 R171 R173 R174 R175 R528 R529	RES, 200PPM,1/8W, 1%,10 OHM,SMD, 1206 1206 CASE	9C12063A10R0FLR	MEPCO	4703-13-1009	14
R132	RES, 115 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A1150LR	PHLIP	4703-13-1150	1
R216	RES,MF, 1/8W, 1%, 200 PPM/C, 12.4 KOHM,SMD 1206 CASE	CRCW12061242FT	DALE	4703-13-1242	1
R189	RES, 12.4 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A12R4FLR	PHLIP	4703-13-1249	1
R162 R167 R187 R188 R197 R505	RES, 150 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A1500FLR	PHLIP	4703-13-1500	6
R124 R525	RES,200PPM,1/8W,1%,1.5K OHM,SMD,1206	9C12063A1501FLR	MEPCO	4703-13-1501	2
R148 R150 R152	RES, 15K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A1502FLR	PHLIP	4703-13-1502	3
R203	RES, 165 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A1650FLR	PHLIP	4703-13-1650	1
R134	RES, 169 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A1690FLR	PHLIP	4703-13-1690	1
R157	RES,MF, 1/8W, 1%, 1.69 KOHM,SMD 1206 CASE	CRCW12061691FT	DALE	4703-13-1691	1
R217 RZ18	RES, 1.87K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A1871LR	PHLIP	4703-13-1871	2
R168	RES,MF, 1/8W, 1%, 200 PPM/C, 196 OHM,SMD 1206 CASE	CRCW12061960FT	DALE	4703-13-1960	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R169 R181 R183	RES, 210 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063AZ100FLR	PHLIP	4703-13-2100	3
R112	RES, 2.32K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063AZ321LR	PHLIP	4703-13-2321	1
R101 R114 R94	RES, 243 OHM, 1%, 1/8W, 200 PPM/C SMD, 1206 CASE	9C12063AZ243RLR	PHLIP	4703-13-2430	3
R166 R186 R199 R201 R202 R204 R205 R227	RES, 200PPM, 1%, 1/8W, 249 OHM, 1206,SMD	9C12063AZ490FLR	MEPCO	4703-13-2490	8
R235	RES, 2.49K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063AZ491FLR	PHLIP	4703-13-2491	1
R522	RES, 1/8W, 1%, 200 PPM/C, 24.9 KOHM,SMD 1206 CASE	CRCW12062492FT	DALE	4703-13-2492	1
R184 R206	RES, 200 PPM, 1%, 1/8W, 28.7,SMD, 1206	9C12063AZ28R7FLR	MEPCO	4703-13-2879	2
R221 R222	RES, 200PPM, 1%, 1/8W, 3.01K, 1206,SMD	9C12063A3011FLR	MEPCO	4703-13-3011	2
R182	RES, 324 OHM, 1%, 1/8W, 200 PPM/C, SMD 1206 CASE	9C12063A3240FLR	PHLIP	4703-13-3240	1
R133	RES, 332 OHM, 1%, 1/8W, 200 PPM/C, SMD 1206 CASE	9C12063A3320FLR	PHLIP	4703-13-3320	1
R117 R507	RES, 3.74K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A3741FLR	PHLIP	4703-13-3741	2
R177 R195	RES, 200 PPM, 1%, 1/8W, 38.3 OHM,SMD 1206 CASE	9C12063A38R3FLR	MEPCO	4703-13-3839	2
R131 R160	RES, 402 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A4020FLR	PHLIP	4703-13-4020	2
R104 R97	RES, 4.32K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A4321LR	PHLIP	4703-13-4321	2
R100 R93	RES,200 PPM, 1/8W,1%, 453 OHM,SMD,1206	9C12063A4530FLR	MEPCO	4703-13-4530	2
R214 R229 R234 R237	RES, 200PPM, 1%, 1/8W, 499 OHM, 1206,SMD	9C12063A4990FLR	MEPCO	4703-13-4990	4
R129 R130 R146 R236 R538 R539	RES, 4.99K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A4991FLR	PHLIP	4703-13-4991	6
R225	RES, 49.9K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A4992FLR	PHLIP	4703-13-4992	1
R156 R163 R176 R226 R500 R501	RES,SMD,200PPM,1%,1/8W,49.9ohm	CRCW1206-49.9FT	DALE	4703-13-4999	6

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R137 R138 R140 R141	RES, 51.1 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A51R1FLR	PHLIP	4703-13-5119	4
R200	RES, 549 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A5490FLR	PHLIP	4703-13-5490	1
R107 R161	RES, 604 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A6040LR	PHLIP	4703-13-6040	2
R109	RES, 61.9K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A192LR	PHLIP	4703-13-6192	1
R230 R233	RES, 681 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A6810LR	PHLIP	4703-13-6810	2
R180	RES,MF, 1/8W, 1%, 200 PPM/C, 7.32 KOHM,SMD 1206 CASE	CRCW12067321FT	DALE	4703-13-7321	1
R506	RES, 750 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A7500LR	PHLIP	4703-13-7500	1
R145	RES, 7.5K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A7501FLR	PHLIP	4703-13-7501	1
R127 R128 R530	RES, 200PPM,75 OHM, 1%, 1/8W, 1206	9C12063A75R0FLR	MEPCO	4703-13-7509	3
R106 R99	RES, 7.87K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A7871LR	PHLIP	4703-13-7871	2
R116	806 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A8060FLR	PHLIP	4703-13-8060	1
R119	RES, 8.25K OHM, 1%, 1/8W, 200 PPM/C SMD, 1206	9C12063A8251FLR	PHLIP	4703-13-8251	1
R108	RES, 887 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A8870LR	PHLIP	4703-13-8870	1
R178 R179	RES, 200 PPM/C, 1%, 1/8W, 909 OHM,SMD 1206 CASE	9C12063A9090FLR	PHLIP	4703-13-9090	2
R570	RES, 90.9K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A9092LR	PHLIP	4703-13-9092	1
R147 R149 R151	RES, 90.9 OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A90R9FLR	PHLIP	4703-13-9099	3
R110	RES, 9.53K OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A9531LR	PHLIP	4703-13-9531	1
R192	RES, 121 OHM, 1%, 200 PPM/C, 1/2W, SMD 1812 CASE	MC1812 121 OHM 1% T	RCD	4703-16-1210	1
R190	RES, 150 OHM, 1%, 200 PPM/C, 1W, SMD, 2512 CASE	MC2512 150 OHM 1% T	RCD	4703-18-1500	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R142 R143 R144	RES, 10M OHM, 5%, 1/8W, 200 PPM/C,SMD 1206 CASE	CRCW1206106JT	DALE	4703-20-1065	3
R111	RES, SMD 1/8 LONG 100PPM 1% 14.3K OHM	9C12063A1432FKR	MEPCO	4703-21-4321	1
R102 R95	RES, SMD 1/8 LONG 100PPM 1% 4.02K OHM	MCR18FXTA4021F	ROHM	4703-24-0211	2
R118	RES, SMD 1/8 LONG 100PPM 1% 51.1K OHM	9C12063A5112FKR	MEPCO	4703-25-1121	1
R185 R191	RES, 88.70 OHM, 1%, 200 PPM/C, 2W,SMD 4020 CASE	MC4020 88.7 OHM 1% T	RCD	4703-30-8879	2
RN28	RES,NTWK,470,2%,16PIN ,SMD,ISOL	628-AL-471G	BECK	4770-00-0062	1
RN25	RES,NTWK, 180 OHM, 2%, 8 SEC,ISOL,SMD	4816P-001-181	BOURN	4770-00-0071	1
RN21 RN24	RES,NTWK, 2.7K, 2%, 8 SEC,ISOL,SMD	4816P-001-272	BOURN	4770-00-0072	2
RN20 RN26	RES,NTWK, 10K, 2%, 8 SEC,ISOL,SMD	4816P-001-103	BOURN	4770-00-0073	2
CR30 CR31 CR33 CR34 CR63	DIODE,ZENER, 6.8V,MLL34 PKG,SMD	MLL5235B	MOT	4801-01-5235	5
CR50 CR64	DIODE,ZENER, 3.3V, 5%, 500mW,SMD,LEADLESS	MLL5226B	MOT	4801-02-5226	2
CR39 CR40 CR61 CR62 CR67 CR68	DIODE,ZENER, 5.1V, 5%, 500mW, SMD,LEADLESS	MLL5231B	MOT	4801-02-5231	6
CR35 CR36 CR502 CR65 CR66	DIODE,ZENER, 9.1V, 5%, 500MW, SMD,LEADLESS	MLL5239B	MOT	4801-02-5239	5
CR45 CR46 CR51 CR56 CR57 CR58	DIODE,SILICON,DUAL,SM D,SOT-23	BA99LT1	MOT	4803-02-0991	6
CR37 CR38 CR73 CR74	RECTIFIER,SCOTTY BARRIER,1 AMP,20V	MBRS120T3	MOT	4806-02-1120	4
CR43 CR44 CR54 CR55 CR59 CR60 CR69 CR70 CR75 CR76 CR77 CR78 CR79	DIODE,DUAL,SCHOTTKY BARRIER,SM,SOT-23	HSMS2822T31	HP	4806-02-2822	13
CR41 CR42 CR49 CR500 CR501	DIODE,LEADLESS EQUIVALENT IN4148,500MW, SMD	RLS4148	ROHM	4807-01-4148	5
CR47 CR48 CR52 CR53	DIODE,SCHOTTKY BARRIER,SMT	HSMS2820T30	HP	4899-00-0061	4
Q41 Q42 Q43 Q44 Q47	TRANS,NPN,HI-FREQ,SMD ,SOT-23 PKG	MMBTH10LT1	MOT	4901-00-1010	5
Q45 Q46	TRANS,PNP,HI-FREQ,SMD ,SOT-23 PKG	MMBTH81LT1	MOT	4901-00-8110	2
Q39	TRANS,NPN,QUAD,SMO,SO -16	MMPQ2222	MOT	4901-02-2222	1
Q38 Q48	TRANS,PNP,QUAD,SMD,SO -16	MMPQ2907	MOT	4901-02-9072	2

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q56	TRANS,PNP, HI FREQ,SMD,SO8 PKG	MRF5583	MOT	4901-05-5831	1
Q54 Q55	TRANS,NPN,HI FREQ,SMD,SO8 PKG	MRF5943	MOT	4901-05-9431	2
Q34 Q40	TRANS,NPN/PNP,QUAD,SMD,SO-16	MMPQ6700	MOT	4901-06-7002	2
U105	OP-AMP,DUAL,JFET,SMD, SO-8	TL0-52CD	TI	7000-00-5201	1
U108 U120 U85 U93 U97	OP-AMP,QUAD,JFET,SMD, SO-14	TL0-54CD	TI	7000-00-5402	5
U94	SWITCH,ANLG,QUAD,FORM B,SMD,SO-16	DG211DY	SLCON	7000-02-1101	1
U100 U106 U107 U99	OP-AMP,HI SLEW RATE, CURNT FDBK,SMD,SO-8	CLC404AJE	COMLR	7000-04-0401	4
U104	OP-AMP,HI SLEW RATE, CURNT FEBK,SMD,SO-8	CLC409AJE	COMLR	7000-04-0901	1
U118	TIMER, UNIVERSAL,SMD, SO-8	MC1455D	MOT	7000-05-5502	1
U101	MULTIPLIER,WIDEBAND,SMD,SO-8	AD834JR	AO	7000-08-3412	1
U96	OP-AMP,ORECISION,LOW OFFSET,QUAD,SMD SOL-16 CASE	LT1014DS	LINTE	7000-10-1402	1
U102	OP-AMP,HIGH SLEW RATE, 800 MHZ, CURR FDBK SMD, SO-8	HFA1100IB	HARIS	7000-11-0002	1
U103	DARLINGTON TRANSISTOR ARRAY, SMD	ULN2004D	SIG	7000-20-0001	1
U90	OP-AMP,DUAL,HIGH CURRENT,BIP,SMD,SO-8	MC33076D	MOT	7000-33-0762	1
U87 U89	DAC, 12 BIT, 4 CHAN,SOIC PKG	MB88351PF	FUJI	7000-88-3511	2
U112	PERIPHERAL,MULTI-FUNC, 52 PIN PLCC	MC68901FN	MOT	8006-89-0102	1
NONE	CRS SHT, 26GA (.018) TINNED	3200-01-0004	WVTK	3200-01-0004	15
NONE	GAL,16V8,15NS	GAL16V8A-15P	LATT	8000-16-8002	1
NONE	GAL,16V8,15NS	GAL16V8A-15P	LATT	8000-16-8002	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT

WAVETEK PARTS LIST	TITLE PCA 50 MHz VXI MAIN BOARD	ASSEMBLY NO. 1100-00-3612-01 PAGE 12	REV L

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	A/D AMPLIFIER BD	1101-00-3605	WVTK	1101-00-3605	1
REF	SCHEMATIC,AMPLIFIER BD	1104-00-3605	WVTK	1104-00-3605	1
2	HEATSINK, OUTPUT AMPLIFIER PCA	1400-02-5313	WVTK	1400-02-5313	1
C22 C23 C24 C25	TANT, 4.7MF, 50V,SMD,EIA 7343 CASE	PCT4.7/50DM	NEMCO	1500-74-7512	4
C1	CAP, SMD CER 5% 50V 1000PF	C1206C102J2GAC	KEMET	1500-81-0201	1
C10 C11 C12 C13 C14 C15 C16 C17 C18 C20 C21 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C37 C38 C39 C4 C5 C6 C7 C9	CAP,CER, 0.1MF, 50V,25U, +80-20%,SMD 1206	C1206C10425UAC	KEMET	1500-81-0401	29
C8	CAP, SMD CER 5% 50V 33PF	C1206C330J2GAC	KEMET	1500-83-3001	1
C2	CAP,SMD,CER, 3.9 PF, 5%, NPO, 1206 CASE	C3R9J1206CFLB OR T	PHLIP	1500-83-9901	1
C19	CAP,VARI, .8-4.0 PF,SMD	2320-0	JOHAN	1500-84-0000	1
C36	CAP,CER, 82 PF, 5%,NPO,SMD 1206 CASE	12061A82RJAT050R OR B	AVX	1500-88-2001	1
1	PCB,AMPLIFIER BD REF: SPEC 0008-00-0455 REV E	1700-00-3605	WVTK	1700-00-3605	1
P1 P3	HEADER, SIP, 15 PIN	MTSW-115-08-S-S-240	SAM	2100-03-0119	2
TP1	TEST POINT,BLK,PC	TP-104-01-00	COMPO	2100-04-0054	1
TP2 TP3 TP4	TEST POINT,RED,PC	TP-104-01-02	COMPO	2100-04-0055	3
3	SPACER, 0.187 OD, 0.120 ID, 0.050 THK NYLON	908-050	BIVAR	2800-04-0025	4
4	NUT,HEX,8-32,3/32 THK,.25 FLT,MINI,SS	2800-16-8106	CMCRL	2800-16-8106	4
5	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	4
6	LOCKWASHER,#8 SPLIT RING,SS	#8SRLW	CMRCL	2800-42-8000	4
7	WASHER, LOCK REG, S/S #4	MS 35338-135	CMRCL	2800-45-4000	4
8	NUT, MACHINE SCREW, 18-8 SS, #4-40	NAS 671C4	CMRCL	2800-50-4100	4
K2 K4	RELAY,2 FORMC,5V,DIP 14	DF2E-DC5V	AROMT	4500-00-0033	2
R32 R33 R76	POT, 100 OHM, 4 mm SQ, SINGLR TURN, SMD	3314J-1-101	BOURN	4600-04-0000	3
R11	RES,MFILM,.1%,1/8W,75 K OHM	CMF-55-7502BT1	DALE	4701-02-7502	1
R79	RES,MF,1/8W,1%,13.7K	RN55D-1372F	TRW	4701-03-1372	1
R55	RES,MF,1/8W,1%,1.5K	RN55D-1501F	TRW	4701-03-1501	1

WAVETEK PARTS LIST	TITLE AMPLIFIER BOARD	ASSEMBLY NO. 1100-00-3605-01	REV C

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R77 R78	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	2
R57 R59	RES,MFLM, 165 OHM, 0.1%, 1/4W, 100 PPM/C	RN60D1650B	BUYOP	4701-04-1650	2
R56 R58	RES,MFLM, 169 OHM, 0.1%, 1/4W, 100 PPM/C	RN60D1690B	BUYOP	4701-04-1690	2
R46 R47 R54 R68 R69	RES, MF,1W,.25%, TZ 100	5053RC100R0C	MEPCO	4701-38-1000	5
R1 R3	RES, 200PPM, 1%, 1/8W, 1K, 1206,SMD 1206 CASE	9C12063A1001FLR	MEPCO	4703-13-1001	2
R13 R16 R17 R26 R27 R28 R29 R40 R41 R42 R43 R44 R4S R70 R71 R72 R73	RES, 200PPM,1/8W, 1%,10 OHM,SMD, 1206 1206 CASE	9C12063A10R0FLR	MEPCO	4703-13-1009	17
R6	RES,200PPM,1/8W,1%,1.5K OHM,SMD,1206	9C12063A1501FLR	MEPCO	4703-13-1501	1
R5 R9	RES, 162 OHM, 1%, 1/8W, 200 PPM,SMD 1206	9C12063A1620FLR	PHLIP	4703-13-1620	2
R20 R21	RES, 1/8W, 1%, 200 PPM/C, 1.78K OHM,SMD 1206 CASE	9C12063A1781FLR	PHLIP	4703-13-1781	2
R18 R19	RES, 200PPM, 1%, 1/8W, 249 OHM, 1206,SMD	9C12063A2490FLR	MEPCO	4703-13-2490	2
R2	RES, 1/8W, 1%, 200 PPM/C, 24.9 KOHM,SMD 1206 CASE	CRCW12062492FT	DALE	4703-13-2492	1
R74 R75	RES, 200 PPM, 1%, 1/8W, 28.7,SMD, 1206	9C12063A28R7FLR	MEPCO	4703-13-2879	2
R22 R23 R34 R35 R38	RES, 200PPM, 1%, 1/8W, 3.01K, 1206,SMD	9C12063A3011FLR	MEPCO	4703-13-3011	5
R30 R36	RES, 1/8W, 1%, 200 PPM/C, 41.2 OHM,SMD 1206 CASE	9C12063A41R2FLR	PHLIP	4703-13-4129	2
R12 R15 R39	RES, 200PPM, 1%, 1/8W, 499 OHM, 1206,SMD	9C12063A4990FLR	MEPCO	4703-13-4990	3
R4	RES, 4.99K OHM, 1%, 1/8W, 200 PPM/C,SMD 1206 CASE	9C12063A4991FLR	PHLIP	4703-13-4991	1
R14 R24 R25	RES,SMD,200PPM,1%,1/8W,49.9ohm	CRCW1206-49.9FT	DALE	4703-13-4999	3
R31 R37	RES, 1/8W, 1%, 200 PPM/C, 57.6 OHM,SMD 1206 CASE	9C12063A57R6FLR	PHLIP	4703-13-5769	2
R10	RES, 200 PPM/C, 1%, 1/8W, 909 OHM,SMD 1206 CASE	9C12063A9090FLR	PHLIP	4703-13-9090	1
R80	RES, 1/8W, 5%, 200 PPM/C, 4.7 OHM,SMD 1206 CASE	CRCW1204R7JRT1	DALE	4703-20-4709	1
JMP1 JMP2	RES, 0 OHM JUMPER	JP02T68G	ROHM	4799-00-0087	2

WAVETEK PARTS LIST	TITLE AMPLIFIER BOARD	ASSEMBLY NO. 1100-00-3605-01	REV C
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR12 CR13 CR14	DIODE,ZENER, 9.1V, 5%, 500MW, SMD,LEADLESS	MLL52398	MOT	4801-02-5239	3
CR5 CR6	DIODE,ZENER, 15V, 5%, 500MW,SMD LEADLESS	MLL5245B	MOT	4801-02-5245	2
CR1 CR2	DIODE,SILICON,DUAL,SM D,SOT-23	BA99LT1	MOT	4803-02-0991	2
CR3 CR4	G.P. RECTIFIER 400V, 1A LEADLESS IN4004, SMD	MLL4004	MOT	4806-03-4004	2
CR10 CR11 CR7 CR8 CR9	DIODE,LEADLESS EQUIVALENT IN4148,500MW, SMD	RLS4148	ROHM	4807-01-4148	5
CB1 CB2	CIRCUIT PROT,SELF RESETING, 0.2 AMP	RXE020	RAYCM	4899-00-0070	2
Q1	TRANS,NPN,RF,SMD, SO8	MRF3866	MOT	4901-03-8661	1
Q7 Q8	TRANS,NPN,HI FREQ,HI VOL,MRF548 STUD MOUNT	MRF548	MOT	4901-05-4801	2
Q6 Q9	TRANS,PNP,HI FREQ,HI VOLTAGE STUD MOUNT, MRF549	MRF549	MOT	4901-05-4901	2
Q3 Q4	TRANS,PNP, HI FREQ,SMD,SO8 PKG	MRF5583	MOT	4901-05-5831	2
Q2 Q5	TRANS,NPN,HI FREQ,SMD,SO8 PKG	MRF5943	MOT	4901-05-9431	2
U3	OP AMP,SMD,SO8 PKG	LM318S8	LINTE	7000-03-1803	1
U1	REG, +12V, SMD	MC78L12ACD	MOT	7000-78-1202	1
U2	REG, -12V, SMD	MC79L12ACD	MOT	7000-79-1202	1

WAVETEK PARTS LIST	TITLE AMPLIFIER BOARD	ASSEMBLY NO. 1100-00-3605-01	REV C
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT

WAVETEK PARTS LIST	TITLE AMPLIFIER BOARD	ASSEMBLY NO. 1100-00-3605-01 PAGE 4	REV C

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	RES NETWORK,4.7K,10PIN,SIP COMM	110A472	AB	0589-00472	1
NONE	CAP, CER, DISC, 10PF,1KV, COG,5%, RAD LD .25	10TCCQ10	SPRAG	1500-01-0031	2
NONE	CAP,CER,.001 MF,+-10%,50V,X7R,.1" LS	SR155C102KAA	AVX	1500-01-0207	1
NONE	CAP,CER,.01MF,+-10%,50V,X7R,.1"LS	SR155C103KAA	AVX	1500-01-0307	1
NONE	CAP,CER,.1 MF,50V,X7R,+-10%,.1" LS	SR205C104KAA	AVX	1500-01-0415	1
NONE	CAP,ELECTR.10MF,16V,20%	TAJD106M016R	STANT	1500-31-0011	2
NONE	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	NRE101M35V10X12.5(OBS)	NIC	1500-31-0102	1
NONE	CAP, TANT, 1MF, 35V	196D1050035HA1(OBS)	SPRAG	1500-71-0512	1
NONE	CAP,TANT,22MF,15V	196D226X9015KA1(OBS)	SPRAG	1500-72-2601	1
NONE	TANT, 4.7MF, 50V,SMD,EIA 7343 CASE	PCT4.7/50DM	NEMCO	1500-74-7512	2
NONE	CAP,TANT, 6.8MF, 20V, 20%, SMD EIA 6032 CASE	PCT6.8/20CM	NEMCO	1500-76-8512	1
NONE	CAP,TANT, 6.8MF, 20%, 35V,SMD	TAJ-D-685-M-035	AVX	1500-76-8513	1
NONE	CAP,CER, 0.1MF, 50V,25U, +80-20%,SMD 1206	C1206C104Z5UAC	KEMET	1500-81-0401	5
NONE	RELAY,2 FORMC,5V,DIP 14	DF2E-DC5V	AROMT	4500-00-0033	1
NONE	RELAY, 2 FORM C, 5V, LOW PROFILE	TQ2E-5V	AROMT	4500-00-0038	1
NONE	RES,NTWK, 82 OHM x 9, 2%, SIP,BUSS	4610X-101-820	BOURN	4770-00-0075	2
NONE	DIODE, DUAL SWITCHING, COMMON CATHODE,SOT-23	MMBD6100L(OBS)	MOT	4807-02-6100	1
NONE	DIODE 5082-2811 SCHOTTKY,15V,20MA	5082-2811	HP	4809-02-2811	1
NONE	DIODE,BB909B	BB909B	PHLIP	4899-00-0040	1
NONE	LED,GREEN,PC MT.,INT HOLDER	550-0206	DIALT	4899-00-0066	1
NONE	LED,YELLOW,PC MOUNT,INT. HOLDER	550-0306	DIALT	4899-00-0067	1
NONE	CIRCUIT PROT.,SELF RESETING, 0.65 AMP	RXE065	RAYCM	4899-00-0069	1
NONE	CIRCUIT PROT,SELF RESETING, 0.2 AMP	RXE020	RAYCM	4899-00-0070	2

WAVETEK PARTS LIST	TITLE MODEL 1391 SPARES KIT	ASSEMBLY NO. 1200-00-3613	REV A
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	1
NONE	TRANS, NPN, TO-92	PN3563	NSC	4901-03-5630	1
NONE	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	1
NONE	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	1
NONE	TRANS,NPN,HI FREQ,HI VOL,MRF548 STUD MOUNT	MRF548	MOT	4901-05-4801	2
NONE	TRANS,N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	1
NONE	TRANS,PNP,HI FREQ,HI VOLTAGE STUD MOUNT, MRF549	MRF549	MOT	4901-05-4901	2
NONE	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
NONE	OP AMP,JFET,SINGLE	TL051CP	TI	7000-00-5100	1
NONE	SRAM,32KX8,120NS,CMOS	HM62256LFP-12T	HTACH	8000-43-0256	1
NONE	MICROPROCESSOR,68000, CPU,CMOS,PLCC	MC68HC000FN8	MOT	8000-68-0008	1
NONE	MULTIVIBRATOR,RETRIG, MONOSTABLE,SOIC	SN74LS123D	TI	8000-74-0123	1
NONE	DECODER/DEMULTIPLEXER ,3-TO-8 LINE SOIC	SN74ALS138D	TI	8000-74-0138	1
NONE	GATE,NOR,DUAL,5 INPUT,SOIC	N74LS260D	SIG	8000-74-0260	1
NONE	COUNTER,DUAL,4 BIT,SOIC	SN74LS393D	TI	8000-74-0393	1
NONE	NON-INVERT BUFFER,HEX,TTL,SOIC	SN74ALS1035D	TI	8000-74-1035	1
NONE	XCVR,OCTAL REGISTERED,3-STATE OUTPUTS,CMOS	IDT74FCT543SO	IDT	8000-74-5430	1
NONE	FLIP FLOP,OCTAL D,W/3 STATE OUTPUTS,CMOS	IDT74FCT574SO	IDT	8000-74-5740	1
NONE	SHFT REG,8-BIT,CMOS,OUTPUT CLR	SN74HCS95N	TI	8000-74-5950	2
NONE	XCVR,OCTAL BUS,3-STATE OUTPUTS,CMOS	IDT74FCT645SO	IDT	8000-74-6450	1
NONE	MECL 10KH HIGH-SPEED ECL	MC10H102P	MOT	8001-01-0201	2
NONE	GATE, OR/NOR, TRIPLE 2-3-2 IN	MC10H105P	MOT	8001-01-0501	1
NONE	RECEIVER-TRIP LN ECL	MC10H116P	MOT	8001-01-1601	1
NONE	GATE,OR AND/OR AND INVER DUAL WIDE, ECL	MC10H121P	MOT	8001-01-2100	1
NONE	1 OF 8 DECODER/DEMULTIPLEXER	MC74HC138AN	MOT	8007-41-3840	1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	REAL TIME CLOCK W/RAM,CMOS	HD146818FP	HTACH	8014-68-1800	1
NONE	GAL,20 PIN,15NS,16V8-15,PLCC	GAL16V8-15LJ	LATT	8016-08-1500	1
NONE	GAL,22V10,EECMOS,15NS ,28PIN PLCC	GAL22V10-15LJ	LATT	8022-10-1500	1
NONE	ENCODER,8-TO-3 PRIORITY	SN74LS148D	TI	8074-14-8000	1
NONE	LINE DRIVER,OCTAL BUFFER,CMOS	IDT74FCT541SO	IDT	8074-54-1000	1
NONE	GATE ARRAY,COUNTER,SYNCH,M ULTI-MODE,32-BIT	CLA53047/BW/DP	PLESS	8700-00-0005	1

WAVETEK PARTS LIST	TITLE MODEL 1391 SPARES KIT	ASSEMBLY NO. 1200-00-3613	REV A
		PAGE 3	

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT

WAVETEK PARTS LIST	TITLE MODEL 1391 SPARES KIT	ASSEMBLY NO. 1200-00-3613	REV A
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A.1 INTRODUCTION

This appendix covers the remote operation of the Model 1391 VXIbus Pulse Generator using the CIIL language in a MATE system. Section 3 of this manual covers the "Native" SCPI operation of the unit. This appendix discusses the MATE system (hardware and language) and the commands and syntax the Model 1391 MATE Pulse Generator will recognize.

A.2 THE MATE SYSTEM

The MATE (Modular Automatic Test Equipment), an Air Force specification for automated test systems, standardizes general purpose test equipment interconnection, installation, and control syntaxes. To recognize MATE commands, the unit must be specified as a "Model 1391 MATE" rather than a standard Model 1391 at the time of purchase.

A.2.1 MATE Hardware

Because of constraints of the VXIbus environment, VXIbus modules do not implement a complete MATE hardware configuration. There will be no panel mounted MATE interface enable switch or Discrete Fault Indication connector usually associated with MATE equipment. Nor is there a front panel display device to indicate MATE status at power-on.

MATE compatibility is limited to CIIL language processing in VXIbus modules. In the Model 1391 MATE, this is accomplished with an instrument ROM change, where both the SCPI and CIIL language parsers are contained in the instrument's firmware. MATE units default into the CIIL parser at power-on.

A.2.2 MATE Language

The operator programs the MATE system controller using the ATLAS language. The controller communicates with the Model 1391 MATE via the IEEE-488 bus (external host) or via the VXIbus (embedded controller) using the CIIL command strings. The Model 1391 MATE uses its language parser to translate the CIIL command strings into the Model 1391's native SCPI language. This appendix deals with only the CIIL commands.

ATLAS (Abbreviated Test Language for All Systems) is an easy-to-read English-like language. The ATLAS language does not allow partial instrument setups. This means all items, except defaults, must be entered in each string. For further information on the ATLAS programming language, refer to ANSI/IEEE Std 416-1981, IEEE Std 716-1982, and IEEE Std 717-1982.

The system uses the CIIL (Control Interface Intermediate Language) language to communicate between the controller and the Pulse Generator. The CIIL commands are sent as an ASCII string. The CIIL language uses standard sets of commands which allow the Model 1391 MATE to be used in test systems without the necessity of rewriting the test software. However, this limits the language to standard commands that will function for all manufactures of a specific type of test equipment. To utilize any unique features of the Model 1391 MATE, it is necessary to use the `GAL` command to exit from the CIIL language and use the native language of the Model 1391 MATE. Use `SYST:LANG:CIIL` command while in native language to return to CIIL. For more information on the CIIL language, refer to Air Force standard 2806763 Revision C, 21 June 1988. The following list defines the Model 1391 MATE's MATE/CIIL capabilities:

- Set up of Pulse Generator functions and pulse characteristics.
- Burst, triggered, gated or continuous output mode setup.
- Output amplitude and dc offset control.
- Output frequency/period/pulse repetition rate control.
- External trigger/gate slope and level control.
- Pulse amplitude modulation.

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A.3 THE MODEL 1391 MATE IN THE MATE SYSTEM

A.3.1 System Connection

The Model 1391 MATE is part of a VXIbus system, and it resides in a VXIbus chassis. As such, it is subject to all benefits and restrictions of the VXIbus environment. When the MATE controller is external to the VXIbus chassis, it communicates over the GPIB bus to the GPIB/VXIbus *translator* located in the Commander (slot 0) slot of the VXIbus chassis. In this case, the VXIbus chassis has a Primary GPIB Address and the 1391 MATE module within the chassis is reached with a GPIB Secondary Address. When the VXIbus Commander is an embedded controller, the GPIB bus is not involved and communication between the Commander and the 1391 MATE module is restricted to the VXIbus Protocols.

The system interconnections for a 1391 MATE unit are the same as for the standard unit described in Section 3 of this manual.

A.3.2 Identifying a Model 1391 MATE

There are two methods of verifying a 1391 is a MATE unit. First, check the "rear panel" of the module; the serial tag between the P1 and P2 connectors will indicate "1391 MATE" for a MATE unit and "1391" for a standard unit under the model number. Also, if the module(s) are plugged into the VXIbus chassis, a standard unit will respond with full Manufacturer and Model number information to the mandated IEEE-488.2 `*IDN` command, whereas the 1391 MATE unit responds with a "space" character, indicating a non-MATE command.

A.4 THE CIIL LANGUAGE

The notations listed in Table A-1 represent the elements of CIIL command strings used in this manual. These notations aid in describing the correct syntax for command strings. In practice the controller transmits the ASCII code for the indicated syntax.

A.4.1 CIIL Command Strings

Shown below is the standard form of the CIIL command string:

```
<op code><b><noun><b><channel
number>[<b><set code><b><mod-
ifier<b><value>..]<cr,lf>
```

Table A-2 defines the command string items used by the Model 1391 MATE. Figure A-1 contains the detailed Pulse/Timing Generator syntax diagrams.

A.4.2 Syntax Paths

The path, as shown in Figure A-1, through the syntax diagram follows the standard form of the CIIL command string. All commands appearing on the syntax path must be included in that command string. When the Model 1391 MATE receives a `<cr,lf>`(carriage return and line feed), the unit assumes the command string is complete. On the diagram, a solid line bypassing some commands indicate defaults; adjacent to each default line is a default value. To get a default, omit the default command from the string.

Table A-1. CIIL Notations

Notation	Meaning
|	Separator between elements in a set of values. Only one element of the values presented may be selected.
<>	These brackets surround elements in a string that are necessary for a complete command string.
[ ]	These brackets surround optional elements in a command string and are not necessary for a complete command string.
...	Indicates that other elements may be required or desired as part of the command string.
b	Indicates the necessity for an ASCII space in the part of the command string where it appears.
chan num	Indicates that a channel number must be specified as part of the command string where it appears.
set code	Indicates that a CIIL set code must appear as part of the command string where it appears. There are only three set codes. They are: SET|SRN|SRX.
noun	Indicates that a CIIL noun must appear as part of the command string where it appears.
modifier	Indicates that a CIIL modifier must appear as part of the command string where it appears.
value	Indicates that a numeric value must appear as part of the command string where it appears. This number can be expressed in floating point, engineering or integer notation. Can also indicate a non numeric value; the possible non-numeric choices in that instance are given in the syntax diagrams.
<cr, lf>	Indicates the necessity for an ASCII carriage return followed by a line feed in the command string where it appears.

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Table A-2. Model 1391 MATE CIIL Commands

Type	CIIL Command	Description	Limits
Op Code	CLS	Closes - activates Pulse Generator output	None
	CNF	Initiates confidence test	None
	FNC	Selects function	PDC, PDT, SQW, or PAM.
	IST	Initiates self-test	None
	OPN	Opens - deactivates Pulse Generator output.	None
	RST	Reset-deactivates Pulse Generator output and returns Pulse Generator to power-up conditions.	None
	STA	Requests status	None
Noun	PAM	Pulse Amplitude Modulation	None
	PDC	Selects single pulse output.	
	PDT	Selects double pulse output.	
	SQW	Selects square wave output.	
Chan Num	:CH0	Selects module	0 only
Set Codes	SET	Set value	None, each code has the same effect on the Model 1391 MATE.
	SRN	Set minimum	
	SRX	Set maximum	
Modifiers	BURS	Sets up burst count.	PDC, PDT, SQW, or PAM; 1 to 10e6 counts.
	CAMP	Sets pulse carrier amplitude (PAM).	PAM only; 0.15 to 16.0 Vpp, (50Ω).
	CFRQ	Sets pulse carrier frequency (PAM).	PAM only; 0.001 Hz to 50e6 Hz.
	DCOF	Sets up dc offset of selected waveform.	PDC, PDT, or SQW; -8.0 to +8.0 Vdc (50Ω).
	DELA	Sets pulse delay relative to sync output.	PDC or PAM; 0.0 ns to 2000 s.
	FREQ	Sets frequency of square wave	SQW only; 0.001 Hz to 10e6 Hz.
	GALV	Sets external gate level.	PDC, PDT, SQW, or PAM; -10.0 Vdc to +10.0 Vdc.

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Table A-2. Model 1391 MATE CIIL Commands (Continued)

Type	CIIL Command	Description	Limits
Modifiers (continued)	GASC	Selects either internal or external gate source.	PDC, PDT, SQW, or PAM; INT or EXT.
	GSTA	Selects the external gate start slope.	PDC, PDT, SQW, or PAM. POS or NEG; must be opposite of GSTO.
	GSTO	Selects the external gate stop slope.	PDC, PDT, SQW, or PAM. POS or NEG; must be opposite of GSTA.
	MDSC	Selects the PAM modulation source: internal or external.	PAM only; EXT only.
	PERI	Sets period of single pulse or square.wave.	PDC or SQW; 10e-9 to 1000 s.
	PLWD	Sets pulse width for single and double pulse and PAM.	PDC, PDT, or PAM; 10e-9 to 2000 s.
	PRFR	Sets pulse repetition rate for single and double pulses and PAM.	PDC, PDT, or PAM; 0.001 to 50e6 Hz (25e6 Hz for double).
	RISE	Set the rise time (10% to 90%) of the leading transitions.	PDC, PDT, SQW, or PAM; 5e-9 to 50e-6 s.
	FALL	Set the fall time (10% to 90%) of the trailing transitions.	PDC, PDT, SQW, or PAM; 5e-9 to 50e-6 s.
	SPCG	Set delay between two pulses in the double pulse mode.	PDT only; 20e-9 to 2000 s.
	TIMP	Sets Pulse Generator output impedance.	PDC, PDT, SQW, or PAM; 50Ω only.
	TRFR	Sets internal triggering frequency.	PDC, PDT, SQW, or PAM; 20e-9 to 2000 s.
	TRLV	Sets external trigger level.	PDC, PDT, SQW, or PAM; +10.0 to -10.0 Vdc.
	TRSC	Selects internal or external triggering source.	PDC, PDT, SQW, or PAM; INT or EXT.
	TRSL	Selects external trigger slope.	PDC, PDT, SQW, or PAM; POS or NEG.
	VLPK	Sets amplitude peak value.	PDC, PDT, or SQW; 75e-3 to 8.0 Vpk
	VLPP	Sets square wave amplitude peak to peak value.	SQW only; 150e-3 to 16.0 Vpp.
	VRMS	Sets square wave RMS amplitude.	SQW only; 75e-3 to 8.0 Vrms.

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NOTE

See Figure A-1 at the rear of this section for MATE syntax diagrams.

A.5. USING THE PULSE GENERATOR IN THE MATE SYSTEM

A.5.1 Power Up Settings

At power up the Pulse Generator defaults to the following conditions:

Output Frequency:	1 MHz.
Waveform:	single pulse; 250 ns width.
Amplitude:	upper +0.5V.
	lower -0.5V.
Mode:	Continuous.
Output:	Off.

To close the output relay, send the CIIL command string:

`CLS<b>:CH0<cr,lf>`

A.5.2 Using CNF (Confidence) Op Code

Use `CNF` (confidence) to test overall Model 1391 MATE operation by programming predetermined module set-ups and verifying the instrument provides the expected output. At the completion of the confidence test, the unit resets to the power-on condition. Use `STA` (status) to verify the Model 1391 MATE has passed the confidence test. To initiate the confidence test, send the command: `CNF<cr,lf>`. See Appendix D for detailed information on the `*TST` self test which is run following this command.

A.5.3 Using IST (Instrument Self Test) Op Code

Use `IST` (instrument self test) to activate the built in test (BIT) to functionally check the module. During the test the instrument uses its own DVM, counter, trigger generator, and VXIbus system clock to evaluate the module. The diagnostics will isolate failures, if they occur, to the module. If a failure is reported, further diagnostics, not necessarily supported in CIIL can be run on a module level to assist in troubleshooting. Use `STA` (status) to verify the unit has passed the self test. To initiate the instrument self test, send the command: `IST<cr,lf>`. See Appendix D for detailed information on the `*TST` self test which is run following this command.

A.5.4 Using STA (Status) Op Code

Send `STA` (status) after a confidence test (`CNF`), internal self-test (`IST`), or setup command (`FNC` transmission). The `STA` command causes the Model 1391 MATE to return one of two valid responses.

`"F07PLG00:<ASCII message><cr,lf>"` indicates a failure was detected during the confidence test, or an error was detected in the information received in the instrument setup command.

`"<b><cr,lf>"` indicates no failures or errors.

To check the status, send the command: `STA<cr,lf>`.

A.5.5 Using the CLS (Close Output) Op Code

The Pulse Generator initializes with the output relay open. Send the `CLS` command string to close the output relay to obtain an output. Send the command string:

`CLS<b>:CH0<cr,lf>`

A.5.6 Using the FNC Op Code

Use the `FNC` command to set up the Pulse Generator. The syntax diagrams, figure A-1, illustrate the `FNC` paths required to set up the generator.

A.5.6.1 Pulse Out Output Amplitude and Timing

Figure 3-4 shows the pulse waveforms and their associated amplitude and timing modifiers.

Values for the voltage peak (`VLPK`) modifier set the peak amplitude for the pulsed dc (`PDC`) and the pulsed dc train (`PDT`) waveforms; the waveform baseline for all waveforms is specified by the dc offset (`DCOF`) value.

Square wave (`SQW`) amplitude can be specified with the modifiers shown; volts-peak-to-peak (`VLPP`) can only be used to specify a value for the square wave peak-to-peak, specifying values for `VLPK` or `VRMS` sets the peak value of the square wave.

Specifying a value for the period (`PERI`) sets the period for all waveforms; the spacing (`SPCG`) value sets the time between the leading edge of the first and second pulses for pulsed dc trains (`PDT`) only.

Specifying a value for the pulse width (`PLWD`) sets the pulse width for pulsed dc and pulsed dc trains only. The transition times for all pulses and the square wave can be set with the rising (`RISE`) and falling (`FALL`) transition times commands.

The pulse repetition frequency (`PRFR`) modifier can be used to specify a value for pulse repetition frequency as an alternative for setting the waveform period.

A.5.6.2 Pulsed DC (PDC) Waveform Programming

Table A-3 shows the modes and controls supported by CIIL for single pulse generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

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A.5.6.3 Pulsed DC Train (PDT) Waveform Programming

Table A-4 shows the modes and controls supported by CIIL for double pulse generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

A.5.6.4 Square wave (SQW) Waveform Programming

Table A-5 shows the modes and controls supported by CIIL for square wave generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

A.5.6.5 Triggering

In the triggered mode, the Pulse Generator starts a waveform when it receives a valid trigger. The following describes the trigger commands. The triggered mode cannot be used for square waves.

Specify the non-numeric values (EXT or INT) to select the trigger source (TRSC). EXT (external) selects the module's TRIG IN input BNC connector as the trigger source. INT (internal) selects Model 1391's internal trigger (TRFR) bus as the trigger source.

Specify the non-numeric values to select the trigger slope (TRSL): positive (POS) or negative (NEG).

Specify the numeric value to sets the trigger level (TRLV).

A.5.6.6 Gating

In the gated mode, the Model 1391 MATE produces a waveform as long as the trigger (gate) is active. Figure 3-7 shows the relationship between the gating signal and the Pulse Out.

Specifying either POS (positive) or NEG (negative) sets the gate start slope (GSTA) or the gate stop slope (GSTO). These values set the trigger slope on which the waveform starts and stops.

The gate start slope (GSTA) and gate stop slope (GSTO) values can never be both positive or both negative. Specifying one value without the other causes the Model 1391 MATE to automatically switch, if necessary, the remaining unspecified modifier value to the opposite slope. Specifying equal values results in an error message and termination of the command string. See Table A-6 at the rear of this appendix for error messages.

A.5.6.7 Burst

In the Burst mode, the Model 1391 MATE produces a user programmed number of waveforms each time the trigger is valid. The burst (BURS) value sets the number of waveform periods generated for each trigger.

A.5.6.8 Output Impedance

The test equipment impedance value (TIMP) selects the module's output impedance. The only allowable value for the Model 1391 is 50Ω.

A.6 SYNTAX EXAMPLES

Follow the syntax diagram, figure A-1, to help understand the CIIL command strings given in the examples.

A.6.1 Pulsed DC (PDC) Continuous

This CIIL command string sets the Pulse Generator output for continuous 10 ns, 4V pulses with a delay of 20 ns. The pulse repetition frequency is 1MHz, and the dc offset is 1V. Output impedance is set to 50Ω. The transition times will be at their default value of 5 ns.

```
FNC<b>PDC<b>:CH0<b>SET<b>VLPK<b>4<b>
SET<b>PLWD<b>10e-9<b>SET<b>PRFR<b>
1e6<b>SET<b>DELA<b>20e-9<b>SET<b>
DCOF<b>1<b>SET<b>TIMP<b>50<cr,lf>
```

A.6.2 Triggered Pulsed DC (PDC)

This CIIL command string sets up the Pulse Generator for triggered 10 ns, 2V pulses. An external source triggers the pulses on the negative slope at +3V. The waveform is offset +2V. The output impedance is 50Ω. The leading edge is 10 ns, and the trailing edge is minimum (5 ns).

```
FNC<b>PDC<b>:CH0<b>SET<b>VLPK<b>2<b>
SET<b>PLWD<b>10e-9<b>SET<b>TRSC<b>
EXT<b>SET<b>TRSL<b>NEG<b>SET<b>TRLV<b>3<b>
SET<b>DCOF<b>2<b>SET<b>TIMP<b>50<b>
SET<b>RISE<b>10e-9<b>SRN<b>FALL<b>
5e-9<cr,lf>
```

A.6.3 Pulsed DC Train (PDT) Burst

This CIIL command string sets up the Pulse Generator for a triggered burst of 50, 10 ns, 5V double pulses at 1 MHz and 20 ns spacing between the double pulses. The external source triggers the module on the positive slope (default slope) at +2V. The pulses are offset +1V. The output impedance is 50 Ω (default impedance).

```
FNC<b>PDT<b>:CH0<b>SET<b>VLPK<b>5<b>
SET<b>PRFR<b>1e6<b>SET<b>BURS<b>50<b>
SET<b>TRSC<b>EXT<b>SET<b>TRLV<b>2<b>
SET<b>PLWD<b>10e-9<b>SET<b>SPCG<b>
20e9<b>P1POS<b>P2POS<b>SET<b>DCOF<b>
1<cr,lf>
```


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Table A-3. Available Pulsed DC Waveform Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

Table A-4. Available Pulsed DC Train Waveform Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

Spacing between double pulses must be specified with the SPCG modifier, its attendant value and the modifiers "P1POS<b>P2POS". These modifiers cannot be used in command strings that control Pulsed DC (PDC) or Square wave (SQW) outputs.

Table A-5. Available Square wave Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

The trigger controls are used for the burst mode only.

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A.8.4 Continuous Square Wave (SQW)

This example sets up the Pulse Generator for continuous 2 Volt peak-to-peak, 2 MHz square waves. The defaults for dc offset and output impedance are used.

```
FNC<b>SQW<b>:CH0<b>VLPP<b>2<b>SET<b>
FREQ<b>2e6<cr,lf>
```

A.8.5 Gated Pulse DC Train

In this example the Pulse Generator produces gated 10 ns, 5V double pulses at a 1 MHz rate. The space between the double pulses is 20 ns. An external source gates the Pulse Generator on the negative slope and stops on the positive slope. Threshold level 1V. DC offset and output impedance are the default values.

```
FNC<b>PDT<b>:CH0<b>SET<b>VLPK<b>5<b>
SET<b>PERI<b>1e-6<b>SET<b>GASC<b>
EXT<b>SET<b>GSTA<b>NEG<b>SET<b>GSTO<b>
POS<b>SET<b>GALV<b>1<b>SET<b>PLWD<b>
10e-9<b>SET<b>SPCG<b>20e-9<b>P1POS
<b>P2POS<cr,lf>
```

A.7 SELECTING PULSE AMPLITUDE MODULATION (PAM)

The Pulse Generator can be pulse amplitude modulated from an external source. To externally modulate the Pulse Generator, apply a modulating signal not greater than 20 kHz to the PAM IN input. The CAMP command sets the pulse amplitude, and the CFRQ sets the pulse carrier frequency.

A.7.1 PAM Example

In this example, the Pulse Generator (at address 3) produces a 2MHz, 3Vp-p, 300ns pulse. The external signal (MATE compatible Function Generator at address 2) modulates the Pulse Generator with a 3Vp-p, 6 kHz triangle wave.

Write @ secondary address 2:

```
"FNC<b>TRI<b>:CH0<b>SET<b>VLPP<b>3<b>
SET<b>FREQ<b>6E3<cr><lf>"
```

Write @ secondary address 3:

```
"FNC<b>PAM<b>:CH0<b>SET<b>CAMP<b>3<b>SET
<b>CFRQ<b>2E6<b>SET<b>MDSC<b>INT<b>SET
<b>PLWD<b>300E-9<cr><lf>"
```

A.8 PULSE GENERATOR ERROR MESSAGES

Table A-6 lists all the possible Pulse/Timing Generator error messages that could occur during normal operation. Each message contains in quotes a brief explanation of the messages meaning. One of two ASCII strings ("`F07PLG00(MOD):`" or "`F07PLG00(DEV):`") precedes each error message.

When the term <ASCII> appears in the error messages listed below, it represents any continuous string of ASCII characters except space, tab, LF, CR. . This string can represent valid nouns, modifiers, or data, as well as misspelled or garbage strings. If the string syntax is valid, then the string could be out of order or there could be some other reason the string was not accepted.

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Table A-8. Error Messages

Error Message	Comments
"<ASCII> not allowed"	This ASCII string cannot be used as entered.
"<ASCII> missing"	A mandatory modifier is missing in the command string. For example, the PDC command requires a VLPK modifer.
"<ASCII> limit error"	The value sent exceeds the modifier's limit.
"GSTA/GSTO slope error"	Both the gate start and stop slopes were set to the same value.
"channel number error"	Only channel 0 can be used with the Pulse Generator, because it has only one programmable output.
"setting missing from FNC command"	The command string was correct up to the mandatory SET modifier which is missing.
"INT/EXT not allowed with <ASCII>"	The modifier is correct, but INT or EXT are not valid modifier values.
"POS/NEG not allowed with <ASCII>"	The modifier is correct, but POS or NEG are not valid modifier values.
"numeric value not allowed with <ASCII>"	The modifier sent does not accept numeric values. TRSC and GASC are examples of modifiers that do not take numeric values.
"value needed with <ASCII>"	The modifier noted in the ASCII string requires a value.
"command terminated before complete"	"FNC PDC<cr><lf>" causes this error message. The command string is correct up to the terminating characters. But, the entire command string is incomplete.
"<ASCII>"	This message represents any Pulse Generator dependent error message.
"TRSL/TRLV not allowed with GASC"	Trigger slope and trigger level values are not valid when set up for a gate source.
"TRSL/TRLV need TRSC EXT"	Trigger slope and trigger level values are only valid when set up for an external trigger source.
"GSTA/GSTO/GALV not allowed with TRSC"	Gate slope and level not valid when using a trigger source.
"GSTA/GSTO/GALV need GASC EXT"	Gate slope and level only valid when using an external gate source.
"BURS not allowed with GASC, needs TRSC"	Burst mode uses TRSC (internal or external trigger source).
"50.0 ohm impedance only"	The only valid arguement for TIMP is 50Ω.
"TRFR is not allowed for EXT source"	TRFR is the internal trigger frequency.
"TRFR is mandatory for INT source"	Must specifiy an internal triggering frequency when triggering from the internal source.
"EXT source only with MDSC"	There is no internal source for PAM modulation source.
"MDSC only allowed with PAM"	Set up the modulation source only with PAM.

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Format of Common Commands

OPN<b>CH0<CR/LF>
CLS<b>CH0<CR/LF>

RST<b> ⟨ PDC / PDT / SQW ⟩ <b>CH0<CR/LF>

IST<CR/LF> PAM
CNF<CR/LF>
STA<CR/LF>

Modifiers Supported in each Function (noun)

MODIFIER	NOUN			
	PAM	PDC	PDT	SQW
BURS	•	•	•	•
CAMP	•			
CFRQ	•			
DCOF		•	•	•
DELA	•	•		
FALL	•	•	•	•
FREQ				•
GALV	•	•	•	•
GASC	•	•	•	•
GSTA	•	•	•	•
GSTO	•	•	•	•
MDSC	•			
PERI		•		•
PLWD	•	•	•	
PRFR	•	•	•	
RISE	•	•	•	•
SPCG			•	
TIMP	•	•	•	•
TRFR	•	•	•	•
TRLV	•	•	•	•
TRSC	•	•	•	•
TRSL	•	•	•	•
VLPK		•	•	•
VLPP				•
VRMS				•

Figure A-1. Pulse Generator CIIL Syntax Diagrams.

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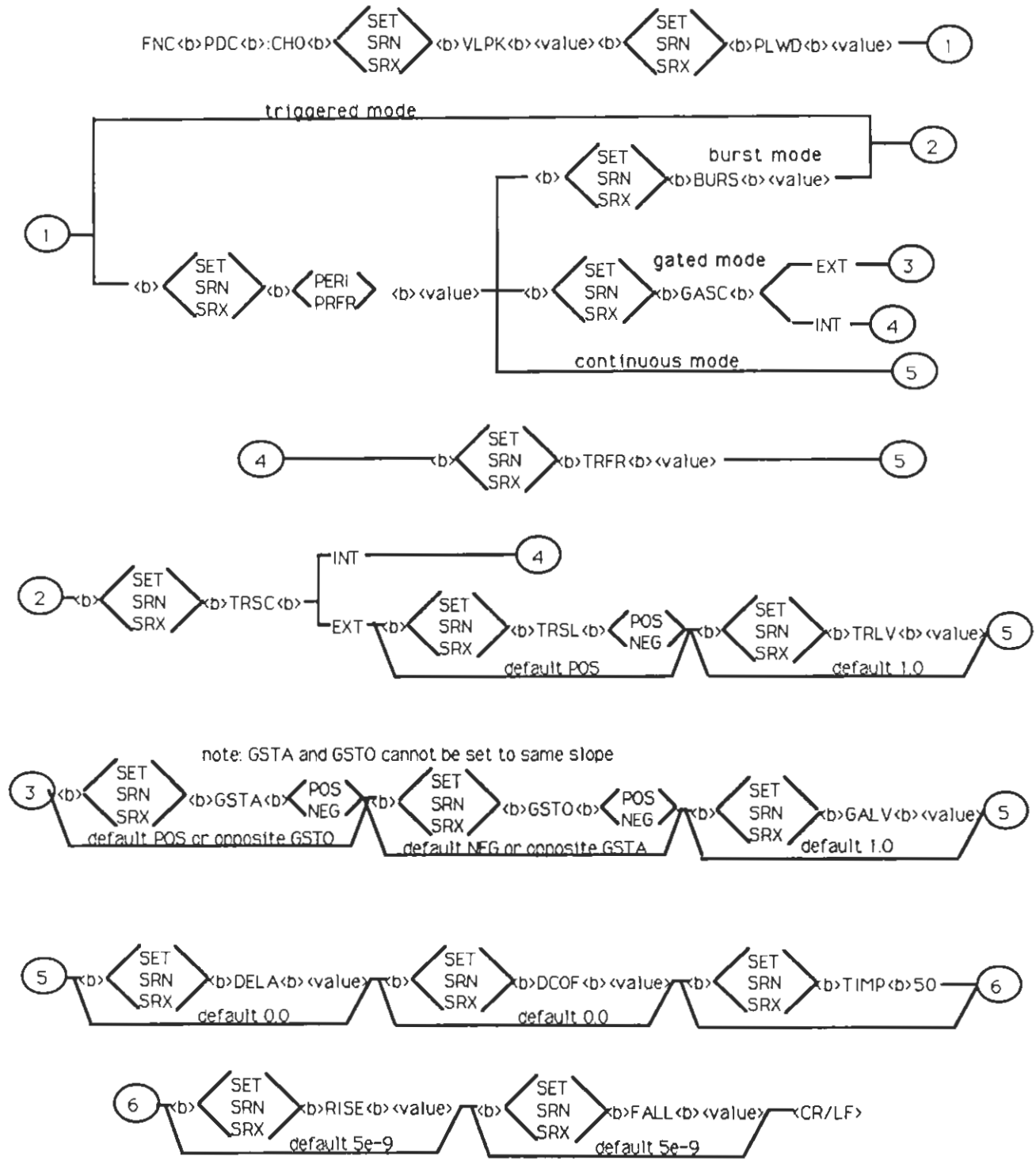


Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

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Format for double pulse

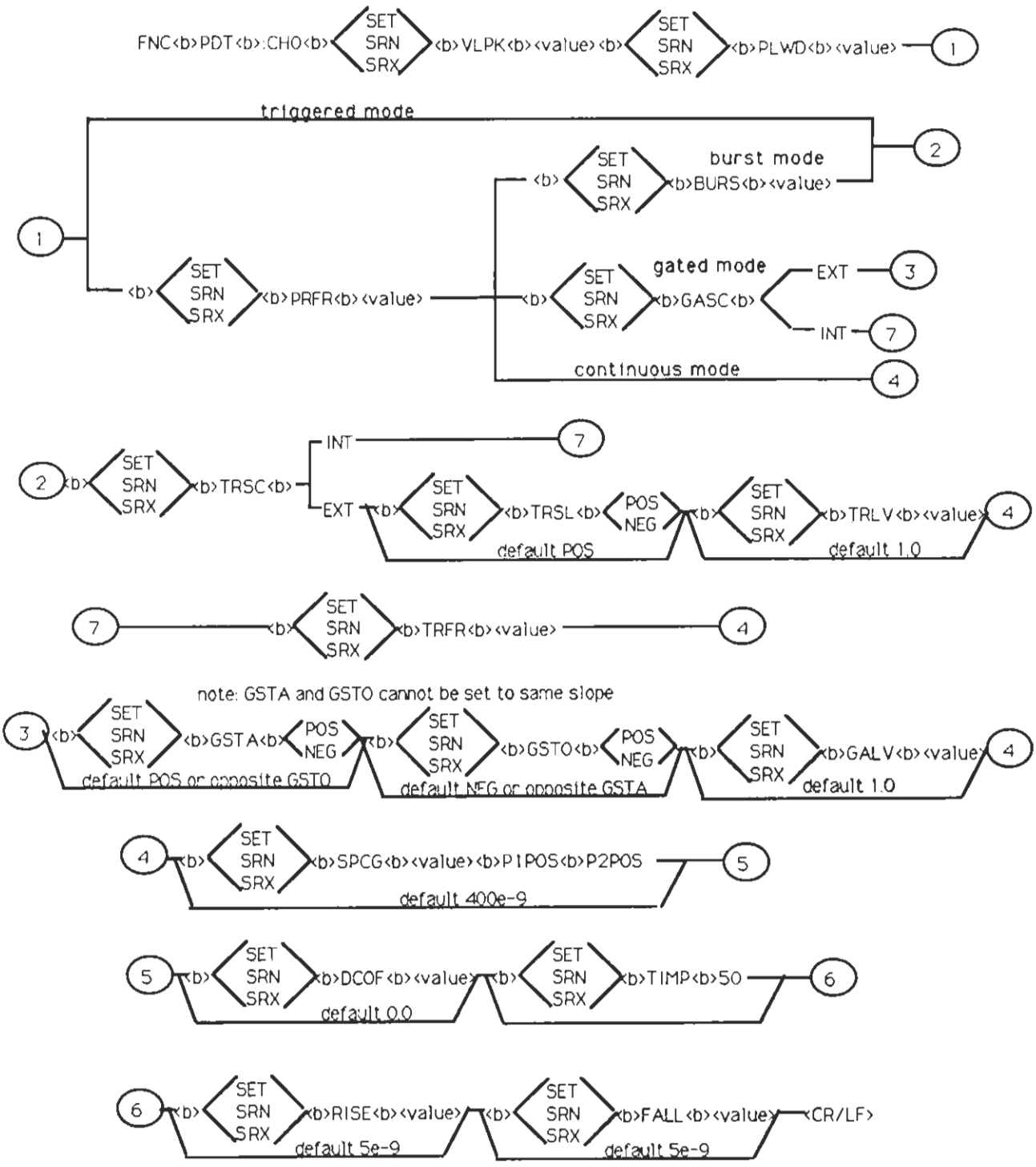


Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

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Format for square

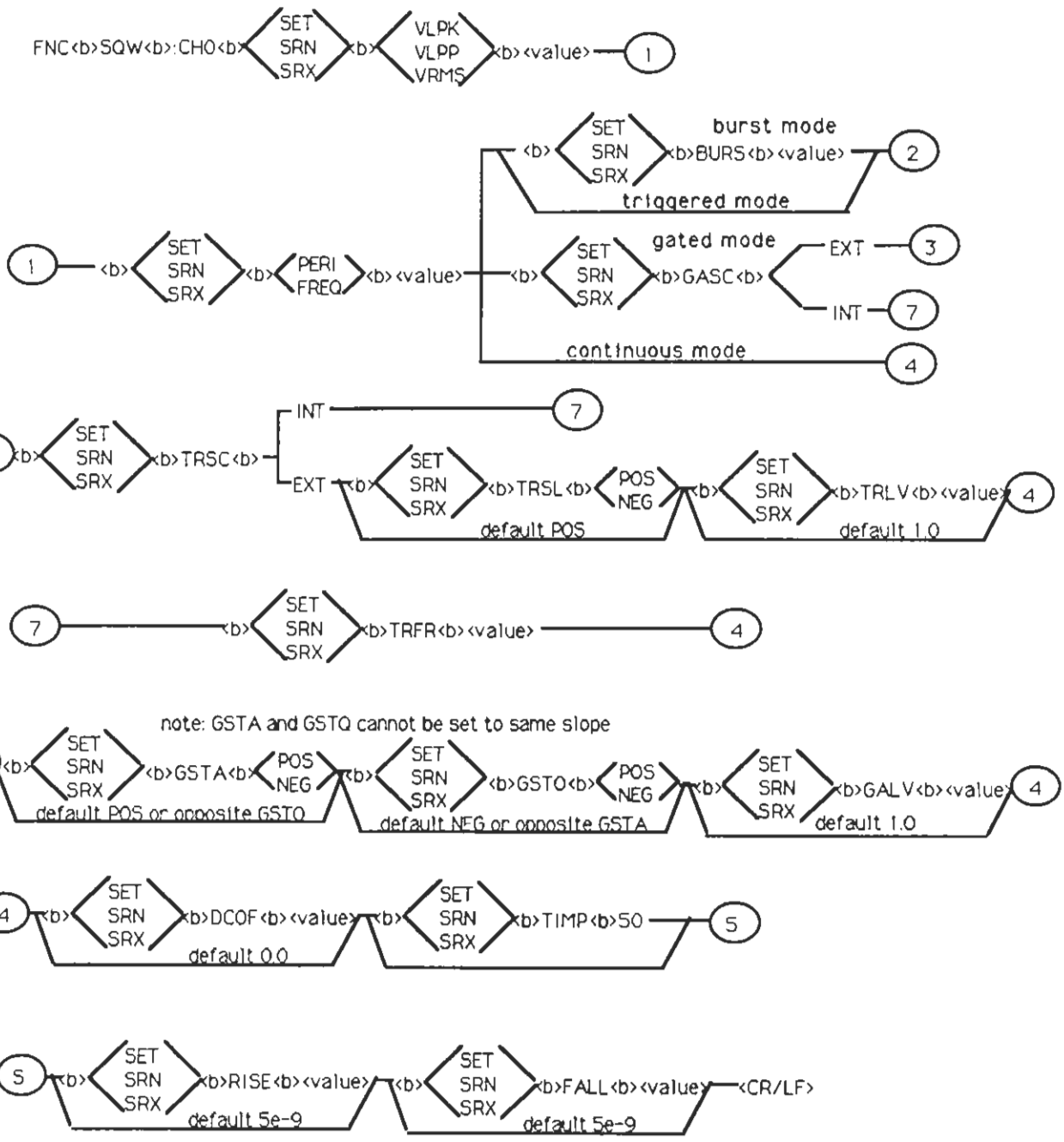


Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

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Format for pulse amplitude modulation

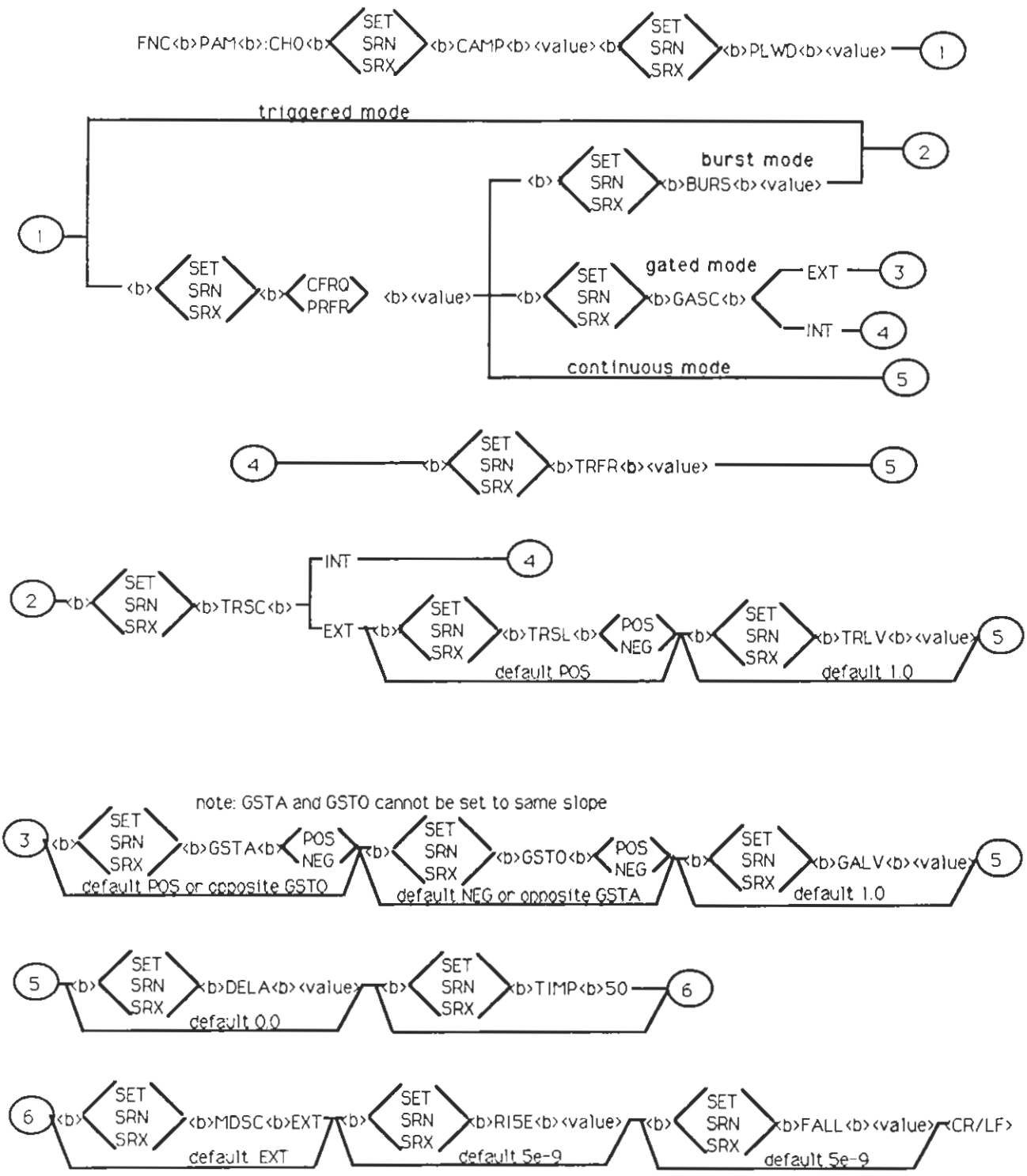


Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

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C.1 Introduction

This appendix provides the Operator/Programmer with additional information needed to interpret a non-zero response value to either the `*CAL?` IEEE-488.2 Common Command or to the SCPI `CALibrate[:ALL]?` query. This information supplements paragraphs 3.3.3.1 (`CALibrate`) and 3.3.4 (`*CAL?`).

C.1.1 CALibrate Query Response

***CAL?**

According to IEEE Std. 488.2-1987 section 10.38, the Calibration query causes an internal Self Calibration to be performed and a response to be placed in the Output Queue. The response to the `*CAL?` query is an ASCII string representing an integer value. The value of 0 is returned if the Self Calibration passed and a non-zero value in the range of 32767 to -32768 is returned if the Self Calibration failed. The interpretation of the value returned in the event of a failed self calibration is defined by the module manufacturer.

The `*CAL?` query invokes the same internal self calibration functions and returns the same reponse as the `CALibrate[:ALL]?` query documented below.

CALibrate[:ALL]?

The `CALibrate[:ALL]?` query returns a detailed error code indicating the nature of a failure. The value of a 16-bit Self Calibration Status Word is returned in response to the Calibration query. The format of the Self Calibration Status Word is shown below:

Self Calibration Status Word

The Self Calibration consists of performing all steps of the Alignment Procedure (Paragraph 5.5) which are indicated as "automatic". If the Self Calibration is successful, the module performs all of these steps and records "fresh" alignment data without external test equipment or operator adjustments, and then returns the value zero as a query response. There are four of these "automatic" Alignment steps, equivalent to sending the SCPI command `:DIAG:CAL? <n>` four times, where "n" equals 1,2,3, and 6.

If the Self Calibration is not successful, the Alignment data is not stored in the instrument and the query response is non-zero. The Error Code field contains a bit-weighted code that is unique to which parameter failed and has the following meaning:

Error Code Bit	Meaning
0	Amplitude
1	Offset
2	Delay gatable oscillator frequency
3	Width gatable oscillator frequency
4	Gatable trigger oscillator minimum frequency greater than 25MHz.
5	Gatable trigger oscillator maximum frequency less than 50 MHz.
6	-
14	Hardware failure.

The auto calibration sets the UUT back to its previous state after the calibration is complete. While performing the auto calibration the output relays remain open so as not to disturb any external devices. For each step, all parameters not listed under the bit number are at reset state during the Self Calibration.

C.1.2 Self Calibration Error Codes

Bit 0 & 1: Amplitude and Offset Error

The Model 1391 is set up according to a `:DIAG:CAL? 6` command, as follows:

```
RESET
VOLT 5
FREQ 1e3
FUNC SQUARE
INIT:CONT    OFF
TRIG:SOUR    TOFF
PULS:POLARITY    COMPLEMENT
```


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The amplitude and offset DAC's are set to 0. The output voltage is read and if it is outside of ± 1.0 volt, bit 1 is set. The offset DAC is then set to 910 (approx. +5.5 V offset). If the output voltage is not between 4.5 Vdc and 6.5 Vdc, bit 1 is set. The offset DAC is then set to 3185 (approx. -5.5 V offset). If the output voltage is not between -6.5 Vdc and -4.5 Vdc, bit 1 is set. The offset DAC is set back to 0 and the amplitude DAC is set to 3185 (approx. +6.5 V level). If the output voltage is not between 5.5 Vdc and 7.5 Vdc, bit 0 is set. The amplitude DAC is set to 910 (approx. +2.0 V level). If the output voltage is not between 1.0 Vdc and 3.0 Vdc, bit 0 is set. These measured values are used to establish zero offset and the value "mV/bit" in amplitude and offset setup routines. These values are saved in the cal data base unless an error occurs, at which time the default values are saved.

Bit 2: Delay Gatable Oscillator Frequency Error

The Model 1391 is set up according to a :DIAG:CAL? 3 command, as follows:

```
RESET
VOLT 5
INIT:CONT    OFF
TRIG:SOUR    BUS
TRIG:COUN 50
PULS:DELAY 500e-6
```

The pulse delay is measured and then the gatable oscillator frequency is determined. If the oscillator frequency is not between 95e6 and 115e6, then bit 2 is set.

Bit 3: Width Gatable Oscillator Frequency Error

The Model 1391 is set up according to a :DIAG:CAL? 2 command, as follows:

```
RESET
VOLT 5
INIT:CONT    OFF
TRIG:SOUR    BUS
TRIG:COUN 50
PULS:WIDTH 500e-6
```

The pulse width is measured and then the gatable oscillator frequency is determined. If not between 95e6 and 115e6, then bit 3 is set.

Bit 4 & 5: Trigger Gateable Oscillator Frequency Error

The Model 1391 is set up according to a :DIAG:CAL? 1 command, as follows:

```
RESET
VOLT 5
FREQ 25e6
FUNC SQUARE
INIT:CONT    OFF
TRIG:SOUR    BUS
TRIG:COUN 50
```

The trigger gatable oscillator DAC is set to 0 and frequency is measured, then the DAC is incremented by 585 and measured until the maximum DAC value is reached. The span should be from less than 25 MHz to greater than 50MHz. If minimum value is > 25e6 then bit 4 is set. If maximum value is < 50e6 then bit 5 is set.

Bit 14: Hardware Error

The processor had a bus failure in trying to access hardware.

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D.1 INTRODUCTION

This appendix provides the Operator/Programmer with additional information needed to interpret a non-zero response value to either the *TST? IEEE-488.2 Common Command or the SCPI TEST[:ALL]? query. This information supplements paragraphs 3.3.3.2 (TEST) and 3.3.4 (*TST?).

D.1.1 TEST Query Response

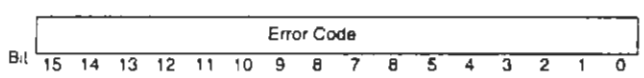
***TST?**

According to IEEE Std. 488.2-1987 section 10.38, the self test query causes an internal Self Test to be performed and a response to be placed in the Output Queue. The response to the *TST? query is an ASCII string representing an integer value. The value of 0 is returned if the Self Test passed, and a non-zero value in the range of 32767 to -32768 is returned if the Self Test failed. The interpretation of the value returned in the event of a failed Self Test is defined by the module manufacturer.

The *TST? query invokes the same internal Self Test functions and returns the same response as the TEST[:ALL]? query documented below.

TEST[:ALL]?

The TEST[:ALL]? query returns a detailed error code indicating the nature of any failure. The value of a 16-bit Self Test Status Word is returned in response to the TEST[:ALL]? query. The format of the Self Test Status Word is shown below:



Self Test Status Word

The Error Code field contains a bit weighted code that is defined in the following table.

Error Code Bit	Meaning
0	Amplitude DAC Control
1	Trailing Edge DAC control & <10ns control
2	Leading Edge DAC control & <10ns control
3	Limit amplifier
4	SUMBUS
5	Delay gateable oscillator
6	Width gateable oscillator
7	25-50 MHz gateable oscillator
8	-
14	Hardware bus error

If no failures were detected by the self test then the Error Code field will be set to zero.

The Self Test saves the state of the instrument prior to starting and restores it after the test is complete. While performing the Self Test, the output relays remain open so as not to disturb any external devices.

D.1.2 Self Test Error Codes

Bit 0: Amplitude DAC

The model 1391 is set according to the following:

RESET

Program amplitude DAC to 0.

Set bit zero (Fail the test) if voltage at ADCCH1 is outside ± 0 .1 Vdc. Program amplitude DAC to 4095 and Set bit zero if voltage at ADCCH1 is outside of 1.048 Vdc ± 0.25 Vdc.

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Bit 1: Trailing Edge DAC

The model 1391 is set according to the following:

```
RESET
```

Program trailing edge DAC to 0 and set bit 1 if voltage at ADCCH2 is > 0.25 Vdc. Program trailing edge DAC to 4095 and set bit 1 if voltage at ADCCH2 is < 3.361 Vdc or > 4.071 Vdc. Program U11-6 & 7 high and set bit 1 if the voltage at ADCCH2 is < 2.761 Vdc or > 3.361 Vdc.

Bit 2: Leading Edge DAC

The model 1391 is set according to the following:

```
RESET
```

Program leading edge DAC to 0 and set bit 2 if the voltage at ADCCH3 is < –0.25 Vdc. Program leading edge DAC to 4095 and set bit 2 if the voltage at ADCCH3 is < -4.089 Vdc or > -3.389 Vdc. Program U11-6 & 7 high and set bit 2 if voltage at ADCCH3 is < -3.3006 Vdc or > -2.706 Vdc.

Bit 3: Limit Amplifier

The model 1391 is set up according to the following:

```
RESET
```

Set bit 3 if the voltage at ADCCH4 is outside ± 0.15 Vdc.

Bit 4: SUMBUS

the model 1391 is set up according to the following:

```
RESET
```

Program U7-5 high and set bit 4 if the voltage at ADCCH5 is outside ± 0.05 Vdc.

Bit 5: Delay Gateable oscillator

The model 1391 is set up according to the following:

```
FREQ 1e3
VOLT 5
PULS:WIDT 250e-6
PULS:DEL 125e-6
FUNC PULSE
TRIG:SOUR BUS
INIT:CONT OFF
TRIG:COUN 50
```

Program U13-6 low and U13-3,4,& 5 high to select the delay pulse signal for the internal measurement circuit. Measure delay and set bit 5 if the delay value is not between 100e-6 and 150e-6.

Bit 6: Width Gateable oscillator

The model 1391 is set up according to the following:

```
FREQ 1e3
VOLT 5
PULS:WIDT 250e-6
PULS:DEL 125e-6
FUNC PULS
TRIG:SOUR BUS
INIT:CONT OFF
TRIG:COUN 50
```

Measure the width and set bit 6 if the width value is not between 200e-6 and 300e-6.

Bit 7: 25-50 MHz Gateable oscillator

the model 1391 is set up according to the following:

```
FREQ 666.7
VOLT 5
FUNC SQUARE
TRIG:SOUR BUS
INIT:CONT OFF
TRIG:COUN 50
```

This setup generates a 749.9625 e-6 width signal to measurement circuit. Measure width and set bit 7 if the width value is not between 700e-6 and 800e-6.

Bit 14: Hardware Bus failure.

The processor had a bus failure in trying to access hardware.

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E.1 INTRODUCTION

This Appendix contains compliance data as required by the SCPI 1992 Specification, Volume 1: Syntax and Style. Specifically, paragraph 4.2.3, Documentation Requirements, specifies the Conformance Information requirements for SCPI products.

E.2 MODEL 1391 SCPI VERSION

The Model 1391 VXIbus Pulse Generator has been designed to comply with SCPI Version 1992.0, dated February 1992.

E.3 MODEL 1391 SCPI COMMAND SYNTAX

The SCPI specification, Version 1992.0, defines three type of SCPI commands which may be used in a SCPI product: Confirmed Commands, Approved Commands, and commands which are not part of the SCPI definition.

E.3.1 SCPI Confirmed Commands

Confirmed Commands are those commands which are published in the SCPI 1992 Specification, Volume 2: Command Reference. Refer to Table E.1 for the complete syntax of Model 1391 SCPI commands. Model 1391 Confirmed Commands will be identified with with the notation "Confirmed" in the third column.

E.3.2 SCPI Approved Commands

Approved Commands are those commands which have been approved by the SCPI Consortium, but are not published in the SCPI 1992 Specification. Refer to Table E.1 for the complete syntax of Model 1391 SCPI commands. Model 1391 Approved Commands will be identified with with the notation "Approved" in the third column.

E.3.3 Commands not part of the SCPI Specification

The SCPI Specification does allow products using the SCPI language to have specialized commands included which are outside of the SCPI definition. Refer to Table E.1 for the complete syntax of Model 1391 SCPI commands. Any Model 1391 commands which are not in the SCPI definition will be identified with the notation "Not SCPI Approved" in the third column.

E.3.4 Incomplete Command Inplementation

The SCPI definition specifies each command completely, and if the command keyword is at the *leaf node*, it specifies the parameter data and query responses. In some cases, a SCPI product may not implement all of the choices given in the specification.

For example, when parameter character data is in the form of a list of choices, the product's hardware may not support all of those choices:

```
[SOURce]:FREQuency:MODE
   <CW|FIXed|SWEep|LIST|SENSe>
```

In this example, a complete list of possible Frequency Modes is given. However, the product's feature set may want to have a settable Frequency Mode in order to set a CW/FIXED frequency, and to enter a Frequency Sweep Mode. The other Modes, LIST and SENSe, may not have any hardware to support them. In this case, the SCPI Syntax Table (see Table E.1) would use footnotes to indicate partial conformance to the SCPI Specification.

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Table E-1. Model 1391 SCPI Command Syntax

KEYWORD	PARAMETER FORM	NOTES
CALibration		Confirmed
[:ALL]?		Confirmed
INITiate		Confirmed
[:IMMediate]		Confirmed
:CONTinuous	<Boolean_data> (ON)	Confirmed
OUTPut		Confirmed
:ECLTrg<n>		Confirmed
[:STATe]	<Boolean_data> (OFF)	Confirmed
:SOURce	<TRIP | PULSe>	Confirmed[1]
[:STATe]	<Boolean_data> (OFF)	Confirmed
:SUMBus		Not SCPI Approved
[:STATe]	<Boolean_data> <OFF)	Not SCPI Approved
:TTLTrg<n>		Confirmed
[:STATe]	<Boolean_data> (OFF)	Confirmed
:SOURce	<TRIP | PULSe>	Confirmed [1]
RESet		Confirmed
[SOURce]		Confirmed
:FREQuency		Confirmed
[:CW | FIXed]	<numeric_value>	Confirmed
:FUNCtion		Confirmed
[:SHAPe]	(<PULSe | SQUare>)	Confirmed [1]
:MARKer		Confirmed
:TYPE	<CLOCk | GATE>	Not SCPI Approved [1]
[:STATe]	<Boolean_data> (OFF)	Confirmed
:PULSe		Confirmed
:WIDTh	<numeric_value>	Confirmed
:DELay	<numeric_value>	Confirmed
:DOUBle		Confirmed
:DELay	<numeric_value>	Confirmed
[:STATe]	<Boolean_data> (OFF)	Confirmed
:POLarity	<NORMal | COMPlement | INVerted>	Confirmed
:PERiod	<numeric_value>	Confirmed
:TRANsition		Confirmed
:STATe	<Boolean_data> (OFF)	Confirmed
[:LEADing]	<numeric_value>	Confirmed
:TRAiling	<numeric_value>	Confirmed
:AUTO	<Boolean_data> (ON)	Confirmed [2]
:SUMBus		Not SCPI Approved
[:STATe]	<Boolean_data> (OFF)	Not SCPI Approved
:VOLTage		Confirmed
[:LEVel]		Confirmed
[:IMMediate]		Confirmed
:HIGH	<numeric_value>	Confirmed
:LOW	<numeric_value>	Confirmed
[:AMPLitude]	<numeric_value>	Confirmed
:OFFSet	<numeric_value>	Confirmed

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Table E-1. Model 1391 SCPI Command Syntax (Continued)

KEYWORD	PARAMETER FORM	NOTES
[SOURce] (Continued)		
:PULM		Confirmed
[:STATe]	<Boolean_data> (OFF)	Confirmed
:AMPLitude	<BIPolar | POSitive | NEGative>	Not SCPI Approved [1]
STATus		Confirmed [3]
:OPERation		Confirmed [3]
:CONDition?		Confirmed [3]
:ENABle	<numeric_value>	Confirmed [3]
[:EVENt]?		Confirmed [3]
:QUEStionable		Confirmed [3]
:CONDition?		Confirmed [3]
:ENABle	<numeric_value>	Confirmed [3]
[:EVENt]?		Confirmed [3]
:PRESet		Confirmed [3]
SYSTem		Confirmed
:ERRor?		Confirmed
:DATE	<year>, <month>, <day>	Confirmed
:TIME	<hour>, <minute>, <second>	Confirmed
:VERSion?		Confirmed
:LANGuage		Confirmed [4]
:CIIL		Confirmed [4]
TRIGger		Confirmed
:COUNt	<numeric_value>	Confirmed
:LEVel	<numeric_value>	Confirmed
:GATE		Not SCPI Approved
[:STATe]	<Boolean_data> (OFF)	Not SCPI Approved
:MODE	<SYNChronous | EXTWidth>	Not SCPI Approved [1]
:MODE	<MASTer | SLAVe>	Not SCPI Approved [1]
:SLOPe	<POSitive | NEGative>	Confirmed [2]
:SOURce	<INTernal | BUS | EXTernal | TTLTrg<n>| ECLTrg<n> | TOFF>	Confirmed [1,2]
:TIMer	<numeric_value>	Confirmed
DIAGnostic		Confirmed
:CALibrate?	<step>	Confirmed [1]
:CALibrate		Confirmed [1]
:MEASure	<step>,<numeric_value>	Confirmed [1]
:SAVE		Confirmed [1]
:INIT		Confirmed [1]
TEST		Confirmed
[:ALL]?		Confirmed

1. Device dependent parameter character data.
2. Incomplete implementation; at least one parameter not supported per SCPI specification.
3. STATus Subsystem commands operate per the specification, but the physical Status Registers are not implemented in the hardware.
4. "System Language" specifies device dependent parameter character data; implemented CIIL as keyword.

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