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numa·logic

PC-100/110 Systems Manual

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Since the equipment explained in this manual has a variety of uses, the user and those responsible for applying this equipment must satisfy themselves as to the acceptability of each application and use of the equipment. Under no circumstances will Westinghouse Electric Corporation be responsible or liable for any damage, including indirect or consequential losses resulting from the use, misuse, or application of this equipment.

The text, illustrations, charts, and examples included in this manual are intended solely to explain the use and application of the **Numa-Logic** PC-100 and PC-110 Programmable Controllers. Due to the many variables associated with specific uses or applications, Westinghouse Electric Corporation **cannot** assume responsibility or liability for actual use based upon the data provided in this manual.

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PC-100/110 Programmable Controllers Systems Manual

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Section 1
Introduction and System Overview

1-1. Unpacking Procedures

Numa-Logic programmable controllers and associated hardware are extensively tested and carefully packaged prior to shipment. Upon delivery, inspect this equipment for visible damage, and take an inventory to verify that both the quantities and types of components ordered have been delivered. The equipment should also be tested to insure that it is operational.

NOTE: File any claim for damages with the carrier, or its agent. Also, notify your Westinghouse representative so that corrective action can be taken at the earliest possible time.

1-2. Basic Control Systems

Control systems basically consist of three sections, as shown in Figure 1-1.

- an **input section**, which gathers the information required to keep track of the real-world operations being controlled;
- a **logic section**, which processes the information acquired by the input section, and which determines which output function should be activated; and
- an **output section**, which provides control by activating the appropriate devices within the real-world operations being controlled.

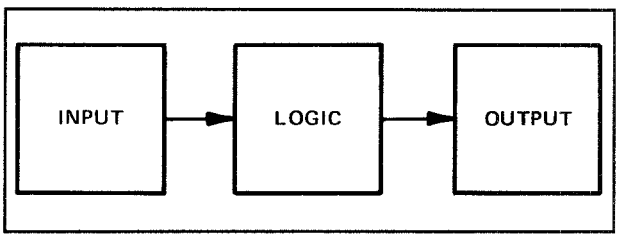


Figure 1-1. Three Sections of Any Control System

The three basic sections of a relay control system are symbolically shown in Figure 1-2. In relay control applications, the input section consists of input devices, such as pushbuttons, limit switches and photocells. The logic section is composed of control relays wired together to produce the desired real-world operations. The output section contains output devices, such as motor starters, solenoids and indicator lights.

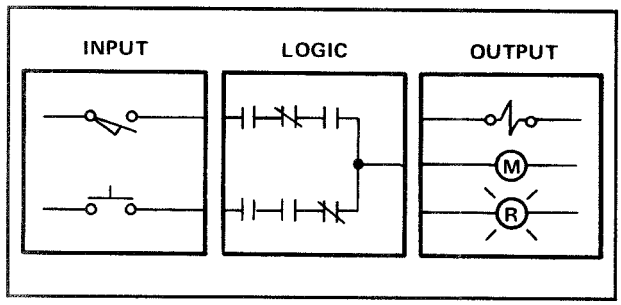


Figure 1-2. Relay-type Control System

Figure 1-3 shows these three sections as they are represented for a programmable control system. The primary difference between the two types of systems is that the control relay logic is replaced by a solid-state processor and memory configuration. Through programming, the processor and memory digitally process all the data for system operation. The processor's memory is programmed to duplicate the required operating instructions of the control relay circuits.

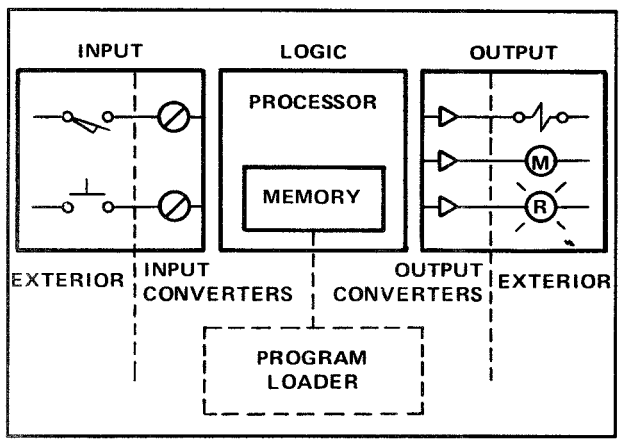


Figure 1-3. Three Sections of a Programmable Controller

The input section contains the same input devices that are found in the relay control system. However, the process input signals produced by these input devices are converted into low-level DC logic voltages suitable for solid-state controller operations. The output section in a programmable control system converts the

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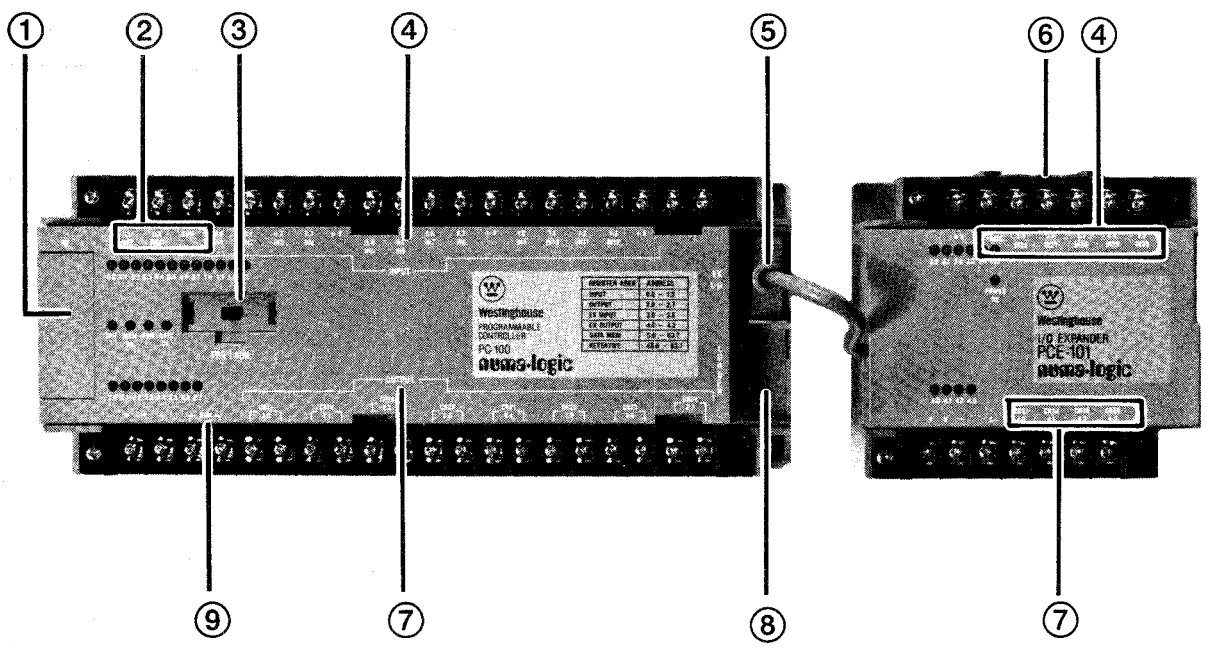
low-level logic signals from the processor into the voltage levels required to operate output devices. The output devices are the same as those utilized in relay control systems.

An advantage of this type of control is the ease with which the system's control logic can be modified into a variety of operating configurations by means of a program loader.

1-3. System Overview

The Numa-Logic PC-100 and PC-110 programmable controllers offer outstanding control capabilities for applications requiring from 20 to 112 inputs and outputs. To provide maximum flexibility in a minimum amount of space, the power supply, CPU, memory, and primary input and output circuitry are all combined into a single, compact package.

Along with its built-in power supply and logic capabilities, the PC-100 provides twelve input circuits and eight output circuits. The PC-100 can also support an I/O Expander that supplies an additional six input circuits and four output circuits for a maximum total of 30 I/O in a PC-100 system. The PC-100's processor has a program capacity of 320 words and also provides 64 data registers.

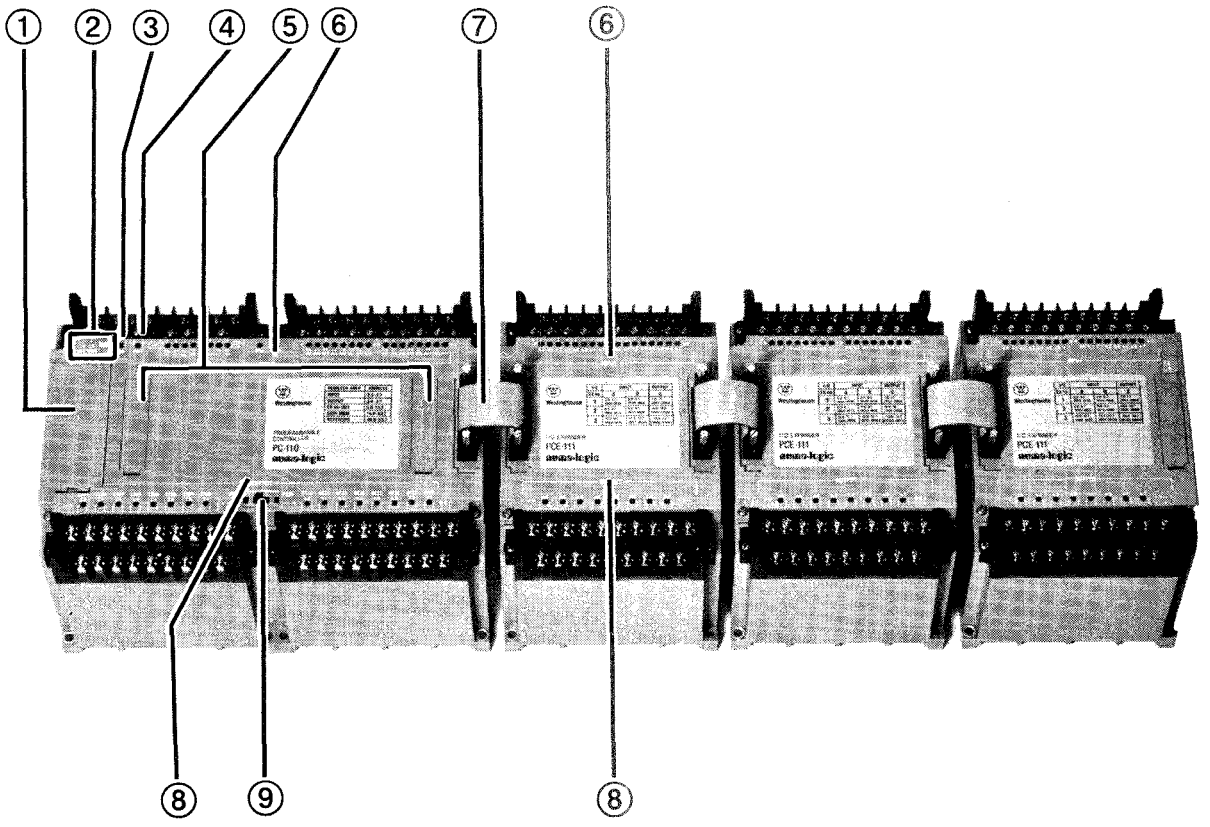


① NLB-100 Battery Cartridge and NLEP-191 EPROM Cartridge Interface
② 24 VDC or 120/220 VAC, 50/60 Hz
③ Mode Selector Switch
④ 24 VDC Dry Contact or 120 VAC Input Circuits
⑤ PCE-101 I/O Expander Cable Interface
⑥ ○○○ 24 VDC or 120/220 VAC 50/60 Hz
⑦ Relay, Triac, or DC Source Output Circuits
⑧ NLLA-185 Loader Adapter Cable Interface
⑨ External Run Contact

Figure 1-4. PC-100 Programmable Controller System

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The PC-110, like the PC-100, includes an integral power supply and processor and provides 24 input circuits and 16 output circuits. The PC-110 can support up to three I/O Expanders, each supplying an additional 16 input circuits and 8 output circuits for a maximum system total of 112 I/O. The PC-110's processor has a program capacity of 1024 words and also provides 64 data registers.



① NLB-100 Battery Cartridge and NLEP-191 EPROM Chip Interface
② 24 VDC or 120/220 VAC, 50/60 Hz
③ External Run Contact
④ External Battery Contact
⑤ NLPL-180 Interface
⑥ 24 VDC Dry Contact or 120 VAC Input Circuits
⑦ PCE-111 Cable Interface
⑧ Relay, Triac, or DC Source Output Circuits
⑨ Mode Selector Switch

Figure 1-5. PC-110 Programmable Controller System

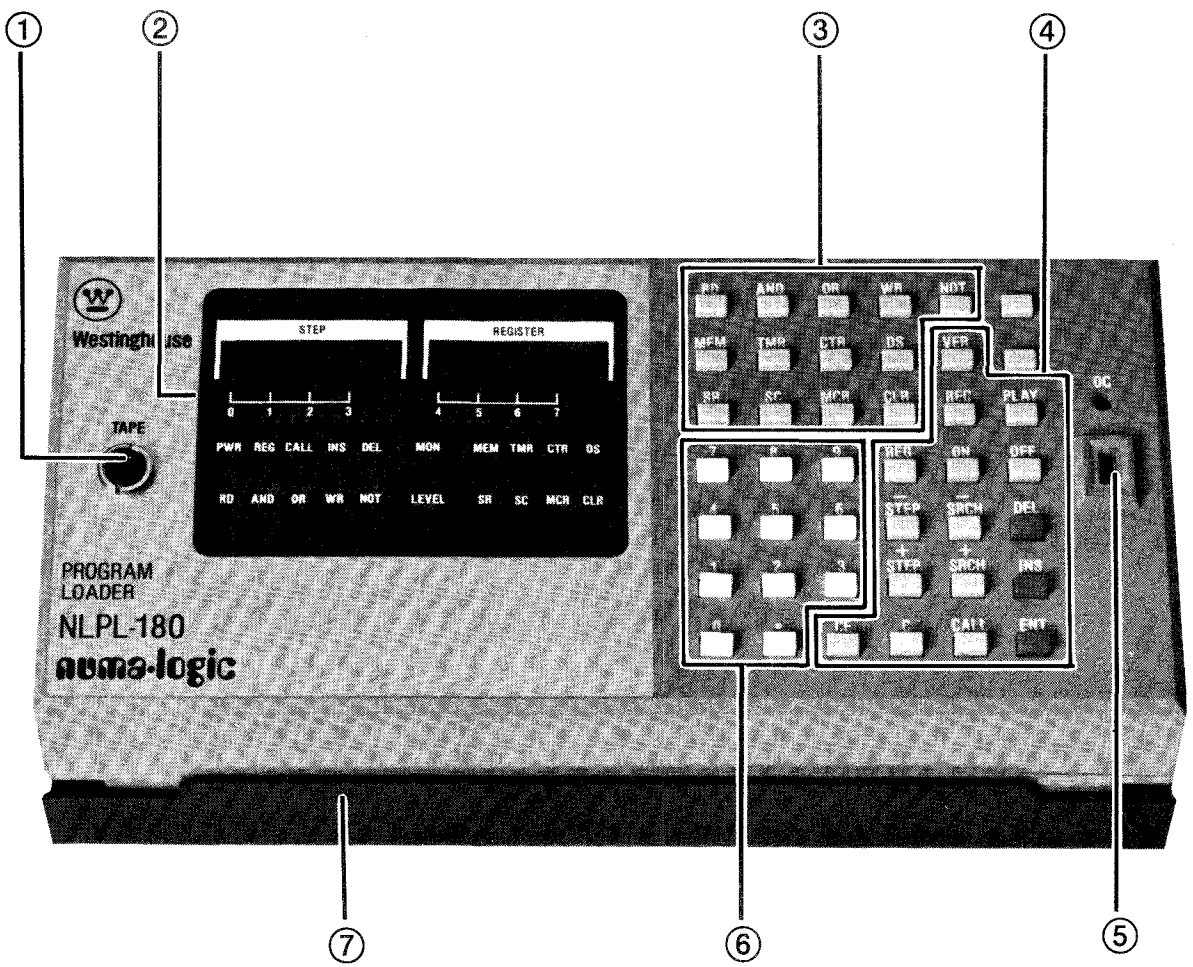
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The field-oriented construction of the PC-100 and PC-110 allow programming, wiring, and maintenance to take place easily from the front panel.

The PC-100 and PC-110 offer two means of back-up for their CMOS RAM. A capacitor, standard in both processors, will support memory for approximately two weeks. An optional lithium battery will provide back-up for up to three years.

For applications where the program will not be changed or where the processor will be idle for a long period, EPROM is available.

The NLPL-180 Program Loader is used to program both the PC-100 and the PC-110. Both systems share the same instruction set and data base, facilitating system expansion. The NLPL-180 is connected to the PC-100 via a loader adapter and cable for programming and monitoring. When interfacing to the PC-110, the loader can be snapped directly to the front panel of the processor or can be connected via a loader adapter and cable.



① Audio Cassette Tape Recorder Interface
② Program Instruction Display
③ Code Keys
④ Control Keys
⑤ Output Controller Switch
⑥ Numeric Keys
⑦ NLLA-185 Loader Adapter

Figure 1-6. NLPL-180 Program Loader

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TABLE 1-1. PC-100 AND ASSOCIATED HARDWARE

The following table outlines and briefly describes all of the available hardware options that can be incorporated into a PC-100 programmable controller system. For an illustration of how these hardware items are configured into a system, refer to Figure 1-7.

Item	I/O Points	Power Supply	Input① Type	Output Type	Remarks
PC-100	12/8	120 VAC 220 VAC 24 VDC	24 VDC 120 VAC	Relay DC Source Triac	320 program steps 64 data registers
PCE-101 I/O Expander	6/4	120 VAC 220 VAC 24 VDC	24 VDC 120 VAC	Relay DC Source Triac	Includes integral cable, 100 mm (3.94 in.)
NLPL-180 Program Loader					Also compatible with PC-110
NLLA-185 Loader Adapter					Required to interface NLPL-180 and NLEP-190 to PC-100; Includes NLC-185 Loader Adapter Cable
NLC-185 Loader Adapter Cable					Interfaces NLLA-185 to PC-100, 800 mm (31.50 in.)
NLB-100 Lithium Battery Cartridge					Provides memory back-up during power loss
NLEP-195 EPROM Cartridge					Provides non-volatile storage of program instructions
NLEP-190 EPROM Writer					Used in conjunction with PC-100 to store program contents on EPROM Cartridge; Compatible with PC-110
NLEP-193 Socket for EPROM Cartridge					Required to program EPROM Cartridge using EPROM Writer

①Voltage for 24 VDC input circuits is supplied by the processor's internal power supply.

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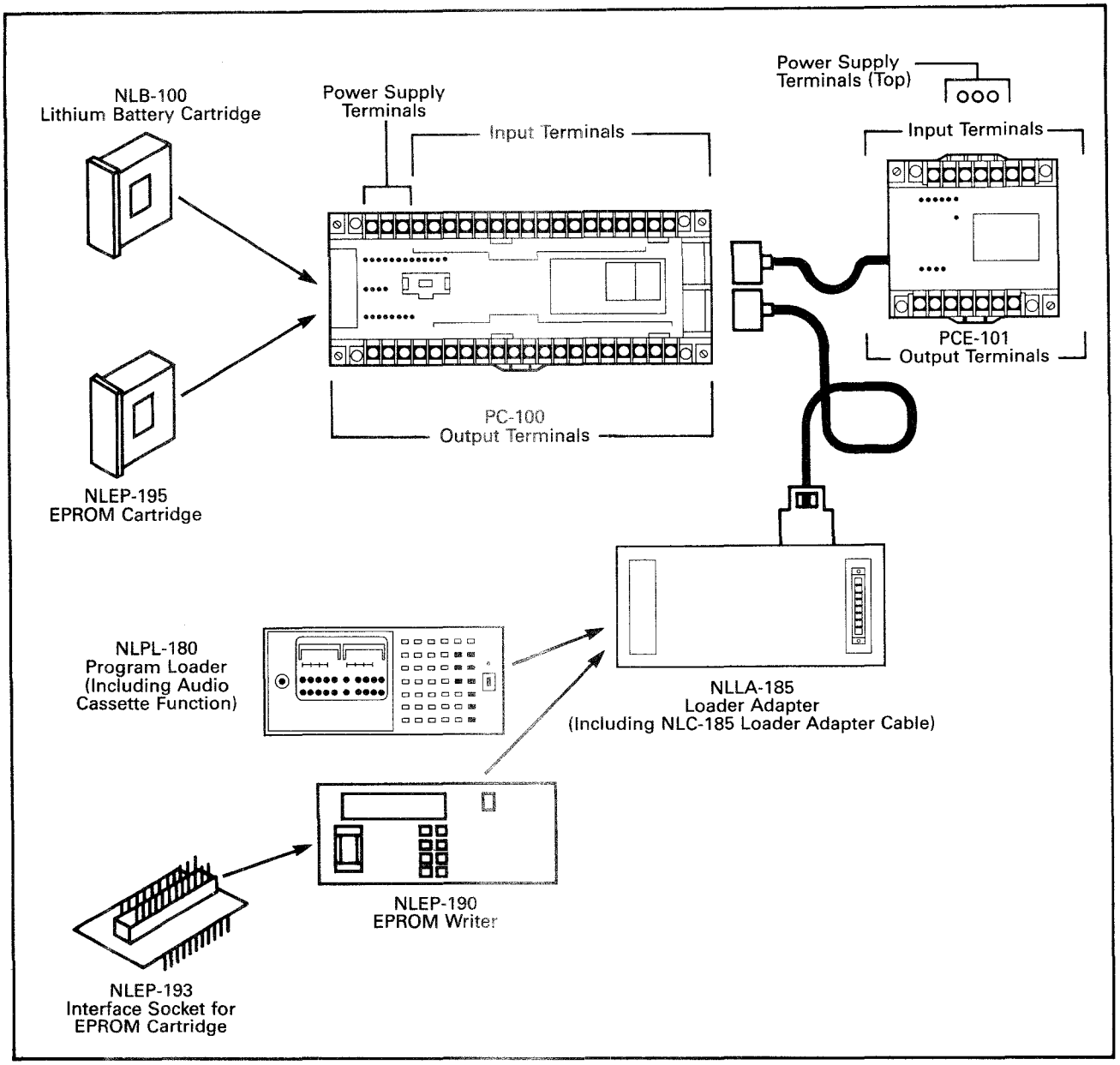


Figure 1-7. PC-100 System Configuration

TABLE 1-2. PC-100 I/O

Total Number of System I/O	20	30
I/O Distribution, Inputs/Outputs	12/8	18/12
Number of PC-100s (12 Inputs/8 Outputs)	1	1
Number of PCE-101 I/O Expanders (6 Inputs/4 Outputs)	0	1

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TABLE 1-3. PC-110 AND ASSOCIATED HARDWARE

The following table outlines and briefly describes all of the available hardware options that can be incorporated into a PC-110 programmable controller system. For an illustration of how these hardware items are configured into a system, refer to Figure 1-8.

Item	I/O Points	Power Supply	Input① Type	Output Type	Remarks
PC-110	24/16	120 VAC 220 VAC 24 VDC	24 VDC 120 VAC	Relay DC Source Triac	1024 program steps 64 data registers
PCE-111 I/O Expander	16/8	from PC-110	24 VDC 120 VAC	Relay DC Source Triac	Up to 3 PCE-111 units can be connected to a PC-110; Includes NLC-050 I/O Expander Cable
NLC-050 I/O Expander Cable for PCE-111					50 mm (1.97 in.)
NLC-400 I/O Expander Cable for PCE-111					400 mm (15.75 in.)
NLPL-180 Program Loader					Snaps directly to front panel of PC-110 or can be used with NLLA-185 and NLC-186; Also compatible with PC-100
NLLA-185 Loader Adapter					Allows hand-held use of NLPL-180
NLC-186 Loader Adapter Cable					Interfaces NLLA-185 to PC-110, 800 mm (31.50 in.)
NLB-110 Lithium Battery Unit					Provides memory back-up during power loss
NLEP-191 EPROM Chip					Provides non-volatile storage of program instructions
NLEP-190 EPROM Writer					Used in conjunction with PC-110 to store program contents on EPROM chip. Also compatible with PC-100

①Voltage for 24 VDC input circuits is supplied by the processor's internal power supply.

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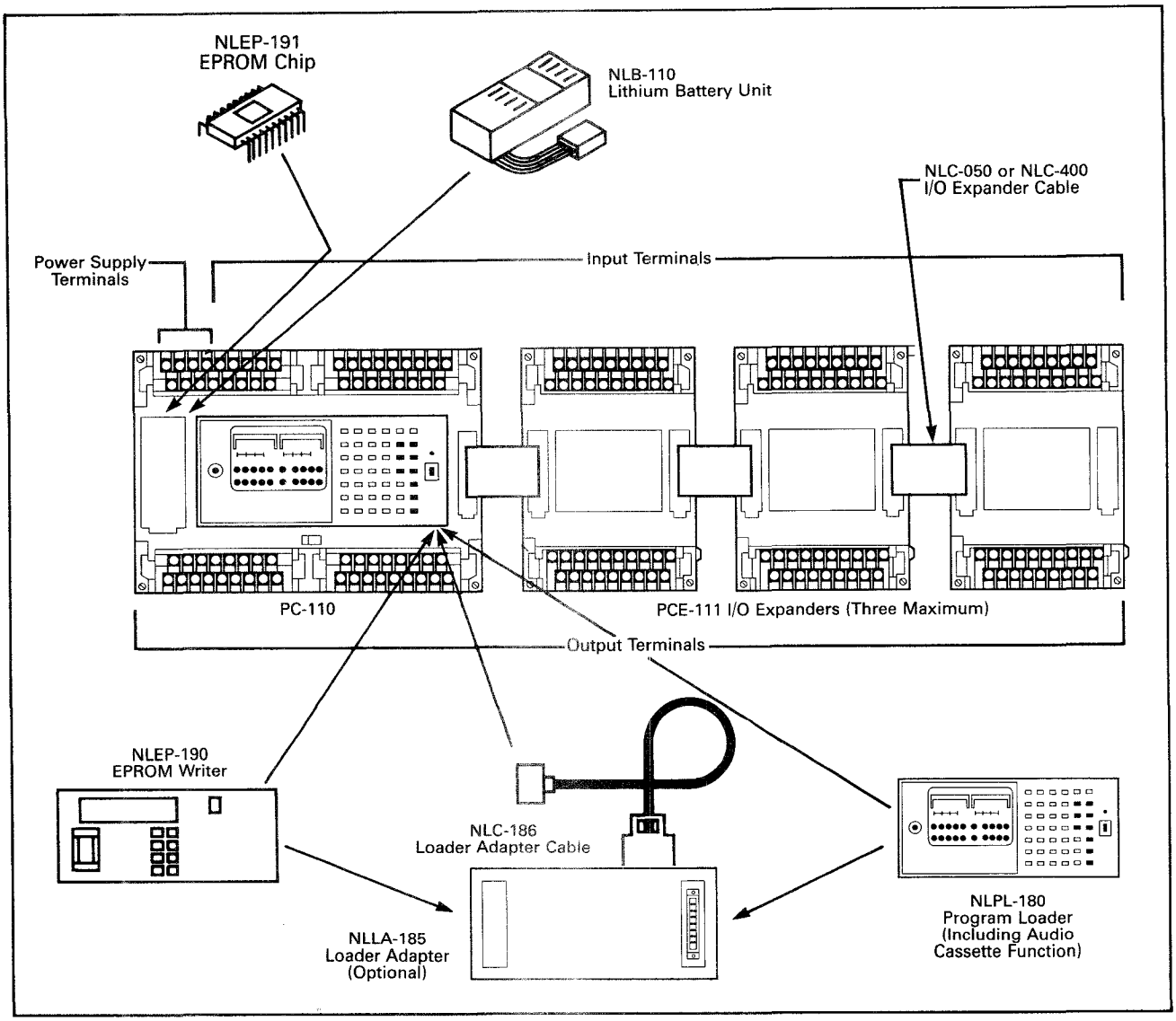


Figure 1-8. PC-110 System Configuration

TABLE 1-4. PC-110 I/O

Total Number of System I/O	40	64	88	112
I/O Distribution, Inputs/Outputs	24/16	40/24	56/32	72/40
Number of PC-110s (24 Inputs/16 Outputs)	1	1	1	1
Number of PCE-111 I/O Expanders (Each With 16 Inputs/8 Outputs)	0	1	2	3

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Section 2
Specifications

TABLE 2-1. LOADER SPECIFICATIONS

Item	Program Loader NLPL-180	EPROM Writer NLEP-190	Program Loader Adapter NLLA-185①
Functions	• Programming and monitoring • Program storage by means of audio cassette recorder	• Storing program onto EPROM cartridge and EPROM chip —Write —Verify —Read —EPROM Blank Check	• Required for interfacing NLPL-180 and NLEP-190 to PC-100 • Optional means of interfacing NLPL-180 and NLEP-190 to PC-110
External Dimensions, mm (in.)	200 (7.87) W x 90 (3.54) H x 44 (1.73) D	200 (7.87) W x 90 (3.54) H x 28.5 (1.12) D	202 (7.95) W x 91 (3.58) H x 38 (1.50) D
Weight, kg (lb.)	360 (0.79)	240 (0.53)	550 (1.20)

TABLE 2-2. GENERAL SPECIFICATIONS FOR PC-100 AND PC-110

Power Supply (ratings apply for 120 VAC and 220 VAC supplies)	
Tolerance	−15%, + 10%
Frequency	47 to 63 Hz
Dropout Tolerance	10 ms min.
Power Consumption	
PC-100	25 VA max.
PCE-101	10 VA max.
PC-110	70 VA max.
PCE-111	10 VA max. (each unit)
Operating Environment	0° to 50°C, 0 to 95% humidity, non-condensing
Storage Environment①	−20° to 85° C, 0 to 95% humidity, non-condensing
Dielectric Strength	1500 VAC, 1 min. between external terminal block and PC mounting plate
Noise Immunity	1000 V, 1 μsec
Insulation Resistance	500 VDC, 10 MΩ between external terminal block and PC mounting plate

①Storage temperature above 70° C will cause an approximate 20% decrease in the memory back-up period of the capacitor (normally 1,000 hours).

Storage temperature above 50° C will markedly reduce the life of the lithium battery. If the storage temperature of the programmable controller unit will exceed 50° C, store the lithium battery separately.

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TABLE 2-3. PC-100 SYSTEM SPECIFICATIONS

CPU	Operational/Control Functions	Logical operation: AND, OR, NOT Functional operation: Timer (0.1 to 12.7 sec.) Counter (1 to 127 counts) Shift Register (8 bits) Step Controller (8 steps) Master Control Relay I/O control: Read, Write Others: Clear, NOP (No operation)		
	Scan Time	5 ms/0.2 K words, 8 ms/320 words; speeds between these values are proportional to the program length		
Program Memory	Capacity	320 words		
	Type	CMOS RAM	Capacitor back-up: at 25° C, approx. one month at 50° C, approx. one week	
			Lithium battery (optional): approx. three years	
		EPROM (optional)		
Data Memory	Total Capacity	512 points (64 registers: I/O buffer memory, internal data memory, including retentive memory)		
	Retentive Memory	128 points (16 of 64 registers when the battery is installed) including 1 point reserved for battery error output		
Number of I/O Points	PC-100	Input: 12 points Output: 8 points	Total I/O points: 30	
	PCE-101 I/O Expander	Input: 6 points Output: 4 points		
I/O Signal Indication		Input: green LEDs; Output: red LEDs		
Self-diagnosis		Processor fault, parity error, watchdog timer, and battery status		
Control Output		Run confirmation contact (RUN)		
Applicable Program Tools		Program Loader NLPL-180 Loader Adapter NLLA-185 (includes NLC-185 Loader Adapter Cable) EPROM Writer NLEP-190		
Weight, kg (lb.)		1.20 (2.60)		

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TABLE 2-4. PCE-101 I/O EXPANDER

Number of Input Points	6
Number of Output Points	4
I/O Signal Indication	Input: green LED Output: red LED
Weight, kg (lb.)	0.5 (1.1)
Length of I/O Expander Cable, mm (in.)	100 (3.94) (permanently connected to I/O Expander)

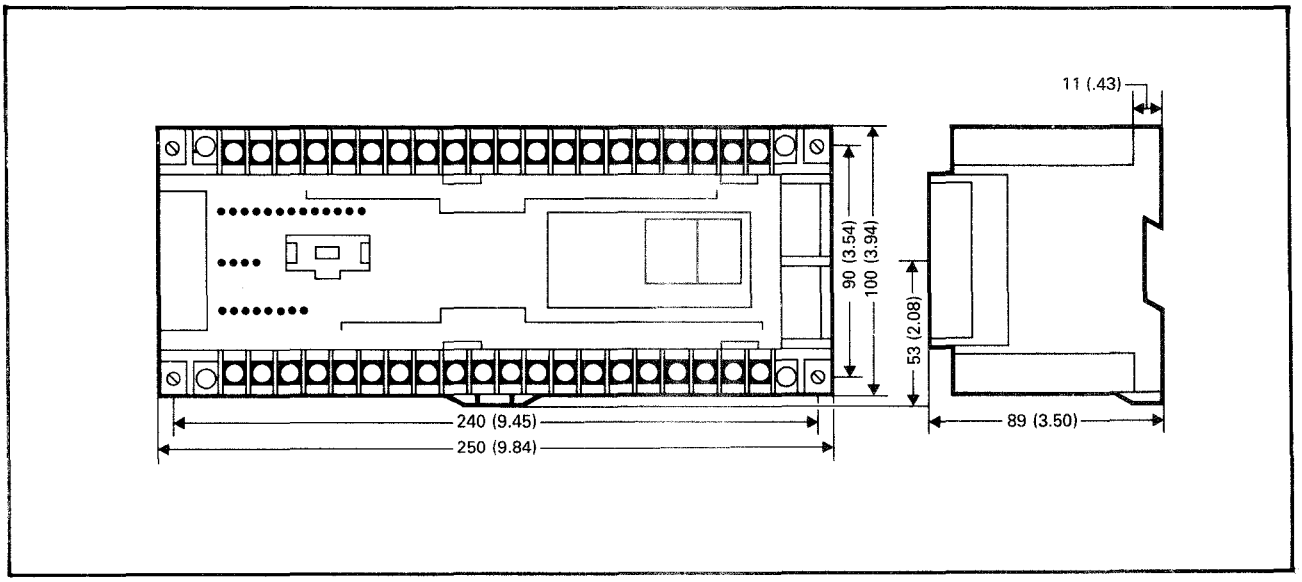


Figure 2-1. External Dimensions for PC-100 in mm (in.)

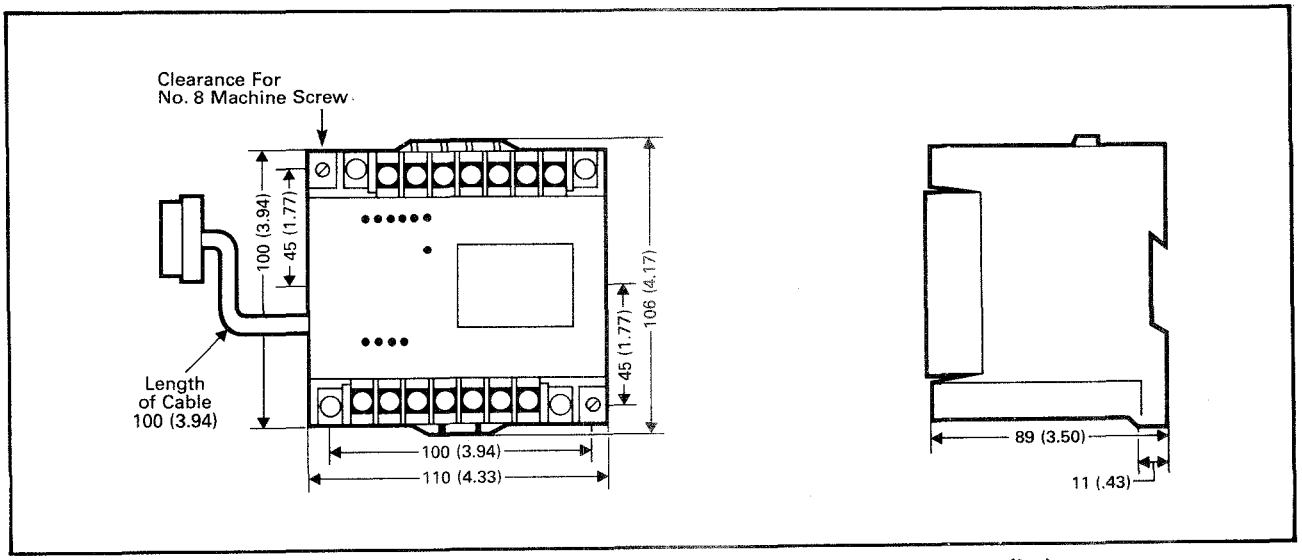


Figure 2-2. External Dimensions for PCE-101 I/O Expander in mm (in.)

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TABLE 2-5. PC-100 AND PCE-101 I/O GENERAL SPECIFICATIONS

Isolation	Rating
Optical Device	2500 VAC for 1 minute
Relay	1500 VAC for 1 minute
I/O Circuit	1500 VAC for 1 minute

TABLE 2-6. PC-100/PCE-101 INPUT CIRCUIT RATINGS

24 VDC Input			
Parameter	**Min.**	**Max.**	**Units**
Off State Voltage	0	5	V
Off State Current	0	2	mA
On State Voltage①	19	27	V
On State Current	5	—	mA
Propagation Delay②	—	4	ms

①The maximum voltage indicated is supplied by the built-in power supply.

②Delay due to filter circuit

TABLE 2-7. PC-100/PCE-101 RELAY OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
AC Voltage①	5	220	VAC RMS
DC Voltage①	5	30	VDC
Output Current	0.003	2	A
Output Current per 8 outputs	—	5	A
Leakage Current②			
at 120 VAC 60 Hz	—	0.55	mA
at 220 VAC 50 Hz	—	0.9	mA
Electrical Life②	3,000,000	—	Electrical cycles
Inrush Current	—	20	A/cycle
Propagation Delay On③	—	15	ms
Propagation Delay Off③	—	5	ms

①Minimum voltage indicated is needed for contact reliability

②Electrical life when relay contact is subjected to energizing and de-energizing 14 VA contactor coil

③The time from the instant when logic signal turns on (off) to the instant when the relay contact closes (opens)

TABLE 2-8. PC-100/PCE-101 DC SOURCE OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
Output Voltage	19	60	VDC
Output Current①	—	−1.5	A
Output Current per 8 Outputs	—	3	A
Leakage Current	—	0.1	mA
Voltage Drop	—	1.5	V
Propagation Delay	—	0.1	ms

①Negative current indicates current leaving the PC

Requirements for External Power Supply

	Min.	Max.	Units
Voltage	19	60	V
Current②	0.3	—	A

②Total current to turn on the transistor; load current not included

TABLE 2-9. PC-100/PCE-101 TRIAC OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
Output Voltage	80	220	VAC RMS
Output Current	0.01	1.5	A
Output Current per 8 Outputs	—	3	A
Inrush Current	—	50	A/cycle
Leakage Current			
at 120 VAC 60 Hz	—	0.55	mA
at 220 VAC 50 Hz	—	0.9	mA
Frequency	47	63	Hz
Voltage Drop	—	1.2	V
Propagation Delay①	—	11	ms

①Not zero crossing

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TABLE 2-10. PC-110 SYSTEM SPECIFICATIONS

CPU	Operational/Control Functions	Logical operation: AND, OR, NOT Functional operation: Timer (0.1 to 12.7 sec.) Counter (1 to 127 counts) Shift Register (8 bits) Step Controller (8 steps) I/O control: Read, Write Others: Clear, NOP (No operation)		
	Scan Time	5 ms/0.2 K words, 8 ms/1K words; speeds between these values are proportional to the program length		
Program Memory	Capacity	1024 words		
	Type	CMOS RAM	Capacitor back-up: at 25° C, approx. 1.5 months at 45° C, approx. 2 weeks	
			Lithium battery (optional): approx. three years	
		EPROM (optional)		
Data Memory	Total Capacity	512 points (64 registers: I/O buffer memory, internal data memory, including retentive memory)		
	Retentive Memory	128 points (16 of 64 registers when the battery is installed)		
Number of I/O Points	PC-100	Input: 24 points Output: 16 points	Total I/O points: 112	
	PCE-111 I/O Expander (up to 3 possible)	Input: 16 points Output: 8 points		
I/O Signal Indication		Input: green LEDs; Output: red LEDs		
Self-diagnosis		Processor fault, parity error, watchdog timer, and battery status		
Control Output		Run confirmation contact (RUN), battery abnormal contact (BATT)		
Applicable Program Tools		Program Loader NLPL-180 Loader Adapter NLLA-185 EPROM Writer NLEP-190		
Weight, kg (lb.)		2.80 (6.20)		

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TABLE 2-11. PCE-111 I/O EXPANDER

Number of Input Points	16
Number of Output Points	8
I/O Signal Indication	Input: green LED Output: red LED
Weight, kg (lb.)	0.85 (1.9)
Length of I/O Expander Cable, mm (in.)	NLC-050 I/O Expander Cable: 50 (1.97) (included with PCE-111) NLC-400 I/O Expander Cable: 400 (15.75) (optional)

2

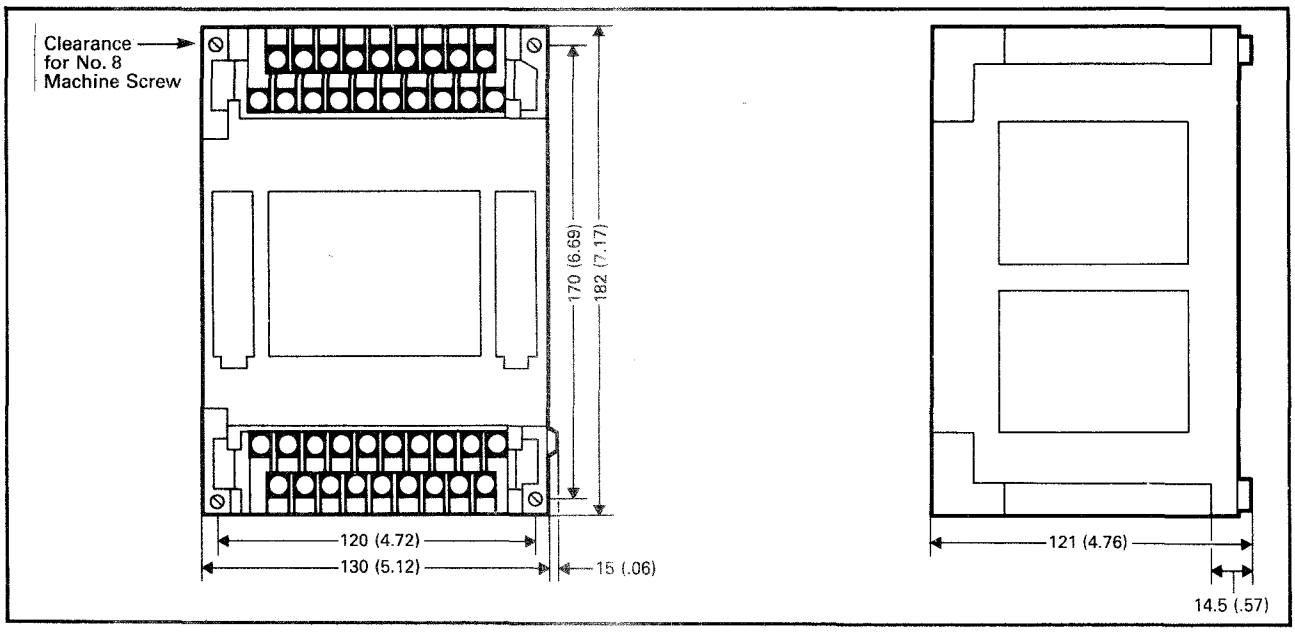


Figure 2-3. External Dimensions for PC-110 in mm (in.)

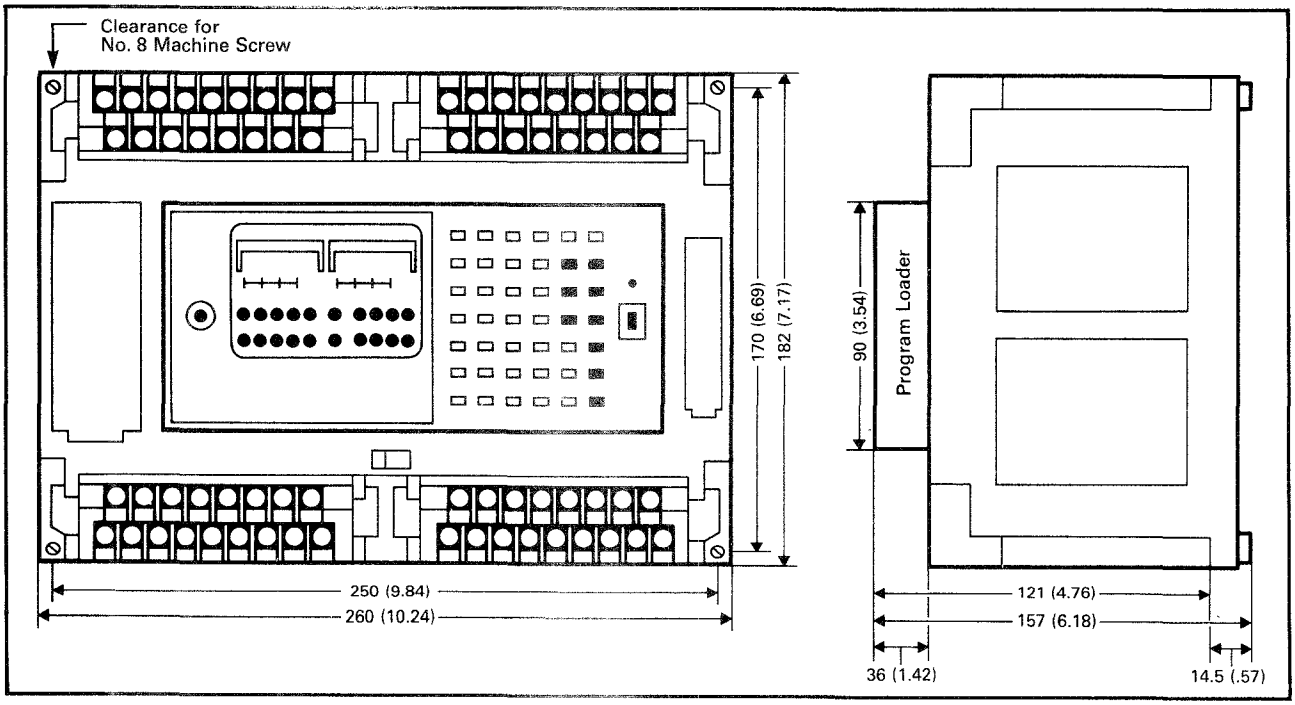


Figure 2-4. External Dimensions for PCE-111 in mm (in.)

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TABLE 2-12. PC-110 AND PCE-111 GENERAL SPECIFICATIONS

Isolation	Rating
Optical Device	2500 VAC for 1 minute
Relay	1500 VAC for 1 minute
I/O Circuit	1500 VAC for 1 minute

TABLE 2-13. PC-110/PCE-111 24 VDC INPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
Off State Voltage	0	5	V
Off State Current	0	2	mA
On State Voltage①	19	27	V
On State Current	7.5	—	mA
Propagation Delay②	—	2	ms

①The maximum voltage indicated is supplied by the built-in power supply

②Delay due to filter circuit

TABLE 2-14. PC-110/PCE-111 RELAY OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
AC Voltage①	5	220	VAC RMS
DC Voltage①	5	30	VDC
Output Current	0.003	2	A
Output Current per 8 Outputs	—	5	A
Leakage Current②			
at 120 VAC 60 Hz	—	0.55	mA
at 220 VAC 50 Hz	—	0.9	mA
Electrical Life②	3,000,000	—	Electrical cycles
Inrush Current	—	20	A/Cycle
Propagation Delay On③	—	15	ms
Propagation Delay Off③	—	5	ms

①Minimum voltage indicated is needed for contact reliability

②Electrical life when relay contact is subjected to energizing and de-energizing 14 VA contactor coil

③The time from the instant when logic signal turns on (off) to the instant when the relay contact closes (opens)

TABLE 2-15. PC-110/PCE-111 DC SOURCE OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
Output Voltage	19	60	VDC
Output Current①	—	−2	A
Output Current per 8 Outputs	—	5	A
Leakage Current	—	0.1	mA
Voltage Drop	—	1.5	V
Propagation Delay	—	0.1	ms

①Negative current indicates current leaving the PC

Requirements for External Power Supply

	Min.	Max.	Units
Voltage	19	60	V
Current②	0.6	—	A

②Total current to turn on the transistor; load current not included

TABLE 2-16. PC-110/PCE-111 TRIAC OUTPUT CIRCUIT RATINGS

Parameter	Min.	Max.	Units
Output Voltage	80	220	VAC RMS
Output Current	0.01	2	A
Output Current per 8 Outputs	—	5	A
Inrush Current	—	50	A/cycle
Leakage Current			
at 120 VAC 60 Hz	—	0.55	mA
at 220 VAC 50 Hz	—	0.9	mA
Frequency	47	63	Hz
Voltage Drop	—	1.2	V
Propagation Delay①	—	11	ms

①Not zero crossing

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Section 3
Address Allocation

3-1. General Description

The PC-100 and PC-110 each contain two areas of memory locations that are available for programming by the user: program memory and data memory (see Tables 3-1 and 3-3).

Program memory is the area which stores the logic instructions that are programmed by the user and that will, in turn, direct the operation of the controller. These instructions, or steps, are stored in successive program memory address locations, with the beginning address (usually Step 0) designated by the user. The PC-100 can store 320 program instructions, beginning at Step 0 and extending to Step 319. The PC-110 can store 1024 program instructions, beginning at Step 0 and extending to Step 1023. See Chapter 4 for detailed information about the instruction set.

Data memory, in both the PC-100 and the PC-110, is an area of 64 registers which store the status of inputs, outputs, internal contacts and coils, and special functions. These 64 data registers, referenced as Registers 0 to 63, can each be further divided into eight bits, referenced as bits 0 to 7. (Refer to Tables 3-2 and 3-4 for detailed analysis of the PC-100 and PC-110 memories.) A complete bit address includes both the address of the register in which the bit is contained and the position of the bit within the register. For example, 5.7 is the address of the last bit (bit 7) in Register 5.

The status of a contact or a coil requires one bit, while the status of a timing register, counting register, Shift Register, or Step Controller function occupies a complete eight-bit register. Bit and register data addresses can be assigned to contacts, coils, and special functions in any manner desired (with the exception of input contacts and output coils, which have dedicated bit addresses, as shown in Tables 3-1, 3-2, 3-3, and 3-4.) The assignment of I/O addresses is detailed in section 3-2.

TABLE 3-1. PC-100 USER MEMORY ORGANIZATION

	Type	Allocation	Address	Remarks
Program Memory	Program instruction	320 steps	Step numbers 0 to 319	Capacitor back-up Additional back-up by lithium battery is optional.
Data Memory	Inputs (PC-100)	12 points	0.0 to 0.7, 1.0 to 1.3 (IN 1 to 12)	Unused I/O addresses can be used as additional internal data addresses.
	Outputs (PC-100)	8 points	2.0 to 2.7 (CR 17 to 24)	
	Inputs (PCE-101 I/O Expander)	6 points	3.0 to 3.5 (IN 25 to 30)	
	Outputs (PCE-101 I/O Expander)	4 points	4.0 to 4.3 (CR 33 to 36)	
	Internal contacts and coils Timers Counters Shift registers Step controllers	43 registers (344 points)	5.0 to 47.7	Volatile—data is lost when power is removed.
		16 registers (128 points)	48.0 to 63.7	Non-volatile—data is retained when power is removed. One point is reserved for battery error output.

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3-2. Memory Organization

The two major areas of memory locations available to the user in the PC-100 are program memory and data memory. A further analysis of the data memory of the PC-100 is shown in Table 3-2.

The table below provides a detailed analysis of the PC-100's data memory area. Note that the area is divided into 64 registers, each containing eight bits.

Input and output circuits have dedicated bit addresses occupying the first five registers. The remaining 59 registers, referenced as Registers 5 to 63, constitute the internal data area. Bit and register addresses from this area can be assigned to internal contacts, coils, and special functions in any manner desired. Note also that the last 16 data memory registers (48 to 63) are non-volatile, that is, their contents are retained during the absence of power (within the limits of the internal capacitor or battery back-up system).

TABLE 3-2. PC-100 DATA MEMORY ORGANIZATION

Register Address	Bit Address 0	1	2	3	4	5	6	7		
0	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	Inputs 0.0 to 0.7, 1.0 to 1.3	PC-100
1	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7		
2	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	Outputs 2.0 to 2.7	
3	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	Inputs 3.0 to 3.5	PCE-101 I/O Expander①
4	4.0	4.1	4.2	4.3	4.4	4.5	4.6	4.7	Outputs 4.0 to 4.3	
5	5.0	5.1	5.2	5.3	5.4	5.5	5.6	5.7	Volatile	Internal Data Area
6	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7		
7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7		
8	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7		
9	9.0	9.1	9.2	9.3	9.4	9.5	9.6	9.7		
10	10.0	10.1	10.2	10.3	10.4	10.5	10.6	10.7		
11	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7		
12	12.0	12.1	12.2	12.3	12.4	12.5	12.6	12.7		
13	13.0	13.1	13.2	13.3	13.4	13.5	13.6	13.7		
14	14.0	14.1	14.2	14.3	14.4	14.5	14.6	14.7		
≈										
47	47.0	47.1	47.2	47.3	47.4	47.5	47.6	47.7		
48	48.0	48.1	48.2	48.3	48.4	48.5	48.6	48.7	Non-volatile②	
≈										
63	63.0	63.1	63.2	63.3	63.4	63.5	63.6	63.7		

① Unused I/O addresses can be used as additional addresses for internal contacts and coils.

② Non-volatile data area should be used for registers and internal contacts and coils whose contents are to be retained during power loss.

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The two major areas of memory locations available to the user in the PC-110 are program memory and data memory. A further analysis of the data memory area of the PC-110 is shown in Table 3-4.

TABLE 3-3. PC-110 USER MEMORY ORGANIZATION

	Type	Allocation	Address	Remarks
Program Memory	Program instruction	1024 steps	Step numbers 0 to 1023	Capacitor back-up Additional back-up by lithium battery is optional.
Data Memory	Inputs (PC-110)	24 points	0.0 to 0.7 (IN 1 to 24)	Unused I/O addresses can be used as additional internal data addresses.
	Outputs (PC-110)	16 points	3.0 to 4.7 (CR 25 to 40)	
	Inputs (PCE-111 I/O Expander 1)	16 points	5.0 to 6.7 (IN 41 to 56)	
	Outputs (PCE-111 I/O Expander 1)	8 points	7.0 to 7.7 (CR 57 to 64)	
	Intputs (PCE-111 I/O Expander 2)	16 points	8.0 to 9.7 (IN 65 to 80)	
	Outputs (PCE-111 I/O Expander 2)	8 points	10.0 to 10.7 (CR 81 to 88)	
	Inputs (PCE-111 I/O Expander 3)	16 points	11.0 to 12.7 (IN 89 to 104)	
	Outputs (PCE-111 I/O Expander 3)	8 points	13.0 to 13.7 (CR 105 to 112)	
	Internal Data including: Internal contacts and coils Timers Counters Shift registers Step controllers	34 registers (272 points)	14.0 to 47.7	Volatile—data is lost when power is removed.
		16 registers (128 points)	48.0 to 63.7	Non-volatile—data is retained when power is removed.

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The table below provides a detailed analysis of the PC-110's data memory area. Note that the area is divided into 64 registers, each containing eight bits. Input and output circuits have dedicated bit addresses occupying the first 14 registers. The remaining 50 registers, referenced as Registers 14 to 63, constitute the internal data area. Bit and register addresses from this area can be assigned to internal contacts, coils, and special functions in any manner desired. Note also that the last 16 data memory registers (48 to 63) are non-volatile, that is, their contents are retained even during the absence of power (within the limits of the internal capacitor or battery back-up system).

TABLE 3-4. PC-110 DATA MEMORY ORGANIZATION

Register Address	Bit Address 0	1	2	3	4	5	6	7		
0	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	Inputs 0.0 to 2.7	PC-110
1	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7		
2	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7		
3	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	Outputs 3.0 to 4.7	
4	4.0	4.1	4.2	4.3	4.4	4.5	4.6	4.7		
5	5.0	5.1	5.2	5.3	5.4	5.5	5.6	5.7	Inputs 5.0 to 6.7	PCE-111 I/O Expanders①
6	6.0	6.1	6.2	6.3	6.4	6.5	6.6	6.7		
7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	Outputs 7.0 to 7.7	
8	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	Inputs 8.0 to 9.7	
9	9.0	9.1	9.2	9.3	9.4	9.5	9.6	9.7		
10	10.0	10.1	10.2	10.3	10.4	10.5	10.6	10.7	Outputs 10.0 to 10.7	
11	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7	Inputs 11.0 to 12.7	
12	12.0	12.1	12.2	12.3	12.4	12.5	12.6	12.7		
13	13.0	13.1	13.2	13.3	13.4	13.5	13.6	13.7	Outputs 13.0 to 13.7	
14	14.0	14.1	14.2	14.3	14.4	14.5	14.6	14.7	Volatile	Internal Data Area
≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈
47	47.0	47.1	47.2	47.3	47.4	47.5	47.6	47.7		
48	48.0	48.1	48.2	48.3	48.4	48.5	48.6	48.7	Non-volatile②	
≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈
63	63.0	63.1	63.2	63.3	63.4	63.5	63.6	63.7		

① Unused I/O addresses can be used as additional addresses for internal contacts and coils.

② Non-volatile data area should be used for registers and internal contacts and coils whose contents are to be retained during power loss.

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3-3. Assignment of I/O Addresses

The I/O addresses of the PC-100 and the PCE-101 I/O Expander are fixed (see Figure 3-1 below). They are also listed in the preceding section and are indicated on the actual units.

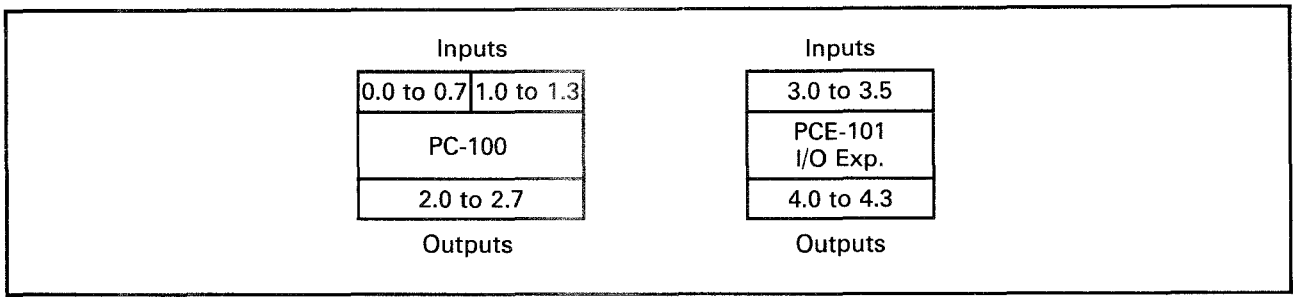


Figure 3-1. PC-100 I/O Address Assignments

3

The I/O addresses of the PC-110 are fixed and are listed in the preceding section and on the actual units. However, because up to three identical PCE-111 I/O Expanders can be connected to a single PC-110, the I/O address assignment of each I/O Expander is determined by its position in the chain (as shown below in Figure 3-2).

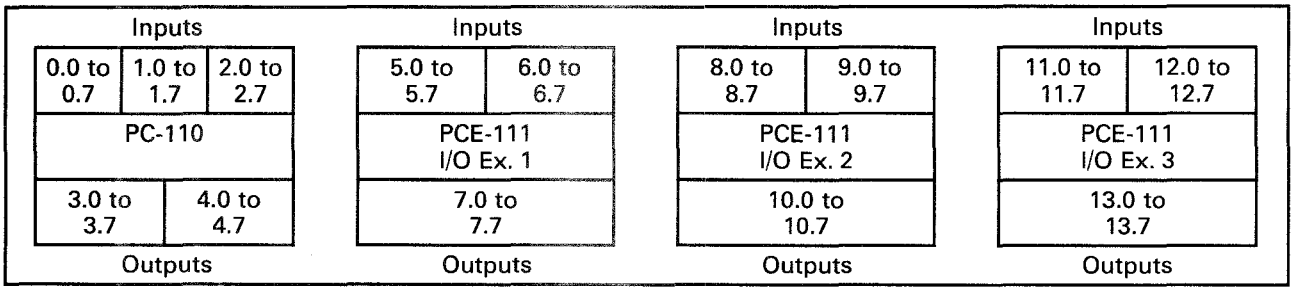


Figure 3-2. PC-110 I/O Address Assignments

NOTE: Follow these precautions upon connecting I/O Expanders.

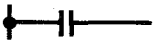
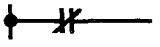
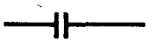
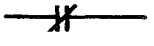
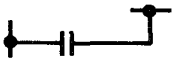
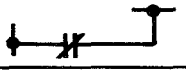
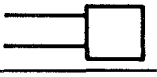
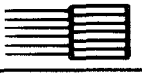
(1) Remove power before connecting and disconnecting I/O Expanders. Connection or disconnection of I/O Expanders during Power ON causes an error, and the operation of PC stops.

(2) Connect I/O Expander cables firmly and securely. If a cable becomes loose while the power is ON, an error will occur and the PC will stop.

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Section 4
Instruction Set

TABLE 4-1. LIST OF INSTRUCTION WORDS

Instruction Word	Ladder Figure Symbol	Reference	Comments
RD		Input contact, internal contact	• Start of logic • Intermediate memory of computation result
RD NOT		Input contact, internal contact	• Start of logic • Intermediate memory of computation result
AND		Input contact, internal contact	• Logical product
AND NOT		Input contact, internal contact	• Logical product
OR		Input contact, internal contact	• Logical sum
OR NOT		Input contact, internal contact	• Logical sum
AND MEM			• Logical product of computation result of up to previous instruction and the contents of intermediate memory①
OR MEM			• Logical sum of computation result of up to previous instruction and the contents of intermediate memory①
WR		Output coil, internal coil	• Coil
WR TMR		Timer	• Timer operation
WR CTR		Counter	• Counter operation
DS			• Preset value of Timer or Counter
WR SR		Shift Register	• Shift register operation
WR SC		Step Controller	• Step controller operation
CLR			• Clearing of data in registers
WR MCR			• Master Control Relay
WR NOT MCR			• Release of Master Control Relay

①Intermediate storage stack (MEM) is for one step.

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4-1. Temporary Storage Registers

The PC-100 and PC-110 require register locations to temporarily store the result of a program operation. The following three types of temporary storage registers are provided.

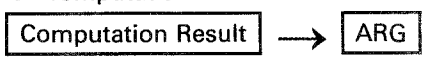
ARG (Arithmetic Register)

The ARG is an internal register not directly accessible from the program loader. It performs the following functions:

- After a RD or RD NOT instruction, the status (ON or OFF) of the contact referenced by the RD or RD NOT instruction is stored in ARG.



- After an AND, AND NOT, OR, or OR NOT instruction, the specified computation result is stored in ARG.



MEM (Memory Register)

The MEM is a register used to store the results of a previous step. Its contents can be accessed by the user. It performs the following functions.

- After a RD or RD NOT instruction, the contents of ARG are first transferred to MEM, and the status of the contact referenced by the RD or RD NOT instruction is then stored in ARG.





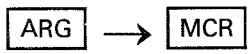
- After an AND MEM or OR MEM instruction, the computation result of the contents of ARG and MEM is stored in ARG.



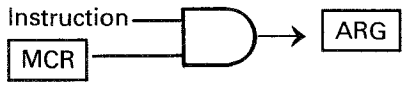
MCR (Master Control Relay Register)

The MCR register, when in the OFF state, disables a specified number of subsequent program steps.

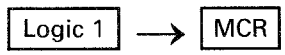
- The WR MCR instruction causes the contents of ARG to be stored in MCR.



- In executing a program, each instruction is ANDed with the contents of MCR, and the computation result is stored in ARG.



- The WR NOT MCR instruction causes a logic 1 to be stored in MCR, allowing return to normal operation.



The following section, "Description of Instructions," includes examples that illustrate the use of the ARG, MEM, and MCR registers.

4-2. Description of Instructions

This section describes the functional operation of each of the instruction words available on the PC-100 and PC-110. Procedures for key entry of these instructions are found in Section 5-7.

NOTE: The programming examples used throughout this manual use reference numbers from the I/O addresses assigned to the PC-100 (inputs 0.0 to 0.7 and 1.0 to 1.3; outputs 2.0 to 2.7). This allows the reader to observe the operation of the programmed examples from the eight LED output indicators (labeled 2.0 to 2.7) located on the lower left of the PC-100.

If attempting to program and observe the operation of these examples using a PC-110 instead, output addresses from the PC-110 (3.0 to 3.7 and 4.0 to 4.7) should be substituted for the PC-100 output addresses used in the examples so that LED's 3.0 to 3.7 and 4.0 to 4.7 will be active.

RD and WR
(Read and Write)

The RD instruction indicates a normally open contact at the start of a line of ladder logic.

The WR instruction indicates an output coil or an internal coil.

Sequence



Coding

Step	Instruction	
0	RD	0.0
1	WR	2.0

Contents of Storage Registers

ARG	MEM
0.0	–
0.0	–

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• Movement of Storage Register Contents

RD stores the status of a specified contact (ON or OFF signal) in ARG and transfers the previous contents of ARG to MEM.

0.0 → ARG → MEM

WR transfers the contents of ARG to a specified coil.

ARG → 2.0

RD NOT and WR
(Read Not and Write)

The RD NOT instruction indicates a normally closed contact at the start of a line of ladder logic.

Sequence



Coding

Step	Instruction	
0	RD NOT	0.0
1	WR	2.0

Contents of Storage Registers

ARG	MEM
0.0	–
0.0	–

• Movement of Storage Register Contents

RD NOT inverts the status of a specified contact and stores it in ARG, and transfers the previous contents of ARG to MEM.

0.1 (inversion) → ARG → MEM

AND

The AND instruction connects a normally open contact in series with the previous logic instruction(s).

Sequence



Coding

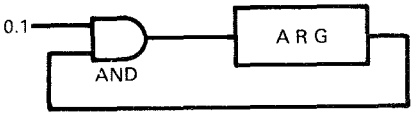
Step	Instruction	
0	RD	0.0
1	AND	0.1
2	WR	2.0

Contents of Storage Registers

ARG	MEM
0.0	–
0.0 0.1	–
0.0 0.1	–

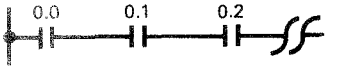
• Movement of Storage Register Contents

AND ANDs the status of a specified contact with the contents of ARG and stores the result in ARG.



• Number of Contacts

The number of program steps available in the processor's memory is the only limitation on the number of contacts that can be connected in series by means of the AND instruction.



Instruction	
RD	0.0
AND	0.1
AND	0.2
⋮	

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AND NOT

The AND NOT instruction connects a normally closed contact in series with the previous logic instruction(s).

Sequence



Coding

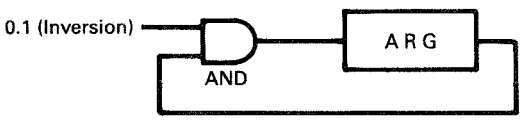
Step	Instruction	
0	RD	0.0
1	AND NOT	0.1
2	WR	2.0

Contents of Storage Registers

ARG	MEM
0.0	–
0.0 0.1	–
0.0 0.1	–

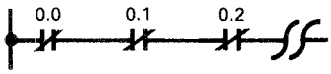
• Movement of Storage Register Contents

AND NOT — Inverts the status of specified contact, ANDs it with the contents of ARG, and stores the result in ARG.



• Number of Contacts

The number of program steps available in the processor's memory is the only limitation on the number of contacts that can be connected in series by means of the AND NOT instruction.



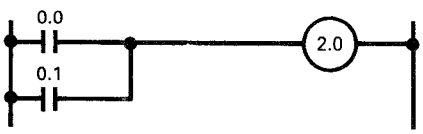
Instruction	
RD	0.0
AND NOT	0.1
AND NOT	0.2
⋮	

4

OR

The OR instruction connects a normally open contact in parallel with the previous logic instruction(s).

Sequence



Coding

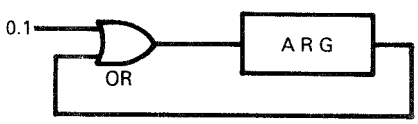
Step	Instruction	
0	RD	0.0
1	OR	0.1
2	WR	2.0

Contents of Storage Registers

ARG	MEM
0.0	–
0.0 0.1	–
0.0 0.1	–

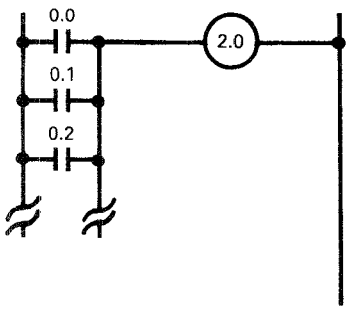
• Movement of Storage Register Contents

OR — ORs the status of a specified contact with the contents of ARG and stores the result in ARG.



• Number of Contacts

The number of program steps available in the processor's memory is the only limitation on the number of contacts that can be arranged in parallel by means of the OR instruction.



Instruction	
RD	0.0
OR	0.1
OR	0.2
⋮	
WR	2.0

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OR NOT

The OR NOT instruction connects a normally closed contact in parallel with the previous logic instruction(s).

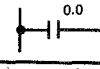
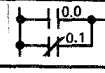
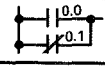
Sequence



Coding

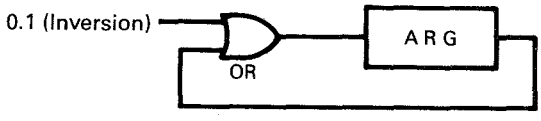
Step	Instruction	
0	RD	0.0
1	OR NOT	0.1
2	WR	2.0

Contents of Storage Registers

ARG	MEM
	–
	–
	–

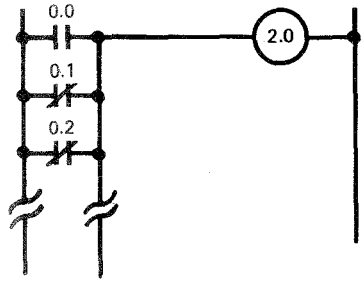
- Movement of Storage Register Contents

OR NOT — Inverts the status of a specified contact, ORs it with the contents of ARG, and stores the result in ARG.



- Number of Contacts

The number of program steps available in the processor's memory is the only limitation on the number of contacts that can be arranged in parallel by means of the OR NOT instruction.



Instruction	
RD	0.0
OR NOT	0.1
OR NOT	0.2
⋮	
WR	2.0

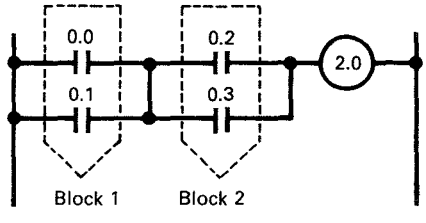
4

AND MEM

The AND MEM instruction connects two blocks of parallel contacts in series.

NOTE: Each block must begin with an RD instruction.

Sequence

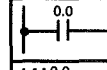
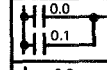
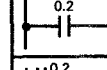
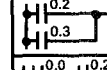
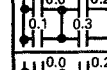
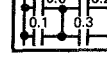


RD 0.2 begins Block 2.
AND MEM connects Block 1 and Block 2 in series.

Coding

Step	Instruction	
0	RD	0.0
1	OR	0.1
2	RD	0.2
3	OR	0.3
4	AND MEM	
5	WR	2.0

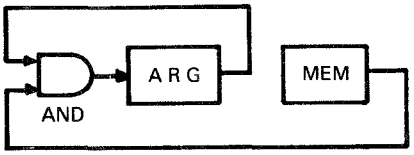
Contents of Storage Registers

ARG	MEM
	
	
	
	
	
	

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• Movement of Storage Register Contents

AND MEM — ANDs the contents of ARG with those of MEM, and stores the result in ARG.



(1) The computation result of Block 1 (RD 0.0 and OR 0.1 instructions) is stored in ARG.

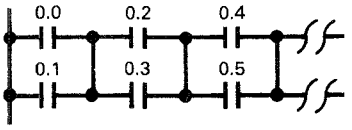
(2) RD 0.2 of Block 2 causes the computation result of Block 1 to be transferred to MEM. The computation result of Block 2 (RD 0.2 and OR 0.3 instructions) is stored in ARG.

(3) When the AND MEM instruction is executed, the computation result of the series connection of MEM (Block 1) and ARG (Block 2) is stored in ARG.

• Number of Blocks

The number of program steps available in the processor's memory is the only limitation on the number of blocks that can be connected by the AND MEM instruction.

The RD, OR, AND MEM sequence of instructions can be used continually as many times as needed.



Instruction	
RD	0.0
OR	0.1
RD	0.2
OR	0.3
AND MEM	
RD	0.4
OR	0.5
AND MEM	
⋮	

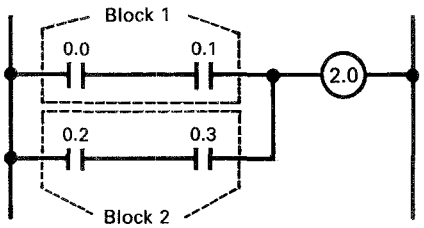
4

OR MEM

The OR MEM instruction connects two blocks of series contacts in parallel.

NOTE: Each block must begin with an RD instruction.

Sequence



RD 0.2 begins Block 2.

OR MEM connects Block 1 and Block 2 in parallel.

Coding

Step	Instruction	
0	RD	0.0
1	AND	0.1
2	RD	0.2
3	AND	0.3
4	OR MEM	
5	WR	2.0

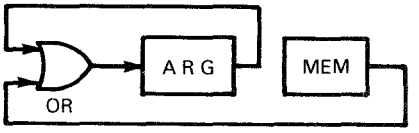
Contents of Storage Registers

ARG	MEM
0.0	
0.0 0.1	
0.2	0.0 0.1
0.2 0.3	0.0 0.1
0.0 0.1 0.2 0.3	
0.0 0.2 0.2 0.3	

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• Movement of Storage Register Contents

OR MEM — ORs the contents of ARG with those of MEM, and stores the result into ARG again.



(1) The computation result of Block 1 (RD 0.0 and AND 0.1 instructions) is stored in ARG.

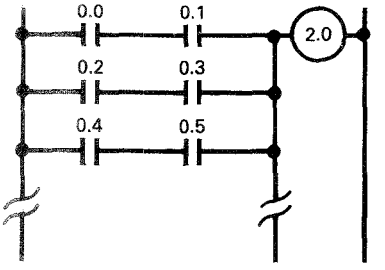
(2) RD 0.2 of Block 2 causes the computation result of Block 1 to be transferred to MEM. The computation result of Block 2 (RD 0.2 and AND 0.3) is stored in ARG.

(3) When the OR MEM instruction is executed, the computation result of the parallel connection of MEM (Block 1) and ARG (Block 2) is stored in ARG.

• Number of blocks

The number of program steps available in the processor memory is the only limitation on the number of blocks that can be connected by the OR MEM instruction.

The RD, AND, OR MEM sequence of instructions can be used continually as many times as needed.



Instruction	
RD	0.0
AND	0.1
RD	0.2
AND	0.3
OR MEM	
RD	0.4
AND	0.5
OR MEM	
⋮	
WR	2.0

4

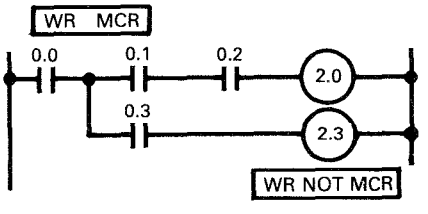
WR MCR and WR NOT MCR

(Master Control Relay)

The MCR instruction allows a prescribed condition to disable a specified number of subsequent program steps. When the contact referenced by MCR is energized (logic 1), the instructions that follow the WR MCR instruction operate normally. However, if the state of the contact referenced by MCR is 0, the instructions that follow and that are between WR MCR and WR NOT MCR will be affected as follows:

- output coils and internal coils turn OFF;
- Timer and Counters are RESET;
- Shift Registers and Step Controllers remain UNCHANGED.

Sequence



In this example, WR MCR/WR NOT MCR is used when the circuit has more than one output branch.

Coding

Step	Instruction	
0	RD	0.0
1	WR MCR	
2	RD	0.1
3	AND	0.2
4	WR	2.0
5	RD	0.3
6	WR	2.3
7	WR NOT MCR	

Contents of Storage Registers

ARG	MEM	MCR
0.0		1 (ON)
0.0		
0.1 O (OFF)	0.0	(ARG) = 1
0.1 0.2 O (OFF)	0.0	
0.1 0.2 O (OFF)	0.0	(ARG)
0.3 O (OFF)	0.1 0.2 O (OFF)	= 0
0.3 O (OFF)	0.1 0.2 O (OFF)	
O (OFF)	O (OFF)	1 (ON)

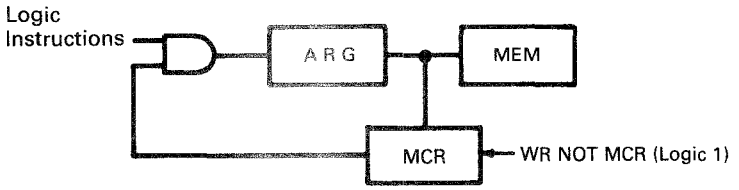
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• Movement of Storage Register Contents

(1) The WR MCR instruction stores the status of ARG in MCR.

(2) Subsequent instructions are ANDed with the contents of MCR. If the status of MCR is at a logic 0 (OFF), the instructions between WR MCR and WR NOT MCR are processed as described above.

(3) The WR NOT MCR instruction sets the status of MCR at a logic 1. After this, the MCR has no effect on the processing of subsequent instructions, that is, the status of contacts, coils, and registers are now determined solely by normal operating conditions.



TMR

(Timer in Tenths of Seconds)

The TMR instruction provides a count-down timer that can energize an output when its current value reaches 0.

The TMR uses two input circuits for operation: an enable circuit and a timing circuit. Both must be energized in order for the timer to begin timing. Anytime the enable circuit is de-energized, the current value is reset to the preset value. If the timing circuit is de-energized while the enable circuit is energized, the current value is held constant. Then, when the timing circuit is re-energized, the timing register resumes its count-down.

Preset: The timer preset is programmed as a constant value using the DS (Data Set) instruction. The preset can be any value between 0 and 127, inclusive. The timer reference pulse is 0.1 sec. Therefore, the range of the timer is 0.0 to 12.7 seconds.

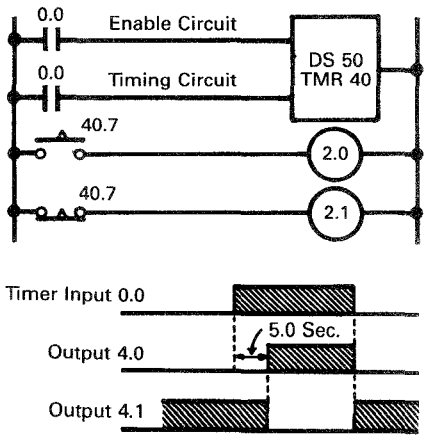
Timing Register: The timing register is programmed using the WR TMR instruction with a valid register address (0 to 63). The current value of the timer resides in the first seven bits (0 to 6) of the timing register. (This is why the range of the timer is 0 to 127 [2^7-1], or 0 to 12.7 seconds.) The eighth bit (bit 7) of the timing register is used to indicate the status of the timer. When the current value reaches 0 (bits 0 to 6 OFF), bit 7 is turned ON.

For example, the address of the status bit of timing register 40 is 40.7. This bit can be used to energize an output coil when the timer times out, as shown in the example below.

Example 1:

Simple TMR Circuit

Sequence



Coding

Step	Instruction		
0	RD	0.0	Enable Circuit
1	RD	0.0	Timing Circuit
2	DS	50	Preset Value
3	WR TMR	40	Timing Register (Contains Current Value)
4	RD	40.7	
5	WR	2.0	
6	RD NOT	40.7	
7	WR	2.1	

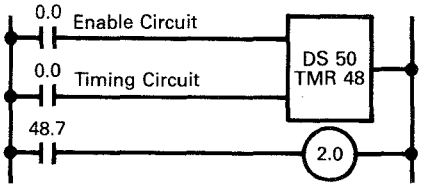
NOTE: The contacts for the enable and timing circuits can be different.

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Example 2:

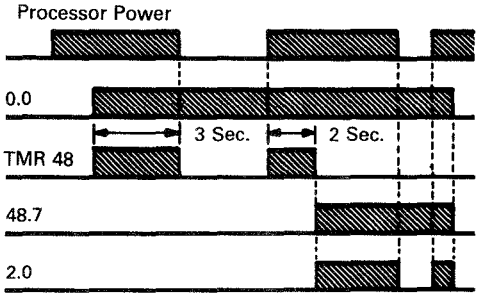
Memory Protection Against Power Failure

The contents of the timing register can be preserved during power loss by choosing a register from the non-volatile memory area (Registers 48 to 63) as the timing register.



Coding

Step	Instruction	
0	RD	0.0
1	RD	0.0
2	DS	50
3	WR TMR	48
4	RD	48.7
5	WR	2.0



CTR
(Counter)

The CTR instruction provides a count-down counter that can energize an output when its current value reaches 0.

The CTR uses two input circuits for operation: an enable circuit and a counting circuit. The enable circuit must be energized in order for the counter to recognize a signal on the counting circuit. Anytime the enable circuit is de-energized, the current value is reset to the preset value. When the enable circuit is energized, the current value in the counting register is decremented by one each time the counting circuit changes from non-conducting to conducting.

Preset: The counter preset is programmed as a constant value using the DS (Data Set) instruction. The preset can be any value between 0 to 127, inclusive.

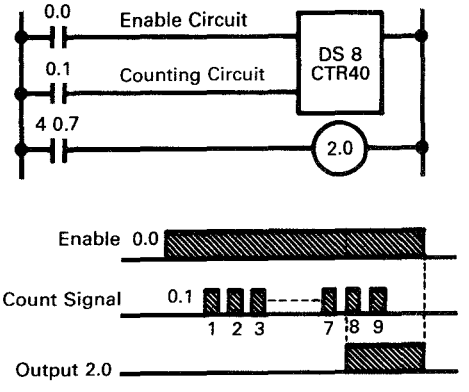
Counting Register: The counting register is programmed using the WR CTR instruction with a valid register address (0 to 63). The current value of the counter resides in the first seven bits (0 to 6) of the counting register. (This is why the range of the counter is 0 to 127 [2^7-1]. The eighth bit (bit 7) of the counting register is used to indicate the status of the counter. When the current value reaches 0 (bits 0 to 6 all OFF), bit 7 is turned ON.

For example, the address of the status bit of counting register 40 is 40.7. This bit can be used to energize an output coil when the counter counts down to 0, as shown in the example below.

Example 1:

Simple CTR Circuit

Sequence



Coding

Step	Instruction		
0	RD	0.0	Enable Circuit
1	RD	0.1	Counting Circuit
2	DS	8	Preset Value
3	WR CTR	40	Counting Register (Contains Current Value)
4	RD	40.7	
5	WR	2.0	

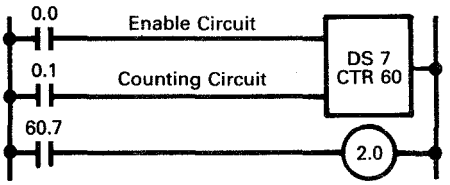
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Example 2:

Memory Protection Against Power Failure

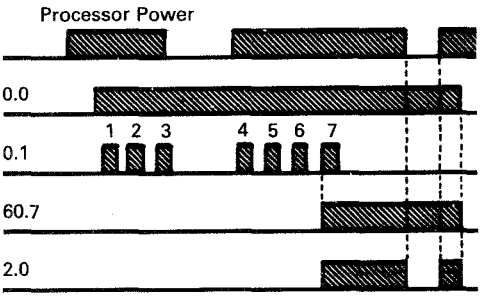
The contents of the counting register can be preserved during power loss by choosing a register from the non-volatile memory area (Registers 48 to 63) as the counting register.

Sequence



Coding

Step	Instruction	
0	RD	0.0
1	RD	0.1
2	DS	7
3	WR CTR	60
4	RD	60.7
5	WR	2.0



SR
(Shift Register)

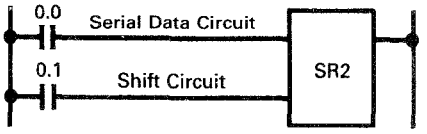
The Shift Register instruction provides a means of serially shifting register data one bit at a time. On command from the program, the status of each bit in the register under SR control is shifted one place to the right.

Two contact circuits control the SR function: the serial data circuit and the shift circuit. Each time the shift circuit changes from non-conducting to conducting, the bits in the register are all shifted one position to the right. The status of the entry position bit (bit 0) is determined by the state of the serial data circuit at the time the SR receives an input to the shift circuit. When the serial data circuit is conducting, a logic 1 is shifted in; when not conducting, a logic 0 is shifted in. When a shift occurs, the data in the last bit (bit 7) is shifted out of the register and lost.

Example 1:

Basic SR Circuit

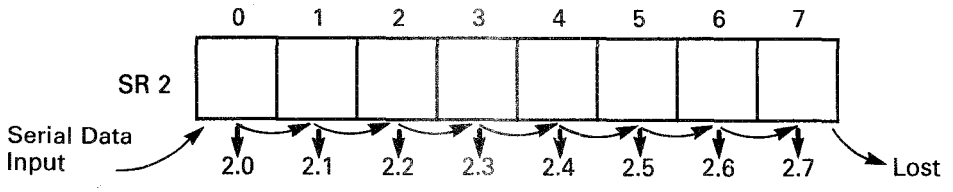
Sequence



Coding

Step	Instruction	
0	RD	0.0
1	RD	0.1
2	WR	SR 2

Shift Register Operation



PARALLEL OUTPUT

Example 2:

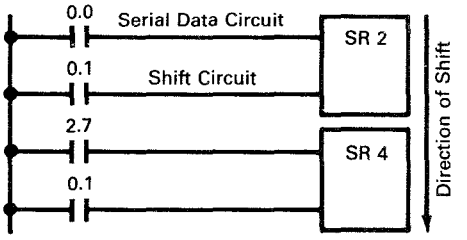
Chaining SRs

Shift registers can be chained to operate synchronously as a single, long register. This is achieved by assigning a common shift circuit to each SR in the chain. The status of bit 7 of the left SR in the chain feeds the serial data circuit of the adjacent SR (second SR in the chain). Likewise, the status of bit 7 of the second SR in the chain

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determines the status of the serial data circuit of the third SR in the chain. Chaining continues in this format until the number of bits in the chain is sufficient to accommodate the application. The status of bit 7 of the right SR (last SR in the chain) is shifted out and lost.

Sequence

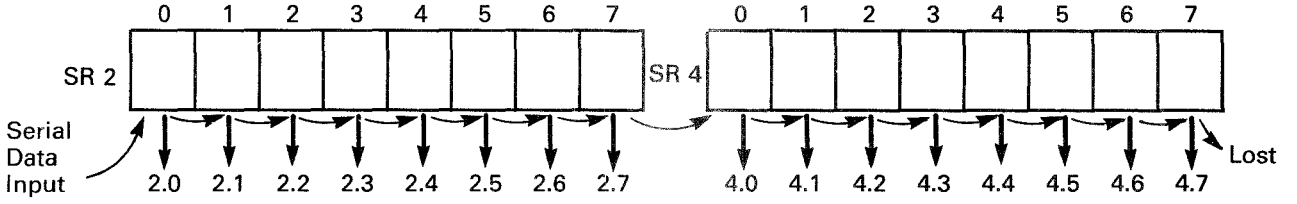


Coding

Step	Instruction	
0	RD	2.7
1	RD	0.1
2	WR SR	4
3	RD	0.0
4	RD	0.1
5	WR SR	2

NOTE: In programming this example, first program SR 4, then SR 2, to insure proper shifting of bit data within the chain.

Chaining Operation



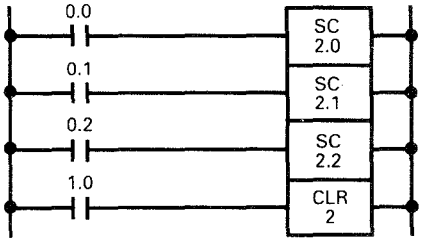
4

SC
(Step Controller)

The Step Controller instruction provides special priority processing of the contents of a register. The Step Controller consists of a block of up to 8 bits of the user-specified SC register.

Typical SC Circuit

Sequence



Coding

Step	Instruction	
0	RD	0.0
1	WR	2.0
2	RD	0.1
3	WR	2.1
4	RD	0.2
5	WR	2.2
6	RD	1.0
7	CLR	2

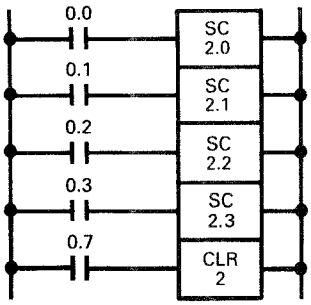
Step Controller Characteristics

- Only one output can be on at any one time.
- Outputs are latched, that is, an output will remain on even after the input which originally initiated it has turned off. The output remains on until the SC recognizes a new output instruction or a CLR (clear) instruction.
- The circuit is a LIFO (Last In, First Out) type. If two or more inputs are present at the same time, priority is given to the output occurring later in the SC block.
- The CLR instruction clears the contents of the specified SC register.

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SC Operation

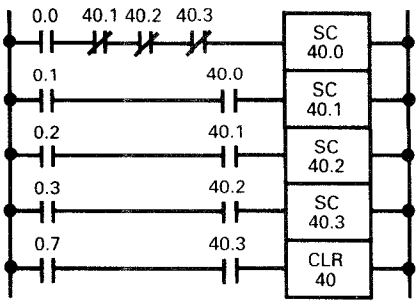
The table below outlines the operation of the simple SC circuit illustrated, and the relationship between its inputs and outputs.



	Input					Output	Remarks
	0.0	0.1	0.2	0.3	0.7		
No Input	---	---	---	---	---	none	
Single Input	●	---	---	---	---	2.0	Latching
	---	---	---	---	---	2.0	Latching
	---	●	---	---	---	2.1	Last output in the SC block has priority
	---	---	●	---	---	2.2	Last output in the SC block has priority
	---	●	---	---	---	2.1	Last output in the SC block has priority
More Than One Input	---	●	●	---	---	2.2	Last output in the SC block has priority
	---	---	●	●	---	2.3	Last output in the SC block has priority
	●	---	●	●	---	2.3	Last output in the SC block has priority
	●	---	●	---	---	2.2	Last output in the SC block has priority
Clear	●	---	---	---	---	2.0	CLR has overall priority
	●	---	---	---	●	none	CLR has overall priority
	---	---	---	---	●	none	CLR has overall priority
	---	---	---	---	---	none	CLR has overall priority

Sequential Operation Circuit

Sequence



Coding

Step	Instruction	
0	RD	0.0
1	AND NOT	40.1
2	AND NOT	40.2
3	AND NOT	40.3
4	WR SC	40.0
5	RD	0.1
6	AND	40.0
7	WR SC	40.1
8	RD	0.2

Coding

Step	Instruction	
9	AND	40.1
10	WR SC	40.2
11	RD	0.3
12	AND	40.2
13	WR SC	40.3
14	RD	0.7
15	AND	40.3
16	CLR	40

This circuit limits the output to a pre-defined sequence. In this example, the outputs are energized in ascending numerical order; that is, in order for an output to energize, the output immediately preceding it must first be on. This circuit is useful in situations where interlocking or safety requirements must first be met in a prescribed sequence in order for final operation to take place.

NOTE: In this example, the SC instruction is operating on an internal register (40), rather than on an output register (2), as shown in previous examples. This is meant to illustrate that the special functions (TMR, CTR, SR, and SC) can operate on any of the 64 data registers and are not restricted only to output registers.

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Section 5

Procedures for Operation

5-1. Program Loader

The NLPL-180 Program Loader programs and monitors both the PC-100 and the PC-110. When used with the PC-100, the loader must first be snapped to the NLLA-185 Loader Adapter. The NLLA-185 acts as an interface to the PC-100 and is connected via the NLC-185 Loader Adapter Cable. When used with the PC-110, the NLPL-180 can be snapped directly to the front panel of the processor or can be connected via the NLLA-185 Loader Adapter and the NLC-186 Loader Adapter Cable for hand-held operation.

The display includes step number, register number, control display, instruction indication, monitor display and other functions.

The program loader has an interface to a cassette tape recorder to provide a means of program storage and retrieval.

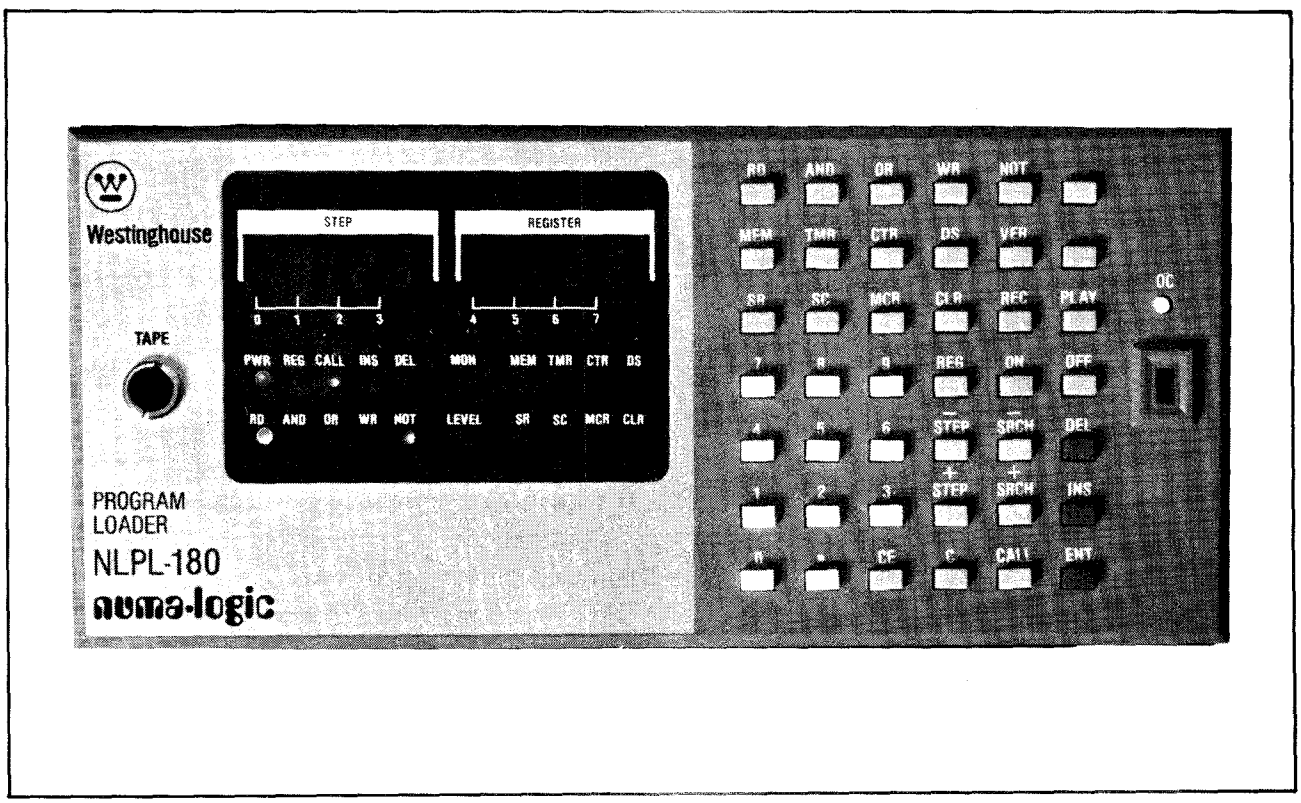


Figure 5-1. NLPL-180 Program Loader

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TABLE 5-1. KEY FUNCTIONS

Classification	Description	Function
Control Keys	C	Clears display, clears memory (when used with INS key)
	CE	Clears number
	CALL	Retrieves and displays program step, register address, and bit address
	ENT	Enters preceding keystrokes into memory
	+ STEP	Increments program step, register address, and bit address by one
	– STEP	Decrements program step, register address, and bit address by one
	+ SRCH	Searches for specific instructions or bit addresses in the direction of ascending program steps
	– SRCH	Searches for specific instructions or bit addresses in the direction of descending program steps
	INS	Clears memory, inserts program instruction
	DEL	Deletes program instruction
	REG	Denotes register and bit data
	ON, OFF	Forces coils ON/OFF (when used with OC switch)
	REC, PLAY, VER	Records, loads, and verifies program
Code Keys	RD, AND, OR, WR, NOT, MEM, TMR, CTR, DS, MCR, CLR	Program instruction words
Numeric Keys	0 to 9	Select program step, register address, bit address, and timer and counter values
Octal Point	•	Distinguishes register and bit addresses from each other

Figure 5-2. Program Loader Keys

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TABLE 5-2. KEY ENTRY PROCEDURES—PROGRAMMING

Operation	Processor Mode Switch	Key Sequence
Clearing Program Memory Area	PRG	(1) C □ (2) INS □ Hold C □ and press INS □ **NOTE: OC switch must be in upper position.**
Clearing Data Memory Area	PRG	(1) C □ (2) INS □ Hold C □ and press INS □ **NOTE: OC switch must be in lower position.**
Calling Program Step	PRG or RUN	(1) C □ (2) Step number (3) CALL □
Incrementing Program Step	PRG or RUN	+ STEP □
Decrementing Program Step	PRG or RUN	− STEP □
Entering Program Instruction	PRG	(1) Code Key (2) Register or bit address (3) ENT □
Inserting Program Instruction (One Step)	PRG	(1) Call program step (2) Code Key (3) Register or bit address (4) INS □
Inserting Program Instructions (n Steps)	PRG	(1) Call program step (2) Delete instruction word (3) Enter the number of instructions to be inserted (4) INS □ **NOTE: n instructions are inserted and the succeeding instructions are incremented by n steps.**
Deleting Program Instruction (One Step)	PRG	(1) Call step to be deleted (2) DEL □
Deleting Program Instruction (n Steps)	PRG	(1) Call program step (2) Delete instruction word (3) Enter the number of instructions to be deleted (4) DEL □ **NOTE: n instructions are deleted and the succeeding instructions are incremented by n steps.**

TABLE 5-3. SEARCHING FOR INSTRUCTIONS

Operation	Processor Mode Switch	Key Sequence
Searching for a Specific Instruction	PRG or RUN	(1) Instruction word (2) + SRCH □ or − SRCH □
Searching for a Specific Register or Bit Address	PRG or RUN	(1) Register or bit address (2) + SRCH □ or − SRCH □

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TABLE 5-4. MONITORING BIT AND REGISTER DATA

Operation	Processor Mode Switch	Key Sequence
Monitoring Bit Data (or Individual I/O Signals)	PRG or RUN	(1) C □ (2) REG □ (3) Bit address (4) CALL □
Monitoring Data Registers (or I/O Signals in Groups of Eight)	PRG or RUN	(1) C □ (2) REG □ (3) Register address (4) CALL □
Monitoring Current Value of TMR and CTR	PRG or RUN	(1) C □ (2) REG □ (3) TMR □ or CTR □ (4) Register address (5) CALL □

TABLE 5-5. FORCING ON/OFF BIT AND REGISTER DATA

Operation	Processor Mode Switch	Key Sequence
Forcing ON or OFF	PRG or RUN	(1) C □ (2) REG □ (3) Register or bit address (4) CALL □ (5) ON □ or OFF □ **NOTE: OC switch must be in upper position**

TABLE 5-6. TAPE FUNCTIONS

Operation	Processor Mode Switch	Key Sequence
Recording Program in Processor Memory onto Cassette Tape	PRG or RUN	(1) C □ (2) REC □ (3) ENT □
Verifying Program Recorded on Cassette Tape	PRG or RUN	(1) C □ (2) VER □ (3) ENT □
Loading Program from Cassette Tape into Processor Memory	PRG	(1) C □ (2) PLAY □ (3) ENT □

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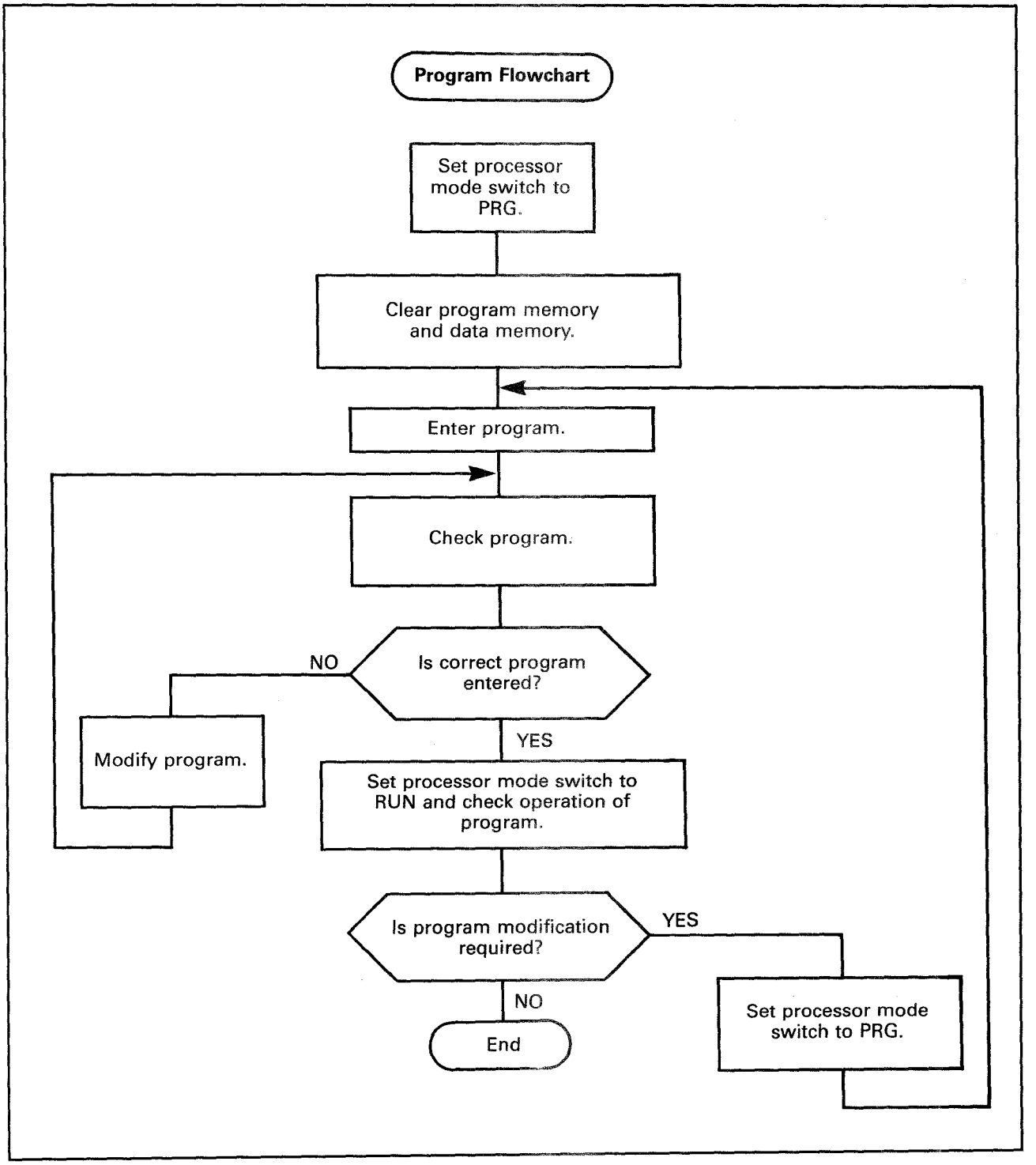


Figure 5-3. Procedures for Entering and Modifying a Program.

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TABLE 5-7. CLEARING PROGRAM MEMORY

Operation Flow	Key Sequence	Results			Remarks
		STEP Display	Instruction Display	REGISTER Display	
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode.
Check OC switch.	OC ○ Lower position				• Must be in lower position.
Press C key and hold.	C □				
Press INS key.	INS □		INS ✱		• Press the INS key while holding the C key.

TABLE 5-8. CLEARING DATA MEMORY

Operation Flow	Key Sequence	Results			Remarks
		STEP Display	Instruction Display	REGISTER Display	
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode.
Check OC switch.	OC ✱ Upper position				• Must be in upper position.
Press C key and hold.	C □				
Press INS key.	INS □		INS ✱		• Press the INS key while holding the C key.

5

5-2. Correcting a Keystroke Error

- Instruction word key
  Press the key of an instruction word whose LED indicator is on to remove the instruction word. Once the incorrect instruction word has been removed, press the key of the correct instruction word.
- Number key
  Press CE key and then enter a correct number.

5-3. Programming Examples

This section illustrates several programming examples and the specific key sequences for entry of the examples. For a description of the functional operation of the instruction words shown in these examples, refer to section 4-3.

To observe the operation of these examples, after programming:

(1) set the processor mode switch to RUN;

(2) energize the appropriate input circuits; and

(3) observe the output LED indicators on the PC.

NOTE: The programming examples used throughout this manual use reference numbers from the I/O addresses assigned to the PC-100 (inputs 0.0 to 0.7 and 1.0 to 1.3; outputs 2.0 to 2.7). This allows the reader to observe the operation of the programmed examples from the eight LED indicators on the lower left of the PC-100.

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TABLE 5-9. PROGRAM ENTRY

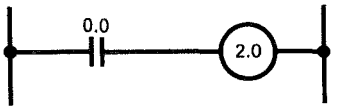
Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG ▨□ RUN				• Must be in PRG mode.
Clear display.	C □				• Calls step 0 **NOTE: In entering a program from step n, call step n, pressing C □ n □ CALL, □ and follow the procedures below.**
Select beginning step number (for example, 0).	0 □	0			
Display selected step.	CALL □	0	CALL ✳	0	
Enter instruction word (for example, RD).	RD □	0	RD ✳	0	• When the key for an instruction word is pressed, the LED indicator corresponding to the instruction word illuminates.
Enter instruction reference number (for example, 0.0).	0 □	0	RD ✳	0	• The register display area indicates the address selected.
	• □	0	RD ✳	0.	
	0 □	0	RD ✳	0.0	• The displayed instruction is written into the program memory.
Enter complete instruction into memory.	ENT □	1		0	• At the same time, the step is incremented by one to allow entry of subsequent instructions.

NOTE: Enter this program from step 0, after clearing the memory.

If attempting to program and observe the operation of these examples using a PC-110 instead, output addresses from the PC-110 (3.0 to 3.7 and 4.0 to 4.7) should be substituted for the PC-100 output addresses used in the examples so that LEDs 3.0 to 3.7 and 4.0 to 4.7 will be active.

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Contact/Coil



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	WR	2.0	WR 2 . 0 ENT

- Operation check
  (1) Set the PRG/RUN selector switch to RUN mode.
  (2) Set switch 0.0 to on.
  (3) Output 2.0 is on when the LED comes on.

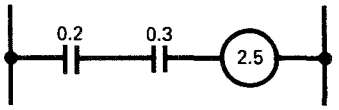
Normally-closed Contact



Step	Instruction		Key Sequence
			C 0 CALL
0	RD NOT	0.1	RD NOT 0 . 1 ENT
1	WR	2.2	WR 2 . 2 ENT

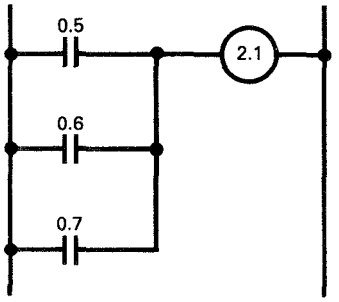
5

Series Contacts



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.2	RD 0 . 2 ENT
1	AND	0.3	AND 0 . 3 ENT
2	WR	2.5	WR 2 . 5 ENT

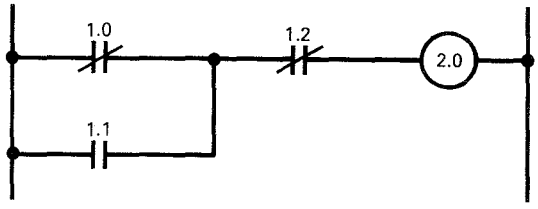
Parallel Contacts



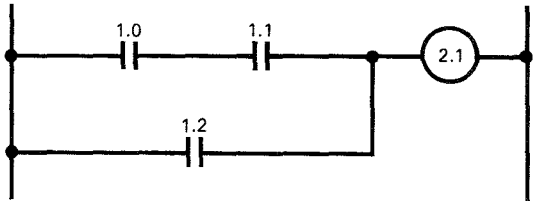
Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.5	RD 0 . 5 ENT
1	OR	0.6	OR 0 . 6 ENT
2	OR	0.7	OR 0 . 7 ENT
3	WR	2.1	WR 2 . 1 ENT

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Series and Parallel

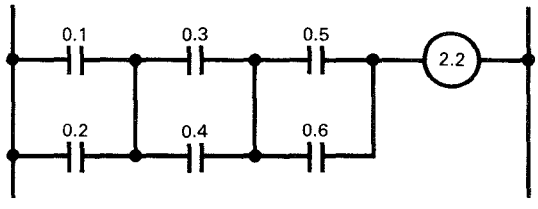


Step	Instruction		Key Sequence
			C 1 0 CALL
10	RD NOT	1.0	RD NOT 1 . 0 ENT
11	OR	1.1	OR 1 . 1 ENT
12	AND NOT	1.2	AND NOT 1 . 2 ENT
13	WR	2.0	WR 2 . 0 ENT



Step	Instruction		Key Sequence
			C 2 7 CALL
27	RD	1.0	RD 1 . 0 ENT
28	AND	1.1	AND 1 . 1 ENT
29	OR	1.2	OR 1 . 2 ENT
30	WR	2.1	WR 2 . 1 ENT

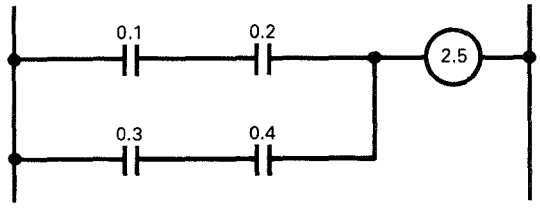
AND MEM



Step	Instruction		Key Sequence
			C 1 0 1 CALL
101	RD	0.1	RD 0 . 1 ENT
102	OR	0.2	OR 0 . 2 ENT
103	RD	0.3	RD 0 . 3 ENT
104	OR	0.4	OR 0 . 4 ENT
105	AND	MEM	AND MEM CE ENT
106	RD	0.5	RD 0 . 5 ENT
107	OR	0.6	OR 0 . 6 ENT
109	AND	MEM	AND MEM CE ENT
110	WR	2.2	WR 2 . 2 ENT

NOTE: Pressing the CE key in steps 105 and 109 clears the REGISTER display.

OR MEM



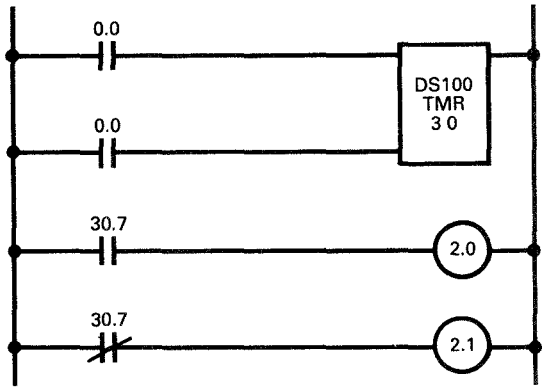
Step	Instruction		Key Sequence
			C 1 7 5 CALL
175	RD	0.1	RD 0 . 1 ENT
176	AND	0.2	AND 0 . 2 ENT
177	RD	0.3	RD 0 . 3 ENT
178	AND	0.4	AND 0 . 4 ENT
179	OR	MEM	OR MEM CE ENT
180	WR	2.5	WR 2 . 5 ENT

NOTE: Pressing the CE key in step 179 clears the REGISTER display.

5

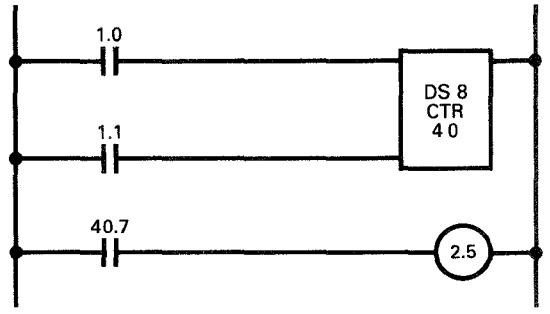
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Timer



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	RD	0.0	RD 0 . 0 ENT
2	DS	100	DS 1 0 0 ENT
3	WR TMR	30	WR TMR 3 0 ENT
4	RD	30.7	RD 3 0 . 7 ENT
5	WR	2.0	WR 2 . 0 ENT
6	RD NOT	30.7	RD NOT 3 0 . 7 ENT
7	WR	2.1	WR 2 . 1 ENT

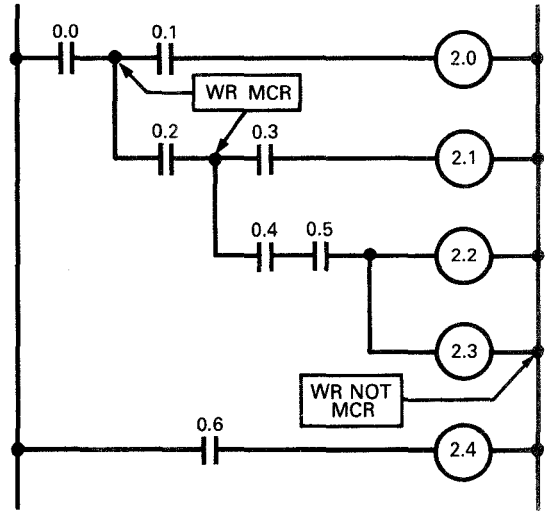
Counter



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	1.0	RD 1 . 0 ENT
1	RD	1.1	RD 1 . 1 ENT
2	DS	8	DS 8 ENT
3	WR CTR	40	WR CTR 4 0 ENT
4	RD	40.7	RD 4 0 . 7 ENT
5	WR	2.5	WR 2 . 5 ENT

NOTE: Enter the WR TMR instruction in the order of DS (setting value) and timing register address.

Master Control Relay (WR MCR/WR NOT MCR)

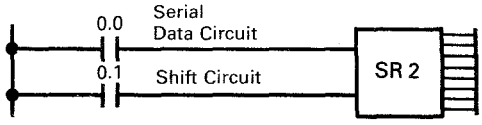


Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	WR	MCR	WR MCR CE ENT
2	RD	0.1	RD 0 . 1 ENT
3	WR	2.0	WR 2 . 0 ENT
4	RD	0.2	RD 0 . 2 ENT
5	WR	MCR	WR MCR CE ENT
6	RD	0.3	RD 0 . 3 ENT
7	WR	2.1	WR 2 . 1 ENT
8	RD	0.4	RD 0 . 4 ENT
9	AND	0.5	AND 0 . 5 ENT
10	WR	2.2	WR 2 . 2 ENT
11	WR	2.3	WR 2 . 3 ENT
12	WR NOT	MCR	WR NOT MCR CE ENT
13	RD	0.6	RD 0 . 6 ENT
14	WR	2.4	WR 2 . 4 ENT

NOTE: Pressing the CE key in steps 1, 5 and 12 clears the REGISTER display.

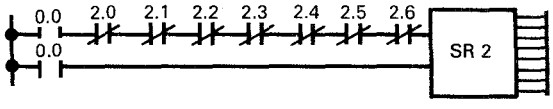
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Shift Register Basic Circuit



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	RD	0.1	RD 0 . 1 ENT
2	WR SR	2	WR SR 2 ENT

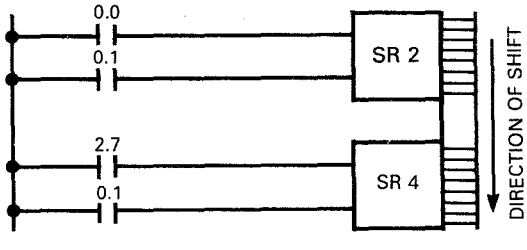
Shift Register Ring Counter



NOTE: Each time IN 0.0 changes from off to on, a logic 1 is shifted one place to the right in register 2. Upon reaching the final bit (2.7) in the register, the next transition from off to on causes the status of bit 2.7 to be shifted into the first bit (2.0) of the register.

Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	AND NOT	2.0	AND NOT 2 . 0 ENT
2	AND NOT	2.1	AND NOT 2 . 1 ENT
3	AND NOT	2.2	AND NOT 2 . 2 ENT
4	AND NOT	2.3	AND NOT 2 . 3 ENT
5	AND NOT	2.4	AND NOT 2 . 4 ENT
6	AND NOT	2.5	AND NOT 2 . 5 ENT
7	AND NOT	2.6	AND NOT 2 . 6 ENT
8	RD	0.0	RD 0 . 0 ENT
9	WR SR	2	WR SR 2 ENT

Shift Register Chaining



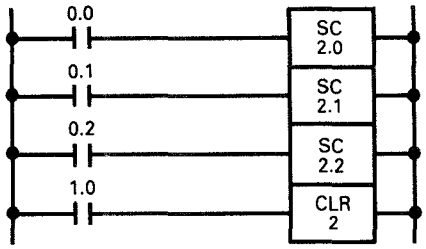
Step	Instruction		Key Sequence
			C 0 CALL
0	RD	2.7	RD 2 . 7 ENT
1	RD	0.1	RD 0 . 1 ENT
2	WR SR	4	WR SR 4 ENT
3	RD	0.0	RD 0 . 0 ENT
4	RD	0.1	RD 0 . 1 ENT
5	WR SR	2	WR SR 2 ENT

NOTE: In programming this example, first program SR 4, then SR 2, to insure proper shifting of bit data within the chain.

5

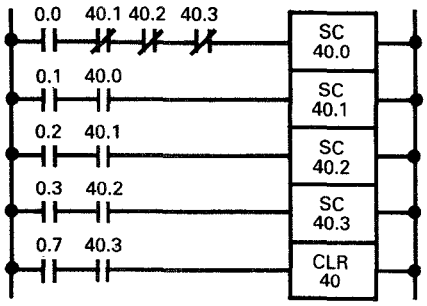
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Step Controller
Basic Circuit (Last In, First Out)



Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	WR SC	2.0	WR SC 2 . 0 ENT
2	RD	0.1	RD 0 . 1 ENT
3	WR SC	2.1	WR SC 2 . 1 ENT
4	RD	0.2	RD 0 . 2 ENT
5	WR SC	2.2	WR SC 2 . 2 ENT
6	RD	1.0	RD 1 . 0 ENT
7	CLR	2	CLR 2 ENT

Step Controller
Basic Circuit for Sequential Operation



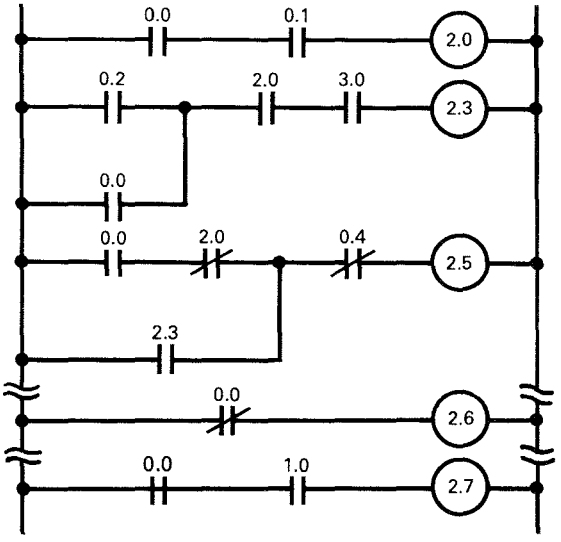
Step	Instruction		Key Sequence
			C 0 CALL
0	RD	0.0	RD 0 . 0 ENT
1	AND NOT	40.1	AND NOT 4 0 . 1 ENT
2	AND NOT	40.2	AND NOT 4 0 . 2 ENT
3	AND NOT	40.3	AND NOT 4 0 . 3 ENT
4	WR SC	40.0	WR SC 4 0 . 0 ENT
5	RD	0.1	RD 0 . 1 ENT
6	AND	40.0	AND 4 0 . 0 ENT
7	WR SC	40.1	WR SC 4 0 . 1 ENT
8	RD	0.2	RD 0 . 2 ENT
9	AND	40.1	AND 4 0 . 1 ENT
10	WR SC	40.2	WR SC 4 0 . 2 ENT
11	RD	0.3	RD 0 . 3 ENT
12	AND	40.2	AND 4 0 . 2 ENT
13	WR SC	40.3	WR SC 4 0 . 3 ENT
14	RD	0.7	RD 0 . 7 ENT
15	AND	40.3	AND 4 0 . 3 ENT
16	CLR	40	CLR 4 0 ENT

NOTE: In this example, the SC instruction is operating on an internal register (40), rather than on an output register (2), as shown in previous examples. To observe the status of the bit addresses within an internal register, refer to Section 6-2.

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5-4. Program Search

This section shows examples of the Search function when the program shown below has been written into memory.



Coding

Step	Instruction	
0	RD	0.0
1	AND	0.1
2	WR	2.0
71	RD	0.2
72	OR	0.0
73	AND	2.0
74	AND	3.0
75	WR	2.3
96	RD	0.0
97	AND NOT	2.0

Coding

Step	Instruction	
98	OR	2.3
99	AND NOT	0.4
100	WR	2.5
⋮		
114	RD NOT	0.0
115	WR	2.6
⋮		
148	RD	0.0
149	AND	1.0
150	WR	2.7

TABLE 5-10. SEARCHING FOR A SPECIFIC INSTRUCTION

The table below shows an example of how the display appears when the steps where RD 0.0 is written are searched.

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Call the step where RD 0.0 is written.	C □				
	0 □	0			
	CALL □	0	RD	0.0	• The instruction word and bit address contained in step 0 are displayed.
Retrieve and display instruction.	+ SRCH □	96	RD	0.0	• The found instruction is displayed.
	+ SRCH □	148	RD	0.0	
	+ SRCH □	nnnn	RD	0.0	• This shows that all instances of RD 0.0 have been found in the direction of the search. ①
	C □	148	RD	0.0	• By means of C key, step 148, which was retrieved earlier, is displayed.

① + SRCH □ Searches in the direction of ascending program steps while − SRCH □ searches in the direction of descending program steps. However, if no designated instruction is found in the direction specified, the STEP display shows nnnn or 0000

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TABLE 5-11. SEARCHING FOR A SPECIFIC REGISTER OR BIT ADDRESS

The table below shows an example of how the display appears when searching for the steps where 0.0 is used as a reference number.

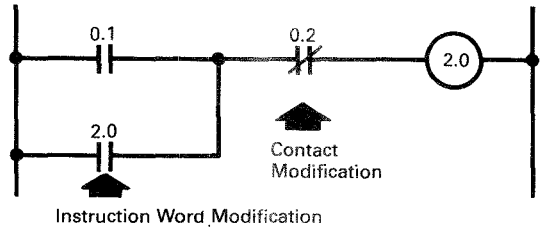
Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
	C □				
Call the step where RD 0.0 is written.	0 □	0			
	CALL □	0	RD ✱	0.0	• The instruction word and bit address contained in step 0 are displayed.
Delete instruction word.	RD □	0		0.0	• When the key for an instruction word displayed is pressed, the word is deleted.
Retrieve and display instruction.	+ SRCH □	72	OR ✱	0.0	• The found bit address and its corresponding instruction word are displayed.
	OR □	72		0.0	• To continue search, delete the displayed instruction word and press + SRCH □
	+ SRCH □	96	RD ✱	0.0	
	RD □	96		0.0	
	+ SRCH □	114	RD NOT ✱✱	0.0	
	RD □	114	NOT ✱	0.0	
	NOT □	114		0.0	
	+ SRCH □	nnnn		0.0	• This shows that all instructions referencing the specified bit address (0.0) have been found in the direction of the search.①
	C □	114	RD NOT ✱✱	0.0	

① + SRCH □ Searches in the direction of ascending program steps while − SRCH □ searches in the direction of descending program steps. However, if no designated instruction is found in the direction specified, the STEP display shows nnnn or uuuu

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5-5. Program Modification

The table below shows the procedure for changing the instruction word from OR to AND in step 1 of the program example.



Coding

Step	Instruction	
0	RD	0.1
1	OR	2.0
2	AND NOT	0.2
3	WR	2.0

TABLE 5-12. MODIFYING AN INSTRUCTION WORD

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG RUN				• Must be in PRG mode.
	C				
	1				
Call instruction to be modified.	CALL	1	OR	2.0	• The instruction to be modified is displayed.
Remove the instruction word to be modified.	OR	1		2.0	• The instruction word to be modified is removed by pressing its key.
Enter the new instruction word.	AND	1	AND	2.0	• The new instruction word is displayed and entered into program memory, causing the subsequent instruction to be displayed.
	ENT	2	AND NOT	0.2	

TABLE 5-13. MODIFYING A CONTACT, COIL, OR REGISTER REFERENCE ADDRESS.

The table below shows the procedure for changing the contact reference address in step 2 of the program example above from 0.2 to 1.2.

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG RUN				• Must be in PRG mode.
	C				
Call instruction to be modified.	2	2			
	CALL	2	AND NOT	0.2	• The instruction to be modified is displayed.
Clear REGISTER display.	CE	2	AND NOT		• The address is deleted.
Enter new address.	1	2	AND NOT	1	• The new address is displayed and entered into program memory, causing the subsequent instruction to be displayed.
	.	2	AND NOT	1.	
	2	2	AND NOT	1.2	
	ENT	3	WR	2.0	

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5-6. Program Insertion

The table below shows the procedure for inserting the normally closed contact 1.4 in series.

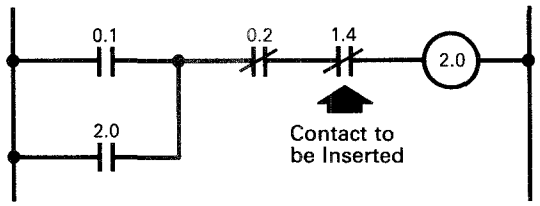


TABLE 5-14. INSERTION OF ONE INSTRUCTION

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG RUN				• Must be in PRG mode.
	C				
Call program step.	3	3			• The step where the instruction is to be inserted is displayed.
	CALL	3	WR	2.0	
Enter instruction to be inserted.	AND	3	AND	2.0	
	NOT	3	AND NOT	2.0	• The instruction to be inserted is displayed and entered into program memory.
	1	3	AND NOT	1	
	.	3	AND NOT	1.	The step addresses of the program instructions that follow the inserted step are all increased by one, and the instruction at the last step address in program memory is lost.
	4	3	AND NOT	1.4	
	INS	3	AND NOT	1.4	
			INS		
Verify insertion.	+ STEP	4	WR	2.0	• This verifies that WR 2.0 is transferred to step 4.

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The table below shows a procedure for inserting eight contacts (1.0 through 1.7) in series.

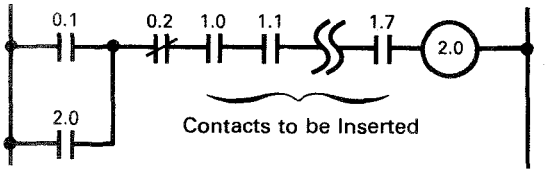


TABLE 5-15. INSERTION OF SUCCESSIVE INSTRUCTIONS (N STEPS).

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode
	C □				
Call program step.	3 □	3			• The step where the first instruction is to be inserted is displayed.
	CALL □	3	WR ✕	2.0	
Delete instruction word.	WR □	3		2.0	• The displayed instruction word is deleted.
Enter the number of instructions to be inserted.	8 □	3		8	• The number of instructions to be inserted is entered and displayed.
	INS □		INS ✕		
Enter additional instructions.	AND □	3	AND ✕	0	
	1 □	3	AND ✕	1	
	. □	3	AND ✕	1.	
	0 □	3	AND ✕	1.0	• The instructions to be inserted are displayed and entered into memory.
	ENT □	4		0	
	⋮				The step addresses of all subsequent instructions are increased by n (8, in this case), where n ranges from 1 to 320 for the PC-100 and from 1 to 1024 for the PC-110.
	AND □	10	AND ✕	0	
	1 □	10	AND ✕	1	
	. □	10	AND ✕	1.	
	7 □	10	AND ✕	1.7	
	ENT □	11	WR ✕	2.0	

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5-7. Program Deletion

The table below shows the procedure for deleting the normally closed contact 0.2.

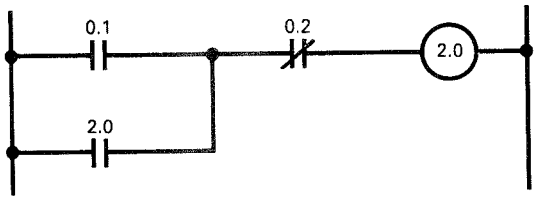


TABLE 5-16. PROGRAM DELETION

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode.
Call the step to be deleted.	C □ 2 □	2			
	CALL □	2	AND NOT	0.2	• The instruction to be deleted is displayed.
Delete instruction.	DEL □	2	WR	2.0	• As a result of deletion, the step addresses of the program instructions that follow the deleted instruction are all decreased by one and the instruction of the step immediately following the deleted instruction step is displayed.

TABLE 5-17. DELETION BY NOP (NO OPERATION)

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode.
Call the step to be replaced by the NOP instruction.	C □ 2 □	2			
	CALL □	2	AND NOT	0.2	• The instruction to be replaced by the NOP instruction is displayed.
Remove instruction word.	AND □	2	NOT	0.2	• The instruction word is removed.
	NOT □	2		0.2	
Remove reference number.	CE □	3			• The address is removed.
Enter NOP instruction.	0 □	2		0	• The NOP instruction is entered and the subsequent instruction is displayed.
	ENT □	3	WR	2.0	

NOTE: Removing an instruction and replacing it with a NOP (no operation) instruction effectively deletes the unwanted instruction, but retains its space (step number) in program memory. This is done by calling the desired step and then separately removing its instruction word and its reference number. The NOP instruction is then entered.

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The table below shows the procedure for deleting eight contacts (1.0 through 1.7).

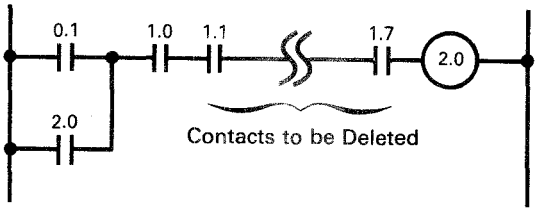


TABLE 5-18. DELETION OF SUCCESSIVE INSTRUCTIONS (N STEPS)

Operation Flow	Key Sequence	Results			Remarks
		STEP Display	Instruction Display	REGISTER Display	
Set mode switch to PRG.	PRG ▨ RUN				• Must be in PRG mode.
Call the first step to be deleted.	C □ 2 □ CALL □	2 2	AND ✕	1.0	• The step containing the first instruction to be deleted is displayed.
Delete instruction word.	AND □	2		1.0	• The displayed instruction word is deleted.
Enter the number of instructions to be deleted.	8 □	2		8	• The number of instructions to be deleted is entered and displayed.
Delete instructions.	DEL □	2	WR ✕	2.0	• The eight instructions contained in steps 2 through 9 are deleted, and the addresses of all subsequent instructions are decreased by 8. Note that n ranges from 1 to 320 for the PC-100 and from 1 to 1024 for the PC-110.

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Section 6

Monitor Function

6-1. Monitoring Inputs, Outputs, Internal Contacts, and Internal Coils

The status of inputs, outputs, internal contacts, and internal coils can be monitored individually (bit data) or simultaneously in groups of eight (register data).

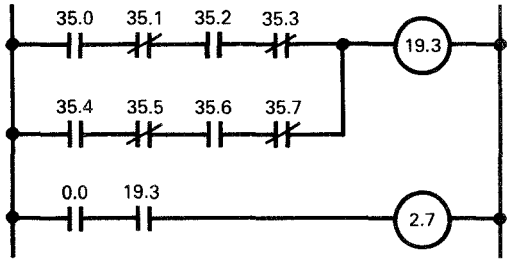
Bit Data—for monitoring the status of contacts or coils individually (see Figure 6-1).

C REG 0 . 0 CALL ☐ ☐ ☐ ☐ ☐ ☐ — (0.0 is on if the MON lamp comes on)

C REG 1 9 . 3 CALL ☐ ☐ ☐ ☐ ☐ ☐ ☐ — (19.3 is energized if the MON lamp comes on)

C REG 3 5 . 5 CALL ☐ ☐ ☐ ☐ ☐ ☐ ☐ — (35.5 is energized if the MON lamp comes on)

Register Data—for monitoring the status of eight contacts or coils simultaneously. In the program example in Figure 6-1, the numbers used to reference the eight contacts in the top rung (35.0 to 35.7) are the eight bit addresses contained in register 35. By calling register 35, rather than the eight bits individually, the status of all eight contacts can be observed simultaneously (see Figure 6-2).



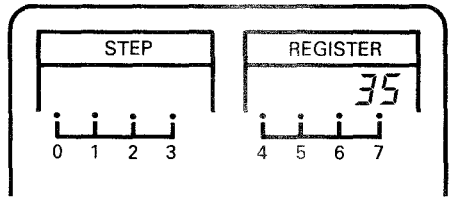
Step	Instruction	
0	RD	35.0
1	AND NOT	35.1
2	AND	35.2
3	AND NOT	35.3
4	RD	35.4
5	AND NOT	35.5

Step	Instruction	
6	AND	35.6
7	AND NOT	35.7
8	OR MEM	
9	WR	19.3
10	RD	0.0
11	AND	19.3
12	WR	2.7

Figure 6-1. Procedures for Monitoring a Program

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C REG 3 5 CALL

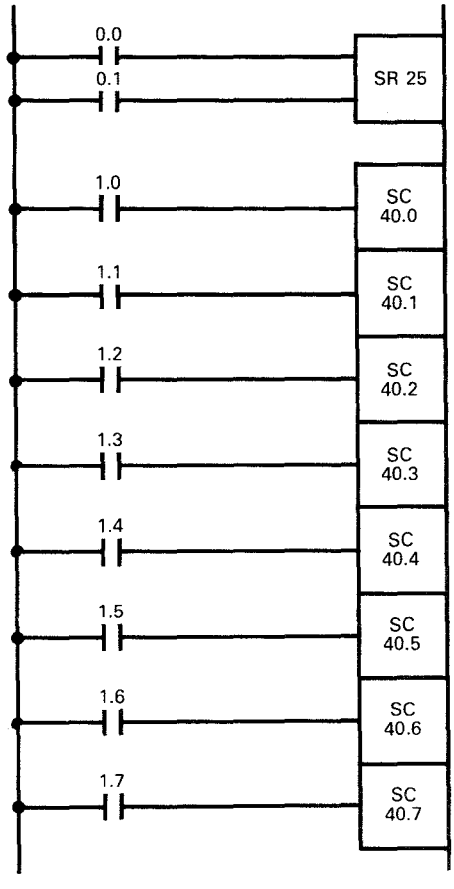


A lit LED indicates that the corresponding contact or coil is energized.

Figure 6-2. Monitoring Register Data

6-2. Monitoring Shift Registers and Step Controllers

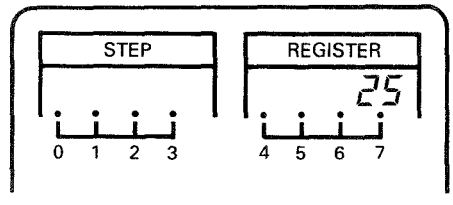
The contents of any register, including registers used in programming the SR (Shift Register) and SC (Step Controller) functions, can be monitored as shown in the program example of Figure 6-3.



To monitor the contents of SR 25:

C REG 2 5 CALL

Display on the loader:



To monitor the contents of SC 40:

C REG 4 0 CALL

Display on the loader:

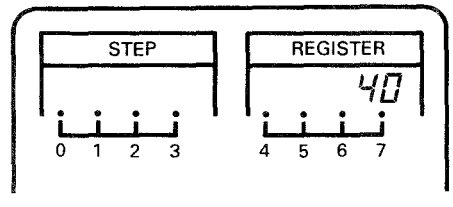


Figure 6-3. Monitoring Shift Registers and Step Controllers.

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6-3. Monitoring the Current Value of the Timer and Counter.

The examples below show how to display the current value of the Timer and Counter, illustrated in Figure 6-4, in decimal and in binary.

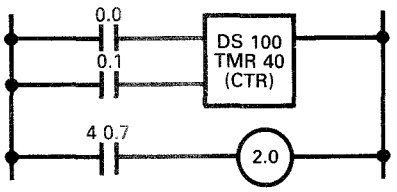
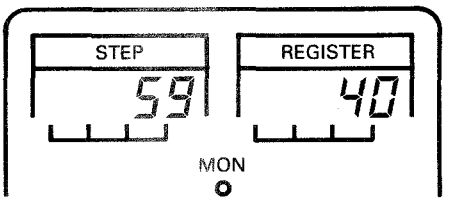


Figure 6-4. Timer (Counter) Circuit

Decimal Display (Numeric)

C TMR (CTR) REG 4 0 CALL

Display on the loader



In this example, register 40, which contains the current value of the timer, has timed down to 5.9 seconds from its preset value of 10.0 seconds.

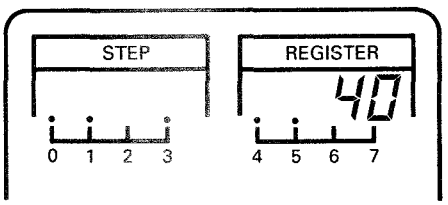
The MON lamp comes on when the register times down to 0.

Figure 6-5. Monitoring in Decimal.

Binary Display (LEDs Indicate Bit Status)

C REG 4 0 CALL

Display on the loader



This example shows that $2^0 + 2^1 + 2^3 + 2^4 + 2^5 = 59$. This means that the timer will time out to 0 in 5.9 seconds.

Figure 6-6. Monitoring in Binary.

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6-4. Forced ON/OFF

Using the Output Controller (OC) switch, it is possible to force (that is, set) output coils, internal coils, and internal contacts (including non-volatile area) ON or OFF from the program loader without any external signal.

Remember the following points when using the Output Controller capability:

(1) Input contacts cannot be forced.

(2) All forces are removed when the position of the PRG/RUN mode switch is changed.

(3) Execution of the user program has priority, in that a force command will not override the status of a contact or coil that has already been determined by logic occurring earlier in the scan of the program.

Follow the procedures in Table 6-1 to force coil 2.0 and its associated contact in the program shown below.

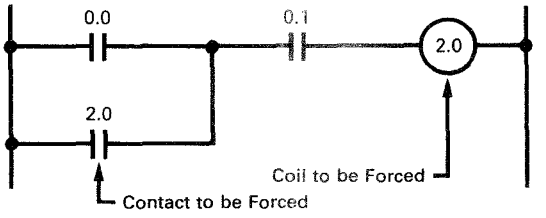


Figure 6-7. Forced ON/OFF.

TABLE 6-1. FORCED ON/OFF

Operation Flow	Key Sequence	Results: STEP Display	Results: Instruction Display	Results: REGISTER Display	Remarks
Set mode switch to RUN.	PRG ▨ RUN				• Must be in RUN mode.
Set OC switch to upper position.	OC ● Upper position				• OC switch must be in upper position.
Call bit added.	C □				
	REG □		REG ●		
	2 □		REG ●	2	
	. □		REG ●	2.	
	0 □		REG ●	2.0	
	CALL □		REG ●	2.0	• The bit address to be forced flashes on the REGISTER display.
Force bit address ON/OFF.	ON □		MON ●	2.0	• The bit address is forced ON.
	OFF □			2.0	• The bit address is forced OFF.

6

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The key entries listed in Table 6-1 cannot be used to force output coil 2.0 above because, in this case, the status of output coil 2.0 is controlled solely by the status of input contact 0.0. Output 2.0 cannot be forced to disagree with input 0.0.

Figure 6-8. Forced ON/OFF Disallowed.

6-5. Manipulation of Timer and Counter

The contents of timing and counting registers can be changed to manipulate the current value and status bit of the timer/counter.

Recall that the timer/counter is a down-count type whose current value is decremented by one every 100 ms (for the timer) or upon an OFF/ON transition of the counting circuit (for the counter). The current value resides in bits 0 to 6 of the register. Under normal operation, when the current value reaches 0 (bits 0 to 6 all OFF), the status bit (bit 7) turns ON.

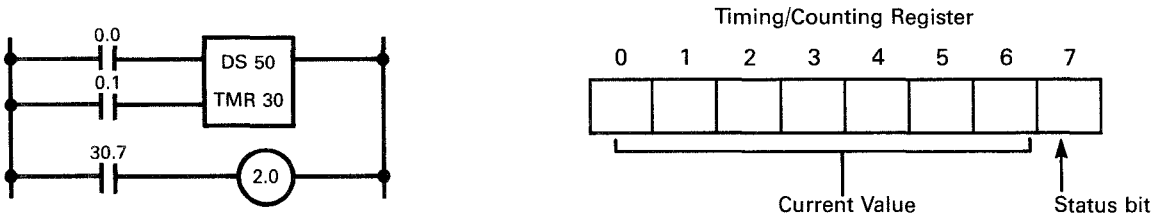


Figure 6-9. Manipulation of Timer and Counter.

Using the procedures described in Section 7-3, individual bits of the timing/counting register can be manipulated and the operations described in Sections 6-6 through 6-8 carried out.

6-6. Forcing ON the Status Bit

Forcing the status bit ON will cause the timer/counter to appear to have timed/counted out and will hold its current value constant.

Example: C REG 3 0 . 7 CALL OC ON

To read the remaining time/count, display the current value, by pressing:

C TMR REG 3 0 CALL

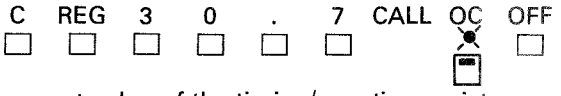
NOTE: A status bit in the OFF state can only be forced ON while the processor is in the RUN mode and the timer/counter enable circuit is conducting. If the status bit is forced ON while the processor is in the PRG mode, the forced ON condition will not be maintained when the processor is switched to RUN. Likewise, if the status bit is forced ON while the timer/counter is not enabled, the forced ON condition will not be maintained when the timer/counter is re-enabled.

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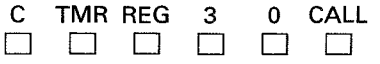
6-7. Removing the Forced Condition ON the Status Bit.

After the operation described in Section 6-6, the timer/counter can be allowed to resume timing/counting by removing the force ON the status bit. The timer/counter will resume where it left off, if the processor is in the RUN mode and the enable circuit is energized.

Example:



To monitor the current value of the timing/counting register, press:



NOTE: The status bit cannot be forced OFF after the timer/counter has timed/counted out normally and has set the status bit on. To reset the timer/counter, the enable circuit must be de-energized.

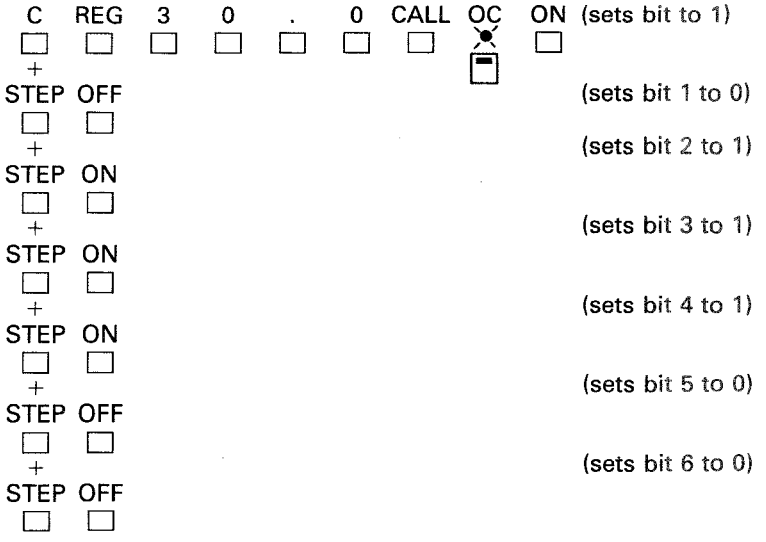
6-8. Altering the Current Value.

After the operation described in Section 6-6, the current value of the timer/counter can be changed to an arbitrary value between 0 and 127. This is accomplished by individually forcing bits 0 through 6 to agree with the binary representation of the desired new current value.

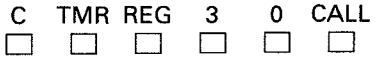
For example, the binary representation of the decimal value 29 is

$$11101_2 = (1 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$$
$$= 16 + 8 + 4 + 0 + 1$$
$$= 29$$

To change the current value of the timing/counting register to decimal value 29, bits 0, 2, 3, and 4 must be set to 1 and bits 1, 5, and 6 must be reset to 0.



To confirm that the current value is now, indeed, 29, display the timing/counting register in decimal, using the procedure explained in Section 6-3.



Removing the force on the status bit will allow the timer/counter to restart from the newly assigned current value.

NOTE:

(1) In any case, opening the enable circuit causes the timer/counter to reset, that is, the current value is cleared and the status bit is set.

(2) All forces to the timer/counter are required to be performed while the processor is in the RUN mode and while the timer/counter enable circuit is conducting. A force attempted under any other conditions will not be held when the required conditions are established.

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TABLE 6-2. ERROR DISPLAY ON PROGRAM LOADER

Display①		Cause and Explanation	Correction
STEP	REGISTER		
	Err0 (Flashing)	• Key entry error • Incorrect instruction entered	Display the instruction by pressing the C key. Then correct it.
	Err1 (Flashing)	• Program entry not allowed (attempt to program in RUN mode; RAM change when the EPROM is installed) • PRG/RUN switch changed during cassette operation	Same as above. While in cassette operation, pressing the C key clears the error from the display.
Error address	Err2	• RAM chip error • The STEP display shows an invalid absolute address in hexadecimal format.	Contact Westinghouse representative at 800-245-6326 (in Pennsylvania, 412-963-1330).
Error step	Err3	• Instruction parity error • The STEP display shows the number of a step having an invalid instruction.	After selecting PRG mode, correct the program at the step containing the invalid instruction.②
Error step	Err4	• Instruction format error • The STEP display shows the number of a step having an invalid instruction.	Same as above.②
E1C	Err5	• Status of output circuitry is invalid. • PCE-111 I/O Expander Cable was disconnected during RUN mode. • Programming not possible due to noise. • Internal circuitry error. • The STEP display shows an invalid code.	Turn off the power. Check the I/O Expander and Cable, and turn on the power again.② If the error persists, contact Westinghouse representative at 800-245-6326 (in Pennsylvania, 412-963-1330).
E1 E2 E3④	Err6	• PCE-111 I/O Expander Cable was connected during RUN mode. • PCE-101 I/O Expander Cable was connected or disconnected during RUN mode. • I/O Expander Cable error. • Communication not possible. • The STEP display shows the number of I/O Expander in fault.	Turn off the power. Check the I/O Expander and Cable, and turn on the power again.②
	Err7	• Display only if the battery is faulty at the time power is turned on. • In other cases, the BATT lamp illuminates.	Check the battery.③

①Display illuminates when the loader is connected. Display is possible even if the loader is connected after an error has occurred.
②After an error has occurred, all inputs and outputs go off and the RUN contact opens. To reset the display, turn the power OFF, remove the cause of the error, and then turn the power ON again.
③The display can be reset only in PRG mode.
④In the PC-110 system, E1, E2, and E3 represent the unit number of the I/O Expander.

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Section 7

Tape Function

The NLPL-180 Program Loader has the ability to interface with an audio cassette recorder for recording and loading the contents of the processor's program memory.

7-1. Recording and Loading Guidelines

(1) If possible, use a tape recorder without sophisticated functions, such as bias for metal-oxide tape, Dolby* noise reduction, etc.

(2) Use the same recorder for recording, verifying, and loading. If a different recorder is used, verification and loading may not be possible.

(3) Do not use a recorder that has worn tape heads because this can reduce recording quality.

(4) Clean the tape heads regularly.

(5) If the unit has tone control, select the highest setting for maximum treble response.

*Registered trademark Dolby Labs.
**Registered trademark Tandy Corporation.

(6) Use a new audio cassette tape of good quality with normal bias. Do not use high bias (CrO_2) and metal tapes, or tapes longer than 30 minutes per side.

(7) To prevent recording errors and extend the life of the tape, do not record beyond the middle of either side of the tape.

(8) Use an AC adapter to insure uniform tape speed. If an AC power adapter is not available, install fresh batteries.

(9) Consult the manufacturer's instructions for proper operation and maintenance of the recorder.

7-2. Connecting the Recorder

Select the appropriate recorder jack for the desired operation, as shown in Figure 7-1. Use a cable with a subminiature phone jack on both ends (Radio Shack** #44-2420 or equivalent).

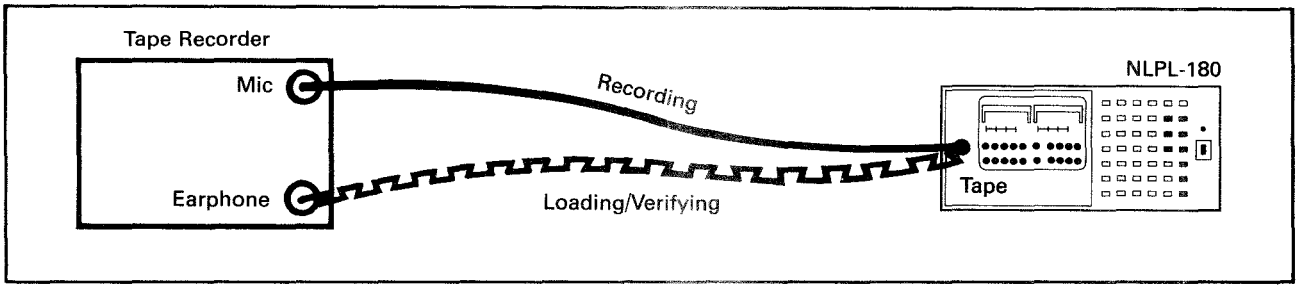


Figure 7-1. Connecting the Recorder.

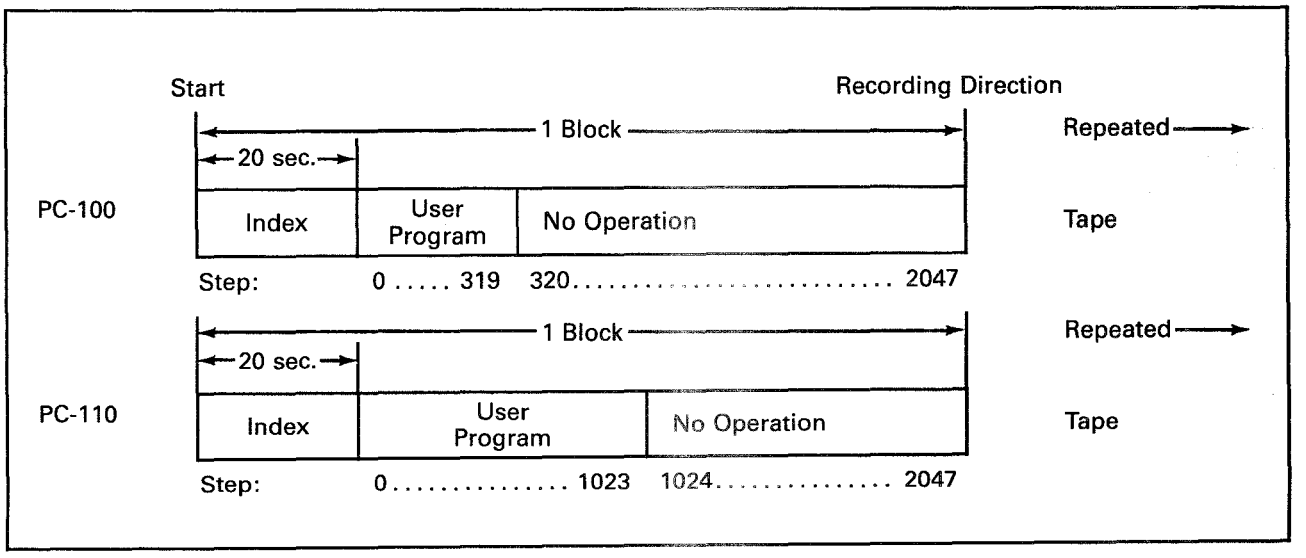


Figure 7-2. Recording Format

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7-3. Recording

This operation is used to record the contents of processor memory onto cassette tape. The volume setting on the recorder is not important for the recording operation. After recording, verify that the information recorded on the cassette tape agrees with the contents of processor memory by performing the procedure described in Section 7-3.

TABLE 7-1. RECORDING

Operation Flow	Key Sequence	Results: STEP Display	Results: REGISTER Display	Remarks
Connect TAPE terminal on the program loader to MIC terminal on the tape recorder.	PRG ▨□ RUN OR PRG □▨ RUN			• Mode switch can be in PRG or RUN position.
Place cassette into tape recorder.				
Select recording mode on tape recorder.	C □			• Press C, REC, and ENT on NLPL-180 within 5 seconds after selecting recording mode on the tape recorder.
Recording.	REC □	0	rEC	• The REGISTER display shows the number of the program step currently being recorded. The STEP display shows the number of recording iterations.
	ENT □	0 1	0000	
		0 1	2047	• NOP (No Operation) instructions are recorded after the last program step (319 or 1023) through step 2047.
Stop recording.	C □	0 2	2047	• The recording stops after the C Key is pressed.

7-4. Recording Format

The PC-100 and the PC-110 record in the format shown in Figure 7-2. Only the contents of memory locations containing program instructions are recorded; the contents of data registers are not recorded. During the recording operation, the step number of the program instruction that is currently being recorded is shown on the REGISTER display. After all program instructions have been recorded (Steps 0 to 319 for the PC-100; Steps 0 to 1023 for the PC-110), the REGISTER display continues to be incremented until its value reaches 2047. (During this time, NOP [no operation] instructions are recorded.) Upon reaching 2047, the recording process is complete: one full block has been recorded. At this time, the recording process will begin again and the digit "1" that was present on the STEP display will be replaced by a "2," indicating that the second recording iteration has begun. The iteration process will continue to record the identical block of data until the C key is pressed, stopping the recording.

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7-5. Verification

This operation is used to verify that the information recorded on the cassette tape agrees with the contents of the processor memory. Always verify after recording or loading, using the procedure outlined in Table 7-2 below. If an inconsistency is found, correct it by repeating the recording or loading procedure. Verify again to see that the recorded information agrees with the contents of program memory.

Before attempting these procedures, see Section 7-6, "Selecting the Correct Volume for Verification."

TABLE 7-2. VERIFICATION

Operation Flow	Key Sequence	Results: STEP Display	Results: REGISTER Display	Remarks
Connect TAPE terminal on the program loader to EAR terminal on the tape recorder.	PRG ▨□ RUN OR PRG □▨ RUN			• Mode switch can be in PRG or RUN position.
Place cassette into tape recorder.				
Select play mode on tape recorder.	C			• Playback begins.
Volume OK? / Turn up recorder volume / No / Yes	VER	-	UEr	• See Section 7-4, "Selecting the Correct Volume."
	ENT	-0-0	Hd	
Stop recorder.	C			
Rewind tape recorder.				
Select play mode on tape recorder.	C			• Playback begins.
Verifying.	VER	-	UEr	• Verification begins. Verification is automatic for up to 10 blocks stored on cassette tape. The STEP display shows the number of the block being verified.
	ENT	-0-0	Hd	
		-1-0	0007	
Stop verification.	C	-2-2	Hd	• Verification stops after the C key is pressed.

7-6. Selecting the Correct Volume for Verification

The range of volume for which the verification and loading operations will function properly is narrow. Follow the suggestions below to arrive at the optimal volume level.

(1) Start at the lowest volume setting on the recorder.

(2) Begin verification, as shown in Section 7-5.

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(3) Allow 20 seconds for the tape header to pass. During this time, the REGISTER display will flash "Hd" and the STEP display will show -0-0.

(4) If the "Hd" message continues to flash on the REGISTER display and the STEP display continues to show -0-0 after 30 seconds, the volume is too low. (Invalid data is being read by the PC.)

(5) Slowly raise the volume setting until the flashing "Hd" message disappears and is replaced by a program step number. This indicates that the correct volume setting has been located and that valid data can be read by the PC.

(6) Once the correct volume setting has been located, rewind the tape and begin the verification procedure at the correct volume level.

7-7. Loading

This operation is used to load a program, which has been prerecorded on cassette tape, into the processor memory.

NOTE: The volume range on the recorder at which the loading operation will function properly is narrow. Before attempting to load, locate the optimal volume setting on the recorder. (If a cassette tape of the program memory currently in the processor is available, locate the correct volume setting by following the procedure in Section 7-4.) After loading, verify that the information loaded into the processor's program memory agrees with the information on the cassette tape by performing the verification procedure described in Section 7-3. If the loading operation was not successful at the chosen volume level, adjust the volume and reattempt the operation. Repeat this sequence until a suitable volume level is found.

TABLE 7-3. LOADING

Operation Flow	Key Sequence	Results: STEP Display	Results: REGISTER Display	Remarks
Set mode switch to PRG.	PRG ▨□ RUN			• Must be in PRG mode.
Connect TAPE terminal on program loader to EAR terminal on tape recorder.				
Place cassette into tape recorder.				
Select play mode on tape recorder.				• Playback begins.
Loading.	C □ PLAY □ ENT □	U U U 1	PLA Hd 0007	• The REGISTER display shows the number of the step currently being loaded. The STEP display shows the number of blocks that have been loaded.
Stop loading.	C □	U 1	End	• "End" is displayed when loading is complete.①

①If a loading error occurs while the processor is checking for errors, it stops loading its block and stands by until the next block is automatically transferred. The processor stops automatically when it has completed the loading operation. The PC-100 reads program instructions from step 0 to 319 and NOP (No Operation) instructions from 320 to 2047. The PC-110 reads program instructions from step 0 to 1023 and NOP instructions from step 1024 to 2047.

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Section 8
Installation and Wiring

8-1 Installation Guidelines

Follow the guidelines listed below when installing the PC-100 and PC-110.

(1) Install the programmable controller in a drip-proof, dustproof enclosure appropriate for the operating environment.

(2) Install the programmable controller so that its mounting surface is placed in a vertical position.

(3) Do not install the programmable controller in a location subject to intense vibration.

(4) For proper ventilation, follow the clearance guidelines shown in Figure 8-1.

(5) Install a fan if the interior temperature of the enclosure exceeds 50°C (122°F).

(6) Do not install a heating element under the programmable controller.

(7) Do not install any high voltage equipment in the same enclosure as the programmable controller.

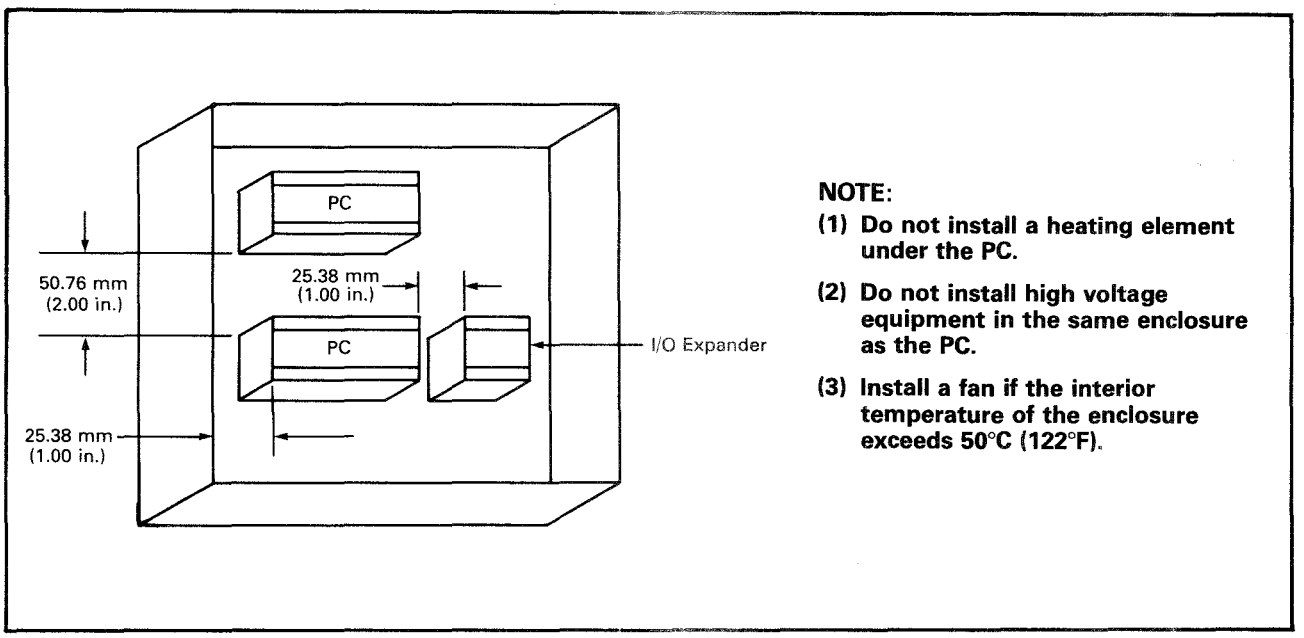


Figure 8-1. Installation Guidelines

8-2 External Connection

(1) Separate the programmable controller's I/O field wiring from any high-voltage cable or power cable, and do not run it in parallel with the power cable.

(2) Isolate the I/O Expander cable from other cables.

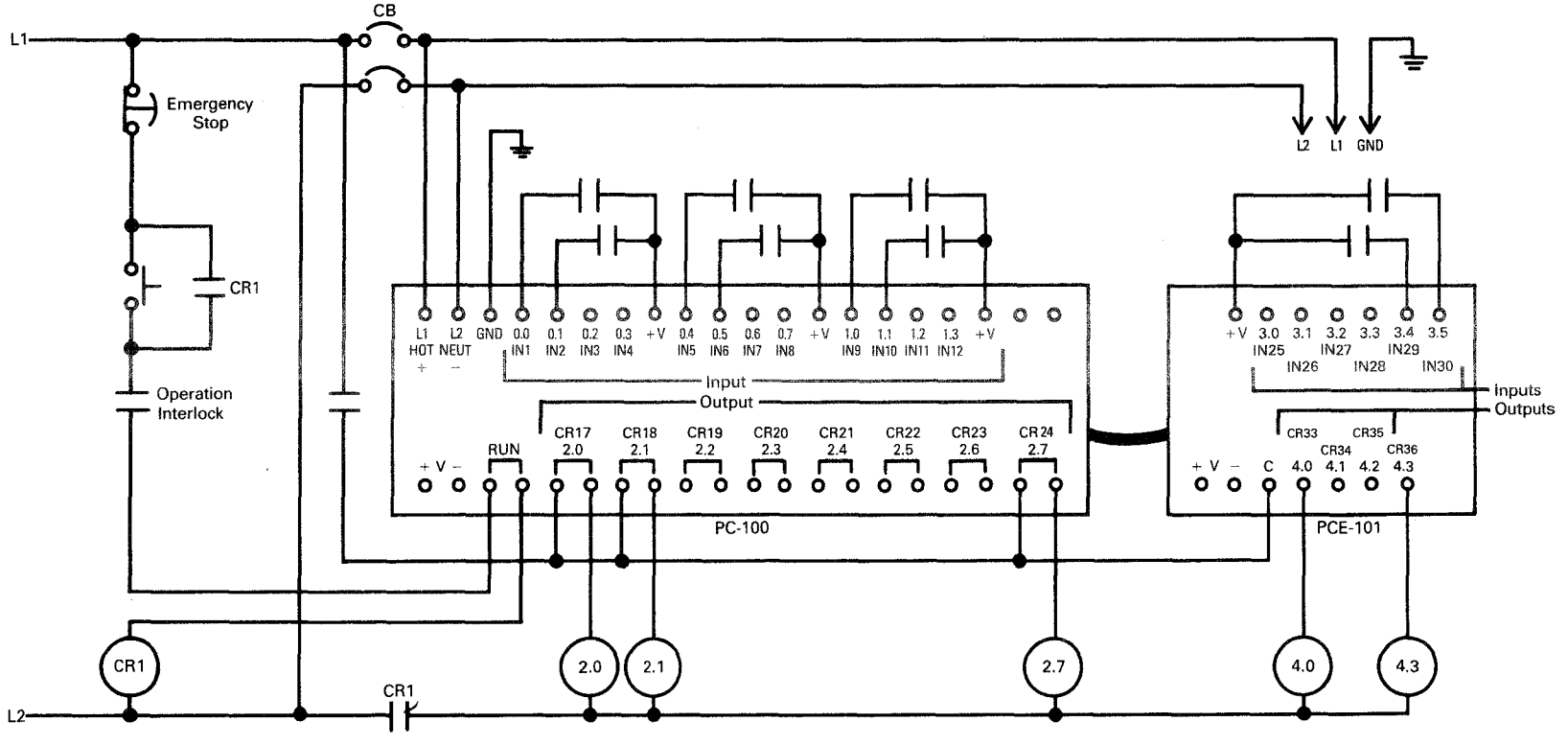
(3) Use No. 16 AWG wire for connection at AC power terminals.

NOTE

For both the PC-100 and the PC-110, the power necessary for the operation of the 24 VDC input circuits is provided by the programmable controllers' internal power supply. Voltage from an external source should not be applied to the 24 VDC input circuit terminals.

8

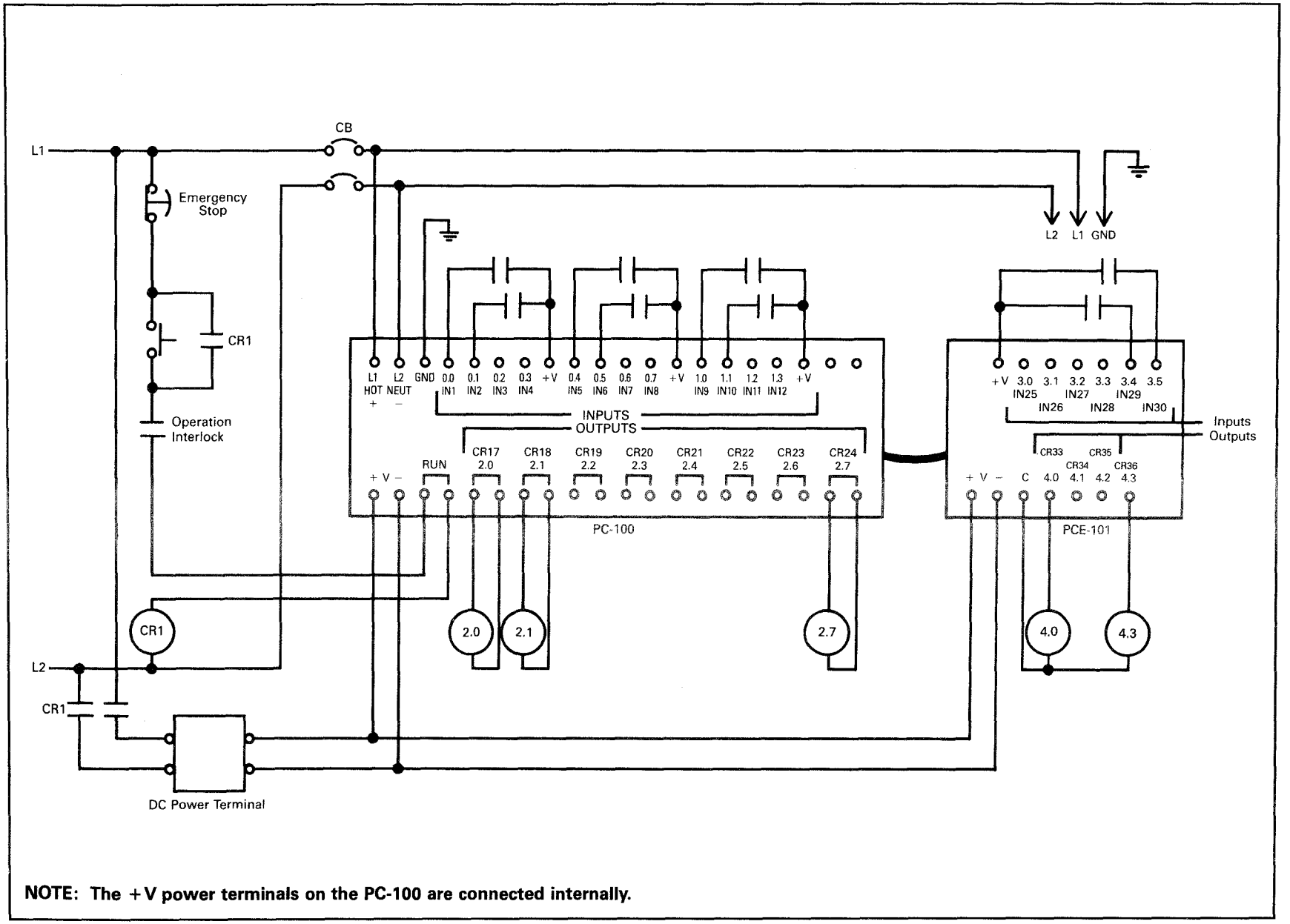
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NOTE: The +V power terminals on the PC-100 are connected internally.

Figure 8-2. PC-100 External Connection: Relay or Triac Outputs.

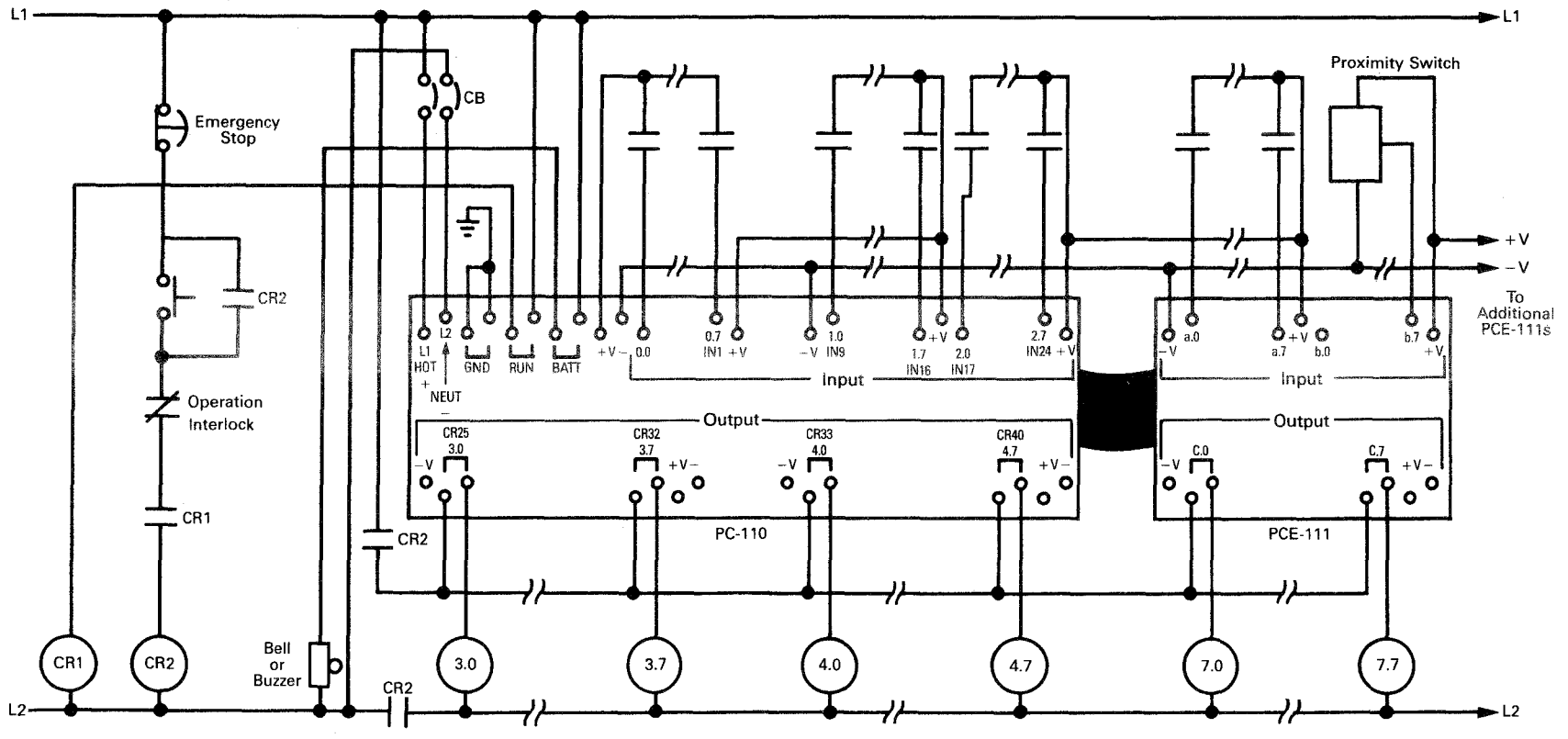
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NOTE: The +V power terminals on the PC-100 are connected internally.

Figure 8-3. PC-100 External Connection: DC Source Outputs

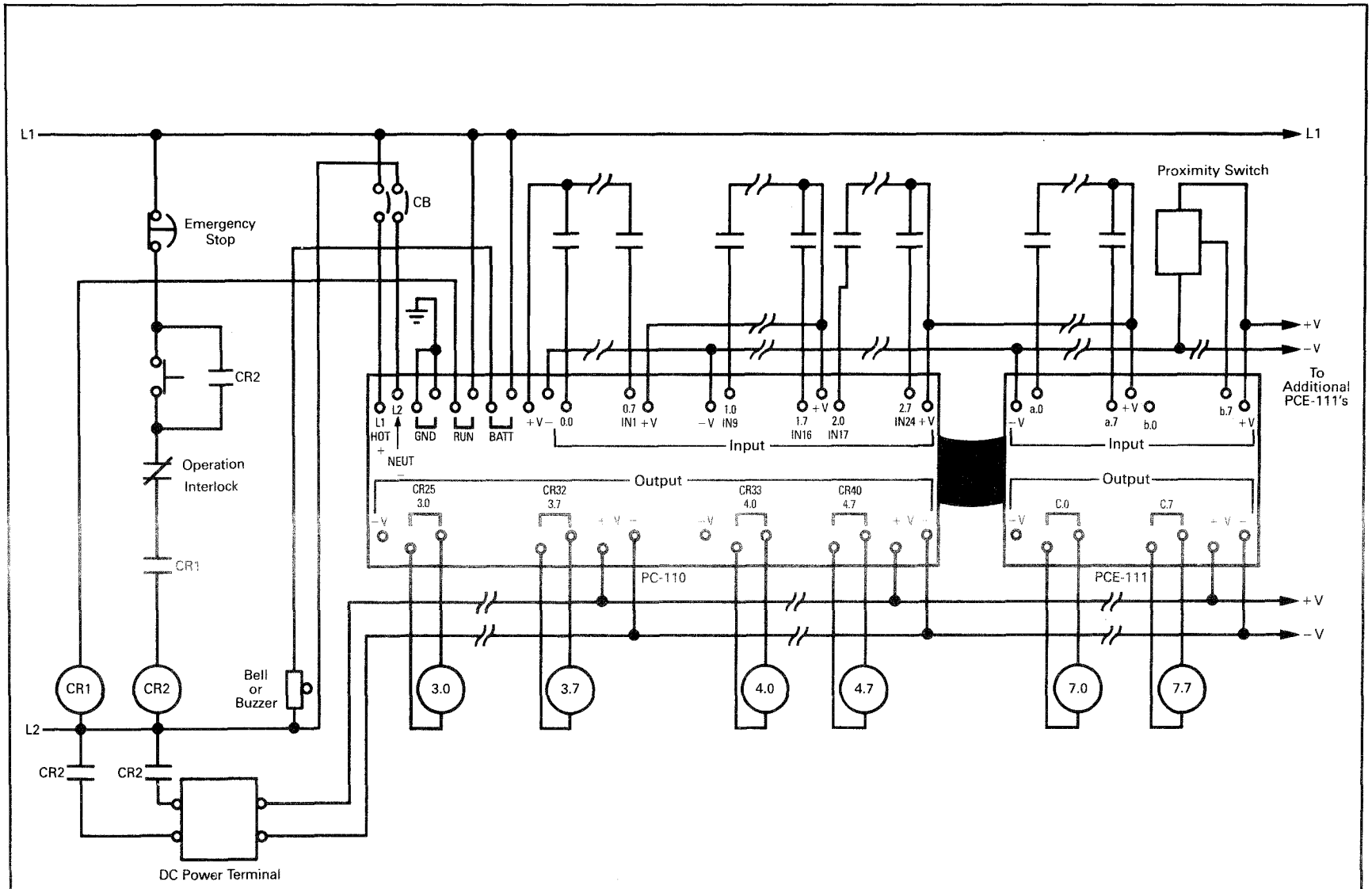
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NOTE: All input and output terminals on the PC-110 and PCE-111 are NOT illustrated in Figure 8-4. In addition, the +V power terminals on both units are connected internally.

Figure 8-4. PC-110 External Connection: Relay or Triac Outputs

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NOTE: All input and output terminals on the PC-110 and PCE-111 are NOT illustrated in Figure 8-5. In addition, the +V power terminals on both units are connected internally.

Figure 8-5. PC-110 External Connection: DC Source Outputs

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Section 9
Start-up and Maintenance

9-1. Start-up Procedures

(1) Confirm that installation is in accordance with the guidelines outlined in Section 8. Check that the enclosure is properly installed; the grounding conductor is correctly connected; and other protective devices, such as a surge suppressor for output control, are provided.

(2) When using I/O Expanders, confirm that each I/O Expander Cable is correctly and securely connected to the programmable controller (or another Expander, for the PC-110 only).

(3) Confirm that the field wiring to the I/O terminals is securely connected.

(4) Before applying power, set the processor mode switch to PRG. Then apply power and check the following:
  (a) the processor RUN contact is open and the RUN LED is off.
  (b) the BATT, CPU, and MEM LEDs are on.①

(5) Set the processor mode switch to RUN and check the following:
  (a) the processor RUN contact is closed and the RUN LED is on.
  (b) the BATT and MEM LEDs remain on, and the CPU LED flashes.
  (c) the I/O modules and their indicators operate as programmed. If the PC does not perform sequential operations as desired, check and modify the program.

(6) Turn OFF the control power before connecting or disconnecting an I/O Expander or EPROM.

①If the back-up capacitor is discharged, it may take several minutes before it recharges and the BATT LED turns on.

9-2. Capacitor and Battery Memory Back-up Systems

In the event of a power loss, the contents of RAM of the PC-100 and PC-110 are supported by an internal capacitor (standard) or by an optional lithium battery. Procedures for installing and replacing the batteries are outlined below.

9-3. PC-100 Memory Back-up

When a Battery Is NOT Used

When neither the Battery Cartridge nor the EPROM Cartridge is installed, the processor defaults to back-up by its internal capacitor. No action is necessary.

When a Battery Is Used

Slide the NLB-100 Battery Cartridge, with its window directed inward, in the slot at the left end of the processor, as shown in Figure 9-1.

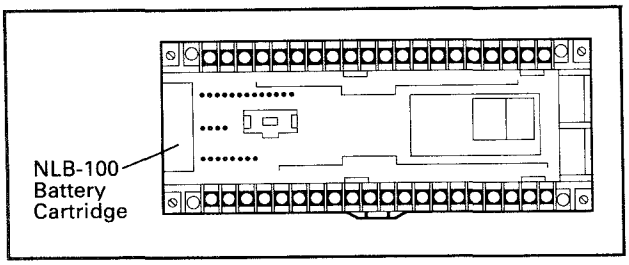


Figure 9-1. PC-100 Battery Cartridge Installation.

9-4. PC-110 Memory Back-Up

When a Battery Is NOT Used

To verify that the internal capacitor is activated, remove the cover of the EPROM socket and check that the short-circuit cable is in place, as shown, in Figure 9-2. The capacitor will not function unless this connection is in place.

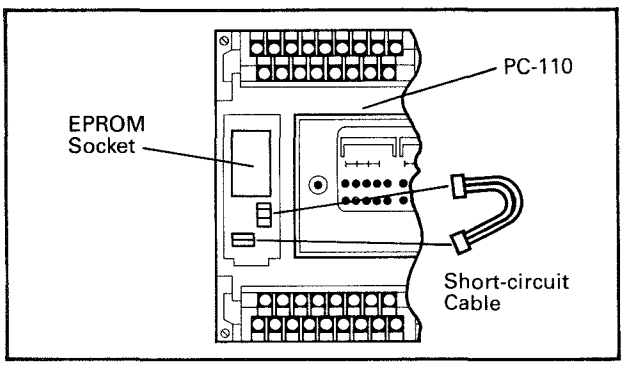


Figure 9-2. Short-circuit Cable Installation.

When a Battery Is Used

Remove the cover of the EPROM socket, and then the short-circuit cable, as shown in Figure 9-2. Next, connect the battery cable to the lower connector, as shown. Finally, snap the battery cover to the processor.

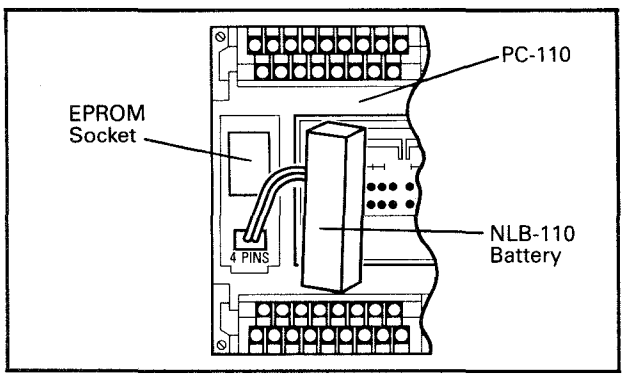


Figure 9-3. PC-110 Battery Installation.

NOTE: Replace the battery periodically, at least once every three years. For a description of conditions indicating battery failure, refer to Section 9-5.

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9-5. Battery Failure

When a battery error occurs immediately after the power is turned ON, the display on the program loader shows "*ERR7*;" the BATT OK indicator turns off; and internal coil 63.0 turns on.① The RUN contact is open even in the run mode, and the RUN indicator remains off.

When a battery error occurs under any other condition than described above, nothing is displayed on the loader, the BATT OK indicator turns off, and internal coil 63.0 turns on.① When the processor is in the run mode, the run contact remains closed and the RUN indicator remains on.

To correct a battery error, set the processor mode switch to PRG and turn OFF the power. Replace the battery with a new one, as described in Section 9-2.

TABLE 9-1. CORRECTION OF BATTERY FAILURE IN PC-100.

	BATT OK LED Indicator	Internal Coil 63.0
During Normal State	On	Open
During Faulty Battery State	Off	Closed

①Internal coil 63.0 can be used to turn on an output, which can, in turn, activate an external alarm announcing the battery fault.

When a battery error occurs immediately after the power is turned ON, the display on the program loader shows "*ERR7*;" the BATT indicator turns off; and the BATT contact closes.② The RUN contact is open even in the run mode, and the RUN indicator remains off.

When a battery error occurs under any other condition than described above, nothing is displayed on the loader; the BATT indicator turns off; and the BATT contact closes.② When the processor is in the run mode, the RUN contact remains closed and the RUN indicator remains on.

To correct a battery error, set the processor mode switch to PRG and turn OFF the power. Replace the battery with a new one, as described in Section 9-2.

TABLE 9-2. CORRECTION OF BATTERY FAILURE IN PC-110.

	BATT LED Indicator	BATT Contact
During Normal State	On	Open
During Faulty Battery State	Off	Closed

②The BATT contact can be used to activate an external alarm announcing the battery fault.

9-6. Troubleshooting I/O

Follow the guidelines below to troubleshoot input and output circuits.

(1) Connect the NLPL-180 Program Loader to the PC.

(2) Call the contact or coil in question (see Section 5-3).

(3) Observe the MON indicator on the Program Loader under the conditions specified in Tables 9-3 and 9-4.

TABLE 9-3. TROUBLESHOOTING INPUT CIRCUITRY

External Input Signal	Input Terminal	Input Indicator	MON Indicator	Cause	Correction
On	Voltage applied	✕	✕	Normal	
On	Voltage applied	○	○	Input circuit defective	• Contact Westinghouse representative.
On	No voltage	○	○	External input device or wiring defective	• Check external input device and wiring.
Off	No voltage	✕	✕	Input circuit defective	• Contact Westinghouse representative.
Off	Voltage applied	✕	✕	External input device or wiring defective; leakage current from external input device; etc.	• Check external input device and wiring.

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TABLE 9-4. TROUBLESHOOTING OUTPUT CIRCUITRY

Signal to External Output Device	Output Terminal	Output Indicator	MON Indicator	Cause	Correction
On	Conductive	✕	✕	Normal	
Off	Non-conductive	✕	✕	Output circuit defective; triac output may cause external failure.	• Contact Westinghouse representative.
Off	Conductive	✕	✕	External wiring defective when relay contacts are used for output. External output device defective.	• Check wiring and external output device.
On	Conductive	○	○	Output circuit defective	• Contact Westinghouse representative.
On	Non-conductive	○	○	External wiring defective, external output device defective, or external interference due to high impedance of external output device.	• Check wiring and external output device.

9-7. EPROM Operation

After programming a sequence in RAM, it is possible to then store the program in EPROM using the EPROM Writer NLEP-190. Once the EPROM is installed in the programmable controller, it controls subsequent processor operations. When an EPROM is not used, the processor operations are controlled from RAM.

The PC-100 utilizes EPROM Cartridge NLEP-195 while the PC-110 utilizes EPROM NLEP-191 (Intel® 2716 or equivalent). Both can be programmed from the NLEP-190 EPROM Writer. When programming the NLEP-195 EPROM Cartridge, the EPROM Interface Socket NLEP-193 must be used as an interface to the NLEP-190. See the instructions included with the NLEP-190 for programming the EPROM.

Once the EPROM is programmed, follow the procedures below for installation in the PC.

Before installing the programmed NLEP-195 EPROM Cartridge, turn OFF the processor's power. Then insert the NLEP-195 into the slot (alternately used for the Battery Cartridge) at the left end of the processor, with its window directed inward, as shown in Figure 9-4.

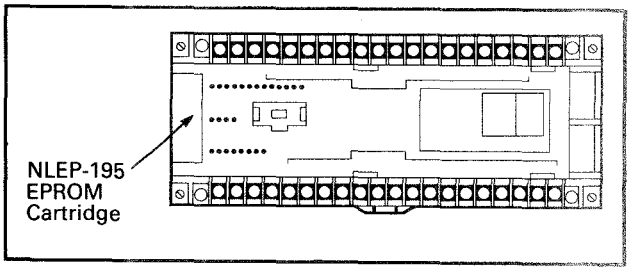


Figure 9-4. PC-100 EPROM Cartridge Installation.

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Before installing the programmed NLEP-191 EPROM, turn OFF the processor's power. Unlock the EPROM locking lever, mount the NLEP-191, and again lock the lever, as shown in Figure 9-5.

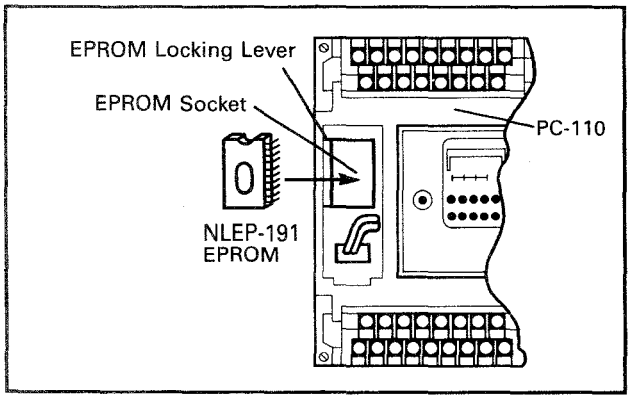


Figure 9-5. PC-110 EPROM Installation.

9-8. EPROM Application Notes

(1) When the power is restored, the program in the EPROM is transferred to RAM for subsequent processor operations.

(2) If a blank EPROM is installed, operation is performed by the original contents of RAM.

(3) Turn OFF the power before removing the EPROM.

(4) When the EPROM is removed, the contents of RAM remain intact.

(5) The RAM program cannot be modified with the EPROM installed.

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Appendix

SAMPLE PROGRAM SHEET

Page ____ of ____

Step No.	Instruction Word(s)	Ref. No.	Remarks	Step No.	Instruction Word(s)	Ref. No.	Remarks
00				50			
01				51			
02				52			
03				53			
04				54			
05				55			
06				56			
07				57			
08				58			
09				59			
10				60			
11				61			
12				62			
13				63			
14				64			
15				65			
16				66			
17				67			
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39				89			
40				90			
41				91			
42				92			
43				93			
44				94			
45				95			
46				96			
47				97			
48				98			
49				99			

Program Name		Format	Prepared by	Checked by	Approved by
Customer	Delivery to	Drawing No.			

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SAMPLE DATA MEMORY ALLOCATION SHEET

	EXTERNAL
	INTERNAL

Page ____ of ____

Address	Contents	Page	Remarks	Address	Contents	Page	Remarks
0.0				5.0			
0.1				5.1			
0.2				5.2			
0.3				5.3			
0.4				5.4			
0.5				5.5			
0.6				5.6			
0.7				5.7			
1.0				6.0			
1.1				6.1			
1.2				6.2			
1.3				6.3			
1.4				6.4			
1.5				6.5			
1.6				6.6			
1.7				6.7			
2.0				7.0			
2.1				7.1			
2.2				7.2			
2.3				7.3			
2.4				7.4			
2.5				7.5			
2.6				7.6			
2.7				7.7			
3.0				8.0			
3.1				8.1			
3.2				8.2			
3.3				8.3			
3.4				8.4			
3.5				8.5			
3.6				8.6			
3.7				8.7			
4.0				9.0			
4.1				9.1			
4.2				9.2			
4.3				9.3			
4.4				9.4			
4.5				9.5			
4.6				9.6			
4.7				9.7			

Program Name		Format	Prepared by	Checked by	Approved by
Customer	Delivery to	Drawing No.			

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Style No. B828/16-350
October, 1984

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