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OPERATIONS MANUAL
EBC-BX

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1 General Information

1.1 Features

- Intel Low Power Celeron Processors and Low Power Pentium III processors
- EBX-compliant board
- 256KB/128KB of pipeline burst L2 cache (Pentium III/Celeron)
- Up to 256MB of SDRAM
- Socket for bootable DiskOnChip or DIP socket for BIOS extension support of Flash or ROM
- PC Compatible uses Intel 443BX chip set
- On board high resolution AGP 1X video controller
- Flat panel video support
- Supports resolutions up to 1280 x 1024
- Simultaneous CRT and LCD operation
- PC-104/Plus and PC/104 expansion buses
- 10/100 Mbps Ethernet using Intel 82559
- 4 RS-232 serial ports with FIFO, COM1 & COM2 supports optional RS-422/485/J1708 support
- Bi-directional LPT port supports EPP/ECP
- Dual IDE channels support UDMA-33 and UDMA-66 Drives
- 48 bi-directional TTL digital I/O lines

1.2 General Description

The EBC-BX is a small, high-performance, embeddable computer system on a single board. It integrates a number of popular I/O options including AGP 1X VGA, Ethernet, Solid-State Disk, and High-Density Parallel I/O. Four PC compatible serial ports are standard, as are the floppy, hard disk, and parallel printer interfaces. The EBC-BX is populated with either an Intel low power Celeron processor or an Intel low power Pentium III processor at speeds from 300 to 700 MHz. Up to 256Mbytes of user installable DIMM memory is supported. A 16-bit PC/104 expansion bus and the PC/104Plus bus is provided for further expansion to an entire industry of add-on peripherals including sound and speech modules, SCSI controllers, Analog I/O modules, and literally hundreds of other options available from WinSystems and a variety of vendors supporting the PC/104 and PC/104-Plus standards. An onboard 32-pin silicon disk socket supports the M-Systems' Disk On Chip Flash modules in sizes ranging from 8 Megabytes to over 500 Megabytes.

1.3 Specifications

1.3.1 Electrical

Bus Interface : PC/104 8-Bit or 16-Bit expansion bus
PC/104-Plus 32-bit expansion bus

System Clock : FSB 100MHz

Interrupts : TTL Level input

VCC : +5V +/- 5% at 2.75A typical with an Intel 400Mhz Celeron processor with 32MB SDRAM

+5V +/-5% at 3.4A typical with an Intel Pentium III processor at 700 Mhz with 32MB SDRAM

VCC1 : +12V +/-5% (Not required. PC/104 Expansion, Flat Panel, use only)

VCC2 : -12V +/-5% (Not required. PC/104 Expansion or Flat Panel use only)

VCC3: 3.3V (Not required. PC/104 Plus expansion use only)

Memory Addressing : 256 Megabyte addressing

BIOS ROM : 256K Atmel Flash (reprogrammable on board)

Memory DIMM Socket : 168-pin 3.3V Dimm Module; PC-100 SDRAM Module

SSD Memory : One 32-pin JEDEC standard socket supporting the M-Systems' 32-Pin DOC (DiskOnChip) module.

1.3.2 Mechanical

Dimensions : 5.75 X 8.0 X 0.60 inches (without PC/104 modules or cables)

PC-Board : FR4 Epoxy Glass with 6 signal layers and 4 power planes with screened component legend, and plated through holes

Jumpers : 0.025" square posts on 0.10" centers

Connectors : Multi I/O : 50-pin RN type IDH-50LP

COM3/COM4 : 20-pin RN type IDH-20LP

Floppy Disk : 34-pin RN type IDH-34-LP

CRT :	14-pin 2mm Molex Type 87331-1420
Flat Panel :	Two, 50-pin 2mm Molex type 87331-5020
Power/Reset :	9-pin in-line Molex type 26-60-7091
Fan Power :	3-pin in-line Molex type 22-11-2032
Mouse :	5-pin in-line latching Molex type 22-11-2052
USB :	4-pin in-line latching Molex type 22-11-2042
PC/104 Bus :	64-Pin SAMTEC type ESQ-132-12-G-D 40-Pin SAMTEC type ESQ-120-12-G-D
PC/104-Plus Bus :	120-Pin SAMTEC type TS-30-Q
IDE :	Two 40-pin 2mm Molex Type 70246-4021
Ethernet :	RJ-45

1.3.3 Environmental :

Operating Temperature :	-40° to +60° C
Non-condensing relative humidity :	5% to 95%

2 EBC-BX Technical Reference

2.1 Introduction

This section of the manual is intended to provide sufficient information regarding the configuration and usage of the EBC-BX board. WinSystems maintains a Technical Support group to help answer questions regarding configuration, usage, or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

2.2 Intel FW82443BX / SMSC Victory-66 Chipset

The EBC-BX utilizes the Intel FW82443BX North bridge coupled with the SMSC Victory-66 South bridge. This combined chipset provides a highly-integrated, high-performance backbone for full Pentium class compatibility. The Chipset contains the logic for DRAM and bus state control as well as the standard complement of 'AT' class peripherals, including :

Two-82C37 DMA controllers
Two-82C59 Interrupt controllers
82C54 Timer/Counter
Real Time Clock
Enhanced Power Management
Full Plug and Play compatibility

These functional units are 100% PC/AT compatible and are supported by the Award BIOS and setup. Users desiring to access these internal peripherals directly should refer to any manufacturers generic literature on the equivalent discrete component.

There are a number of internal registers within the BX chipset that are used by the BIOS for control and configuration. Refer to the I/O map in Appendix A for port usage to avoid conflicts when adding external I/O devices.

2.3 Memory Installation

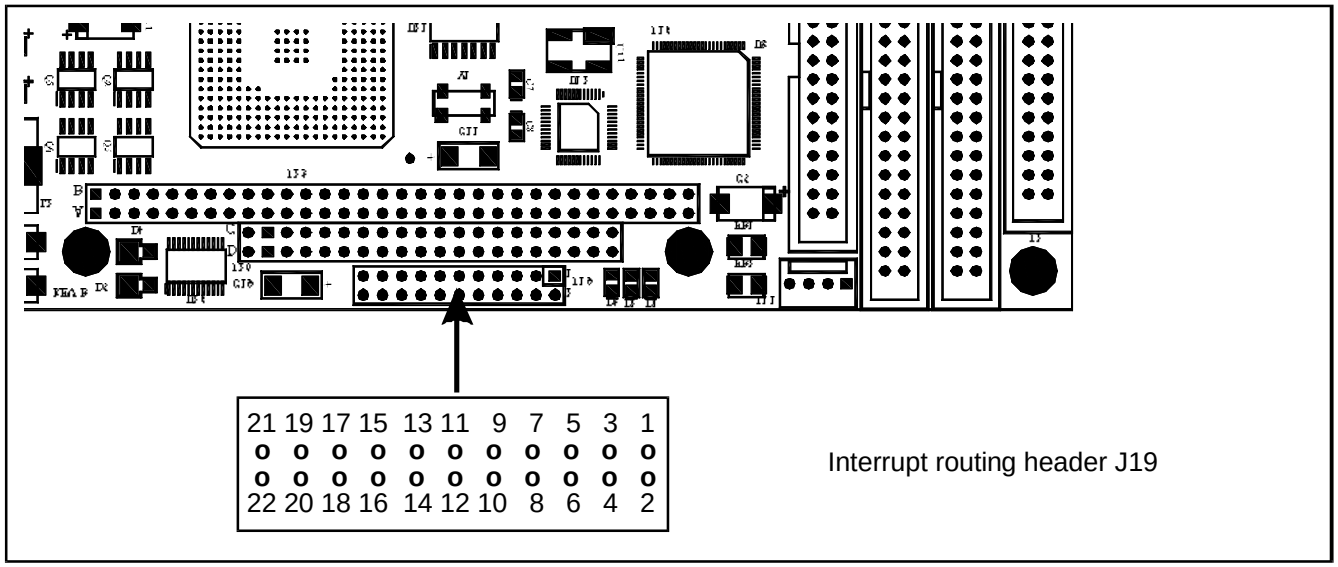
The EBC-BX supports a single user installable 168-pin standard DIMM. DIMM modules should be a minimum speed of PC-100 and x64 or x 72. Either ECC on non-ECC parts may be used. A single DIMM socket is provided which can support SDRAM sizes from 32MB to 256MB. For a list of qualified DIMMs, go to **http://www.winsystems.com/memory**

Installation is accomplished with power off by inserting the DIMM module directly into the connector at M1. The DIMM module is keyed in 2 places and cannot be inserted backwards without ex-

treme force. The module is inserted until the retaining clips snap into place. Removal is the reverse process. Push down on the retaining clips, moving them outward. The DIMM module, once released, will be forced up to an appropriate removal position.

2.4 Interrupt Routing

All interrupts on the EBC-BX are routed to their respective PC/104 bus pins. On board non-PnP peripherals, are routed to their typical usage interrupts using the jumper block at J19. This block allows disconnecting or rerouting of the onboard interrupts. The layout for the J19 header and the default jumper settings are shown below.

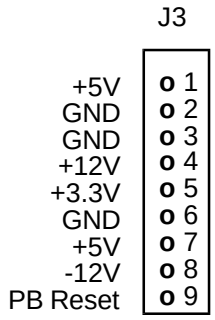


J19

IRQ3	1 o o	2	N/C
IRQ4	3 o o	4	N/C
IRQ5	5 ▬	6	COM3
IRQ7	7 o o	8	N/C
IRQ6	9 o o	10	N/C
IRQ14	11 ▬	12	Primary IDE
IRQ15	13 ▬	14	Secondary IDE
IRQ12	15 o o	16	COM4
IRQ11	17 o o	18	COM3
IRQ10	19 ▬	20	Parallel I/O
IRQ9	21 ▬	22	COM4

2.5 Power/Reset Connections

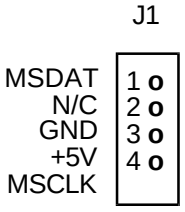
Power is applied to the EBC-BX via the connector at J3 (Molex part number 26-60-7091). The pin definitions for J3 are given below. An optional push-button-reset (Normally Open) may also be routed into J3 if desired. Momentary closure to ground forces a hardware reset.



Note : The 3.3 Volt input pin does not provide power to any devices on the board. It is routed directly to the PC/104Plus Bus and is only required if there are PC/104Plus cards that require 3.3 Volts be supplied from the Bus. The +12 and -12 Volt pins are routed directly to the PC/104 connectors and flat-panel connectors and are not required for normal board operation.

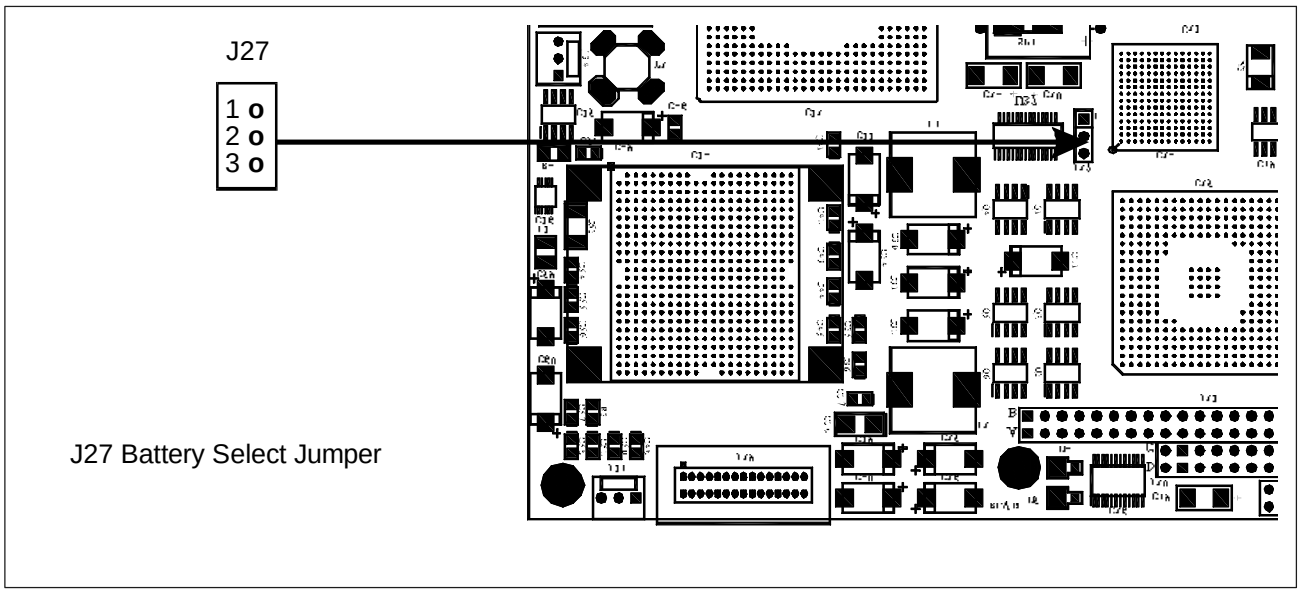
2.6 Mouse Interface

A PS/2 mouse may be attached via the connector at J1. An adapter cable, CBL-225-1 is available from WinSystems to adapt to a conventional PS/2 mouse connector. The pin out for J1 is shown here.



2.7 Real Time Clock/Calendar

The EBC-BX contains an onboard Clock/Calendar within the Victory-66 chip. This clock is fully compatible with the MC146818A used in the original PC-AT computers. This clock has a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept within the CMOS RAM contained in the clock section. This RAM holds all of the setup information regarding hard and floppy disk types, video type, shadowing, wait states, etc. Refer to the section on the Award BIOS Setup for what is configured via the CMOS RAM.



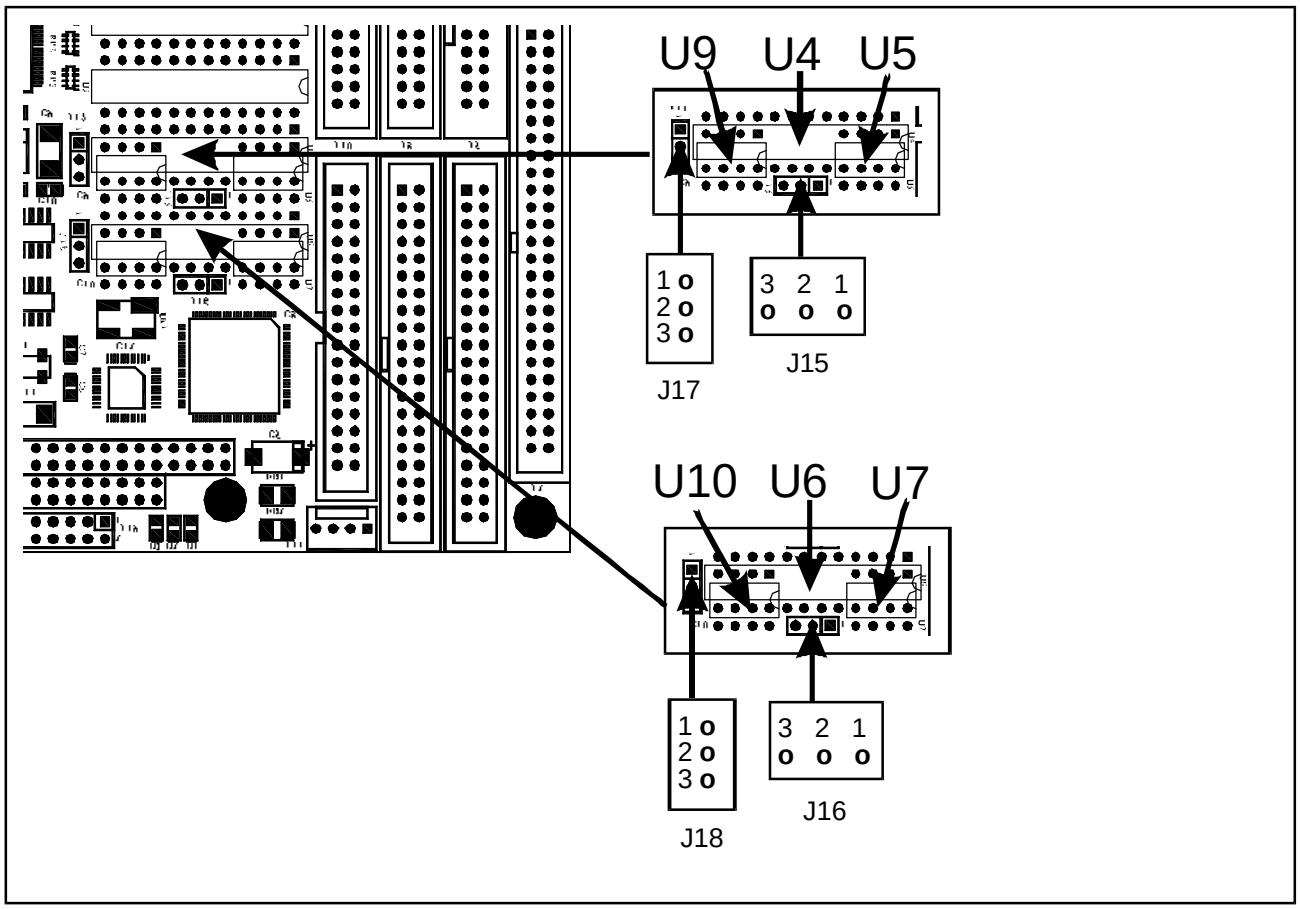
It may become necessary at some time to make the CMOS RAM forget its current configuration and to start fresh with factory defaults. This may be accomplished by removing power from the board . Then remove the jumper from pins 2-3 on J27 and place on pins 1-2 for 10 seconds. Replace the jumper on J27 pins 2-3, power-up, and reconfigure the CMOS settings as desired.

If is desired to operate the board without a battery J27 must be jumpered on pins 1-2.

2.8 Keyboard Interface

The EBC-BX contains an onboard PS/2 style keyboard controller. Keyboard connection is made through the Multi-I/O connector at J2. An adapter cable P/N CBL-247-1 is available from Win Systems to make ready access to all of the devices terminated at the Multi-I/O connector. Users desiring custom connections should refer to the Multi-I/O connector pin definitions given later in this manual.

2.9 Serial Interface



The EBC-BX provides four 16550 compatible RS-232 serial ports at the following addresses :

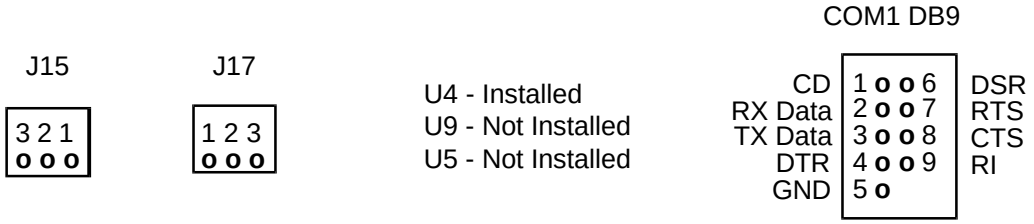
COM1	3F8H	at IRQ 4	(PnP Device)
COM2	2F8H	at IRQ 3	(PnP Device)
COM3	3E8H*	at IRQ 5**	
COM4	2E8H*	at IRQ 9**	

*COM ports 3 and 4 can be enabled or disabled individually via the jumper block at J24. When J24 pins 1-2 are jumpered, COM3 is enabled. When J24 pins 3-4 are jumpered, COM4 is enabled.

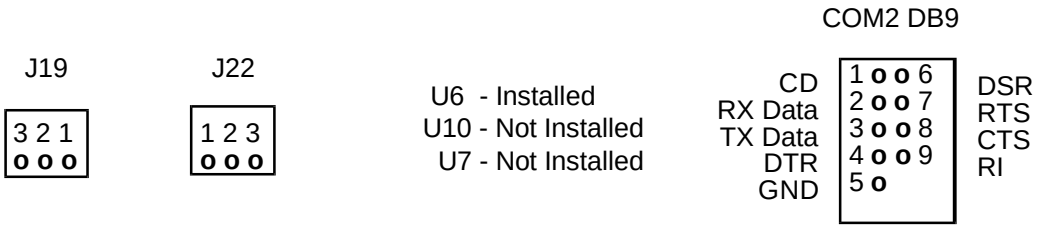
**The interrupts are not disconnected when COM3 or COM4 are disabled. Use the interrupt routing block J19 described earlier to disconnect the default interrupts if desired.

The two primary serial ports, COM1 and COM2 are configurable for RS-422, RS-485 or J1708, with the addition of optional driver ICs (WinSystems P/N CK-75176-2). The configuration options for each of the supported modes are shown on the following pages. Connection to COM1 and COM2 is made through the Multi-I/O connector at J2. An adapter cable (P/N CBL-247-1) is available from WinSystems to adapt to standard DB9 connectors.

COM1 - RS-232



COM2 - RS-232



COM3/COM4 - RS-232

COM3 and COM4 are RS-232 only and are terminated at J4. An adapter cable is available from WinSystems (P/N CBL-173-1), which adapts J4 to two standard DB9M connectors. The pin definitions for J4 are shown here :

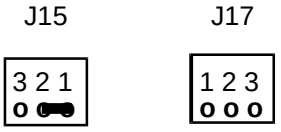
J4

COM3 DCD	1 o o 2	COM3 DSR
COM3 RX	3 o o 4	COM3 RTS
COM3 TX	5 o o 6	COM3 CTS
COM3 DTR	7 o o 8	COM3 RI
GND	9 o o 10	N/C
COM4 DCD	11 o o 12	COM4 DSR
COM4 RX	13 o o 14	COM4 RTS
COM4 TX	15 o o 16	COM4 CTS
COM4 DTR	17 o o 18	COM4 RI
GND	19 o o 20	N/C

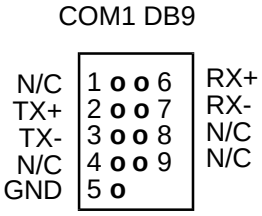
2.9.1 RS-422 Mode Configuration

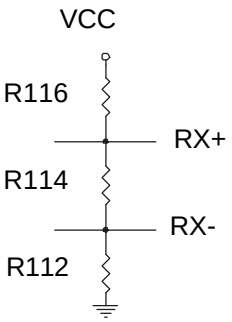
RS-422 levels are supported on both COM1 and COM2 with the installation of the optional “Chip Kit”, WinSystems part number CK-75176-2. This kit provides the driver ICs necessary for a single channel of RS-422. If two channels of RS-422 are required then two kits will be needed. RS-422 is a 4-wire point-to-point full-duplex interface allowing much longer cable runs than are possible with RS-232. The differential transmitter and receiver twisted pairs offer a high degree of noise immunity. RS-422 usually requires the lines be terminated at both ends. This termination can be accomplished either on the cable or by installing resisters on the board in locations reserved for them. The method for determining the correct resistor values is beyond the scope of this document but it is recommended that trial values of 100 ohms be used in all three locations at the receiver end. The following illustration shows the correct mode jumpering, driver IC installation, I/O connector pin definitions, and termination resistor locations for each of the channels when used in RS-422 mode.

COM1 - RS-422



U4 - Not Installed
U9 - Installed
U5 - Installed

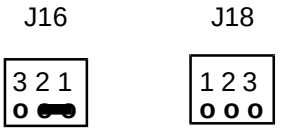




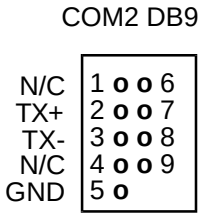
RS-422 NOTE : When used in RS-422 mode, the transmitter must be enabled by setting the RTS bit in the Modem Control Register (Bit1).

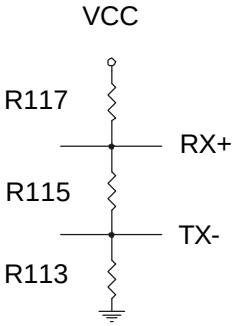
*** Important Note: All serial termination components are surface mount 0805 packages on the bottom side of the board. These should only be installed by surface mount qualified individuals.**

COM2 - RS-422



U6 - Not Installed
U10 - Installed
U7 - Installed





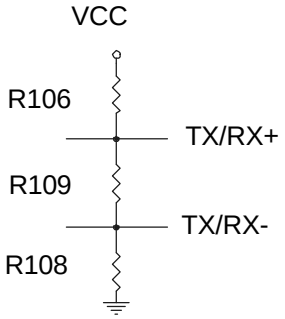
RS-422 NOTE: When used in RS-422 mode, the transmitter must be enabled by setting the RTS bit in the Modem Control Register (Bit).

2.9.2 RS-485 Mode Configuration

The RS-485 Multi-drop interface is supported on both channels with the installation of the optional "Chip Kit", WinSystems' part number CK-75176-2. A single kit is sufficient to configure both channels for RS-485. RS-485 is a 2-wire multi-drop interface where only one station at a time talks (transmits) while all others listen (receive). RS-485 usually requires the twisted pair be terminated at each end of the run. The required termination values are dependent upon a number of factors including: line impedance, line length, etc. A good trial value is 100 ohms in all three resistor locations. The following illustrations show the correct jumpering, driver IC installation, I/O connector pinout, and termination resistor locations for each of the channels when used in RS-485 mode.

COM1 - RS-485

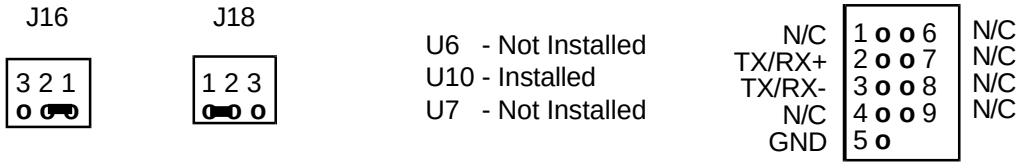


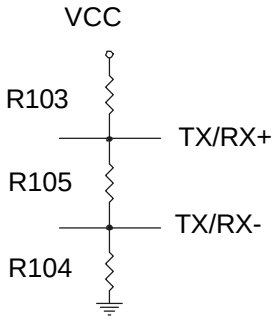


RS-485 NOTE : Because RS-485 uses a single twisted-pair, all transmitters are connected in parallel. Only one station at a time may transmit or have its transmitter enabled. The transmitter Enable/Disable is controlled in software using bit 1 in the Modem Control Register (RTS). When RTS is set, the transmitter is enabled, and when cleared (the normal state) the transmitter is disabled and the receiver is enabled. Note that it is necessary to allow some minimal settling time after enabling the transmitter before transmitting the first character. Likewise, following a transmission, it is necessary to be sure that all characters have been completely shifted out of the UART (Check Bit 6 in the Line Status Register) before disabling the transmitter to avoid chopping off the last character.

Important Note: All serial termination components are surface mount 0805 packages on the bottom of the board. These should only be installed by surface mount qualified individuals.

COM2 - RS-485





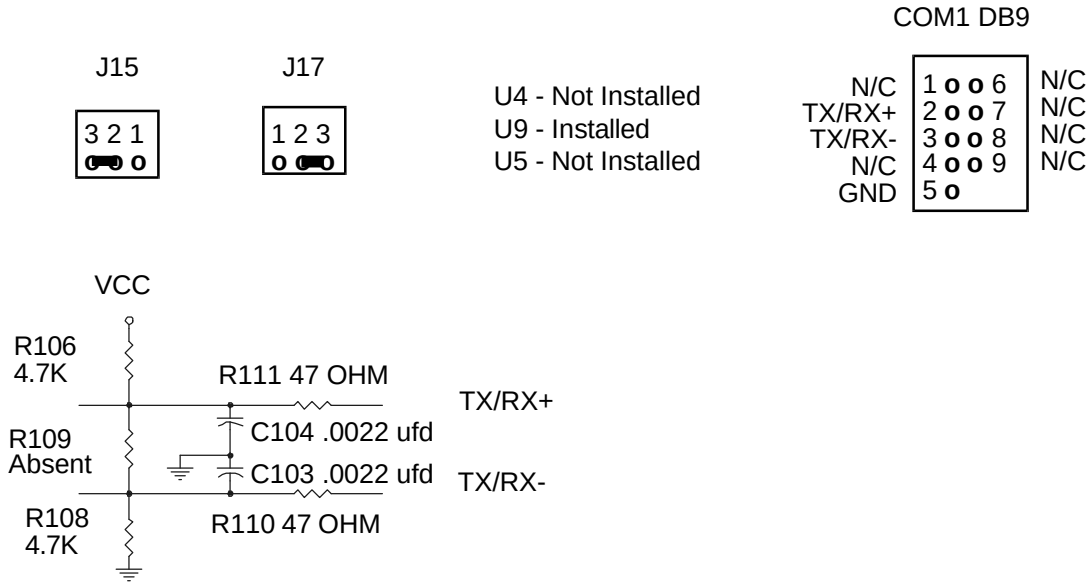
RS-485 NOTE : Because RS-485 uses a single twisted-pair, all transmitters are connected in parallel. Only one station at a time may transmit or have its transmitter enabled. The transmitter Enable/Disable is controlled in software using bit 1 in the Modem Control Register (RTS). When RTS is set, the transmitter is enabled, and when cleared (the normal state) the transmitter is disabled and the receiver is enabled. Note that it is necessary to allow some minimal settling time after enabling the transmitter before transmitting the first character. Likewise, following a transmission, it is necessary to be sure that all characters have been completely shifted out of the UART (Check Bit 6 in the Line Status Register) before disabling the transmitter to avoid chopping off the last character.

Important Note : All serial termination components are surface mount 0805 packages. These should only be installed by surface mount qualified individuals.

2.9.3 SAE J1708 Configuration

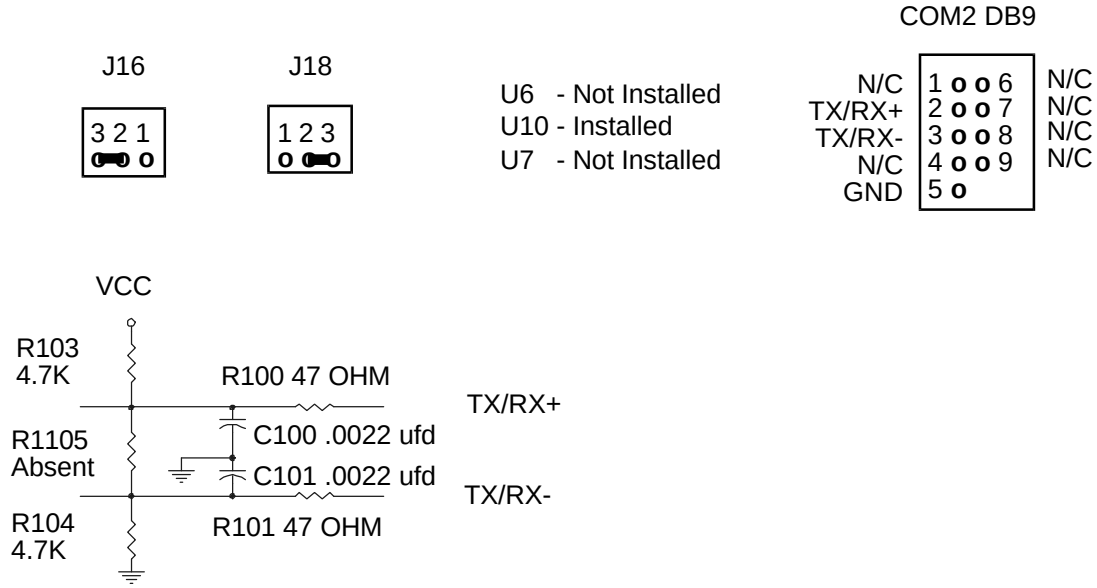
The Society of Automotive Engineers (SAE) J1708 interface is a variation of the RS-485 interface which is used for "Serial Data Communications between Microcomputer Systems in Heavy Duty Vehicle Applications". It is beyond the scope of this document to go into detail on the J1708 specification. The EBC-BX may be user configured for J1708 by the addition of the CK-75176-2 "Chip Kit". One "Chip Kit" is sufficient to configure both channels for J1708. The illustrations that follow show the correct jumpering, driver IC installation, I/O connector pin definitions, and the termination network details for each of the channels when used in J1708 mode.

COM1 - J1708



Important Note : All serial termination components are surface mount 0805 packages on the bottom of the board. These should only be installed by surface mount qualified individuals.

COM2 - J1708



2.10 Parallel Printer Port

The EBC-BX supports a fully bi-directional parallel printer port capable of EPP and ECP operations. The PnP parallel port is mapped by default at 378H and is terminated at the Multi-I/O connectors at J3. Other I/O and interrupt mapping are available using the Award BIOS setup menu options. The pin definitions for the parallel port DB25 connector when using the CBL-247-1 cable are shown below:

STROBE	1 o o 14	AUTOFD
PD0	2 o o 15	ERROR
PD1	3 o o 16	INIT
PD2	4 o o 17	SLIN
PD3	5 o o 18	GND
PD4	6 o o 19	GND
PD5	7 o o 20	GND
PD6	8 o o 21	GND
PD7	9 o o 22	GND
ACK	10 o o 23	GND
BUSY	11 o o 24	GND
PE	12 o o 25	GND
SLCT	13 o	

2.11 Speaker/Sound Interface

The EBC-BX utilizes a high-impedance piezo type device for audio output. BIOS beep codes, error signaling, or user-defined tones can be presented via this device.

2.12 PC/104 Bus Interface

The EBC-BX supports I/O expansion through the standard PC/104 connectors at J20 and J23. The EBC-BX supports both 8-bit and 16-bit PC/104 modules. The PC/104 connector pin definitions are provided on the following page for reference purposes.

J23

GND	B1	o o	A1	IOCHK
RESET	B2	o o	A2	BD7
+5V	B3	o o	A3	BD6
IRQ9	B4	o o	A4	BD5
-5V	B5	o o	A5	BD4
DRQ2	B6	o o	A6	BD3
-12V	B7	o o	A7	BD2
0WS	B8	o o	A8	BD1
+12V	B9	o o	A9	BD0
GND	B10	o o	A10	IOCHRDY
MEMW	B11	o o	A11	AEN
MEMR	B12	o o	A12	SA19
IOW	B13	o o	A13	SA18
IOR	B14	o o	A14	SA17
DACK3	B15	o o	A15	SA16
DRQ3	B16	o o	A16	SA15
DACK1	B17	o o	A17	SA14
DRQ1	B18	o o	A18	SA13
REFRESH	B19	o o	A19	SA12
SYSCLK	B20	o o	A20	SA11
IRQ7	B21	o o	A21	SA10
IRQ6	B22	o o	A22	SA9
IRQ5	B23	o o	A23	SA8
IRQ4	B24	o o	A24	SA7
IRQ3	B25	o o	A25	SA6
DACK2	B26	o o	A26	SA5
TC	B27	o o	A27	SA4
BALE	B28	o o	A28	SA3
+5V	B29	o o	A29	SA2
OSC	B30	o o	A30	SA1
GND	B31	o o	A31	SA0
GND	B32	o o	A32	GND

J20

GND	C0	o o	D0	GND
SBHE	C1	o o	D1	MEMCS16
LA23	C2	o o	D2	IOCS16
LA22	C3	o o	D3	IRQ10
LA21	C4	o o	D4	IRQ11
LA20	C5	o o	D5	IRQ12
LA19	C6	o o	D6	IRQ15
LA18	C7	o o	D7	IRQ14
LA17	C8	o o	D8	DACK0
MEMR	C9	o o	D9	DRQ0
MEMW	C10	o o	D10	DACK5
SD8	C11	o o	D11	DRQ5
SD9	C12	o o	D12	DACK6
SD10	C13	o o	D13	DRQ6
SD11	C14	o o	D14	DACK7
SD12	C15	o o	D15	DRQ7
SD13	C16	o o	D16	VCC
SD14	C17	o o	D17	MASTER
SD15	C18	o o	D18	GND
KEY	C19	o o	D19	GND

2.13 PC/104Plus Bus Interface

The EBC-BX supports I/O expansion through the standard PC/104Plus connector at J22. The PC/104Plus Bus pin definitions are provided on the following page for reference purposes.

J22				
Pin	A	B	C	D
1	GND/5.0 KEY	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD06
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3.V	C/BE3*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY

2.14 Floppy Disk Interface

The EBC-BX supports up to 2 standard 3 1/2" or 5 1/4" PC compatible floppy disk drives. The drives are connected via the I/O connector at J10. Note that the interconnect cable to the drives is a standard floppy I/O cable used on desktop PCs. The cable must have the twisted section prior to the drive A position. The pin definitions for the J10 connector are shown on the following page:

J10

GND	1	2		RPM/LC
GND	3	4		N/C
GND	5	6		N/C
GND	7	8		INDEX
GND	9	10		MTR0
GND	11	12		DRV1
GND	13	14		DRV0
GND	15	16		MTR1
GND	17	18		DIR
GND	19	20		STEP
GND	21	22		WDATA
GND	23	24		WGATE
GND	25	26		TRK0
GND	27	28		WPRT
GND	29	30		RDATA
GND	31	32		HDSEL
GND	33	34		DSKCHG

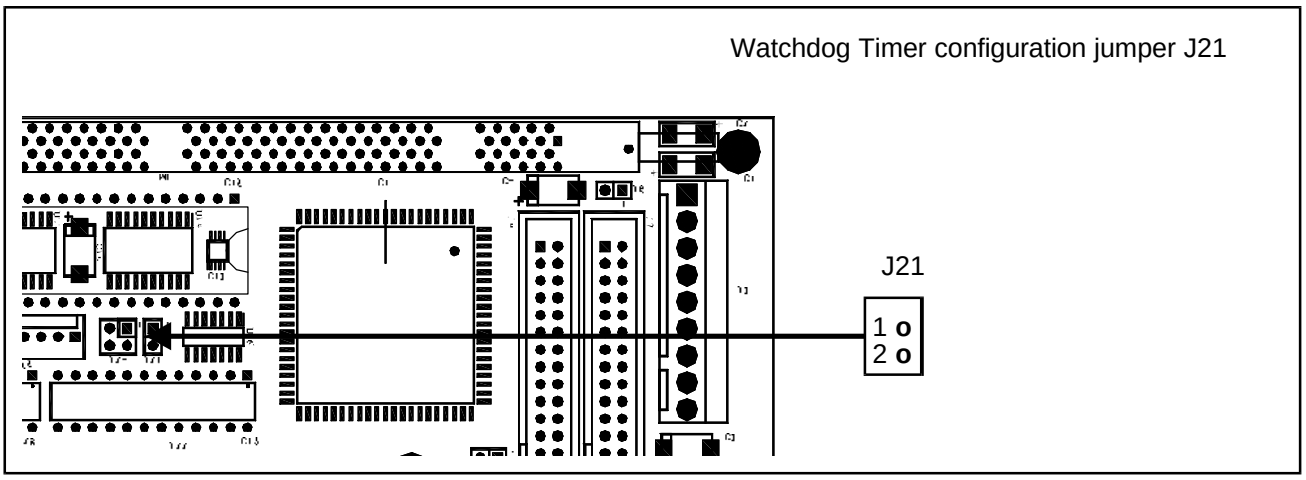
2.15 IDE Hard Disk Interface

The EBC-BX supports standard IDE fixed disks through the I/O connectors at J5 (primary) and J8 (secondary). The EBC-BX supports multiple PIO modes as well as Ultra-DMA (UDMA)33 and UDMA 66 drives when used with an UDMA 80-pin cable (WinSystems P/N CBL-126-10). A red activity LED is present at D3 and D2 for the primary and secondary hard drive controllers respectively. The pin definitions for J5 and J8 are shown here:

J5 and J8

RST	1	2		GND
D7	3	4		D8
D6	5	6		D9
D5	7	8		D10
D4	9	10		D11
D3	11	12		D12
D2	13	14		D13
D1	15	16		D14
D0	17	18		D15
LED	19	20		N/C
DRQ	21	22		GND
IOW	23	24		GND
IOR	25	26		GND
RDY	27	28		NC
DACK	29	30		GND
IRQ	31	32		NC
A1	33	34		NC
A0	35	36		A2
CS1	37	38		CS3
VCC	39	40		GND

2.16 Watchdog Timer Configuration



The EBC-BX board features a power-on voltage detect, and power-down/power brownout reset circuit to protect memory and I/O from faulty CPU operation during periods of illegal voltage levels. This supervisor circuitry also features a watchdog timer which can be used to guard against software lock ups. An internal timer with a period of 1.5 or 150 seconds will, when enabled, reset the CPU if the watchdog has not been serviced within the allotted time. The watchdog timer powers-up disabled and must be enabled in software before timing will begin. Enabling is accomplished by writing a 1 to I/O port 1EEH. Writing a 0 to I/O port 1EEH will disable the watchdog. After enabling, petting may be accomplished by writing any value to I/O port 1EFH at least every 1.5 if J21 is not jumpered or at least every 150 seconds if J21 is jumpered, or a reset will occur. This mode of operation can be used with the BIOS or DOS provided that the watchdog is disabled before making any extensive BIOS or DOS calls, especially video or disk I/O calls which could exceed the time seconds allowed when the 1.5 second mode is used.

2.17 Status LED

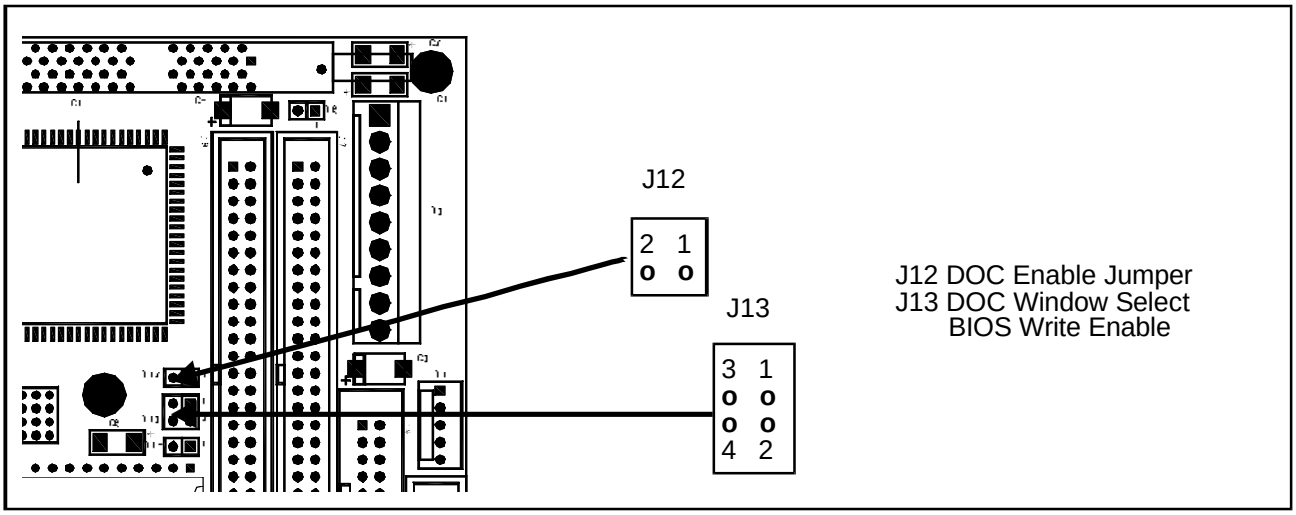
A green LED is populated on the board at D1 which can be used for any application specific purpose. The LED can be turned on in software by writing a 1 to I/O port 1EDH. The LED can be turned off by writing a 0 to 1EDH.

2.18 Battery Select Control

An onboard 350mAH nominal capacity, lithium battery is provided for the CMOS Clock/Calendar. A master battery enable jumper is provided at J27. When J27 is jumpered pins 2-3, battery power is supplied to the Clock/Calendar. When J27 is jumpered pins 1-2, the battery is totally disconnected and no current will be drawn from it. Battery life is highly dependent upon duty cycle as there is no current drawn from the battery when +5 volts is applied to the board. Both storage and operational temperatures play a prominent factor in battery life. High temperatures will shorten battery life significantly. J27 must be jumpered 1-2 if a battery is not installed.

2.19 DiskOnChip Configuration

The DiskOnChip can be enabled by jumpering J12 and J13 as shown below.



Note : J13 pins 1-2 control BIOS write, and must be jumpered at all times for proper Plug-N-Play operation.

J12

2 1

DiskOnChip Enabled

J13

2 1

o o

4 3

DOC at D800:0000

J12

2 1

o o

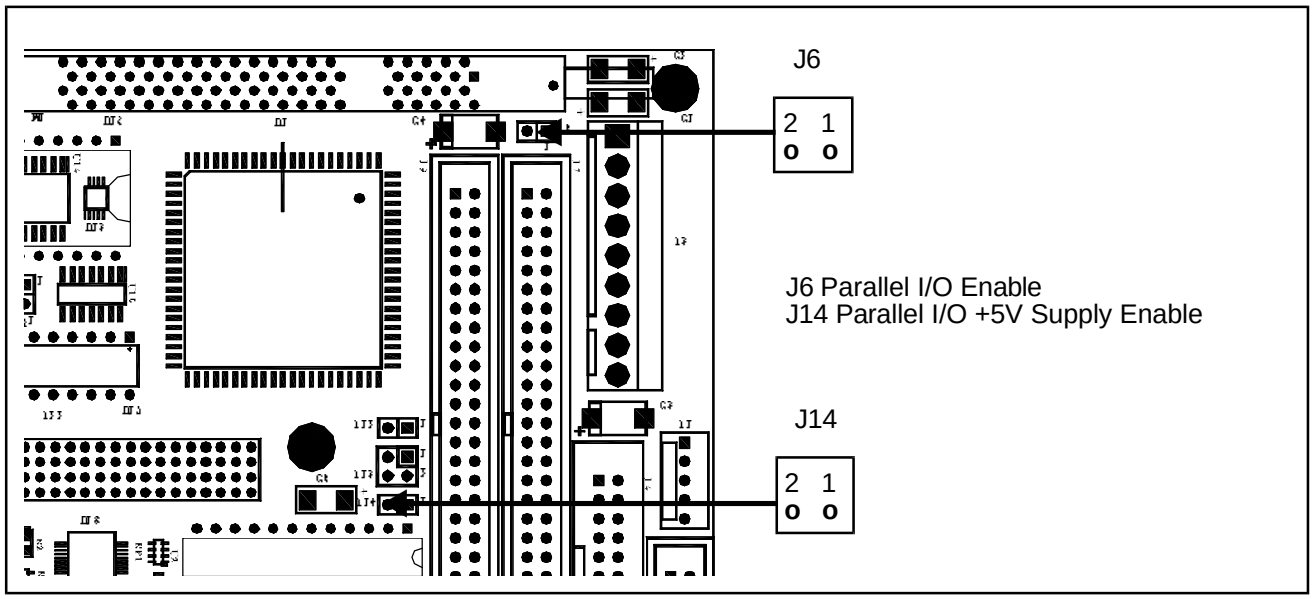
DiskOnChip Disabled

J13

2 1

4 3

DOC at D000:0000



2.20 Parallel I/O

The EBC-BX utilizes the WinSystems WS16C48 ASIC high-density I/O chip mapped at a base address of 120H. The first 24 lines are capable of fully latched event sensing with sense polarity being software programmable. Two, 50-pin connectors allow for easy mating with industry standard I/O racks. The pinout for the two connectors are shown on the next page.

2.20.1 Parallel I/O Enable

The parallel features of the EBC-BX can be enabled or disabled using the jumper block at J6. When J6 is jumpered the parallel I/O is enabled at I/O address 120H. When J6 is open the 16 addresses starting at I/O address 120H are free for use by other devices.

2.20.2 Parallel I/O VCC Enable

The I/O connectors can provide +5 volts to an I/O rack or for miscellaneous purposes by jumpering J14. When J14 is jumpered +5 volts is provided at pin 49 of both J7 and J9. It the user's responsibility to limit current to a safe value (less than 400mA) to avoid damaging the CPU board.

2.20.3 Parallel I/O Connectors

The 48 lines of parallel I/O are terminated through two 50-pin connectors at J7 and J9. The J7 connector handles I/O ports 0-2 while J9 handles ports 3-5. The pin definitions for J7 and J9 are shown on the following page.

J7

Port 2 Bit 7	1 o o 2	GND
Port 2 Bit 6	3 o o 4	GND
Port 2 Bit 5	5 o o 6	GND
Port 2 Bit 4	7 o o 8	GND
Port 2 Bit 3	9 o o 10	GND
Port 2 Bit 2	11 o o 12	GND
Port 2 Bit 1	13 o o 14	GND
Port 2 Bit 0	15 o o 16	GND
Port 1 Bit 7	17 o o 18	GND
Port 1 Bit 6	19 o o 20	GND
Port 1 Bit 5	21 o o 22	GND
Port 1 Bit 4	23 o o 24	GND
Port 1 Bit 3	25 o o 26	GND
Port 1 Bit 2	27 o o 28	GND
Port 1 Bit 1	29 o o 30	GND
Port 1 Bit 0	31 o o 32	GND
Port 0 Bit 7	33 o o 34	GND
Port 0 Bit 6	35 o o 36	GND
Port 0 Bit 5	37 o o 38	GND
Port 0 Bit 4	39 o o 40	GND
Port 0 Bit 3	41 o o 42	GND
Port 0 Bit 2	43 o o 44	GND
Port 0 Bit 1	45 o o 46	GND
Port 0 Bit 0	47 o o 48	GND
+5V	49 o o 50	GND

J9

Port 5 Bit 7	1 o o 2	GND
Port 5 Bit 6	3 o o 4	GND
Port 5 Bit 5	5 o o 6	GND
Port 5 Bit 4	7 o o 8	GND
Port 5 Bit 3	9 o o 10	GND
Port 5 Bit 2	11 o o 12	GND
Port 5 Bit 1	13 o o 14	GND
Port 5 Bit 0	15 o o 16	GND
Port 4 Bit 7	17 o o 18	GND
Port 4 Bit 6	19 o o 20	GND
Port 4 Bit 5	21 o o 22	GND
Port 4 Bit 4	23 o o 24	GND
Port 4 Bit 3	25 o o 26	GND
Port 4 Bit 2	27 o o 28	GND
Port 4 Bit 1	29 o o 30	GND
Port 4 Bit 0	31 o o 32	GND
Port 3 Bit 7	33 o o 34	GND
Port 3 Bit 6	35 o o 36	GND
Port 3 Bit 5	37 o o 38	GND
Port 3 Bit 4	39 o o 40	GND
Port 3 Bit 3	41 o o 42	GND
Port 3 Bit 2	43 o o 44	GND
Port 3 Bit 1	45 o o 46	GND
Port 3 Bit 0	47 o o 48	GND
+5V	49 o o 50	GND

2.20.4 WS16C48 Register Definitions

The EBC-BX uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 17 unique registers within the WS16C48. The following table summarizes the registers and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	N/A	Pol_0	Enab_0	Int_ID0
09H	N/A	Pol_1	Enab_1	Int_ID1
0AH	N/A	Pol_2	Enab_2	Int_ID2

Register Details

Port 0-5 I/O - Each I/O bit in each of the 6 ports can be individually programmed for input or output. Writing a '0' to a bit position causes the corresponding output pin to go to a High-Impedance state (pulled high by external 10K ohm resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a '0' in the register. Writing a '1' to a bit position causes the output pin to sink current (up to 12mA), effectively pulling it low.

INT_PENDING - This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower 3 bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK - This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A '1' written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0-POL2 - These registers are accessible when page 1 is selected. They allow interrupt polarity selection on a port-by-port and bit-by-bit basis. Writing a '1' to a bit position selects the rising edge detection interrupts while writing a '0' to a bit position selects falling edge detection interrupts.

ENAB0-ENAB2 - These registers are accessible when page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a '1' the edge detection interrupt is enabled for the corresponding port and bit. When cleared to a '0', the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and reenabling the pending interrupt.

INT_ID0 - INT_ID2 - These registers are accessible when page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a '1' indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

2.21 VGA Configuration

The EBC-BX uses a fourth generation CRT/Flat panel Super VGA controller. It supports standard VGA output as well as a variety of Flat Panel Displays using optional Flat Panel Adapter (FPA) kits. The video on the EBC-BX uses the Asiliant 69000 series VGA controllers. The Asiliant controller supports standard and super-VGA as well as Color and Monochrome panels with 8, 9, 12, 15, 16, 18,24 and 36-bit interfaces.

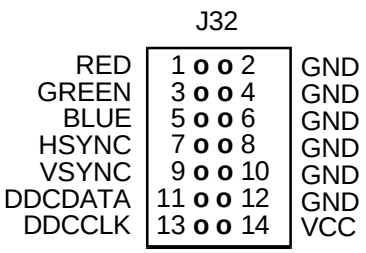
WinSystems provides flat panel support through a series of Flat Panel Adapter (FPA) kits. Contact your WinSystems Applications Engineer for the most current list of available FPA's and supported panels.Details regarding interfacing to specific Flat Panels is not provided in this manual but should be referenced in the documentation accompanying the FPA kit. Attempted connection to any flat panel not directly supported by a WinSystems FPA module is at the user's risk and extreme care should be exercised to avoid damaging or destroying the panel.

HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring or handling the inverter output. To avoid danger of shock and to avoid damaging fragile and expensive panels, make all connection changes with power removed.

Note: J26 must be jumpered 1-2 for Sharp-type panels, and 2-3 for NEC-type panels.

2.21.1 CRT Output Connection

Video output to a standard VGA monitor is made via the connector at J32. An adapter cable part number CBL-234-1 is available from WinSystems to adapt from J32 to the standard DB15 VGA connector. The pin definitions for the J32 connector are shown here :



2.21.2 Panel Backlight Connection

Panel Backlight connection is made via the connector at J25. The pinout for J25 is shown here for reference.

J25

+12	o 1	
+12	o 2	
GND	o 3	
GND	o 4	
ENBKL	o 5	
VCC	o 6	
VCC	o 7	

2.21.3 Flat Panel Output Connection

Connection to all flat panels is made via the two 50-pin connectors at J31 and J32. These connectors are cabled to the appropriate FPA (Flat Panel Adapter) module which then breaks out the necessary cabling for attachment to the panel itself. The FPA module also supplies any special controls that may be needed for the panel. Refer to the FPA documentation for specific hookup instructions. The pin definitions for J30 and J33 are shown here :

J30

FP12	1 o	o 2		GND
FP13	3 o	o 4		GND
FP14	5 o	o 6		GND
FP15	7 o	o 8		GND
FP16	9 o	o 10		GND
FP17	11 o	o 12		GND
FP18	13 o	o 14		GND
FP19	15 o	o 16		GND
FP20	17 o	o 18		GND
FP21	19 o	o 20		GND
FP22	21 o	o 22		GND
FP23	23 o	o 24		GND
FP24	25 o	o 26		GND
FP25	27 o	o 28		GND
FP26	29 o	o 30		GND
FP27	31 o	o 32		GND
FP28	33 o	o 34		GND
FP29	35 o	o 36		GND
FP30	37 o	o 38		GND
FP31	39 o	o 40		GND
FP32	41 o	o 42		GND
FP33	43 o	o 44		GND
FP34	45 o	o 46		GND
FP35	47 o	o 48		GND
SWVCC	49 o	o 50		SWVCC

J33

SW0	1 o	o 2		SW1
SW2	3 o	o 4		SW3
FPO	5 o	o 6		GND
FP1	7 o	o 8		GND
FP2	9 o	o 10		GND
FP3	11 o	o 12		GND
FP4	13 o	o 14		GND
FP5	15 o	o 16		GND
FP6	17 o	o 18		GND
FP7	19 o	o 20		GND
FP8	21 o	o 22		GND
FP9	23 o	o 24		GND
FP10	25 o	o 26		GND
FP11	27 o	o 28		GND
PCSHCLK	29 o	o 30		GND
PCFLM	31 o	o 32		GND
PCLP	33 o	o 34		GND
PCM	35 o	o 36		GND
PHSYNC	37 o	o 38		GND
PVSYNC	39 o	o 40		GND
ENVCC	41 o	o 42		GND
ENBKL	43 o	o 44		GND
ENVEE	45 o	o 46		-12V
+12V	47 o	o 48		+12V
SWVCC	49 o	o 50		SWVCC

2.21.4 Video Mode Table

The EBC-BX video section supports a number of standard and extended VGA modes. The following table extracted from the Asiliant 69000 databook shows the video modes supported.

Resolution	Color depth (bpp)	Refresh Rates
640 x 480	8	60, 75, 85
640 x 480	16	60, 75, 85
640 x 480	24	60, 75, 85
800 x 600	8	60, 75, 85
800 x 600	16	60, 75, 85
800 x 600	24	60, 75, 85
1024 x 768	8	60, 75, 85
1024 x 768	16	60, 75, 85
1280 x 1024	8	60

2.22 Ethernet Controller

The 82559 is part of Intel's second generation family of fully integrated 10BASE-T/100BASE-TX LAN solutions. The 82559 consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution.

The 82559 is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities which enables it to perform high-speed data transfers over the PCI bus. The 82559 bus master capabilities enable the component to process high-level commands and perform multiple operations offloading communication tasks from the system CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns, allowing the 82559 to transmit data with minimum interframe spacing (IFS).

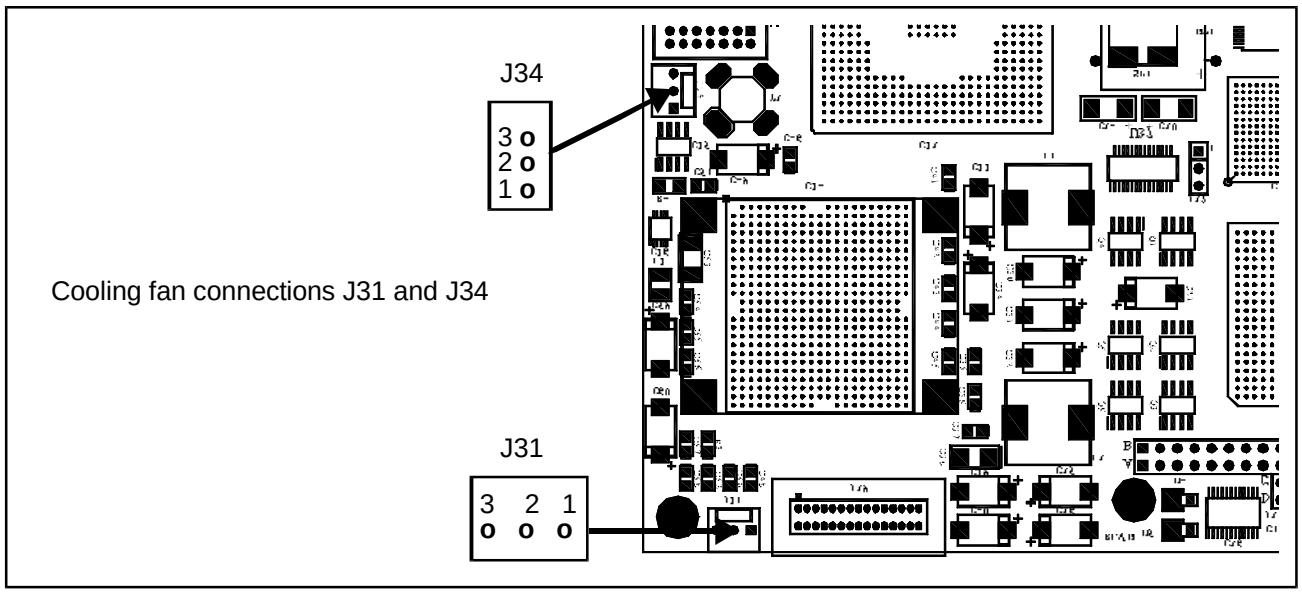
The 82559 can operate in either full duplex or half duplex mode. In full duplex mode the 82559 adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The 82559 includes a simple PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex, and flow control. The 82559 also includes an interface to a serial (4-pin) EEPROM. The EEPROM provides power-on initialization for hardware and software configuration parameters. The 82559 is also 100% PnP compatible and is configured through this interface. Ethernet connection to the EBC-BX is made through the connector at J28.

There are Ethernet status LED's at D6, D7, and D8. The color and function of each LED is listed below :

D6 = Ethernet 100BASE-TX (Red)
D7 = Ethernet activity LED (Green)
D8 = Ethernet link LED (Yellow)

For ethernet drivers go to:
http://developer.intel.com/design/network/drivers/



J31 and J34

GND	1 o
FAN POWER	2 o
FAN TACH	3 o

2.23 Fan Power Connector

The EBC-BX has a connector located at J31 to supply power to the processor cooling fan. The pin definitions are shown here for reference. There is also a connector at J34 for use with an auxiliary system cooling fan. The pin definitions for these connectors is shown here :

Both J31 and J34 provide +5V nominal at 250mA max.

2.24 Multi I/O Connector

The I/O to the primary serial channels, the printer port, and keyboard are all terminated via the connector at J2. An adapter cable, part number CBL-247-1, is available from WinSystems to adapt to the conventional I/O connectors. The pin definitions for J2 are shown here

J2

COM1 - DCD	1	2	COM1 - DSR
COM1 - RXD	3	4	COM1 - RTS
COM1 - TXD	5	6	COM1 - CTS
COM1 - DTR	7	8	COM1 - RI
COM1 - GND	9	10	COM2 - DCD
COM2 - DSR	11	12	COM2 - RSX
COM2 - RTS	13	14	COM2 - TXD
COM2 - CTS	15	16	COM2 - DTR
COM2 - RI	17	18	COM2 - GND
LPT - STROBE	19	20	LPT - AUTOFD
LPT - PD0	21	22	LPT - ERROR
LPT - PD1	23	24	LPT - INIT
LPT - PD2	25	26	LPT - SLCTIN
LPT - PD3	27	28	LPT - GND
LPT - PD4	29	30	LPT - GND
LPT - PD5	31	32	LPT - GND
LPT - PD6	33	34	LPT - GND
LPT - PD7	35	36	LPT - GND
LPT - ACK	37	38	LPT - GND
LPT - BUSY	39	40	LPT - GND
LPT - PE	41	42	LPT - GND
LPT - SLCT	43	44	KEYBD - GND
KEYBD - GND	45	46	KEYBD - GND
KEYBD - KDATA	47	48	KEYBD - CLK
KEYBD - +5V	49	50	KEYBD - +5V

2.25 USB Connector

A USB cable may be attached via the connector at J11. An adapter cable, CBL-249-1 is available from WinSystems to adapt to a conventional USB port. The pinout for J11 is shown here.

J11

1	USBV0
2	D0-
3	D0+
4	USBG0

2.26 Jumper/Connector Summary

Connector/ Jumper	Description	Page Reference
J1	Mouse connector	2-3
J2	Multi-I/O connector	2-25
J3	Power connector	2-3
J4	COM3, COM4 connector	2-7
J5	Primary IDE connector	2-15
J6	Parallel I/O enable jumper	2-18
J7	Parallel I/O connector	2-18
J8	Secondary IDE connector	2-15
J9	Parallel I/O connector	2-18
J10	Floppy disk connector	2-14
J11	USB connector	2-25
J12	DOC Enable jumper	2-17
J13	DOC configuration jumper	2-17
J14	Parallel I/O VCC select jumper	2-18
J15	COM1 RS-422/RS-485 configuration jumper	2-5
J16	COM2 RS-422/RS-485 configuration jumper	2-5
J17	COM1 RS-422/RS-485 configuration jumper	2-5
J18	COM1 RS-422/RS-485 configuration jumper	2-5
J19	IRQ routing jumper	2-2
J20	PC/104 16-bit connector	2-13
J21	Watchdog Timer configuration jumper	2-16
J22	PC/104Plus connector	2-13
J23	PC/104 8-bit connector	2-13
J24	COM3/COM4 Enable jumper	2-5
J25	Flat Panel backlight connector	2-22
J26	Flat Panel backlight type select jumper	2-21
J27	Master Battery select jumper	2-4
J28	Ethernet connector	2-23
J29	ITP Debug port	N/A
J30	Flat Panel/FPA connector	2-22
J31	CPU Fan/tachometer connector	2-24
J32	VGA CRT output connector	2-21
J33	Flat Panel/FPA connector	2-22
J34	Auxiliary Fan/Tachometer connector	2-24

3 Award BIOS Configuration

3.1 General Information

The EBC-BX comes equipped with a standard Award BIOS with Setup in ROM that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains Setup information when power is turned off.

3.2 Entering Setup

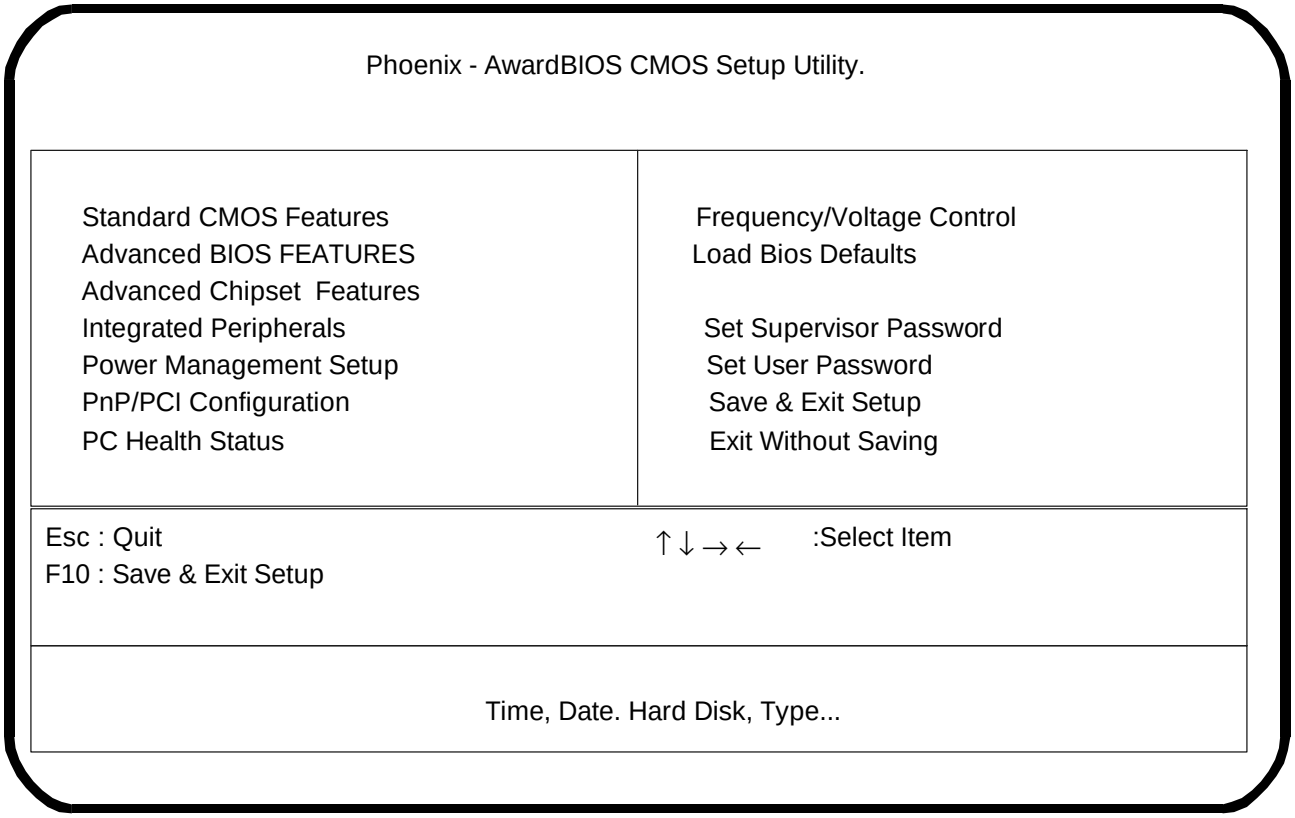
To enter setup, power on the computer and press the DEL key immediately after the message " Press DEL to Enter Setup" appears on the lower left of the screen. If the message disappears before you respond and you still wish to enter setup, restart the system by turning it OFF and then ON or by pressing the RESET button, if so equipped, or by pressing the CTRL, ALT and DEL key simultaneously. Alternately, under certain error conditions of incorrect setup the message:

"Press F1 to continue or DEL to Enter Setup"

may appear. To Enter Setup at that time, press the DEL key. To attempt to continue, ignoring the error condition, press the F1 key.

3.3 Setup Main Menu

The main menu screen is displayed on the following page. Each of the options will be discussed in this section. Use the arrow keys to highlight the desired selection and press ENTER to enter the submenu or to execute the function selected.



3.4 Standard CMOS Features

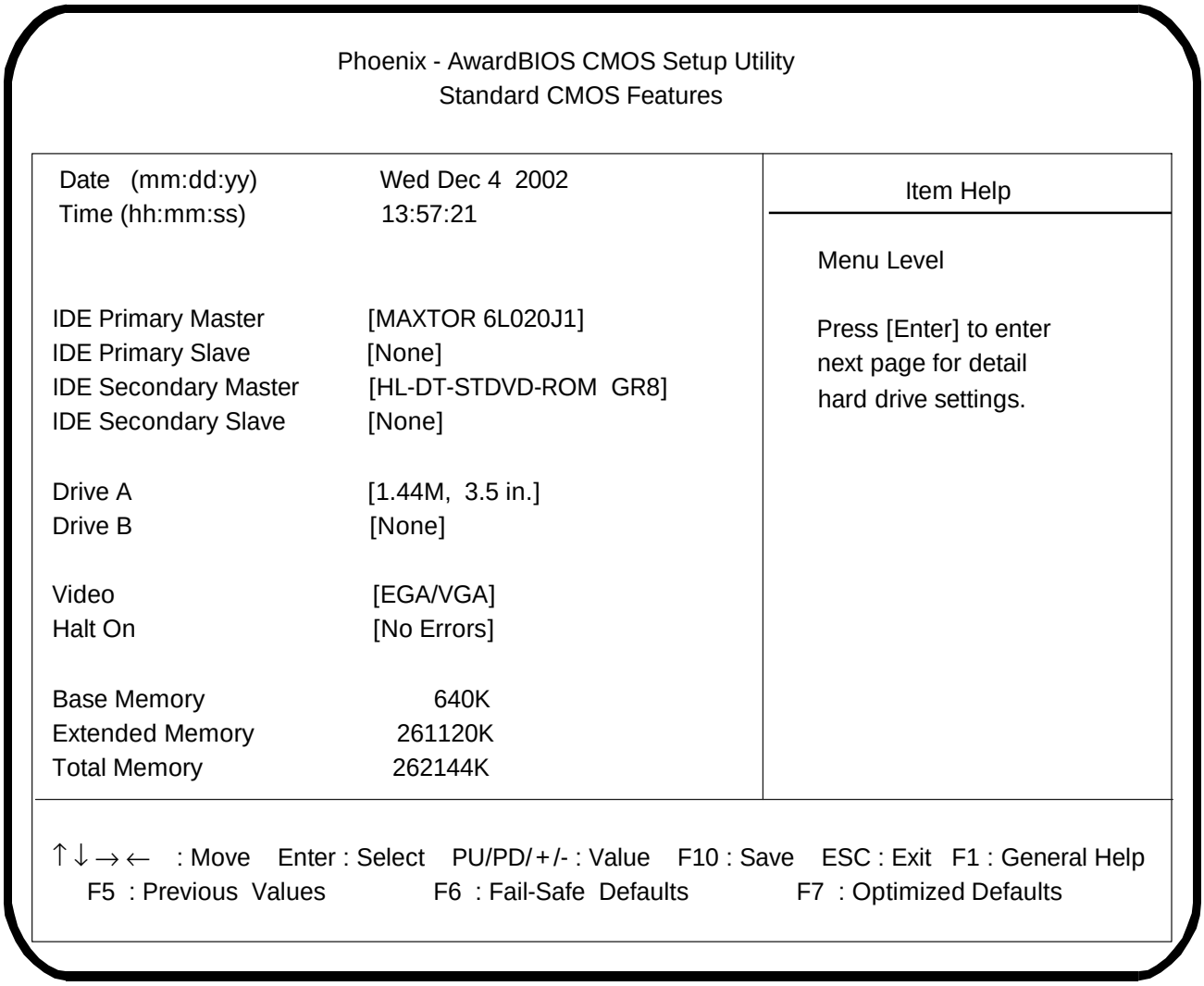
The items in the Standard CMOS Setup menu are divided into several categories. Each category may include one or more setup items. Use the arrow keys to highlight the item and then use the PgUp, PgDn, +.-. keys to select the desired value for the item.

Date

The date format is <day>,< date>,< month>, <year>
Day = The day, from Sun to Sat, determined by the BIOS and is display only
Date = the date, from 1 to 31 (or the maximum for the current month)
Month = the month, JAN through DEC
Year = The year, from 1900 to 2099

Time

The time is hour, minute, second. The time is calculated on the 24-hour, military-time clock such that 1:00PM is 13:00:00.



IDE Primary Master

Pressing [Enter] brings up a sub-menu screen of choices regarding the Primary fixed disk.

IDE HDD Auto-Detection

Pressing [Enter] when this selection is highlighted will cause the system to interrogate the attached hard disk and choose the parameters automatically

IDE Primary Master

Pressing [Enter], when this item is highlighted, allows for selection of how parameters for the hard drive will be determined. The choices are :

None - No Hard Drive is installed
Auto - Automatically detect the hard disk parameters at power-up (Recommended Setting)
Manual - Use the parameters entered manually by the user

Access Mode

Pressing [Enter] when this option is highlighted allows selection of the hard disk access mode. The choices are :

CHS - The drive will be accessed using direct Cylinder, Head, Sector mode. No translation will take place. This can only be used when the "manual" mode is selected above.
LBA - This selection allows the native mode of the drive to be translated to Cylinder, head, and sector counts that are compatible with allowable BIOS parameter restrictions. Drives up to 120GB can be used with this mode.
LARGE - This is another translation scheme that is not commonly used but may be required for some O/Ss.
AUTO - This mode chooses the appropriate translation mode (usually LBA) for the actual drive attached. (Recommended Setting)

Drive Parameters/Size

The drive size in MB is displayed for all modes. When manual and CHS modes are selected the user may enter values into these fields :

Cylinder - 0 to 65535
Head - 0 to 255
Precomp - 0 to 65535
Landing Zone - 0 to 65535
Sector - 0 to 255

IDE Primary Slave

This selection is identical to the IDE Primary Master shown above.

IDE Secondary Master

This selection is identical to the IDE Primary Master shown above.

IDE Secondary Slave

This selection is identical to the IDE Primary Master shown above.

Drive A type/Drive B type

This category identifies the type of floppy drives attached as Drive A: or Drive B:. The choices are as follows :

NONE
360K, 5.25 in.
1.2M, 5.25 in.
720K, 3.5 in
1.44M, 3.5 in.
2.88M 3.5 in.

Video

This category specifies the type of video adapter used for the primary system monitor that matches your video display board and monitor. The available choices are:

EGA/VGA
CGA40
CGA80
MONO

The EBC-BX has built-in VGA support so EGA/VGA should be selected.

Error Halt

This category determines whether the system will halt if a nonfatal error is detected during the power-up self test. The choices are:

No Errors : The system will not be stopped for any error that may be detected.

All Errors : Whenever the BIOS detects a nonfatal error, the system will be stopped and a prompt will appear.

All, but Keyboard : The system will not stop for a keyboard error, it will stop for all other errors.

All, but diskette : The system will not stop for disk errors. All others will result in a prompt.

All but Disk/Key : All errors except diskette or keyboard will result in a halt and a prompt.

Memory

This category is display only and is determined by the BIOS POST (Power-On Self Test).

Base Memory

The POST routines in the BIOS will determine the amount of base (conventional) memory installed in the system. The value of the base memory is typically 640K for systems with a Megabyte of memory or greater.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address space.

Total Memory

The BIOS displays the total of the Base memory and the Extended memory installed in the system.
.

3.5 Advanced BIOS Features Setup

Virus Warning

This option when enabled, protects the boot sector and partition table of the hard disk against unauthorized writes through the BIOS. Any attempt to alter these areas will result in an error message and a prompt to authorize the activity.

CPU Internal Cache

This option, when enabled, provides maximum performance by caching instructions and data using the on-chip cache of the Pentium processor.

External Cache

This option, when enabled, further enhances performance by caching recently used instructions and data into fast SRAM.

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

		Item Help
Virus Warning	[Disabled]	
CPU Internal Cache	[Enabled]	Menu Level
External Cache	[Enabled]	
CPU L2 Cache ECC Checking	[Enabled]	Allows you to choose the VIRUS warning feature for IDE hard disk boot sector protection. If this function is enabled and someone attempt to write data into this area , BIOS will show a warning message on screen and alarm beep
Processor Number Feature	[Disabled]	
Quick Power On Self Test	[Enabled]	
First Boot Device	[Floppy]	
Second Boot Device	[HDD-0]	
Third Boot Device	[CD-ROM]	
Boot Other Device	[Enabled]	
Swap Floppy Drives	[Disabled]	
Boot Up Floppy Seek	[Disabled]	
Boot Up Numlock Status	[On]	
Gate A20 Options	[Fast]	
Typematic Rate Setting	[Enabled]	
Typematic Rate (Chars/Sec)	[6]	
Typematic Delay (Msec)	[250]	
Security Option	[Setup]	
OS Select for DRAM > 64MB	[Non-OS2]	
Report No FDD for WIN 95	[No]	
Video BIOS Shadow	[Enabled]	
C8000-CBFFF Shadow	[Disabled]	
CC000-CFFFF Shadow	[Disabled]	
D0000-D3FFF Shadow	[Disabled]	
D4000-D7FFF Shadow	[Disabled]	
D8000-DBFFF Shadow	[Disabled]	
DC000-DFFFF Shadow	[Disabled]	
Small Logo (EPA) Show	[Disabled]	

↑↓→← : Move Enter : Select PU/PD/+/- : Value F10 : Save ESC : Exit F1 : General Help
F5 : Previous Values F6 : Fail-Safe Defaults F7 : Optimized Defaults

CPU L2 Cache ECC Checking

This option when enable provides ECC validity checking to the L2 cache reads.

Processor Number Feature

This feature when enabled allows software to read the unique Processor Serial number present on the Intel processors.

Quick Power On Self Test (POST)

This option, when enabled, speeds up the POST during power up. The BIOS will shorten and/or skip some items during POST.

First Boot Device

This options allows for selection of the primary or “First” boot device. The BIOS will attempt to boot from this device first. The menu selection are :

Floppy
LS120
HDD-0
SCSI
CD-ROM
HDD-1
HDD-2
HDD-3
ZIP100
LAN
Disabled

Note : Not all of these devices will be available and selection of a nonexistent device may result in a drastic increase in boot time.

Second Boot Device

This option allows for selection of the secondary choice for boot media usage. The options are identical to those given above for the “First Boot Device”.

Third Boot Device

This option allows for selection of a third choice of boot media. The options are the same as for the previous two menu items.

Boot Other Device

The option when enabled allows other devices with self-contained boot firmware to become the primary boot media.

Swap Floppy Drive

This option allows for swapping of the A: and B: floppy drives without actually relocating the drives on the cable.

Boot Up Floppy Seek

During POST, when this option is enabled, the BIOS will determine if the floppy drive is 40 track or 80 tracks. If disabled, no seek test will be performed and no error can be reported.

Boot Up Numlock Status

This allows user selection of the Numlock state at boot time.

Gate A20 Option

This option allows for the selection of the source for the gate A20 signal. The choices are:

Normal - Sourced from the keyboard controller
Fast - Sourced from the Chipset

Typematic Rate Setting

This option enables or disables the typematic rate programming at boot time. Typematic is the auto-repeat function for the keyboard.

Typematic Rate

When the typematic rate setting is enabled, the typematic repeat speed is set via this option. The supported rates are :

6 characters per second
8 characters per second
10 characters per second
12 characters per second
15 characters per second
20 characters per second
24 characters per second
30 characters per second

Typematic Delay

When typematic rate setting is enabled, this option specifies the time in milliseconds before auto-repeat begins. The supported values are:

250 mS
500 mS
750 mS
1000 mS

Security Option

This option allows you to limit access to the system and setup, or just to setup. The choices are:

System - The system will not boot and access will be denied if the correct password is not entered at the prompt.

Setup - The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

NOTE: To disable security, select "Password Setting" at the Setup Main Menu and then you will be asked to enter a password. Do not type anything, just hit ENTER. Once the security is disabled, the system will boot and you can enter Setup freely.

OS Select for DRAM > 64MB

This option allows selection of an operating system for DRAM greater than 64MB.
The options are:

OS2
Non-OS2

Report No FDD for Win 95

This option, when enabled, signals Windows 95 if there is no floppy present.
The options are:

Yes
No

Shadowing Options

When shadowing for a particular address range is enabled, it instructs the BIOS to copy the BIOS located in ROM into DRAM. This shadowing from an 8-bit EPROM into fast 32-bit DRAM results in a Multi-magnitude increase in performance. The main BIOS is shadowed automatically but there are other areas that may be selected for shadowing as shown here:

Video BIOS Shadow - C000-C7FFF EGA/VGA BIOS ROM
C8000-CBFFF
CC000-CFFFF
D0000-D3FFF
D4000-D7FFF
D8000-DBFFF
DC000-DFFFF

Small Logo(EPA) Show

This option when enabled instructs the BIOS to display the EPA Energy-Star logo in the upperright corner of the screen during the POST process.

3.6 Chipset Features Setup

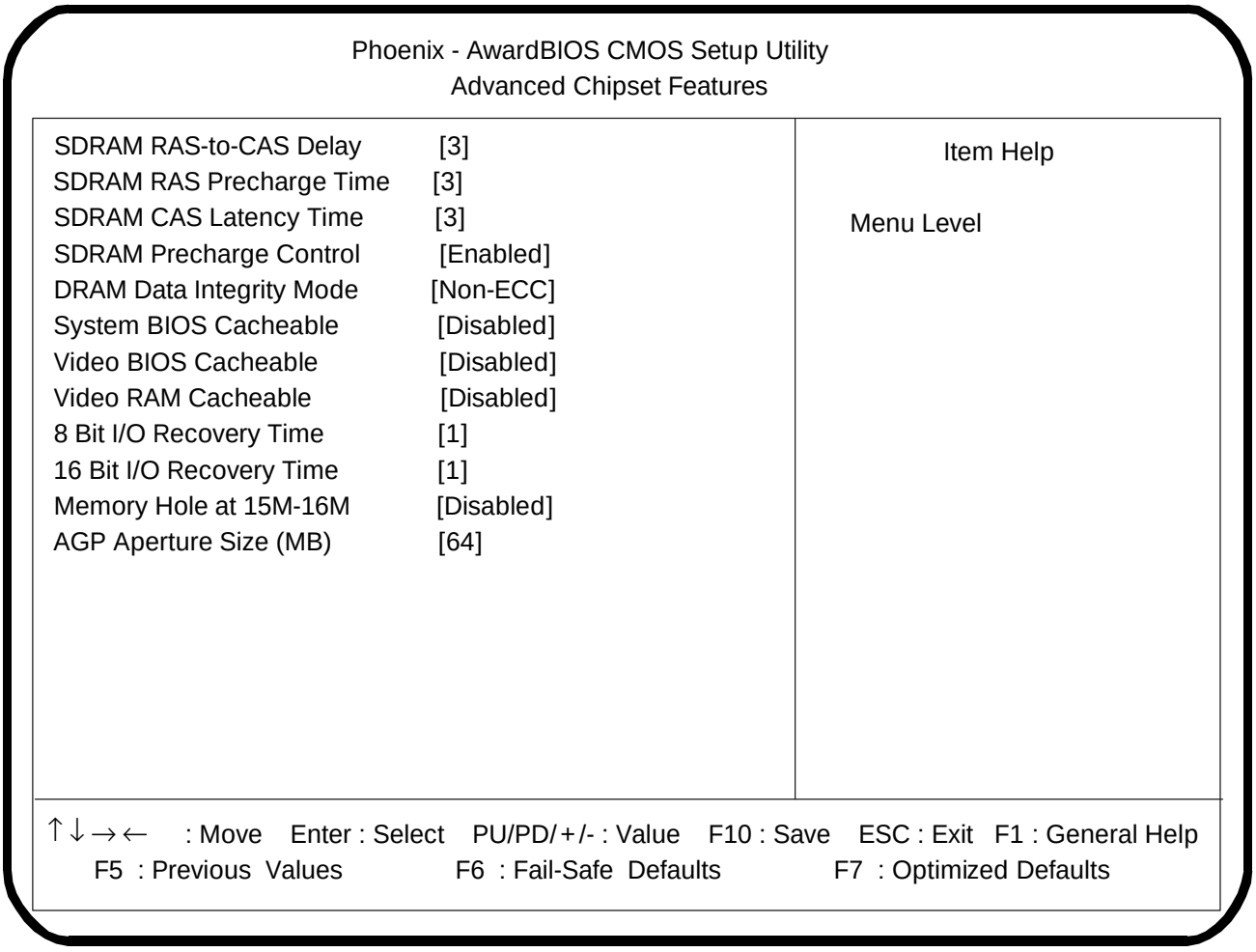
The options in this section control the chipset programming at boot time. In most cases, the default settings should be used unless you have a clear understanding of the significance of the change. It is possible using these options to create a system that will either not boot or is very unstable or unreliable. If this should occur, there are two methods to return the system to a stable configuration. If the system works well enough to get into Setup, simply choose the “Load BIOS Defaults” option and then select “Save and Exit Setup” to restore factory defaults. If the system will not run well enough to run Setup, it will be necessary to remove the battery source temporarily until the CMOS memory decays. Refer to Section 2.7 for details on reinitializing the CMOS RAM.

Each of the options for the Chipset Features Menu will be briefly discussed in the sections that follow.

SDRAM RAS-to-CAS Delay

This option allows for selection of the number of clock to delay the RAS to CAS transition. The available choices are :

3 Clocks
2 Clocks



SDRAM RAS Precharge Time

This options allows for setting the SDRAM RAS precharge timing. The choices are :

3 clocks
2 clocks

SDRAM CAS Latency Time

This option allows control of the SDRAM CAS latency timing. The choices are :

3 clocks
2 clocks

SDRAM Precharge Control

This option, when enabled, allow control of the SDRAM precharge timing.

System BIOS Cacheable

This option enables or disables cacheability of the system BIOS.

Video BIOS Cacheable

This option enables or disables cacheability of the video BIOS.

8 Bit I/O Recovery

Enables and defines 8-bit I/O recovery time in number of clocks.

16 Bit I/O Recovery

Enables and defines 16-bit I/O recovery time in number of clocks.

Memory Hole At 15M-16M

This option, when enabled, disables onboard memory between 15M and 16M.

AGP Aperture Size (MB)

This option specifies the amount of address space to allocate to the AGP video aperture. The choices are :

4
8
16
32
64
128
256

3.7 Integrated Peripherals Setup

The options in this section allow for control of the integrated peripherals, i.e. Floppy and IDE controllers, serial ports, and the parallel port.

Phoenix - Award BIOS CMOS Setup Utility
Integrated Peripherals

IDE 1st Channel Cable	[40 Pins]	Item Help
IDE 2nd Channel Cable	[40 Pins]	
IDE Primary Master PIO	[Auto]	Menu Level
IDE Primary Slave PIO	[Auto]	
IDE Secondary Master PIO	[Auto]	
IDE Secondary Slave PIO	[Auto]	
IDE Primary Master UDMA	[Auto]	
IDE Primary Slave UDMA	[Auto]	
IDE Secondary Master UDMA	[Auto]	
IDE Secondary Slave UDMA	[Auto]	
On-Chip Primary PCI IDE	[Enabled]	
On-Chip Secondary PCI IDE	[Enabled]	
USB Keyboard Support	[Disabled]	
Init Display First	[AGP]	
IDE HDD Block Mode	[Enabled]	
Onboard FDC Controller	[Enabled]	
Onboard Serial Port 1	[3F8/IRQ4]	
Onboard Serial Port 2	[2F8/IRQ3]	
Onboard Parallel Port	[378/IRQ7]	
Parallel Port Mode	[ECP+EPP1.9]	
ECP Mode Use DMA	[3]	

↑↓→← : Move Enter : Select PU/PD/+/- : Value F10 : Save ESC : Exit F1 : General Help
F5 : Previous Values F6 : Fail-Safe Defaults F7 : Optimized Defaults

IDE 1st Channel Cable

This option allows for specification of the cable type attached to the Primary IDE channel. The choices are :

40 Pins
80 Pins

IDE 2nd Channel Cable

This option allows the cable type to be specified for the secondary IDE channel. The choices are :

40 Pins
80 Pins

IDE Primary Master PIO

This option allows selection of the PIO mode to be used with the Primary Master IDE device. The choices are :

Auto
Mode 0
Mode 1
Mode 2
Mode 3
Mode 4

IDE Primary Slave PIO

This option allows for selection of the PIO mode to be used with a Primary Slave IDE device. The choices are :

Auto
Mode 0
Mode 1
Mode 2
Mode 3
Mode 4

IDE Secondary Master PIO

This option allows selection of the PIO mode to be used with the Secondary Master IDE device. The choices are :

Auto
Mode 0
Mode 1
Mode 2
Mode 3
Mode 4

IDE Secondary Slave PIO

This option allows for selection of the PIO mode to be used with a Secondary Slave IDE device. The choices are :

Auto
Mode 0
Mode 1
Mode 2
Mode 3
Mode 4

IDE Primary Master UDMA

This option allows for selecting whether an UDMA mode will be used for disk transfers on the Primary Master IDE device. The choices are :

Disabled
Auto

IDE Primary Slave UDMA

This option allows for selecting whether an UDMA mode will be used for disk transfers on the Primary Slave IDE device. The choices are :

Disabled
Auto

IDE Secondary Master UDMA

This option allows for selecting whether an UDMA mode will be used for disk transfers on the Secondary Master IDE device. The choices are :

Disabled
Auto

IDE Secondary Slave UDMA

This option allows for selecting whether an UDMA mode will be used for disk transfers on the Secondary Slave IDE device. The choices are :

Disabled
Auto

On-Chip Primary PCI IDE

This option enables or disables the onboard Primary IDE controller.

On-Chip Secondary PCI IDE

This option enables or disables the onboard Secondary IDE controller.

USB Keyboard Support

This option enables or disables BIOS support for USB keyboards.

Init Display First

This option allows selection of the source for the first, or primary, video controller. The choices are :

PCI Slot
AGP

Note : The onboard video is implemented on the AGP bus. An alternate primary video display may be used by installing a PC/104Plus video card and setting this option to PCI Slot.

IDE Block Mode

This option allows enabling of the IDE block mode for disk transfers.

Onboard FDC Controller

This option controls the onboard Floppy Disk controller. The options are :

Enabled
Disabled

Onboard Serial Port 1

This option allows for control of the first onboard serial port. The options are :

Disabled
3F8/IRQ4
2F8/IRQ3
3E8/IRQ4
2E8/IRQ3
Auto

Onboard Serial Port 2

This option allows for control of the second onboard serial port. The options are :

Disabled
3F8/IRQ4
2F8/IRQ3
3E8/IRQ4
2E8/IRQ3
Auto

Onboard Parallel Port

This option allows for configuration of the onboard parallel printer port. The options are :

Disabled
3BC/IRQ7
378/IRQ7
278/IRQ5

Parallel Port Mode

This option controls the operating mode of the onboard parallel port. The options are :

SPP
EPP1.9+SPP
ECP
ECP+EPP1.9
Normal
EPP1.7+SPP
ECP+EPP1.7

ECP Mode Use DMA

This option controls which DMA channel will be used for ECP transfers. The choices are:

3
1

3.8 Power Management Setup

The items in this menu control operation of the BIOS based power management functions.

ACPI function

This option allows for control of the BIOS level ACPI functionality.

Phoenix - Award BIOS CMOS Setup Utility
Power Management Setup

ACPI Function	[Enabled]	Item Help
Power Management	[User Define]	
PM Control by APM	[Yes]	Menu Level
Video Off Method	[V/H SYNC + Blank]	
Video Off After	[Standby]	
Modem Use IRQ	[3]	
Doze Mode	[Disabled]	
Standby Mode	[Disabled]	
Suspend Mode	[Disabled]	
HDD Power Down	[Disabled]	
VGA Active Monitor	[Disabled]	
IRQ 8 Break Suspend	[Disabled]	
USB Keyboard Support	[Disabled]	
** Reload Global Timer Events **		
IRQ[3-7, 9-15],NMI	[Disabled]	
Primary IDE 0	[Disabled]	
Primary IDE 1	[Disabled]	
Secondary IDE 0	[Disabled]	
Secondary IDE 1	[Disabled]	
Floppy Disk	[Disabled]	
Serial Port	[Disabled]	
Parallel Port	[Disabled]	

↑↓→← : Move Enter : Select PU/PD/+/- : Value F10 : Save ESC : Exit F1 : General Help
F5 : Previous Values F6 : Fail-Safe Defaults F7 : Optimized Defaults

Power Management

This option allows for the specification for the type and extent of power management options. The choices are :

User Define
Min Saving
Max Saving

PM Control by APM

This option, when enabled, allows an APM aware OS to control system power management. The options are :

Yes
No

Video Off Method

This option specifies the method used for Video blanking or PM shutdown. The options are :

Blank Screen
V/H SYNC + Blank
DPMS

Video Off After

This option specifies at what power-management stage the video off function will be exe cuted. The options are :

NA
Suspend
Standby
Doze

Modem Use IRQ

This option allows specification of the IRQ used by the modem for PM control functions. The options are :

NA
3
4
5
7
9
10
11

Doze Mode

This option allows for setting the time-out value before entering Doze mode or for disabling Doze mode completely. The options are :

Disable
1 Min
2 Min
4 Min
8 Min
12 Min
20 Min
30 Min
40 Min
1 Hour

Standby Mode

This option allows for setting the time-out value before entering Standby mode or for disabling Standby mode completely. The options are :

Disable
1 Min
2 Min
4 Min
8 Min
12 Min
20 Min
30 Min
40 Min
1 Hour

Suspend Mode

This option allows for setting the time-out value before entering Suspend mode or for disabling Suspend mode completely. The options are :

Disable
1 Min
2 Min
4 Min
8 Min
12 Min
20 Min
30 Min
40 Min
1 Hour

HDD Power Down

This option allows selection of a Hard disk power down timer. The options are :

Disable
1 Min
2 Min
3 Min
4 Min
5 Min
6 Min
7 Min
8 Min
9 Min
10 Min
11 Min
12 Min
13 Min
14 Min
15 Min

VGA Active Monitor

This option when enabled tracks video changes for PM activity status.

IRQ 8 Break Suspend

This option when enabled allows an RTC alarm event to awaken from a suspend event.

Reload Global Timer Events

The 8 options that follow allow individual selection of IRQs or devices to monitor. Activity on any of the enabled options resets the countdown timers delaying any further power management steps.

The items that can be enabled for monitoring are :

IRQ[3-7, 9-15], NMI
Primary IDE 0
Primary IDE 1
Secondary IDE 0
Secondary IDE 1
Floppy Disk
Serial Port
Parallel Port

3.9 PNP/PCI Configuration

The options in this section control PNP and PCI resources.

Phoenix - AwardBIOS CMOS Setup Utility
PNP/PCI Configuration

		Item Help
PNP OS Installed	[No]	
Reset Configuration Data	[Disabled]	Menu Level
Resources Controlled by	[Manual]	
IRQ Resources	[Press Enter]	Select yes if you are using a Plug and Play capable operating system. Select No if you need the BIOS to configure non-boot devices
DMA Resources	[Press Enter]	
Memory Resources	[Press Enter]	
PCI/VGA Palette Snoop	[Disabled]	

↑↓→← : Move Enter : Select PU/PD/+/- : Value F10 : Save ESC : Exit F1 : General Help
F5 : Previous Values F6 : Fail-Safe Defaults F7 : Optimized Defaults

PNP OS Installed

This option allows the user to assign whether the operating system is Plug and Play compatible. The options are:

Yes
No

Reset Configuration Data

This option, when enabled, will reset the configuration data on power up. The options are:

Enabled
Disabled

Resources Controlled By

This option allows the user to select resource control of the system. The options are:

Auto (ESCD)
Manual

IRQ Resources

This option allows for IRQs to be reserved for Legacy ISA devices or to be used in the pool of available IRQs for PCI and ISA PnP devices.

DMA Resources

This option allows for DMA resources to be reserved for legacy ISA devices or to be used in the pool of available DMA resources for PCI or ISA PnP devices.

Memory Resources

This option allows for reserving an upper memory block with a size between 8K and 64K Bytes. The available starting segment addresses for this reserved block are :

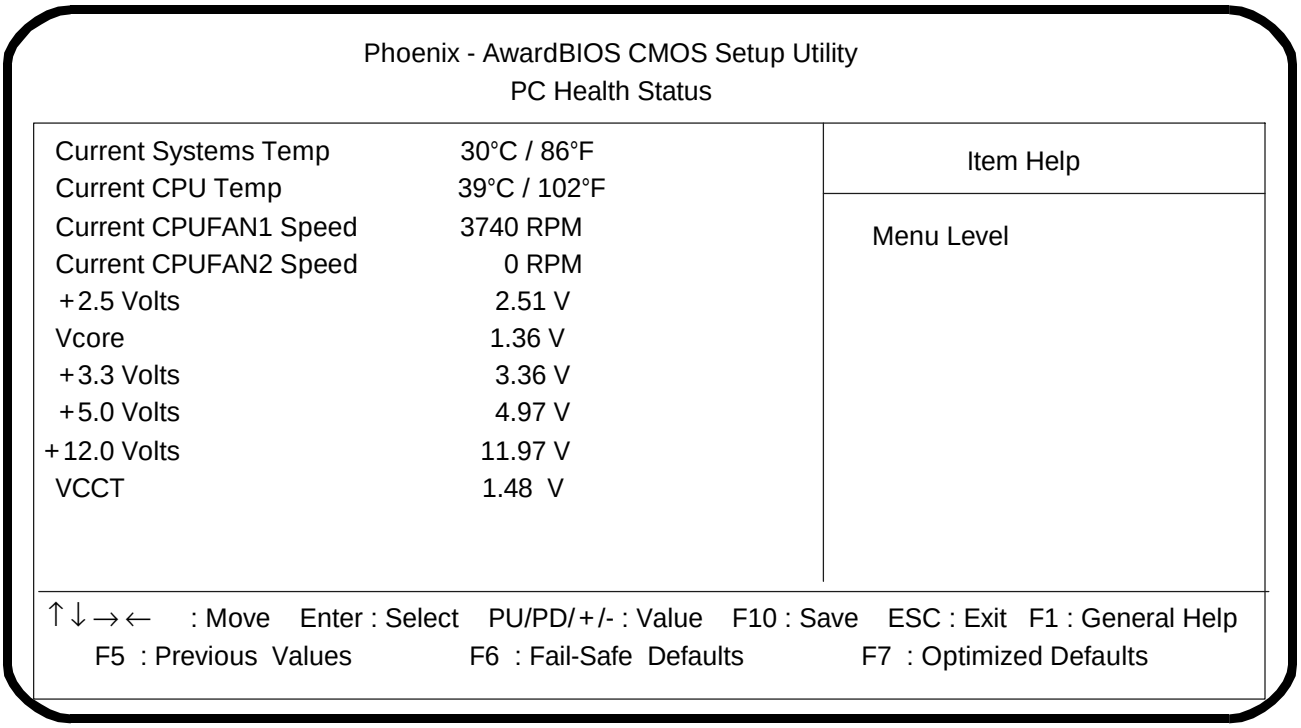
C800
CC00
D000
D400
D800
DC00

PCI/VGA Palette Snoop

This option when enabled permits PCI/VGA palette snooping.

3.10 PC Health Status

This option is different from the other setup menu items in that there are no configurable options. This is simply a status screen that can be used to examine the status of various temperatures and voltages on the board.

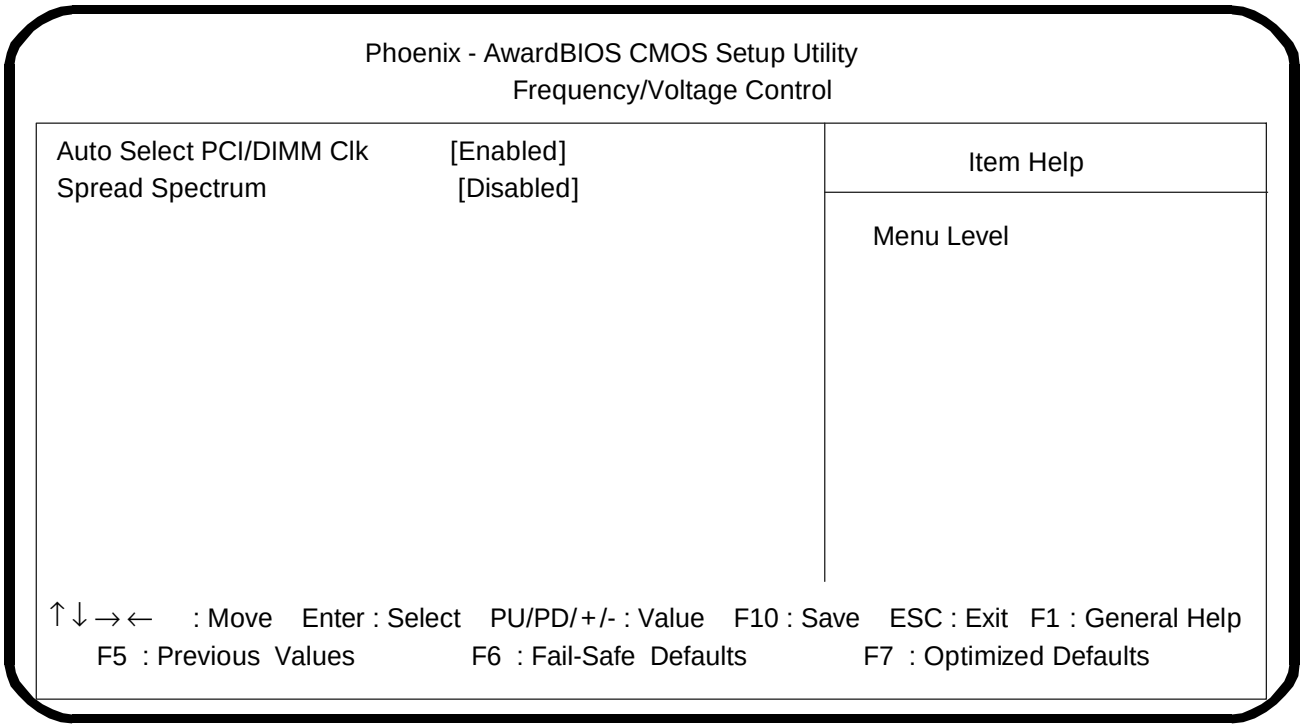


3.11 Frequency/Voltage Control

The items in this menu allow for configuration of certain clock control items.

Auto Detect PCI/DIMM Clk

This option when enabled, instructs the BIOS to turn off unused clocks to DIMM sockets and PCI slots.



Spread Spectrum

This option enables the purposeful jittering of all of the primary Clock frequencies by the percentages given by the choices shown here.

Disabled
-0.5%
+/-0.5%
+/-0.25%

3.12 Load BIOS Defaults

This option when selected, reloads all of the CMOS settings with the factory specified settings.

3.13 Set Supervisor Password

This option, when a password has been entered, protects the Setup menus from unauthorized alteration of the options. Hitting "Enter" when prompted for the password, disables the password security.

3.14 Set User Password

This option provides a second level of password security to the BIOS setup screens. When both the Supervisor and the User passwords are enabled. The user will only be able to alter fixed disk info. If no Supervisor password is enabled, the user access password allows full access to the Setup screens. The security option is disabled by hitting "Enter" at the password prompt.

3.15 Save & Exit Setup

This function writes all changes to CMOS RAM and restarts the system.

3.16 Exit without Saving

This option exits setup without saving any changes made and then restarts the system.

4 EBC-BX DiskOnChip Configuration

4.1 DiskOnChip Usage

The EBC-BX supports the M-Systems' DiskOnChip (DOC) flash device in sizes ranging from 8MB to over 500MB. The DOC device contains a BIOS extension, the TFFS (True Flash File System), and the Flash memory all in a single 32-pin device. The DOC emulates a hard disk and can be used as a secondary hard disk to a physical IDE drive or it can be the only hard disk in the system.

The DOC is installed into the socket at U15. Refer to the section 2.19 for correct device jumpering and enabling of the DOC.

4.2 DOC Initialization

The DOC is initialized in an identical fashion to a fixed disk. DOS is booted (from floppy or hard disk), FDISK is run on the DOC drive (be sure to get the right drive), the system is rebooted and then the DOC is formatted using the DOS format command.

If the /S switch was used during formatting and there is no other fixed disk device specified or attached to the system the DOC will become the boot device. If a hard disk is present, the DOC will become a secondary fixed disk.

5 WS16C48 Programming Reference

5.1 Introduction

This section provides basic documentation for the included I/O routines. It is intended that the accompanying source code equip the programmer with a basic library of I/O functions for the WS16C48 or can serve as the basis from which application specific code can be derived.

5.2 Function Definitions

This section briefly describes each of the functions contained in the driver. Where necessary, short examples will be provided to illustrate usage. Any application making use of any of the driver functions should include the header file “uio48.h”, which includes the function prototypes and the needed constant definitions.

Note that all of the functions utilize the concept of “bit_number”. The “bit_number” is a value from 1 to 48 (1 to 24 for interrupt related functions) that correlates to a specific I/O pin. Bit_number 1 is port 0 bit 0 and continues through to bit_number 48 at port 5 bit 7.

INIT_IO - Initialize I/O, set all ports to input

Syntax

```
void init_io(unsigned io_address);
```

Description

This function takes a single argument:

io_address - The I/O address of the WS16C48 chip.

There is no return value. This function initializes all I/O pins for input (sets them high), disables all interrupt settings, and sets the image values.

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READ_BIT - Reads an I/O port Bit

Syntax

int read_bit(int bit_number);

Description

This function takes a single argument:

bit_number - This is a value from 1 to 48 that indicates the I/O pin to read from.

This function returns the state of the I/O pin. A '1' is returned if the I/O pin is low and a '0' is returned if the pin is high.

WRITE_BIT - Write a 1 or 0 to an I/O pin

Syntax

void write_bit(int bit_number, int value);

Description

This function takes two arguments:

bit_number - This is value from 1 to 48, which is the bit to be acted upon.

Value - is either 1 or 0.

This function allows for writing of a single bit to either a '0' or a '1' as specified by the second argument. There is no return value and other bits in the I/O port are not affected.

SET_BIT - Set the specified I/O Bit

Syntax

void set_bit(int bit_number);

Description

This function takes a single argument:

bit_number - a value between 1 and 48 specifying the port bit to be set.

This function sets the specified I/O port bit. Note that set ting a bit re sults in the I/O pin actually going low. There is no return value and other bits in the same I/O port are unaffected.

CLR_BIT - Clear the specified I/O Bit

Syntax

void clr_bit(int bit_number);

Description

This function takes a single argument:

bit_number - a value from 1 to 48 indicates the bit number to clear.

This function clears the specified I/O bit. Note that clearing the I/O bit results in the actual I/O pin going high. This function does not affect any bits other than the one specified.

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ENAB_INT - Enable Edge Interrupt, Select Polarity

Syntax

void enab_int(int bit_number, int polarity);

Description

This function requires two arguments:

bit_number - A value from 1 to 24 specifying the appropriate bit

polarity - Specifies rising or falling edge polarity detect. The constants RISING and FALLING are defined in “uio48.h”

This function enables the edge detection circuitry for the specified bit at the specified polarity. It does not unmask the interrupt controller, install vectors, or handle interrupts when they occur. There is no return value and only the specified bit is affected.

DISAB_INT - Disable Edge Detect Interrupt Detection

Syntax

void disab_int(int bit_number);

Description

This function requires a single argument:

bit_number - A value from 1 to 24 specifying the appropriate bit.

This function shuts down the edge detection interrupts for the specified bit. There is no return value and no harm is done by calling this function for a bit which did not have edge detection interrupts enabled. There is no affect on any other bits.

CLR_INT - Clear the specified pending interrupt

Syntax

void clr_int(int bit_number);

Description

This function requires a single argument:

bit_number - The specified bit number from 1 to 24 to reset the interrupt.

This function clears a pending interrupt on the specified bit. It does this by disabling andreenabling the interrupt. The net result after the call is that the interrupt is no longer pending andis rearmed for the next transition of the same polarity. Calling this function on a bit that has not been enabled for interrupts will result in its interrupt being enabled with an undefined polarity. Calling this function with no interrupt pending will have no adverse affect. Only the specified bit is affected.

GET_INT - Retrieve bit number of pending interrupt

Syntax

int get_int(void);

Description

This function requires no arguments and returns either a '0' for no bit interrupts pending or a value between 1 and 24 representing a bit number that has a pending edge detect interrupt. The function returns with the first interrupt found and begins its search at Port 0 Bit 0 proceeding through to Port 2 Bit 7. It is necessary to use either clr_int() or disab_int() to avoid returning the same bit continuously. This function may either be used in an application's ISR or can be used in the foreground to pollfor bit transitions.

5.3 Sample Programs

There are three sample programs in source code form included on the EBC-BX diskette in the UIO48 directory. These programs are not useful by themselves but are provided to illustrate the usage of the I/O functions provided in UIO48C.

FLASH.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:

```
bcc flash.c uio48.c
```

This program illustrates the most basic usage of the WS16C48. It uses three functions from the driver code. The io_init() function is used to initialize the I/O functions and the set_bit() and clr_bit() functions are used to sequence through all 48 bits turning each on and then off in turn.

POLL.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:

```
bcc poll.c uio48.c
```

This program illustrates additional features of the WS16C48 and the I/O library functions. It programs the first 24 bits for input, arms them for falling edge detection, and then polls using the library routine get_int() to determine if any transitions have taken place.

INT.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:

```
bcc int.c uio48.c
```

This program is identical in function to the "poll.c" program except that interrupts are active and all updating of the transition counters is accomplished in the background during the interrupt service routine.

Summary

The source code for all three programs as well as the I/O routines are included on the accompanying diskette. The source code is also provided in printed form in APPENDIX F. These I/O routines along with the sample program should provide for a good basis on which to build an application using the features of the WS16C48.

6 APPENDIX A - I/O Port Map

The following is a list of PC I/O ports. Ad dresses marked with a '-' are not used on the EBC-BX but their use should be carefully qualified so as not to conflict with other I/O boards. I/O addresses marked with a '+' are used on the EBC-BX board and are unique to the WinSystems' design. I/O Addresses marked with '**' are generally un used and should be the ba sis for the first choices in I/O address selection.

Hex Range	Usage
000-00F	8237 DMA #1
**010-01F	FREE
020-021	8259 PIC #1
+022-023	Finali 486 Chipset Registers
**024-03F	FREE
040-043	8254 Timer
**044-05F	FREE
060-06F	8042 Keyboard Controller
070-071	CMOS RAM/RTC
**072-07F	FREE
080-08F	DMA Page Registers
**090-09F	FREE
0A0-0BF	8259 PIC #2
0C0-0DF	8237 DMA #2
**0E0-0EF	FREE
0F0-0F1	Coprocessor Control
**0F2-11F	FREE
+120-12F	WS16C48 HDIO
**130-1DF	FREE
+1E0-1EF	SSD, Led, Watchdog control
1F0-1FF	Fixed Disk I/O
-200-20F	Joystick port
-210-21F	PCM SSD I/O Ports
-220-22F	Soundblaster I/O ports
**230-237	FREE
-238-23B	BUS Mouse
**240-277	FREE
278-27F	LPT1
**280-2AF	FREE
-2B0-2DF	EGA Video
-2E0-2E7	GPIB Interface
2E8-2EF	COM4
**2F0-2F7	FREE
2F8-2FF	COM2
-300-31F	Prototype Card
-320-32F	XT Hard Disk
**330-377	FREE
-378-37F	Parallel Printer
-380-3AF	SDLC

-3B0-3BB	DMA
-3C0-3CF	EGA
3E8-3EF	COM3
3F0-3F6	Floppy Disk
3F8-3FF	COM1

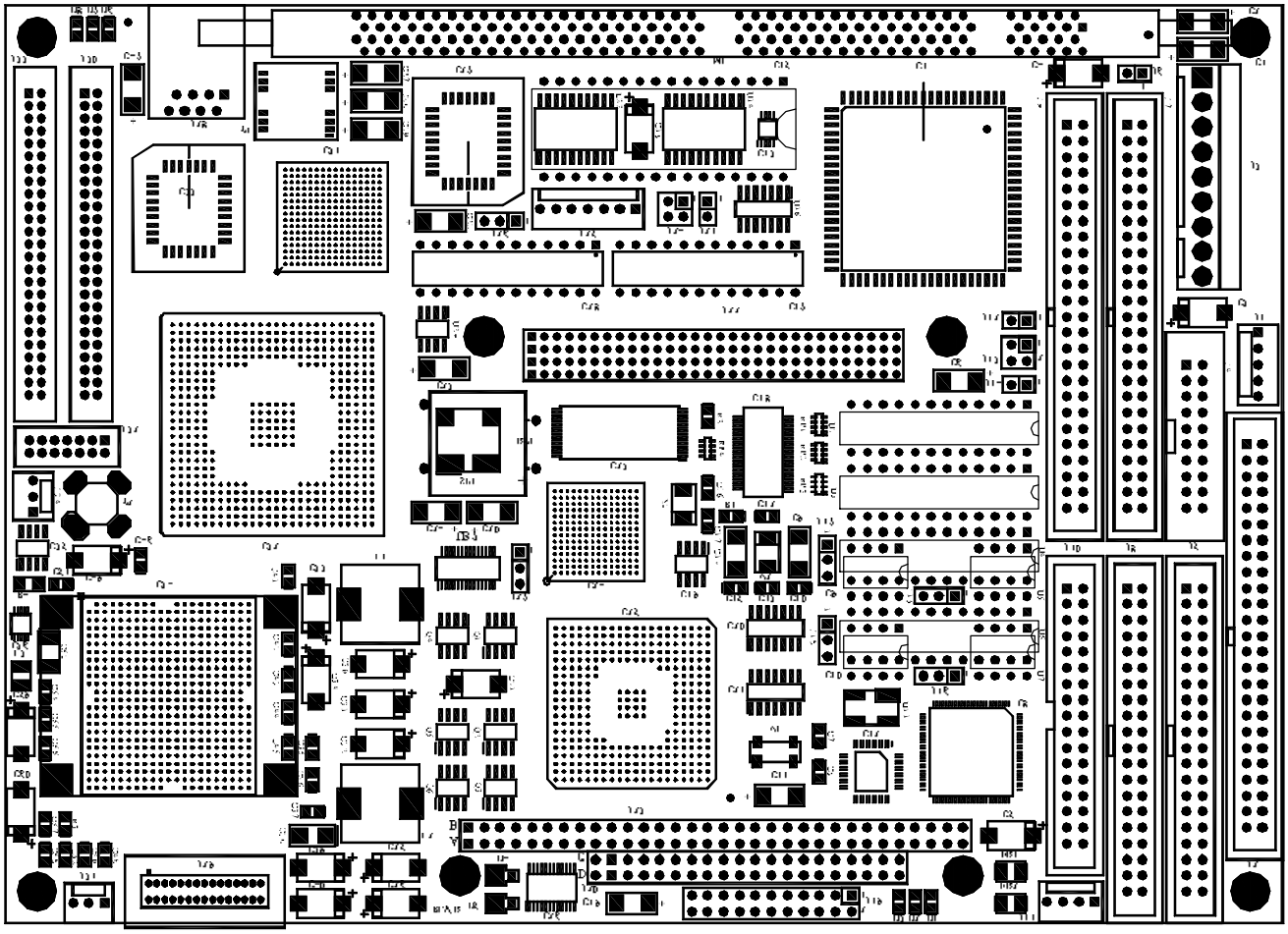
7 APPENDIX B - Interrupt Map

No.	Address	Type	Description
0	00	CPU	Divide by 0
1	04	CPU	Single Step 386 Debug Exception
2	08	CPU	NMI
3	0C	CPU	Breakpoint
4	10	CPU	Overflow
5	14	BIO	Print Screen
		186	Bound Exception
6	18	186	Invalid opcode exception
7	1C	186	Coprocessor unavailable
8	20	Hardware	IRQ0 - 18.2Hz heart beat
		286	LIDT - Double fault exception
9	24	Hardware	IRQ1 - Keyboard interrupt
		286	Coprocessor segment
A	28	Hardware	IRQ2 - XT Reserved, AT-Slaved Controller
		286	Invalid TSS exception
B	2C	Hardware	IRQ3 - COM2
		286	Segment not present
C	30	Hardware	IRQ4 - COM1
		286	Stack fault exception
D	34	Hardware	IRQ5 - XT Hard Disk, AT Free
		286	Protection fault exception
E	38	Hardware	IRQ6 - Floppy Disk Interrupt
		386	Page fault exception
F	3C	Hardware	IRQ7 - LPT1
10	40	BIOS	Video BIOS functions
		286	Coprocessor exception
11	44	BIOS	BIOS Equipment check
		486	Alignment check exception
12	48	BIOS	Memory Size function
13	4C	BIOS	BIOS Disk functions
14	50	BIOS	BIOS serial functions
15	54	BIOS	Cassette/protected mode functions
16	58	BIOS	Keyboard BIOS functions
17	5C	BIOS	BIOS printer functions
18	60	BIOS	SROM Basic Entry point (IBM)
19	64	BIOS	Boot loader function
1A	68	BIOS	BIOS time of day functions
1B	6C	BIOS	Keyboard break vector
1C	70	BIOS	User chained timer tick
1D	74	BIOS	Video Initialization
1E	78	BIOS	Floppy Disk parameter table
1F	7C	BIOS	CGA graphic character font

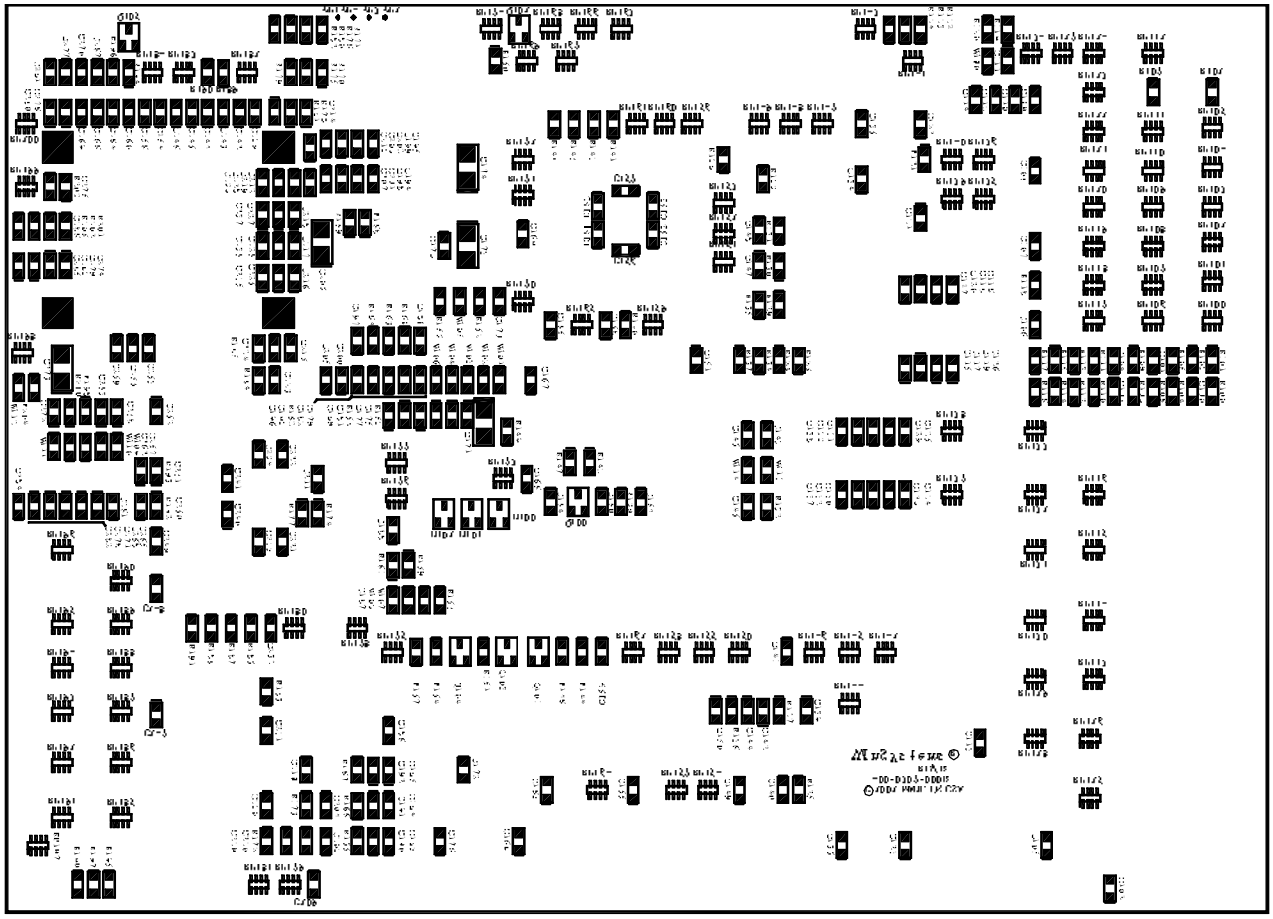
20	80	MS-DOS	Program terminate
21	84	MS-DOS	DOS function call
22	88	MS-DOS	Terminate Address
23	8C	MS-DOS	Ctrl-Break Address
24	90	MS-DOS	Fatal Error Vector
25	94	MS-DOS	Absolute disk read
26	98	MS-DOS	Absolute disk write
27	9C	MS-DOS	Terminate
28	A0	MS-DOS	Idle Signal
29	A4	MS-DOS	TTY output
2A	A8	MS-DOS	MS-Net services
2F	BC	MS-DOS	Print Spool
30	C0	MS-DOS	Long jump interface
33	CC	MS-DOS	Mouse functions
3F	FC	MS-DOS	Overlay interrupt
40	100	BIOS	Floppy I/O when fixed disk is present
41	104	BIOS	Fixed disk 1 parameter table
42	108	BIOS	EGA Chain
43	10C	BIOS	EGA Parameter table pointer
44	110	BIOS	EGA graphics character font
4A	128	BIOS	AT Alarm exit address
50	140	BIOS	AT Alarm interrupt
51	144	BIOS	Mouse functions
5A	168	NET	Functions
5B	16C	NET	Boot chain
5C	170	NET	Net BIOS entry
67	19C	MS-DOS	EMS functions
6D	1B4	VGA	VGA Service
70	1C0	Hardware	IRQ8 - Real Time clock
71	1C4	Hardware	IRQ9 - Redirected IRQ2
72	1C8	Hardware	IRQ10 - Unassigned
73	1CC	Hardware	IRQ11 - Unassigned
74	1D0	Hardware	IRQ12 - Unassigned
75	1D4	Hardware	IRQ13 - Unassigned
76	1D8	Hardware	IRQ14 - IDE Fixed Disk
77	1DC	Hardware	IRQ15 - Unassigned
80	200		
F0	3C0	Basic	
F1	3C4		
FF	3FC	Not Used	

8 APPENDIX C

EBC-BX Parts Placement Guide - Top



EBC-BX Parts Placement Guide - Bottom



9 APPENDIX D

EBC-BX Parts List

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
EBC-BXPLUS-700		EBX-COMPATIBLE 700 MHZ LP PENTIUM 3 OMB	EBX-COMPATIBLE 700 MHZ LP PENTIUM 3 OMB SD	F	1.0
1	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
1	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
1	999-9999-001	SPECIAL NOTES	05/21/02 MEB (REV A)	I	1.0
1	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
1	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
1	0307-001-0000C	ASSY CORE, BOT-SMT EBC-BX REV.C	ASSY CORE, BOT-SMT EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44 REVC	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/02/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	02-06-03 KMT ECO 03-09	I	1.0
2	999-9999-001	SPECIAL NOTES	05/08/03 KMT ECO# 03-36	I	1.0
2	400-0307-000C	PCB, EBC-BX REV.C		I	1.0
2	601-0000-503	RES 0 Ohm 5% 1/10w 0805	R100,R101,R110,R111,R118,R182,W100,	I	13.0
2	999-9999-001	SPECIAL NOTES	W105,W107,W109,W112,W113,W114	I	1.0
2	601-0100-503	RES 10 Ohm 5% 1/10w 0805	R149,R165,R166,R167	I	4.0
2	601-0101-503	RES 100 Ohm 5% 1/10w 0805	R127,R139,R183	I	3.0
2	601-0102-503	RES 1K Ohm 5% 1/10W 0805	R128,R130,R131,R137,R138,R140,R144,R151,	I	11.0
2	999-9999-001	SPECIAL NOTES	R154,R171,R180	I	1.0
2	601-0103-503	RES 10K Ohm 5% 1/10W 0805	R126,R129,R132,R134,R135,R146,R150,R155,	I	12.0
2	999-9999-001	SPECIAL NOTES	R187,R188,R191,R204	I	1.0
2	601-0203-503	RES 20K Ohms 5% 1/10W 0805	R156	I	1.0
2	601-0220-503	RES 22 Ohm 5% 1/10w 0805	R174,R177,R186	I	3.0
2	601-0271-503	RES 270 Ohm 5% 1/10w 0805	R175,R190,R196	I	3.0
2	601-0303-503	RES 30K OHM 5% 0805 1/10W SMT	R152,R160,R205	I	3.0
2	601-0331-503	RES 330 Oh, 5%, 0805	R121,R122,R123,R124,R141,R143,R145,R148,	I	12.0
2	999-9999-001	SPECIAL NOTES	R195,R197,R199,R202	I	1.0
2	601-0332-503	RES 3.3K Ohm, 5%, 0805 1/10W SMT	R158,R162,R176	I	3.0
2	601-0470-503	RES 47 Ohm 5% 1/10w 0805	R170,R194	I	2.0
2	601-0471-503	RES 470 Ohm 20% 1/10w 0805	R102,R107	I	2.0
2	601-0474-503	RES 470K Ohm 5% 1/10W 0805	R120	I	1.0
2	601-0564-503	RES 560K Ohm 5% 1/10W 0805	R119	I	1.0
2	601-0683-503	RESISTOR 68K 5% 0805 SMT	R153	I	1.0
2	601-0750-503	RES 75 Ohm 5% 1/10W 0805	R193	I	1.0
2	601-1000-303	RES 100 Ohm 1% 1/10w 0805 SMT	R161,R172,R181	I	3.0
2	601-1001-303	RES 1K OHM 1% 1/10W SMT 0805	R185,R201,R203	I	3.0
2	601-1100-303	RES 110 OHM 1% 0805 1/10W SMT	R168	I	1.0
2	601-1210-303	RES 121 Ohm 1% 1/10w 0805	R173	I	1.0
2	601-1432-303	RES 14.3K Ohm 1% 1/10w 0805	R163	I	1.0
2	601-1500-303	RES 150 Ohm 1% 1/10w 0805	R159,R178,R192	I	3.0
2	601-1501-303	RES 1.5K Ohm 1% 1/10w 0805	R125,R136,R184	I	3.0
2	601-3922-303	RES 39.2K Ohms 1% 1/10W 0805	R198	I	1.0
2	601-4532-303	RES 45.3K 1% 0805	R164,R200	I	2.0
2	601-5490-303	RES 549 Ohms 1% 0805	R142,R157	I	2.0
2	601-562A-303	RES 56.2 OHM 1% 0805 1/10W SMT	R169,R179,R189	I	3.0
2	601-6040-303	RES 604 Ohms 1% 1/10W 0805	R147	I	1.0

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	602-0100-524	RN 10 Ohm, 5%, 4RES ARRAY	RP170,RP198	I	2.0
2	602-0101-524	RN 100 Ohm, 5%, 4RES ARRAY	RP150	I	1.0
2	602-0102-524	RN 1K Ohm, 5%, 4RES ARRAY	RP105,RP121,RP139,RP141,RP154,RP163,RP173,	I	10.0
2	999-9999-001	SPECIAL NOTES	RP184,RP199,RP200	I	1.0
2	602-0103-524	RN 10K Ohm, 5%, 4RES ARRAY	RP100,RP101,RP102,RP103,RP104,RP113,	I	37.0
2	999-9999-001	SPECIAL NOTES	RP114,RP115,RP116,RP125,RP126,RP128,RP129,	I	1.0
2	999-9999-001	SPECIAL NOTES	RP130,RP131,RP132,RP133,RP134,RP135,	I	1.0
2	999-9999-001	SPECIAL NOTES	RP136,RP137,RP138,RP143,RP144,RP145,RP146,	I	1.0
2	999-9999-001	SPECIAL NOTES	RP147,RP149,RP157,RP159,RP160,RP161,	I	1.0
2	999-9999-001	SPECIAL NOTES	RP164,RP165,RP167,RP171,RP172	I	1.0
2	602-0151-524	RN 15O OHM 4 RES 8 PIN PKG 5%	RP182,RP183	I	2.0
2	602-0152-524	RN 1.5K OHM 4 RESISTOR 8 PIN PKG	RP174	I	1.0
2	602-0220-524	RN 22 Ohm, 5%, 4RES ARRAY	RP185,RP186,RP187,RP188,RP189,RP190,RP191	I	11.0
2	999-9999-001	SPECIAL NOTES	RP192,RP193,RP194,RP195	I	1.0
2	602-0272-524	RN 2.7K Ohm, 5%, 4RES ARRAY	RP142,RP155,RP158,RP162	I	4.0
2	602-0330-524	RN 33 Ohm, 5%, 4RES ARRAY	RP106,RP107,RP108,RP109,RP111,RP112,RP117,	I	16.0

2	999-9999-001	SPECIAL NOTES	RP118,RP119,RP120,RP122,RP123,RP124,RP127,	I	1.0
2	602-0331-524	RN 330 Ohm, 5%, 4RES ARRAY	RP151,RP152	I	2.0
2	602-0471-524	RN 470 Ohm, 4 RES 8 PIN RPACK	RP168,RP169	I	2.0
2	602-0472-524	RN 4.7K Ohm, 5%, 4RES ARRAY	RP110,RP140,RP148,RP166,RP197	I	5.0
2	602-0750-524	RN 75 Ohm, 5%, 4RES ARRAY	RP181,RP196	I	2.0
2	602-0822-524	RN 8.2K Ohm, 5%, 4RES ARRAY	RP153,RP156,RP175,RP176,RP177,RP178,RP179,	I	8.0
2	999-9999-001	SPECIAL NOTES	RP180	I	1.0
2	603-1027-803	CAP 1000pF 50v 20% CER 0805	C111,C272	I	2.0
2	603-1037-803	CAP .01uF 50v 20% CER 0805	C155,C168,C176,C209	I	4.0
2	603-1047-803	CAP .1uF 50v 20% CER 0805	C102,C105,C106,C107,C108,C109,C113,C114,	I	109.0
2	999-9999-001	SPECIAL NOTES	C115,C116,C117,C118,C119,C120,C121,C122,	I	1.0
2	999-9999-001	SPECIAL NOTES	C123,C124,C125,C126,C127,C128,C129,C130,	I	1.0
2	999-9999-001	SPECIAL NOTES	C131,C132,C133,C134,C135,C136,C137,C138,	I	1.0
2	999-9999-001	SPECIAL NOTES	C139,C140,C141,C142,C143,C144,C145,C146,	I	1.0
2	999-9999-001	SPECIAL NOTES	C147,C149,C151-C154,C156,C157,C158,C159,	I	1.0
2	999-9999-001	SPECIAL NOTES	C160,C161,C162,C163,C164,C165,C167,C170,	I	1.0
2	999-9999-001	SPECIAL NOTES	C172,C178,C179,C180,C183,C184,C185,C186,	I	1.0
2	999-9999-001	SPECIAL NOTES	C187,C188,C189,C190,C191,C192,C205,C210,	I	1.0
2	999-9999-001	SPECIAL NOTES	C214,C221,C223,C229,C231,C232,C233,C234,	I	1.0
2	999-9999-001	SPECIAL NOTES	C236,C237,C239,C240,C241,C242,C243,C247,	I	1.0
2	999-9999-001	SPECIAL NOTES	C250,C251,C252,C253,C255,C256,C257,C258,	I	1.0
2	999-9999-001	SPECIAL NOTES	C260,C261,C262,C263,C264,C267,C274,C284,	I	1.0
2	999-9999-001	SPECIAL NOTES	C285	I	1.0
2	603-1052-803	CAP 1uF 10v 20% CER 0805	C166,C182,C222	I	3.0
2	603-1055-807	CAP 1uF 25v 20% CER 1812	C171,C173,C174,C206,C273	I	5.0
2	603-1061-803	CAP 10uF 6.3v 20% X5R SMT 0805	C150	I	1.0
2	603-1527-803	CAP .0015uF 50v 20% CER 0805	C230	I	1.0
2	603-2219-803	CAP 220pF 200v 20% CER 0805	C278,C282,C286	I	3.0
2	603-8217-803	CAP 820pF 50v 20% CER 0805	C181,C196	I	2.0
2	603-3307-503	CAP 33pF 50v 2% CER 0805	C283	I	1.0

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	603-3317-803	CAP 330PF 20% 50V 0805 SMT X7R	C177,C197	I	2.0
2	603-4707-803	CAP 47pF 50v 20% CER 0805 4k per reel	C110,C112,C265,C268,C271	I	5.0
2	603-4737-803	CAP .047uF 50v 20% CER 0805	C148,C169	I	2.0
2	603-56R7-303	CAP 5.6pF 50V +/-.5PF 0805 SMT NPO	C175,C193	I	2.0
2	603-82R7-303	CAP 8.2pF 50v .50pF CER 0805	C220	I	1.0
2	607-0008-000	DIODE SMT SCHOTTKY SOT-23	D100,D101,D102	I	3.0
2	660-0002-002	TRANS MMBT2222ALT1 SOT-23	Q100,Q101,Q103,Q104	I	4.0
2	665-0004-002	FAIRCHILD FDV301N NCHANNEL DIGITAL FET	Q102	I	1.0
SUB-ASSEMBLY TOTAL: 0307-001-0000C ARLIN - 93 Items					
1	0307-002-0000C	ASSY CORE, TOP-TH EBC-BX REV.C	ASSY CORE, TOP-TH EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	07-01-03 MEB ECO 03-36	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/15/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	200-0040-000	SOCKET 40 POS QPHFZ-40-B-1W (Aptos)	J20	I	1.0
2	200-0064-000	SOCKET 64 POS QPHFZ-64-B-1W (Aptos)	J23	I	1.0
2	200-0120-000	CONN PC104 PLUS Aptos PQECOK9.35/2.28	J22	I	1.0
2	200-0168-100	SOCKET 168 PIN 3.0V SDRAM DIMM,VERTICAL	M1	I	1.0
2	201-0003-001	HDR 3 PIN MOLEX 22-11-2032	J31,J34	I	2.0
2	201-0004-003	HDR MOLEX 4 POS 22-11-2042	J11	I	1.0
2	201-0005-003	HEADER 5 PIN LATCH MOLEX 22-11-2052	J1	I	1.0
2	201-0009-003	HEADER 9 POS. RA .156" SP GOLD PLATING	J3	I	1.0
2	201-0034-021	HDR 34 ST IDH-34LP-S3-TR (720)	J10	I	1.0
2	201-0036-010	HDR 1X36 UN Aptos LHY-36S-E-060/030	J12,J21=1X2	I	.6
2	999-9999-001	SPECIAL NOTES	J15,J16,J17,J18,J27=1X3	I	1.0
2	201-0040-022	HDR 40 POS IDC W/PIN 20 REMOVED 80/tray	J5,J8	I	2.0
2	201-0050-021	HDR 50 ST IDH-50LP-S3-TR (504) 60/tray:	J2	I	1.0
2	201-0072-120	HDR 2X36 UN Aptos LHZ-72S-E-060/030	J13=2X2 J19=2X11	I	.4
2	250-0320-001	TERMINAL STRIP 316-93-132-41-006000	U15=2X16	I	1.0
2	250-0320-200	SKT STRP 32 POS SS-132-G-2 (SAM)	U4,U6=2X12 U5,U7,U9,U10=2X4	I	3.0
2	200-0243-100	SOCKET 24 P .3 ICO-243-S8A-T (1,496)	U17,U28	I	2.0
SUB-ASSEMBLY TOTAL: 0307-002-0000C ARLIN - 23 Items					
1	0307-004-0000C	ASSY CORE, TOP-SMT EBC-BX REV.C	ASSY CORE, TOP-SMT EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0

2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/15/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	0.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	125-0008-000	TRANSISTOR SI4947DY DUAL P-CHANNEL FET	U29	I	1.0
2	601-0220-503	RES 22 Ohm 5% 1/10w 0805	R1,R2	I	2.0

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	601-2508-304	RES .025 OHM 1/2WATT 1% 1206 SMT	R4	I	1.0
2	602-0330-524	RN 33 Ohm, 5%, 4RES ARRAY	RP1,RP2,RP3,RP4	I	4.0
2	603-1047-803	CAP .1uF 50v 20% CER 0805	C10,C15,C36,C42-C46,C48,C50,C56	I	11.0
2	603-1055-807	CAP 1uF 25v 20% CER 1812	C38,C53	I	2.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C1,C2,C9,C11,C14,C19,C20,C24	I	8.0
2	603-107C-85F	CAP 100UF 8VOLT 20% POLYMER ALUM 7343H	C3,C21,C30,C31,C32,C33,C34	I	7.0
2	603-187B-85F	IC, CAP 180UF 4V 20% POLYMER ALUM 7343H	C25,C26,C39,C40,C49,C60	I	6.0
2	603-2207-503	CAP 22PF 50v 2% NPO 0805	C12,C13,C16,C17	I	4.0
2	603-3365-82E	CAP 33UF 25V 20% 7343 TANT.SMT	C5,C59	I	2.0
2	603-4763-82E	CAP 47uF 16v 20% TAN 7343	C4,C18	I	2.0
2	603-68R7-203	CAP 6.8pF 50v +/-.5pf CER 0805 4k/reel	C7,C8	I	2.0
2	605-1005-000	INDUCTOR 4.7uh 0805 SMT	L3	I	1.0
2	605-2001-000	FERRITE BEAD, SMT 3528	FB1,FB2	I	2.0
2	606-0006-000	IC, 5VH 4AMP TRANSFORMER	T2	I	1.0
2	606-0008-000	IC, SHIELDED INDUCTOR SMT	L1,L2	I	2.0
2	607-0005-005	LED, GREEN SMT	D1,D7	I	2.0
2	607-0006-005	LED, RED SMT	D2,D3,D6	I	3.0
2	607-0007-005	LED, YELLOW SMT	D8	I	1.0
2	607-0010-013	IC UPS5819 POWERMITE SCHOTTKY DIODE 1A	D4,D5	I	2.0
2	611-0004-001	IC, 74HC04M Philips 74HC04D-T 2500/reel	U20	I	1.0
2	611-0125-001	IC, 74HC125 QUAD TRI-STATE BUFFER	U16	I	1.0
2	611-0245-002	IC, 74HC245DW-T Philips 2k/reel	U22	I	1.0
2	612-0014-001	IC, 74HCT14 (SM)	U21	I	1.0
2	612-0688-002	IC, 74HCT688D-T (SM) Philips 2k/reel	U14	I	1.0
2	621-0025-024	IC, FDC37C672-MD SUPER I/O TQFP	U8	I	1.0
2	622-0002-019	IC, LTC1726EMS8-5 SUPERVISOR	U13	I	1.0
2	622-0020-021	IC, SYSTEM HARDWARE MONITOR	U26	I	1.0
2	622-0021-019	IC, FREQ. SYNTH CY28317ZC-2T TSSOP	U18	I	1.0
2	623-0011-025	IC, INTEL 82443BX HOST BRIDGE/CONTROLLER	U32	I	1.0
2	623-0012-025	IC, SMSC SLC90E66 PCI SOUTH BRIDGE	U25	I	1.0
2	650-0032-002	SOCKET 32P AMP 822498-1 (28)	U27	I	1.0
2	665-0005-008	IC, N CHANNEL SMPS MOSFET S0-8 PKG	Q1,Q2,Q3,Q4,Q5,Q6	I	6.0
2	668-0001-008	IC, DUAL COMPLIMENTARY MOSFET S0-8 PKG	U35	I	1.0
2	677-0006-029	IC, SWITCHING REGULATOR CONTROLLER	U36	I	1.0
2	677-0007-019	IC, DUAL SWITCHING CONT. W/150ma LD0	U37	I	1.0
2	681-0002-007	XTAL, 14.31818mhz 18pf SMT FA-365	Y2	I	1.0
2	681-0004-001	XTAL 32.768KHZ SMT 6pf load capacity	Y1	I	1.0
2	682-0003-006	OSC 1.8432MHZ CMOS SG-710 SERIES	U11	I	1.0
2	690-0001-000	TRANSDUCER, AUDIO STAR MQT-03D	SP1	I	1.0
SUB-ASSEMBLY TOTAL: 0307-004-0000C ARLIN - 46 Items					
1	0307-010-0000C	SUB ASSY CORE, EBC-BX REV.C	SUB ASSY CORE, EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/15/02 MEB (REVA)	I	1.0

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	999-9999-001	SPECIAL NOTES	02-05-03 KMT ECO 0309	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	111-0047-000	BATTERY, LTC-3PN 3.5V (EAGLE PICHER)	BT1 *MUST HAND SOLDER AFTER ASSEMBLY	I	1.0

2	201-0002-000	PLUG JUMPER 999-19-310-00-000000	J12=1-2 J13=1-2 3-4	I	9.0
2	999-9999-001	SPECIAL NOTES	J19=5-6 11-12 13-14 19-20 21-22	I	1.0
2	999-9999-001	SPECIAL NOTES	J27=2-3	I	1.0
2	637-0008-015	FLASH, 256KX8 AT29C020-PLCC (32/TUBE)	U27 CS=4A9B \EBCBX\REL0416.BIN	I	1.0
2	730-0083-000	IC, SP208CP (SIPEX), MAX208CNG (15)	U4,U6	I	2.0
2	901-0011-000	IC, PALC22V10-35PC (15,TI) (17,CYP)	U17 CS=8503 \EBCBX\EBCBXU17.JED	I	2.0
2	999-9999-001	SPECIAL NOTES	U28 CS=2B84 \EBCBX\EBCBXU28.JED	I	1.0
2	999-9999-001	SPECIAL NOTES	NOTE: INST. FOR ASSY. OF FAN / HEAT SINK	I	1.0
2	403-0307-200	ASSY DRAWING, CPU COOLER	DRAWING, CPU COOLER INSTRUCTIONS.	I	1.0
2	502-0515-200	CPU COOLER, 54mm 5V W/TACH 10 wk LT	U34 * SEE 403-0307-200 INSTRUCTIONS	I	1.0
2	502-0009-000	HEAT SINK 1" X 1" MATERIAL/PART# RD-339C	U34 * SEE 403-0307-200 INSTRUCTIONS	I	1.0
2	502-0018-000	HEAT 'SPREADER' 1.25"x 1.60" COPPER	U34 * SEE 403-0307-200 INSTRUCTIONS	I	1.0
2	502-0209-000	HEAT SINK .750"x.750" THERMAGAP .020"THK	U34 * SEE 403-0307-200 INSTRUCTIONS	I	1.0
2	500-0200-033	SCREW PPH 4-40 X 1/4"	U34 * SEE 403-0307-200 INSTRUCTIONS	I	4.0
2	CBL-238-1	CABLE, CPU COOLING FAN	U34 * SEE 403-0307-200 INSTRUCTIONS	I	1.0
2	502-0016-000	HEAT SINK,BDN14-3CB 1.41"SQUARE x.355"HT	U32 * INST. W/THERMAL ADHESIVE 502-0009-00	I	1.0
2	502-0009-000	HEAT SINK 1" X 1" MATERIAL/PART# RD-339C	U32 * INST. ON 502-0016-000	I	1.0

SUB-ASSEMBLY TOTAL: 0307-010-0000C ARLIN - 24 Items

1	0307-200-0000C	ASSY ENET, TOP-SMT, EBC-BX REV.C	ASSY ENET, TOP-SMT, EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	12/06/02 KT ECO# 02-73	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C22	I	1.0
2	606-0007-000	IC, 10/100 LAN MAGNETICS	T1	I	1.0
2	621-0038-025	IC, GD82551QM ETHERNET PCI CONTROLLER	U24	I	1.0
2	635-0001-001	IC, 24C02 SEEPROM S08 SERIAL 16X64	U19	I	1.0
2	681-0001-007	XTAL, 25.0000mhz 18pf SMT FA-365	Y3	I	1.0

SUB-ASSEMBLY TOTAL: 0307-200-0000C ARLIN - 11 Items

1	0307-202-0000C	ASSY ENET, TOP-TH EBC-BX REV.C	ASSY ENET, TOP-TH EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	201-0008-500	TEL JACK RJ45 MOLEX 950-01-2881	J28	I	1.0

SUB-ASSEMBLY TOTAL: 0307-202-0000C ARLIN - 6 Items

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
1	0307-300-0000C	ASSY VIDEO,TOP-SMT EBC-BX REV.C	ASSY VIDEO,TOP-SMT EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C23,C27,C28,C29,C47	I	5.0
2	650-0032-002	SOCKET 32P AMP 822498-1 (28)	U33	I	1.0
2	621-0026-025	IC, VIDEO CONTROLLER, 69K 256 PIN MBGA	U31	I	1.0

SUB-ASSEMBLY TOTAL: 0307-300-0000C ARLIN - 8 Items

1	0307-302-0000C	ASSY VIDEO,TOP-THR EBC-BX REV.C	ASSY VIDEO,TOP-THR EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	201-0007-003	HEADER 7 PIN MOLEX 22-11-2072	J25	I	1.0
2	201-0014-420	HDR., 2X7 2MM SHROUDED	J32	I	1.0
2	201-0036-010	HDR 1X36 UN Aptos LHY-36S-E-060/030	J26=1X3	I	1.0
2	201-0050-420	HDR, Sam., STMM-125-02-S-D	J30,J33	I	2.0

SUB-ASSEMBLY TOTAL: 0307-302-0000C ARLIN - 9 Items

1	0307-310-0000C	SUB ASSY VIDEO, EBC-BX REV.C	SUB ASSY VIDEO, EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	03/21/03 MEB ECO 03-20	I	1.0

2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	637-0003-015	IC, AT29C010A-12JC 128K X 8 FLASH ROM	U33 CS=3B00 EBCBX\PCIVID\REL0314.BIN	I	1.0
2	201-0002-000	PLUG JUMPER 999-19-310-00-000000	J12=1-2	I	2.0
2	999-9999-001	SPECIAL NOTES	J26=2-3	I	1.0
SUB-ASSEMBLY TOTAL: 0307-310-0000C		ARLIN - 9 Items			
1	0307-400-0000C	ASSY SECOND SERIAL TOP-SMT,EBC-BX REVC	ASSY SECOND SERIAL TOP-SMT,EBC-BX REVC	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	621-0033-024	IC, ST16C2550CQ48 DUAL UART	U12	I	1.0
SUB-ASSEMBLY TOTAL: 0307-400-0000C		ARLIN - 6 Items			

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
1	0307-402-0000C	ASSY SECOND SERIAL TOP-TH,EBC-BX REV.C	ASSY SECOND SERIAL TOP-TH,EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	201-0020-021	HEADER 2x10 ST Aptos LPHS-20S3-B-032-SP	J4	I	1.0
2	201-0072-120	HDR 2X36 UN Aptos LHZ-72S-E-060/030	J24=2X2	I	.1
2	250-0320-200	SKT STRP 32 POS SS-132-G-2 (SAM)	U2=2X12 U3=2X12	I	.7
SUB-ASSEMBLY TOTAL: 0307-402-0000C		ARLIN - 8 Items			
1	0307-410-0000C	SUB ASSY SECOND SERIAL,EBC-BX REV.C	SUB ASSY SECOND SERIAL,EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	730-0083-000	IC, SP208CP (SIPEX), MAX208CNG (15)	U2,U3	I	2.0
2	201-0002-000	PLUG JUMPER 999-19-310-00-000000	J24=1-2 3-4	I	2.0
SUB-ASSEMBLY TOTAL: 0307-410-0000C		ARLIN - 7 Items			
1	0307-500-0000C	ASSY DIGITAL TOP SMT, EBC-BX REV.C	ASSY DIGITAL TOP SMT, EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C6	I	1.0
2	650-0084-002	SOCKET, 84 POSITION PLCC 213-084-602	U1	I	1.0
SUB-ASSEMBLY TOTAL: 0307-500-0000C		ARLIN - 7 Items			
1	0307-502-0000C	ASSY DIGITAL TOP TH, EBC-BX REV.C	ASSY DIGITAL TOP TH, EBC-BX REV.C	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	201-0036-010	HDR 1X36 UN Aptos LHY-36S-E-060/030	J6,J14=1X2	I	.1
2	201-0050-021	HDR 50 ST IDH-50LP-S3-TR (504) 60/tray:	J7,J9	I	2.0
SUB-ASSEMBLY TOTAL: 0307-502-0000C		ARLIN - 7 Items			
1	0307-510-0000C	SUB ASSY DIGITAL, EBC-BX REV.C	SUB ASSY DIGITAL, EBC-BX REV.C	F	1.0

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	201-0002-000	PLUG JUMPER 999-19-310-00-000000	J6=1-2	I	1.0
2	905-0030-000	IC, UD27-PL84-M3B:D	U1	I	1.0
SUB-ASSEMBLY TOTAL: 0307-510-0000C		ARLIN - 7 Items			
1	0307-720-0000C	SUB ASSY BOT-SMT PROCESSOR 700MHZ REVC	SUB ASSY BOT-SMT PROCESSOR 700MHZ REVC	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	603-2252-803	CAP 2.2uF X5R 10v 20% CER 0805	C194,C195,C198,C199,C201,C202,C207,C208,	I	35.0
2	999-9999-001	SPECIAL NOTES	C212,C213,C215,C216,C217,C218,C219,C224,	I	1.0
2	999-9999-001	SPECIAL NOTES	C225,C226,C227,C228,C235,C238,C244,C245,	I	1.0
2	999-9999-001	SPECIAL NOTES	C246,C254,C259,C266,C269,C270,C275,C276,	I	1.0
2	999-9999-001	SPECIAL NOTES	C277,C280,C281	I	1.0
2	601-0000-503	RES 0 Ohm 5% 1/10w 0805	W102,W106	I	2.0
SUB-ASSEMBLY TOTAL: 0307-720-0000C		ARLIN - 11 Items			
1	0307-725-0000C	SUB ASSY TOP-SMT PROCESSOR 700MHZ REVC	SUB ASSY TOP-SMT PROCESSOR 700MHZ REVC	F	1.0
2	999-9999-001	SPECIAL NOTES	07/24/03 MEB ECO 03-44	I	1.0
2	999-9999-001	SPECIAL NOTES	09/11/02 MEB ECO 02-42	I	1.0
2	999-9999-001	SPECIAL NOTES	05/16/02 MEB (REVA)	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	999-9999-001	SPECIAL NOTES	SPECIAL NOTES	I	1.0
2	603-2252-803	CAP 2.2uF X5R 10v 20% CER 0805	C35,C37,C41,C51,C52,C54,C55,C57,C58	I	9.0
2	620-0017-025	IC, PROC. KC80526GY850256 850MHZ PIII	U34	I	1.0
SUB-ASSEMBLY TOTAL: 0307-725-0000C		ARLIN - 7 Items			
1	950-0001-100	BAG STATIC BARRIER 07-0810 8X10	BAG STATIC BARRIER 07-0810 8X10	I	1.0
1	910-0024-000	LABEL, STATIC SENSITIVE 130-02	LABEL, STATIC SENSITIVE 130-02	I	1.0
1	910-0037-000	LABEL, AWARD BIOS, D686 Pentium	INSTALL BIOS LABEL ON PC104 CONNECTOR.	I	1.0
1	999-9999-001	SPECIAL NOTES	NOTE: JUMPER SETUP SUMMARY	I	1.0
1	999-9999-001	SPECIAL NOTES	J6=1-2	I	1.0
1	999-9999-001	SPECIAL NOTES	J12=1-2	I	1.0
1	999-9999-001	SPECIAL NOTES	J13=1-2, 3-4	I	1.0
1	999-9999-001	SPECIAL NOTES	J19=5-6, 11-12, 13-14, 19-20, 21-22	I	1.0
1	999-9999-001	SPECIAL NOTES	J24=1-2, 3-4	I	1.0
1	999-9999-001	SPECIAL NOTES	J26=2-3	I	1.0

ASSM ITEM FROM: EBC-BXPLUS-700 ASSM ITEM THRU: EBC-BXPLUS-700
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
1	999-9999-001	SPECIAL NOTES	J27=2-3	I	1.0
TOP ASSEMBLY TOTAL: EBC-BXPLUS-700		ARLIN - 33 Items			

REPORT RECAP

0 WARNING(S)

PARAMETER RECAP

PARAMETER KEY : 10 BOM for Manuals
REPORT TITLE : Range on Parent Item

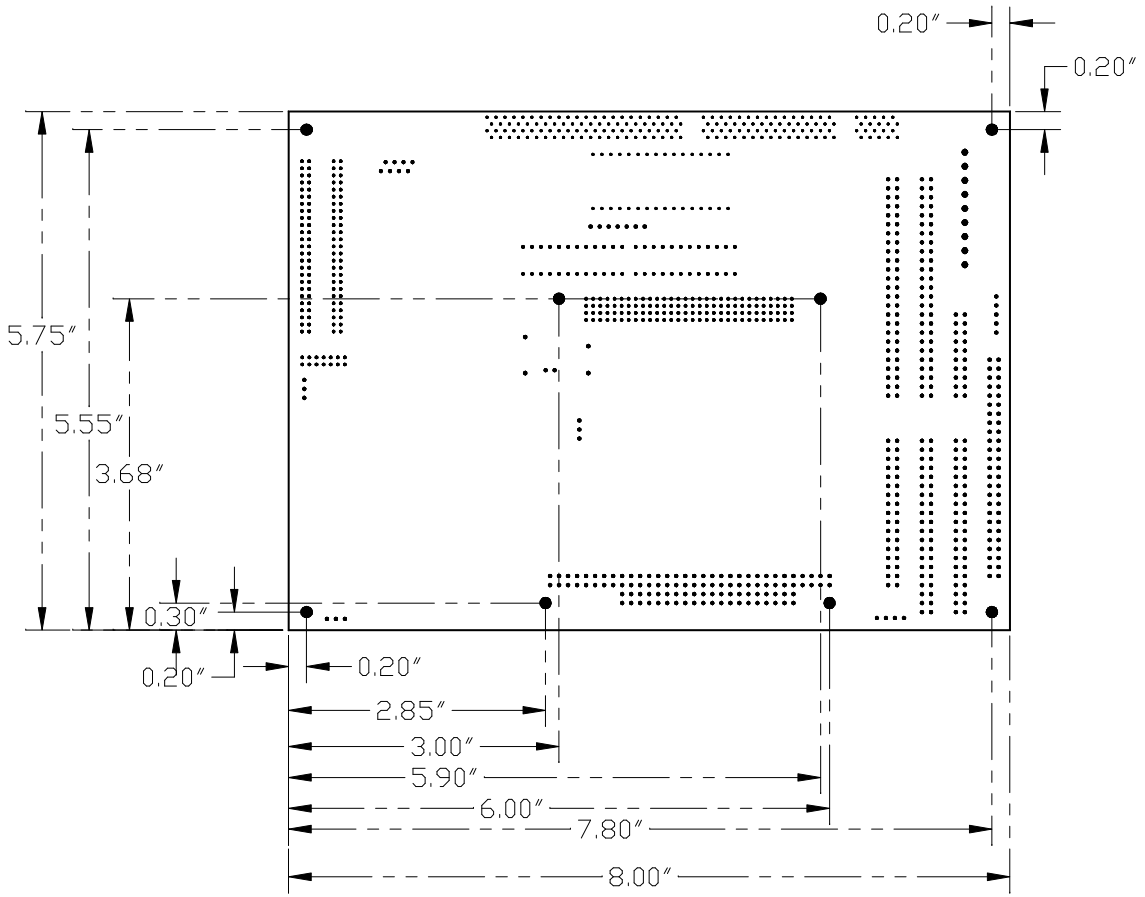
ASSM ITEM RANGE : EBC-BXPLUS-700 THRU EBC-BXPLUS-700 COSTING METHOD : A
PARENT LOC RANGE : <FIRST> THRU <LAST> QUANTITY TO EXPLODE : 1

```
PRODUCT KEY RANGE   : <FIRST>           THRU <LAST>           USE SCRAP FACTOR (Y/N) : N
COMMODITY KEY RANGE : <FIRST>           THRU <LAST>           UPDATE INV STD COST    : N
                                                              NO. LEVELS TO EXPLODE  : 999
DEFAULT COMP LOC    : ARLIN                                   COLUMNS OF DESC TEXT   : 42
BOM STATUS PRIORITY : A                                       SHORT OR LONG    (S/L) : S
                                                              PRINT ITEM DESC  (Y/N) : Y
```

10 APPENDIX E

EBC-BX Mechanical Drawing

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	CHANGED BY



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCE
FRACTIONS ANGLES +/- 1/2°
DECIMALS: .XX ± .03 .XXX ± .010

MACHINE FINISH:

CUSTOMER APPROVAL	DATE	
APPROVAL	DATE	
CHECKER	DATE	
DRAFT/DESIGN M.BROWNING	DATE 01/08/03	

WinSystems, Inc.
"THE STD BUS AUTHORITY"

EBC-BX
MOUNTING DIMENSIONS

SIZE	CAGE CODE	DWG NO.	REV
C	1AU87	EBCBX.DWG	A
SCALE	CAD ID: EBCBX.DWG		SHEET 1 OF 1

11 APPENDIX F

WS16C48 I/O Routines and Sample Program Listings

```
/* UIO48.H

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      or damage, real or consequential resulting from the usage of this
      source code. It is the user's sole responsibility to determine
      fitness for any considered purpose.
*/
/*************************************************************************
*     Name  : uio48.h
*
*     Project     : PCM-UIO48 Software Samples/Examples
*
*     Date  : October 30, 1996
*
*     Revision: 1.00
*
*     Author      : Steve Mottin
*
*************************************************************************
*
*     Changes :
*
*     Date        Revision    Description
*     ________    ________    ___________________________________________
*     10/30/96    1.00        Created
*
*************************************************************************
*/

#define RISING 1
#define FALLING 0

void init_io(unsigned io_address);
int read_bit(int bit_number);
void write_bit(int bit_number);
void set_bit(int bit_number);
void clr_bit(int bit_number);
void enab_int(int bit_number, int polarity);
void disab_int(int bit_number);
void clr_int(int bit_number);
int get_int(void);
```

```
/* UIO48.C

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*/
/*************************************************************************
*     Name  : uio48.c
*
*     Project     : PCM-UIO48 Software Samples/Examples
*
*     Date  : October 30, 1996
*
*     Revision: 1.00
*
*     Author      : Steve Mottin
*
*************************************************************************
*
*     Changes :
*
*     Date        Revision    Description
*     ________    ________    ___________________________________________
*     10/30/96    1.00        Created
*
*************************************************************************
*/

#include <dos.h>

/* This global holds the base address of the UIO chip */

unsigned base_port;

/* This global array holds the image values of the last write to each I/O
   ports. This allows bit manipulation routines to work without having to
   actually do a read-modify-write to the I/O port.
*/

unsigned port_images[6];

/*=======================================================================
*                              INIT_IO
*
*  This function take a single argument :
*
*
*  io_address  :    This is the base I/O address of the 16C48 UIO Chip
*                           on the board.
*
```

```
*
*  This function initializes all I/O pins for input, disables all interrupt
*  sensing, and sets the image values.
*
*=============================================================================*/

void init_io(unsigned io_address)
{
int x;

      /* Save the specified address for later use */

      base_port = io_address;

      /* Clear all of the I/O ports. This also makes them inputs */

      for(x=0; x < 7; x++)
            outportb(base_port+x, 0);

      /* Clear our image values as well */

      for(x=0; x < 6; x++)
            port_images[x] = 0;

      /* Set page 2 access, for interrupt enables */

      outportb(base_port+7,0x80);

      /* Clear all interrupt enables */

      outportb(base_port+8,0);
      outportb(base_port+9,0);
      outportb(base_port+0x0a,0);

      /* Restore normal page 0 register access */
      outportb(base_port+7,0);

}

/*=============================================================================
*
*                                READ_BIT
*
*
*  This function takes a single argument :
*
*
*  bit_number    :  The integer argument specifies the bit number to read.
*                   Valid arguments are from 1 to 48.
*
*  return value : The current state of the specified bit, 1 or 0.
*
*  This function returns the state of the current I/O pin specified by
*  the argument bit_number.
*
*=============================================================================*/

int read_bit(int bit_number)
{
unsigned port;
int val;
```

```
      /* Adjust the bit_number to 0 to 47 numbering */

      --bit_number;

      /* Calculate the I/O port address based on the updated bit_number */

      port = (bit_number / 8) + base_port;

      /* Get the current contents of the port */

      val = inportb(port);

      /* Get just the bit we specified */

      val = val & (1 << (bit_number % 8));

      /* Adjust the return for a 0 or 1 value */

      if(val)
            return 1;

      return 0;
}

/*========================================================================
*
*                                WRITE_BIT
*
* This function takes two arguments :
*
*
*  bit_number :  The I/O pin to access is specified by bit_number 1 to 48.
*
*  val  :   The setting for the specified bit, either 1 or 0.
*
*  This function sets the specified I/O pin to either high or low as dictated
*  by the val argument. A non zero value for val sets the bit.
*
*========================================================================*/

void write_bit(int bit_number, int val)
{
unsigned port;
unsigned temp;
unsigned mask;


      /* Adjust bit_number for 0 based numbering */

      --bit_number;

      /* Calculate the I/O address of the port based on the bit number */

      port = (bit_number / 8) + base_port;

      /* Use the image value to avoid having to read the port first. */

      temp = port_images[bit_number / 8]; /* Get current value */

      /* Calculate a bit mask for the specified bit */
```

```
      mask = (1 << (bit_number % 8));

      /* Check whether the request was to set or clear and mask accordingly */

      if(val)           /* If the bit is to be set */
            temp = temp | mask;
      else
            temp = temp & ~mask;

      /* Update the image value with the value we're about to write */

      port_images[bit_number / 8] = temp;

      /* Now actually update the port. Only the specified bit is affected */

      outportb(port,temp);
}

/*=========================================================================
*                                  SET_BIT
*
*
*  This function takes a single argument :
*
*  bit_number :  The bit number to set.
*
*  This function sets the specified bit.
*
*=========================================================================*/

void set_bit(int bit_number)
{

      write_bit(bit_number,1);
}

/*=========================================================================
*                                  CLR_BIT
*
*
*  This function takes a single argument :
*
*  bit_number :  The bit number to clear.
*
*  This function clears the specified bit.
*
*=========================================================================*/

void clr_bit(int bit_number)
{
      write_bit(bit_number,0);
}

/*=========================================================================
*
*                                ENAB_INT
*
*  This function takes two arguments :
*
*  bit_number  : The bit number to enable intterups for. Range from 1 to 48.
```

```
*
*  polarity   : This specifies the polarity of the interrupt. A non-zero
*               argument enables rising-edge interrupt. A zero argument
*               enables the interrupt on the flling edge.
*
*  This function enables within the 16C48 an interrupt for the specified bit
*  at the specified polarity. This function does not setup the interrupt
*  controller, nor does it supply an interrupr handler.
*
*=============================================================================*/

void enab_int(int bit_number, int polarity)
{
unsigned port;
unsigned temp;
unsigned mask;

      /* Adjust for 0 based numbering */

      --bit_number;

      /* Calculate the I/O address based uppon the bit number */

      port = (bit_number / 8) + base_port + 8;

      /* Calculate a bit mask based on the specified bit number */

      mask = (1 << (bit_number % 8));

      /* Turn on page 2 access */

      outportb(base_port+7,0x80);

      /* Get the current state of the interrupt enable register */

      temp = inportb(port);

      /* Set the enable bit for our bit number */

      temp = temp | mask;

      /* Now update the interrupt enable register */

      outportb(port,temp);

      /* Turn on access to page 1 for polarity control */

      outportb(base_port+7,0x40);

      /* Get the current state of the polarity register */

      temp = inportb(port);         /* Get current polarity settings */

      /* Set the polarity according to the argument in the image value */

      if(polarity)            /* If the bit is to be set */
            temp = temp | mask;
      else
            temp = temp & ~mask;

      /* Write out the new polarity value */
```

```
      outportb(port,temp);

      /* Set access back to Page 0 */

      outportb(base_port+7,0x0);

}

/*=========================================================================
*
*                               DISAB_INT
*
* This function takes a single argument :
*
* bit_number : Specifies the bit number to act upon. Range is from 1 to 48.
*
* This function shuts off the interrupt enabled for the specified bit.
*
*=========================================================================*/

void disab_int(int bit_number)
{
unsigned port;
unsigned temp;
unsigned mask;

      /* Adjust the bit_number for 0 based numbering */

      --bit_number;

      /* Calculate the I/O Address for the enable port */

      port = (bit_number / 8) + base_port + 8;

      /* Calculate the proper bit mask for this bit number */

      mask = (1 << (bit_number % 8));

      /* Turn on access to page 2 registers */

      outportb(base_port+7,0x80);

      /* Get the current state of the enable register */

      temp = inportb(port);

      /* Clear the enable bit int the image for our bit number */

      temp = temp & ~mask;

      /* Update the enable register with the new information */

      outportb(port,temp);

      /* Set access back to page 0 */

      outportb(base_port+7,0x0);

}
```

```
/*=============================================================================
*
*                                CLR_INT
*
*  This function takes a single argument :
*
*  bit_number : This argument specifies the bit interrupt to clear. Range
*               is 1 to 24.
*
*
*  This function is use to clear a bit interrupt once it has been recognized.
*  The interrupt left enabled.
*
*============================================================================*/

void clr_int(int bit_number)
{
unsigned port;
unsigned temp;
unsigned mask;


      /* Adjust for 0 based numbering */

      --bit_number;

      /* Calculate the correct I/O address for our enable register */

      port = (bit_number / 8) + base_port + 8;

      /* Calculate a bit mask for this bit number */

      mask = (1 << (bit_number % 8));

      /* Set access to page 2 for the enable register */

      outportb(base_port+7,0x80);

      /* Get current state of the enable register */

      temp = inportb(port);

      /* Temporarily clear only OUR enable. This clears the interrupt */

      temp = temp & ~mask;          /* clear the enable for this bit */

      /* Write out the temporary value */

      outportb(port,temp);

      /* Re-enable our interrupt bit */

      temp = temp | mask;

      /* Write it out */

      outportb(port,temp);

      /* Set access back to page 0 */

      outportb(base_port+7,0x0);
```

```
}


/*=========================================================================
*
*                                GET_INT
*
*  This function take no arguments.
*
*  return value : The value returned is the highest level bit interrupt
*                 currently pending. Range is 1 to 24.
*
*  This function returns the highest level interrupt pending. If no interrupt
*  is pending, a zero is returned. This function does NOT clear the interrupt.
*
*=========================================================================*/

int get_int(void)
{
int temp;
int x;

      /* read the master interrupt pending register, mask off undefined bits */

      temp = inportb(base_port+6) & 0x07;

      /* If there are no interrupts pending, return a 0 */

      if((temp & 7) == 0)
            return(0);

      /* There is something pending, now we need to identify what it is */


      /* Set access to page 3 for interrupt id registers */

      outportb(base_port+7,0xc0);

      /* Read interrupt ID register for port 0 */

      temp = inportb(base_port+8);


      /* See if any bit set, if so return the bit number */

      if(temp !=0)
      {
            for(x=0; x <=7; x++)
            {
                  if(temp & (1 << x))
                  {
                        outportb(base_port+7,0);      /* Turn off access */
                        return(x+1);            /* Return bitnumber with active
int */
                  }
            }
      }

      /* None in Port 0, read port 1 interrupt ID register */
```

```
	temp = inportb(base_port+9);

	/* See if any bit set, if so return the bit number */

	if(temp !=0)
	{
		for(x=0; x <=7; x++)
		{
			if(temp & (1 << x))
			{
				outportb(base_port+7,0);	/* Turn off access */
				return(x+9);		/* Return bitnumber with active
int */
			}
		}
	}

	/* Lastly, read status of port 2 int id */

	temp = inportb(base_port+0x0a);		/* Read port 2 status */

	/* If any pending, return the appropriate bit number */

	if(temp !=0)
	{
		for(x=0; x <=7; x++)
		{
			if(temp & (1 << x))
			{
				outportb(base_port+7,0);	/* Turn off access */
				return(x+17);		/* Return bitnumber with active
int */
			}
		}
	}

	/* We should never get here unless the hardware is misbehaving but just
	    to be sure. We'll turn the page access back to 0 and return a 0 for
	    no interrupt found.
	*/


	outportb(base_port+7,0);
	return 0;
}
```

```
/* FLASH.C

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      fitness for any considered purpose.
*/

#include <stdio.h>
#include <conio.h>
#include <dos.h>
#include "uio48.h"

/* This is where we have our board jumpered to */

#define BASE_PORT 0x120


/* This is an utlra-simple demonstration program of some of the functions
   available in the UIO48 source code library. This program simply sets and
   clears each I/O line in succession. It was tested by hooking LEDs to all
   of the I/O lines and wathching the lit one race through the bits.
*/

void main()
{
int x;


      /* Initialize all I/O bits, and set then for input */

      init_io(BASE_PORT);

      /* We'll repeat our sequencing until a key is pressed */

      while(!kbhit())
      {
            /* We will light the LED attached to each of the 48 lines */
            for(x=1; x <=48; x++)
            {
                  /* Setting the bit lights the LED */
                  set_bit(x);
                  /* The wait time is subjective. We liked 100mS */
                  delay(100);
                  /* Now turn off the LED */
                  clr_bit(x);
            }
      }
      getch();
}
```

```
/* POLL.C

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      fitness for any considered purpose.

*/

#include <stdio.h>
#include <conio.h>
#include "uio48.h"


#define BASE_PORT 0x120

/* This program uses the edge detection interrupt capability of the
   WS16C48 to count transitions on the first 24 lines. It does this
   however, no by using true interrupts but by polling for transitions
   using the get_int() function.

*/


/* Our transition totals are stored in this array */


unsigned int_counts[25];

/* Definitions for local functions */

void check_ints(void);

void main()
{
int x;


      /* Initialize the I/O ports.  Set all I/O pins to input */

      init_io(BASE_PORT);


      /* Initialize our transition counts, and enable falling edge
         transition interrupts.
      */

      for(x=1; x<25; x++)
      {
            int_counts[x] = 0;      /* Clear the counts */
            enab_int(x,FALLING);    /* Enable the falling edge interrupts */
```

```
	}

	/* Clean up the screen for our display. Nothing fancy */
	clrscr();

	for(x=1; x<25; x++)
	{
		gotoxy(1,x);
		printf("Bit number %02d ",x);
	}


	/* We will continue to display until any key is pressed */

	while(!kbhit())
	{

		/* Retrieve any pending transitions and update the counts */

		check_ints();

		/* Display the current count values */

		for(x=1; x < 25; x++)
		{
			gotoxy(16,x);
			printf("%05u",int_counts[x]);
		}
	}
	getch();
}

void check_ints()
{
int current;

	/* Get the bit number of a pending transition interrupt */

	current = get_int();

	/* If it's 0 there are none pending */

	if(current == 0)
		return;

	/* Clear and rearm this one so we can get it again */

	clr_int(current);

	/* Tally a transition for this bit */

	++int_counts[current];
}
```

```
/* INTS.C

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      or damage, real or consequential resulting from the usage of this
      source code. It is the user's sole responsibility to determine
      fitness for any considered purpose.

*/

#include <stdio.h>
#include <dos.h>
#include <conio.h>
#include "uio48.h"

#define BASE_PORT 0x120

/* This program like the poll.c sample uses the edge detection interrupt
   capability of the WS16C48 to count edge transitions. Unlike poll.c,
   however this program actually uses interrupts and update all of the
   transition counters in the background.

*/


/* Our transition totals are stored in this global array */

unsigned int_counts[25];

/* Function declarations for local functions */

void check_ints(void);
void interrupt int_handler(void);
void interrupt (*old_handler)(void);

void main()
{
int x;

      /* Initialize the I/O ports. Set all I/O pins to input */

      init_io(BASE_PORT);

      /* Install an interrupt handler for the board */


      /* We disable interrupts whenever we're changing the environment */

      disable();  /* Disable interrupts during initialization */

      /* Get the old handler and save it for later resoration */
```

```
    old_handler = getvect(0x72);    /* Hardwired for IRQ10 */

/* Install out new interrupt handler */

    setvect(0x72,int_handler);

  /* Clear the transition count values and enable the falling edge
     interrupts.
  */

  for(x=1; x<25; x++)
  {
        int_counts[x] = 0;      /* Clear the counts */
        enab_int(x,FALLING);    /* Enable the falling edge interrupts */
  }


  /* Unmask the interrupt controller */

    outportb(0xa1,(inportb(0xa1) & 0xfb));  /* Unmask IRQ 10 */

  /* Reenable interrupts */
  enable();


  /* Set up the display */

  clrscr();   /* Clear the Text Screen */

  for(x=1; x<25; x++)
  {
        gotoxy(1,x);
        printf("Bit Number %02d  ",x);
  }


  /* We will continuously print the transition totals until a
     key is pressed */


  /* All of the processing of the transition interrupts, including
     updating the counts is done in the background when an interrupt
     occurs.
  */

  while(!kbhit())
  {
        for(x=1; x < 25; x++)
        {
              gotoxy(16,x);
              printf("%05u",int_counts[x]);
        }
  }

  getch();

  /* Disable interrupts while we restore things */

  disable();

  /* Mask off the interrupt at the interrupt controller */
```

```
        outportb(0xa1,inportb(0xa1) | 0x02);    /* Mask IRQ 10 */

      /* Restore the old handler */

        setvect(0x72,old_handler);      /* Put back the old interrupt handler */

      /* Reenable interrupts. Things are back they way they were before we
         started.
    */

      enable();
}


/* This function is executed when an edge detection interrupt occurs */

void interrupt int_handler(void)
{
int current;

      /* Get the current interrupt pending. There really should be one
         here or we shouldn't even be executing this function.
    */

      current = get_int();

      /* We will continue processing pending edge detect interrupts until
         there are no more present. In which case current == 0
    */

      while(current)
      {

            /* Clear the current one so that it's ready for the next edge */

            clr_int(current);

            /* Tally up one for the current bit number */

            ++int_counts[current];

            /* Get the next one, if any others pending */

            current = get_int();
      }

      /* Issue a non-specific end of interrupt command (EOI) to the
         interrupt controller. This rearms it for the next shot.
      */

        outportb(0xa0,0x20);    /* Do non-specific EOI */
        outportb(0x20,0x20);
}
```



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4. Name, address, telephone and FAX number of the person making the request.
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