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OPERATIONS MANUAL
LPM / MCM - IO48/96/144

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TABLE OF CONTENTS

Paragraph Title	*Chapter-Page*
1 General Information	**1-1**
1 Features	1-1
2 General Description	1-1
3 Specifications	1-2
2 IO48/96/144 Technical Reference	**2-1**
1 Introduction	2-1
2 IO48/96/144 Chipset	2-1
3 Connector Pinout	2-2
4 I/O Map	2-3
5 Interrupt Routing	2-4
6 STD Bus Interface	2-5
7 Connector/Jumper Summary	2-6
Appendix A	**Parts Lists**
Appendix B	**Sample Code / Examples**
Appendix C	**Schematics**

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1 General Information

1.1 Features

- 48, 96, OR 144 Digital I/O pins per card.
- Extensive Interrupt Capabilities, bit selectable.
- Interrupt ID register for more efficient ISR's.
- Each pin capable of sinking 12ma for use with Opto modules.
- Read back / Input available for each pin.
- Write mask register allows write protection of selected ports.
- 50 Pin connector directly interfaces to Opto Racks.
- CMOS version available as LPM-IO48/96/144
- 5 volt only operation.
- 8-bit STD Bus interface

1.2 General Description

The IO48/96/144 is a low cost high density I/O card with extensive interrupt capabilities.

For a given configuration, half of the pins have interrupt capabilities. Interrupts are programmable on a bit-by-bit basis for enable, and edge polarity.

Board Name	Total I/O	With Interrupts
LPM/MCM-IO48	48	24
LPM/MCM-IO96	96	48
LPM/MCM-IO144	144	72

All lines are Open Collector I/O. In addition, each group of 48 lines has a six bit Write Mask register which allows the user to disable writes on a byte wide basis.

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1.3 Specifications

1.3.1 Electrical

Bus Interface: STD-Bus & CMOS STD-Bus compatible.

			No Load LPM / MCM	I/O Pins
VCC	+5V	@	0.014mA / 0.090mA	144
			0.013mA / 0.089mA	96
			0.012mA / 0.088mA	48

1.3.2 Memory

Addressing: 12-bit, 10-bit, or 8-bit, with or without IOEXP, Jumper selectable.

I/O Space: Each 48 line group occupies 8 ports for normal I/O or 16 ports when interrupts are available. Please note that these cards may only be mapped with base addresses starting on 32 port boundaries for 8 port mode, or 64 port boundaries for 16 port mode.

1.3.3 Mechanical

Dimensions: 4.5 x 6.5

PC Boards: FR-4 epoxy glass with 2 signal layers, 2 power planes, screened component legend, plated through holes and gold plated edge fingers.

Jumpers: .025" square posts on 0.1" centers.

Connectors: Six 2 x 25 .1" spaced shrouded male IDH connectors with .025" square pins.

1.3.4 Environmental

Operating Temperature -40° to 85° C (LPM)
0° to 65° C (MCM)

Non-condensing Humidity: 5 to 95%

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2 IO48/96/144 Technical Reference

2.1 Introduction

This section of the manual is intended to provide sufficient information for the configuration and usage of the LPM / MCM-IO48/96/144 board. WinSystems® also maintains a support group to help answer questions regarding configuration, usage, or programming of this board. Contact Technical support at (817) 274-7553 between 8A.M. and 5P.M. Central Time.

2.2 IO48/96/144 Chipset

The IO48/96/144 board uses the WS16C48 single-chip I/O. This WinSystems exclusive device has many state-of-the-art features which greatly enhance performance.

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2.3 Connector Pinout

Connectors J1 through J6 are used to connect the IO48/96/144 to the outside world. These connectors are .1" spaced 2x25 pin shrouded headers with .025" square posts, compatible with IDC female headers.

Signal	Pin	No.	Signal
I/O 23	1	2	GND
I/O 22	3	4	GND
I/O 21	5	6	GND
I/O 20	7	8	GND
I/O 19	9	10	GND
I/O 18	11	12	GND
I/O 17	13	14	GND
I/O 16	15	16	GND
I/O 15	17	18	GND
I/O 14	19	20	GND
I/O 13	21	22	GND
I/O 12	23	24	GND
I/O 11	25	26	GND
I/O 10	27	28	GND
I/O 9	29	30	GND
I/O 8	31	32	GND
I/O 7	33	34	GND
I/O 6	35	36	GND
I/O 5	37	38	GND
I/O 4	39	40	GND
I/O 3	41	42	GND
I/O 2	43	44	GND
I/O 1	45	46	GND
I/O 0	47	48	GND
5 VOLTS	49	50	GND

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2.4 I/O Map

Each group of 48 lines has 20 registers accessible through 16 ports as follows:

IA1	IA0	Port	D7	D6	D5	D4	D3	D2	D1	D0
x	x	0	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
x	x	1	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
x	x	2	I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16
x	x	3	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
x	x	4	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
x	x	5	I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16
x	x	6	0	0	0	0	0	IRQ2	IRQ1	IRQ0
x	x	7	**IA1**	**IA0**	Mask 5	Mask 4	Mask 3	Mask 2	Mask 1	Mask 0
0	0	8	0	0	0	0	0	0	0	0
0	0	9	0	0	0	0	0	0	0	0
0	0	A	0	0	0	0	0	0	0	0
0	1	8	Pol 7	Pol 6	Pol 5	Pol 4	Pol 3	Pol 2	Pol 1	Pol 0
0	1	9	Pol 15	Pol 14	Pol 13	Pol 12	Pol 11	Pol 10	Pol 9	Pol 8
0	1	A	Pol 23	Pol 22	Pol 21	Pol 20	Pol 19	Pol 18	Pol 17	Pol 16
1	0	8	Ena 7	Ena 6	Ena 5	Ena 4	Ena 3	Ena 2	Ena 1	Ena 0
1	0	9	Ena 15	Ena 14	Ena 13	Ena 12	Ena 11	Ena 10	Ena 9	Ena 8
1	0	A	Ena 23	Ena 22	Ena 21	Ena 20	Ena 19	Ena 18	Ena 17	Ena 16
1	1	8	P/C 7	P/C 6	P/C 5	P/C 4	P/C 3	P/C 2	P/C 1	P/C 0
1	1	9	P/C 15	P/C 14	P/C 13	P/C 12	P/C 11	P/C 10	P/C 9	P/C 8
1	1	A	P/C 23	P/C 22	P/C 21	P/C 20	P/C 19	P/C 18	P/C 17	P/C 16

Ports 0-2 correspond to the odd numbered connector (I.E. J1), Ports 3-5 correspond to the even numbered connector (I.E. J2). Ports 0-5 can always be read, but can be blocked from writes by the Mask bits. (Below). Please note that all pins are inverted, so that 0 volts = 1 and 5 volts = 0. This applies to drive and read-back. This means that in order for a pin to be an input, you should write a zero to it to turn off the drive. A switch from the pin to GND will then show a reading of 1 for that pin when the switch is closed. A zero read-back means the pin is floating at 5 volts. The built in pull-up resistors assure that an unconnected pin returns 0.

IRQ2-0: Interrupt I.D. bits. IRQ2-0 indicate an interrupt(s) from I/O Port(s) 2-0 respectively.

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2.4 I/O Map (Cont.)

Mask 0-5: Write Mask bits, when these bits are set, they disable writes to I/O Ports 0-5 respectively. Note: ONLY Ports 0-5 are affected. These bits have no influence on any of the other ports.

IA1-IA0: Internal Address bits. These bits provide a window into the register array for the interrupt portion of the chip. They are configured by a write to the two most significant bits of port 7. These two bits determine the access available through ports 8-10. Zero has no write function, and always reads zeroes. It is recommended that all routines that deal with interrupt configuration registers return IA1-IA0 the zero, to prevent accidental writes.

Note for IRQ0-3, Pol 0-23, Ena 0-23, P/C 0-23: All of these registers apply to the odd numbered connector(s) only, and are associated with the I/O 0-23 of ports 0-2. For all of these, Ports 8-10 correspond directly to Ports 0-2, bit for bit.

Pol 0-23: These bits determine the edge polarity of the interrupt, if the interrupt is enabled (see Ena 0-23). For each of these bits, a zero indicates that the corresponding pin will produce an interrupt on the rising edge. (Pin switching from 0 volts to 5 volts). Please note that upon receiving the interrupt, the I/O port address will have a ZERO for this bit. Conversely, a one in the Pol register will produce an interrupt on the falling edge, with a one at the I/O port.

Ena 0-23: These bits determine whether or not a pin will produce an interrupt. Setting a bit to 1 will enable the interrupt for the corresponding pin. Note: clearing the enable bit also clears the Pending bit. You may clear individual bits in a Pending register by toggling the corresponding enable bit.

P/C 0-23: Pending / Clear bits. Reading these registers gives you the interrupt(s) pending. Writing any value clears that byte. I.E., any output to register 8 will clear all bits in register 8. These bits are latched by the event, so that even a short duration pulse will be recognized. See Ena 0-23 above for information on clearing individual bits.

All 20 registers are set to all zero's with System Reset (STD-BUS pin 47).

2.5 Interrupt Routing

The IO48/96/144 has only one interrupt output, regardless of how many points are available. This pin must be routed to the appropriate back plane interrupt with J10. The pinout of J10 is shown below.

Jumper 1-2 for STD-BUS pin 44.
Jumper 3-4 for STD-BUS pin 37.
Jumper 5-6 for STD-BUS pin 50.
Jumper 7-8 for STD-BUS pin 46.

	Pin No.		
44	1	2	IRQ
37	3	4	IRQ
50	5	6	IRQ
46	7	8	IRQ

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2.6 STD Bus Interface

The IO48/96/144 is designed for use in STD-Bus systems. The specifics are defined by jumpers on J7, J8, J9, and J11.

J7: Base Address Select. This value will be added to the Port number to give the actual address of a given port. For instance a base address of 100h gives Port 7 an actual address of 107h.

A jumper installed is a zero.
A jumper installed for IOEXP = /IOEXP.
Example: 100h, IOEXP High or Ignored, W/WO Extended 12 bit addressing;
3-4,5-6,7-8,11-12,13-14, (15-16 if 8 port mode, see J8)
Extended 12 bit addressing quadruples your usable I/O space. Please note that you should still restrict the lower 10 bits to addresses usable by your system, as only 10 bits of address decode exist on most IBM compatible peripherals & chipsets.

Signal	Pin	No.	Signal
GND	1	2	IOEXP
GND	3	4	A11
GND	5	6	A10
GND	7	8	A9
GND	9	10	A8
GND	11	12	A7
GND	13	14	A6
GND	15	16	A5

J8: Interrupt access. This jumper is factory set at 16. If you wish to give up the interrupt functions, and only occupy 8 ports per chip you may do so with this jumper and J11

Signal	Pin	No.	Signal
A3	1	2	mux0
mux1	3	4	A4
A5	5	6	N/C

16 Port mode with Interrupts: 2-4,3-5.
8 Port mode without Interrupts: 1-2,3-4.

J9: Addressing mode select. Choose from 8 bit, 8 bit W/IOEXP (Hi or Lo), or 10 bit. Also select 8 Port or 16 Port mode.

Signal	Pin	No.	Signal
IOEXP	1	2	Enabled
A11	3	4	Enabled
A10	5	6	Enabled
A9	7	8	Enabled
A8	9	10	Enabled
A5	11	12	Enabled

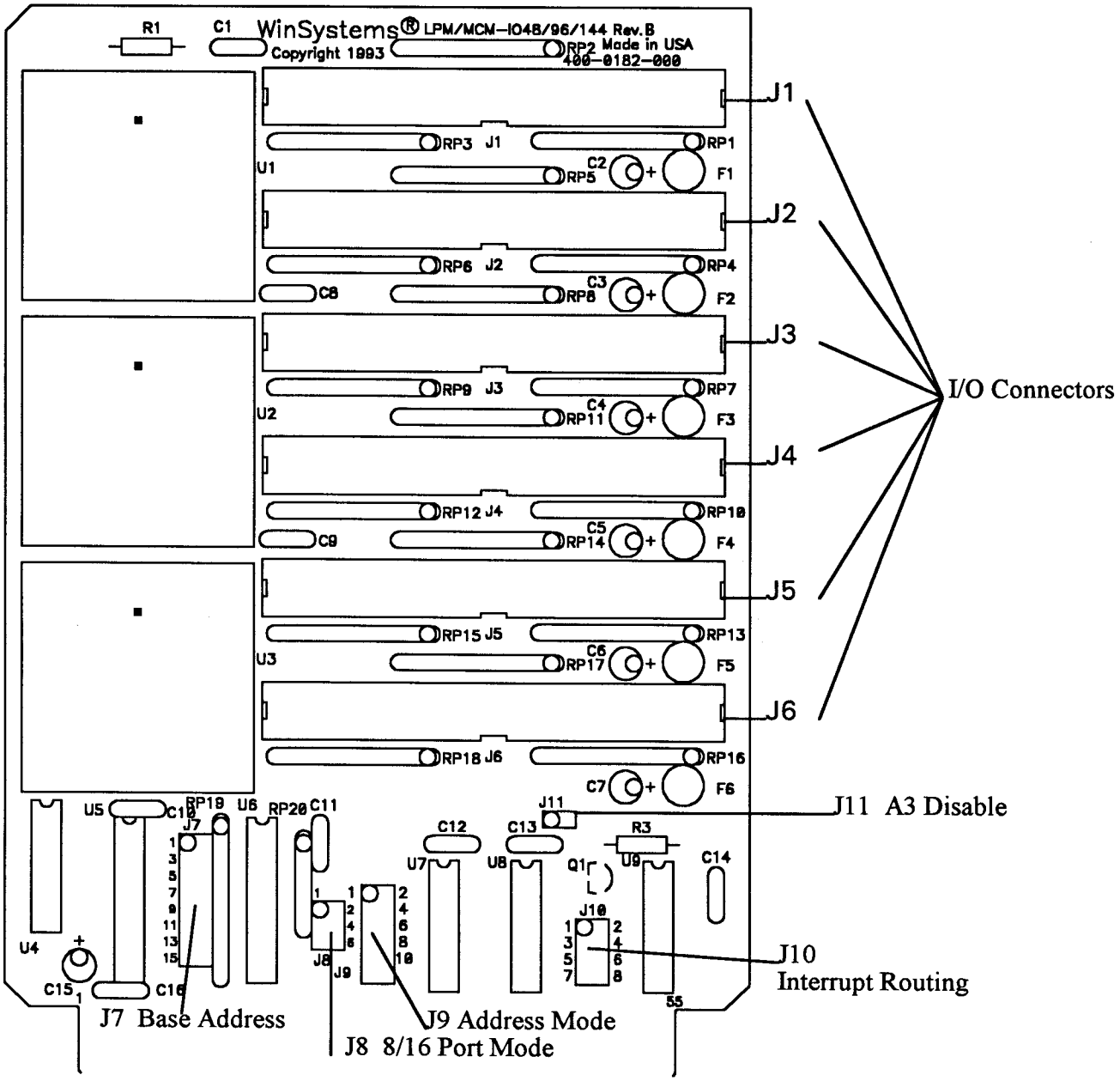
Jumper 1-2 to enable IOEXP.
Jumper 3-4 & 5-6 to expand address decode to 12 Bits. Care must be exercised in selecting the lower 10 bits, as IBM compatible peripherals and chipsets only decode 10 bits.
Jumper 7-8,9-10 to enable 10 Bit addressing.
Jumper 11-12 to enable A5 (8 port mode only).
Using IOEXP with 10 Bit addressing is not supported.

J11: Interrupt Access. This jumper is factory set for 16 Port mode, but may be installed for 8 Port mode (See J8 Above).

J11 Installed: 8 Port mode.
J11 Open: 16 Port mode.

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2.7 Connector/Jumper Summary



Connector:	Page	Description:
J1-6	2-2	Input / Output Connectors
J7	2-5	Base Address Select
J8	2-5	8/16 Port Mode Select
J9	2-5	Addressing Mode Select
J10	2-4	Interrupt Routing Jumper
J11	2-5	A3 Disable for 8 Port Mode

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Appendix A IO48/96/144 Parts Lists

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Appendix B Sample Code / Examples

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Example: Set J1 for input, J2 for output, (J1 & J2 are on the first chip.)

```
Pseudo - code:
out base+7,0   /* Clear the Write Mask Register so we can access ports 0-5 */
out base,0     /* Clear ports 0 through 5*/
out base+1,0
out base+2,0
out base+3,0
out base+4,0
out base+5,0
out base+7,7   /* Set the write mask bits to protect ports 0-2 */
readval = inp base     /* values are now read with an I/O Read operation. Pin tied to
                          Ground will return a bit set in this result */
out base+3,writeval    /* Values are now written with an I/O Write operation.  */
check = inp(base+3)    /* Since an I/O Read operation returns the value of the PIN, it
                          is possible to see if another device is driving this output line,
                          such as a manual override. */
```

Example: Reset all registers in the 1st chip.

```
Pseudo - Code
out base+7,0                          /* Clear Write Mask Register */
a = 0 to 5:out base+a,0                    /* Write zeroes to ports 0 through 5 */
a = 1 to 3:{
        out base+7,(a) shifted left 6 times    /* Sequence IA1,IA0 from 1 to 3 with (a) */
        b=0 to 2: out base+b+8,0               /* for each value of a, write zeroes to ports
                                                  8-10 */
 }
out base+7,0                          /* Clear write mask register & IA1,IA0 */
```

Microsoft C (argument passed into chp is the chip number to be cleared, 0-2 = U1-U3)

Note: <<*n* means shift left by *n* places.

basadd is a global variable set to the base address.

```
void clrchp(unsigned int chp)
{
unsigned int a;
        outp(basadd+(chp<<4)+7,0);              /* Set all regs to writeable */
        for(a=0; a<6; a++)                      /* Clear I/O ports 0-5 */
                outp(basadd+(chp<<4)+a,0);      /* (chp<<4) assumes 16 port mode */
        for(a = 1; a < 3; a++)                  /* clear interrupt control registers */
        {       /* a<<6 moves the values 1 through 3 into position for IA1 & IA0 */
                outp(basadd+(chp<<4)+7,(a<<6)); /* choose pol/ena/pnd registers */
                for(b=0; b<3; b++)
                        outp(basadd+(chp<<4)+b+8,0);      /* Zero each one */
        }
        outp(basadd+(chp<<4)+7,0);              /* Return IA1-IA0 to zero. */
}
```

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Example: Set Interrupt enable for J1 pin 41, and set polarity for it to falling edge.

Pin 41 of J1 is accessed for I/O from port 0, bit 3. It is mapped into the interrupt control registers at port eight. Generally speaking, you should set the polarity first. For falling edge polarity, the polarity bit must be set. Two to the third power is sixteen, so to set bit 3 you could use the following pseudo code.
All values are in base 10 (decimal) for simplicity.

```
out base + 7, 64        /* set IA1 & IA0 to point to the polarity registers. */
out base + 8,16         /* set bit 3 in port zero's interrupt polarity register. */
out base + 7,128        /* set IA1 & IA0 to point to the Enable registers. */
/* Note: you should have initialized your ISR and the appropriate Interrupt Vectors at this
point. You will also need to unmask the interrupt in the 8259 equivalent if you are using a
PC-STD system. */
out base + 8,16         /* set bit 3 in port zero's interrupt enable register. */
out base + 7,0          /* set IA1-IA0 to 0, or use 192 instead to point to Pend/Clear */
```

At this point, the hardware interrupt is live, and your ISR will need to check it. Your ISR may read port 6 and get the port number Interrupting. In this case, 0. You may then set port 7's upper two bits to 3 and read the Pending bits from port 8. In this example, you would get 16.

```
int port = input base + 6       /* Port Number, 0-2 */
a = input base + 7              /* Read Mask */
out base + 7, a or 192          /* Make sure we point to Pending regs. */
int bits = input base + 8       /* int bits will contain a 1 bit for each bit pending */
out base + 8,0                  /* Data doesn't matter, writing to Pending Register clears all
                                        Pending bits. */
out base + 7, a                 /* Put it back the way we found it */
```

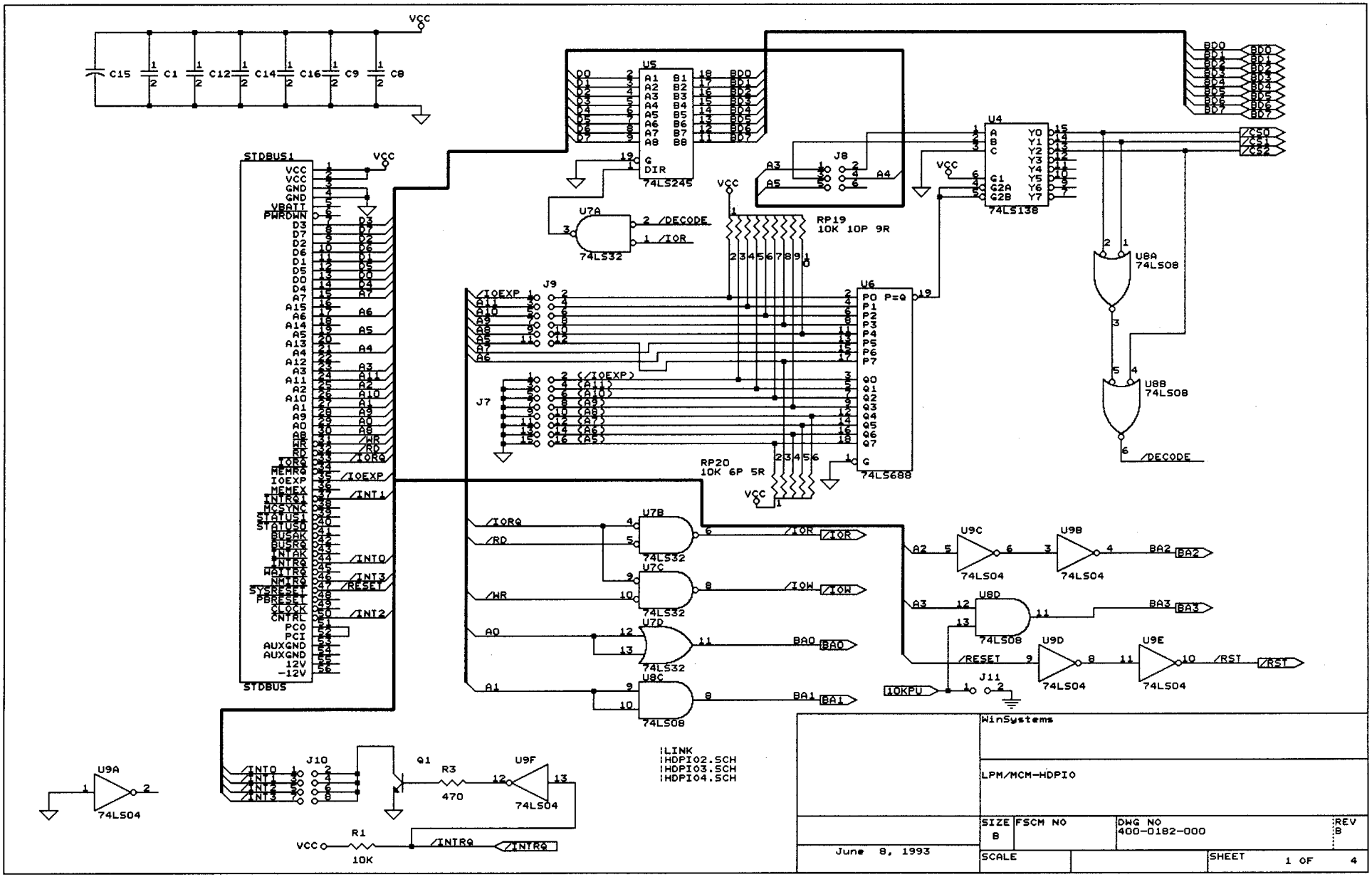
It is recommended that the read from the pending register by immediately followed by a write to clear it. This minimizes the chance of missing an interrupt due to multiple interrupts occurring close together.

For simplicity, most of the preceding examples are for a single chip board, however, you may use these same routines for multi-chip/multi-board systems by simply adding 8 or 16 to the address for each chip used. Whether you add 8 or 16 depends on how that particular board is configured (8 Port I/O only, or 16 Port I/O w/Interrupts).

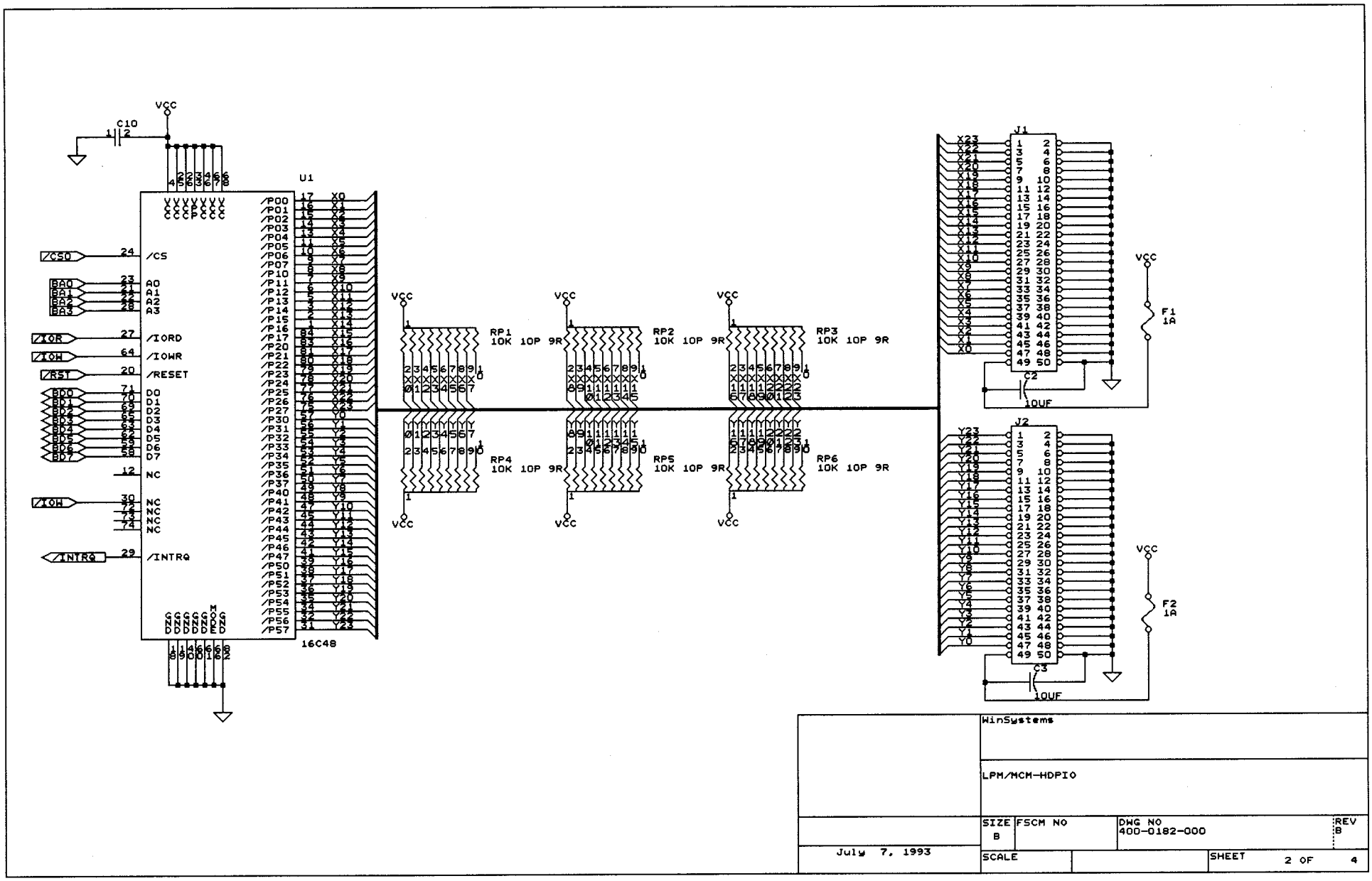
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Appendix C Schematics

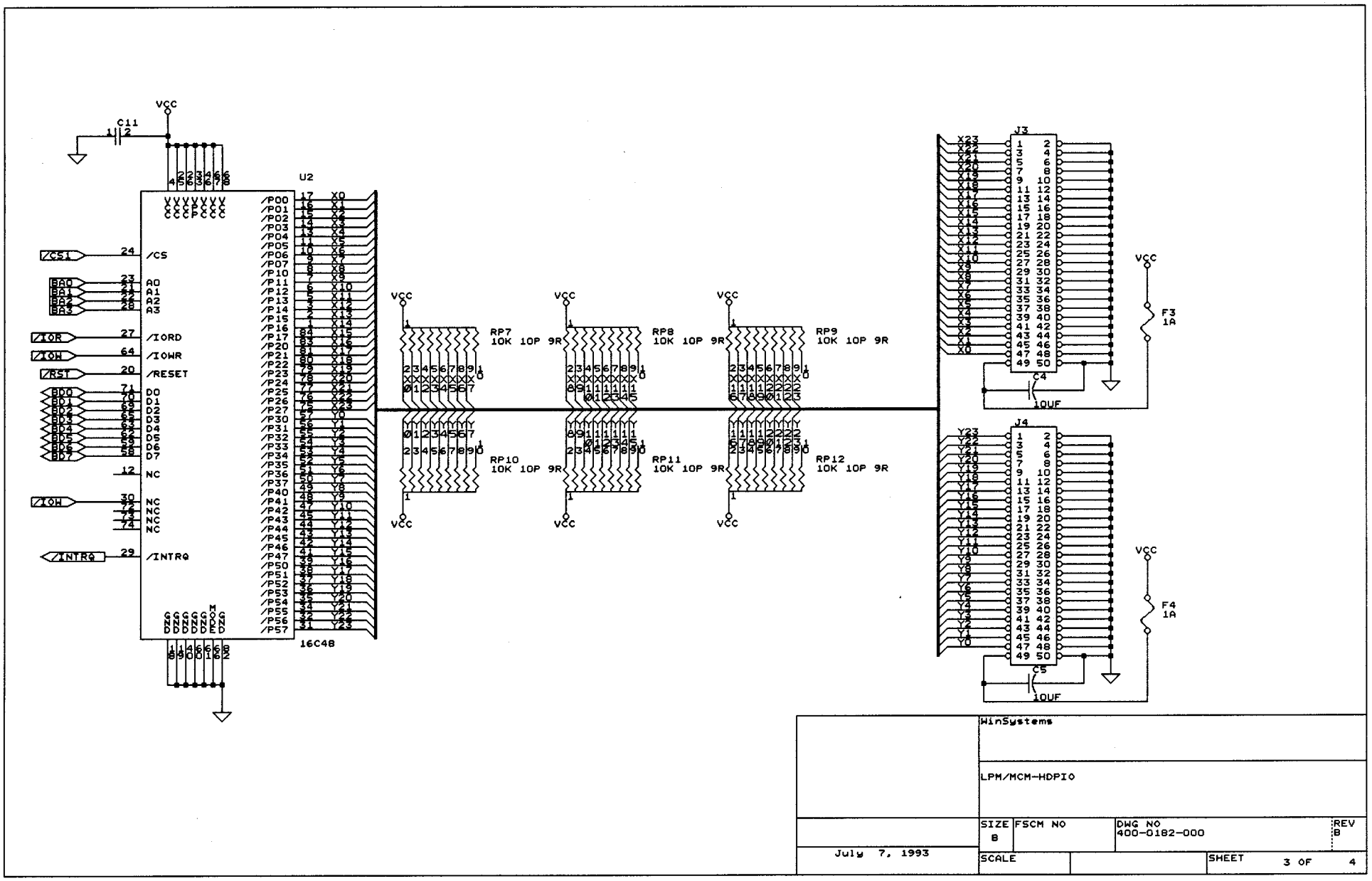
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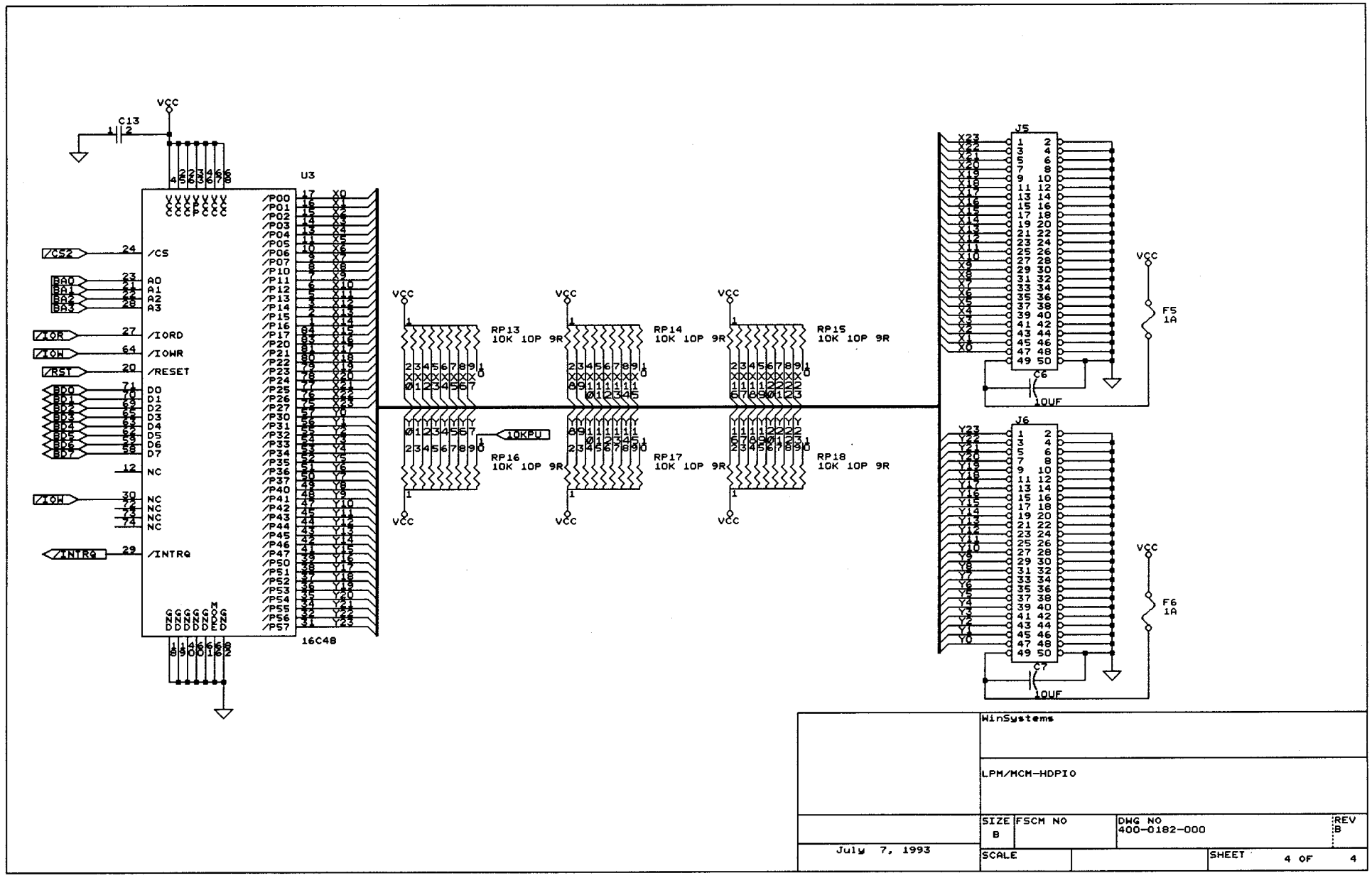


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2. Reason for the return.
3. Invoice number and date of purchase (if available), and original purchase order number.
4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

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The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.

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