OPERATIONS MANUAL
PCM-A/D-16
PCM-A/D-12

REVISION HISTORY

P/N 403-0230-000

ECO Number	Date Code	Rev Level
Originated	960206	B
97-31	970513	B1

TABLE OF CONTENTS

1 GENERAL INFORMATION

1.1 Features

- Low Power/Low Cost PC/104 A/D Converter Module
- 16 Single ended or 8 Differential input channels
- Available in 12-Bit or 16-Bit models
- 30uS Auto Conversion Time
- Interrupt available on end of conversion
- Input ranges of 0-5V and +/-10V
- Output format in straight Binary or Signed two's complement Binary
- Extended industrial operating temperature range
- Optional DC/DC converter for +5V only operation

1.2 General Description

The PCM-A/D-16 and PCM-A/D-12 are low cost, general purpose, successive approximation analog-to-digital converters. The PCM-A/D-16 uses the Burr-Brown ADS7807 16-bit converter while the PCM-A/D-12 uses the Burr-Brown ADS7806 12-bit converter. Appendix C contains the datasheet reprints on these components.

The PCM-A/D supports 16 channels in a unipolar 5V range, or a bipolar +/-10 volt range. Alternately 8 channels of differential input is supported in a 5 volt or 10 volt range. Repetitive channel conversion time is 25uS and random channel access time is 30uS. The end of conversion can be determined via software polling or by an interrupt to the CPU.

1.3 Specifications

1.3.1 Electrical

Bus Interface : PCM-A/D-XX-8 PC/104 8-Bit stackthrough
PCM-A/D-XX-16 PC/104 16-Bit stackthrough

Power requirements :

+5V +/- 5% at 200mA typ. with DC-DC converter installed
15mA typ. w/o DC-DC converter installed

+12V +/-5% at 5mA typ. w/o DC-DC converter installed

-12V +/-5% at 5mA typ. w/o DC-DC converter installed

1.3.2 Mechanical

Dimensions : 3.6" X 3.8" X 0.6"

PC Board : FR4 Epoxy glass with 2 signal layers and 2 power planes with screened component legend and plated through holes.

Jumpers : 0.025" square posts on 0.10" centers.

Connectors :
Analog input : 16-pin 0.10" grid RN type IDH-26-LP

1.3.3 Environmental

Operating Temperature : -40° C to +85° C

Non-condensing relative humidity : 5% to 95%

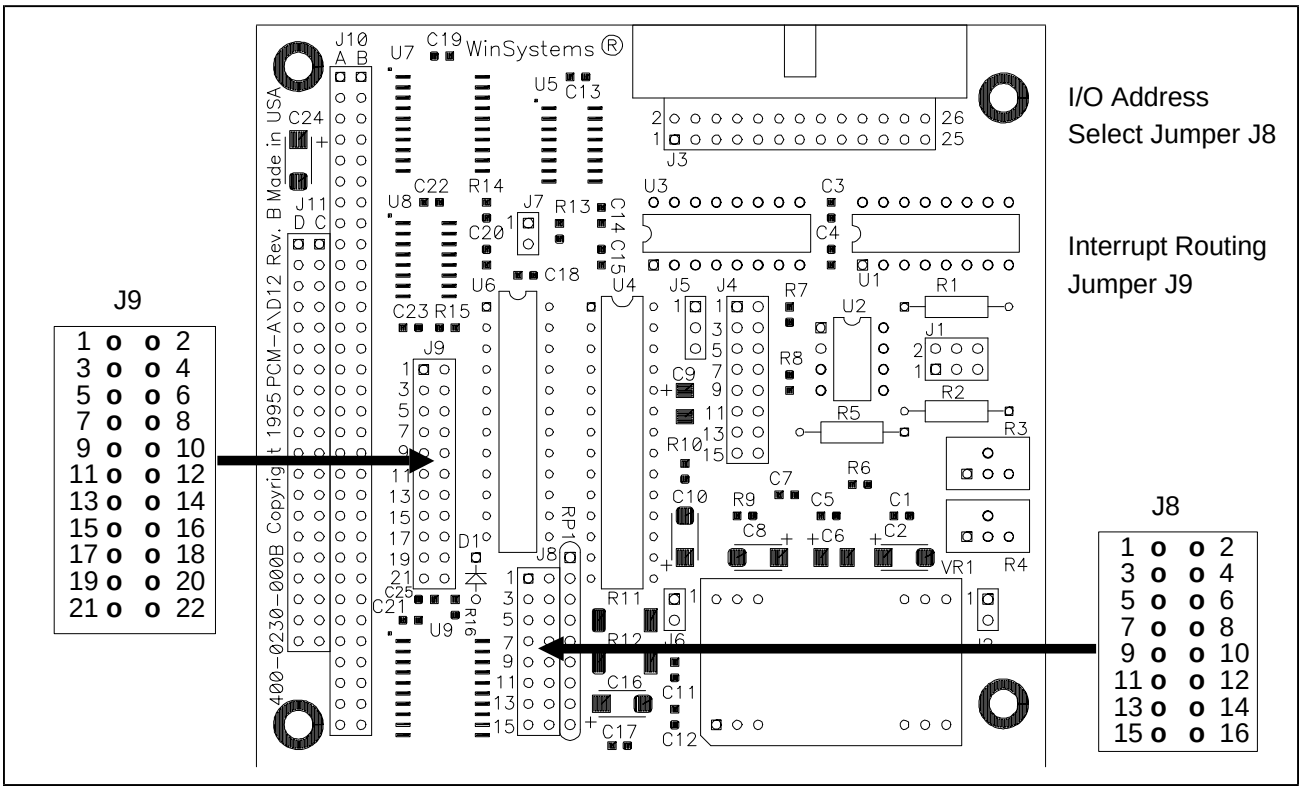
2 PCM-A/D Technical Reference

2.1 Introduction

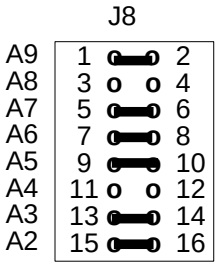
This section of the manual is intended to provide sufficient information regarding configuration and usage of the PCM-A/D-16 and PCM-A/D-12 modules. WinSystems maintains a Technical Support Group to help answer questions regarding configuration and programming of the board. For answers to questions not adequately addressed in this manual contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time. Technical Support may also be requested by FAX at (817) 548-1358.

The PCM-A/D has 16 single-ended inputs or 8 differential inputs and converts in 25-30uS. The end of conversion can be determined in any of three ways. A software timed delay of 30-35uS can be used, the status register can be polled, or an end of conversion interrupt can be used.

2.2 I/O Address Selection



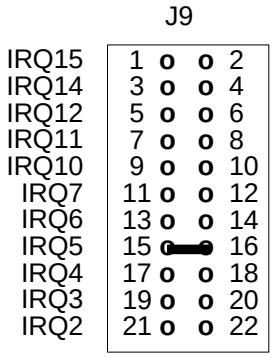
The PCM-A/D uses four consecutive I/O addresses with the base address determined by the setting of the jumpers on J8. Each position on the J8 jumper corresponds to an address bit. A jumper installed matches a '0' in the address and a jumper left open matches a '1' in the address. The illustration below shows the relationship between jumper positions and address bits and also shows the correct jumpering for a base I/O address of 110H.



BASE I/O ADDRESS 110H

2.3 Interrupt Routing

The end of conversion interrupt may be routed to any unused PC/104 interrupt line using the jumper block at J9. The illustration below shows the relationship between the jumper position and the interrupt selected. A sample jumpering for IRQ5 is also shown.



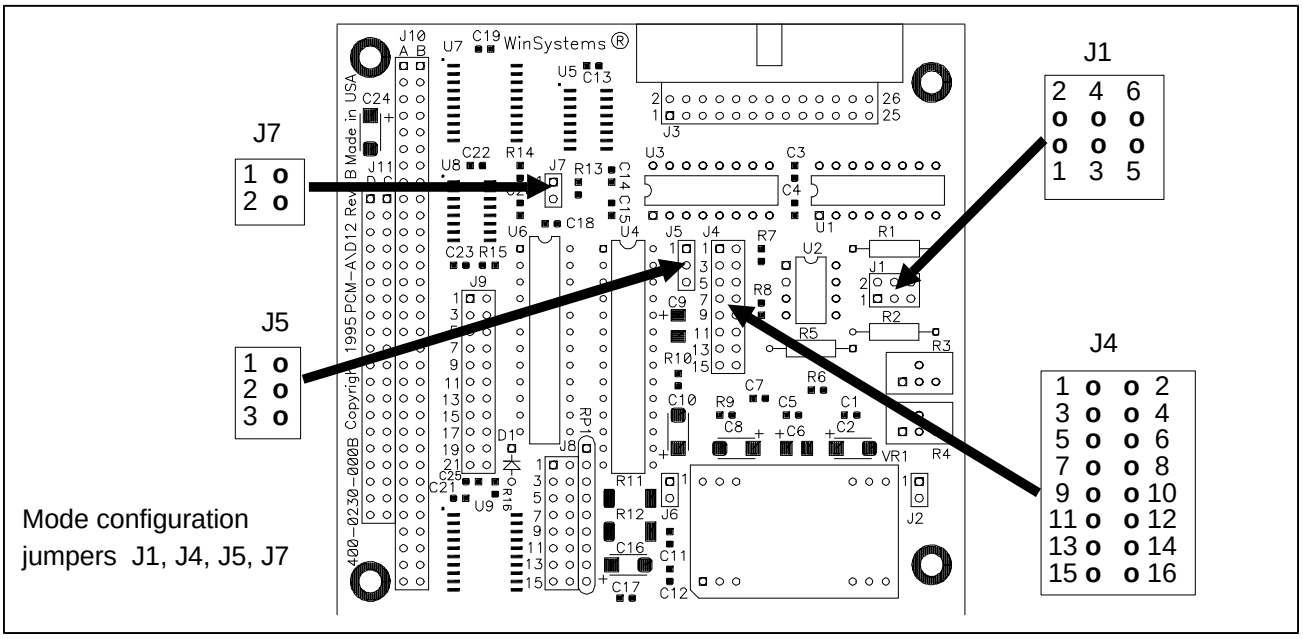
INTERRUPT ROUTING - IRQ5

2.4 DC-DC Converter Selection

To allow for slightly better linearity across the full +/-10V input range supported, an optional DC-DC converter is populated at VR1. When installed, it provides +15V and -15V to the analog circuitry. This allows the board to function with a +5 volt only supply. Jumper blocks at J2 and J6 are jumpered to route the +12 and -12 volts from the PC/104 bus to the analog circuitry when the DC-DC converter is not installed.

WARNING: The J2 and J6 jumpers should NEVER be installed when the DC-DC converter is installed or damage to the PCM-A/D board, other PC/104 modules, the CPU board, or the power supply may result. Boards provided with DC-DC converters from the factory will not have the jumper posts installed at J2 and J6.

2.5 Input Mode Selection



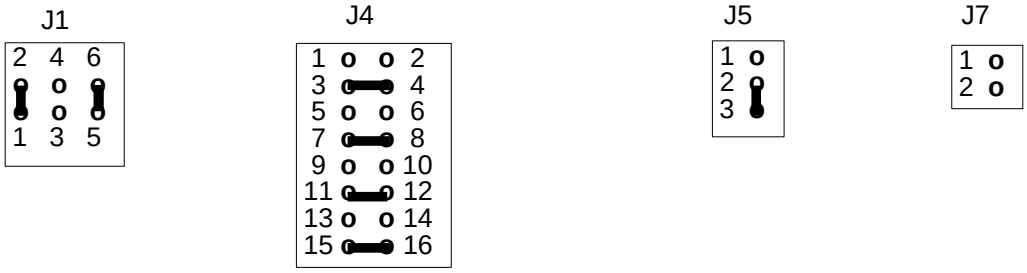
The PCM-A/D is jumper selectable for one of 4 input modes. The supported modes are.

1. 16 single-ended unipolar channels of 0-5V
2. 16 single-ended bipolar channels of +/-10V
3. 8 differential channels of 0-5V
4. 8 differential channels of +/-10V

2.5.1 **Mode 1** - 0-5V Single-Ended Unipolar

This input mode provides for 16 channels of 0-5 volt input range. In no case should the input be driven negative in this mode. The correct jumpering for this mode is shown below :

Each channel's input is delivered at J3. Refer to section 2.6 for input pin definitions.



0-5 Volt - Single-Ended Mode

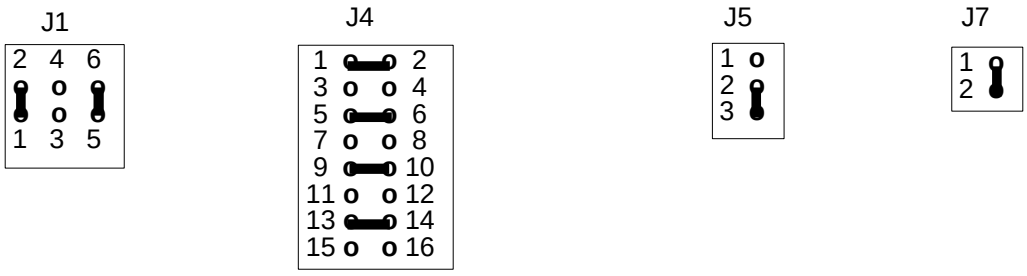
When used in mode 1, binary values from 0 to FFF0H (FFFFH) are read from the converter according to the following table.

Full Scale Range:	0.0 - 5.0 Volts	
Least Significant Bit (LSB) :	76uV (16-Bit) or 1.22mV (12-Bit)	
+Full Scale (FS-1LSB) :	4.999924V (16-Bit) or 4.99878V (12- Bit)	FFFFH
Midscale :	2.50V	8000H
One LSB Below Midscale :	2.4999924V(16-Bit) or 2.49878(12-Bit)	7FFFH
-Full Scale :	0.0V	0000H

NOTE : On the PCM-A/D-12 the lower nibble of the hex value will always be 0.

2.5.2 **Mode 2** - +/-10V Single-Ended Bipolar

This input mode provides for 16 channels of +-10V input range. The correct jumpering for this mode is shown below :



+/-10 Volt - Single Ended Bipolar Mode

Each channel's input is connected to J3. Refer to section 2.6 for input pin definitions.

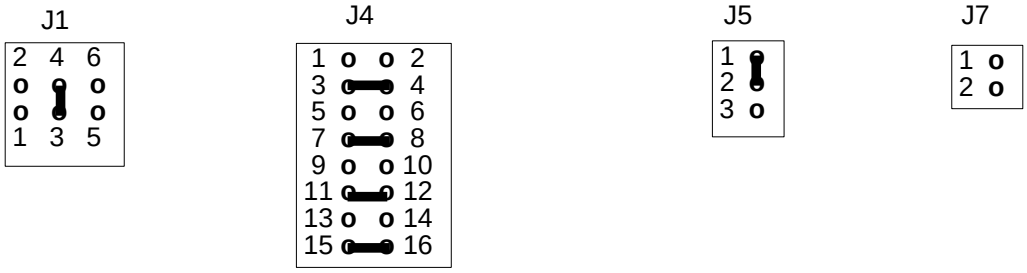
When used in mode 2, two's complement binary values from 8000H to 7FFFH are read from the converter according to the following table.

Full Scale Range :	+/-10.0V	
Least Significant bit :	305uV (16-Bit) or 4.88mV (12-Bit)	
+Full Scale (FS-1LSB) :	9.999695V (16-Bit) or 9.99512 (12-Bit)	7FFFH
Midscale :	0.0V	0000H
One LSB below Midscale :	-305uV (16Bit) or -4.88mV (12-Bit)	FFFFH
-Full Scale :	-10.0V	8000H

NOTE: On the PCM-A/D-12 the lower nibble of all hex values will be 0.

2.5.3 **Mode 3** - 0-5V Differential

This input mode provides for 8 channels of 0-5volt differential input. The correct jumpering for this mode is shown below :



0-5 Volt - Differential Mode

Each channel's input is connected to J3. Refer to section 2.6 for the input pin definitions.

When used in mode 3, binary values range from 0 to FFFFH as shown in the following table.

Full Scale Range :	0.0 - 5.0 Volts	
Least Significant Bit (LSB) :	76uV (16-Bit) or 1.22mV (12-Bit)	
+Full Scale (FS-1LSB) :	4.999924V(16-Bit) or 4.99878V (12- Bit)	FFFFH
Midscale :	2.50V	8000H
One LSB Below Midscale :	2.4999924V(16-Bit) or 2.49878(12-Bit)	7FFFH
-Full Scale	0.0V	0000H

NOTE : On the PCM-A/D-12 the lower nibble of the hex value will always be 0.

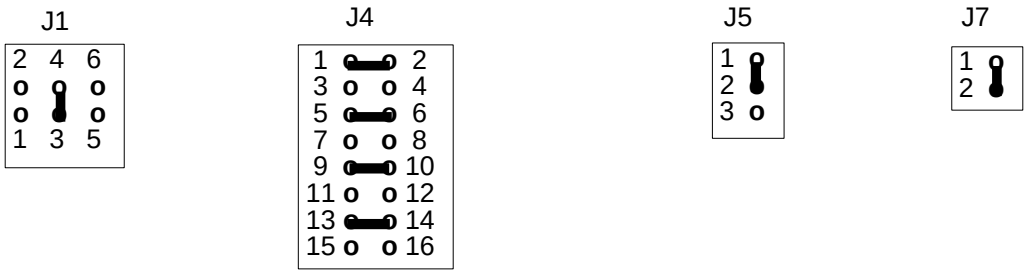
2.5.4 **Mode 4** - +/-10 Volt differential/Bipolar

This mode provides 8 channels of differential input with 2 important limitations.

1. The maximum differential voltage between the two legs is 10V.

2. Neither input leg can be, as referenced to ground, greater than +10V nor less than -10V.

The jumpering for this mode is as shown below :



+/-10 Volt - Differential/Bipolar Mode

Each channel's input voltage is applied to J3 as referenced in section 2.6. Be sure to use the differential pin definitions when using this mode.

Two's complement binary values are read from the converter per the following table.

Full Scale Range :	+/-10.0V	
Least Significant bit :	305uV (16-Bit) or 4.88mV (12-Bit)	
+Full Scale (FS-1LSB) :	9.999695V (16-Bit) or 9.99512 (12-Bit)	7FFFH
Midscale :	0.0V	0000H
One LSB below Midscale :	-305uV (16Bit) or -4.88mV (12-Bit)	FFFFH
-Full Scale :	-10.0V	8000H

NOTE: On the PCM-A/D-12 the lower nibble of all hex values will be 0.

2.6 Input Connector Pin definitions

Input to the PCM-A/D board is made via J3. When used in the single-ended mode, 16-channels are available and when used in a differential mode, 8 channels are available. The illustration below shows the pin definitions for each case.

J3

CH0	1 o	o 2	CH8
CH1	3 o	o 4	CH9
GND	5 o	o 6	GND
CH2	7 o	o 8	CH10
GND	9 o	o 10	GND
CH3	11 o	o 12	CH11
GND	13 o	o 14	GND
CH4	15 o	o 16	CH12
GND	17 o	o 18	GND
CH5	19 o	o 20	CH13
GND	21 o	o 22	GND
CH6	23 o	o 24	CH14
CH7	25 o	o 26	CH15

Single-Ended Input Channels

J3

CH0+	1 o	o 2	CH0-
CH1+	3 o	o 4	CH1-
GND	5 o	o 6	GND
CH2+	7 o	o 8	CH2-
GND	9 o	o 10	GND
CH3+	11 o	o 12	CH3-
GND	13 o	o 14	GND
CH4+	15 o	o 16	CH4-
GND	17 o	o 18	GND
CH5+	19 o	o 20	CH5-
GND	21 o	o 22	GND
CH6+	23 o	o 24	CH6-
CH7+	25 o	o 26	CH7-

Differential Input Channels

2.7 PC/104 Bus Pin Definitions

The PC/104 connectors at J10 and J11 are shown here with the signal designations.

GND	B1 o	o A1	IOCHK
RESET	B2 o	o A2	BD7
+5V	B3 o	o A3	BD6
IRQ9	B4 o	o A4	BD5
-5V	B5 o	o A5	BD4
DRQ2	B6 o	o A6	BD3
-12V	B7 o	o A7	BD2
0WS	B8 o	o A8	BD1
+12V	B9 o	o A9	BD0
GND	B10 o	o A10	IOCHRDY
MEMW	B11 o	o A11	AEN
MEMR	B12 o	o A12	SA19
IOW	B13 o	o A13	SA18
IOR	B14 o	o A14	SA17
DACK3	B15 o	o A15	SA16
DRQ3	B16 o	o A16	SA15
DACK1	B17 o	o A17	SA14
DRQ1	B18 o	o A18	SA13
REFRESH	B19 o	o A19	SA12
SYSCLK	B20 o	o A20	SA11
IRQ7	B21 o	o A21	SA10
IRQ6	B22 o	o A22	SA9
IRQ5	B23 o	o A23	SA8
IRQ4	B24 o	o A24	SA7
IRQ3	B25 o	o A25	SA6
DACK2	B26 o	o A26	SA5
TC	B27 o	o A27	SA4
BALE	B28 o	o A28	SA3
+5V	B29 o	o A29	SA2
OSC	B30 o	o A30	SA1
GND	B31 o	o A31	SA0
GND	B32 o	o A32	GND

GND	C0 o	o D0	GND
SBHE	C1 o	o D1	MEMCS16
LA23	C2 o	o D2	IOCS16
LA22	C3 o	o D3	IRQ10
LA21	C4 o	o D4	IRQ11
LA20	C5 o	o D5	IRQ12
LA19	C6 o	o D6	IRQ15
LA18	C7 o	o D7	IRQ14
LA17	C8 o	o D8	DACK0
MEMR	C9 o	o D9	DRQ0
MEMW	C10 o	o D10	DACK5
SD8	C11 o	o D11	DRQ5
SD9	C12 o	o D12	DACK6
SD10	C13 o	o D13	DRQ6
SD11	C14 o	o D14	DACK7
SD12	C15 o	o D15	DRQ7
SD13	C16 o	o D16	+5V
SD14	C17 o	o D17	MASTER
SD15	C18 o	o D18	GND
KEY	C19 o	o D19	GND

2.8 Connector/Jumper Summary

Connector/ Jumper	Description	Page Reference
J1	Mode Select, differential or single-ended	2-3
J2	DC-DC Converter Enable	2-3
J3	Analog input connector	2-8
J4	Input range select jumper	2-3
J5	Mode select, differential vs. single-ended	2-3
J6	DC-DC Converter Enable	2-3
J7	Mode Select, binary vs. two's complement	2-3
J8	I/O Address Select	2-2
J9	Interrupt Routing Select	2-2
J10	PC/104-8 Connector	2-8
J11	PC/104-16 Connector	2-8

3 PCM-A/D Programming Reference

3.1 I/O Register Definitions

The PCM-A/D uses 4 consecutive I/O addresses beginning with a base address selected via jumper block J8. See Section 2.1 for I/O address selection details. The four allocated I/O addresses are used as shown here :

ADDRESS	Write Register	Read Register
BASE	Channel Select	Status Register
BASE+1	Channel Select/Conversion Start	LSB Data
BASE+2	Conversion Start Only	MSB Data
BASE+3	Reserved	Reserved

Each Register will be examined in more detail.

3.1.1 Base Address

Write Register - Channel Select

D7 - N/A
D6 - N/A
D5 - N/A
D4 - N/A
D3 - Bit 3 of select nibble
D2 - Bit 2 of select nibble
D1 - Bit 1 of select nibble
D0 - Bit 0 of select nibble

Writing a value to the BASE I/O port will cause the onboard multiplexers to select a new input channel. The channel number selected is the binary value of the lower 4 bits. No conversion is started and a delay of approximately 6uS for multiplexer settling is required before beginning a conversion.

Read Register - Conversion Status

D7 - N/A
D6 - N/A
D5 - N/A
D4 - N/A
D3 - N/A
D2 - N/A
D1 - Busy 0 = Converter busy, 1 = Conversion complete
D0 - Interrupt 0 = Conversion in progress, 1 = Conversion complete

This status register indicates when a conversion is complete. It is recommended that software routines wait until both the Conversion complete and the Interrupt bits are both set before reading the conversion data.

3.1.2 Base + 1 Address

Write Register - Select Channel/Start Conversion

D7 - N/A
D6 - N/A
D5 - N/A
D4 - N/A
D3 - Bit 3 of select nibble
D2 - Bit 2 of Select nibble
D1 - Bit 1 of select nibble
D0 - Bit 0 of select nibble

Writing a value to the BASE + 1 I/O address not only selects the channel number as encoded in bits 3-0 but after a hardware settling delay of approximately 6uS starts a conversion. This is the normal method to begin a conversion as the channel selection and conversion start are automated into a single write.

Read Register - LSB Data

D7 - D7 of conversion data
D6 - D6 " " "
D5 - D5 " " "
D4 - D4 " " "
D3 - D3 " " "
D2 - D2 " " "
D1 - D1 " " "
D0 - D0 " " "

Reading of I/O base address + 1 will present the lower 8-bits of the 16-bit conversion data. Note that on the 12-Bit converter module, the lower 4 bits of this register will always read as 0. This allows software to transparently use either the 12-bit or the 16-bit module.

Note that the data is only valid if both the BUSY and INTERRUPT bits are both set to 1 in the status register.

3.1.3 Base + 2 Address

Write Register - Start Conversion

D7 = N/A
D6 = N/A
D5 = N/A
D4 = N/A
D3 = N/A
D2 = N/A
D1 = N/A
D0 = N/A

A write to this register with any value will start the A/D converter on whatever channel was previously selected by the Channel Select Register or the Channel Select/Start Conversion register. This method of starting the converter allows for maximum throughput when repetitively converting on the same channel as no multiplexer settling time is required.

Read Register - MSB Data

D7 = D15 of conversion data
D6 = D14 " "
D5 = D13 " "
D4 = D12 " "
D3 = D11 " "
D2 = D10 " "
D1 = D9 " "
D0 = D8 " "

Reading from this register gives the upper 8-bits of the 16-bit conversion data. This data is only valid if both the BUSY and INTERRUPT bits are set to 1 in the status register.

3.2 Conversion Techniques

The PCM-A/D can be programmed in any language supporting port I/O instructions. The code snippet below is in the 'C' language and demonstrates a simple function that takes as an argument the channel number and returns a 16-bit unsigned value corresponding to the current conversion value. The next section describes a sample/test/calibration program included with the PCM-A/D board both in executable and source form.

```
#define BASE_ADDRESS 0x110


unsigned convert(int channel_number)
{
unsigned return_value;

/* Start the conversion by writing to the Select/Start conversion Register */

      outportb(BASE_ADDRESS + 1, channel_number);

/* Now wait for the conversion to complete */

      while((inportb(BASE_ADDRESS) & 0x03) != 3)
                              ;

/* Now read out the 2 bytes that make up the value */

        return_value = inportb(BASE_ADDRESS + 2);


/* Shift the MSB value up 8 bits in preparation for the LSB */

         return_value = return_value < 8;

/* Read the LSB value and 'OR' it into the prepared MSB value */

        return_value = return_value | inportb(BASE_ADDRESS + 1);

         return return_value;
}
```

3.3 PCM-A/D Demonstration Program

Included on a 3 1/2" diskette with the PCM-A/D board is a sample program in both 'C' source code and in MS-DOS executable format. The PCMAD12.EXE file was created using Borland C/C++ Version 3.1. This demo program may be used as a diagnostic/calibration program or portions of its source code may be used in a user's application program. The program's source code demonstrates both interrupt driven and polled-mode converter techniques. PCMAD12.EXE is executed from the MS-DOS command line with:

PCMAD12 <Enter>

A screen display like that shown below should be displayed and the interrupt counter in the lower right corner should be counting conversions.

Channel Number	RAW DATA	HIGH DATA	LOW DATA	DATA DEV.	CURRENT VOLTAGE	MAX VOLTAGE	MIN VOLTAGE	VOLTAGE DEVIATION
00	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
01	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
02	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
03	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
04	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
05	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
06	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
07	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
08	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
09	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
10	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
11	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
12	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
13	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
14	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000
15	FFFF	FFFF	FFFF	0000	5.0000	5.0000	5.0000	0.0000

'T' Toggle Scale, 'B' Converter toggle 'M' Interrupt Mode toggle, 'R' Reset Values

Scale : +0 to +5 Volts - Single-Ended 12-Bit Interrupt Mode 34256

NOTE: The PCMAD12.EXE program assumes that a base address of 110H has been selected and the IRQ5 is also selected. Refer to Section 2 of this manual for hardware selection details.

There are 5 keystrokes recognized by PCMAD12.EXE. They are as follows :

'**T**' - Toggles the input mode through the 4 supported modes :

+0 to +5 Volts - Single Ended
-10 to +10 Volts - Single Ended
+0 to +5 Volts - Differential
-10 to +10 Volts - Differential

NOTE : Pressing 'T' only changes the software's interpretation of the mode being used. The values displayed will be meaningless in any mode except for the one for which the board has been jumpered for.

'**B**' - Toggles the converter type between 12-bit and 16-bit.

'**M**' - Toggle the conversion mode

This key toggles the conversion mode between “Interrupt Mode” and “Polled Mode”. When in the “Interrupt Mode” a counter in the lower right corner will display the number of interrupts received since the last 'M', 'T', or 'R' command.

'**R**' - Reset Values

Pressing the 'R' key resets the High, Low and Deviation values to 0. This may be desirable after changing modes or input voltages to check the stability of the PCM-A/D or the input source.

'**ESCAPE**' - Exit to DOS

Pressing 'ESCAPE' will unhook the current interrupt vectors and return the system to the DOS prompt.

3.4 Calibration Procedures

1. Jumper the board for 0-5 Volt Single-Ended Mode. Base Address 110H and IRQ5.

2. Run the PCMAD12.EXE program.

3. Apply a precision (+/-1.5mV) input source to channel 0. Set the source to 0.00V

4. Turn R3 and R4 pots full clockwise. Clear values by pressing the 'R' key.

5. Adjust R3 slowly counter-clockwise for a stable zero voltage reading on channel 0. Ignore other channel values.

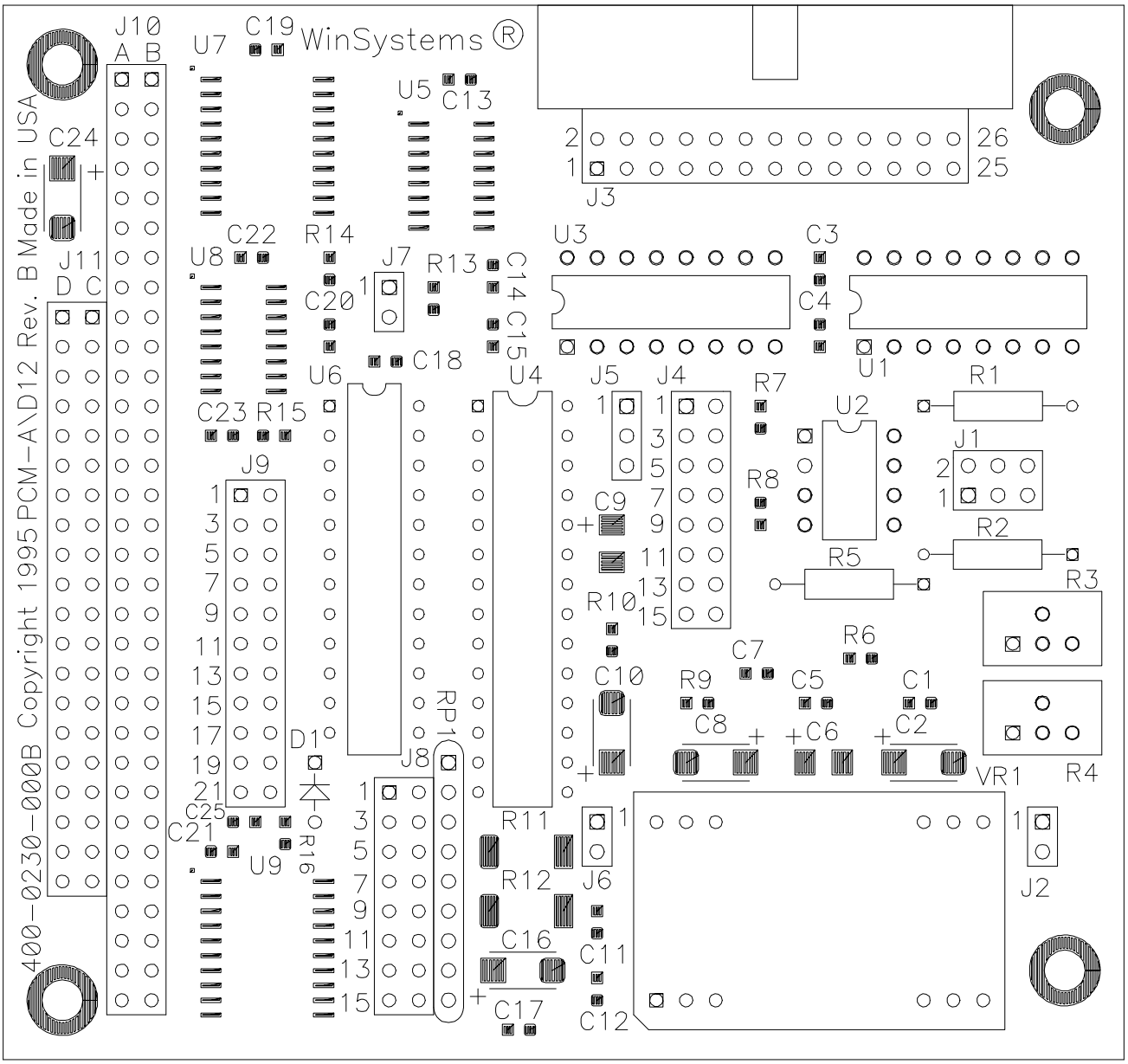
6. Set the precision input source to 4.99 volts and again clear current values by pressing the 'R' key.

7. Adjust R4 counter-clockwise for a reading corresponding to the input source. Some lower bit deviation may be experienced and is normal.

8. Set the input source to 5.00 volts. Hit 'R' to clear the current values. Look for a solid 5.00 Volt reading. If the display is not stable at 5.00V, repeat steps 3 through 8. If the value cannot be stabilized after repeating the steps, slowly turn R4 clockwise up to one full turn to achieve acceptable results. Turning beyond this point will destroy board linearity. If the voltages cannot be stabilized the board is not functioning properly and will need to be repaired.

4 APPENDIX A

PCM-A/D Parts Placement Guide



5 APPENDIX B

PCM-A/D Parts List

ASSM ITEM FROM: PCM-A/D12-16 ASSM ITEM THRU: PCM-A/D12-16
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
	PCM-A/D12-16	PC/104, 12-BIT A/D CONVERTER	PC/104, 12-BIT A/D CONVERTER	F	1.0
1	999-9999-001	SPECIAL NOTES	11-30-95 MEB (NEW)	I	1.0
1	0230-200-0000	ASSY PCM-A/D12-16 REV.B1	ASSY PCM-A/D12-16 REV.B1	F	1.0
2	CONTRACT LABOR	OUTSIDE CONTRACT LABOR	OUTSIDE CONTRACT LABOR	L	3.0
2	999-9999-001	SPECIAL NOTES	01-08-96 MEB ECBOM(U1,U3 P/N)	I	1.0
2	999-9999-001	SPECIAL NOTES	10-03-95 MEB ECO 95-89	I	1.0
2	999-9999-001	SPECIAL NOTES	08-15-95 MEB ECO 95-75	I	1.0
2	999-9999-001	SPECIAL NOTES	08-15-95 MEB ECBOM	I	1.0
2	603-1047-803	CAP .1uF 50v 20% CER 0805	C1,C3,C4,C5,C7,C11,C12,C13,C14,C15,C17,	I	15.0
2	999-9999-001	SPECIAL NOTES	C18,C19,C21,C22	I	1.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C2,C8,C10,C16,C24	I	5.0
2	603-2255-72B	CAP 2.2uF 25v 10% TAN 3528	C6,C9	I	2.0
2	603-1027-703	CAP 1000pF 50v 10% CER 0805	C20,C23,C25	I	3.0
2	124-0006-000	DIODE BAT47/BAT48	D1	I	1.0
2	121-0103-050	RN SIP 9P 8 RES 10K L091S103 (BKMN)	RP1	I	1.0
2	113-0503-201	POT 50K 15 TURN BECKMAN 64ZR50K	R3,R4	I	2.0
2	601-0333-503	RES 33K Ohm 5% 1/10w 0805	R6	I	1.0
2	601-0201-503	RES 200 Ohm 5% 1/10w 0805	R7	I	1.0
2	601-0101-503	RES 100 Ohm 5% 1/10w 0805	R8,R9	I	2.0
2	601-0105-503	RES 1M Ohm 5% 1/10W 0805	R10	I	1.0
2	601-0100-507	RES 10 Ohm 5% 1w 2512	R11,R12	I	2.0
2	601-0103-503	RES 10K Ohm 5% 1/10W 0805	R13,R14	I	2.0
2	601-0102-503	RES 1K Ohm 5% 1/10W 0805	R16	I	1.0
2	601-0222-503	RES 2.2K Ohm 5% 1/10w 0805	R15	I	1.0
2	200-0163-100	SOCKET 16 PIN 316-AG19DC (1040)	U1,U3	I	2.0
2	200-0083-100	SOCKET 8 PIN 308-AG19DC (2080)	U2	I	1.0
2	200-0328-100	SOCKET, 28 P .3 PRCICNTC LT0328TBB (17)	U4	I	1.0
2	611-0175-002	IC, 74HC175D S0-16	U5	I	1.0
2	200-0243-100	SOCKET 24 P .3 324-AG19DC (425)	U6	I	1.0
2	612-0245-002	IC, 74HCT245DW (SM)	U7	I	1.0
2	611-0221-002	IC, 74HC221D SO-16	U8	I	1.0
2	612-0688-002	IC, 74HCT688AF (SM)	U9	I	1.0
2	200-0064-100	SCKT 64 POS STK QPHF2-64-020-1Z (PLAST)	J10 CLIP PIN B10, MUST BE HAND SOLDERED	I	1.0
2	200-0040-100	SCKT 40 POS STK QPHF2-40-020-1Z (PLSTRN)	J11 CLIP PIN C19, MUST BE HAND SOLDERED	I	1.0
2	201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J1=2X3 J4,J8=2X8 J9=2X11	I	.8
2	201-0036-010	HDR 1X36 UN TSW-136-07-G-S (SAM)	J2,J6,J7=2X1 J5=1X3	I	.2
2	201-0026-121	HDR 26 P RA 636-2607 (2500)	J3	I	1.0
2	400-0230-000B	PCB, PCM-A/D12 REV.B	PCB, PCM-A/D12 REV.B	I	1.0
2	999-9999-001	SPECIAL NOTES	MASK THE FOLLOWING: R1,R2,R5,VR1	I	1.0
SUB-ASSEMBLY TOTAL: 0230-200-0000 ARLIN - 36 Items					
1	0230-300-0000	SUB ASSY PCM-A/D12 REV.B	SUB ASSY PCM-A/D12 REV.B	F	1.0
2	999-9999-001	SPECIAL NOTES	08-15-95 MEB ECO 95-75	I	1.0
2	999-9999-001	SPECIAL NOTES	08-15-95 MEB ECBOM	I	1.0
2	730-0085-000	IC, INA111AP BURR-BROWN	U2	I	1.0

ASSM ITEM FROM: PCM-A/D12-16 ASSM ITEM THRU: PCM-A/D12-16
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	730-0005-000	IC, DG408DJ (Harris) (Siliconix)	U1,U3	I	2.0
2	730-0086-000	IC, ADS7806P (13) BURR-BROWN	U4	I	1.0
2	901-0011-000	IC, PALC22V10-35PC (15,TI) (17,CYP)	U6 CS=8D0E \SPRINT\PCMAD12_____\	I	1.0
2	201-0002-000	PLUG JUMPER 999-19-310-00	J1=1-2 5-6	I	16.0
2	999-9999-001	SPECIAL NOTES	J2=1-2	I	1.0
2	999-9999-001	SPECIAL NOTES	J4=3-4 7-8 11-12 15-16	I	1.0
2	999-9999-001	SPECIAL NOTES	J5=3-4	I	1.0
2	999-9999-001	SPECIAL NOTES	J6=1-2	I	1.0
2	999-9999-001	SPECIAL NOTES	J8=1-2 5-6 7-8 9-10 13-14 15-16	I	1.0
2	999-9999-001	SPECIAL NOTES	J9=15-16	I	1.0
2	KIT-PCM-STANDOFF-2	PC/104 STANDOFF KIT CONSISTING OF 2	** DO NOT SEND TO ASSY **	F	1.0
3	CONTRACT LABOR	OUTSIDE CONTRACT LABOR		L	.1
3	999-9999-001	SPECIAL NOTES	04-28-95 MEB (NEW BOM)	I	1.0
3	500-0200-091	SPACER M/F RAF 4000-440-N-MODL.600	SPACER M/F RAF 4000-440-N-MODL.600	I	2.0
3	500-0200-033	SCREW PPH 4-40 X 1/4"	SCREW PPH 4-40 X 1/4"	I	2.0
3	500-0200-092	NUT HEX NYLON 4-40	NUT HEX NYLON 4-40	I	2.0

```
  3     525-0304-001              SIZE 3 COIN ENVLPE 2.5" X 4.25" 50260    SIZE 3 COIN ENVELOPE 2 1/2 X 4 1/4          I       1.0
-------------------------------------------------------------------------------------------------------------------------------------------
SUB-ASSEMBLY TOTAL: KIT-PCM-STANDOFF-2 ARLIN - 6 Items
-------------------------------------------------------------------------------------------------------------------------------------------
-------------------------------------------------------------------------------------------------------------------------------------------
SUB-ASSEMBLY TOTAL: 0230-300-0000      ARLIN - 14 Items
-------------------------------------------------------------------------------------------------------------------------------------------
  1 910-0024-000                  LABEL, STATIC SENSITIVE 130-02           LABEL, STATIC SENSITIVE 130-02              I       1.0
  1 950-0001-000                  BAG STATIC BARRIER 07-0610 6X10          BAG STATIC BARRIER 07-0610                  I       1.0
  1 KIT-PCM-STANDOFF-2            PC/104 STANDOFF KIT CONSISTING OF 2      PC/104 STANDOFF KIT CONSISTING OF 2         F       1.0
  2   CONTRACT LABOR              OUTSIDE CONTRACT LABOR                                                               L        .1
  2   999-9999-001                SPECIAL NOTES                            04-28-95 MEB (NEW BOM)                      I       1.0
  2   500-0200-091                SPACER M/F RAF 4000-440-N-MODL.600       SPACER M/F RAF 4000-440-N-MODL.600          I       2.0
  2   500-0200-033                SCREW PPH 4-40 X 1/4"                    SCREW PPH 4-40 X 1/4"                       I       2.0
  2   500-0200-092                NUT HEX NYLON 4-40                       NUT HEX NYLON 4-40                          I       2.0
  2   525-0304-001                SIZE 3 COIN ENVLPE 2.5" X 4.25" 50260    SIZE 3 COIN ENVELOPE 2 1/2 X 4 1/4          I       1.0
-------------------------------------------------------------------------------------------------------------------------------------------
SUB-ASSEMBLY TOTAL: KIT-PCM-STANDOFF-2 ARLIN - 6 Items
-------------------------------------------------------------------------------------------------------------------------------------------
===========================================================================================================================================
TOP ASSEMBLY TOTAL: PCM-A/D12-16       ARLIN - 6 Items
===========================================================================================================================================

REPORT RECAP
------------
                  0 WARNING(S)
```



```
PARAMETER RECAP
---------------
PARAMETER KEY       : 10 BOM with Ref. Desc.
REPORT TITLE        : BOM for Manuals

ASSM ITEM RANGE     : PCM-A/D12-16       THRU PCM-A/D12-16       COSTING METHOD         : A
PARENT LOC RANGE    : <FIRST>            THRU <LAST>             QUANTITY TO EXPLODE    : 1
PRODUCT KEY RANGE   : <FIRST>            THRU <LAST>             USE SCRAP FACTOR (Y/N) : N
COMMODITY KEY RANGE : <FIRST>            THRU <LAST>             UPDATE INV STD COST    : N
                                                                 NO. LEVELS TO EXPLODE  : 999
DEFAULT COMP LOC    : ARLIN                                      COLUMNS OF DESC TEXT   : 42
BOM STATUS PRIORITY : A                                          SHORT OR LONG    (S/L) : S
                                                                 PRINT ITEM DESC  (Y/N) : Y
```

6 APPENDIX C

BURR-BROWN ADS7806/ADS7807 Datasheet Reprint

BURR - BROWN®

ADS7806

Low-Power 12-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

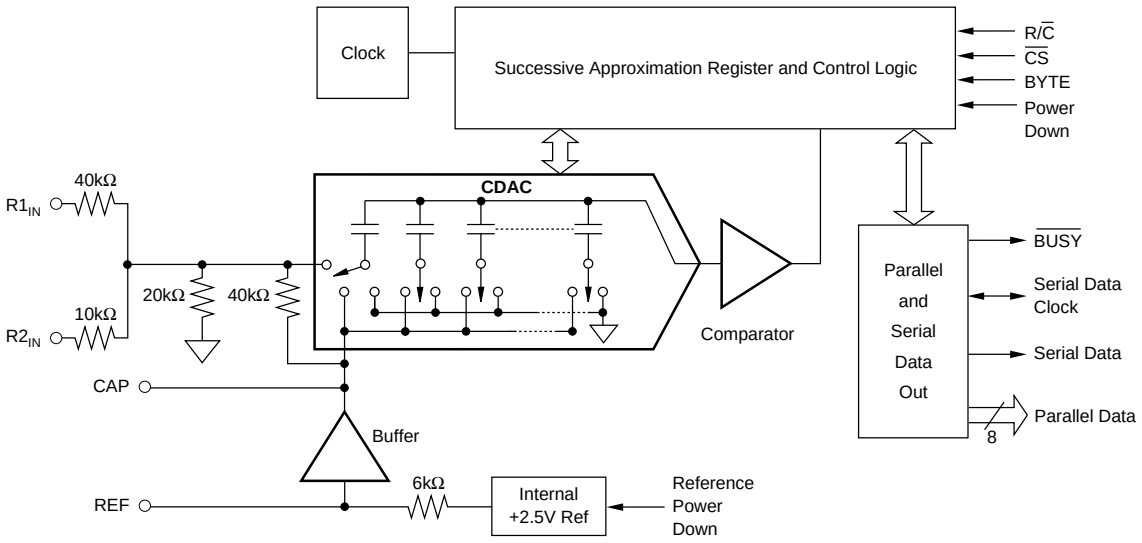
- 35mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- 25µs max ACQUISITION AND CONVERSION
- ±1/2LSB max INL AND DNL
- 72dB min SINAD WITH 1kHz INPUT
- ±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES
- SINGLE +5V SUPPLY OPERATION
- PARALLEL AND SERIAL DATA OUTPUT
- PIN-COMPATIBLE WITH 16-BIT ADS7807
- USES INTERNAL OR EXTERNAL REFERENCE
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7806 is a low-power 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit accuracy in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7806 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1158C
Printed in U.S.A. November, 1994

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U			ADS7806PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±0.9		*	±0.45	LSB[1]
Differential Linearity Error			±0.15	±0.9		*	±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise[2]			0.1			*		LSB
Gain Error			±0.2			±0.1		%
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down[5]	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V	80	90		*	*		dB[6]
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–90	–80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Usable Bandwidth[7]			130			*		kHz
Full Power Bandwidth (-3dB)			600			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			20			*		ps
Transient Response	FS Step			5			*	µs
Overvoltage Recovery[8]			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format			Parallel 12-bits in 2-bytes; Serial					
Data Coding			Binary Two's Complement or Straight Binary					
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U			ADS7806PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	R_L = 3.3kΩ, C_L = 50pF			83			*	ns
Bus Relinquish Time	R_L = 3.3kΩ, C_L = 10pF			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6			*		mA
I_{ANA}			5.0			*		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 40kHz		28	35		*	*	mW
	REFD HIGH		23			*		mW
	PWRD and REFD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7806 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$ ..... ±25V
$R2_{IN}$ ..... ±25V
CAP ..... V_{ANA} +0.3V to AGND2 –0.3V
REF ..... Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7806P	±0.9	70	–40°C to +85°C	Plastic DIP
ADS7806PB	±0.45	72	–40°C to +85°C	Plastic DIP
ADS7806U	±0.9	70	–40°C to +85°C	SOIC
ADS7806UB	±0.45	72	–40°C to +85°C	SOIC

PACKAGE INFORMATION

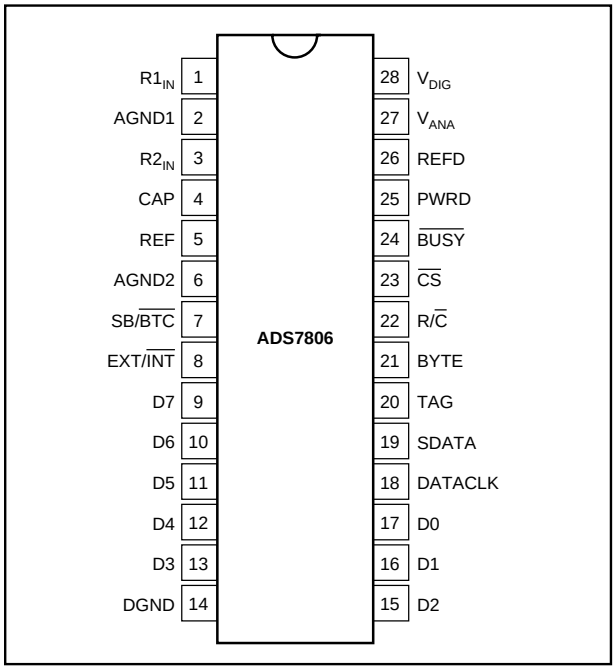
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7806P	Plastic DIP	246
ADS7806PB	Plastic DIP	246
ADS7806U	SOIC	217
ADS7806UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R1_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Sense Ground.
3	$R2_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH) on parallel output pins.
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



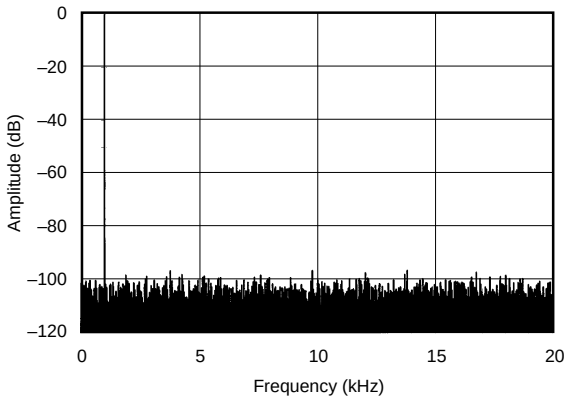
ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

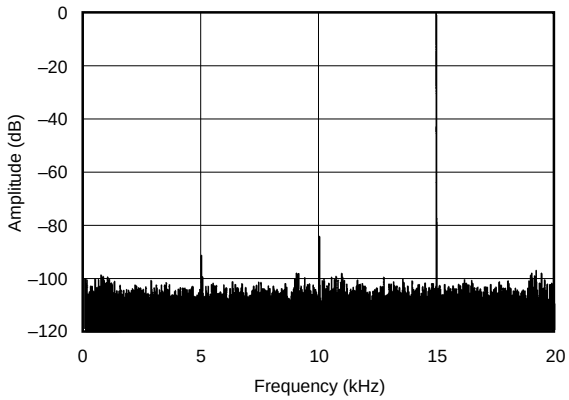
TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

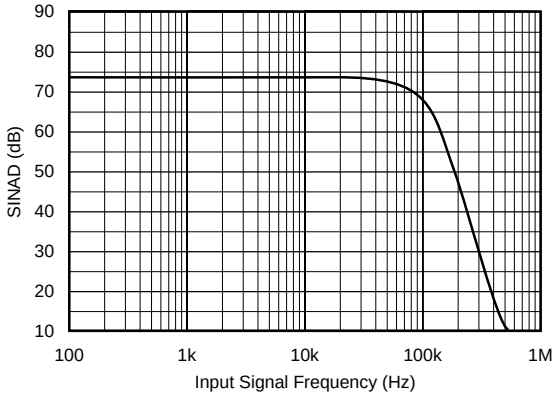
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



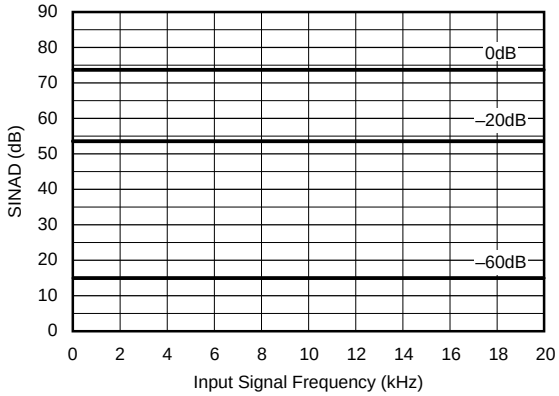
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



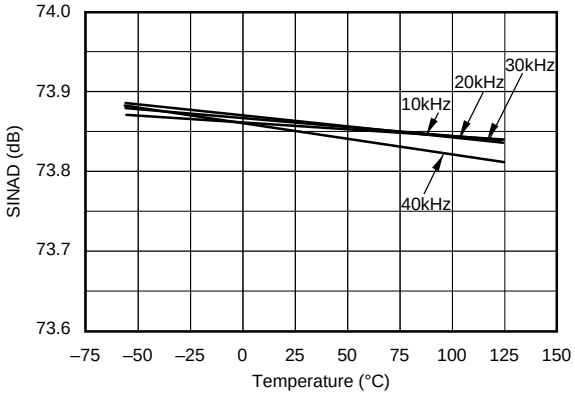
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



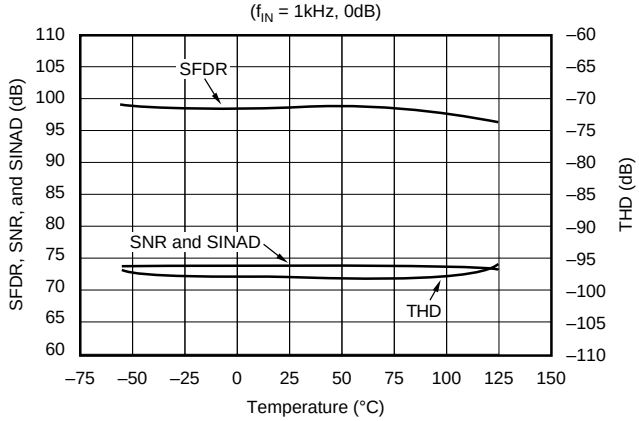
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

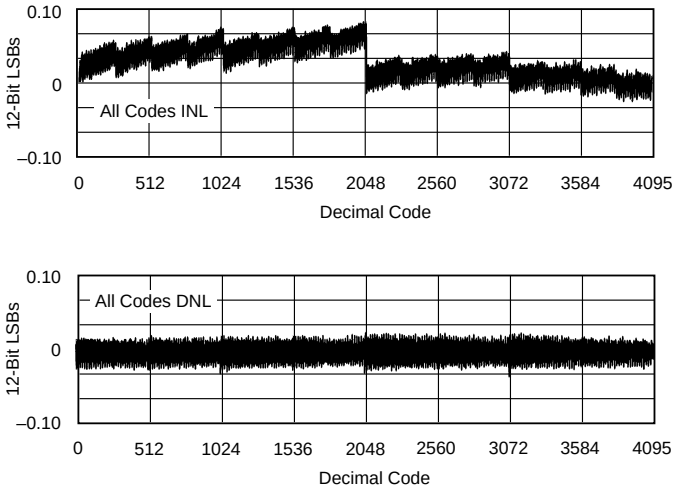


A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

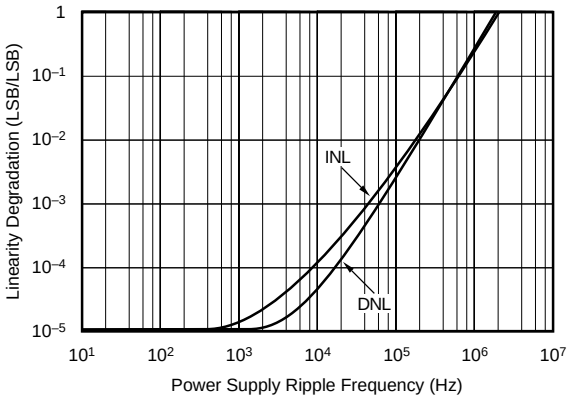


TYPICAL PERFORMANCE CURVES (CONT)

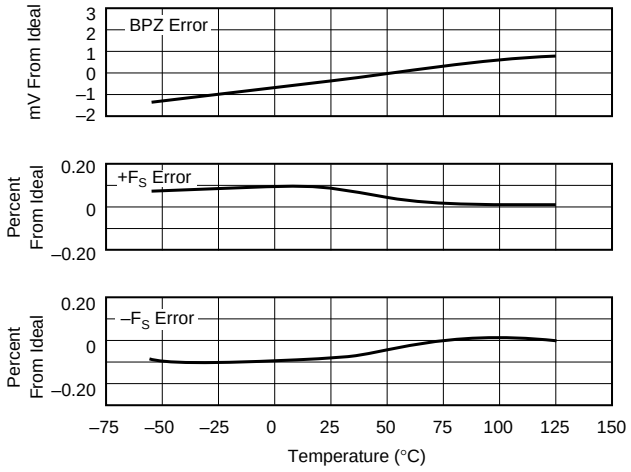
T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.



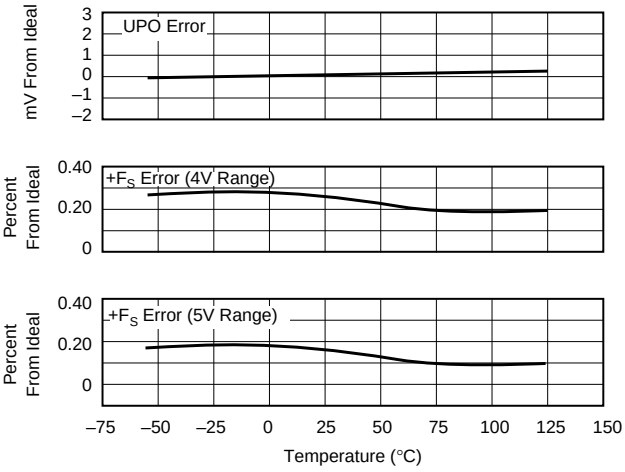
POWER SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE



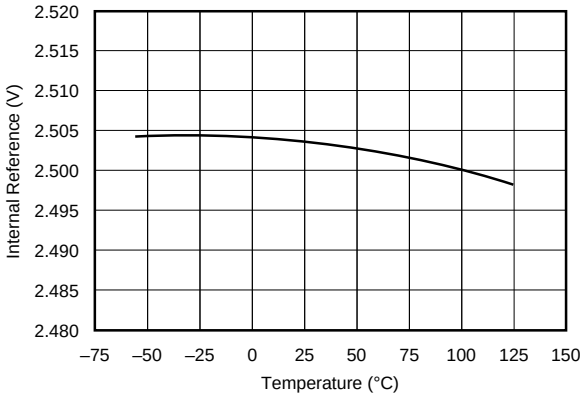
ENDPOINT ERRORS (20V BIPOLAR RANGE)



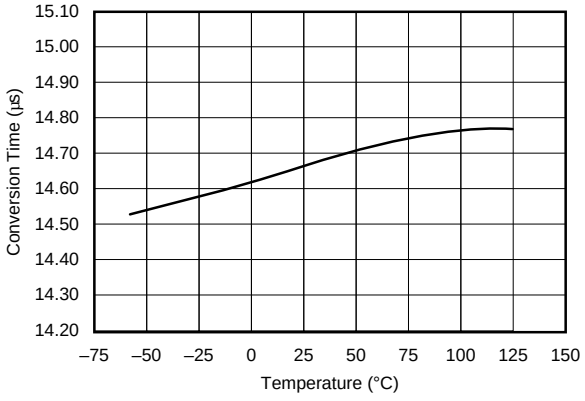
ENDPOINT ERRORS (UNIPOLAR RANGES)



INTERNAL REFERENCE VOLTAGE vs TEMPERATURE



CONVERSION TIME vs TEMPERATURE



BASIC OPERATION

PARALLEL OUTPUT

Figure 1a) shows a basic circuit to operate the ADS7806 with a ±10V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the 8 most significant bits will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the 4 least significant bits will be valid when $\overline{BUSY}$ rises. Data will be output in Binary Two's Complement format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b) shows a basic circuit to operate the ADS7806 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 12 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

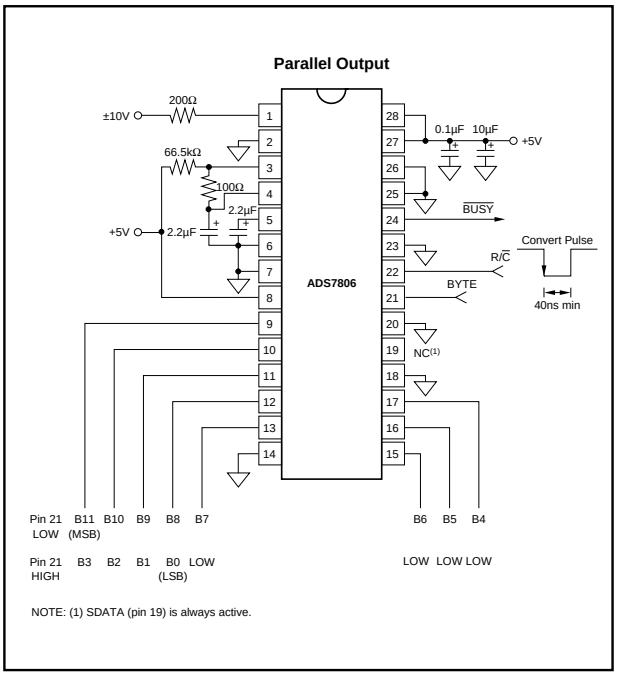


FIGURE 1a. Basic ±10V Operation, both Parallel and Serial Output.

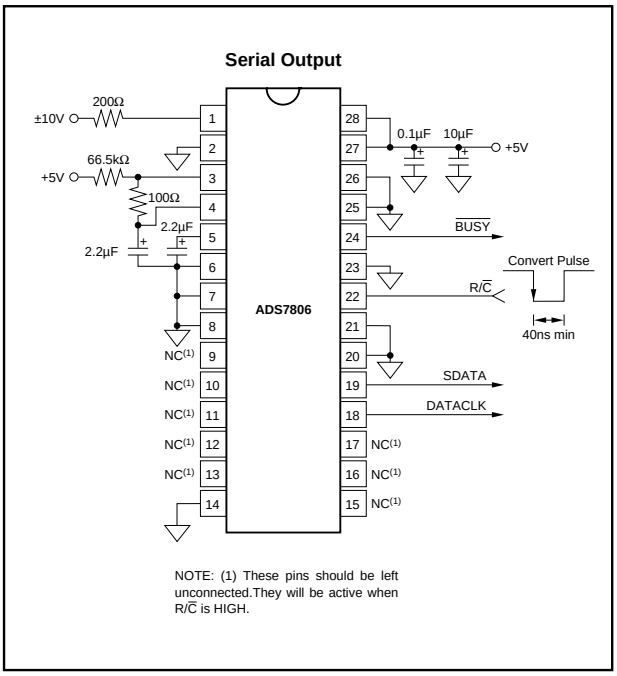


FIGURE 1b. Basic ±10V Operation with Serial Output.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n-1' will be output on SDATA (pin 19) following the start of conversion 'n'. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7806 outputs serial or parallel data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion "n" completed. Valid data from conversion "n" clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	↑	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion "n-1".

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-Scale Range	±10	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	1.22mV	976µV				
				BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.99512V	4.99878V	3.999024V	0111 1111 1111 1111	7FF	1111 1111 1111 1111	FFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	000	1000 0000 0000 0000	800
One LSB Below Midscale	–4.88mV	2.49878V	1.999024V	1111 1111 1111 1111	FFF	0111 1111 1111 1111	7FF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	800	0000 0000 0000 0000	000

Table V. Output Codes and Ideal Input Voltages.

port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{C}$ (pin 22) is HIGH and $\overline{CS}$ (pin 23) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 4 least significant bits will be valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data beyond 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

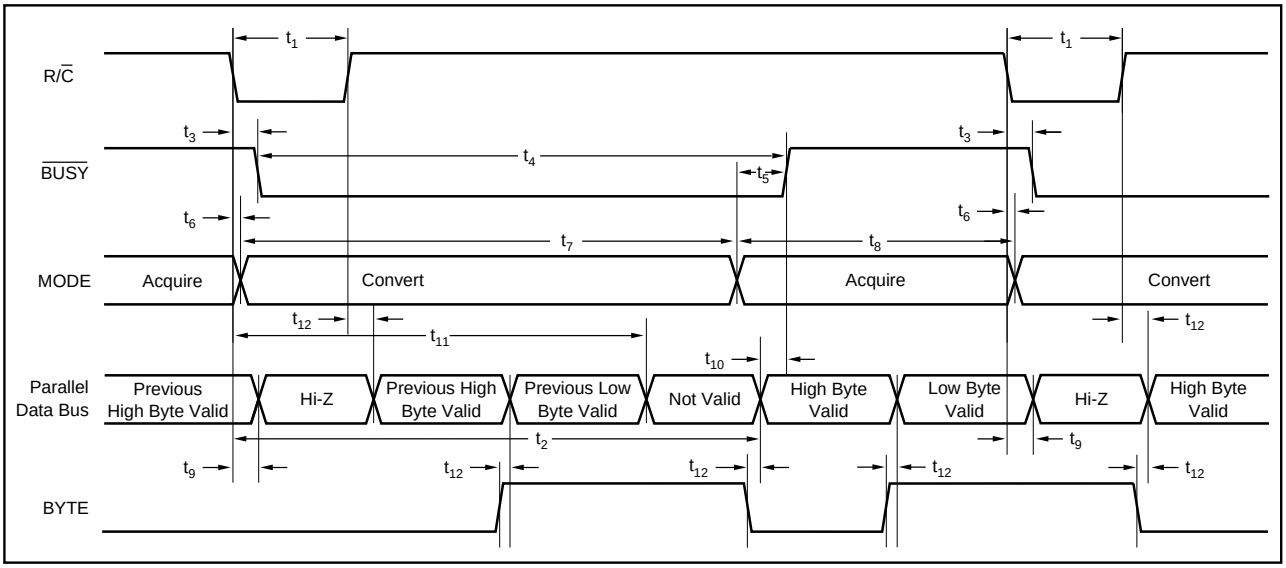


FIGURE 2. Conversion Timing with Parallel Output ($\overline{CS}$ and DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

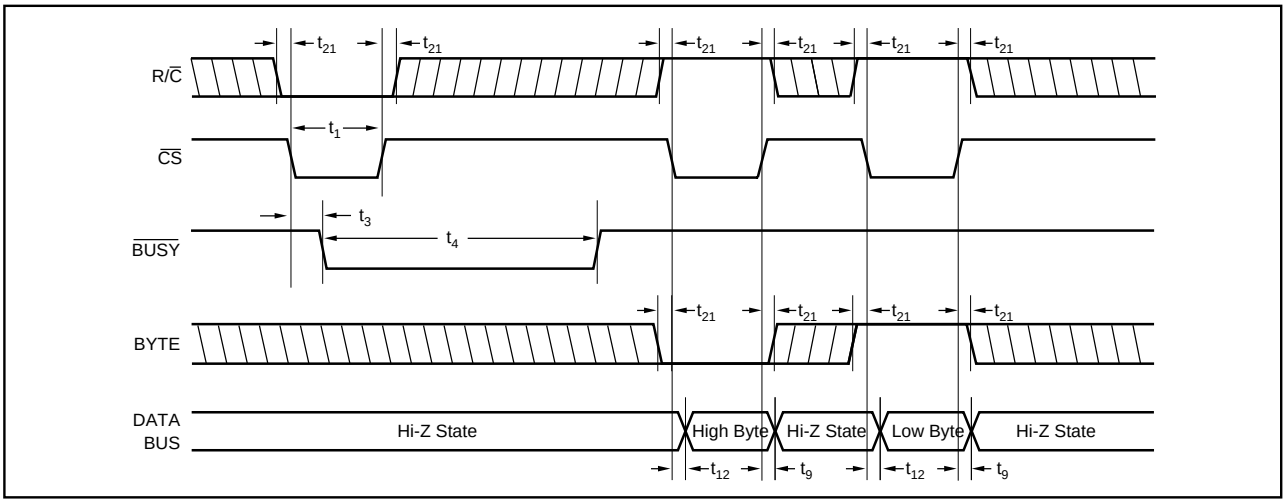


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		14.7	20	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		14.7	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		14.7	20	µs
t_8	Acquisition Time			5	µs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	14.7		µs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE VI. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During A Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7806 will output 12 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 12 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7806, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ LOW and use R/$\overline{C}$ to initiate conversions. While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12µs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift the results of conversion 'n' into the output register. If $\overline{CS}$ is LOW, R/$\overline{C}$ is HIGH, and the external clock is HIGH at this point, data will be lost. So, with $\overline{CS}$ LOW, either R/$\overline{C}$ and/or DATACLK must be LOW during this period to avoid losing valid data.

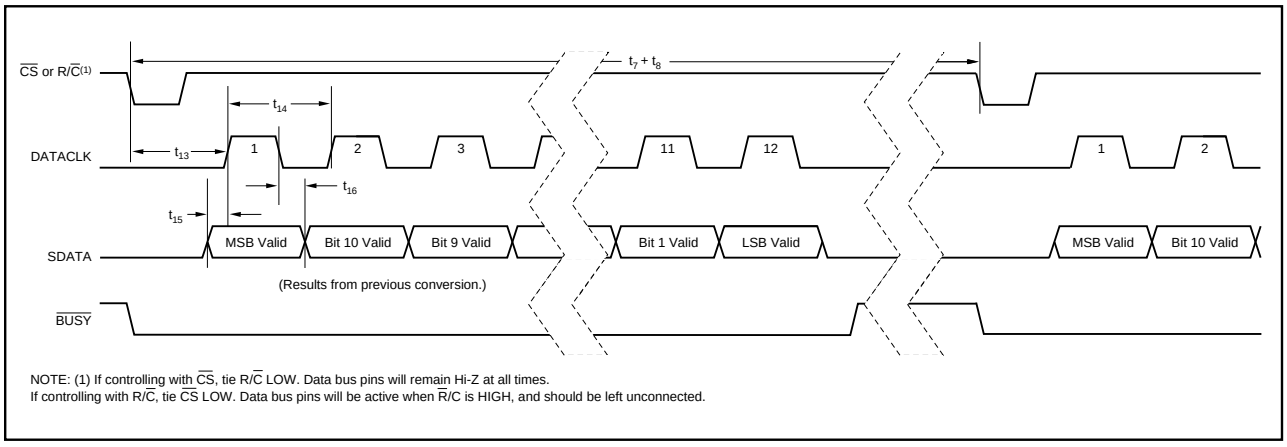


FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

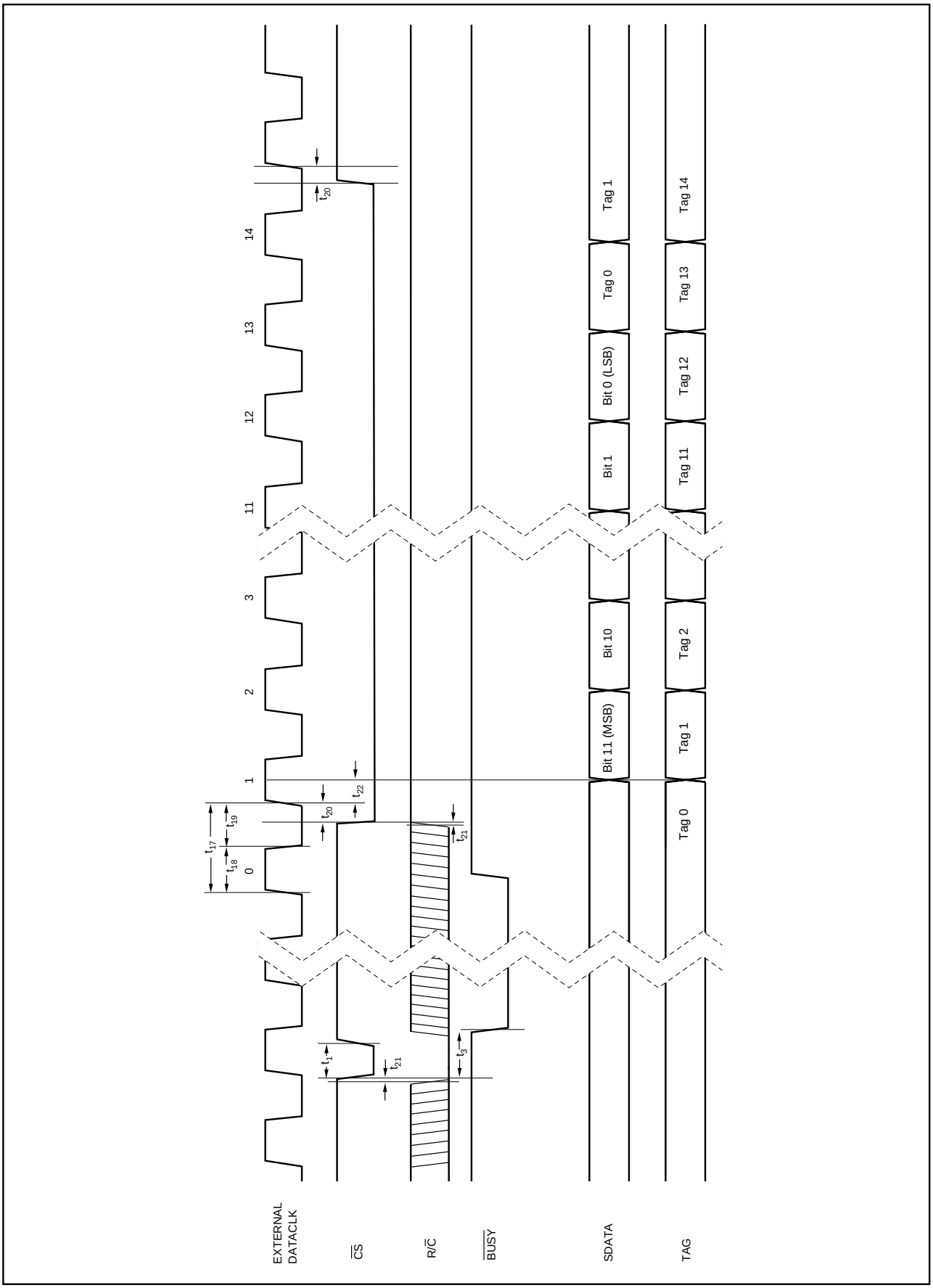


FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

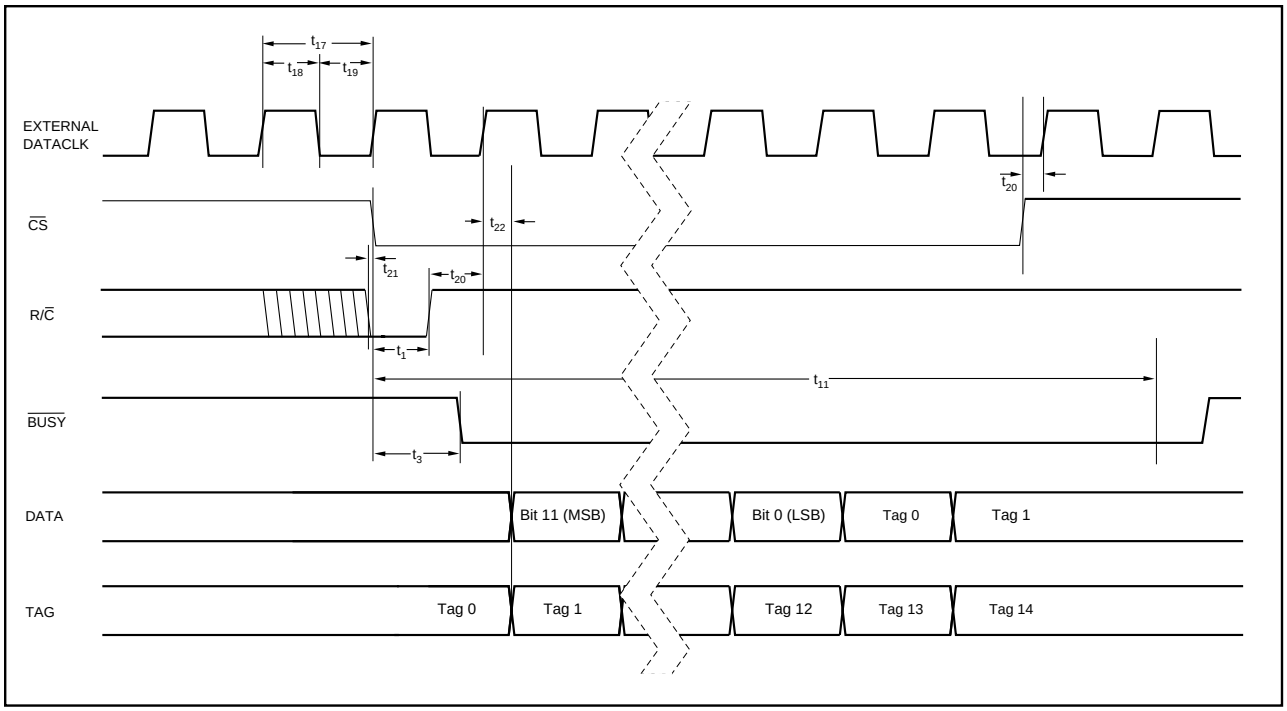


FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH) Read During a Conversion.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 12th falling edge and 13th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 13th falling edge and the 14th rising edge of DATACLK; the second input bit will be valid on the 14th falling edge and the 15th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 12 bits of valid data have been output.

INPUT RANGES

The ADS7806 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range (see Figure 8). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7806 in hardware, install the resistors shown in Figure 7a. Table VII lists the hardware trim ranges relative to the input for each input range.

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 7b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VIII for the range of offset and gain errors with and without the external resistors.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VII. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 7a).

NO CALIBRATION

See Figure 7b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered.

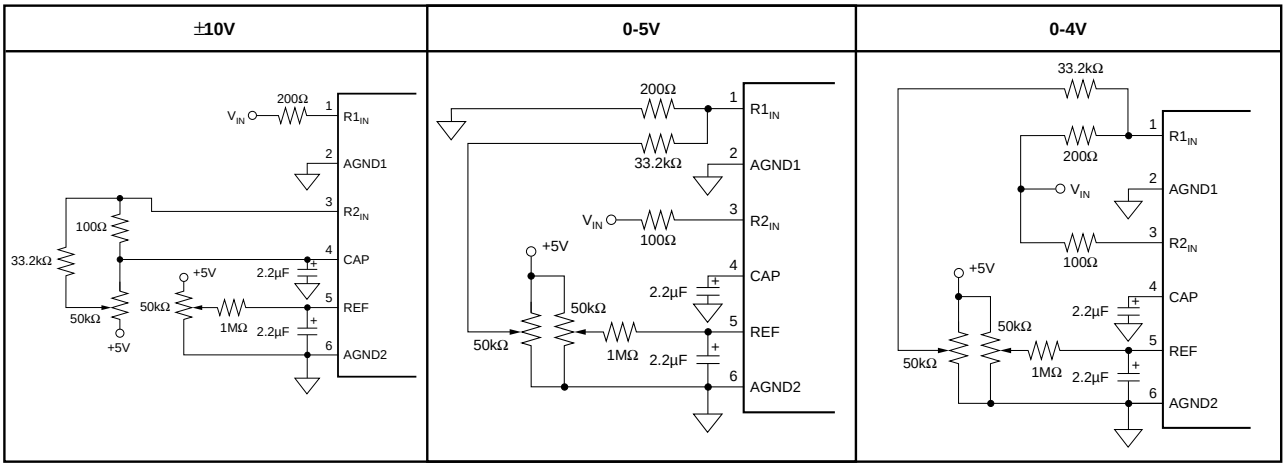


FIGURE 7a. Circuit Diagrams (With Hardware Trim).

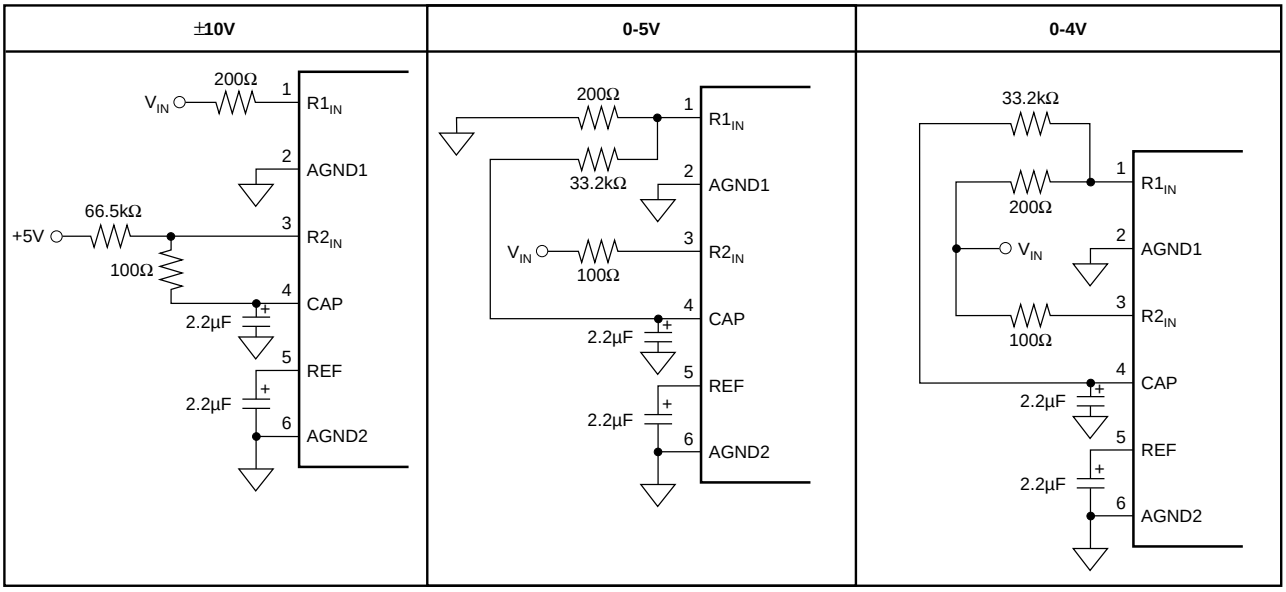


FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

ered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VIII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 8 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 9. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ADS7806 can operate with its internal 2.5V reference or an external reference. By applying an external reference to

INPUT RANGE (V)	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	–10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	+15	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–0.3 ≤ G ≤ 0.5 –0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	–3 ≤ UPO ≤ 3	–12 ≤ UPO ≤ –3	–7.5	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
0 to 4	–3 ≤ UPO ≤ 3	–10.5 ≤ UPO ≤ –1.5	–6	–0.4 ≤ G ≤ 0.4 –0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
Note: (1) High Grade.						

TABLE VIII. Range of Offset and Gain Errors with and without External Resistors

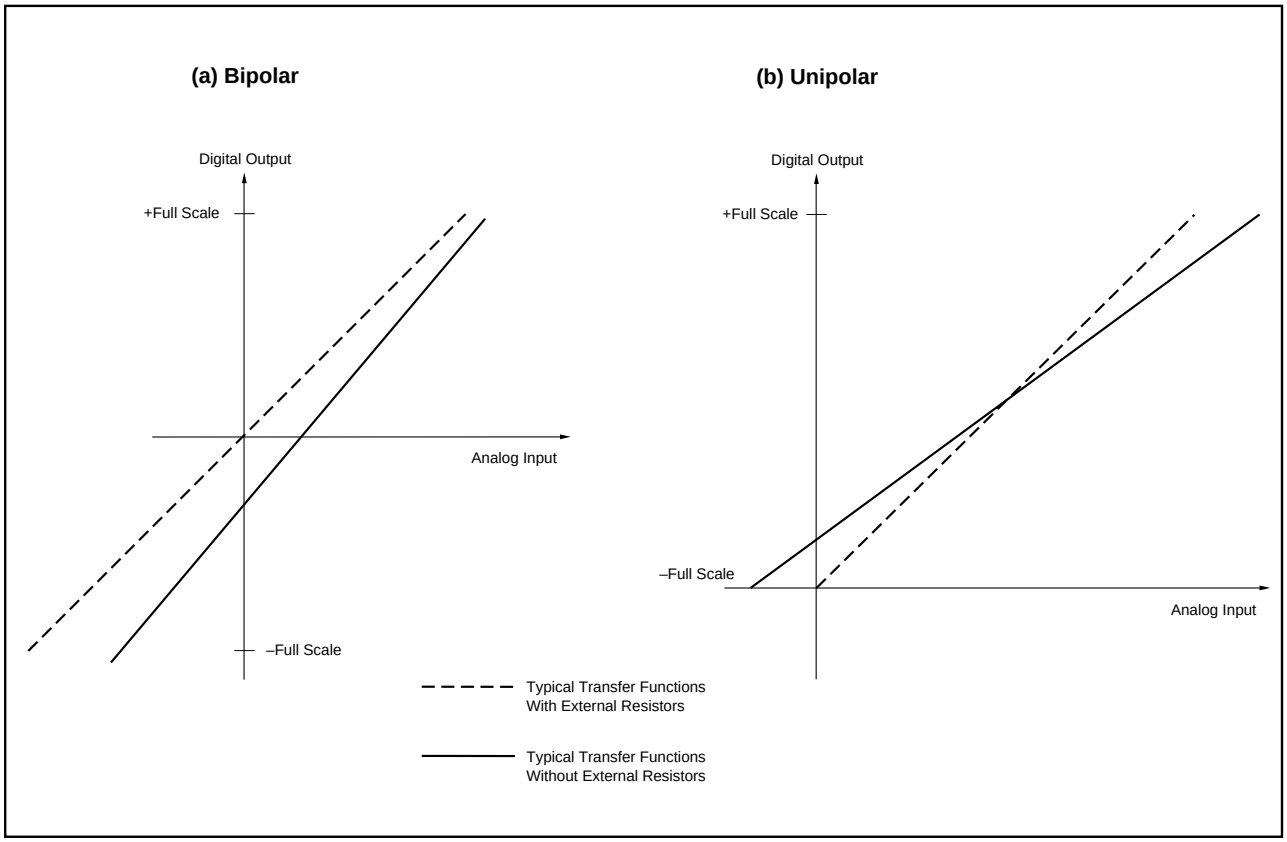


FIGURE 8. Typical Transfer Functions With and Without External Resistors.

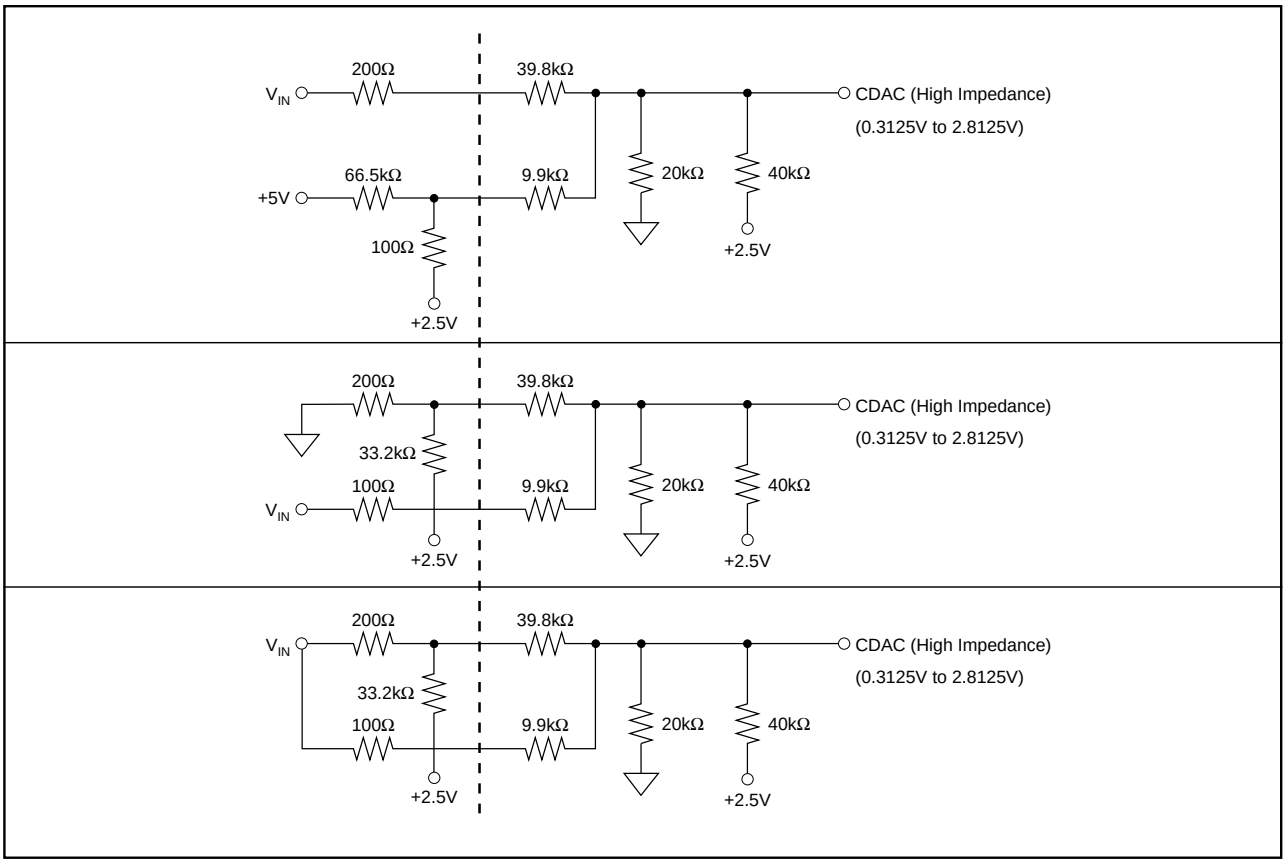


FIGURE 9. Circuit Diagrams Showing External and Internal Resistors.

pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing the overall power consumption of the ADS7806 by approximately 5mW.

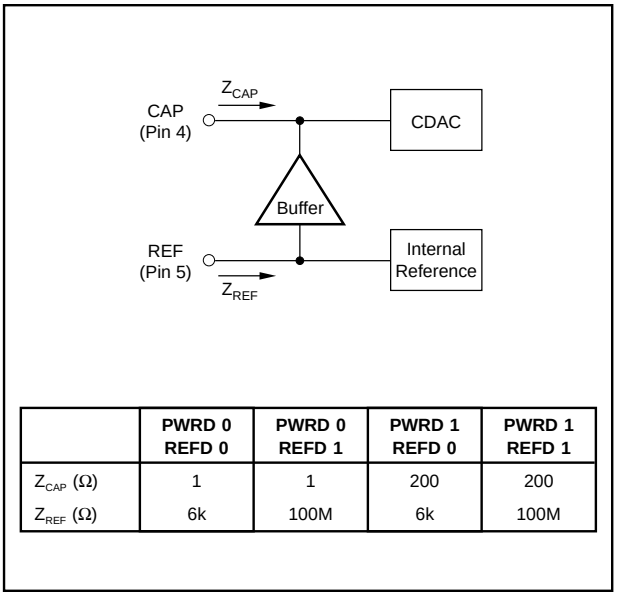
The internal reference has approximately an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS7806 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the

output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

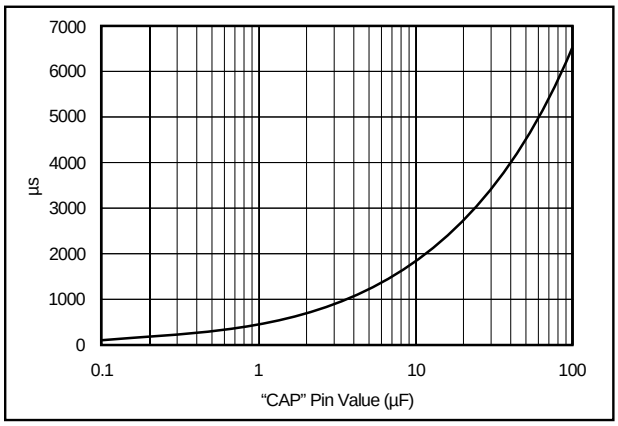


FIGURE 11. Power-Down to Power-Up Time vs Capacitor Value on CAP.

REFERENCE AND POWER DOWN

The ADS7806 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms, using a 2.2µF capacitor connected to CAP. See Figure 11 for power-down to power-up recovery time relative to the capacitor value on CAP. With +5V applied to V_{DIG}, the digital circuitry of the ADS7806 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7806 uses 90% of its power for the analog circuitry. The ADS7806 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7806. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground to which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7806 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7806.

The resistive front end of the ADS7806 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7806 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7806 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7807 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38µV.

APPLICATIONS INFORMATION

QSPI INTERFACING

Figure 12 shows a simple interface between the ADS7806 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7806 is the only serial peripheral.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select (SS) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the and the A/D may be "out-of-sync."

Figure 13 shows another interface between the ADS7806 and a QSPI equipped microcontroller. The interface allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial

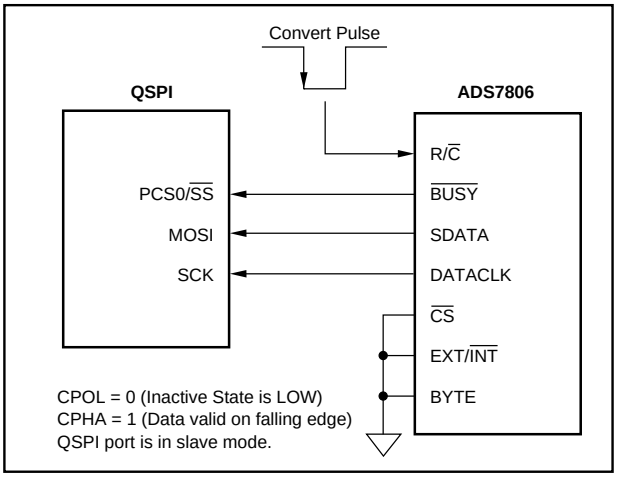


FIGURE 12. QSPI Interface to the ADS7806.

bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7806 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated and prevent a conversion from taking place.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW starting a conversion. The second, a twelve bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

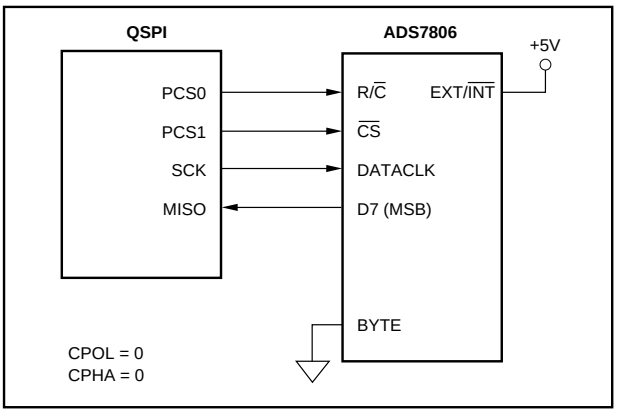


FIGURE 13. QSPI Interface to the ADS7806. Processor Initiates Conversions.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7806. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to twelve bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the twelve bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 12. The microcontroller will need to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 13 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has an SPI compatibility mode with some enhancements. Figure 14 shows an interface between the ADS7806 and the DSP56000 which is very similar to the QSPI interface seen in Figure 12. As mentioned in the QSPI section, the DSP56000 must be programmed to enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 15. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to five.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet shows that the pulse width is (0.7)RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is 35.6kHz. If a slower oscillator can be tolerated on the DSP56000, a conversion rate of 40kHz can be achieved by using a 19.2MHz clock and a prescale modulus of four.

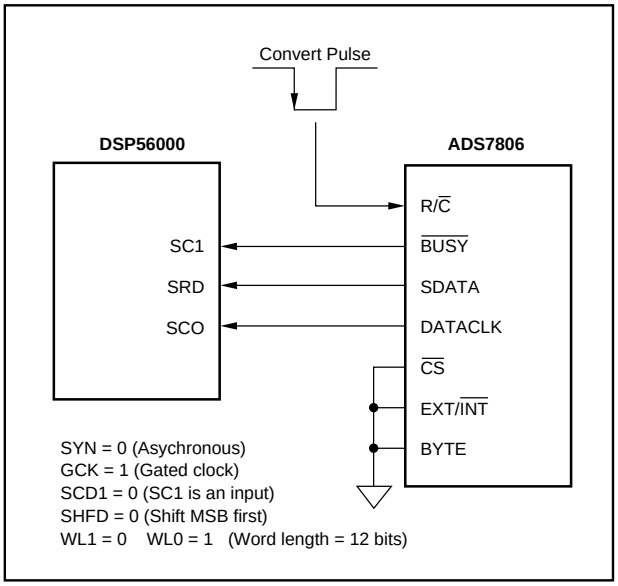


FIGURE 14. DSP56000 Interface to the ADS7806.

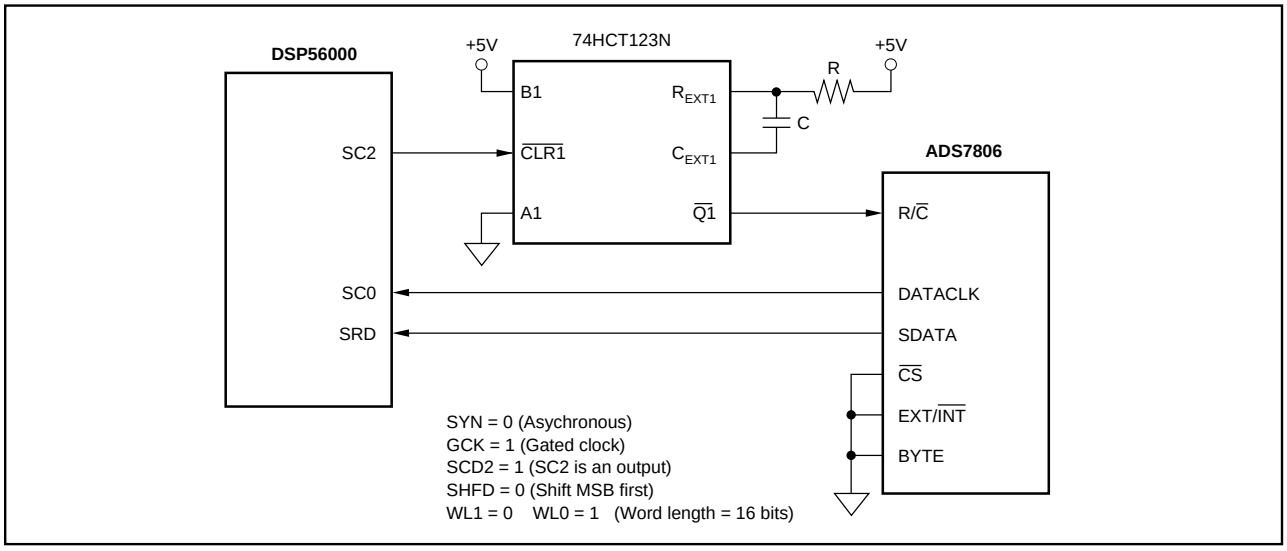
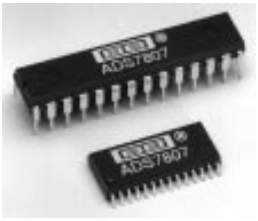


FIGURE 15. DSP56000 Interface to the ADS7806. Processor Initiates Conversions.

BURR - BROWN®



ADS7807

Low-Power 16-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

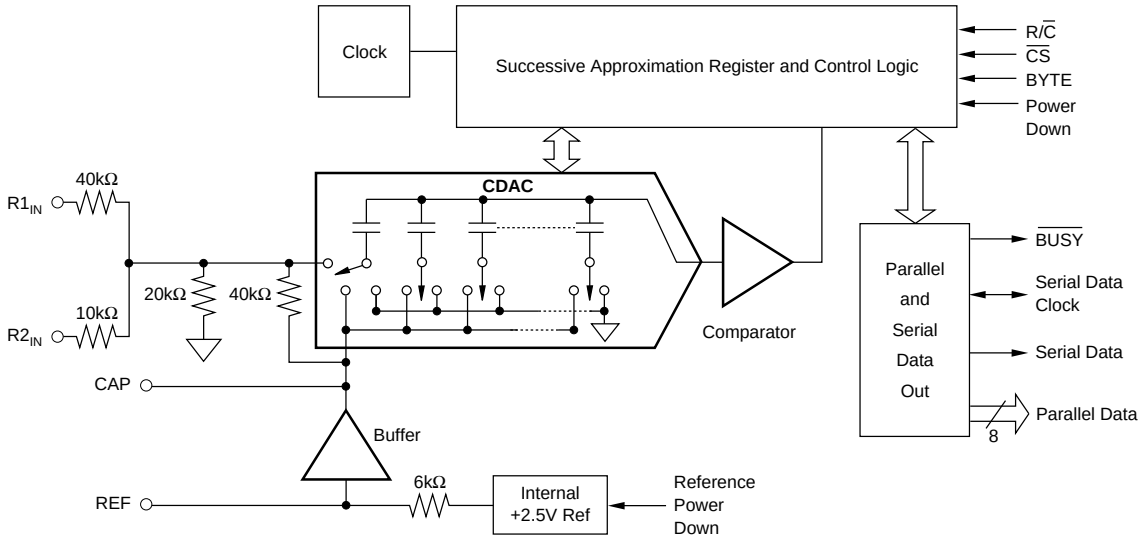
- 35mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- 25µs max ACQUISITION AND CONVERSION
- ±1.5LSB max INL
- DNL: 16 bits "No Missing Codes"
- 86dB min SINAD WITH 1kHz INPUT
- ±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES
- SINGLE +5V SUPPLY OPERATION
- PARALLEL AND SERIAL DATA OUTPUT
- PIN-COMPATIBLE WITH 12-BIT ADS7806
- USES INTERNAL OR EXTERNAL REFERENCE
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7807 is a low-power, 16-bit, sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7807 can acquire and convert 16-bits to within ±1.5LSB in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7807 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1159C
Printed in U.S.A. November, 1994

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, –2			+1.5, –1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			0.8			*		LSB
Gain Error			±0.2			±0.1		%
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down[5]	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V	90	100		96	*		dB[6]
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–100	–90		*	–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V	83	88		86	*		dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V	83	88		86	*		dB
Usable Bandwidth[7]			130			*		kHz
Full Power Bandwidth (–3dB)			600			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			20			*		ps
Transient Response	FS Step			5			*	µs
Overvoltage Recovery[8]			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS		Parallel 16 bits in 2-bytes; Serial						
Data Format		Binary Two's Complement or Straight Binary						
Data Coding								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	R_L = 3.3kΩ, C_L = 50pF			83			*	ns
Bus Relinquish Time	R_L = 3.3kΩ, C_L = 10pF			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6			*		mA
I_{ANA}			5.0			*		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 40kHz		28	35		*	*	mW
	REFD HIGH		23			*		mW
	PWRD and REFD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 305µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7807 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$ ..... ±25V
$R2_{IN}$ ..... ±25V
CAP ..... V_{ANA} +0.3V to AGND2 –0.3V
REF ..... Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7807P	±3	15	83	–40°C to +85°C	Plastic DIP
ADS7807PB	±1.5	16	86	–40°C to +85°C	Plastic DIP
ADS7807U	±3	15	83	–40°C to +85°C	SOIC
ADS7807UB	±1.5	16	86	–40°C to +85°C	SOIC

PACKAGE INFORMATION

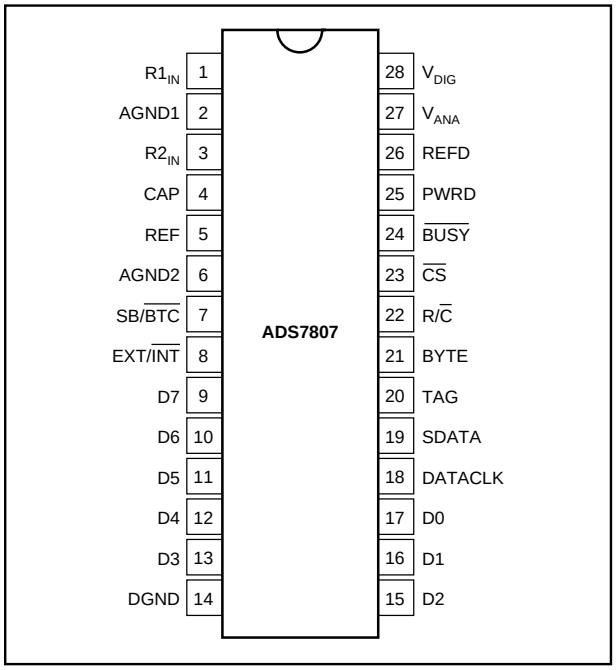
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7807P	Plastic DIP	246
ADS7807PB	Plastic DIP	246
ADS7807U	SOIC	217
ADS7807UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R1_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Sense Ground.
3	$R2_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 7 if BYTE is HIGH. Data bit 15 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 6 if BYTE is HIGH. Data bit 14 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 5 if BYTE is HIGH. Data bit 13 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 4 if BYTE is HIGH. Data bit 12 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	Data Bit 3 if BYTE is HIGH. Data bit 11 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH) on parallel output pins.
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



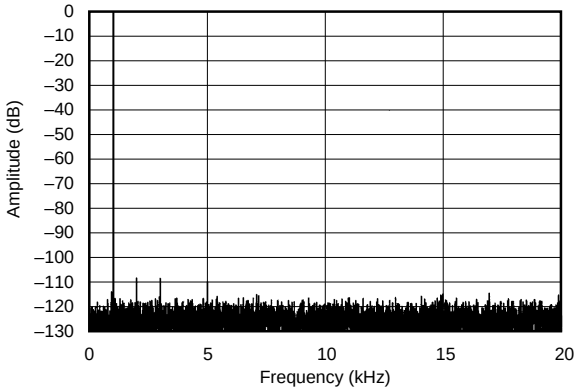
ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

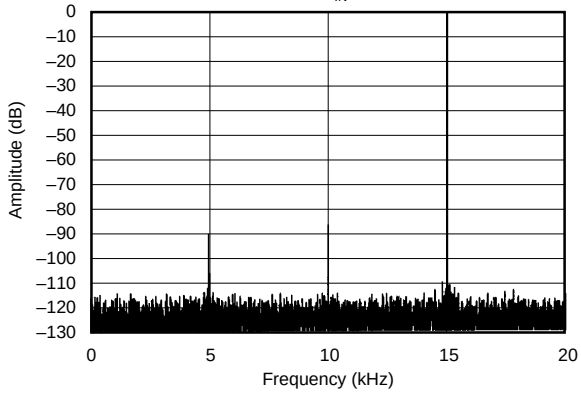
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

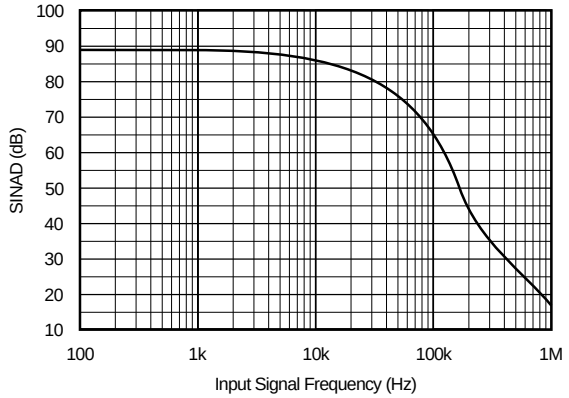
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



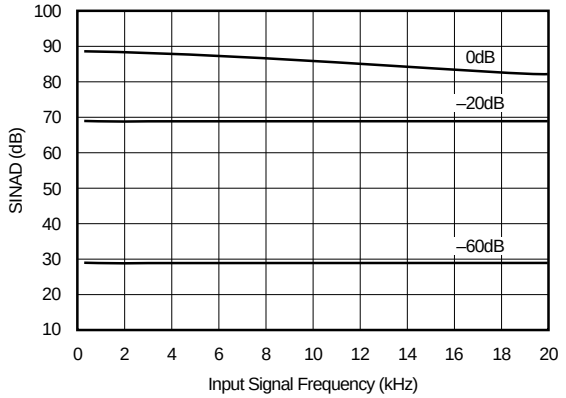
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



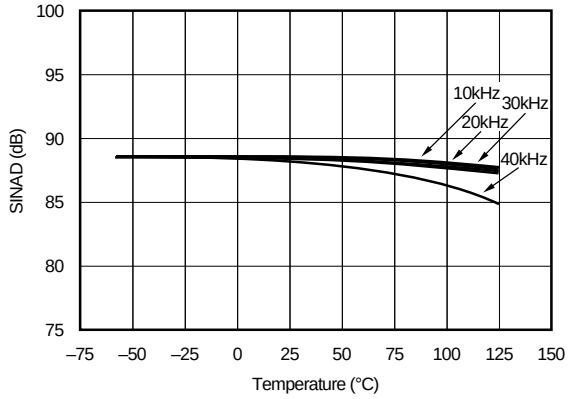
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



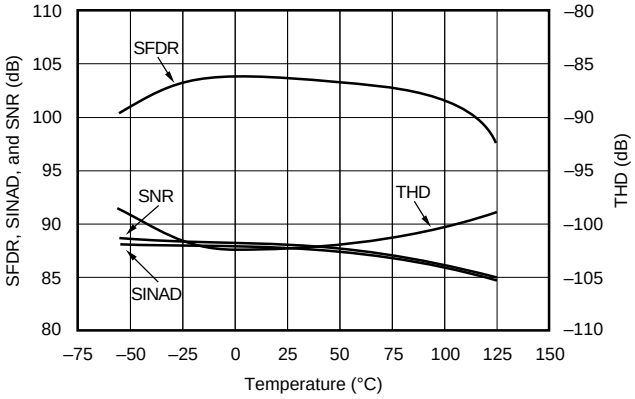
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

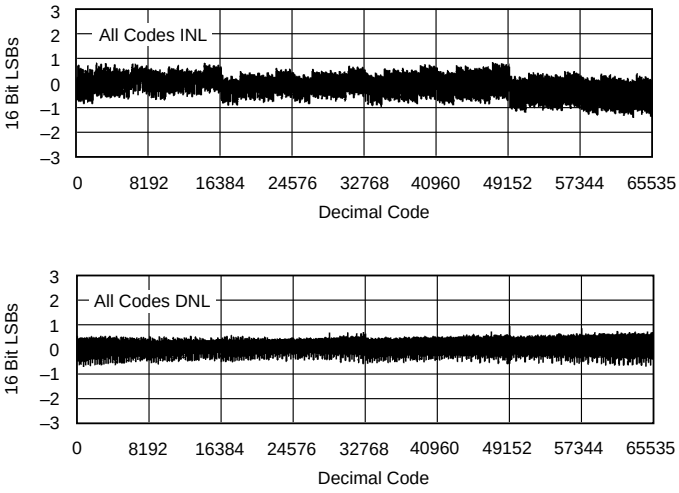


A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

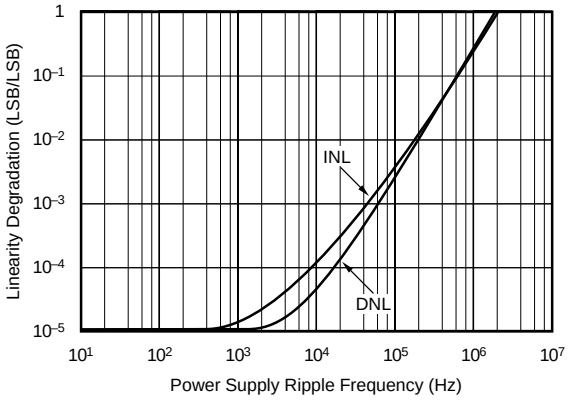


TYPICAL PERFORMANCE CURVES (CONT)

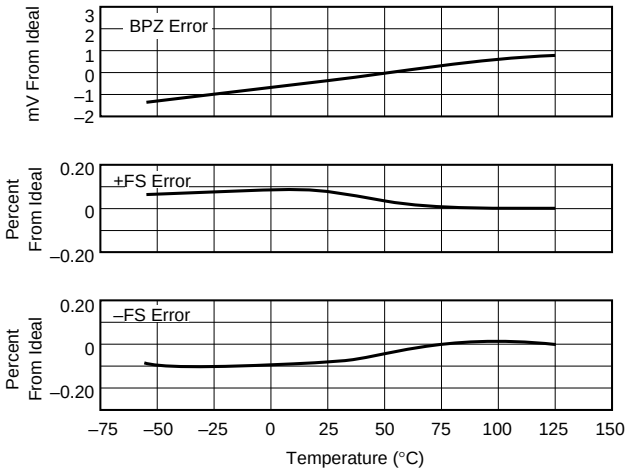
At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.



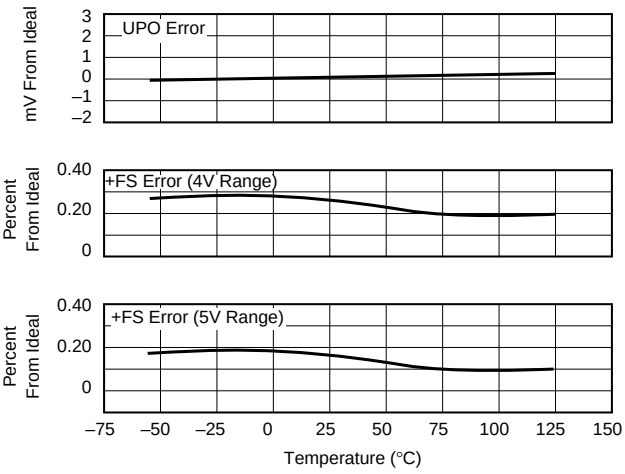
POWER SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE



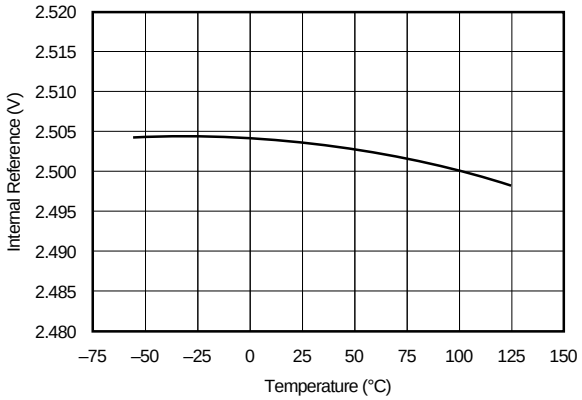
ENDPOINT ERRORS (20V BIPOLAR RANGE)



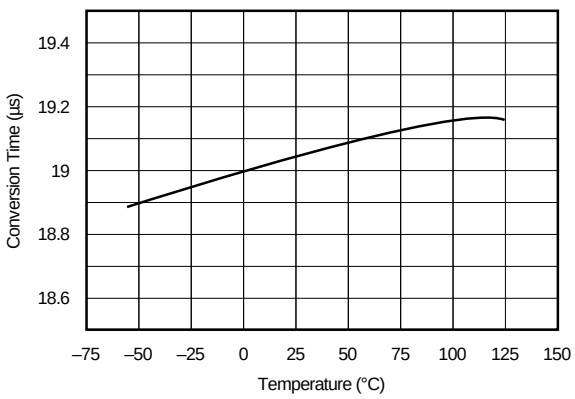
ENDPOINT ERRORS (UNIPOLAR RANGES)



INTERNAL REFERENCE VOLTAGE vs TEMPERATURE



CONVERSION TIME vs TEMPERATURE



BASIC OPERATION

PARALLEL OUTPUT

Figure 1a) shows a basic circuit to operate the ADS7807 with a ±10V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns (12µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the 8 most significant bits will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the 8 least significant bits will be valid when $\overline{BUSY}$ rises. Data will be output in Binary Two's Complement format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b) shows a basic circuit to operate the ADS7807 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 16 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns puts the sample/hold of the ADS7807 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

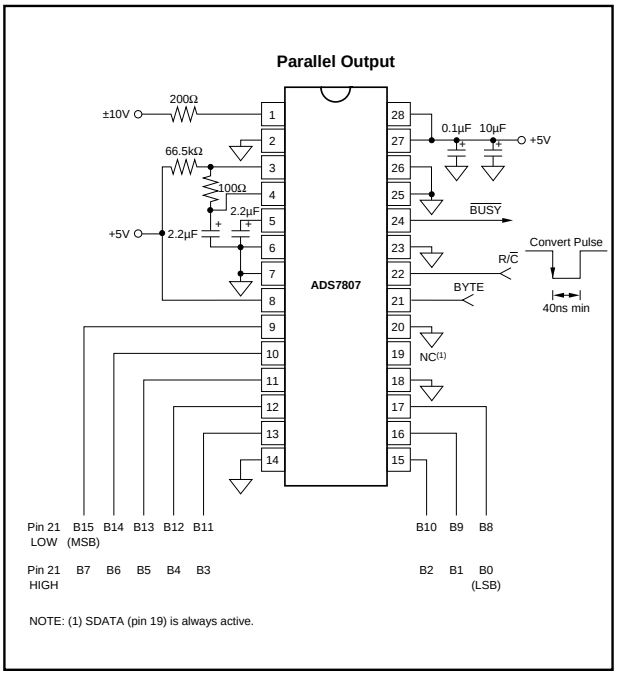


FIGURE 1a. Basic ±10V Operation, both Parallel and Serial Output.

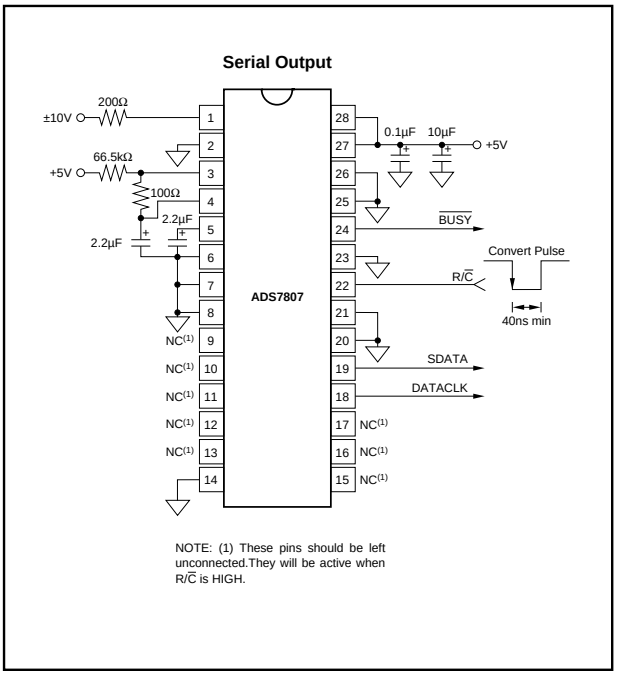


FIGURE 1b. Basic ±10V Operation with Serial Output.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion “n”. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion “n”. Databus enters Hi-Z state.
0	1	↑	Conversion “n” completed. Valid data from conversion “n” on the databus.
↓	1	1	Enables databus with valid data from conversion “n”.
↓	1	0	Enables databus with valid data from conversion “n-1”(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion “n-1”(1). Conversion “n” in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion “n” in progress.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion “n-1”.

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR’d and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion ‘n’, be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion ‘n’, serial data from conversion ‘n-1’ will be output on SDATA (pin 19) following the start of conversion ‘n’. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7807 outputs serial or parallel data in Straight Binary or Binary Two’s Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion “n”. Valid data from conversion “n-1” clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion “n”. Valid data from conversion “n-1” clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion “n”. Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion “n”. Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion “n” completed. Valid data from conversion “n” clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion “n-1” output on SDATA synchronized to external data clock. Conversion “n” in progress.
0	↑	0	1	Input	Valid data from conversion “n-1” output on SDATA synchronized to external data clock. Conversion “n” in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion “n” in progress.

NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion “n-1”.

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO’S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-Scale Range Least Significant Bit (LSB)	±10 305µV	0V to 5V 76µV	0V to 4V 61µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.999695V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

Table V. Output Codes and Ideal Input Voltages.

port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{C}$ (pin 22) is HIGH and $\overline{CS}$ (pin 23) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 8 least significant bits will be valid with the LSB on D0. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data beyond 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

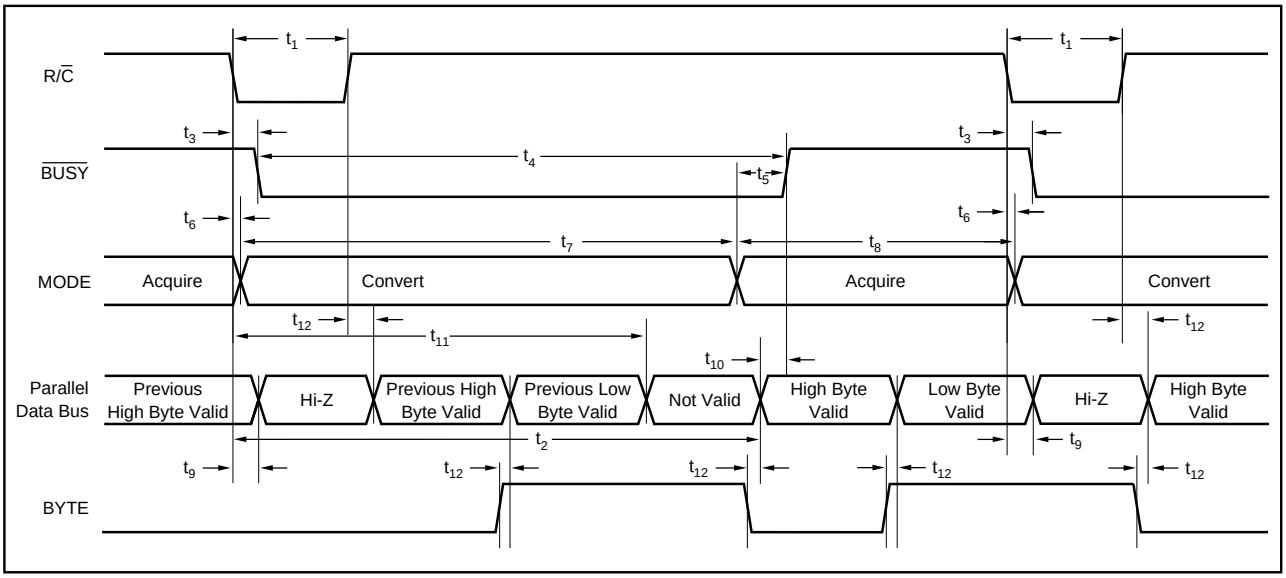


FIGURE 2. Conversion Timing with Parallel Output ($\overline{CS}$ and DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

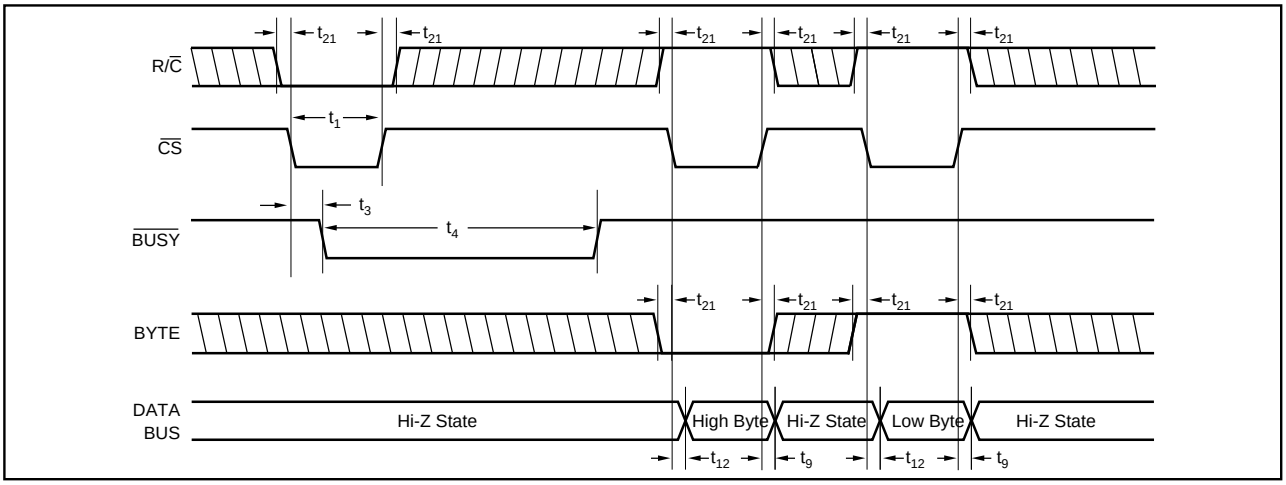


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active. Refer to the **Applications Information** section for specific serial interfaces.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		19	20	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		19	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		19	20	µs
t_8	Acquisition Time			5	µs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	19		µs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE VI. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During a Conversion)

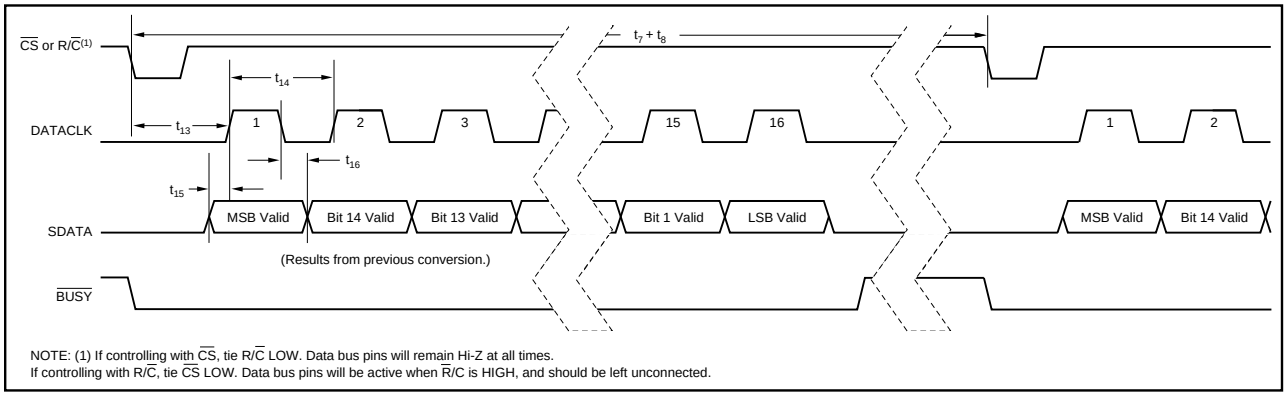
To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7807 will output 16 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 16 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 16th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7807, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ LOW and use R/$\overline{C}$ to initiate conversions.

While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12µs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift the results of conversion 'n' into the output register. If $\overline{CS}$ is LOW, R/$\overline{C}$ HIGH, and the external clock is HIGH at this point, data will be lost. So, with $\overline{CS}$ LOW, either R/$\overline{C}$ and/or DATACLK must be LOW during this period to avoid losing valid data.



NOTE: (1) If controlling with $\overline{CS}$, tie R/$\overline{C}$ LOW. Data bus pins will remain Hi-Z at all times.
If controlling with R/$\overline{C}$, tie $\overline{CS}$ LOW. Data bus pins will be active when R/$\overline{C}$ is HIGH, and should be left unconnected.

FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

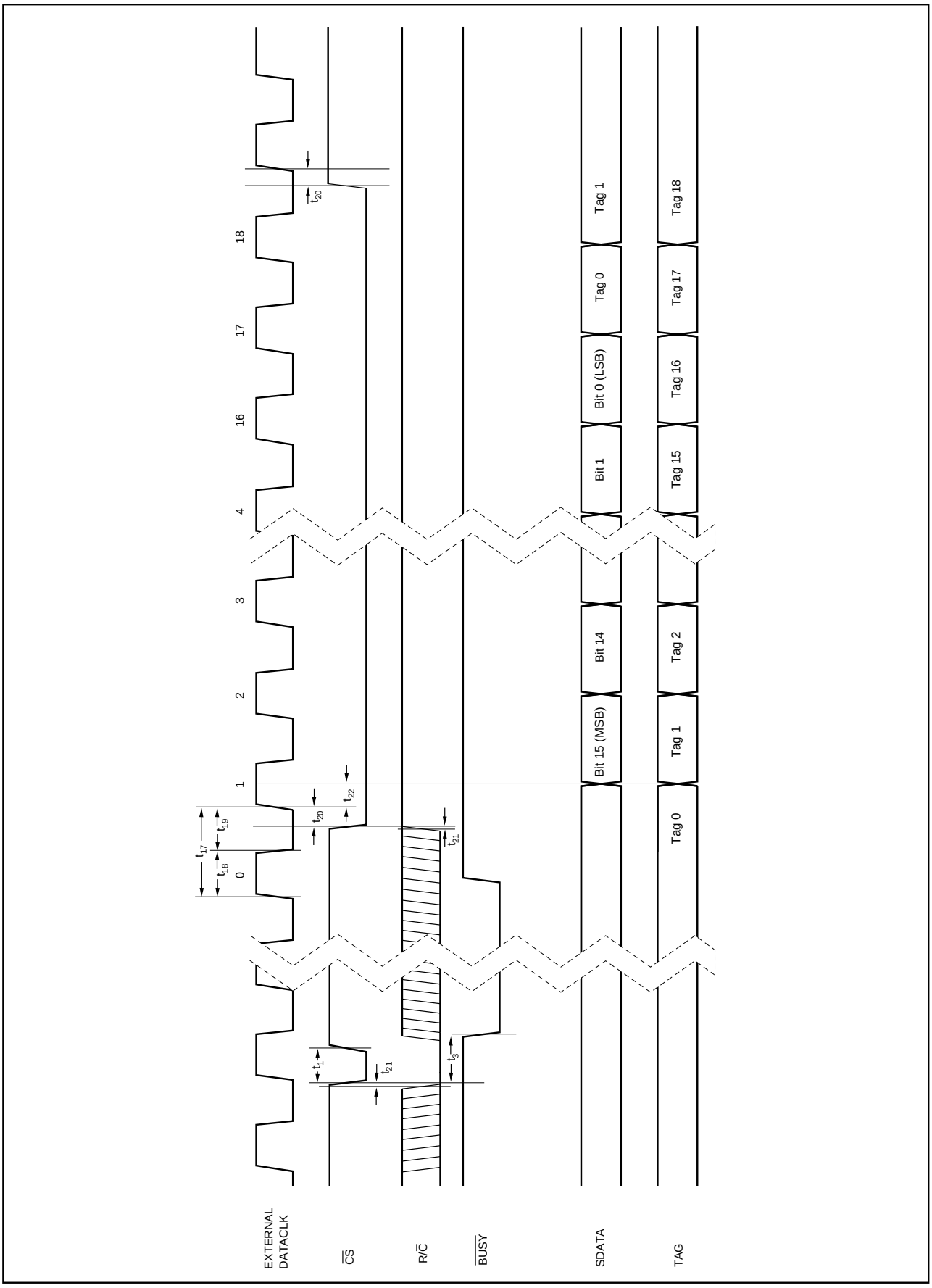


FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

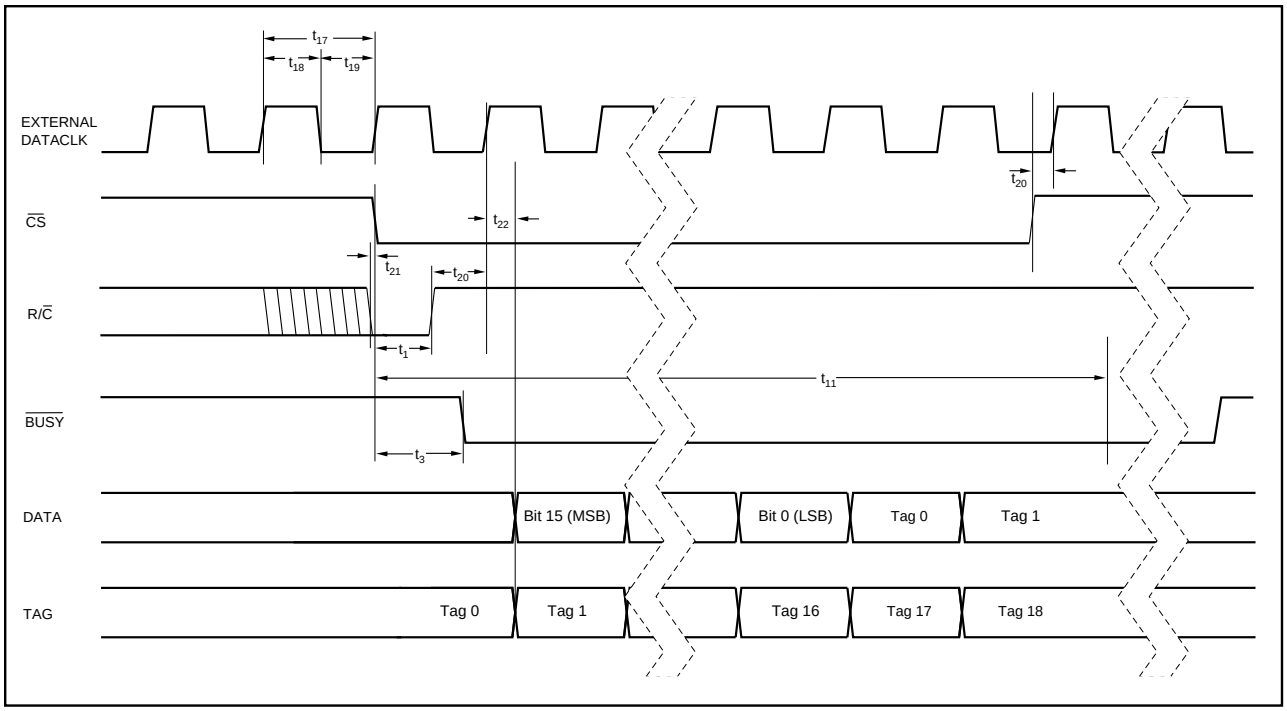


FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH) Read During a Conversion.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 16th falling edge and 17th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 17th falling edge and the 18th rising edge of DATACLK; the second input bit will be valid on the 18th falling edge and the 19th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 16 bits of valid data have been output.

INPUT RANGES

The ADS7807 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range (see Figure 8). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. Wrapping or folding over for analog inputs outside the nominal range will not occur.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VII. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 7a).

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7807 in hardware, install the resistors shown in Figure 7a. Table VII lists the hardware trim ranges relative to the input for each input range.

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 7b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VIII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 7b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

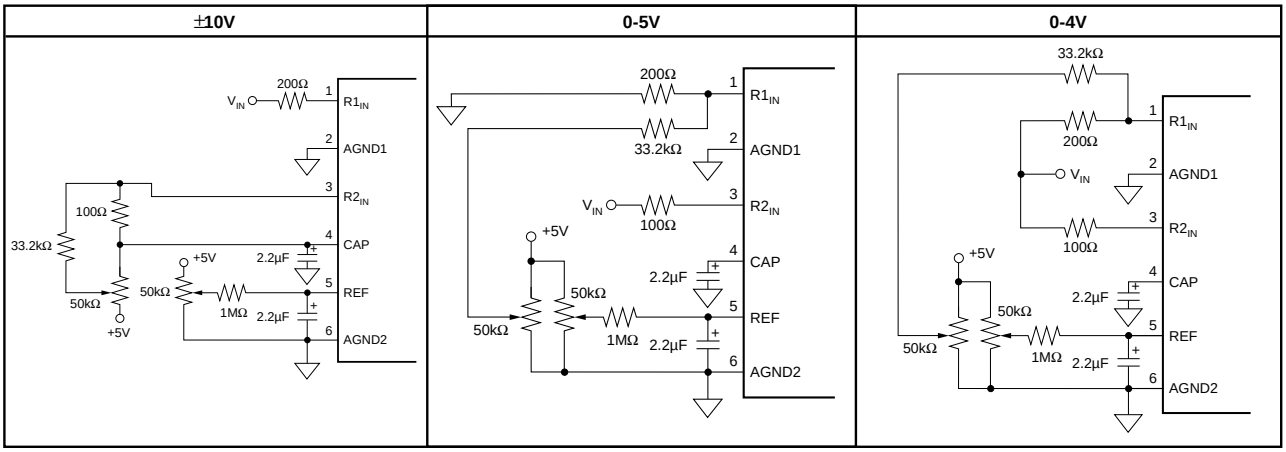


FIGURE 7a. Circuit Diagrams (With Hardware Trim).

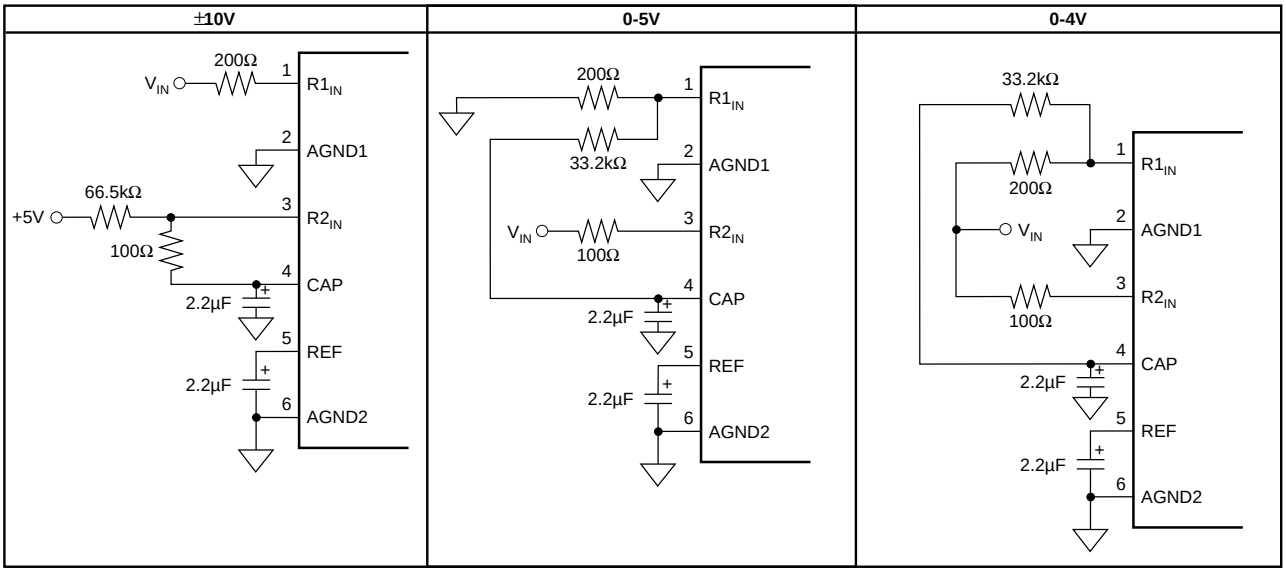


FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VIII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 8 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 9. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full scale specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ADS7807 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing

INPUT RANGE (V)	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	–10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	15	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–0.3 ≤ G ≤ 0.5 –0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	–3 ≤ UPO ≤ 3	–12 ≤ UPO ≤ –3	–7.5	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
0 to 4	–3 ≤ UPO ≤ 3	–10.5 ≤ UPO ≤ –1.5	–6	–0.4 ≤ G ≤ 0.4 –0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
Note: (1) High Grade.						

TABLE VIII. Range of Offset and Gain Errors with and without External Resistors.

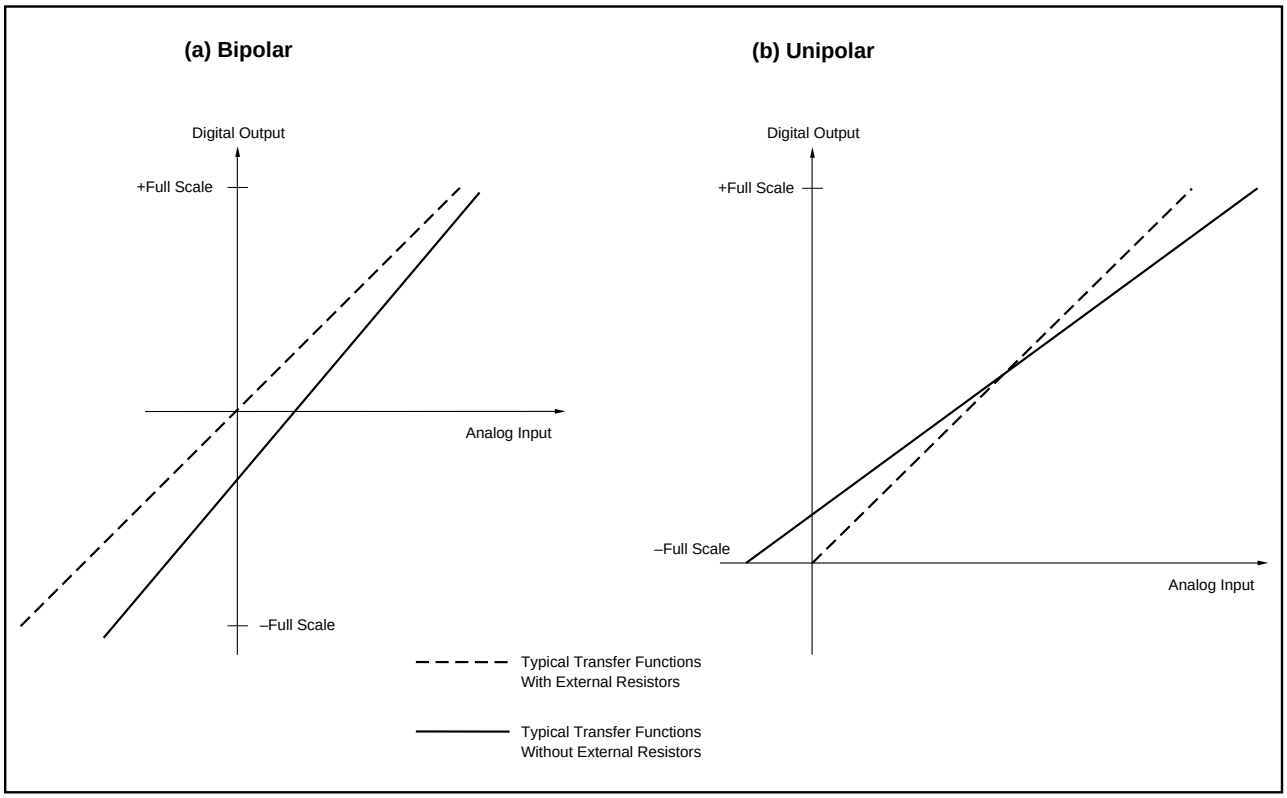


FIGURE 8. Typical Transfer Functions With and Without External Resistors.

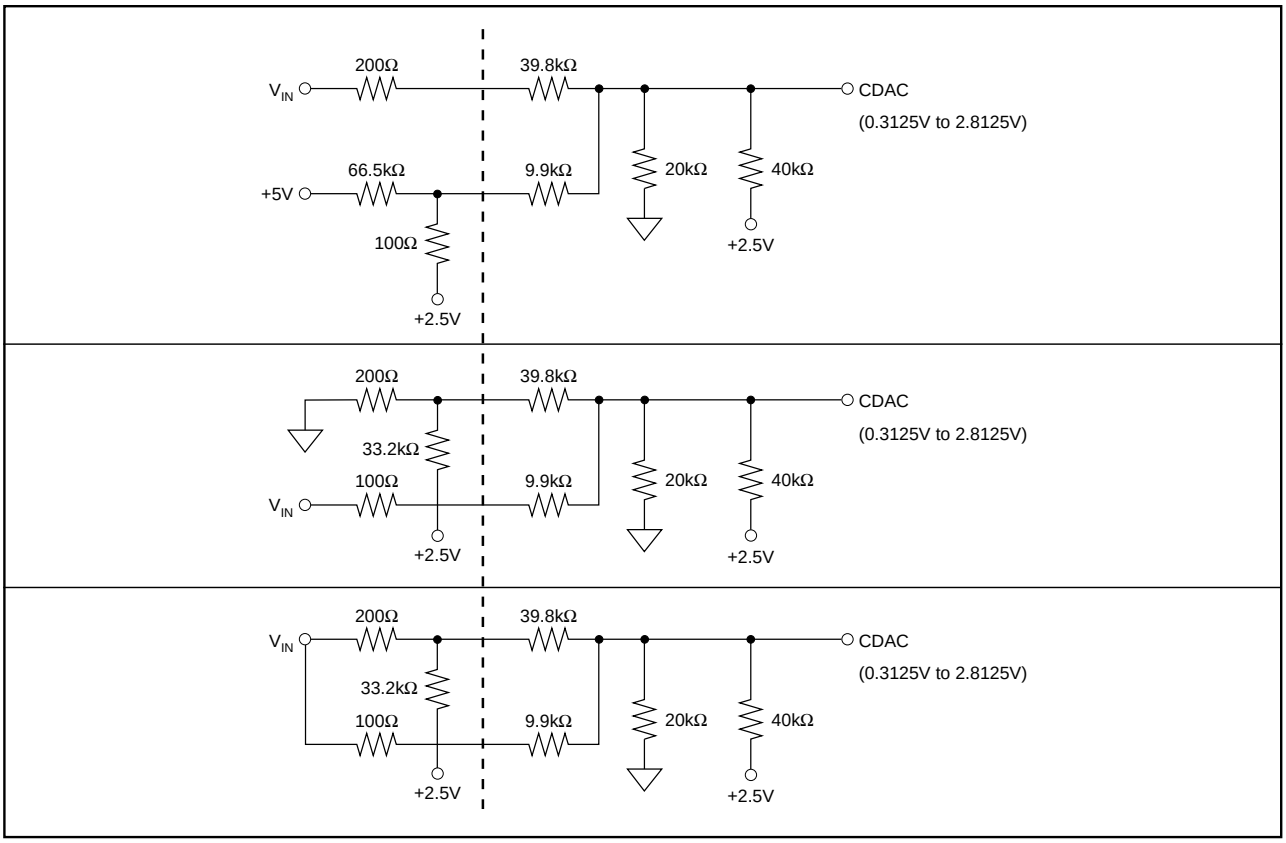


FIGURE 9. Circuit Diagrams Showing External and Internal Resistors.

the overall power consumption of the ADS7807 by approximately 5mW.

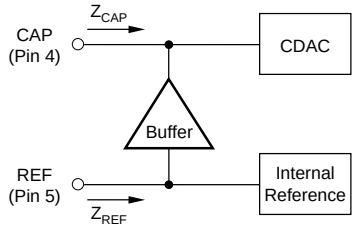
The internal reference has approximately an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS7807 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion

cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

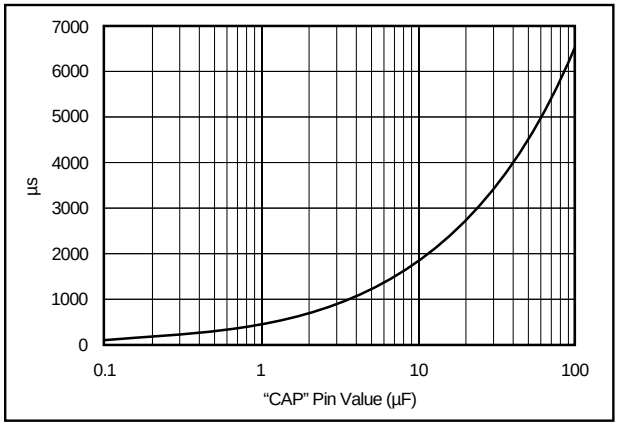


FIGURE 11. Power-Down to Power-Up Time vs Capacitor Value on CAP.

REFERENCE AND POWER DOWN

The ADS7807 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms, using a 2.2µF capacitor connected to CAP. See Figure 11 for power-down to power-up recovery time relative to the capacitor value on CAP. With +5V applied to V_{DIG}, the digital circuitry of the ADS7807 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7807 uses 90% of its power for the analog circuitry. The ADS7807 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7807. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground to which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7807 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7807.

The resistive front end of the ADS7807 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7807 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7807 has an internal LSB size of 38µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

APPLICATIONS INFORMATION

TRANSITION NOISE

Apply a DC input to the ADS7807 and initiate 1000 conversions. The digital output of the converter will vary in output codes due to the internal noise of the ADS7807. This is true for all 16-bit SAR converters. The transition noise specification found in the electrical specifications section is a statistical figure which represents the one sigma limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal output code for the input voltage value. The ±1σ, ±2σ, and ±3σ distributions will represent 68.3%, 95.5%, and 99.7% of all codes. Multiplying TN by 6 will yield the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the 5 code distribution when executing 1000 conversions. The ADS7807 has a TN of 0.8 LSBs which yields 5 output codes for a ±3σ distribution. See Figures 12 and 13 for 1000 and 10,000 conversion histogram results.

AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$ where n is the number of averages. For example, averaging four conversion results will reduce the TN by 1/2 to 0.4 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to lowpass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by two, the signal-to-noise ratio will improve 3dB.

QSPI INTERFACING

Figure 14 shows a simple interface between the ADS7807 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7807 is the only serial peripheral.

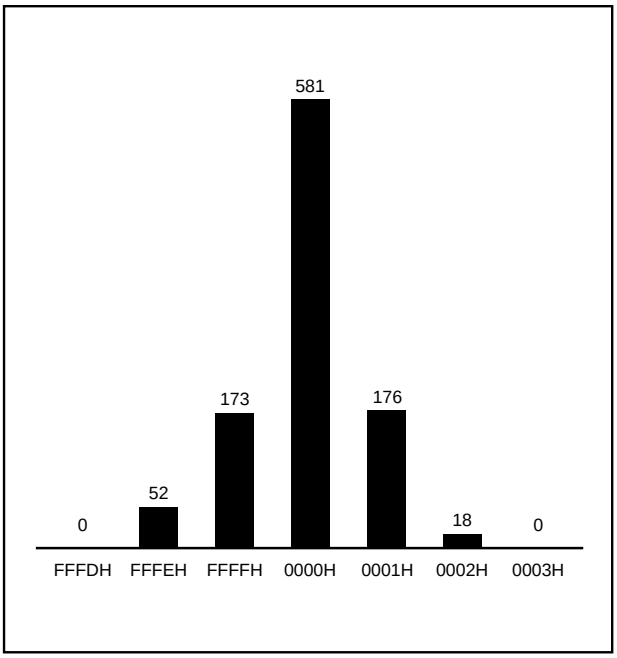


FIGURE 12. Histogram of 1000 Conversions with Input Grounded.

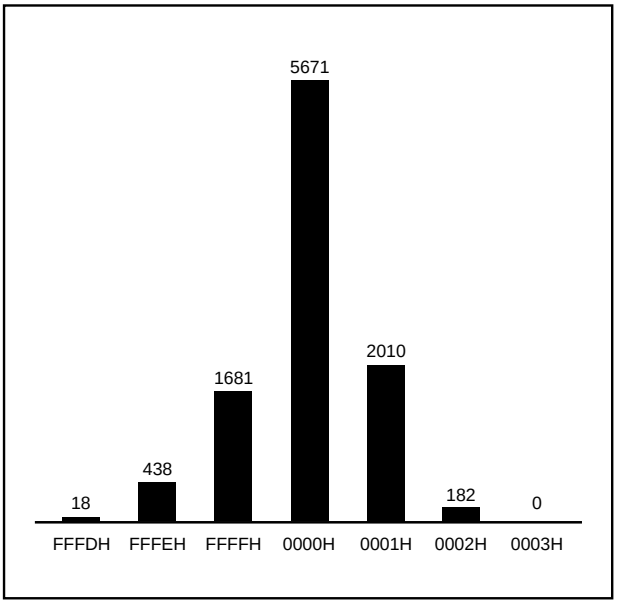


FIGURE 13. Histogram of 10,000 Conversions with Input Grounded.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select (SS) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D may be "out-of-sync".

Figure 15 shows another interface between the ADS7807 and a QSPI equipped microcontroller which allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7807 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated.

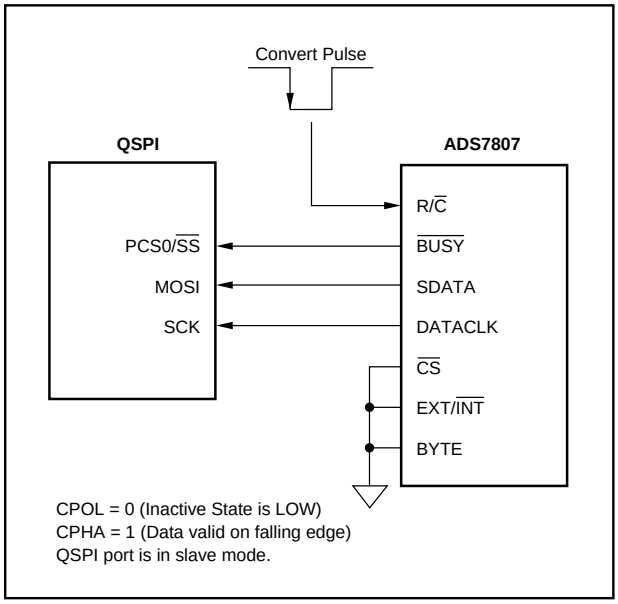


FIGURE 14. QSPI Interface to the ADS7807.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW starting a conversion. The second, a sixteen bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7807. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to 16 bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently

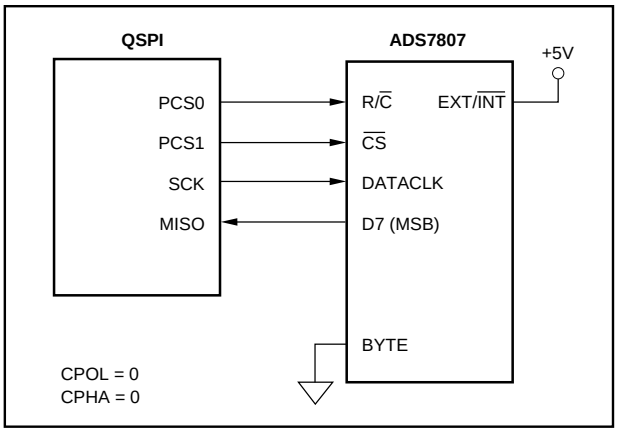


FIGURE 15. QSPI Interface to the ADS7807. Processor Initiates Conversions.

initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the sixteen bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 14. The microcontroller will need to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 15 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has SPI compatibility mode with some enhancements. Figure 16 shows an interface between the ADS7807 and the DSP56000 which is very similar to the QSPI interface seen in Figure 14. As mentioned in the QSPI section, the DSP56000 must be programmed to enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 17. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to three.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet shows that the pulse width is (0.7) RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is exactly 40kHz. Note that this will not be the case for the ADS7806. See the ADS7806 data sheet for more information.

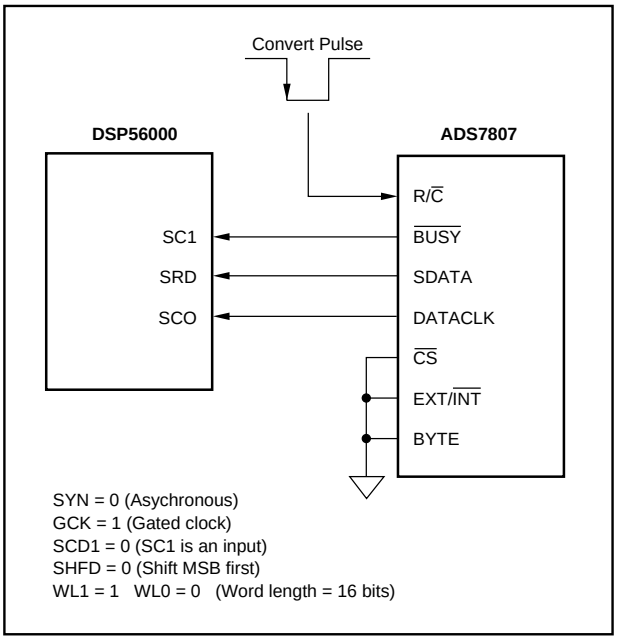


FIGURE 16. DSP56000 Interface to the ADS7807.

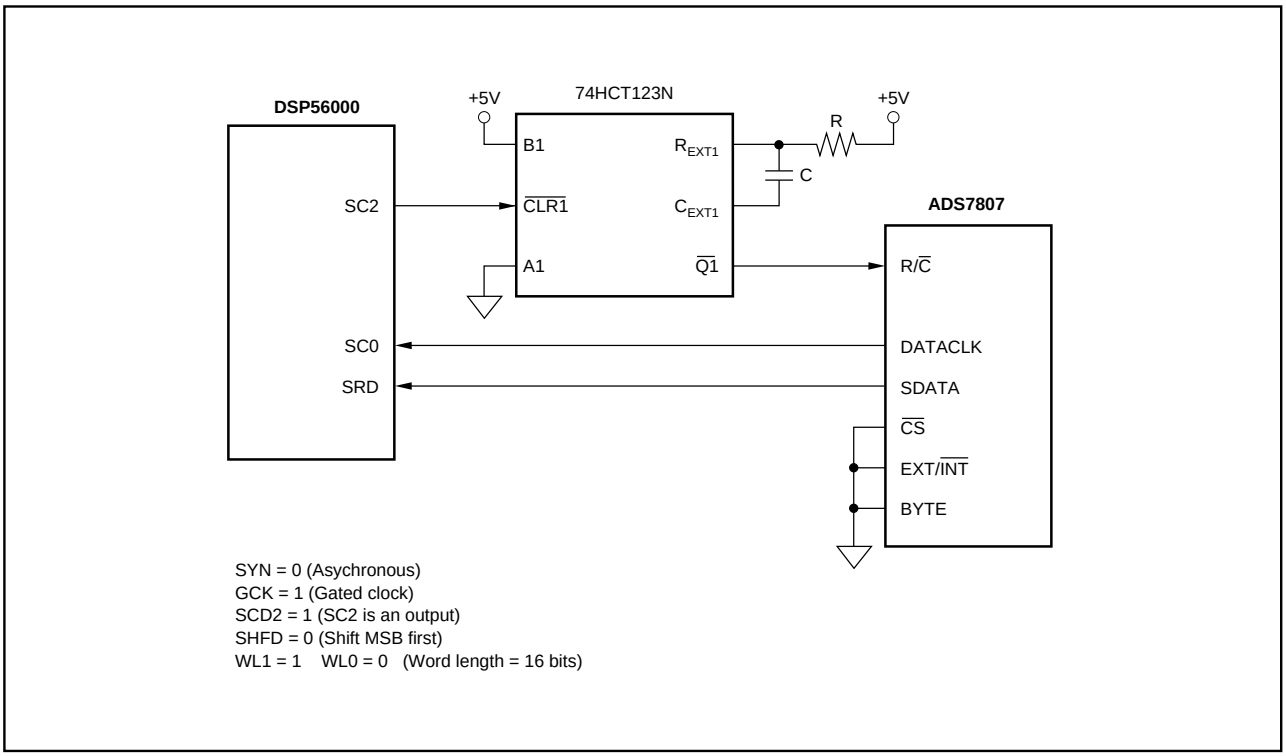


FIGURE 17. DSP56000 Interface to the ADS7807. Processor Initiates Conversions.

7 APPENDIX D

PCM-A/D Demo Software Source Listing

```
/* pcmad.c Copyright 1996 WinSystems. All Rights Reserved */
/*****************************************************************************
*
*     Project           : PCM-AD12
*
*     Purpose           : Test, Example code, calibration code
*
*     Revision    : 1.02
*
*     Date        : January 15, 1996
*
*     Author            : Steve Mottin
*
*****************************************************************************
*
*     Changes :
*
*           Revision    Date        Desciption
*           --------    ------
            ---------------------------------------------
*           1.00        10/22/95    Original
*           1.01        01/15/96    Removed swap code for REV A board deficiency.
*           1.02        02/07/96    Clean-up and comments for release.
*
*****************************************************************************
*/

/* Permission is hereby granted to users of the Winsystems PCM-A/D-12 and
   PCM-A/D-16 boards to freely use this source code as-is or in any user
   modified form for personal or commercial use. WinSystems provides this
   sample source code on an as-is basis and makes no warranty as to fitness
   of purpose. In no event shall WinSystems be liable for consequential,
   incidental or special damages of any kind through the use of this
   software source code or works derived thereof.
*/

#include <stdio.h>
#include <dos.h>
#include <conio.h>

/* The BASE address of the board is assumed to be at 110H. Change this define
   to change the base address.
*/

#define AD_BASE 0x110

/* The interrupt used is assumed to be IRQ5. The vector for IRQ5 is 8 + 5 = 13.
   The mask for IRQ5 is (1 << 5) = 0x20. Change these two appropriately for a
   different interrupt.
*/

#define IRQ_VECTOR 0x0d
#define IRQ_MASK 0x20


/* Function prototypes for functions used in this module */

void wait_complete(void);
void interrupt (*old_isr)();
void interrupt ad_isr();
```

```
/* These four arrays, store the low, high, and current values for each
   of the 16 channels. There are more elegant ways to code this but this
   is the ultimate in simplicity.
*/
unsigned current_val[16];
unsigned high_val[16];
unsigned low_val[16];
char flag[16];

/* Various global variables used to keep track of the current channel
   and the floating point values used in calculating voltages.
*/
unsigned channel_number;
float full_scale = 5.00;
float offset_val = 0.00;
unsigned full_count = 65520;
int max_channel = 16;
int interrupt_mode = 1;
long interrupt_count = 0;
int mode = 0;


/* Program entry point */

void main()
{
unsigned char lsb,msb;
char c;
unsigned low,high,current;
int channel;

      channel_number = 0;

      /* To start we, will install our interrupt handler, saving the old handler
         for when we exit.
    */

      disable();
      old_isr = getvect(IRQ_VECTOR);
      setvect(IRQ_VECTOR,ad_isr);
      enable();

      /* This is the restart point whenever we change modes. I usually go to
         extreme efforts to avoid using "goto" in C, but in this case it is
         only used for a special occasion and it's not to hard to follow
      */

restart:

      /* Clear the screen and display the the headers */

      clrscr();         /* Clear the screen */
      window(1,1,80,25 );
      printf("Channel  RAW    HIGH   LOW    DATA   CURRENT    MAX       MIN
VOLTAGE  \n");
      printf("Number   DATA   DATA   DATA   DEV.   VOLTAGE    VOLTAGE   VOLTAGE
DEVIATION\n");
      printf
("--------------------------------------------------------------------------
```

```
\n");

      /* Display  all of the channel numbers and clear the flags */

      for(channel = 0; channel < max_channel; channel++)
      {
            flag[channel] = 0;
            gotoxy(1,channel + 4);
            printf(" %02d",channel);
      }

      /* Display the screen footer */

      gotoxy(1,21);
      printf
("-------------------------------------------------------------------------------
\n");
      printf("'T' Toggle Scale, 'B' Converter toggle 'M' Interrupt toggle, 'R'
Reset values\n");
      printf
("-------------------------------------------------------------------------------
\n");

      /* Display mode dependent screen information */

      gotoxy(1,25);


      switch(mode)
      {
            case 0:
                  printf("Scale : +0  to  +5 Volts - Single-Ended");
                  break;
            case 1:
                  printf("Scale : -10 to +10 Volts - Single-Ended");
                  break;
            case 2:
                  printf("Scale : +0  to  +5 Volts - Differential");
                  break;
            case 3:
                  printf("Scale : -10 to +10 Volts - Differential");
                  break;
      }
      if(full_count == 65535)
            printf(" 16-Bit");
      else
            printf(" 12-Bit");

      gotoxy(48,25);
      if(interrupt_mode)
            printf("Interrupt Mode");
      else
            printf("Polled Mode   ");


      /* Enable and unmask interrupts as specified by the "interrupt_mode"
         variable.
       */

      interrupt_count = 0;
```

```
	if(!interrupt_mode)
		outportb(0x21,inportb(0x21) | IRQ_MASK);
	else
	{
		outportb(0x21,inportb(0x21) & ~IRQ_MASK);
		outportb(AD_BASE+1,channel_number); /* Jump start the background task
*/
	}

	/* This loop runs until we exit or until we change modes */

	while(1)
	{
		if(kbhit())
		{
			/* If a kestroke detected, see what is is and handle it
			   accordingly.

			   The keys recognized are :

				r - reset deviation values.
				t - toggle voltage mode.
				m - toggle betweent interrupt and polled mode.
			*/

			c = getch();
			if(c == 'r')
			{
				for(channel = 0; channel < max_channel; channel++)
					flag[channel] = 0;
			}
			else if(c == 't')
			{
				mode++;
				mode = mode & 3;
				if(mode == 0)	/* 0-5V Single-Ended */
				{
					max_channel = 16;
					offset_val = 0.0;
					full_scale = 5.0;
					goto restart;
				}
				if(mode == 1)	/* +-10V Single Ended */
				{
					max_channel = 16;
					offset_val = 10.0;
					full_scale = 20.0;
					goto restart;

				}
				if(mode == 2) /* 0-5V Differential */
				{
					max_channel =  8;
					offset_val = 0.0;
					full_scale = 5.0;
					goto restart;
				}
				if(mode == 3) /* +-10V differential */
```

```
                        {
                              max_channel = 8;
                              offset_val = 10.0;
                              full_scale = 20.0;
                              goto restart;
                        }

                  }
                  else if(c == 'm')
                  {
                        interrupt_mode++;
                        interrupt_mode = interrupt_mode & 1;
                        goto restart;
                  }
                  else if(c == 'b')
                  {
                        full_count = full_count ^ 0x000f;
                        goto restart;
                  }
                  else
                        break;
            }

            /* Go through channel by channel displaying the current value */

            for(channel = 0; channel < max_channel; channel++)
            {
                  /* If we're not in interrupt mode. We must poll the channel
                     before displaying it's value.
                  */

                  if(!interrupt_mode)
                  {
                        outportb(AD_BASE+1,channel);        /* Start the
conversion */
                        wait_complete();        /* wait for the channel to
complete */

                        lsb = inportb(AD_BASE+1);     /* assemble the word result
*/
                        msb = inportb(AD_BASE+2);     /* from the two byte values
read */

                        current_val[channel] = (msb << 8) | lsb;

                        if(!flag[channel])      /* If this is the first time for
this channel */
                        {
                              high_val[channel] = current_val[channel];
                              low_val[channel] = current_val[channel];
                              flag[channel]++;  /* Set the flag, we've don this
channel */
                        }

                        if(mode & 1)      /* If a signed mode, do the compare
correctly */
                        {
                              if((current_val[channel] ^ 0x8000) < (low_val
[channel] ^ 0x8000))
                                    low_val[channel] = current_val[channel];
```

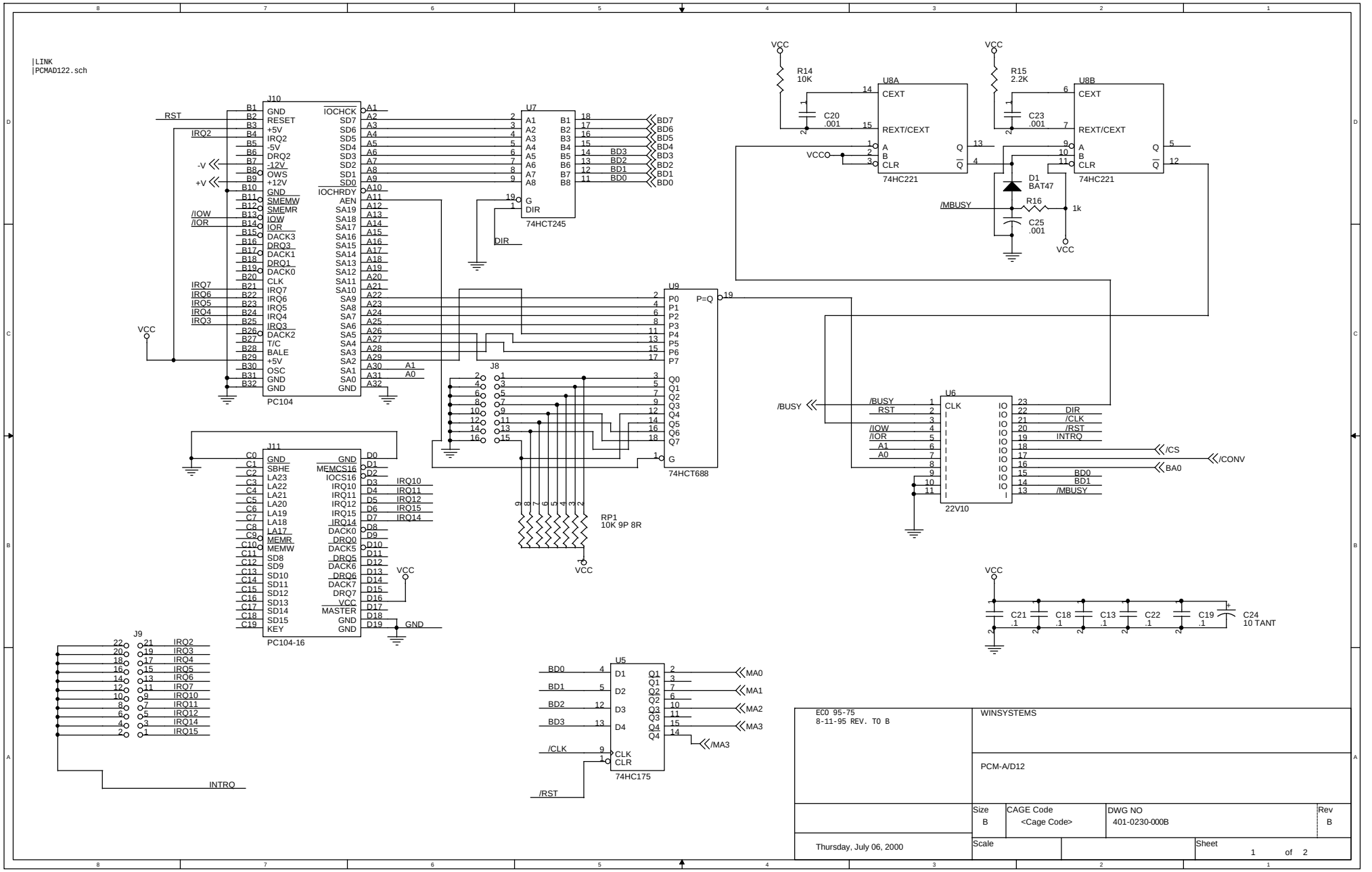
```
                              if((current_val[channel] ^ 0x8000) > (high_val
[channel] ^ 0x8000))
                                    high_val[channel] = current_val[channel];
                        }
                        else
                        {
                              if(current_val[channel] < low_val[channel])
                                    low_val[channel] = current_val[channel];
                              if(current_val[channel] > high_val[channel])
                                    high_val[channel] = current_val[channel];
                        }
                  }

                  gotoxy(10,channel + 4);
                  printf("%04X   %04X   %04X   ",current_val[channel],high_val
[channel],low_val[channel]);
                  printf("%04X  ",high_val[channel] - low_val[channel]);
                  if(mode & 1)  /* If signed mode, adjust values when printing */
                  {
                        printf("%8.4f  ",(((float)(current_val[channel] ^ 0x8000)
/ (float)full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",(((float)(high_val[channel] ^ 0x8000) /
(float)full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",(((float)(low_val[channel] ^ 0x8000) /
(float)full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",((float)((high_val[channel] ^ 0x8000) -
(low_val[channel]) ^ 0x8000) / (float)full_count) * full_scale);
                  }
                  else
                  {
                        printf("%8.4f  ",(((float)current_val[channel] / (float)
full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",(((float)high_val[channel] / (float)
full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",(((float)low_val[channel] / (float)
full_count) * full_scale) - offset_val);
                        printf("%8.4f  ",((float)(high_val[channel] - low_val
[channel]) / (float)full_count) * full_scale);
                  }
                  if(channel < (max_channel-1))
                        printf(" ");

                  /* In interrupt mode, display a counter of the number of
                     interrupts that have occured.
                  */
                  if(interrupt_mode)
                  {
                        gotoxy(65,25);
                        printf("%ld",interrupt_count);
                  }
            }
      }

      /* Be sure to restore the original interrupt state before exit */

      disable();
      outportb(0x21,inportb(0x21) | IRQ_MASK);
      setvect(IRQ_VECTOR,old_isr);
      enable();
```

```
      clrscr();
}

/* This function polls the AD chip awaiting the completion of the conversion
   in progress.
*/

void wait_complete()
{
int stat;

      while(1)
      {
            stat = inportb(AD_BASE);  /* Read status */
            if((stat & 0x03) == 3)
                  break;
            if(kbhit()) /* We allow a keystroke to also get us out */
                  break;
      }
}

/* This is the interrupt service routine. It reads the current channel,
   compares it against maximum deviation values and stores the results
   in the arrays for display by the foreground routine.
*/

void interrupt ad_isr()
{
int temp;
unsigned char lsb,msb;
unsigned current;

      ++interrupt_count;
      temp = channel_number;

      lsb = inportb(AD_BASE+1);
      msb = inportb(AD_BASE+2);

      ++channel_number;
      if(channel_number > (max_channel-1))
            channel_number = 0;

      outportb(AD_BASE+1,channel_number);       /* start next channel converting
*/

      current = (msb << 8) | lsb;

      current_val[temp] = current;        /* Store the current reading */

      if(!flag[temp])
      {
            high_val[temp] = current;
            low_val[temp] = current;
            flag[temp]++;
      }

      if(mode & 1)      /* If a signed mode, do the comparisons correctly */
      {
            if((current ^ 0x8000) < (low_val[temp] ^ 0x8000))
                  low_val[temp] = current;
```

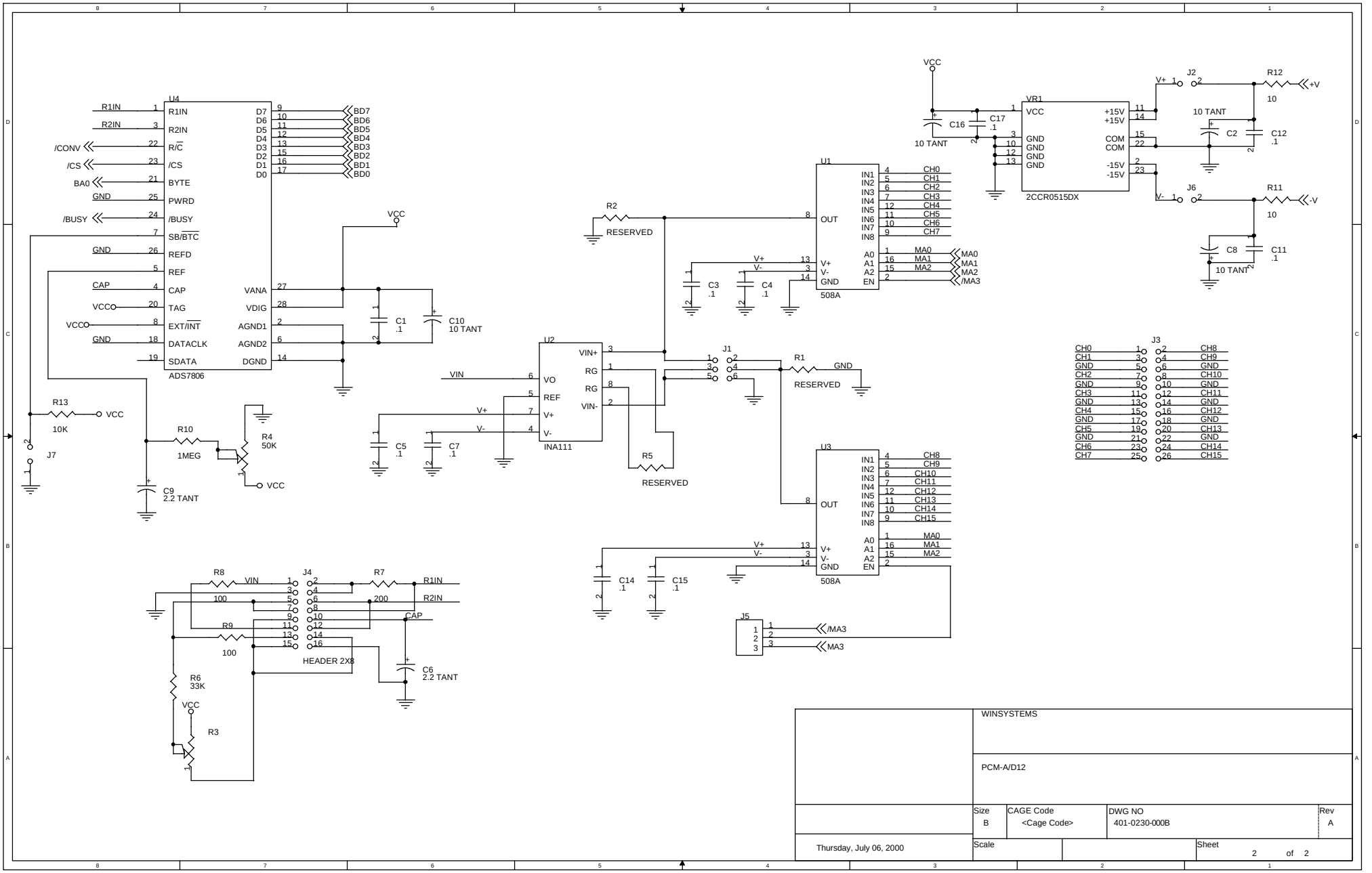
```
            if((current ^ 0x8000) > (high_val[temp] ^ 0x8000))
                  high_val[temp] = current;
      }
      else
      {
            if(current < low_val[temp])
                  low_val[temp] = current;
            if(current > high_val[temp])
                  high_val[temp] = current;
      }

      /* Send the EOI to the interrupt controller to re-arm for next interrupt */
      outportb(0x20,0x20);
}
```

8 APPENDIX E

PCM-A/D Schematic Diagrams



ECO 95-75 8-11-95 REV. TO B	WINSYSTEMS		
	PCM-A/D12		
	Size: B	CAGE Code: <Cage Code>	DWG NO: 401-0230-000B — Rev: B
Thursday, July 06, 2000	Scale:		Sheet: 1 of 2



Telephone: 817-274-7553 . . Fax: 817-548-1358
http://www.winsystems.com . . E-mail: info@winsystems.com

WARRANTY

WinSystems warrants that for a period of two (2) years from the date of shipment any Products and Software purchased or licensed hereunder which have been developed or manufactured by WinSystems shall be free of any material defects and shall perform substantially in accordance with WinSystems' specifications therefore. With respect to any Products or Software purchased or licensed hereunder which have been developed or manufactured by others, WinSystems shall transfer and assign to Customer any warranty of such manufacturer or developer held by WinSystems, provided that the warranty, if any, may be assigned. The sole obligation of WinSystems for any breach of warranty contained herein shall be, at its option, either (i) to repair or replace at its expense any materially defective Products or Software, or (ii) to take back such Products and Software and refund the Customer the purchase price and any license fees paid for the same. Customer shall pay all freight, duty, broker's fees, insurance changes and other fees and charges for the return of any Products or Software to WinSystems under this warranty. WinSystems shall pay freight and insurance charges for any repaired or replaced Products or Software thereafter delivered to Customer within the United States. All fees and costs for shipment outside of the United States shall be paid by Customer. The foregoing warranty shall not apply to any Products or Software which have been subject to abuse, misuse, vandalism, accidents, alteration, neglect, unauthorized repair or improper installations.

THERE ARE NO WARRANTIES BY WINSYSTEMS EXCEPT AS STATED HEREIN. THERE ARE NO OTHER WARRANTIES EXPRESS OR IMPLIED INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, IN NO EVENT SHALL WINSYSTEMS BE LIABLE FOR CONSEQUENTIAL, INCIDENTAL, OR SPECIAL DAMAGES INCLUDING, BUT NOT LIMITED TO, DAMAGES FOR LOSS OF DATA, PROFITS OR GOODWILL. WINSYSTEMS' MAXIMUM LIABILITY FOR ANY BREACH OF THIS AGREEMENT OR OTHER CLAIM RELATED TO ANY PRODUCTS, SOFTWARE, OR THE SUBJECT MATTER HEREOF, SHALL NOT EXCEED THE PURCHASE PRICE OR LICENSE FEE PAID BY CUSTOMER TO WINSYSTEMS FOR THE PRODUCTS OR SOFTWARE OR PORTION THEREOF TO WHICH SUCH BREACH OR CLAIM PERTAINS.

WARRANTY SERVICE

All products returned to WinSystems must be assigned a Return Material Authorization (RMA) number. To obtain this number, please call or FAX WinSystems' factory in Arlington, Texas and provide the following information:

1. Description and quantity of the product(s) to be returned including its serial number.
2. Reason for the return.
3. Invoice number and date of purchase (if available), and original purchase order number.
4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

After the RMA number is issued, please return the products promptly. Make sure the RMA number is visible on the outside of the shipping package.

The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.