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OPERATIONS MANUAL
PCM-D/A12

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REVISION HISTORY

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1 GENERAL INFORMATION

1.1 Features

- PC/104 Form Factor
- 8 Independent Analog Output Channels
- 12-Bit D/A Resolution
- 0-5V, 0-10V and +/-5V Ranges configurable on each channel
- Extended Temperature -40°C to +85°C
- No Alignment Required
- Low Power Consumption
- Optional DC-DC Converter
- 10uS Maximum Settle Time

1.2 General Description

The PCM-D/A-12 is a low cost, general purpose, analog output board in a small PC/104 form factor. It provides 8 channels of 12-bit analog output each of which can be individually configured for any of three output ranges, 0-5V, 0-10V, and +/-5V. The maximum settling rate of 10uS allows for update speeds of better than 100KHz. The PCM-D/A-12 uses up to 4 of the popular Analog Devices AD7237 converters, each of which supports 2 independent output channels.

1.3 Specifications

1.3.1 Electrical

Bus Interface : PCM-D/A12-8 PC/104 8-Bit stackthrough
PCM-D/A12-16 PC/104 16-Bit stackthrough

Power Requirements :

+5V +/-5% at 450mA typ. with DC-DC installed
75mA typ. w/o DC-DC installed

+12V +/-5% at 35mA typ. w/o DC-DC converter installed

-12V +/-5% at 7mA typ. w/o DC-DC converter installed

1.3.2 Mechanical

Dimensions : 3.6" X 3.8" X 0.6"

PC Board : FR4 Epoxy glass with 2 signal layers and 2 power planes with screened component legend and plated through holes.

Jumpers : 0.025" square posts on 0.10" centers.

Connectors : Analog output 16-pin 0.10" grid RN type IDH-16-LP

1.3.3 Environmental

Operating Temperature : -40° C to +85° C

Non-Condensing relative humidity : 5% to 95%

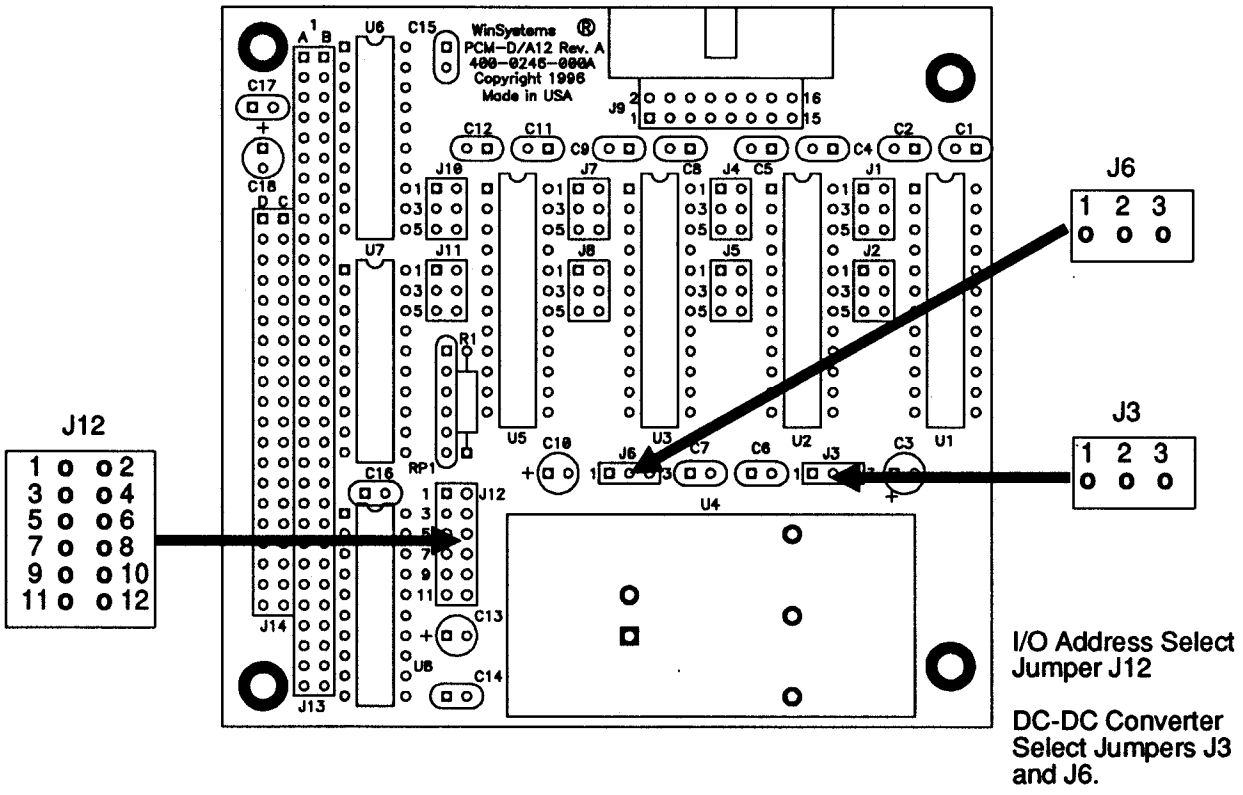
2 PCM-D/A12 Technical Reference

2.1 Introduction

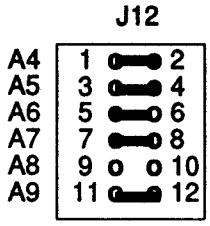
This section of the manual is intended to provide sufficient information regarding the configuration and usage of the PCM-D/A12 module. WinSystems maintains a Technical Support Group to help answer questions regarding configuration and programming of the board. For answers to questions not adequately addressed in this manual contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time. Technical support may also be requested via FAX at (817) 548-1358.

The PCM-D/A12 has 8 independently configurable D/A output channels each of which can be individually updated by software. Section 3 of this manual provides additional details regarding the programming of the module.

2.2 I/O Address selection



The PCM-D/A-12 uses 16 consecutive I/O addresses with the base address determined by the setting of the jumpers on J12. Each position on J12 corresponds to an address bit. A jumper installed matches a '0' in the address and a jumper left open matches a '1' in the address. The illustration below shows the relationship between the jumper positions and the address bits and also shows the correct jumpering for a base I/O address of 100H.



BASE I/O ADDRESS 100H

2.3 DC-DC Converter Select

The PCM-D/A-12 needs a DC-DC converter to supply the full +/-15 volts required for full output capability. When the DC-DC converter is installed, +/-12 volts are not required. There is, however, a fairly hefty current demand (See Specifications page) when the DC-DC converter is installed. It is possible to operate the board without the DC-DC converter if only the 0-5V range and/or the +/-5V range is required. Also note that the D/A linearity is affected by supply voltage as shown in the Typical Performance Graphs present in Appendix C. Jumper blocks at J3 and J6 allow selection of the DC-DC converter when installed as shown in the illustration below. The factory will normally configure these jumpers depending on the presence of the DC-DC converter.

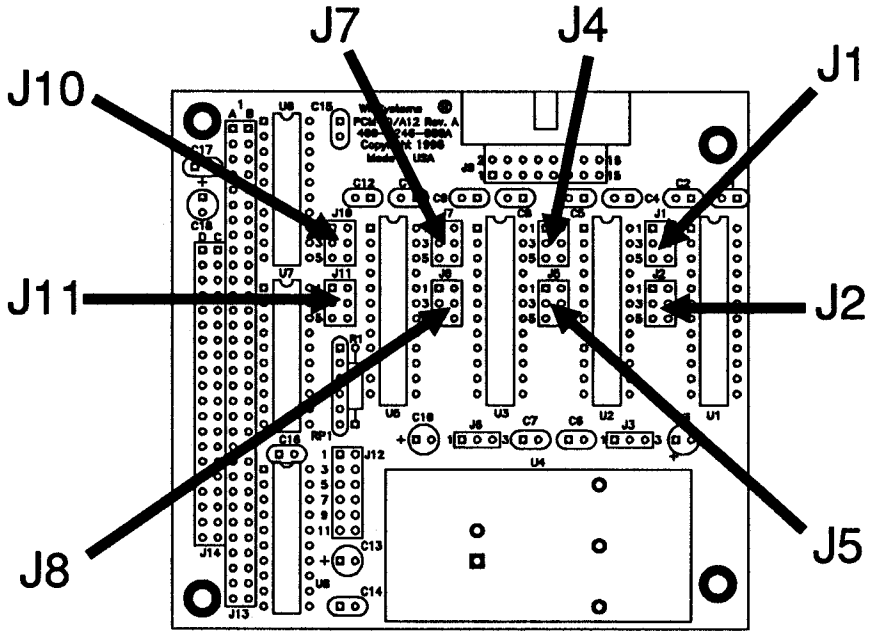


DC-DC Converter Installed



DC-DC Converter Absent

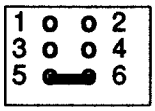
2.4 Output Mode Selection



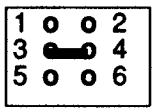
Each of the 8 output channels is individually configurable as to the output range. The correlation between the channel and the jumper controlling its range is shown here :

Channel 0 - J10
Channel 1 - J11
Channel 2 - J7
Channel 3 - J8
Channel 4 - J4
Channel 5 - J5
Channel 6 - J1
Channel 7 - J2

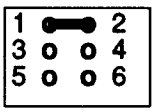
There are 3 output ranges available for each channel as shown in the following illustration.



0V to 5V Range



0V to 10V Range



-5V to +5V Range

2.5 Output Connector Pin Definitions

The 8 D/A channels are terminated at the output connector J9. The pin definitions for J9 are shown below :

J9

Channel 0	1 o	o 2	AGND
Channel 1	3 o	o 4	AGND
Channel 2	5 o	o 6	AGND
Channel 3	7 o	o 8	AGND
Channel 4	9 o	o 10	AGND
Channel 5	11 o	o 12	AGND
Channel 6	13 o	o 14	AGND
Channel 7	15 o	o 16	AGND

2.6 PC/104 BUS Pin Definitions

The PC/104 connectors at J13 and J14 are shown here with their signal designations.

J13

GND	B1 o	o A1	IOCHK
RESET	B2 o	o A2	BD7
+5V	B3 o	o A3	BD6
IRQ9	B4 o	o A4	BD5
-5V	B5 o	o A5	BD4
DRQ2	B6 o	o A6	BD3
-12V	B7 o	o A7	BD2
0WS	B8 o	o A8	BD1
+12V	B9 o	o A9	BD0
GND	B10 o	o A10	IOCHRDY
SMEMW	B11 o	o A11	AEN
SMEMR	B12 o	o A12	SA19
IOW	B13 o	o A13	SA18
IOR	B14 o	o A14	SA17
DACK3	B15 o	o A15	SA16
DRQ3	B16 o	o A16	SA15
DACK1	B17 o	o A17	SA14
DRQ1	B18 o	o A18	SA13
REFRESH	B19 o	o A19	SA12
SYSCLK	B20 o	o A20	SA11
IRQ7	B21 o	o A21	SA10
IRQ6	B22 o	o A22	SA9
IRQ5	B23 o	o A23	SA8
IRQ4	B24 o	o A24	SA7
IRQ3	B25 o	o A25	SA6
DACK2	B26 o	o A26	SA5
TC	B27 o	o A27	SA4
BALE	B28 o	o A28	SA3
+5V	B29 o	o A29	SA2
OSC	B30 o	o A30	SA1
GND	B31 o	o A31	SA0
GND	B32 o	o A32	GND

J14

GND	C0 o	o D0	GND
SBHE	C1 o	o D1	MEMCS16
LA23	C2 o	o D2	IOCS16
LA22	C3 o	o D3	IRQ10
LA21	C4 o	o D4	IRQ11
LA20	C5 o	o D5	IRQ12
LA19	C6 o	o D6	IRQ15
LA18	C7 o	o D7	IRQ14
LA17	C8 o	o D8	DACK0
MEMR	C9 o	o D9	DRQ0
MEMR	C10 o	o D10	DACK5
SD8	C11 o	o D11	DRQ5
SD9	C12 o	o D12	DACK6
SD10	C13 o	o D13	DRQ6
SD11	C14 o	o D14	DACK7
SD12	C15 o	o D15	DRQ7
SD13	C16 o	o D16	+5V
SD14	C17 o	o D17	MASTER
SD15	C18 o	o D18	GND
KEY	C19 o	o D19	GND

2.7 Connector/Jumper Summary

Connector/ Jumper	Description	Page Reference
J1	Channel 6 mode select jumper	2-3
J2	Channel 7 mode select jumper	2-3
J3	DC-DC Converter Select jumper	2-2
J4	Channel 4 mode select jumper	2-3
J5	Channel 5 mode select jumper	2-3
J6	DC-DC Converter Select jumper	2-2
J7	Channel 2 mode select jumper	2-3
J8	Channel 3 mode select jumper	2-3
J9	Analog output connector	2-4
J10	Channel 0 mode select jumper	2-3
J11	Channel 1 mode select jumper	2-3
J12	I/O Address select jumper	2-2
J13	PC/104-8 Connector	2-4
J14	PC/104-16 Connector	2-4

3 PCM-D/A-12 Programming Reference

3.1 I/O Register Definitions

Each D/A channel occupies two I/O addresses in the 80X86 I/O space. The base address of the board is determined by the jumpering of J12 as documented in section 2.2 of this manual. The entire board uses 16 I/O addresses that are allocated per the following table:

Address	Write	Read
BASE + 0	Channel 0 LSB Data	Update Channel 0
BASE + 1	Channel 0 MSB Data	N/A
BASE + 2	Channel 1 LSB Data	Update Channel 1
BASE + 3	Channel 1 MSB Data	N/A
BASE + 4	Channel 2 LSB Data	Update Channel 2
BASE + 5	Channel 2 MSB Data	N/A
BASE + 6	Channel 3 LSB Data	Update Channel 3
BASE + 7	Channel 3 MSB Data	N/A
BASE + 8	Channel 4 LSB Data	Update Channel 4
BASE + 9	Channel 4 MSB Data	N/A
BASE + 10	Channel 5 LSB Data	Update Channel 5
BASE + 11	Channel 5 MSB Data	N/A
BASE + 12	Channel 6 LSB Data	Update Channel 6
BASE + 13	Channel 6 MSB Data	N/A
BASE + 14	Channel 7 LSB Data	Update Channel 7
BASE + 15	Channel 7 MSB Data	N/A

NOTE : Reading the update register (or any register within the decoded I/O space) on ANY channel will result in the simultaneous update of ALL channels. To speed programming it is possible to load all of the MSB and LSB values and to update them all simultaneously with a single I/O read instruction.

3.2 Conversion Techniques

Programming the PCM-D/A-12 is a simple matter in any language allowing I/O type instructions. The pseudo-code sample below illustrates this simplicity :

```
OUT CHANNEL_BASE, LSB_DATA        Write the lower 8 bits of the data to the LSB port latch.
OUT CHANNEL_BASE+1, MSB_DATA      Write the upper 4 bits of the data to the MSB port latch.

 IN CHANNEL_BASE                  This read, updates the channel and transfers the MSB and
                                  LSB latch contents to the converter.
```

A sample da_out() function in Borland 'C' should further illustrate the programming interface.

```
#define DA_BASE 0x100

void da_out(int channel,unsigned data)
{
unsigned channel_base;


/* The channel argument is a value from 0 to 7 indicating the channel number to update. The data
    argument is a 12-bit value 0-4095 that will be sent to the D/A converter  */

        channel_base = DA_BASE + (channel * 2);     /* Build the base address for this channel */

        outportb(channel_base, data & 0xff);        /* Write out the lower 8-bits of the data to the
                                                       LSB data latch */

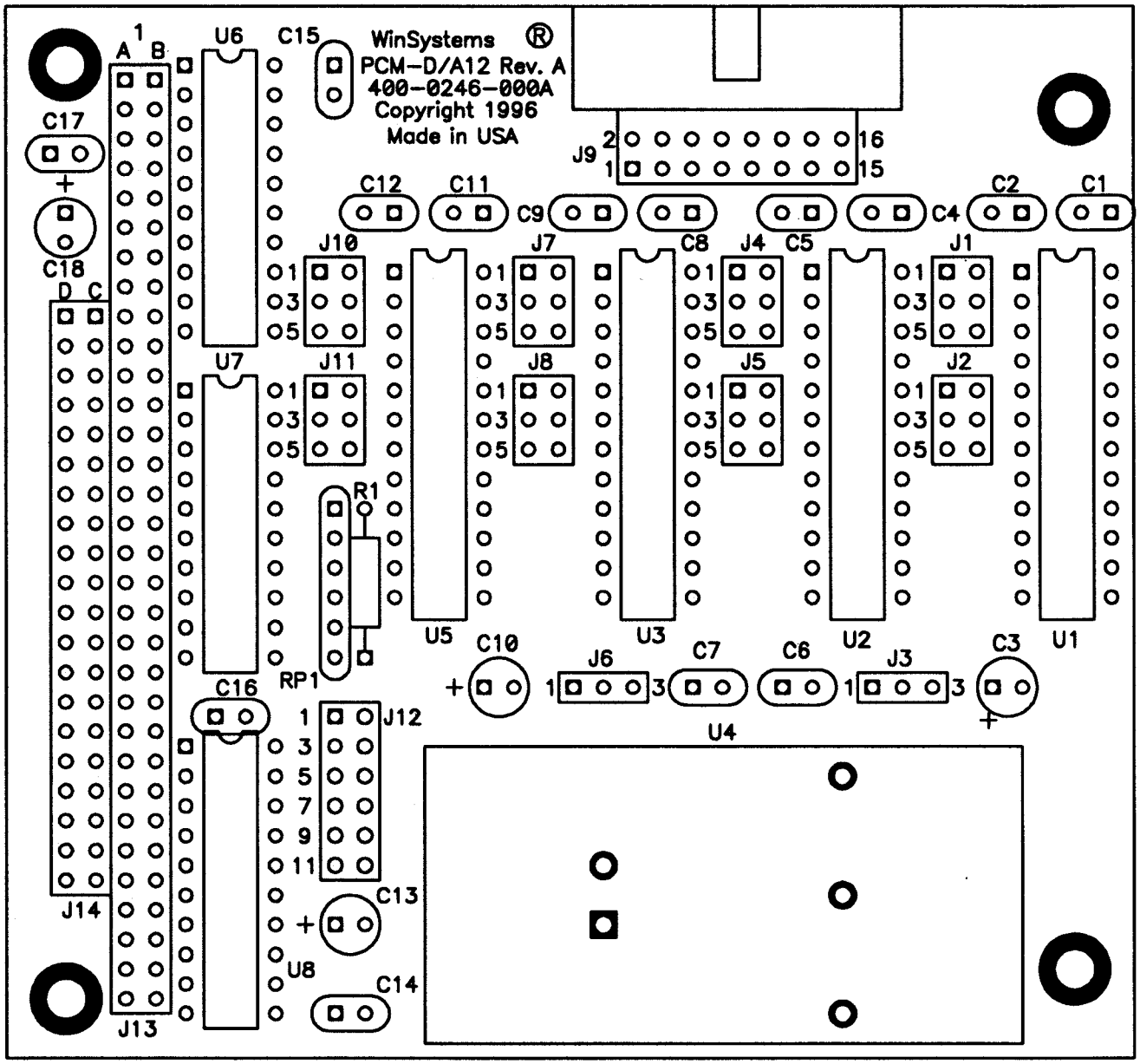
        outportb(channel_base+1, data >> 8);        /* Write out the upper 4 bits of the 12-bit data
                                                       to the MSB data latch */

         inportb(channel_base);                     /* This dummy read updates the D/A output
                                                       with the data in the MSB and LSB latches */

}
```

4 APPENDIX A

PCM-D/A12 Parts Placement Guide



5 APPENDIX B

PCM-D/A12 Parts List

BEGINNING RANGE: 0246-100-0000 ENDING RANGE: 0246-200-0000

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	0246-100-0000	ASSY PCM-D/A12 REV.A					1
2	999-9999-001	SPECIAL NOTES	02-16-96 MEB ** PRELIMINARY **	ARLIN		Inv	1
2	110-0011-003	CAP.1UF.1 SP RAD SR205E104MAATR1	C1,C2,C4,C5-C9,C11,C12,C14-C17	ARLIN		Inv	14
2	110-0042-005	CAP 10UF 35V TAN RAD 581-10M35	C3,C10,C13,C18	ARLIN		Inv	4
2	201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J1,J2,J4,J5,J7,J8,J10,J11=2X3 J12=2X6	ARLIN		Inv	.84
2	201-0036-010	HDR 1X36 UN TSW-136-07-G-S (SAM)	J3,J6=1X3	ARLIN		Inv	.17
2	201-0016-121	HDR 16 POS RA IDH-16LP-SR3-TG/TR	J9	ARLIN		Inv	1
2	200-0064-100	SCKT 64 POS STK AT-ES1-64-12-2-G	J13	ARLIN		Inv	1
2	200-0040-100	SCKT 40 P STACK ES1-40-12-2-GF (	J14	ARLIN		Inv	1
2	115-0103-050	RN SIP 6P-5 RES 10K (BKMN)L061S1	RP1	ARLIN		Inv	1
2	114-0103-450	RESISTOR 10K 1/4 5%, CR25 10k 5%	R1	ARLIN		Inv	1
2	200-0243-100	SOCKET 24 P .3 ICO-243-S8A-T (14	U1,U2,U3,U5	ARLIN		Inv	4
2	743-0036-000	DC TO DC CONV. 5V TO +/-15V DC	U4	ARLIN		Inv	1
2	200-0203-100	SOCKET 20 PIN ICO-203-S8A-T (176	U6,U7,U8	ARLIN		Inv	3
2	400-0246-000A	PCB, PCM-D/A12 REV.A	PCB, PCM-D/A12 REV.A	ARLIN		Inv	1
1	0246-200-0000	SUB ASSY PCM-D/A12 REV.A					1
2	999-9999-001	SPECIAL NOTES	02-16-96 MEB ** PRELIMINARY **	ARLIN		Inv	1
2	730-0088-000	IC, AD7237 12 BIT 2CHANNEL D/A C	U1,U2,U3,U5	ARLIN		Inv	4
2	745-0244-200	IC, 74HCT244	U6	ARLIN		Inv	1
2	745-0688-200	IC, 74HCT688	U7	ARLIN		Inv	1
2	901-0002-000	IC, EP320IPI-40 ALTERA (18)	U8 CS=_____ \PCMDA12\U8.JED	ARLIN		Inv	1
2	201-0002-000	PLUG JUMPER 999-19-310-00	*JUMPERS FOR TEST*	ARLIN		Inv	15
2	999-9999-001	SPECIAL NOTES	J1=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J2=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J3=2-3	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J4=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J5=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J6=1-2	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J7=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J8=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J10=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J11=5-6	ARLIN		Inv	1
2	999-9999-001	SPECIAL NOTES	J12=1-2 3-4 5-6 7-8 11-12	ARLIN		Inv	1

BEGINNING RANGE: 0246-100-0000 ENDING RANGE: 0246-200-0000

LEVEL ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED

REPORT RECAP

0 WARNING(S) * Indicates no BOM Found for Item
0 ERROR(S)

REPORT PARAMETERS

ASSEMBLY RANGE : 0246-100-0000 to 0246-200-0000
TYPE : RWF

COMPONENT RANGE : <FIRST> to <LAST>
TYPE : RWF

MASKING : Inv-Explode Specific Inv Items (No Masks)

QUANTITY (TO EXPLODE): 1

DESC LENGTH: ITEM : 32
COMMENT : 40
LOCATION: 0
OVERHEAD: 0

NESTING INDENT LENGTH: 20

TOTAL REPORT WIDTH : 132

6 APPENDIX C

Analog Devices AD7237 Datasheet Reprint

LC²MOS Dual 12-Bit DACPORT

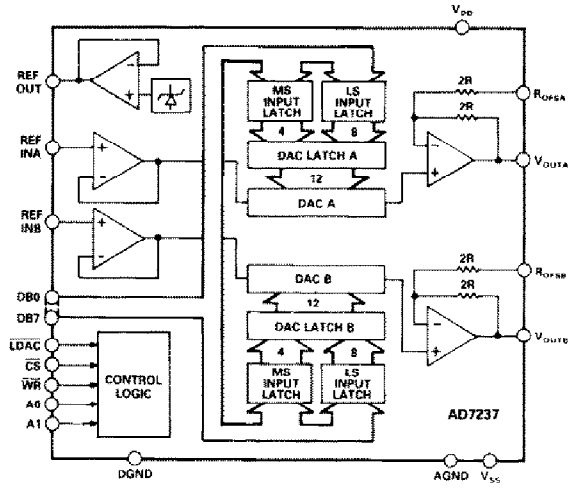
AD7237/AD7247

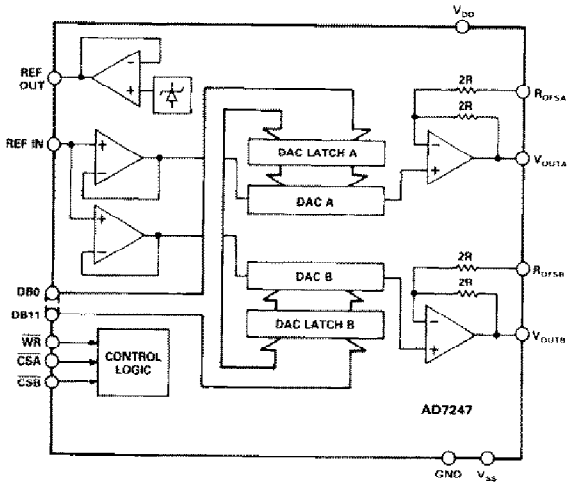
FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Parallel Loading Structure: AD7247
(8+4) Loading Structure: AD7237
Single or Dual Supply Operation
Low Power – 165 mW typ in Single Supply

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7237/AD7247 is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237 has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237 updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237/AD7247 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3" wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

DACPORT is a trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD7237/AD7247 is a dual 12-bit DACPORT™ on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. Between them, the AD7237 and AD7247 offer a versatile interface arrangement to either 8-bit or 16-bit data bus structures.

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD7237/AD7247—SPECIFICATIONS (V_{DD} = +15 V[1] ±5%, V_{SS} = 0 V or −15 V[1] ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A, S[2]	K, B, T	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	LSB max	V_{SS} = 0 V or −15 V. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±4	±4	LSB max	V_{SS} = −15 V. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 4]	±5	±5	LSB max	
Full-Scale Mismatch[4]	±1	±1	LSB typ	
REFERENCE OUTPUT				
REF OUT				
J, K, A, B Versions	4.97/5.03	4.97/5.03	Vmin/Vmax	
S, T Versions	4.95/5.05	4.95/5.05	Vmin/Vmax	
Reference Temperature Coefficient	±25	±25	ppm/°C typ	
Reference Load Change				
(ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–100 μA)
REFERENCE INPUT				
Reference Input Range	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current[5]	±5	±5	μA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
I_{INH} (Control Inputs)[6]	±10	±10	μA max	V_{IN} = V_{DD}
I_{INL} (Control Inputs)[6]	−150	−150	μA max	V_{IN} = 0 V
Input Capacitance[5]	16	16	pF max	
ANALOG OUTPUTS				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges	+5, +10	+5, +10	V	V_{SS} = 0 V. Pin Strappable
Output Voltage Ranges	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −15 V. Pin Strappable
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Full-Scale Change				V_{DD} = +15 V, V_{SS} = −15 V
J, K, A, B Versions	10	10	μs max	
S, T Versions	12	12	μs max	
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	
Digital Feedthrough[3]	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	nV secs typ	
POWER REQUIREMENTS				
V_{DD}	+15	+15	V nom	±5% for Specified Performance Unless Otherwise Stated
V_{SS}	−15	−15	V nom	±5% for Specified Performance Unless Otherwise Stated
I_{DD}	15	15	mA max	Output Unloaded. Typically 11 mA
I_{SS} (Dual Supplies)	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES

[1]Parts are functional at V_{DD} = +12 V ±10% and V_{SS} = 0 V or −12 V ±10%. See typical performance graphs.

[2]Temperature ranges are as follows: J, K Versions, −40°C to +85°C; A, B Versions, −40°C to +85°C; S, T Versions, −55°C to +125°C.

[3]See Terminology.

[4]Measured with respect to REF IN and includes unipolar/bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

[6]Control inputs are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$ for the AD7237 and $\overline{CSA}$, $\overline{CSB}$ and $\overline{WR}$ for the AD7247.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +15 V ±5%; V_{SS} = 0 V or −15 V ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247])

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	130	150	ns min	$\overline{WR}$ Pulse Width
t_4	128	150	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5[3]	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[4]	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[4]	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[4]	100	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 5 and 7.
[3]If 0 ns<t_2<10 ns, add t_2 to t_5. If t_2≥10 ns, add 10 ns to t_5.
[4]AD7237 only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247) . . . . . −0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237) . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND (AD7237) . . . . . −0.3 V , V_{DD} +0.3 V
V_{OUTA}[1], V_{OUTB}[1] to AGND (GND)
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
REF OUT to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND) . . . . . −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]Short-circuit current is typically 80mA. The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237JN	−40°C to +85°C	±1 max	N-24
AD7237KN	−40°C to +85°C	±1/2 max	N-24
AD7237JR	−40°C to +85°C	±1 max	R-24
AD7237KR	−40°C to +85°C	±1/2 max	R-24
AD7237AQ	−40°C to +85°C	±1 max	Q-24
AD7237BQ	−40°C to +85°C	±1/2 max	Q-24
AD7237SQ	−55°C to +125°C	±1 max	Q-24
AD7237TQ	−55°C to +125°C	±1/2 max	Q-24
AD7247JN	−40°C to +85°C	±1 max	N-24
AD7247KN	−40°C to +85°C	±1/2 max	N-24
AD7247JR	−40°C to +85°C	±1 max	R-24
AD7247KR	−40°C to +85°C	±1/2 max	R-24
AD7247AQ	−40°C to +85°C	±1 max	Q-24
AD7247BQ	−40°C to +85°C	±1/2 max	Q-24
AD7247SQ	−55°C to +125°C	±1 max	Q-24
AD7247TQ	−55°C to +125°C	±1/2 max	Q-24

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC).

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD7237 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

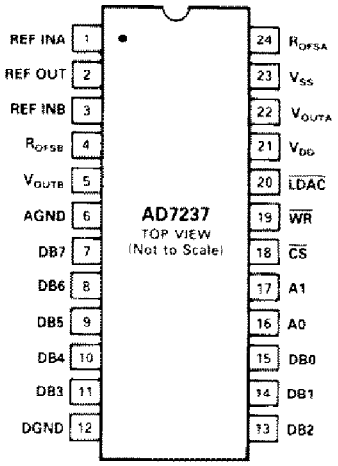
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8–10	DB6–DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply, +15 V.
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply, −15 V.
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7247 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to + 10 V and ± 5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9–DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply, +15 V.
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply, −15 V.
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247 is 5 V.

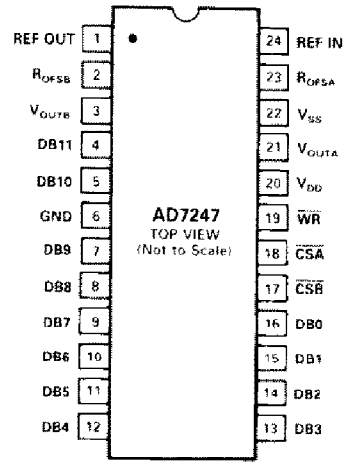
AD7237 PIN CONFIGURATIONS

DIP and SOIC



AD7247 PIN CONFIGURATIONS

DIP and SOIC



TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifiers of the AD7237/AD7247 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1. This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

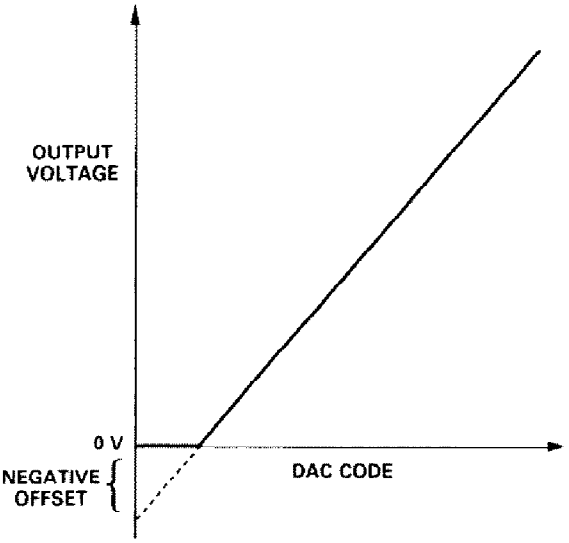


Figure 1. Effect of Negative Offset (Single Supply)

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7237/AD7247 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset, i.e., linearity is measured between Codes 3 and 4095.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the measured output voltage from V_{OUTA} or V_{OUTB} with all zeros loaded into the DAC latches when the DACs are configured for unipolar output. It is a combination of the offset errors of the DAC and output amplifier.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the voltage measured at V_{OUTA} or V_{OUTB} when the DAC is connected in the bipolar mode and loaded with code 2048. It is due to a combination of offset errors in the DAC, amplifier offset and mismatch in the application resistors around the amplifier.

FULL-SCALE ERROR

Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse injected for the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

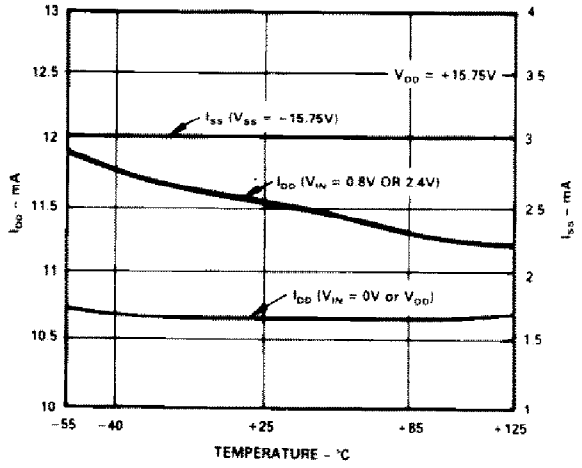
For the AD7237 it is measured with $\overline{LDAC}$ held high. For the AD7247 it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

DIGITAL CROSSTALK

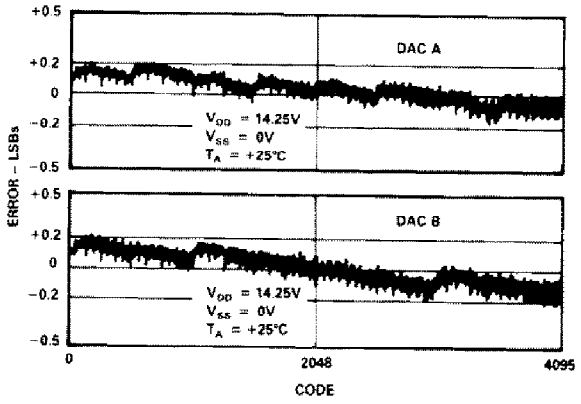
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code to the DAC latch of the other converter. It is specified in nV secs.

DIGITAL-TO-ANALOG GLITCH IMPULSE

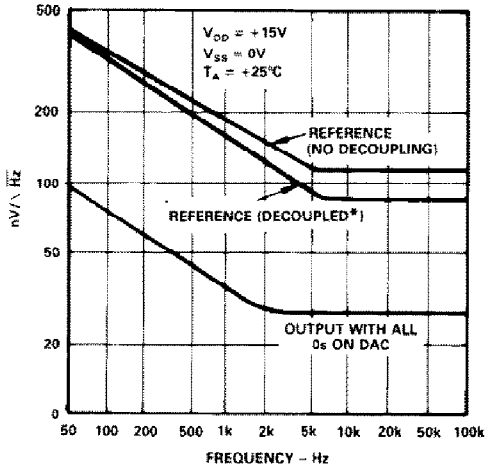
This is the voltage spike that appears at the output of the DAC when the digital code changes before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).



Power Supply Current vs.Temperature

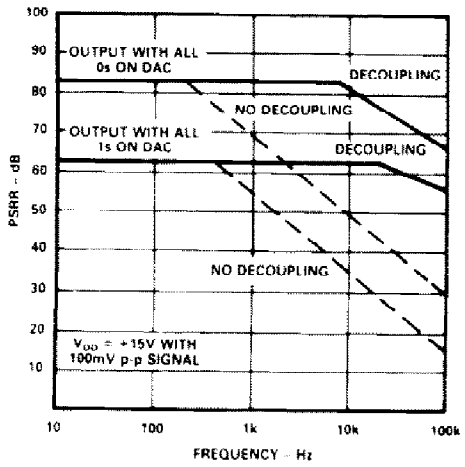


DAC-to-DAC Linearity Matching



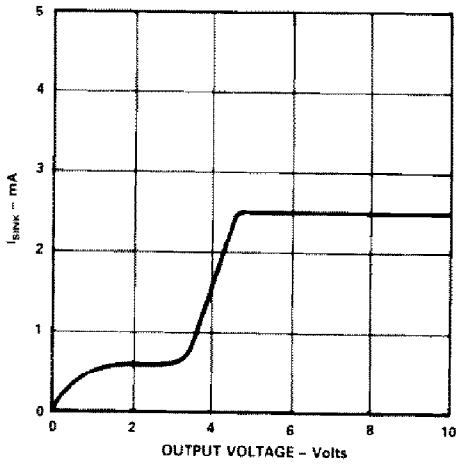
*REFERENCE DECOUPLING COMPONENTS ARE A 200Ω RESISTOR IN SERIES WITH A PARALLEL COMBINATION OF 10μF AND 0.1μF TO GND.

Noise Spectral Density vs. Frequency

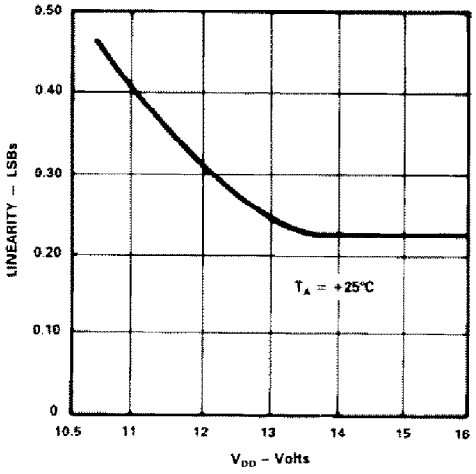


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF AND 0.1μF

Power Supply Rejection Ratio vs. Frequency



Single Supply Sink Current vs. Output Voltage



Linearity vs. Power Supply Voltage

CIRCUIT INFORMATION

D/A Section

The AD7237/AD7247 contains two 12-bit voltage-mode D/A converters consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The output voltage from the converters has the same polarity as the reference voltage, REF IN, allowing single supply operation. The simplified circuit diagram for one of the D/A converters is shown in Figure 2.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converters. The D/A converters are configured and scaled for a 5 V reference and the device is tested with 5 V applied to REF IN.

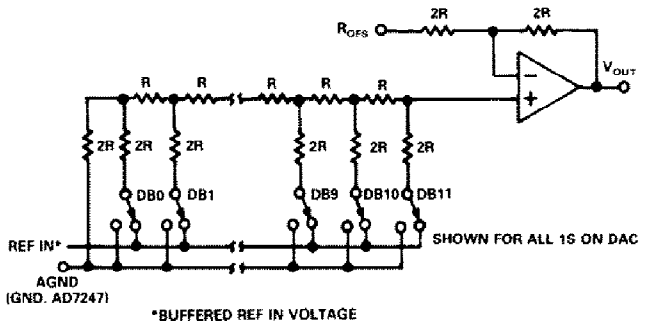


Figure 2. D/A Simplified Circuit Diagram

Internal Reference

The AD7237/AD7247 has an on-chip temperature compensated buried Zener reference (see Figure 3) which is factory trimmed to 5 V ±30 mV (±50 mV for S, T Versions). The reference voltage is provided at the REF OUT pin. This reference can be used to provide the reference voltage for the D/A converter (by connecting the REF OUT pin to the REF IN pin) and the offset voltage for bipolar outputs (by connecting REF OUT to R_{OFS}).

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND (GND) with a 200 Ω resistor in series with parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

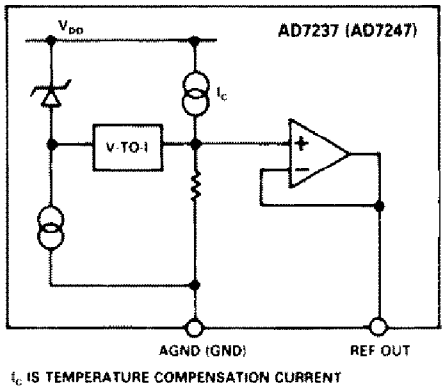


Figure 3. Internal Reference

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7237/AD7247 reference input. References such as the AD586 5 V reference provide the ideal external reference source for the AD7237/AD7247 (see Figure 9).

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows different output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to GND. The output amplifier can be operated from a single +15 V supply by tying V_{SS}=0 V. The amplifier can also be operated from dual supplies (±15 V) to allow a bipolar output range of −5 V to +5 V. The advantages of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0 V, full sink capability of 2.5 mA maintained over the entire output range and the elimination of the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the single supply output sink capability of the amplifier is shown in the Typical Performance Graphs section.

INTERFACE LOGIC INFORMATION - AD7247

Table I shows the truth table for AD7247 operation. The part contains a single, parallel 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. If $\overline{CSA}$ and $\overline{CSB}$ are both low, with $\overline{WR}$ low, the same data will be written to both DAC latches. All control signals are level triggered and therefore either or both latches can be made transparent. Input data is latched to the respective latch on the rising edge of $\overline{WR}$. Figure 4 shows the input control logic for the AD7247, while the write cycle timing diagram for the part is shown in Figure 5.

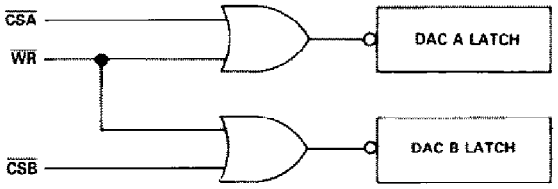


Figure 4. AD7247 Input Control Logic

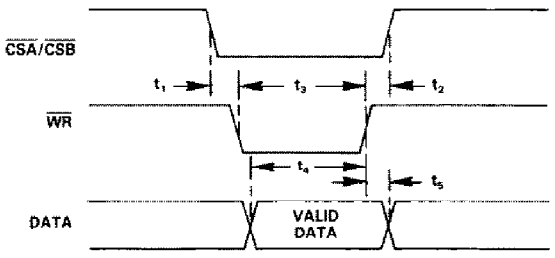


Figure 5. AD7247 Write Cycle Timing Diagram

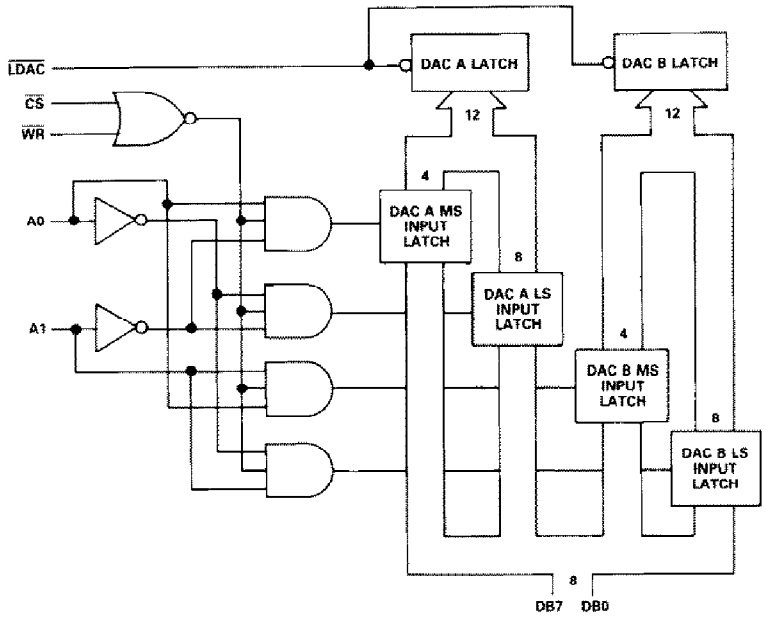


Figure 6. AD7237 Input Control Logic

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X = Don't Care

Table I. AD7247 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

Table II. AD7237 Truth Table

INTERFACE LOGIC INFORMATION – AD7237

The input loading structure on the AD7237 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC – an input latch and a DAC latch. Each input latch is further subdivided into a least significant 8-bit latch and a most significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7237 is shown in Figure 6, while the write cycle timing diagram is shown in Figure 7.

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The selection of the input latches is shown in the truth table for AD7237 operation in Table II.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. Both DAC latches, and hence both analog outputs, are updated at the same time. The $\overline{LDAC}$ signal is level triggered and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7237s.

However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

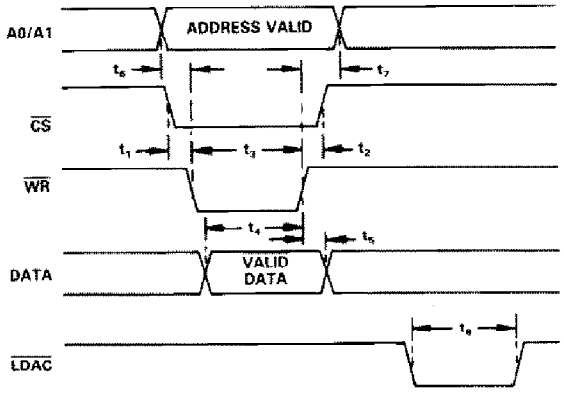


Figure 7. AD7237 Write Cycle Timing Diagram

APPLYING THE AD7237/AD7247

The internal scaling resistors provided on the AD7237/AD7247 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input the two DACs on each part can be set up for different output ranges.

Unipolar (0 V to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor, R_{OFSA}, or R_{OFSB}, to AGND (GND for AD7247). In this configuration, the AD7237/AD7247 can be operated from single or dual supplies. Figure 8 shows the connection diagram for unipolar operation for DAC A of the AD7237, while the table for output voltage versus digital code in the DAC latch is shown in Table III. Similar connections apply to the AD7247.

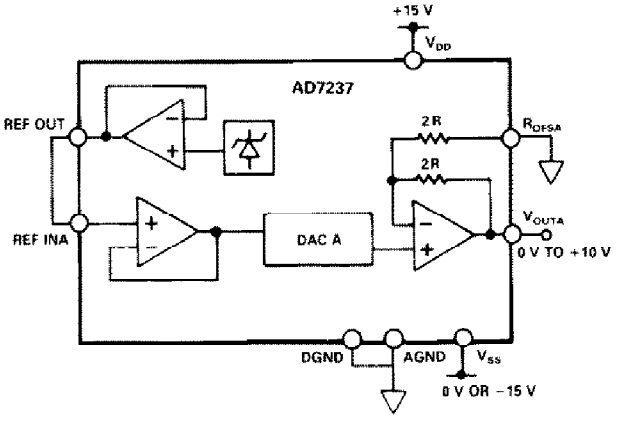


Figure 8. Unipolar (0 to +10 V) Configuration

Unipolar (0 V to +5 V) Configuration

The 0 V to +5 V output voltage range is achieved by tying R_{OFSA} or R_{OFSB} to V_{OUTA} or V_{OUTB}. Once again, the AD7237/AD7247 can be operated single supply or from dual supplies. The table for output voltage versus digital code is as in Table III, with 2 · REF IN replaced by REF IN. Note, for this range, 1 LSB = REF IN · (2^{-12}) = (REF IN/4096).

Bipolar Configuration

The bipolar configuration for the AD7237/AD7247, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFSA}, or R_{OFSB}, to REF IN. The AD7237/AD7247 must be operated from dual supplies to achieve this output voltage range. Figure 9 shows the connection diagram for bipolar operation for DAC A of the AD7247. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REF OUT to REF IN. The code table for bipolar operation is shown in Table IV. Similar connections apply for the AD7237.

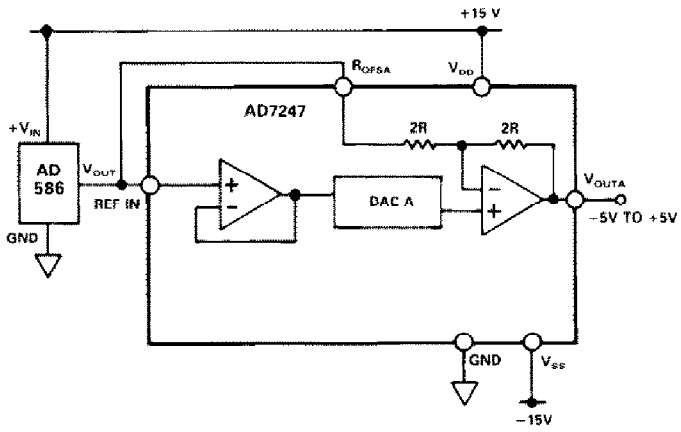


Figure 9. Bipolar Configuration

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+2 · REF IN · (4095/4096)
1000 0000 0001	+2 · REF IN · (2049/4096)
1000 0000 0000	+2 · REF IN · (2048/4096) = +REF IN
0111 1111 1111	+2 · REF IN · (2047/4096)
0000 0000 0001	+2 · REF IN · (1/4096)
0000 0000 0000	0 V

Note: 1 LSB = REF IN/2048.

Table III. Unipolar Code Table (0 to +10 V Range)

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+REF IN · (2047/2048)
1000 0000 0001	+REF IN · (1/2048)
1000 0000 0000	0 V
0111 1111 1111	−REF IN · (1/2048)
0000 0000 0001	−REF IN · (2047/2048)
0000 0000 0000	−REF IN · (2048/2048) = −REF IN

Note: 1 LSB = REF IN/2048.

Table IV. Bipolar Code Table

MICROPROCESSOR INTERFACING – AD7247

Figures 10 to 12 show interfaces between the AD7247 and the ADSP-2101 DSP processor and the 8086 and 68000 16-bit microprocessors. In all three interfaces, the AD7247 is memory-mapped with a separate memory address for each DAC.

AD7247 – ADSP-2101 Interface

Figure 10 shows an interface between the AD7247 and the ADSP-2101. The 12-bit word is written to the selected DAC latch of the AD7247 in a single instruction, and the analog output responds immediately. Depending on the clock frequency of the ADSP-2101, either one or two wait states will have to be programmed into the data memory wait state control register of the ADSP-2101.

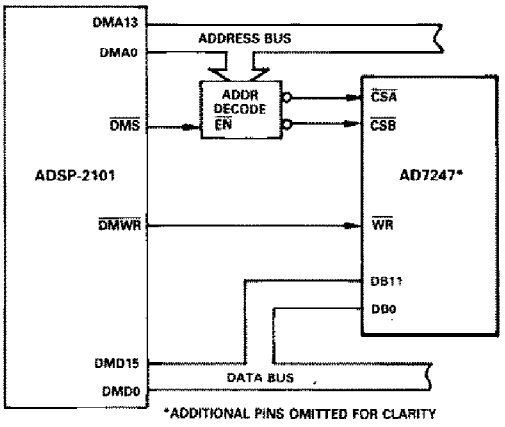


Figure 10. AD7247 to ADSP-2101 Interface

AD7247 – 8086 Interface

Figure 11 shows an interface between the AD7247 and the 8086 microprocessor. The 12-bit word is written to the selected DAC latch of the AD7247 in a single MOV instruction, and the analog output responds immediately.

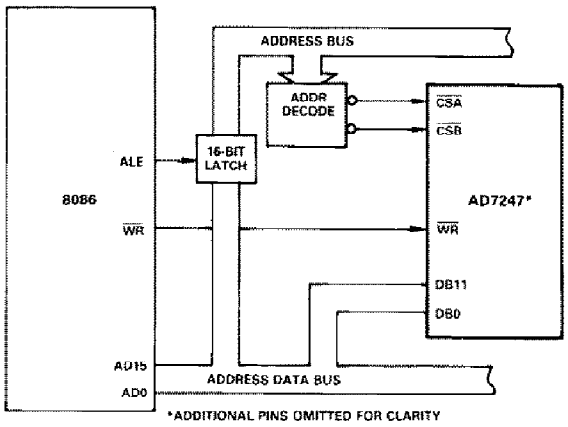


Figure 11. AD7247 to 8086 Interface

AD7247 – MC68000 Interface

Interfacing between the AD7247 and the MC68000 microprocessor is achieved using the circuit of Figure 12. Once again, the 12-bit word is written to the selected DAC latch of the AD7247 in a single MOVE instruction. $\overline{CSA}$ and $\overline{CSB}$ have to be AND-gated to provide a $\overline{DTACK}$ signal for the MC68000 when either DAC latch is selected.

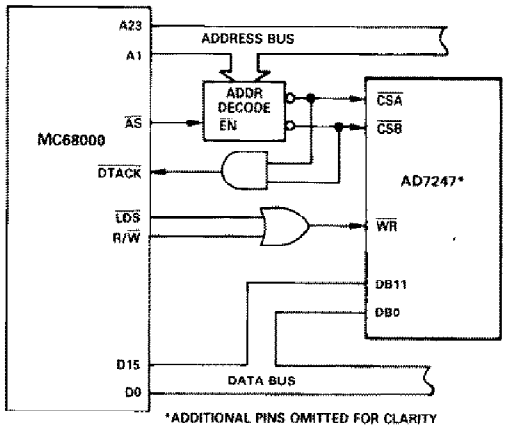


Figure 12. AD7247 to MC68000 Interface

MICROPROCESSOR INTERFACING – AD7237

Figures 13 to 15 show the AD7237 configured for interfacing to microprocessors with 8-bit databus systems. In all cases, data is right-justified, and the AD7237 is memory-mapped with the two lowest address lines of the microprocessor address bus driving the A0 and A1 inputs of the converter.

AD7237 – 8085A/8088 Interface

Figure 13 shows the connection diagram for interfacing the AD7237 to both the 8085A and the 8088. This scheme is also suited to the Z80 microprocessor, but the Z80 address/databus does not have to be demultiplexed. The AD7237 requires five separate memory addresses, one for the each MS latch and one for each LS latch and one for the common $\overline{LDAC}$ input. Data is written to the respective input latch in two write operations.

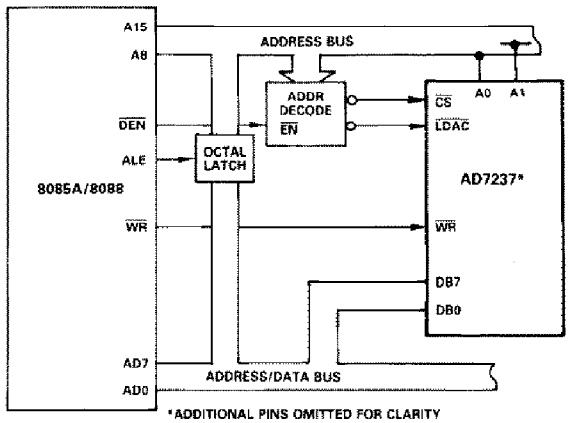


Figure 13. AD7237 to 8085A/8088 Interface

Either high byte or low byte data can be written first to the input latch. A write to the AD7237 DAC Latch address transfers the data from the input latches to the respective DAC latches and updates both analog outputs. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7237s for simultaneous updating of a number of voltage channels.

AD7237 – 68008 Interface

An interface between the AD7237 and the 68008 is shown in Figure 14. In the diagram shown, the $\overline{LDAC}$ is derived from an asynchronous $\overline{LDAC}$ signal, but this can be derived from the address decoder as in the previous interface diagram.

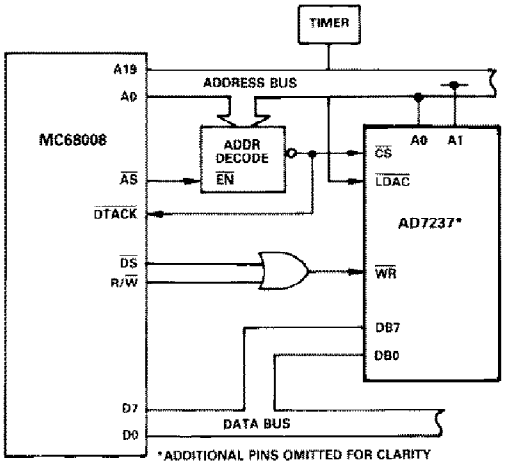


Figure 14. AD7237 to 68008 Interface

AD7237 – 6502/6809 Interface

Figure 15 shows an interface between the AD7237 and the 6502 or 6809 microprocessor. The procedure for writing data to the AD7237 is as outlined for the 8085A/8088 interface. For the 6502 microprocessor, the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

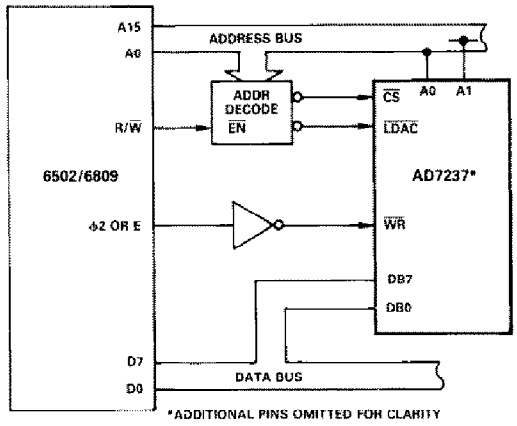
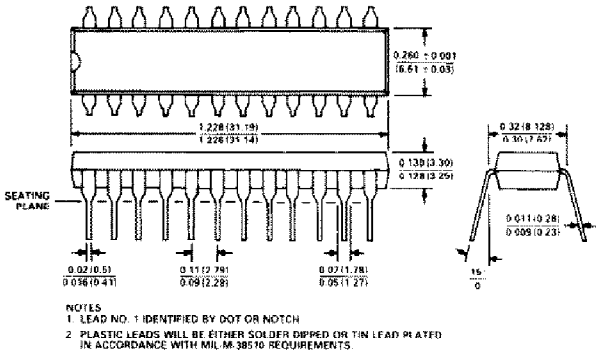


Figure 15. AD7237 to 6502/6809 Interface

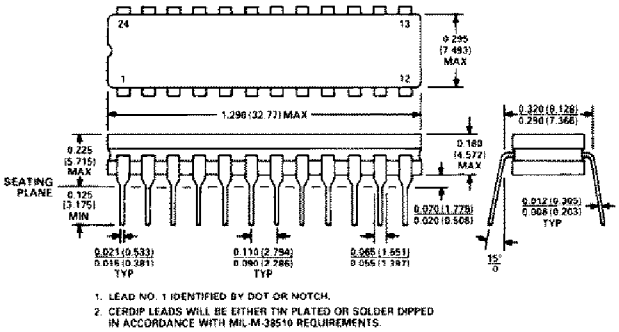
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

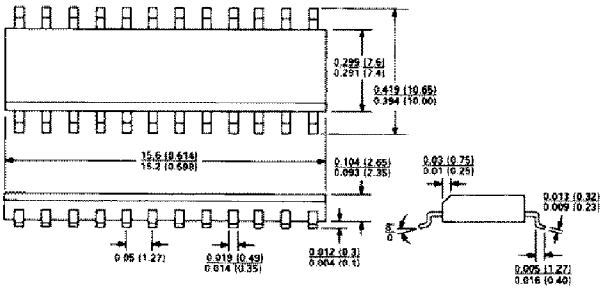
Plastic DIP (N-24)



Cerdip (Q-24)



SOIC (R-24)

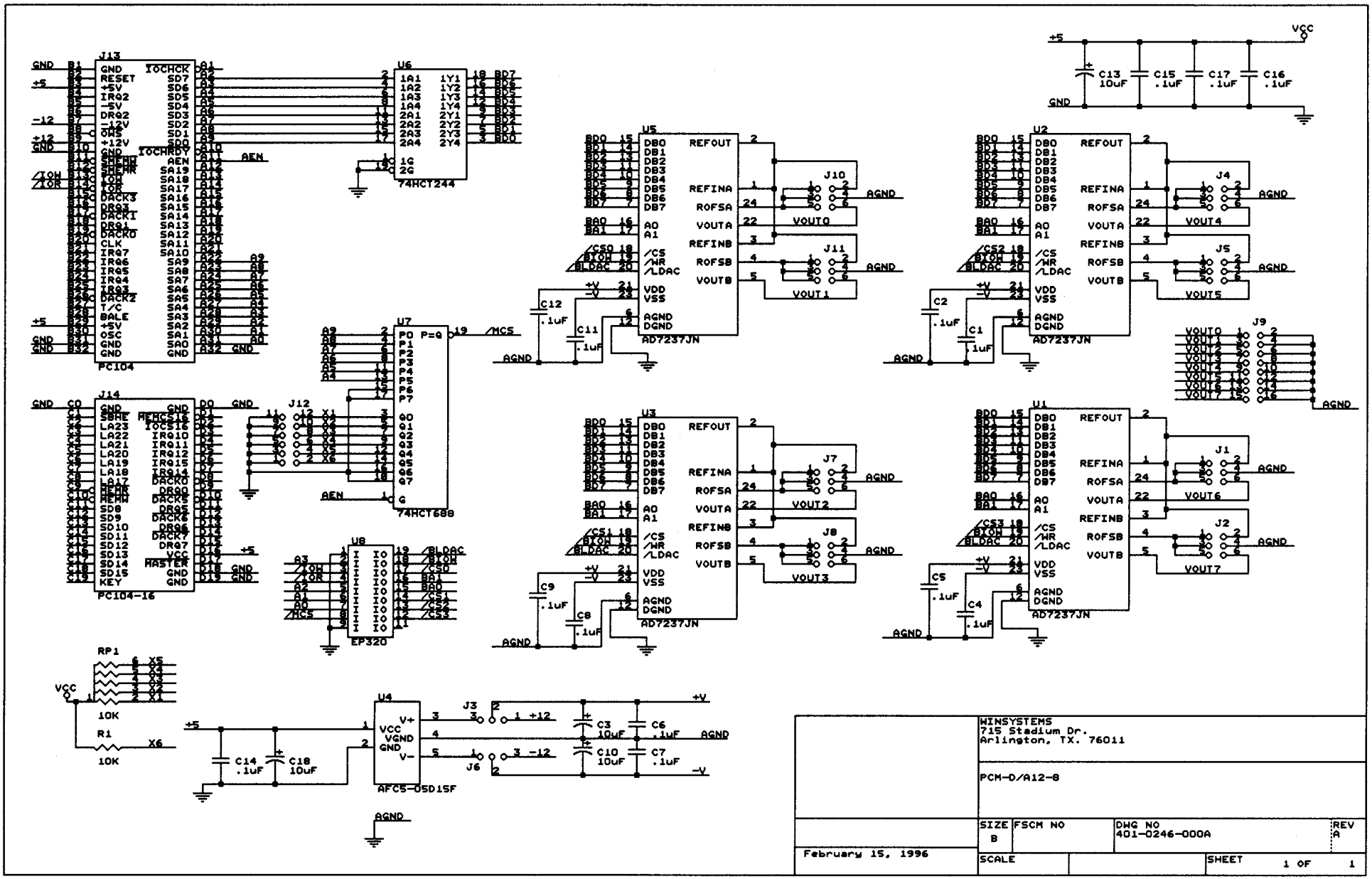


C1324a–10–8/91

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7 APPENDIX D

PCM-D/A12 Schematic Diagram


J13
PC104
U6
74HCT244
U5
AD7237JN
U2
AD7237JN
U7
74HCT688
J14
PC104-16
J12
U8
EP320
U3
AD7237JN
U1
AD7237JN
RP1
10K
R1
10K
U4
AFC5-05D15F
C13 10uF
C15 .1uF
C17 .1uF
C16 .1uF
C12 .1uF
C11 .1uF
C2 .1uF
C1 .1uF
C9 .1uF
C8 .1uF
C5 .1uF
C4 .1uF
C14 .1uF
C18 10uF
C3 10uF
C6 .1uF
C10 10uF
C7 .1uF
J10
J11
J4
J5
J9
J7
J8
J1
J2
J3
J6
VOUT0
VOUT1
VOUT2
VOUT3
VOUT4
VOUT5
VOUT6
VOUT7
AGND
GND
VCC
+5
-12
+12
/MCS
AEN
WINSYSTEMS
715 Stadium Dr.
Arlington, TX. 76011
PCM-D/A12-8
SIZE B
FSCM NO
DWG NO 401-0246-000A
REV A
February 15, 1996
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SHEET 1 OF 1

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