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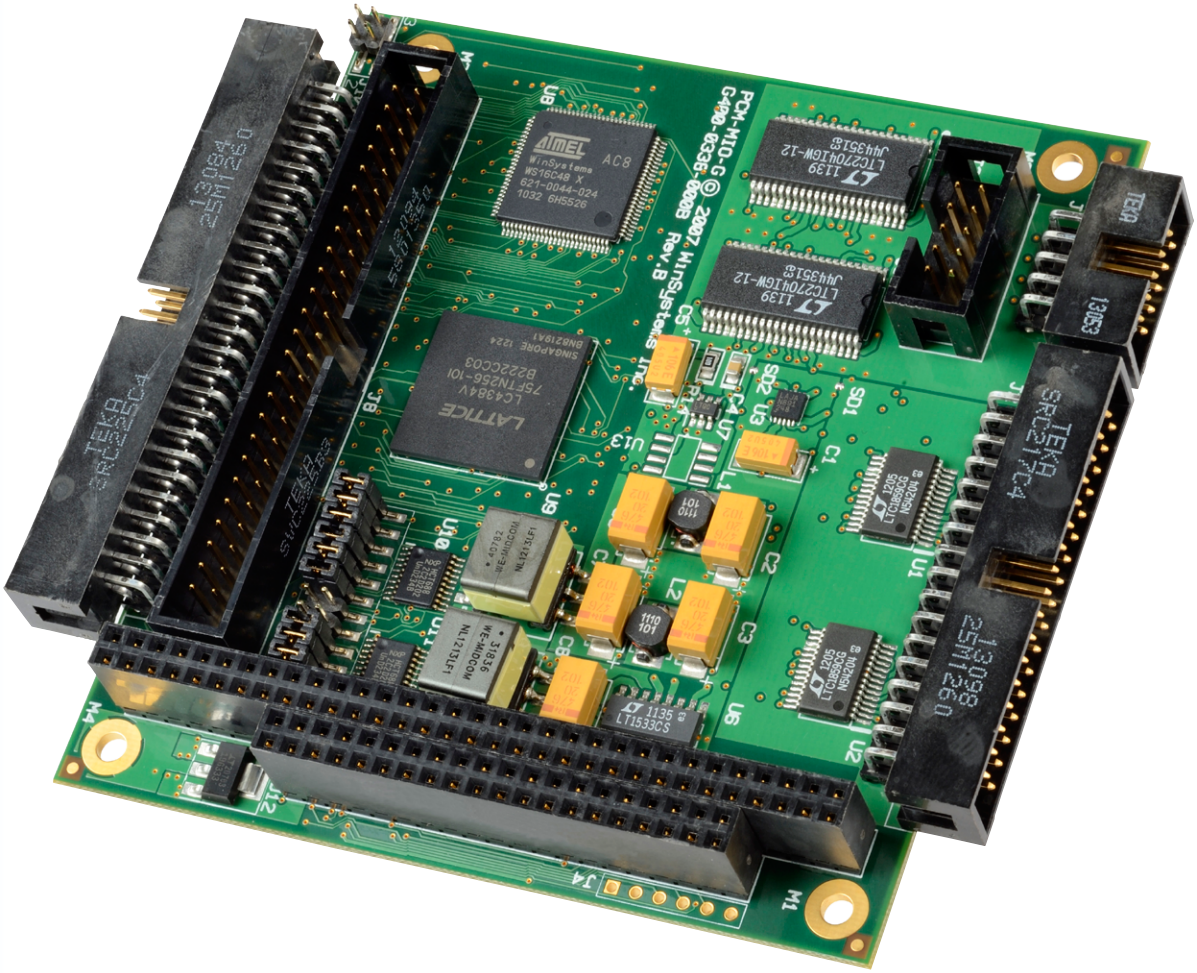
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Find the *WinSystems PCM-MIO-G-1* at our website: *Click HERE*

PCM-MIO-G-1

16 Channel, 16-bit Analog Inputs
8 Channel, 12-bit Analog Outputs, and
48 Digital I/O

PRODUCT MANUAL



WinSystems, Inc.
715 Stadium Drive
Arlington, TX 76011

http://www.winsystems.com

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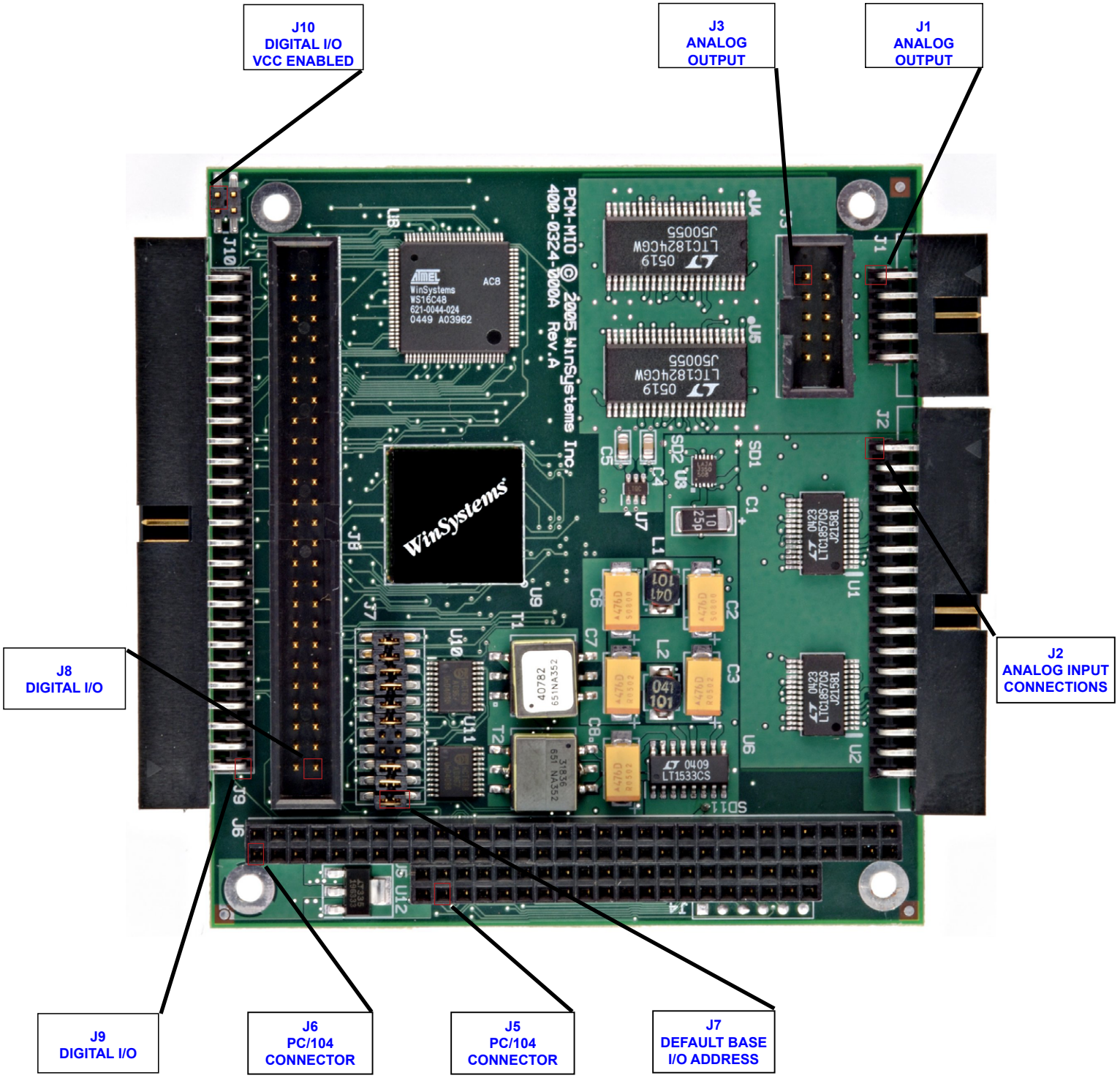
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Visual Index - Top View (Connectors)



NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

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JUMPER REFERENCE

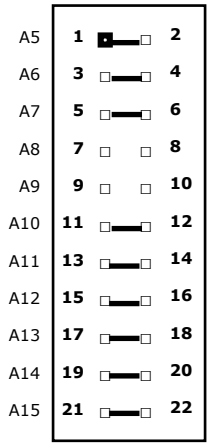
NOTE: Jumper Part numbers W/S# G201-0002-005 and SAMTEC 2SN-BK-G are applicable to all jumpers. These are available in a five piece kit from WinSystems (Part# KIT-JMP-G-200).

BASE I/O SELECTION

J7 - Base I/O Address

Visual Index

J7



Example - 300HEX Default

0	0	0	0	0	0	1	1	0	0	0	X	X	X	X	X
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Jumper OPEN = 1

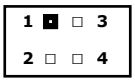
Jumper INSTALLED = 0

DIGITAL I/O

J10 - VCC Enable

Visual Index

J10



+5V is provided at pin 49 of **J9**	3-4
+5V is provided at pin 49 of **J8**	1-2
No Power at Pin 49 of **J8/J9** (default)	OPEN

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INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the PCM-MIO digital I/O module. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

GENERAL INFORMATION

The PCM-MIO is a versatile, PC/104 analog input, analog output, and digital I/O board designed for high accuracy and high channel count analog and digital I/O. The board is based upon Linear Technologies' state of the art precision converters and voltage references which require no external callibration.

FEATURES

Analog Input

- Two 8-channel, 16-bit Analog-to-Digital (A/D) (LTC-1859CG) with sample-and-hold-circuit support
- Conversion Rate: 100 ksps max
- Any combination of up to 16 single-ended input channels and up to 8 differential input channels
- Each channel independently programmable for input type and range
- Input ranges: 0-5V, 0-10V, ±5V or ±10V
- Input Protection: ±25V
- Supports industry standard signal conditioners
- Programmable interrupt and DMA support

Analog Output

- Two 4-channel, 12-bit Digital-to-Analog (D/A) (LTC-2704CGW-12)
- Output ranges: 0-5V, 0-10V, ±5V or ±10V, +/-2.5V, -2.5V to 7.5V
- Each channel independently programmable for output type and range
- Output channels can be updated and cleared individually or simultaneously
- Interrupt I/O supported
- Supports industry standard signal conditioners

Digital I/O

- 48 bidirectional lines with Input, Output, or Output with Readback (WS16C48)
- 12 mA sink current per line
- Ability to generate an interrupt on signal change-of state (24 bits)
- Write-protection mask register for each port
- Programmable Edge Polarity

Power

- +5V required, 490mA typical

Operating Temperature

- -40°C to 85°C

Form Factor

- 3.6 x 3.8 inches (90 x 96 mm)

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FUNCTIONALITY

Base I/O Address

The PCM-MIO is I/O mapped and requires 32 sequential port addresses. The base address is jumper selectable at **J7**. Care should be taken to choose an I/O area that does not conflict with other resources in the system. The specific device locations and register offsets are discussed in more detail in the Software Summary section.

INTERRUPTS

The PCM-MIO provides flexible interrupt configuration options. Each D/A converter and 24 Digital I/O lines are capable of generating an interrupt. They can be setup to use individual interrupts, a single shared interrupt, or any combination of the two. The interrupts are completely software configurable and require no jumpers or other configuration. The individual registers and configuration for each device are discussed in the Software Summary section under each device.

The PCM-MIO can be configured to use IRQ's 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 depending on availability in the system. IRQ's 0, 1, 2, 8, and 13 are not supported.

DMA SUPPORT

The PCM-MIO supports DMA on the A/D and D/A device. Commands can be configured on DMA channels 0, 1, 2, and 3, which are 8-bit channels. Data can be configured on DMA channels 5, 6, and 7, which are 16-bit channels. DMA Channel 4 is not available.

Analog-To-Digital

The PCM-MIO analog-to-digital conversion inputs are implemented by using two, 16-bit Linear Technologies LTC-1859CG devices. The board supports up to 16 single-ended input channels, 8 differential input channels or various combinations of both. The channel configuration word selects whether an input will operate in single-ended or differential mode and also selects the desired input range (0V to 5V, 0V to 10V, ±5V and ±10V).

The LTC-1859CG uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog input signal to 16-bit digital data. The output is two's complement binary for bipolar mode and offset binary for unipolar mode.

Digital-to-Analog

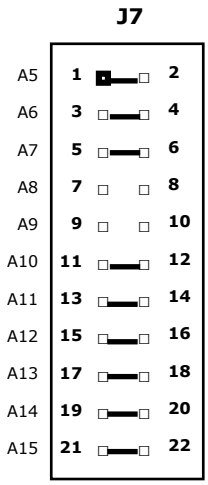
The PCM-MIO provides digital-to-analog conversion using two 12-bit Linear Technologies LTC-2704 devices. These SoftSpan™ quad Digital-to-Analog converters (DACs) are software programmable for either unipolar or bipolar mode with specific voltage ranges on a per channel basis. Each of the 8 channels can be programmed to any one of the output ranges (0V to 5V, 0V to 10V, ±2.5V,±5V, ±10V and -2.5V to 7.5V).

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I/O ADDRESS

J7 - Base I/O Address

Visual Index



Example - 300HEX Default

0	0	0	0	0	0	1	1	0	0	0	X	X	X	X	X
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Jumper OPEN = 1

Jumper INSTALLED = 0

The PCM-MIO is I/O mapped and requires 32 sequential port addresses. The base address is jumper selectable at **J7**. Care should be taken to choose an I/O area that does not conflict with other resources in the system. The specific device locations and register offsets are discussed in more detail in the Software Summary section.

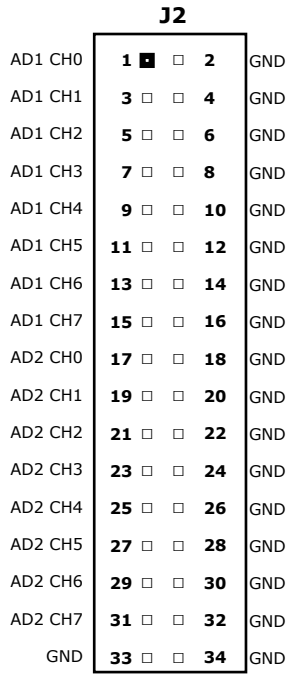
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ANALOG INPUT (ADC)

J2 - ADC Analog Input Connections

Visual Index

PCB Connector: G650-2034-1HA, TEKA SRC217C425M126-0
Mating Connector: ITW-PANCON 050-034-455A



NOTE: In differential input mode, only the even channel numbers (0, 2, 4, ...) are used and the signal is applied between the even channel number and the next odd channel input pin.

The PCM-MIO analog-to-digital conversion inputs are implemented by using two, 16-bit Linear Technologies LTC-1859CG devices. The board supports up to 16 single-ended input channels, 8 differential input channels or various combinations of both. The channel configuration word selects whether an input will operate in single-ended or differential mode and also selects the desired input range (0V to 5V, 0V to 10V, ±5V and ±10V).

The LTC-1859CG uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog input signal to 16-bit digital data. The output is two's complement binary for bipolar mode and offset binary for unipolar mode.

Programming information for the A/D controller is provided in the Software Summary section of this manual.

The analog input channels are terminated at **J2**. The pin definitions are shown in the illustration above.

NOTE: When the board is powered off, the A/D input has a 20K input impedance and is protected to ±20V. When the board is powered on, the A/D differential channel input has a 31K input impedance and the single-ended channel input has a 42K input impedance. Power on inputs are protected to ±25V.

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ANALOG OUTPUT (DAC)

J1, J3 - D/A Analog Output Connections

Visual Index

PCB Connector: TEKA SRC205C425M126-0 (J1), TEKA SVC205B3580135-0 (J3)
Mating Connector: ITW-PANCON 050-010-455A



The PCM-MIO provides digital-to-analog conversion output using two of the 12-bit Linear Technologies LTC-2704 devices. These SoftSpan™ quad Digital-to-Analog converters (DACs) are software programmable for either unipolar or bipolar mode with specific voltage ranges on a per channel basis. Each of the 8 channels can be programmed to any one of the six output ranges (0V to 5V, 0V to 10V, ±2.5V,±5V, ±10V and -2.5V to 7.5V).

Programming information for the D/A controller is provided in the Software Summary section of this manual.

The Analog Output channels are terminated at **J1** and **J3**. The pin definitions are shown in the illustration above.

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DIGITAL I/O INTERFACE

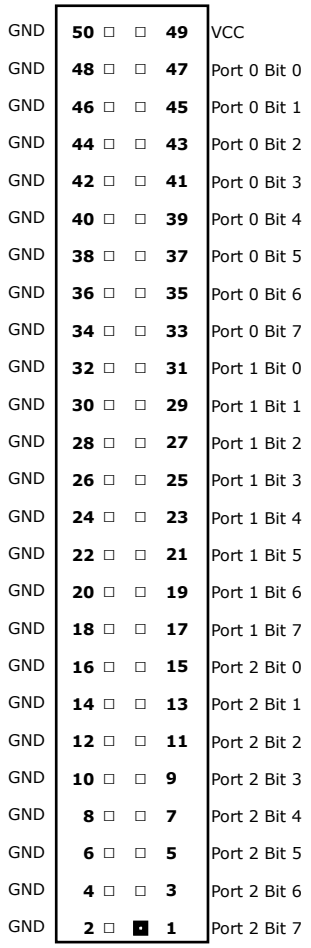
J8, J9 - Digital I/O

Visual Index

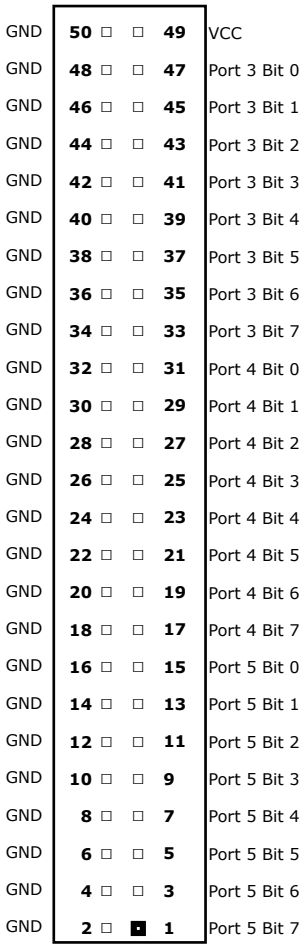
PCB Connector: TEKA SVC225B3580135-0 (J8), TEKA SRC225C425M126-0 (J9)

Mating Connector: ITW-PANCON 050-050-455A

J9



J8



Parallel I/O

The PCM-MIO utilizes the WinSystems WS16C48 ASIC high-density I/O chip. The 48 lines are each individually programmable as input or output and the first 24 lines are capable of fully latched event sensing with edge polarity being software programmable.

Digital I/O Connectors

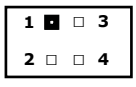
The 48 lines of parallel I/O are terminated through two 50-pin connectors at **J8** and **J9**. The **J9** connector handles I/O ports 0-2 while **J8** handles ports 3-5. The pin definitions for **J8** and **J9** are shown above.

J10 - VCC Enable

Visual Index

The digital I/O connector can provide +5V to an I/O rack, when required. +5V is provided at pin 49 on connector **J9** when **J10** is jumpered, pin 3-4. +5V is provided at pin 49 of **J8** when **J10** is jumpered, pin 1-2. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the board.

J10



+5V is provided at pin 49 of **J9**	3-4
+5V is provided at pin 49 of **J8**	1-2
No Power at Pin 49 of **J8/J9** (default)	OPEN

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PC/104 BUS INTERFACE

J5, J6 - PC/104

Visual Index

PCB Connector: **TEKA PC232-A-W1A7-M (J6)**
TEKA PC220-A-W1A7-M (J5)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PCM-MIO's connectors, located at **J5** and **J6**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided here for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J5

GND	**D0**	**C0**	GND
MEMCS16#	**D1**	**C1**	SBHE#
IOCS16#	**D2**	**C2**	LA23
IRQ10	**D3**	**C3**	LA22
IRQ11	**D4**	**C4**	LA21
IRQ12	**D5**	**C5**	LA20
IRQ15	**D6**	**C6**	LA19
IRQ14	**D7**	**C7**	LA18
DACK0#	**D8**	**C8**	LA17
DRQ0	**D9**	**C9**	MEMR#
DACK5#	**D10**	**C10**	MEMW#
DRQ5	**D11**	**C11**	SD8
DACK6#	**D12**	**C12**	SB9
DRQ6	**D13**	**C13**	SD10
DACK7#	**D14**	**C14**	SD11
DRQ7	**D15**	**C15**	SD12
+5V	**D16**	**C16**	SD13
MASTER#	**D17**	**C17**	SD14
GND	**D18**	**C18**	SD15
GND	**D19**	**C19**	KEY

J6

IOCHK#	**A1**	**B1**	GND
SD7	**A2**	**B2**	RESET
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	SRDY#
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	KEY
AEN	**A11**	**B11**	SMEMW#
SA19	**A12**	**B12**	SMEMR#
SA18	**A13**	**B13**	IOW#
SA17	**A14**	**B14**	IOR#
SA16	**A15**	**B15**	DACK3#
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1#
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	REFRESH#
SA11	**A20**	**B20**	BCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2#
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	GND
GND	**A32**	**B32**	GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

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SOFTWARE SUMMARY

A/D Converters

The PCM-MIO uses two Linear Tech LTC-1859CG 8-channel A/D converters. Each device is independently software configurable to support the listed input modes and ranges. The devices use a full-duplex serial interface which transmits and receives data simultaneously. An 8-bit command is shifted into the ADC interface to configure it for the next conversion. At the same time, the data from the previous conversion is shifted out of device. Consequently, the conversion result is delayed by one conversion from the command word.

A/D1 - Starting at BASE +0

The COMMAND register, RESOURCE register and RESOURCE ENABLE registers are used to configure the A/D device operation. The specific options of each register are detailed here.

Register	Address (Base+)	Read/Write	7	6	5	4	3	2	1	0
DATA_LO	0	R	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
DATA_HI	1	R	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
COMMAND (1)	2	R/W	COMMAND							
			CMD-BIT 7	CMD-BIT 6	CMD-BIT 5	CMD-BIT 4	CMD-BIT 3	CMD-BIT 2	CMD-BIT 1	CMD-BIT 0
RESOURCE (2)	2	R/W	DMA CHANNEL ASSIGNMENT				INTERRUPT ROUTING ASSIGNMENT IRQ[15-3] 0, 1, 2, 8 AND 13 NOT AVAILABLE			
			DATA REGISTER BIT 1	DATA REGISTER BIT 0	DATA REGISTER BIT 1	DATA REGISTER BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
RESOURCE ENABLE	3	W	X	X	X	REGISTER SELECT		DATA DRQ ENABLE (3)	CMD DRQ ENABLE (3)	INTERRUPT ENABLE (3)
						BIT 1	BIT 0			
STATUS	3	R	DATA READY	DATA DMA REQUEST PENDING (3)	CMD DMA REQUEST PENDING (3)	INTERRUPT REQUEST PENDING (3)	REGISTER SELECT STATUS	DATA DRQ ENABLE STATUS (3)	CMD DRQ ENABLE STATUS (3)	INTERRUPT EANBLE BIT STATUS (3)

Notes: **(1) Accessed when REGISTER SELECT (BASE +3 bit 4 & 3) = 00**
(2) Accessed when REGISTER SELECT (BASE +3 bit 4 & 3) = 01
(3) 0=Disabled, 1=Enable

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A/D2 - Starting at BASE +4

The interface for the second A/D device is almost identical to the first device. Notice in this table that the REGISTER SELECT function within the RESOURCE ENABLE register is only a single bit. In both software examples shown below, action 1 (one) should be replaced with:

1. Write **xxxx1xxx** to bit 3 of BASE +7 (select access to Resources).

Since bit 4 is a don't care in this case, it is possible to use identical code for both devices just noting the different base address.

Register	Address (Base+)	Read/Write	7	6	5	4	3	2	1	0
DATA_LO	4	R	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
DATA_HI	5	R	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
COMMAND (1)	6	R/W	COMMAND							
			CMD-BIT 7	CMD-BIT 6	CMD-BIT 5	CMD-BIT 4	CMD-BIT 3	CMD-BIT 2	CMD-BIT 1	CMD-BIT 0
RESOURCE (2)	6	R/W	DMA CHANNEL ASSIGNMENT				INTERRUPT ROUTING ASSIGNMENT IRQ[15-3] 0, 1, 2, 8 AND 13 NOT AVAILABLE			
			DATA REGISTER BIT 1	DATA REGISTER BIT 0	CMD REGISTER BIT 1	CMD REGISTER BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
RESOURCE ENABLE	7	W	X	X	X	X	REGISTER SELECT	DATA DRQ ENABLE (3)	CMD DRQ ENABLE (3)	INTERRUPT ENABLE (3)
STATUS	7	R	DATA READY	DATA DMA REQUEST PENDING (3)	CMD DMA REQUEST PENDING (3)	INTERRUPT REQUEST PENDING (3)	REGISTER SELECT STATUS	DATA DRQ ENABLE STATUS (3)	CMD DRQ ENABLE STATUS (3)	INTERRUPT EANBLE BIT STATUS (3)

Notes: **(1) Accessed when REGISTER SELECT (BASE +7 bit 3) = 0**
(2) Accessed when REGISTER SELECT (BASE +7 bit 3) = 1
(3) 0=Disabled, 1=Enable

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Command Register

Each A/D device contains an 8-bit command register to configure the inputs to single-ended or differential mode and the desired input range (0V - 5V, 0V - 10V, ±5V, and ±10V). The following describes the register options.

				INPUT RANGE			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SGL / DIFF	ODD SIGN	SELECT 1	SELECT 0	UNI	GAIN	NAP	SLEEP
MUX CHANNEL SELECTION						**NOT SUPPORTED**	

Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	6	7	SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	6	7	COM
		1	0											1	0									
0	0	0	0	+	-							1	0	0	0	+								-
0	0	0	1			+	-					1	0	0	1			+						-
0	0	1	0					+	-			1	0	1	0					+				-
0	0	1	1							+	-	1	0	1	0							+		-
0	1	0	0	-	+							1	1	0	0		+							-
0	1	0	1			-	+					1	1	0	1				+					-
0	1	1	0					-	+			1	1	1	0						+			-
0	1	1	1							-	+	1	1	1	1								+	-

Channel Selection

Bits 7 - 4 of the command register assign the channel configuration for the requested conversion. The converter will measure the voltage between the two channels indicated by the + and - signs in the table below. In differential mode measurements are from any of the four adjacent input pairs in either polarity. In single-ended mode, all input channels are measured with respect to GND. Both the + and - inputs are sampled simultaneously so commode mode noise in rejected.

Range Selection

Bits 3 and 2 of the command register determine the input range for the conversion. Setting UNI to a logical one selects a unipolar conversion while a zero selects bipolar. The GAIN bit selects the input span for the conversion in conjuntion with the UNI bit. The table below defined the selection options.

Input Range Selection

3	2	
UNI	GAIN	INPUT RANGE
0	0	±5V
1	0	0V to 5V
0	1	±10V
1	1	0V to 10V

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Examples of Multiplexer Options

CHANNEL	
0,1	+(-) -(+)
2,3	+(-) -(+)
4,5	+(-) -(+)
6,7	+(-) -(+)

4 Differential

CHANNEL	
0	+
1	+
2	+
3	+
4	+
5	+
6	+
7	+
	COM(-)

8 Single-Ended

CHANNEL	
0,1	+ -
2,3	- +
4	+
5	+
6	+
7	+
	COM(-)

Combinations of Differential and Single-Ended

CHANNEL	
....	....
4,5	+ -
6,7	+ -
	COM(-) (UNUSED)

1st Conversion

CHANNEL	
....	....
4,5	- +
	+
6	+ -
7	COM(-)

2nd Conversion

Changing the MUX Assignment On The Fly

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Example 1 - ADC1

The following is a polled mode example for A/D1.

1. Write **xxx00xxx** to bits 3 & 4 of BASE +3.	Select access to CMD
2. Write **CMD** selection to BASE +2.	Set MUX channel operation & range
3. Read data from BASE +0 and discard.	Lo_Byte unknown data
4. Read data from BASE +1 and discard.	Hi_Byte unknown data
5. Write **CMD** selection to BASE +2 again.	Set MUX channel operation & range
6. Read data from BASE +0.	Lo_Byte
7. Read data from BASE +1.*	Hi_Byte
*The data received is actually the result of the first CMD written. Realize that all readings will be offset by one action due to the latching of the serial input mechanism.	
8. Additional readings are achieved by repeating steps 5 through 7.	

Example 2 - ADC2

The following is a polled mode example for A/D2, note the difference in starting address and resource enable.

1. Write **xxxx0xxx** to bit 3 of BASE +7.	Select access to CMD
2. Write **CMD** selection to BASE +6.	Set MUX channel operation & range
3. Read data from BASE +4 and discard.	Lo_Byte unknown data
4. Read data from BASE +5 and discard.	Hi_Byte unknown data
5. Write **CMD** selection to BASE +6 again.	Set MUX channel operation & range
6. Read data from BASE +4.	Lo_Byte
7. Read data from BASE +5.*	Hi_Byte
*The data received is actually the result of the first CMD written. Realize that all readings will be offset by one action due to the latching of the serial input mechanism.	
8. Additional readings are achieved by repeating steps 5 through 7.	

Please read the documentation included with the sample programs and drivers for more complex examples.

A/D Interrupts

To operate using interrupt mode, IRQ routing must be configured and interrupts enabled for each device. This is achieved with the Resource and Resource Enable registers. The following would apply to A/D1:

1. Write **xxx01xxx** to bits 4 & 3 of BASE +3 (select access to Resource Register).
2. Write IRQ selection (0-15 hex) to bits 3-0 of BASE +2 (**xF Hex =** IRQ 15).
3. Write **xxxxxx1** BASE +3 to enable the IRQ.

Enabling an interrupt for A/D2 can be achieved in the same manner with the appropriate offset.

It is possible for both devices to share an interupt or use individual interrupts. When sharing interrupts, the most efficient method to determine which device generated an interrupt request is to utilize the Master Interrupt Status Register.

DMA Support

DMA operation is available for this device. A sample of these operations under DOS is provided on website. These operations under other operating systems can be quite complex and are beyond the scope of this manual.

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D/A Converters

The PCM-MIO contains two Linear Tech LTC-2704 Digital-to-Analog Converter (DAC) devices. Each device is a 4-channel converter with software selectable output span.

D/A1 - Starting at BASE +8

The COMMAND register, RESOURCE register and RESOURCE ENABLE registers are used to configure the D/A device operation. The specific options of each register are detailed here.

Register	Address (Base+)	Read/Write	7	6	5	4	3	2	1	0
DATA_LO	8	R/W	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
READBACK (1)	8	R	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
DATA_HI	9	R/W	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
READBACK (1)	9	R	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
COMMAND (2)	10	R/W	COMMAND							
			CMD-BIT 7	CMD-BIT 6	CMD-BIT 5	CMD-BIT 4	CMD-BIT 3	CMD-BIT 2	CMD-BIT 1	CMD-BIT 0
RESOURCE (3)	10	R/W	DMA CHANNEL ASSIGNMENT				INTERRUPT ROUTING ASSIGNMENT IRQ[15-3] 0, 1, 2, 8 AND 13 NOT AVAILABLE			
			DATA REGISTER BIT 1	DATA REGISTER BIT 0	DATA REGISTER BIT 1	DATA REGISTER BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
RESOURCE ENABLE	11	W	X	X	X	READBACK ENABLE	REGISTER SELECT	DATA DRQ ENABLE (4)	CMD DRQ ENABLE (4)	INTERRUPT ENABLE (4)
STATUS	11	R	DATA READY	DATA DMA REQUEST PENDING (4)	CMD DMA REQUEST PENDING (4)	INTERRUPT REQUEST PENDING (4)	REGISTER SELECT STATUS	DATA DRQ ENABLE STATUS (4)	CMD DRQ ENABLE STATUS (4)	INTERRUPT EANBLE BIT STATUS (4)

Notes: **(1) Accessed when READBACK ENABLE (BASE +11 bit 4) = 1**

(2) Accessed when REGISTER SELECT (BASE +11 bit 3) = 0

(3) Accessed when REGISTER SELECT (BASE +11 bit 3) = 1

(4) 0=Disabled, 1=Enable

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D/A2 - Starting at BASE +12

As shown in the table below, interface to the 2nd device is almost identical to the first with a change in the base address. The RESOURCE ENABLE register does contain an additional register select bit, MASTER IRQ / DA2 SELECT. If this bit is set to 1, reading BASE +15 will result in the status of the Master Interrupt Status Register.

Register	Address (Base+)	Read/Write	7	6	5	4	3	2	1	0
DATA_LO	12	R/W	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
READBACK (1)	12	R	LOW ORDER DATA BYTE							
			DATA-BIT 7	DATA-BIT 6	DATA-BIT 5	DATA-BIT 4	DATA-BIT 3	DATA-BIT 2	DATA-BIT 1	DATA-BIT 0
DATA_HI	13	R/W	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
READBACK (1)	13	R	HIGH ORDER DATA BYTE							
			DATA-BIT 15	DATA-BIT 14	DATA-BIT 13	DATA-BIT 12	DATA-BIT 11	DATA-BIT 10	DATA-BIT 9	DATA-BIT 8
COMMAND (2)	14	R/W	COMMAND							
			CMD-BIT 7	CMD-BIT 6	CMD-BIT 5	CMD-BIT 4	CMD-BIT 3	CMD-BIT 2	CMD-BIT 1	CMD-BIT 0
RESOURCE (3)	14	R/W	DMA CHANNEL ASSIGNMENT				INTERRUPT ROUTING ASSIGNMENT IRQ[15-3] 0, 1, 2, 8 AND 13 NOT AVAILABLE			
			DATA REGISTER BIT 1	DATA REGISTER BIT 0	DATA REGISTER BIT 1	DATA REGISTER BIT 0	BIT 3	BIT 2	BIT 1	BIT 0
RESOURCE ENABLE	15	W	X	X	D/A2 SELECT	READBACK ENABLE	REGISTER SELECT	DATA DRQ ENABLE (4)	CMD DRQ ENABLE (4)	INTERRUPT ENABLE (4)
STATUS (5)	15	R	DATA READY	DATA DMA REQUEST PENDING (4)	CMD DMA REQUEST PENDING (4)	INTERRUPT REQUEST PENDING (4)	REGISTER SELECT STATUS	DATA DRQ ENABLE STATUS (4)	CMD DRQ ENABLE STATUS (4)	INTERRUPT EANBLE BIT STATUS (4)
IRQ REGISTER (6)	15	R	DATA READY	DATA DMA REQUEST PENDING (4)	CMD DMA REQUEST PENDING (4)	DA2 IRQ PENDING	DIO IRQ PENDING	DA/1 IRQ PENDING	AD/2 IRQ PENDING	AD/1 IRQ PENDING

Notes: **(1) Accessed when READBACK ENABLE (BASE +15 bit 4) = 1**

(2) Accessed when REGISTER SELECT (BASE +15 bit 3) = 0

(3) Accessed when REGISTER SELECT (BASE +15 bit 3) = 1

(4) 0=Disabled, 1=Enable

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The Linear Tech LTC-2704 devices are unique in that each channel consists of a double-buffered data register (B1 Code and B2 Code) and a double-buffered span register (B1 Span and B2 Span). B1 buffers are the holding buffers and data is loaded into each one using a write operation, the DAC outputs are not affected. The contents of the B2 buffers can only be updated by copying the contents of B1 into B2 via an update operation initiated by the Command Code. The contents of the B2 buffers (both DAC Span and DAC Code) directly control the DAC output voltage or the DAC output range. Configuration, programming and writing of the D/A data is achieved through a series of control registers listed below for each DAC.

Command Register

Each DAC contains a command register used to configure the span and load the data. The command word consists of a 4-bit command and a 4-bit address, as shown. Each DAC contains a command register used to configure the span and load the data. The command word consists of a 4 bit command and a 4-bit address, as shown.

7	6	5	4	3	2	1	0
C3	C2	C1	C0	A3	A2	A1	A0

Command Codes

C3	C2	C1	C0	COMMAND	Readback Point Current Input Word	Readback Pointer Next Input Word
0	0	1	0	Write to B1 Span DAC n	Set by Previous Command	B1 Span DAC n
0	0	1	1	Write to B1 Span DAC n	Set by Previous Command	B1 Code DAC n
0	1	0	0	Update B1 → B2 DAC n	Set by Previous Command	B2 Span DAC n
0	1	0	1	Update B1 → B2 All DAC n	Set by Previous Command	B2 Code DAC n
0	1	1	0	Write to B1 Span DAC n Update B1 → B2 DAC n	Set by Previous Command	B1 Span DAC n
0	1	1	1	Write to B1 Code DAC n Update B1 → B2 DAC n	Set by Previous Command	B2 Code DAC n
1	0	0	0	Write to B1 Span DAC n Update B1 → B2 All DACs	Set by Previous Command	B2 Span DAC n
1	0	0	1	Write to B1 Code DAC n Update B1 → B2 All DACs	Set by Previous Command	B2 Code DAC n
1	0	1	0	Read B1 Span DAC n	B1 Span DAC n	
1	0	1	1	Read B1 Code DAC n	B1 Code DAC n	
1	1	0	0	Read B2 Span DAC n	B2 Span DAC n	
1	1	0	1	Read B2 Code DAC n	B2 Code DAC n	
1	1	1	1	No Operation	Set by Previous Command	B2 Span DAC n

Codes not shown are reserved and should not be used

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Address Codes

A3	A2	A1	A0	n	Readback Pointer n
0	**0**	**0**	**0**	DAC A	DAC A
0	**0**	**1**	**0**	DAC B	DAC B
0	**1**	**0**	**0**	DAC C	DAC C
0	**1**	**1**	**0**	DAC D	DAC D
1	**1**	**1**	**1**	All DACs	DAC A

Codes not shown are reserved and should not be used

Span Codes

The span for each channel is set by loading the desired value into the data registers, then issuing one of the span commands. The last 4 bits set the span as shown below. The rest of the data should be set to **0**.

S3	S2	S1	S0	Span
0	**0**	**0**	**0**	Unipolar 0V to 5V
0	**0**	**0**	**1**	Unipolar 0V to 10V
0	**0**	**1**	**0**	Bipolar -5V to 5V
0	**0**	**1**	**1**	Bipolar -10V to 10V
0	**1**	**0**	**0**	Bipolar -2.5V to 2.5V
0	**1**	**0**	**1**	Bipolar -2.5V to 7.5V

Codes not shown are reserved and should not be used

Readback Enable

Each time a command is issued to one of Linear Tech LTC-2704 devices, the value of one of the buffers is simultaneously shifted out of the device. Except when issuing one of the specific readback commands (Ax, Bx, Cx, Dx), the data returned corresponds to the Readback Pointer from the previous command as shown in the Command Codes Table. The Readback Enable bit must be set to **1** to read this data.

Note: If the Readback Enable bit is set to **0**, a read of the DAC data registers will return the last value written to that register not the Readback value of the actual buffers.

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D/A Interrupts

To operate using interrupt mode, IRQ routing must be configured and interrupts enabled for each device. This is achieved with the Resource and Resource Enable registers. The following would apply to D/A1:

1. Write **xxxx1xxx** to bit 3 of BASE +11 (select access to Resource Register).
2. Write IRQ selection (0-15 hex) to bits 3-0 of BASE +10 (**xF Hex** = IRQ 15).
3. Write **xxxxxx1** BASE +11 to enable the IRQ.

Enabling an interrupt for D/A2 can be achieved in the same manner with the appropriate offset.

It is possible for both devices to share an interupt or use individual interrupts. When sharing interrupts, the most efficient method to determine which device generated an interrupt request is to utilize the Master Interrupt Status Register.

DMA Support

DMA operation is available for this device. A sample of these operations under DOS is provided on website. These operations under other operating systems can be quite complex and are beyond the scope of this manual.

D/A Examples

The most basic method is to first set the output span for a channel and then write the output value for that channel. Notice that the configuration and data write operations can each be performed with either a single or double instruction sequence. Each channel can be updated individually using command values 6x & 7x (for configuration and output data, respectively) which will pre-load the value and present it to the DAC with a single instruction sequence. The second option is to pre-load the configuration and output data using command values 2x & 3x and then present the values to the DAC either individually (with command value 4x) or simultaneously (with command value 5x).

Example 1 - Single Instruction Sequence

To configure and write data to a DAC channel, each with a single command sequence, is very simple. The configuration must be set first and then the data output is written. Of course the span configuration is only required to be set once unless changes are required during the application.

1. Write **xxxx0xxx** to bit 3 of BASE +11.	Select access to CMD
2. Write **Span data 0000xxxx** to BASE +8.	Where **xxxx** = Span
3. Write **00000000 (zero)** BASE +9.	High order byte for Span
4. Write **CMD 01100xxx** to BASE +10.	Where **xxx** = DAC channel
5. Write **Low Byte data** to BASE +8.	
6. Write **High Byte data** to BASE +9.	
7. Write **CMD 01110xxx** to BASE +10.	Where **xxx** = DAC channel
8. Additional channels are then programmed by repeating steps 2 through 7.	

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Example 2 - Double Instruction Sequence

The second option is to pre-load the configuration and output data using command values 2x and 3x and then present the values to the DAC either individually using command value 4x simultaneously with command value 5x.

This example will demonstrate pre-loading the span configuration and data output values for each DAC channel and then presenting the information simultaneously to all DAC channels.

1. Write **xxxx0xxx** to bit 3 of BASE +11.	Select access to **CMD**
2. To set Span Configuration for Channel 0:	
Write **Span Configuration data 00000000 (zero**) to BASE +8.	Set **Span** = 0V to 5V
Write **00000000 (zero)** to BASE +9.	High Order Data Byte
Write **CMD 00100000** to BASE +10.	Move data to B1 Span
3. To set Span Configuration for Channel 1:	
Write **Span Configuration data 00000001** to BASE +8.	Set **Span** = 0V to 10V
Write **00000000 (zero)** to BASE +9.	High Order Data Byte
Write **CMD 00100010** to BASE +10.	Move data to B1 Span
4. To set Span Configuration for Channel 2:	
Write **Span Configuration data 00000010** to BASE +8.	Set **Span** = -5V to 5V
Write **00000000 (zero)** to BASE +9.	High Order Data Byte
Write **CMD 00100100** to BASE +10.	Move data to B1 Span
5. To set Span Configuration for Channel 3:	
Write **Span Configuration data 00000011** to BASE +8.	Set **Span** = -10V to 10V
Write **00000000 (zero)** to BASE +9.	High Order Data Byte
Write **CMD 00100110** to BASE +10.	Move data to B1 Span
6. To pre-load Data Output for Channel 0:	
Write **Low Byte data** to BASE +8.	
Write **High Byte data** to BASE +9.	
Write **CMD 00110000** to BASE +10.	Move data to B1 Code
7. To pre-load Data Output for Channel 1:	
Write **Low Byte data** to BASE +8.	
Write **High Byte data** to BASE +9.	
Write **CMD 00110010** to BASE +10.	Move data to B1 Code
8. To pre-load Data Output for Channel 2:	
Write **Low Byte data** to BASE +8.	
Write **High Byte data** to BASE +9.	
Write **CMD 00110100** to BASE +10.	Move data to B1 Code
9. To pre-load Data Output for Channel 3:	
Write **Low Byte data** to BASE +8.	
Write **High Byte data** to BASE +9.	
Write **CMD 00110110** to BASE +10.	Move data to B1 Code
10. To simultaneously update all DAC channels:	

If the application requires all DAC channels to be configured to the same output span, command value 8x supports this action with a single instruction sequence. Likewise if all DAC channels will be written with the same data output then command value 9x both pre-loads and presents the value to all DAC channels with a single instruction sequence.

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REGISTERS

Register Definitions (WS16C48)

The PCM-MIO uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 17 unique registers within the WS16C48. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

BASE+	I/O Address Offset	Page 0	Page 1	Page 2	Page 3
16	**00H**	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
17	**01H**	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
18	**02H**	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
19	**03H**	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
20	**04H**	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
21	**05H**	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
22	**06H**	Int_Pending	Int_Pending	Int_Pending	Int_Pending
23	**07H**	Page/Lock	Page/Lock	Page/Lock	Page/Lock
24	**08H**	IRQ_REG	Pol_0	Enab_0	Int_ID0
25	**09H**	REV_LO	Pol_1	Enab_1	Int_ID1
26	**0AH**	REV_HI	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK

This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

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IRQ_REG

This register is accessible when Page 0 is selected. It is used to select the bus routine for the generated interrupt.

REV_LO

This register is accessible when Page 0 is selected. This register returns the low byte of the current revision level for the FPGA firmware.

REV_HIGH

This register is accessible when Page 0 is selected. This register returns the high byte of the current revision level for the FPGA firmware.

POL0 - POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

INT_ID0 – INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

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Master Interrupt Status Register

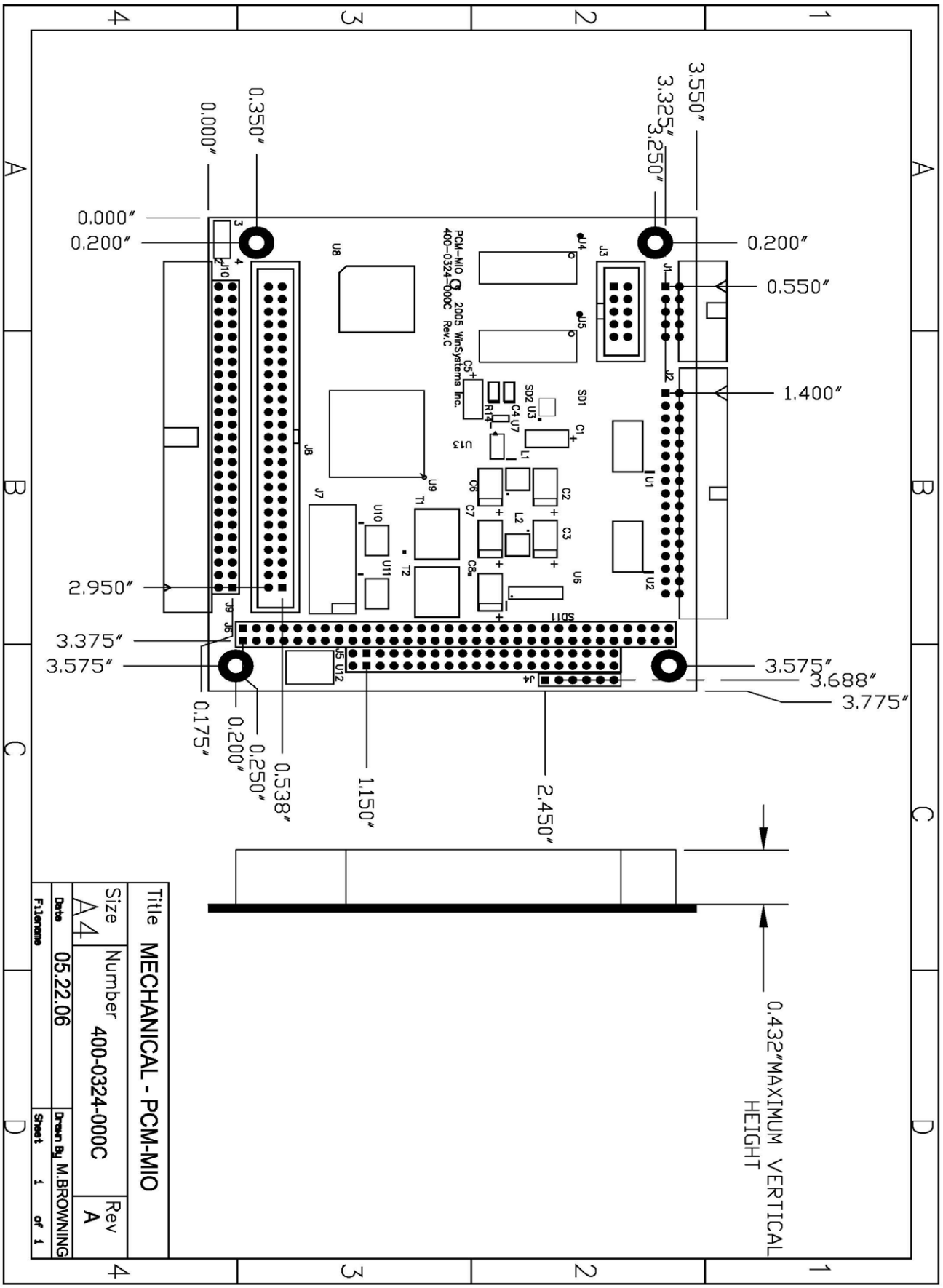
Although each device contains an interrupt pending status bit, a single read only register is also available to provide the status of all devices in one location. With the limited number of interrupts available, this register is very helpful by allowing your application to share a single interrupt amongst all the on-board devices. The register is accessible by properly selecting BIT 5 at BASE +15. When BIT 5 is set to 1, the register at (BASE+15) can be read as follows:

Interrupt Pending

X	X	X	D/A2	DIO	D/A1	A/D2	A/D1

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MECHANICAL DRAWING



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(http://www.winsystems.com/warranty.cfm)

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WARRANTY SERVICE

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.

2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.

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