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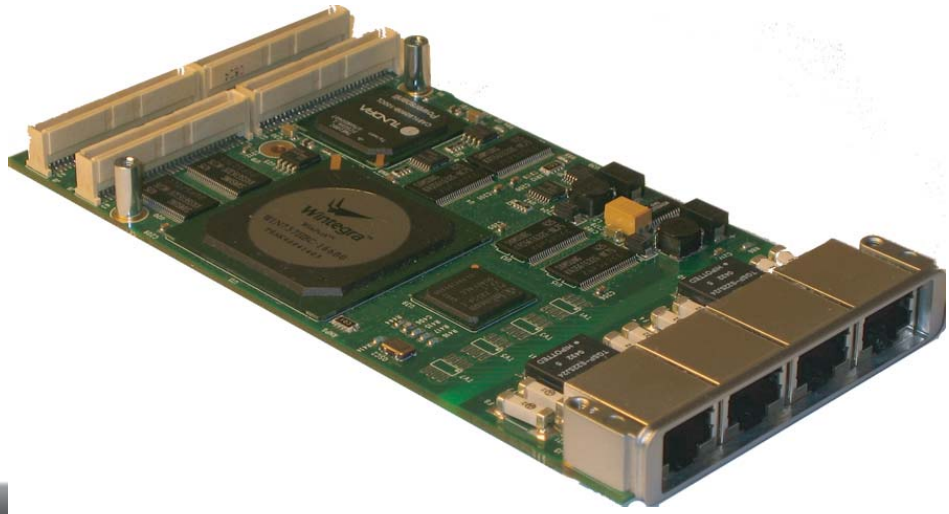
Find the *Xalyo Systems XS-TDM* at our website: ***Click HERE***

XS-TDM

Quad E1 / T1 / J1 Interface

Applications

- ATM
- SS7
- Sigtran
- Voice over Packet
- Wireless Networks
- Media/Signaling Gateways



Main Features

- ATM AAL0, AAL1, AAL2 & AAL5
- IMA
- PPP
- PICMG® 2.15 PT3MC
- WinPath™ Network Processor
- On-board 64-bit MIPS 5Kc™
- On-board Switching
- 384 MB SDRAM
- 16 MB Flash EPROM
- 8 KHz Tx and Rx Ref. Clock
- Linux and VxWorks®

XS-TDM is the third member of a family of PCI Telecom Mezzanine Card (PTMC) which offers high-end ATM and IP services at an attractive price. XS-TDM provides termination, switching and interworking capabilities from any port to any port.

XS-TDM performance and features are ideally suited for applications such as Wireless networking, Voice over Packet and Media Signaling Gateways.

Using the state of the art Wintegra™'s WinPath™ Network Processor, XS-TDM is the perfect interface to handle both ATM and IP simultaneously.

XS-TDM on-board 64-bit MIPS processor can run advanced protocols (e.g. 3GPP, SS7, ATM, VoIP) while the Network Processor handles all the data path.

Each of the four E1/T1/J1 ports can be individually programed by software and supports full E1/T1/J1, fractional E1/T1/J1 and channelized E1/T1/J1.

Compliant with IEEE 1386.1 PCI Mezzanine card (PMC) and PICMG 2.15 PCI Telecom Mezzanine Card (PTMC), the XS-TDM can be used in cPCI, cPSB, AdvancedTCA™, VME, PC, and proprietary applications.

XS-TDM architecture allows to bypass the bottleneck of current systems by handling all the processing on-board and performing segmentation and reassembly locally, which not only allows to offload the CPU on the carrier board but also optimizes bus transfers while doing termination.

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XS-TDM

Quad E1 / T1 / J1 Interface

ATM

- AAL0, AAL1, AAL2 & AAL5 (1)
- ATM cell switching
- AAL2 CID switching
- Traffic management as per TM 4 .1: CBR, VBR, GFR and UBR
- Per VC queueing
- Full UNI/NNI VPI/VCI range
- OAM F4 and F5 as per ITU-T I.610
- IMA (Inverse Multiplexing for ATM)
- CES (Circuit Emulation Services)

PT3MC

- PICMG® 2.15 compliant (3)
- UTOPIA L2 @ 50 MHz
- 8-bit data bus interface
- Master and slave configuration
- Cell size from 52 to 65 octets
- 8 KHz Tx and Rx reference clock
- Serial port
- RMII interface
- 6 x 8.192 MHz CT bus lines

Network Processor

- Wintegra™ WinPath™ @ 166 MHz
- 128 MBytes Packet SDRAM (4)
- 128 MBytes Parameter SDRAM
- 64-bit / 100 MHz SDRAM
- MIPS 5Kc™ CPU @ 166 MHz
- 2 WinGines
- Handles more than 18 data path protocols to date
- For more details see www.wintegra.com

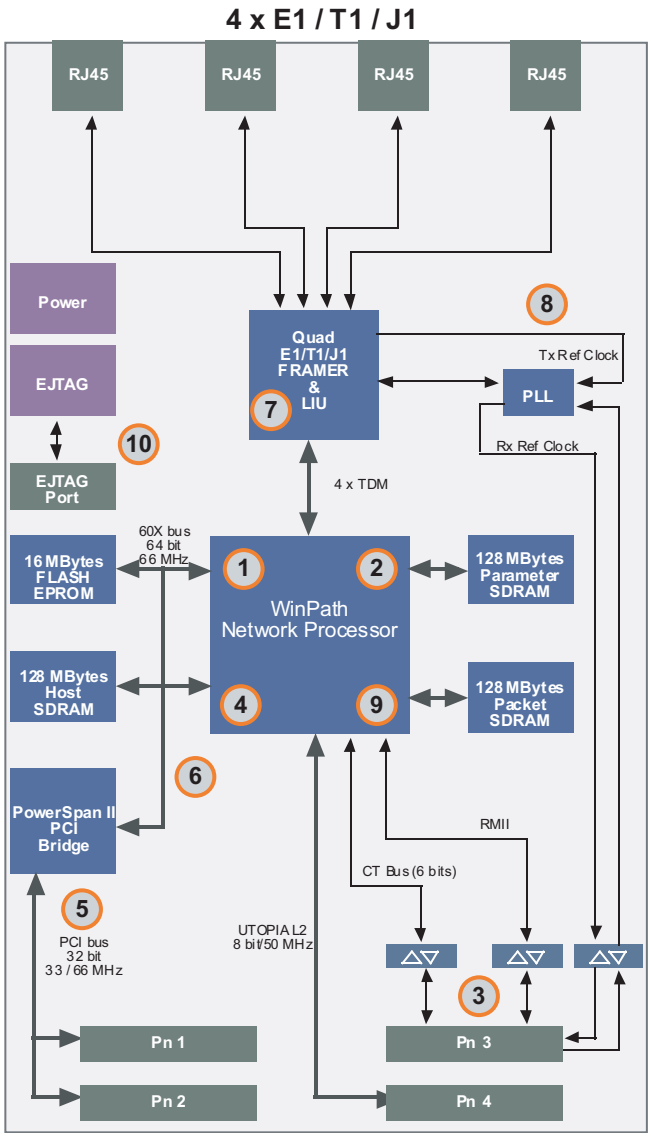
Interworking

- IP routing and forwarding over ATM (RFC 1483/2684/1577)
- IP routing and forwarding over PPP (RFC 1661)
- Multiple fields classification and DiffServ (RFC 2474/2475)
- MPLS tagging/detagging
- L2 interworking between ATM and Ethernet
- Interworking at 750'000 PPS

IP

- PPP support (2)
- HDLC support up to OC-12 rates
- Parsing of PPP over HDLC frames (RFC 2615 and RFC 1662)
- Packet scheduling

Block Diagram



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XS-TDM

Quad E1 / T1 / J1 Interface

System busses

PCI bus (5)

- PCI 2.2 Specification compliant
- 32-bit interface
- 33 / 66 MHz operation
- 3.3 V and 5 V signaling
- Intelligent I2O messaging

Host bus (6)

- PPC 60X @ 66 MHz
- 64-bit interface
- 128 MBytes Host Memory
- 16 MBytes Flash EPROM

Physical Layer

E1 / T1 / J1 (7)

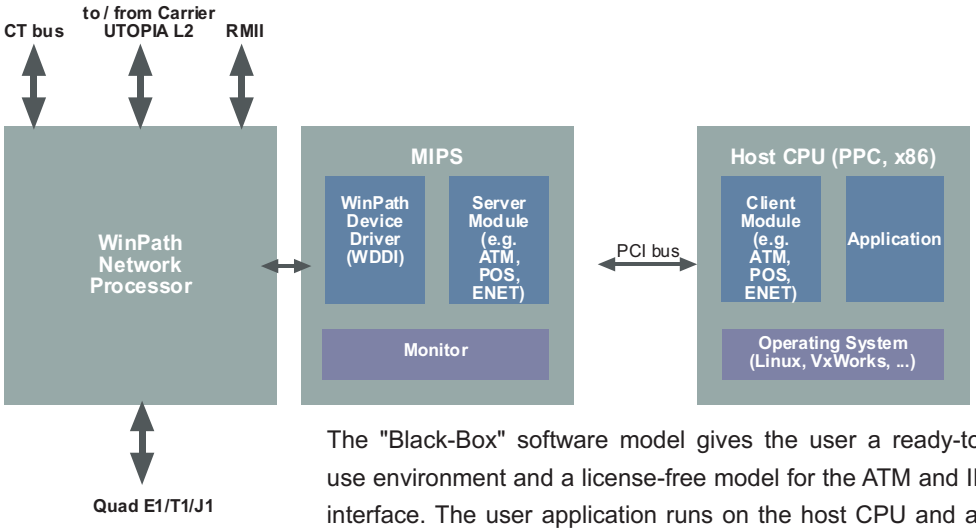
- Quad E1/T1/J1 ports
- Channelized or non-channelized
- Configuration selectable per port
- Fractional
- 4 x RJ45 connectors
- Protection cicuitry

Telecom Clock

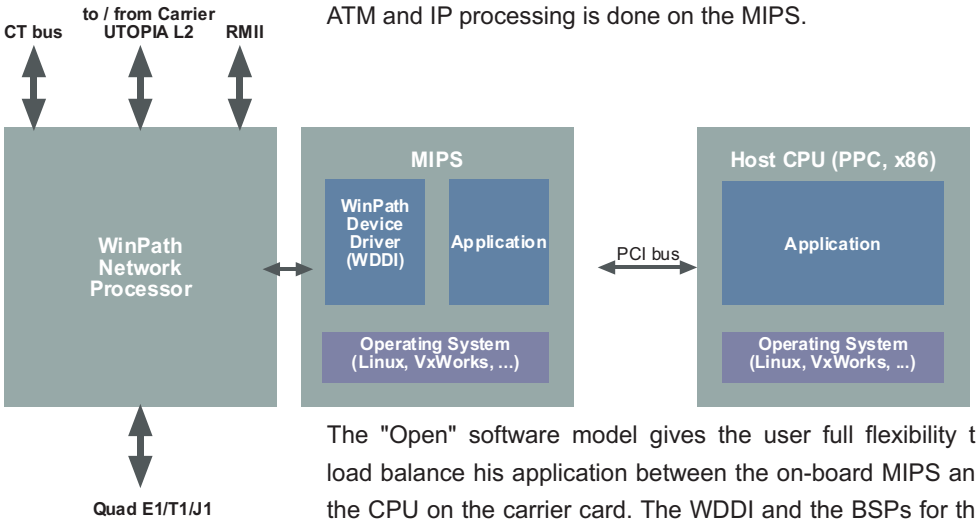
(8)

- 8 KHz PLL
- Meets TR62411, ETS300 011 and GR-1244 for Jitter/Wander for Stratum 3 and higher
- 8 KHz selectable from backplane or any E1/T1/J1 port
- 8 KHz reference output to backplane
- Locks to 8 KHz +/- 100 ppm

Software Model



The "Black-Box" software model gives the user a ready-to-use environment and a license-free model for the ATM and IP interface. The user application runs on the host CPU and all ATM and IP processing is done on the MIPS.



The "Open" software model gives the user full flexibility to load balance his application between the on-board MIPS and the CPU on the carrier card. The WDDI and the BSPs for the different operating systems are available in source code.

Protocols Supported

(9)

- ATM IMA
- AAL1 CES
- Frame Relay
- MTP2

Debug Connector

(10)

- 14 points Enhanced JTAG port for debugging (software breakpoints, single step mode)
- Easy to fit optionnal connector

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XS-TDM

Quad E1 / T1 / J1 Interface

Specifications

Form factor	PTMC Option 3
Dimensions	74 mm x 149 mm
PCI bus	32-bit, 33 and 66 MHz
Host bus	64-bit, 66 MHz
UTOPIA bus	8-bit, 50 MHz, L2
E1/T1/J1 connector	RJ-45
Telecom reference clock	8 Khz
Communication ports	4 x E1/T1 J1
UART	RS232
Protocols	ATM and IP
Flash memory	16 MBytes, 150 ns
Host memory	128 MBytes, 66 MHz
Parameter memory	128 MBytes, 100 MHz
Packet memory	128 MBytes, 100 MHz
Operating systems	Linux, VxWorks®
Operating temperature	0 to 55°C
Storage temperature	-40 to 85°C
Relative humidity	5% to 90% non-condensing
Altitude	0 to 15'000 ft
Power consumption	7.0 W max
3.3 V	3.0 W max
5.0 V	4.0 W max

Standards compliance

PCI	PCI Local Bus Specification Rev. 2.2
IEEE P1386	CMC: Common Mezzanine Card
IEEE P1386.1	PMC: PCI Mezzanine Card
IEEE 1149.1	JTAG
IEEE 802.3	CSMA/CD (EThernet)
PICMG® 2.15	PTMC: PCI Telecom Mezzanine Card
RFC 1483	Multiprotocol Encapsulation over AAL5
RFC 1577	Classical IP and ARP over ATM
RFC 1661	The Point-to-Point Protocol (PPP)
RFC 1662	PPP in HDLC-like Framing
RFC 2474	Definition of the Differentiated Services Field in the IPv4 and IPv6 Headers
RFC 2475	An Architecture for Differentiated Services
RFC 2684	Multiprotocol Encapsulation over AAL5
ITU-T I.431	Primary Rate User-Network Interface - Layer 1 Specification
ITU-T I.432	B-ISDN User-Network Interface
ITU-T I.363.1	B-ISDN ATM Adaptation Layer Type 1
ITU-T I.363.2	B-ISDN ATM Adaptation Layer Type 2
ITU-T I.363.5	B-ISDN ATM Adaptation Layer Type 5
ITU-T I.366.1	Segmentation and Reassembly Service Specific Convergence Sublayer for the AAL type 2
ITU-T I.610	B-ISDN Operation and Maintenance Principles and Functions
ITU-T G.703	Physical/electrical Characteristics of Hierarchical Digital Interfaces
ITU-T G.704	Synchronous Frame Structures
ITU-T G.706	Frame Alignment and CRC for G.704
ITU-T G.732	Characteristics of Primary PCM Multiplex Equipment at 2048 kbit/s
ITU-T G.736	Characteristics of Synchronous digital Multiplex equipment at 2048 kbit/s
ITU-T G.775	LOS, AIS and RDI criteria for PDH
ITU-T G.781	Synchronization Layer Functions
ITU-T G.804	ATM Cell Mapping intpo PDH
ITU-T G.823	Control of Jitter and Wander (E1)
ITU-T Q.703	Signaling Link
GR-1244	Clocks for the Synchronized Network: Common Generic Criteria
ATM Forum TM4.1	Traffic Management
AT&T TR62411	Control of Jitter and Wander (T1/J1)

Why choose XS-TDM ?

XS-TDM: A Flexible Solution

XS-TDM brings even more flexibility to the concept of PMC with the use of a network processor which is entirely re-configurable to support new standards. The PTMC standard adds modularity to the way building blocks are connected together at the system level. Support for ATM, IMA, PPP and channelized TDM interface on a per E1/T1/J1 port basis provides the user with all the options on a very compact form factor.

XS-TDM: A High Performance Solution

XS-TDM architecture improves the overall throughput by segmenting and reassembling packets on the PMC itself. This allows maximizing PCI bandwidth and reaching performance levels that are impossible to achieve on conventional designs. As all the resources are dedicated for the ATM and IP traffic in a deterministic way, XS-TDM data rates are more reliable, resulting in better quality of service.

XS-TDM: A Scalable and Coherent Solution

XS-TDM is the third member of a family of interfaces implementing data rates from E1/T1 to OC-12 and Gigabit Ethernet, all using the same architecture, thus giving the same look and feel to the user.

XS-TDM: A Modern Solution

Xalyo Systems' ATM and IP interfaces are based on a leading edge network processor handling all the data path in hardware while the control path is handled by a processor running VxWorks® or LINUX. An open API is provided on the PCI bus which makes the solution plug and play on virtually any platform, any processor, and any operating system.

Ordering Information

XS-TDM	Quad E1 / T1 / J1 Interface, 166 MHz, 384 MB SDRAM, 16 MB Flash

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