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XVME-675

VMEbus PC/AT Processor Module

P/N 74675-001B

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XYCOM
750 North Maple Road
Saline, Michigan 48176-1292
734-429-4971 (phone)
734-429-1010 (fax)

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1.1 PRODUCT OVERVIEW

The XVME-675 is a VMEbus PC/AT processor module designed to combine the high performance and rugged packaging of the VMEbus with the broad application software base of the IBM PC/AT standard. This 6U double-high module requires a single VMEbus slot, is PC/AT compatible, and supports all standard PC/AT software. XVME-675 incorporates the 100 MHz 80486DX4 processor. The board is available with two memory options: 16 or 32 Mbytes of dual-access DRAM.

The XVME-675 contains a VMEbus and PC/AT-bus interface, a floppy disk interface, a high-performance IDE hard disk controller, and a Super VGA graphics controller with 1 Mbyte of Video RAM. The module provides two serial ports, one parallel port, PS/2-compatible keyboard and mouse ports, and a watchdog timer.

The module features complete 32-bit VMEbus master/slave interfaces, which allows users to communicate easily with the VMEbus short I/O, standard, and extended address spaces. This module also contains VMEbus slot 1 functions, as well as a complete VMEbus interrupter and interrupt handler.

1.2 XVME-675 FEATURES

The XVME-675 PC/AT Processor Module has the following features:

- 100 MHz 80486DX4 microprocessor
- 16 or 32 Mbytes of dual-access DRAM
- Shadow RAM option for system BIOS and the VGA BIOS
- Zero wait-state DRAM controller with intelligent write buffer
- Floppy disk controller: 360 Kbytes, 720 Kbytes, 1.2 Mbytes, and 1.44 Mbytes
- Super VGA controller
- BitBLT engine
- 1024x768, 256 colors
- 64 x 64 hardware cursor
- 1 Mbyte video RAM
- IDE hard drive controller (AT Drive)
- Two RS-232C-compatible serial ports
- One Centronics-compatible parallel port
- PS/2-compatible keyboard and mouse ports
- PC/104 expansion site
- VMEbus A32/A24/A16:D32/D16/D08(EO) DTB Master
- VMEbus A32/A24:D32/D16/D08(EO) DTB Slave
- Programmable byte-swapping hardware for VMEbus master and slave

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- Programmable Release On Request (ROR)
- VMEbus IH(1)-IH(7) interrupt handler
- VMEbus I(1)-I(7) dynamic interrupter
- VMEbus system resource module (slot 1) functions with programmable bus timeout
- Programmable R(0-3) bus request level
- VMEbus SYSFAIL driver
- Single-level bus arbiter

1.3 OPERATIONAL DESCRIPTION

The XVME-675 block diagram is illustrated in Figure 1-1.

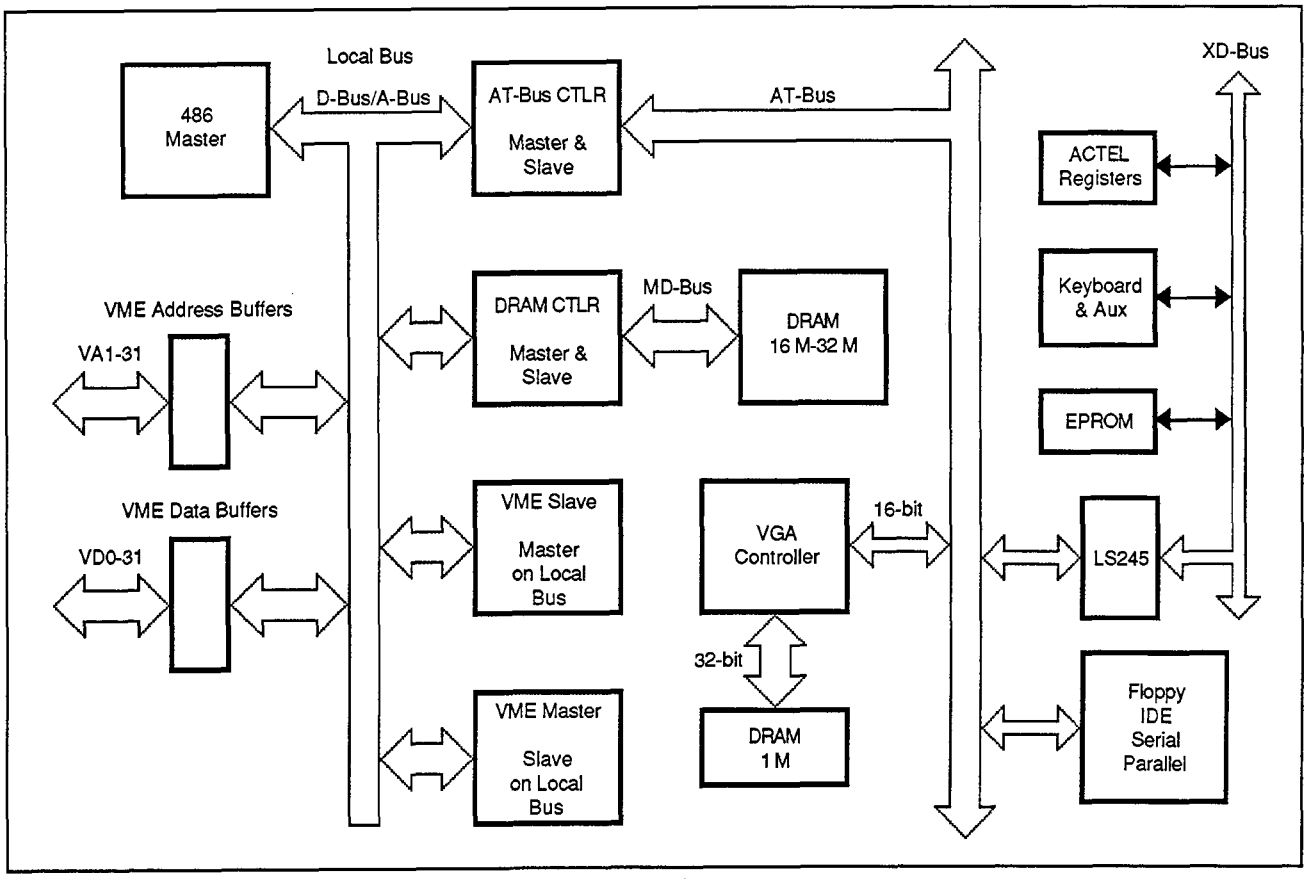


Figure 1-1. XVME-675 Block Diagram

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1.4 ARCHITECTURE

As Figure 1-1 illustrates, the XVME-675 provides a complete 80486DX4 PC/AT-compatible computer with a full 32-bit VMEbus interface in a single VMEbus slot. The module uses an integrated AT chipset to provide basic PC/AT functions. This chipset features an intelligent DRAM controller with write buffer technology for system DRAM interface and an integrated AT-bus controller.

The VMEbus master/slave interface is located on the 80486 local bus to increase the performance of VMEbus cycles. The VMEbus slave interface duplicates an 80486 local bus cycle when reading or writing to the dual-access system DRAM. This architecture allows the DRAM controller to respond to a VMEbus slave access as if it were an 80486 access.

The on-board AT bus provides the interface to a standard set of PC/AT peripheral devices, such as serial ports, printer port, keyboard and mouse ports, system BIOS, Super VGA controller, floppy and hard disk controllers, and the PC/104 expansion site.

1.4.1 CPU

The XVME-675 features a 100 MHz 80486DX4, offering a 50% increase in performance over the Intel 486DX2. The DX4 features a 16-Kbyte on-chip cache, internal floating point unit, paged, virtual memory management, and complete 32-bit internal architecture.

1.4.2 DRAM Controller

The XVME-675 is available with 16 or 32 Mbytes of DRAM memory. It features an advanced DRAM controller that has an internal write buffer that is four double words deep. The write buffer allows writes from the CPU to be completed in zero wait states. The writes are then posted to the DRAM in First-In, First-Out (FIFO) order. Three features are included to increase the efficiency of the write buffers: out of order operation (reads propagate ahead of writes), byte gathering, and the ability to service reads from the write buffers. The DRAM controller also supports 80486 burst CPU reads from DRAM.

1.4.3 AT-bus Controller

The AT-bus controller contains the 8237 DMA controllers, the 8259 interrupt controllers, the 8254 interval timer, and the control logic to convert the 80486 CPU cycles to AT-bus cycles. The AT-bus signals are driven directly from this chip.

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1.4.4 VGA Controller

The VGA controller uses a 16-bit AT-bus interface and a 32-bit interface to video RAM. This feature allows all writes to video RAM accesses to be performed with zero wait states.

The VGA BIOS can be optionally shadowed using 32-bit DRAM. Shadowing the VGA BIOS increases video performance. Performance of the video controller is greatly enhanced by the addition of a Bit Block Transfer (BitBLT) engine and a 64 x 64 hardware cursor. The BitBLT engine off-loads the CPU when doing screen-to-screen memory transfers. This enhances the performance of graphical programs and operating systems such as Microsoft® Windows™. A display driver is required to take advantage of these features.

The XVME-675 VGA controller supports all IBM VGA modes to the register level. It also supports the EGA, CGA, and MDA modes to the register level. The VGA adapter with 1 Mbyte of DRAM installed supports Super VGA up to 1024 x 768 by 256 colors.

The VGA controller supports IBM modes 0-13h. In addition to these standard IBM modes, the following Super VGA resolutions are supported:

640 x 480 x 256 colors
640 x 480 x 32k colors
640 x 480 x 64k colors
800 x 600 x 16 colors
800 x 600 x 256 colors
800 x 600 x 32k colors
800 x 600 x 64k colors
1024 x 768 x 16 colors (interlaced or non-interlaced)
1024 x 768 x 256 colors (interlaced or non-interlaced)

A jumper is provided on interrupt 9 (IRQ9) to allow the VGA controller to drive the interrupt or other cards to use the interrupt. An additional jumper is provided to disable the VGA controller and BIOS. This allows other video adapters to be used instead of the controller provided on the XVME-675.

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1.4.5 Serial and Parallel Ports

There are two 16550-compatible serial ports and one parallel port on the XVME-675. The RS-232C-compatible serial ports are controlled in the BIOS Setup Menu. This allows the ports to be software enabled or disabled.

1.4.6 Floppy Drive Controller

The floppy drive controller supports two AT-compatible drives. These drives may be any combination of 3.5-inch or 5.25-inch disk drives with 360 Kbyte, 720 Kbyte, 1.2 Mbyte, or 1.44 Mbyte capacities.

1.4.7 Hard Drive Controller

The XVME-675 uses the IDE interface for the hard drive controller. This 16-bit interface provides hardware-level compatibility to the IBM AT hard drive controller.

Two drives may be connected to the interface by daisy chaining the ribbon cable and setting one drive as a master and the other drive as a slave. This setting is usually done through jumpers on the drive (consult your drive manual). The IDE ribbon cable should be no longer than 18 inches.

CAUTION
Please check your IDE drive manual for formatting procedures. Most IDE drives should never be low-level formatted.

1.4.8 Keyboard Controller

The PS/2-compatible XVME-675 keyboard controller not only supports the PS/2 keyboard, but also provides an auxiliary input for a PS/2-compatible mouse, trackball, etc. The connector is a six-pin MINI DIN for both the keyboard and the auxiliary device. An interface cable is shipped with every module to allow the use of a standard PC/AT keyboard.

1.4.9 PC/104 Expansion Site

To support additional PC/AT functions, the XVME-675 provides an open-architecture PC/104-compatible expansion site. This allows the use of PC/104-compatible modules to provide functions such as Ethernet, solid state disks, SCSI interface, or additional serial ports. Power for expansion modules is provided through the connector.

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1.5 SPECIFICATIONS

Table 1-1. XVME-675 Environmental Specifications

Specification	**Description**
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-operating	50 g peak acceleration, 11 msec duration
Vibration	
Frequency	5 to 2000 Hz
Operating	.015" peak-to-peak displacement 2.5 g (maximum) acceleration
Non-operating	.030" peak-to-peak displacement 5.0 g (maximum) acceleration
Humidity	5% to 95% RH non-condensing
Altitude	
Operating	Sea level to 10,000 feet (3048 m)
Non-operating	Sea level to 50,000 feet (15240 m)
Temperature	
Operating	0° to 28°C (32° to 82°F), no air flow 0° to 64°C (32° to 147°F), 600 feet/min air flow
Non-operating	-40° to 85°C (-40° to 185°F)

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Table 1-2. XVME-675 Hardware Specifications

Specification	**Description**
CPU speed	100 MHz 80486DX4
AT-bus speed	8.25 MHz
Graphics controller	VGA analog output Maximum resolution: 1024 x 678, 256 colors
Floppy disk interface	AT compatible; supports two drives
Hard disk interface	IDE controller
Keyboard interface	PS/2 compatible
PS/2 AUX port	PS/2 mouse compatible
Serial ports	RS-232C compatible
Parallel port	Centronics compatible
Power specifications +12V -12V +5V	 24 mA maximum -24 mA maximum 3.9 A typical, 4.9 A maximum

Following are the VMEbus compliance specifications for the XVME-675, which complies with VMEbus specification IEEE 1014—1987 Rev. C1:

- A32/A24/A16:D32/D16/D08(EO) DTB Master
- A32/A24:D32/D16/D08(EO) DTB Slave
- R(0-3) Bus Requester
- Interrupter I(1)-I(7) DYN
- SYSCLK and SYSRESET Driver
- SGL Arbiter
- RWD, ROR bus release
- Form Factor: DOUBLE
  233.35 mm x 160 mm (9.2" x 6.3")

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2.1 INTRODUCTION

This chapter provides configuration information for the XVME-675 VMEbus PC/AT Processor Module. It also describes how to install the XVME-675 into a backplane and add extended BIOS.

2.2 JUMPERS

The XVME-675 uses 10 jumpers to configure hardware options. All jumpers are shipped in position A.

> **NOTE**
> Unless you wish to disable VGA or replace the BIOS EPROM with Flash, all jumpers should be left in the default position.

> **NOTE**
> Silk screened jumper definitions are located on the top of the CPU board.

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Table 2-1. Jumper Settings

Jumper	Setting	Description
J1	A✓ B	CPU option 80486 CPU option 80486SX
J2	A✓ B	CPU option 80486 CPU option 80486SX
J3	A✓ B	CMOS okay CMOS clear
J4, J5, J6	OUT	Install for +5V P24T Pentium overdrive processor
J7	A✓ B	ROM or Flash non-writable +5 V Flash +12 V
J8	A✓ B	VGA enabled VGA disabled
J9	A✓ B	IRQ12 driven by auxiliary port IRQ12 not driven by auxiliary port
J10	A✓ B	IRQ9 driven by the VGA controller IRQ9 not driven by the VGA controller

✓ = default setting

NOTE

Perform the following steps to clear the CMOS RAM configuration:

1. Change J3 to position B.
2. Power up the board until both the Pass and Fail LEDS turn off.
3. Turn off the power and switch J3 to position A.
4. Power up the board again.

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2.3 SWITCH SW1

Switch SW1 on the XVME-675 allows critical options not under software control to be enabled in one common area.

> **NOTE**
> Silk screened switch definitions are located on the back of the CPU board.

Table 2-2. Switch SW1 Settings

Position	Setting	Description
1	Open Closed✓	VME SYSRESET* not driven on power up VME SYSRESET* driven on power up
2	Open Closed✓	VME SYSRESET* not caused by toggle switch VME SYSRESET* caused by toggle switch
3	Open✓ Closed	VME SYSFAIL not driven on VMEbus VME SYSFAIL driven on VMEbus
4	Open Closed✓	System resources disabled System resources enabled
5	Open✓ Closed	Local reset disabled Local reset caused by toggle switch
6	Open✓ Closed	Reserved Reserved
7	Open✓ Closed	Keyboard enabled Keyboard inhibited
8	Open✓ Closed	Open✓ Closed

✓ = default setting

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2.4 CONNECTORS

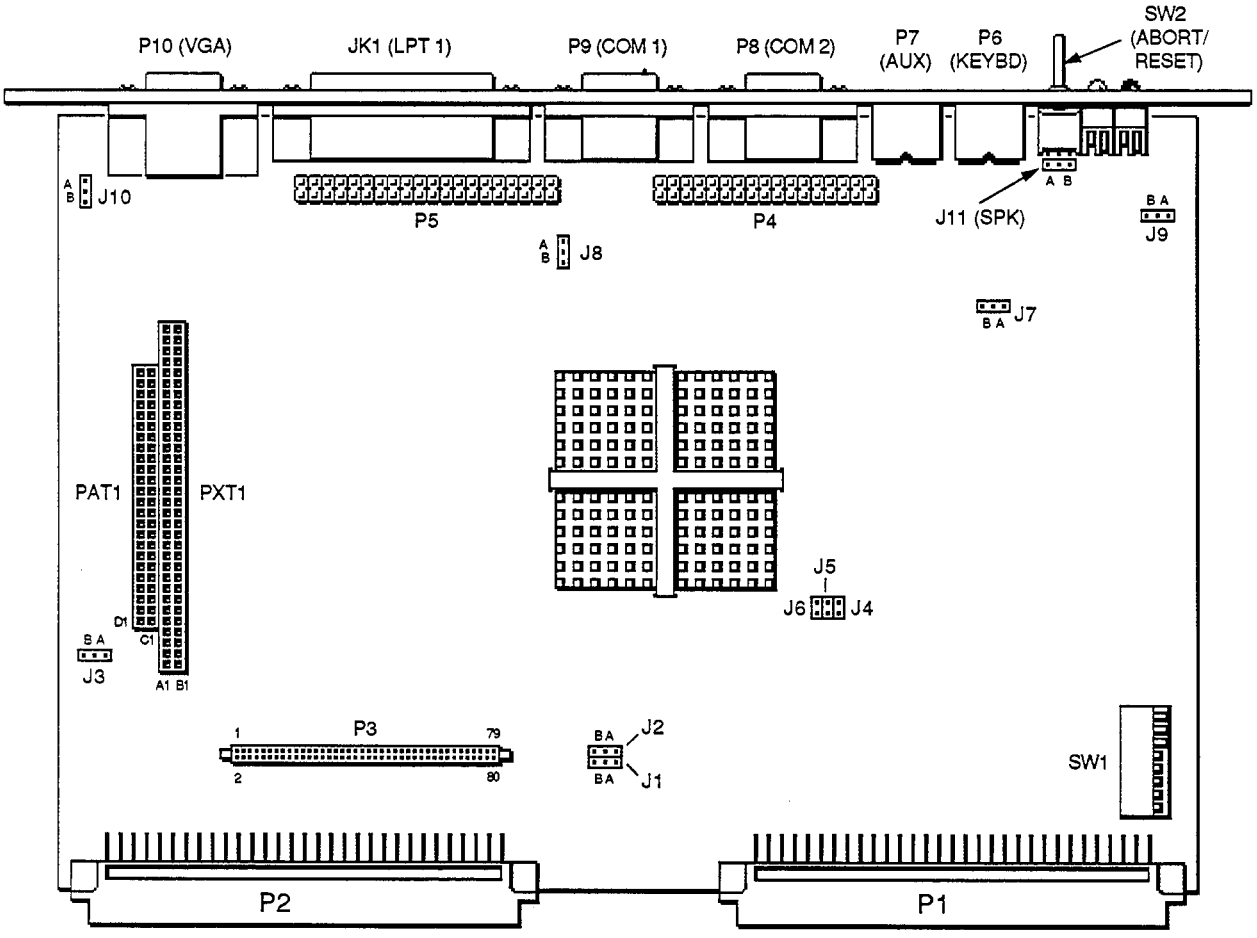


Figure 2-1. XVME-675 Connectors and Jumpers

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2.4.1 Keyboard Connector

The keyboard connector, P6, is a six-pin MINI DIN connector.

Table 2-3. Keyboard Connector (P6)

Pin	Description
1	DATA
2	NC
3	GND
4	+5V
5	CLK
6	NC

2.4.2 Auxiliary Connector

The auxiliary connector, P7, is a six-pin MINI DIN connector designed to be PS/2 compatible. This port accepts a PS/2-compatible mouse, track ball, etc.

Table 2-4. Auxiliary Connector (P7)

Pin	Description
1	DATA
2	NC
3	GND
4	+5V
5	CLK
6	NC

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2.4.3 Speaker Connector

The speaker connector, J11, is a three-pin header.

Table 2-5. Speaker Connector (J11)

Pin	Description
1	Signal
2	+5V
3	NC

2.4.4 COM1 Serial Port Connector

The primary serial connector, located on the front panel, is a nine-pin D subminiature designated P9.

Table 2-6. COM1 Serial Port Connector (P9)

Pin	Description
1	DCD1
2	RXD1
3	TXD1
4	DTR1
5	GND
6	DSR1
7	RTS1
8	CTS1
9	R11

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2.4.5 COM2 Serial Port Connector

The secondary serial connector, located on the front panel, is a nine-pin D subminiature designated P8.

Table 2-7. COM2 Serial Port Connector (P8)

Pin	Description
1	DCD2
2	RXD2
3	TXD2
4	DTR2
5	GND
6	DSR2
7	RTS2
8	CTS2
9	R12

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2.4.6 **Parallel Port Connector**

The parallel port connector, JK1, is a 25-pin female D subminiature connector.

Table 2-8. Parallel Port Connector (JK1)

Pin	Description
1	STROBE
2	PDOUT0
3	PDOUT1
4	PDOUT2
5	PDOUT3
6	PDOUT4
7	PDOUT5
8	PDOUT6
9	PDOUT7
10	PACK
11	PBUSY
12	PE
13	SELECT
14	AUTOFEED
15	PERROR
16	INIT
17	SELIN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

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2.4.7 VGA Connector

The VGA connector, P10, is a high-density 15-pin D subminiature.

Table 2-9. VGA Connector (P10)

Pin	Description
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	KEY
10	GND
11	NC
12	NC
13	HSYNC
14	VSYNC
15	NC

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2.4.8 **Floppy Drive Connector**

The floppy drive connector, P4, is a 34-pin header.

Table 2-10. Floppy Drive Connector (P4)

Pin	Description
1	GND
2	FRWC*
3	GND
4	NC
5	KEY
6	NC
7	GND
8	IDX*
9	GND
10	MOI*
11	GND
12	FDS2*
13	GND
14	FDS1*
15	GND
16	MO2*
17	GND
18	FDIRC*
19	GND
20	FSTEP*
21	GND
22	FWD*
23	GND
24	FWE*
25	GND
26	FTKO*
27	GND
28	FWP*
29	GND
30	FRDD*
31	GND
32	FHS*
33	GND
34	DCHG*

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2.4.9 IDE Drive Connector

The IDE Drive Connector, P5, is a 40-pin connector.

Table 2-11. IDE Drive Connector (P5)

Pin	Description
1	RESET*
2	GND
3	SD7
4	SD8
5	SD6
6	SD9
7	SD5
8	SD10
9	SD4
10	SD11
11	SD3
12	SD12
13	SD2
14	SD13
15	SD1
16	SD14
17	SD0
18	SD15
19	GND
20	N/C
21	N/C
22	GND
23	IOW*
24	GND
25	IOR*
26	GND
27	N/C
28	ALE
29	N/C
30	GND
31	IDINT
32	ATIOCS16*
33	SA1
34	N/C
35	SA0
36	SA2
37	HCS0*
38	HCS1*
39	N/C
40	GND

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2.4.10 **VMEbus Connectors**

The P1 and P2 VMEbus connectors are 96-pin DIN connectors.

Table 2-12. VMEbus Connector (P1)

Pin	A	B	C
1	D00	BBBUSY	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5v STDBY	+12V
32	+5V	+5V	+5V

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Table 2-13. VMEbus Connector (P2)

Pin	A	B	C
1	N/C	+5V	N/C
2	N/C	GND	N/C
3	N/C	N/C	N/C
4	N/C	A24	N/C
5	N/C	A25	N/C
6	N/C	A26	N/C
7	N/C	A27	N/C
8	N/C	A28	N/C
9	N/C	A29	N/C
10	N/C	A30	N/C
11	N/C	A31	N/C
12	N/C	GND	N/C
13	N/C	+5V	N/C
14	N/C	D16	N/C
15	N/C	D17	N/C
16	N/C	D18	N/C
17	N/C	D19	N/C
18	N/C	D20	N/C
19	N/C	D21	N/C
20	N/C	D22	N/C
21	N/C	D23	N/C
22	N/C	GND	N/C
23	N/C	D24	N/C
24	N/C	D25	N/C
25	N/C	D26	N/C
26	N/C	D27	N/C
27	N/C	D28	N/C
28	N/C	D29	N/C
29	N/C	D30	N/C
30	N/C	D31	N/C
31	N/C	GND	N/C
32	N/C	+5V	N/C

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2.4.11 PXT1 Connector (PC/104 Expansion Site)

PXT1 is a 32-pin connector that, along with PAT1, is used to add PC/104 expansion modules to the XVME-675.

Table 2-14. PXT1 Connector

Pin	Row A Signal	Row B Signal
1	IOCHCHK*	GND
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	N/C
6	SD3	DRQ2
7	SD2	-12V
8	SD1	N/C
9	SD0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW*
12	SA19	SMEMR*
13	SA18	IOW*
14	SA17	IOR*
15	SA16	DACK3*
16	SA15	DRQ3
17	SA14	DACK1*
18	SA13	DRQ1
19	SA12	REF*
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2*
27	SA4	T/C
28	SA3	ALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND

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2.4.12 PAT1 Connector (PC/104 Expansion Site)

PAT1 is a 24-pin connector that, along with PXT1, is used to add PC/104 expansion modules to the XVME-675.

Table 2-15. PAT1 Connector

Pin	Row C Signal	Row D Signal
0	GND	GND
1	SBHE*	MEMCS16*
2	LA23	IOCS16*
3	LA22	IRQ10
4	LA21	IRQ11
5	LA20	IRQ12
6	LA19	IRQ15
7	LA18	IRQ14
8	LA17	DACK0*
9	MEMR*	DRQ0
10	MEMW*	DACK5*
11	SD8	DRQ5
12	SD9	DACK6*
13	SD10	DRQ6
14	SD11	DACK7*
15	SD12	DRQ7
16	SD13	+5V
17	SD14	N/C
18	SD 15	GND
19	KEY	GND

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2.5 INSTALLING THE XVME-675 INTO A BACKPLANE

This section provides the information necessary to install the XVME-675 PC/AT Processor Module into the VMEbus backplane.

Xycom modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-675 is a double-high, single-board VMEbus module. As such, it requires one slot with both the P1 and P2 backplanes.

> **CAUTION**
> Do not attempt to use the XVME-675 in a VMEbus system without a P2 backplane.

The XVME-955 Hard Disk/Floppy Disk Module, available from Xycom, is ideally suited for use with the XVME-675. It combines a high-capacity, 3.5-inch IDE drive and a 3.5-inch, 1.44 Mbyte micro-floppy in a unit that occupies only two double-high VMEbus slots. Ask your Xycom representative for details.

The XVME-957 Hard Disk/Floppy Disk Module, available from Xycom, is also ideally suited for use with the XVME-675. The XVME-957 contains a 2.5-inch IDE hard disk and a 3.5-inch, 1.44 Mbyte floppy disk. The unit plugs easily into a VMEbus backplane and occupies only one VMEbus slot.

> **WARNING**
> Do not install or remove any boards before turning off power to the bus and all related external power supplies.

1. Turn off the power to the backplane.

2. Make sure the P1 and P2 backplane connectors are accessible.

3. Verify all jumper settings.

4. Connect the floppy disk cable to P4 on the component side of the XVME-675 board. Refer to Figure 2-1 for the location of P4.

5. Connect the IDE hard drive cable to P5 on the component side of the XVME-675 module. Refer to Figure 2-1 for the location of P5.

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6. Verify that the card cage slot that will hold the XVME-675 is clear and accessible. If using the XVME-675 in conjunction with the XVME-955 module, make sure that the two card cage slots to the right of the XVME-675 (which will hold the XVME-955) are also clear. If using the XVME-675 in conjunction with the XVME-957 module, make sure that one card cage slot to the right of the XVME-675 (which will hold the XVME-957) is also clear.

7. Install the XVME-675 into the card cage by centering the unit on the plastic guides in the slots (P1 connector facing up) and pushing the boards slowly toward the rear of the chassis until the P1 and P2 connectors engage. The boards should slide freely in the plastic guides.

> **CAUTION**
> Do **not** use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

8. Secure the module to the chassis by tightening the machine screw at the top and bottom of the board.

9. Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the XVME-675 board as follows: VGA cable—VGA, keyboard—KeyBD, serial devices—COM1 and COM2, and parallel device—LPT1. Refer to Figure 2-2 for locations of these connectors.

Assuming the steps in the previous sections of this chapter have been followed, turn on the power to the VMEbus card cage.

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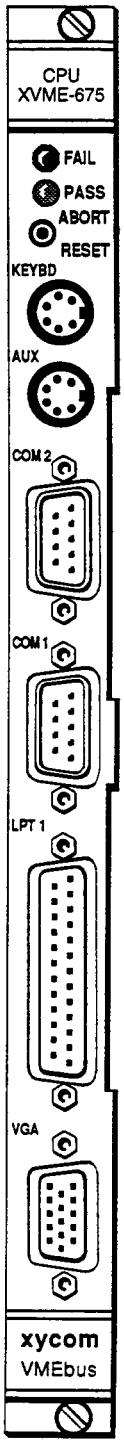


Figure 2-2. XVME-675 Board Front Panel

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2.6 ADDING EXTENDED BIOS

The XVME-675 has one 256Kx8 EPROM that can represent the entire IBM BIOS range. In Figure 2-3, the device address is the physical address which is viewed from an EPROM programmer, such as a data I/O. The system address is the address at which the code appears when plugged into the EPROM site on the XVME-675, as addressed by the 80486 processor.

A diagram of the XVME-675 and EPROM programmer addresses is shown below:

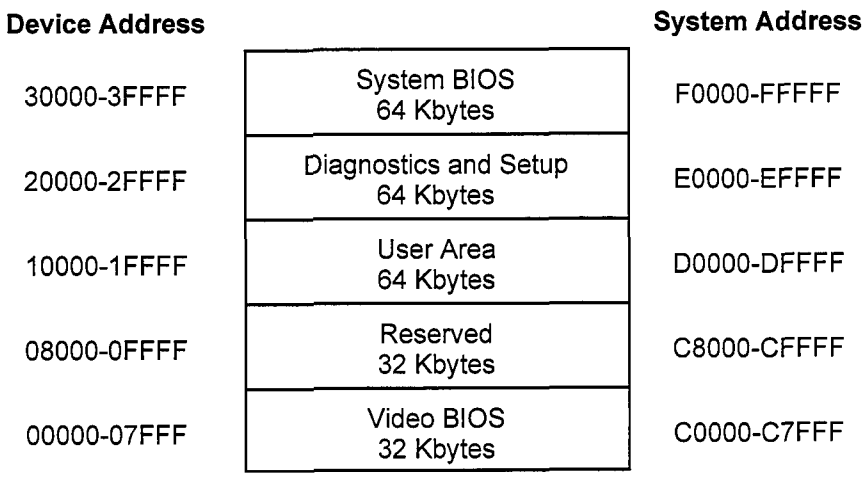


Figure 2-3. EPROM Programmer Addresses

Adding on-board extended BIOS to the XVME-675 involves two major steps: programming the EPROM and enabling the proper BIOS area in the Extended BIOS Setup Menu.

2.6.1 Programming the EPROM

Before beginning, make sure your EPROM programmer supports 2-Mbit devices.

1. Remove the 32-pin EPROM from socket U8.

2. Place the EPROM into the EPROM programmer's socket.

3. Load the EPROM into the RAM of the programmer. Set the starting address at 0h.

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4. Remove the EPROM from the socket.

> **NOTE**
> At this point, the data should be stored to a disk to protect the information in case of an error in programming.

5. Use a UV light to erase the EPROM.

6. Place the BIOS code into RAM, starting at location 10000h. The code should not exceed 64 Kbytes.

7. Reburn the EPROM with the new code. This places the new extended BIOS in the D000:0000-D0000-DFFFF block.

8. Place the EPROM back into socket U8 on the XVME-675.

2.6.2 Enabling the new BIOS code

1. Power up the XVME-675. After the memory tests and before your system loads the operating system, press `[Ctrl+Alt+S]` to enter the Extended BIOS Setup Menu.

2. Enable the on-board extended BIOS from D0000-DFFFF. Be sure the on-board extended BIOS for E0000-EFFFF is disabled.

3. Select `[F10]` to save the configuration, and then press `[Esc]` to exit the menu.

The procedure is now complete.

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3.1 BIOS OVERVIEW

The XVME-675 is an Intel 80486DX4™ - based PC/AT-compatible VMEbus processor. A custom BIOS has been developed for this processor board so it can surpass the functionality provided for normal PC/ATs. The custom BIOS allows users to access the value-added features present on the XVME-675 module without accessing the hardware directly.

The XVME-675 BIOS is a Quadtel 80486 BIOS with Xycom extensions. These extensions are

- ROM DOS (Solid State Disk) support
- Menus for configuring Xycom value-added features
- XVME BIOS functions for access to Xycom's value-added features

General instructions for navigating through the screens are described below:

- Arrow keys move the cursor up, down, left, and right. Press `[Enter]` to validate your selection.
- `[Esc]` exits the menu. You are prompted to save any changes.
- `[F5]` selects the previous or smaller value.
- `[F6]` selects the next or higher value.
- `[F9]` automatically configures the system with the default values. These default values are defined by the system configuration and the values set in the Setup Menu.

> **NOTE**
> Disk drives must be configured manually.

- `[F10]` saves the current configuration. With the exception of time and date, the configuration is not saved until `[F10]` is pressed.

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3.2 BIOS MAIN SETUP MENU

The BIOS Main Setup Menu is presented as the top level in the BIOS setup menu structure. To access the Main Setup Menu, depicted below, press `[Ctrl+Alt+S]` after the BIOS has completed the RAM test and before your system loads the operating system.

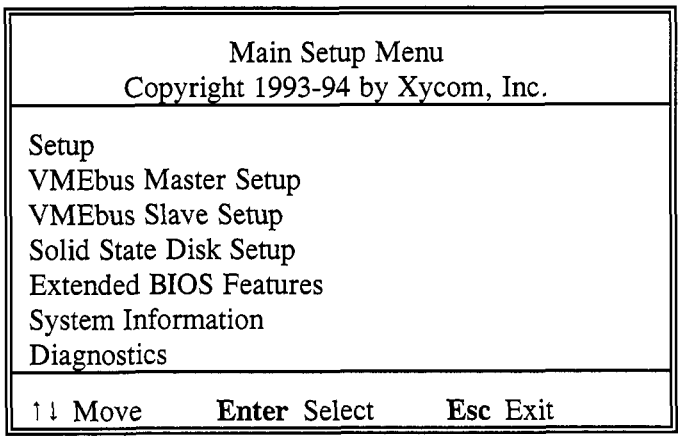


Figure 3-1. Main Setup Menu

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3.2.1 **Setup Menu**

On the Setup Menu, depicted in Figure 3-2 below, the time, date, and setup information contained in the CMOS RAM can be changed. This information is used by the System BIOS for system configuration.

```
                Extended BIOS Setup - Copyright 1989-91 Quadtel Corporation

Current Date:          [01/01/1988]      Video System:          [EGA / VGA  ]
Current Time:          [00:00:00]        Power-up Speed:        Normal

[     640]K  System Memory               BIOS Shadow:           [System in RAM]
[   15360]K  Extended Memory                                    [Video in RAM]
[      96]K  Shadow Memory               Wait States:           0,  All banks

Internal COM A:        [COM1,  3F8H]     Internal Floppy:       [Enabled    ]
Internal COM B:        [COM2,  2F8H]     Internal IDE:          [Enabled    ]
Internal LPT:          [LPT1,   378H]    Setup Prompt:          [Enable     ]

Diskette Drive 0:      [1.44 MB, 3 1/2]  System Memory Cache:   [On  ]
Diskette Drive 1:      [Not Installed  ]

Fixed Disk 0:  Type:[None]
Fixed Disk 1:  Type:[None]

←↑↓→  Move          F5  Previous Value     F9  Automatic Configuration
F1    Help          F6  Next Value         F10 Save Configuration
Esc   Exit
```

Figure 3-2. Setup Menu

Each of the options on the Setup Menu are described on the next few pages. Default items are underlined.

3.2.1.1 **Date** (<u>01/01/1988</u> format)

The date entry sets the real time clock for the month, day, and year. The left and right arrow keys and the enter key are used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.

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3.2.1.2 **Time** (00:00:00 format)

The time entry sets the real time clock for hours, minutes, and seconds. During the power-up sequence, time is read from the real time clock and saved in the BIOS system time.

The hour is calculated according to a 24-hour military clock, i.e., 00:00:00 through 23:59:59. The left and right arrow keys and the enter key are used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.

3.2.1.3 **Setup RAM Configuration**

The RAM on the XVME-675 can be partitioned or allocated between system memory, extended memory, and shadow memory. The `[F9]` key is used to automatically resize memory and select default memory values. The default memory configuration is 640 Kbytes system memory, 96 Kbytes shadow memory, and 15360 Kbytes or 31744 Kbytes of extended memory, depending on the XVME-675 version.

3.2.1.4 **System Memory**

This option should always indicate the size of conventional system memory as 640 Kbytes.

3.2.1.5 **Extended Memory**

This option sets the amount of extended memory in Kbyte increments. The maximum amount of extended memory is 31 Mbytes (31744 Kbytes).

3.2.1.6 **Shadow Memory**

This field displays the amount of shadow memory in use. The contents of this field are controlled by BIOS shadow selection. Shadow memory is used to copy the system and/or video BIOS into RAM to improve performance. The XVME-675 allocates for shadow RAM in Kbytes, and this number will be displayed on the menu. This field, which cannot be edited, is controlled by the BIOS shadow selections (Section 3.2.1.13). It is for reference only.

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The default shipping configuration for the XVME-675 will have the system BIOS and the video BIOS shadowed. Shadowing the BIOS increases system performance.

> **NOTE**
> Shadow RAM is always allocated for BIOS shadow only. Disabling the BIOS shadow option will not increase the amount of system memory.

3.2.1.7 **Internal Floppy and IDE** (Disabled/Enabled)

These selections enable or disable the internal floppy and IDE hard disk drive controllers.

3.2.1.8 **Setup Prompt** (Disabled/Enabled)

When this selection is enabled, the following prompt appears when you boot your system:

```
Press <Ctrl><Alt><S> to enter setup...
```

If you select disable, no prompt will appear, but you will still be able to enter the BIOS Setup Menus by pressing `<Ctrl><Alt><S>`.

3.2.1.9 **Diskette Drives 0 and 1**

Diskette Drive 0 (none/1.44MB, 3½"/360KB, 5¼"/1.2MB, 5¼"/720KB, 3½")
Diskette Drive 1 (none/1.44MB, 3½"/360KB, 5¼"/1.2MB, 5¼"/720KB, 3½")

These fields are used to specify the types of floppy disk drives connected to the PC/AT.

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3.2.1.10 **Fixed Disk Drives 0 and 1**

Fixed Disk 0 (none/1-14/16-45/User)
Fixed Disk 1 (none/1-14/16-45/User)

This selection individually configures the disk drives as one of 45 drive types, a user-defined type, or not installed. All 45 drive types are displayed on the screen if `[F1]` is pressed. If the type "User" is selected, several fixed disk parameters must be specified: number of cylinders (CY), heads (HD), sectors per track (ST), landing zone cylinder (LZ), and write precompensation (WP). Consult your fixed disk drive manual for information on these parameters.

3.2.1.11 **Video System**

There are four video adapter choices:

- EGA/VGA (Enhanced Graphics Adapter, Video Graphics Array, or any special video adapter)
- 40 Color (Color Adapter, power up in 40 column mode)
- 80 Color (Color Adapter, power up in 80 column mode)
- Monochrome Adapter

This field should not be changed from EGA/VGA, its default. This allows video functions to be controlled by the video BIOS rather than the system BIOS.

3.2.1.12 **Power-Up Speed**

This field is display only and always reads normal.

3.2.1.13 **BIOS Shadow** (System in RAM/ROM, Video in RAM/ROM)

The system BIOS and the VGA BIOS may be shadowed into DRAM to increase system performance. Shadowing is the process of loading the BIOS from EPROM into DRAM after power up. Since the DRAM bus width is 32 bits and the EPROM is only eight bits, opcode fetches from the DRAM significantly increase system performance. In addition to shadowing, the VGA BIOS is also cached. System BIOS occupies one eight-bit EPROM. If shadow DRAM is used, the BIOS is copied into DRAM and executed. This substantially increases BIOS execution speed.

3.2.1.14 **Wait States**

This indicates the number of wait states for memory controlled by the chipset. This setting is always zero for all banks.

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3.2.1.15 **Internal COM A and COM B**

These selections individually set the port address that will be programmed by the BIOS for each port. Each port offers three options:

- COM A (Off/COM1, 3F8/COM3, 3E8)
- COM B (Off/COM2, 2F8/COM4, 2E8)

> **NOTE**
> It is recommended that automatic configuration be used to select the COM and LPT ports. Automatic configuration selects the first logical port address that does not conflict with any other communication ports in your system. If the addresses are selected manually, conflicts with other devices in the system may occur.

3.2.1.16 **Internal LPT** (off/LPT1, 378h/LPT1, 278h/LPT1, 3BCh)

This item selects the port address to be programmed by the BIOS for the internal LPT port. There are four options:

- Off
- LPT1 at 378h
- LPT1 at 278h
- LPT1 at 3BCh

3.2.1.17 **System Memory Cache** (Off/On)

The system memory cache option—which refers to the 16 Kbyte internal cache on the 80486DX4—can be enabled or disabled by changing the field to On or Off. If the cache is disabled (Off), the XVME-675 will take longer to perform memory accesses, thereby degrading system performance.

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3.2.2 VMEbus Master Setup Menu

The VMEbus Master Setup Menu, depicted in Figure 3-3 below, allows configuration of the XVME-675 VMEbus master interface, auxiliary non-maskable interrupts (ANMIs), auxiliary maskable interrupts (AMIs), and the VMEbus interrupt handler.

```
                VMEbus Master Setup - Copyright 1993-94 by Xycom, Incorporated

VMEbus Master Configuration:                    System Resources          Disabled
Master Interface          [Disabled]            VMEbus Request Level      [3]
Master Byte Swapping      [Enabled]             VMEbus BERR Timeout
Master Access Mode        [Non-Privileged]      VMEbus Release            [16 µs]

Auxiliary NMI Configuration:                    VMEbus BERR               [Disabled]
Abort Push Button         [Disabled]            VMEbus SYSFAIL            [Disabled]
                                                VMEbus ACFAIL             [Disabled]

VMEbus Interrupt Handler Configuration:   L1 [Disabled]          L2 [Disabled]
 L3 [Disabled]   L4 [Disabled]      L5 [Disabled]   L6 [Disabled]   L7 [Disabled]

XVME Register Access via I/O Ports 330H through 33F:                [Disabled]

←↑↓→ Move              F5  Previous Value          F10 Save Configuration
F6   Next Value        Esc Exit
```

Figure 3-3. VMEbus Master Setup Menu

3.2.2.1 **Master Interface** (Disabled/Enabled)

Select Enable for the system to power up with the VMEbus master interface enabled. If disabled, the XVME-675 cannot access VMEbus memory or perform VMEbus interrupt acknowledge (IACK) cycles.

3.2.2.2 **Master Byte Swapping** (Disabled/Enabled)

This feature enables or disables byte swapping for VMEbus master cycles. When enabled, the master swaps the byte orientation of the data before sending it to the VMEbus. When disabled, the master passes the data straight through to the VMEbus. For example, if this feature is enabled, the master swaps data from little endian byte order (used by Intel processors) to big endian byte order (used by Motorola processors) before sending it to the VMEbus.

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3.2.2.3 **Master Access Mode** (Non-privileged/Supervisory)

This option allows the choice of Non-privileged or Supervisory accesses for VMEbus master cycles. This selection controls the AM2 signal on the VMEbus when the XVME-675 performs VMEbus accesses.

3.2.2.4 **System Resources** (Display Only)

This option displays the state of the SYSRES switch, which determines if the VMEbus system resources will be provided by the XVME-675 or another VMEbus processor. The system resources are VMEbus Arbiter, BERR timeout, SYSCLK, and IACK daisy chain driver. These resources must be provided by the module installed in the left-most slot of the VMEbus.

3.2.2.5 **VMEbus Request Level** (0/1/2/3)

This feature sets which bus request level (0, 1, 2, 3) will be used by the XVME-675 when requesting use of the VMEbus. If the XVME-675 is providing the system resources, this option is automatically set to 3.

3.2.2.6 **VMEbus BERR Timeout** (8/16/32/64 μs)

This selection will determine the length of the VMEbus timeout from among the following choices: 8, 16, 32, or 64 μs. The default is 16 μs. This option is unavailable if XVME-675 system resources are disabled.

3.2.2.7 **Auxiliary Non-maskable Interrupts and Auxiliary Maskable Interrupts Configuration**

The XVME-675 has both individual and group enable bits for the auxiliary non-maskable interrupts (ANMIs) and auxiliary maskable interrupts (AMIs). Individual ANMI and AMI bits are configured by the VMEbus Master Menu, but the group enable bits are left disabled and must be enabled by software (via XVME BIOS functions 21h and 51h) before the actual interrupts can be processed. This is because non-maskable interrupt (NMI) and/or IRQ10 handlers must be provided by a user application or the operating system, not by the BIOS.

The VMEbus BERR ANMI is a special case. It behaves like the other XVME ANMIs when the XVME ANMI groups is enabled on IRQ10. When the VME ANMI group is enabled on NMI, the VMEbus BERR ANMI comes in on the I/O channel check NMI.

The software watchdog timer enable bit is not offered in the BIOS setup menus because the ANMI group enable bit does not apply to the software watchdog timer (i.e., it becomes active as soon as it is enabled). The software watchdog timer ANMI comes in on the 486 NMI regardless of how the ANMI group is configured.

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These options are used to define which of the following ANMIs are enabled at power up:

- ABORT Switch
- VMEbus BERR
- VMEbus SYSFAIL
- VMEbus ACFAIL

Each ANMI can be enabled or disabled. All are disabled by default.

> **NOTE**
> To enable XVME ANMIS and AMIs, you must enable the XVME ANMI and AMI groups in addition to enabling the individual enable bits. See XVME-BIOS functions 23h (Enable/Disable Specific XVME ANMI Interrupts) and 51h (Set VMEbus Interrupt Group Configuration) in Chapter 5.

3.2.2.8 **VMEbus Interrupt Handler Configuration**

This option determines which VMEbus-level AMIs can be handled by the XVME-675. Each of the interrupt levels (1-7) can be enabled or disabled. All are disabled by default.

3.2.2.9 **XVME Register Access via I/O Ports 330H through 33FH** (Disabled, Enabled)

The VMEbus control and status registers on the XVME-675 are always accessible via I/O ports 30h-30Fh. These registers can also be accessed via I/O ports 330h-33Fh when this feature is enabled.

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3.2.3 VMEbus Slave Setup Menu

The VMEbus Slave Setup Menu, depicted in Figure 3-4 below, is used to configure of the XVME-675 VMEbus slave interface.

VMEbus Slave Setup - Copyright 1993-94 by Xycom, Incorporated			
VMEbus Slave Options:		Total Memory Size	[4]MB
Slave Interface	[Disabled]	Slave Memory Size	[4]MB
Slave Byte Swapping	[Enabled]	Slave Address Space	[VMEbus Extended]
Slave Access Mode	[Data]	Slave Address	[AA4]00000H
	[Non-privileged]		
←↑↓→ Move	F5 Previous Value	F10 Save Configuration	
	F6 Next Value	Esc Exit	

Figure 3-4. VMEbus Slave Setup Menu

3.2.3.1 **Slave Interface** (Disabled/Enabled)

This field determines whether the VMEbus slave interface is enabled on power up. If the VMEbus slave interface is disabled, other VMEbus masters cannot access memory on the XVME-675.

3.2.3.2 **Slave Byte Swapping** (Disabled/Enabled)

This feature enables or disables byte swapping for VMEbus slave accesses to the XVME-675 dual-access RAM. When enabled, the slave swaps the byte orientation of the data it receives. When disabled, the slave accepts the data as received. For example, if this feature is enabled and data is sent in big endian byte order (used by Motorola processors), the slave swaps it to little endian byte order (used by Intel processors) before storing the data in dual-access RAM.

3.2.3.3 **Slave Access Mode** (Data/Program and Non-privileged/Supervisory)

This feature determines to which type of VMEbus slave accesses the XVME-675 dual-access DRAM responds. The first field determines whether the slave interface responds to Data accesses only, or to both Program and Data accesses. The second field determines whether the slave interface responds to Supervisory accesses only, or to both Supervisory and Non-privileged accesses.

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3.2.3.4 **Total Memory Size** (Display Only)

This field displays the amount of on-board memory detected by the BIOS. Values can be 16 or 32 Mbytes.

3.2.3.5 **Slave Memory Size** (4/16/32 MBytes)

This option determines the amount of dual-access memory (4, 16, or 32 Mbytes) that is available to external VMEbus masters when the Slave Address Space option is set to Extended. If the Slave Address Space option is set to Standard, the slave memory size is fixed at 4 Mbytes. The slave memory size cannot be more than the total memory size (see Section 3.2.3.4).

3.2.3.6 **Slave Address Space** (VMEbus Standard/Extended)

This option determines if external VMEbus masters access the XVME-675's dual-access memory via VMEbus Standard (A24) or VMEbus Extended (A32) addressing.

3.2.3.7 **Slave Address** (AA400000H)

This option sets the VMEbus address of the XVME-675 dual-access RAM. When the Slave Address Space option is set to VMEbus Standard (A24), the dual-access memory must be located on a 4 Mbyte boundary and the upper two hex digits of the slave address are ignored. When the Slave Address Space option is set to VMEbus Extended (A32), the slave address must be a multiple of the slave memory size.

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3.2.4 Solid State Disk Setup

The Solid State Disk Setup Menu, depicted in Figure 3-5 below, configures the XVME-675 Solid State Disk (SSD) interface and the on-board extended BIOS areas.

Solid State Disk Setup - Copyright 1993-94 by Xycom, Incorporated			
Solid State Disk Options:		SSD Size	[128]KBytes
SSD Interface	[Disabled]	SSD Address	[000]00000H
Boot from SSD	[Disabled]	SSD Device Type	[RAM]
SSD Location	[VMEbus Standard]	XVME-956/101 Device Size	[1]Mbit
Onboard Extended BIOS Options:			
E0000-EFFFF	[Disabled]	D0000-D7FFF	[Disabled]
C8000-CFFF	[Disabled]	D8000-DFFF	[Disabled]
←↑↓→ Move	F5 Previous Value	F10 Save Configuration	
	F6 Next Value	Esc Exit	

Figure 3-5. Solid State Disk Setup Menu

3.2.4.1 **SSD Interface** (Disabled/Enabled)

When enabled, the SSD driver is initialized when the CPU is booted; if disabled, the SSD driver is not initialized.

3.2.4.2 **Boot from SSD** (Disabled/Enabled)

If enabled, the SSD is assigned the drive C designator and the system attempts to boot from drive C. If disabled, the SSD is assigned the drive D designator and the system does not attempt to boot from drive D. This option is only valid if the SSD Interface has been enabled.

3.2.4.3 **SSD Location** (VMEbus Standard/VMEbus Extended/XVME-956/101)

There are three options:

VMEbus Standard	The SSD resides in VMEbus standard memory (A24).
VMEbus Extended	The SSD resides in VMEbus extended memory (A32).
XVME-956/101	The SSD resides on the Xycom PC/104 Expansion Bus.

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3.2.4.4 **SSD Size** (128KBytes)

This defines the size of the SSD in 128 Kbyte increments, up to 32 Mbytes.

3.2.4.5 **SSD Address** (00000000H)

This indicates the starting address of the SSD in hexadecimal, on 1 Mbyte boundaries. The SSD Address is set to zero if the SSD Location is XVME-956/101. The upper two hexadecimal digits of the address cannot be configured if the SSD location is set to VMEbus Standard.

3.2.4.6 **SSD Device Type** (RAM/ROM/FLASH/EEPROM)

This specifies the device type used by the SSD. The EEPROM option is not implemented at this time.

3.2.4.7 **XVME-956 Device Size** (1/2/4 MBits)

This is necessary only if the SSD Location Field has been set to XVME-956/101. It specifies the size (1 Mbit, 2 Mbit, or 4 Mbit) of the devices used for the SSD.

3.2.4.8 **On-board Extended BIOS**

An extended BIOS may be on board or off board. The XVME-675 may contain on-board extended BIOS code in its ROM. An off-board extended BIOS may be located on a module installed in the on-board PC/104 site. During power up, the XVME-675 BIOS scans memory to locate any extended BIOS. The on-board extended BIOS setup options indicate where extended BIOS code is located. All extended BIOS areas are assumed to be off board by default. On-board extended BIOS areas must be enabled to function properly.

The D0000-DFFFF extended BIOS memory ranges are automatically disabled when Solid State Disk memory is set to XVME-956/101. The E000-EFFFh memory ranges are automatically disabled when Solid State Disk memory is set to VMEbus Standard or VMEbus Extended.

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3.2.5 **Extended BIOS Features Menu**

The Extended BIOS Features Menu is depicted below.

Extended BIOS Features - Copyright 1989-91, Quadtel Corp.			
Auto-park Disk: [No]		Keyboard Click:	[No]
Quick Boot: [No]		Keyboard Delay:	[3/4 Sec]
Screen Saver: [Disabled]		Keyboard Rate:	[22 / Sec]
		Numlock Boot State:	[Auto]
←↑↓→ Move	F5 Previous Value	F9	Auto Configuration
Esc Exit	F6 Next Value	F10	Save Configuration

Figure 3-6. Extended BIOS Features Menu

Each of the menu choices are described below.

3.2.5.1 **Auto Park Disk** (No/Yes)

This selection determines whether the system BIOS automatically parks the fixed disk drive. If this option is enabled, the system BIOS parks the fixed disk drive(s) heads after several seconds of inactivity. Most modern hard disk drives have self-parking heads, so enabling this option may not be necessary.

CAUTION

This feature can be incompatible with fixed disk drives that are not BIOS compatible and could cause problems with programs that do not utilize the BIOS for fixed disk I/O.

NOTE

Parking the heads causes some drives to spin down so that they do not respond to accesses quickly enough and display the message: "Not ready reading drive C. Abort, Retry, Fail?"

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3.2.5.2 **Quick Boot** (No/Yes)

When Quick Boot is selected, system BIOS bypasses floppy disk drive tests, memory tests, and floppy disk drive boot on power up or soft reset. The system initializes and boots from the fixed disk in a few seconds.

> **CAUTION**
> During hard disk partitioning and formatting, the quick boot selection must be set to No. Otherwise, an operating system missing error is displayed, and the system does not boot.

> **NOTE**
> If yes is the option selected, memory is not tested and the floppy disk drive(s) defined in the Setup Menu must be correct. **Also, the system will not boot from drive A.**

3.2.5.3 **Screen Saver** (Disabled/10 min/30 min/1 hour)

This option allows blanking the screen after a specified period of keyboard inactivity. This ensures that the data displayed does not permanently burn into the monitor. Blanking can be set to occur after 10 minutes, 30 minutes, or one hour, or this option can be disabled. Press any key to redisplay the screen after the screen saver has been activated.

> **CAUTION**
> Do not enable the screen saver when running programs that do not use the BIOS for keyboard handling, such as Microsoft Windows. If the screen saver is enabled with these programs, the screen blanks after the specified time, regardless of activity, and can only be restored by exiting the program.

3.2.5.4 **Keyboard Click** (No/Yes)

If enabled, this function provides audible key press feedback by causing the BIOS to click through the system speaker every time a key is pressed. This option is only valid for systems with a speaker connected to the speaker jack (J11).

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3.2.5.5 **Keyboard Delay** (1/2/3/4 quarters of a second)

This sets the amount of time that elapses after a key is pressed before the key starts to repeat. The smaller the time selected, the sooner the key starts to repeat.

3.2.5.6 **Keyboard Rate** (2/6/10/13/18/22/27/30 per second)

This option defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats.

3.2.5.7 **Numlock Boot State** (Auto/On/Off)

This option determines how the BIOS defines the Numlock key at power up or soft reset. Normally, the BIOS sets the Numlock (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If an 84-key keyboard is detected, Numlock is turned off (cursor keys selected). Select Auto to keep this state; On to select the numeric keys, regardless of keyboard; or Off to select the cursor keys, regardless of keyboard.

3.2.6 **System Information Menu**

The System Information Menu, depicted in Figure 3-7 below, provides the following information:

System Information - Copyright 1989-91 by Xycom, Incorporated

Processor:	486DX4	LPT1 Address:	0378H
Coprocessor:	Internal	LPT2 Address:	Unused
		LPT3 Address:	Unused
BIOS ID:	352080004		
BIOS Revision:	03.06.01	COM1 Address:	03F8H
		COM2 Address:	02F8H
Programmable Memory:	16384K	COM3 Address:	Unused
Other Memory:	0K	COM4 Address:	Unused
		Internal Mouse:	No

Press <any key> to exit.

Figure 3-7. System Information Menu

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The System Information Menu states the type of processor and math co-processor used and the port addresses. The BIOS ID and revision identify the BIOS and may vary. Programmable memory is controlled by the BIOS. Other memory includes AT-bus memory that is annexed as system memory. (This memory could be from a PC/104 expansion card.)

3.2.7 **Diagnostics Menu**

The Advanced Diagnostics Software System is a collection of utility programs that provide advanced tests for PC/AT-compatible systems. This section contains information on using the Advanced Diagnostics Software System on the XVME-675. All pertinent menu instructions are included.

The Diagnostics Menu offers the following choices: Park Fixed Disks, Diagnostics, and Format Fixed Disk. Each of the choices is explained in the following sections.

3.2.7.1 **Park Fixed Disks**

This menu selection parks the fixed disk drive(s) by placing the fixed heads over the diagnostic cylinder so vibration does not damage the usable media. This operation should be performed before transporting the system.

3.2.7.2 **Diagnostics**

When Diagnostics is selected from the Main Menu, a warning message is displayed. It states that running the utility can cause problems with other running software. You are also told to do the following:

- Reboot your system after running diagnostics.
- Format your floppy disks using DOS after exiting the utility.
- Insert scratch diskettes into all drives.

After reading the warning and inserting the disks, press (N) to abort the operation or (Y) to continue.

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If you select (Y), the Advanced Diagnostics Menu appears. It is shown in Figure 3-8 below.

Advanced Diagnostics V1.04A, Copyright 1989, 1990 Quadtel Corporation

Continuous: **[No]** Stop on error: **[Yes]** Echo log to LPT1: **[No]**

[P]	System Board	**[N]**	Monochrome Adapter
[84]	Keyboard	**[N]**	Color Graphics Adapter
[640K]	System Memory	**[N]**	Enhanced Graphics Adapter
[15360K]	Extended Memory	**[P]**	Video Graphics Array
		[N]	Monochrome Parallel
[1.2 MB]	Diskette Drive 0	**[P]**	Primary Parallel
[360 KB]	Diskette Drive 1	**[P]**	Secondary Parallel
[P]	Fixed Disk 0	**[P]**	Primary Serial
[N]	Fixed Disk 1	**[P]**	Secondary Serial

↑↓	Move	F5	Previous Value	F9	Test Present Devices
F1	Help	F6	Next Value	F10	Test Selected Devices
Esc	Exit				

Figure 3-8. Advanced Diagnostics Menu

Items that appear in **bold** in the menus indicate fields that users can change. Default settings initially appear on the screen.

Each of the selections on the menu indicate the hardware item to test and the configuration of that item. Some items are present (P) or not present (N), while others specify a hardware type. For example, Keyboard can be an 84-key keyboard, a 101-key keyboard, or not present.

The selections shown in the menu are detected by the diagnostics system. General instructions for navigating through these menus are described below:

- Arrow keys move the cursor up, down, left, and right. Use these keys to select items to change to override the automatic selection process or to exclude certain tests from being performed.
- `[Enter]` validates your selection.
- `[Esc]` exits the menu. You are prompted to save any changes.
- `[F5]` selects the previous or smaller value.
- `[F6]` selects the next or higher value.

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- `[F9]` tests all currently available items. Set these selections to not present (N) if there are specific tests that you do not want to perform.
- `[F10]` is used to select a specific test. Move the cursor to the specificed test and press [F10]. The selection to test cannot be set to N or None.

Each of the tests selected from the Diagnostics Menu is described below.

When a test is initiated, a window like the one shown in Figure 3-9 is displayed. The information shown depends on the type of test selected.

```
        Advanced Diagnostics  Copyright 1989, 1990 Quadtel Corporation

 Continuous: No      Stop on error: Yes          Echo log to LPT1: No
                     Press <ESC> to abort current test.

Testing: Primary Async                          Test Results:

External Loopback ...          None
Modem control lines... Passed
Baud rate clock (110 baud)...  Testing
```

Figure 3-9. Advanced Diagnostics Test Menu

The left side of the screen shows information relating to the test(s) being performed; the right side shows results of completed tests.

CAUTION

Tests that are labeled destructive could destroy information. Use caution when testing floppy and hard disks.

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3.2.7.3 Test Control Options

The fields at the top of the screen are options that control how the tests are performed. These options must be set before a test or tests are initiated.

Continuous Test Set to Yes or No. When set to Yes, the test is performed continuously until you stop it by pressing [Esc]. After pressing [Esc], press the space bar to continue or press [Esc] to abort the test(s). Continuous test works with a single test (selected by [F10]) or several tests (selected by [F9]).

Stop on Error Set to Yes or No. When set to Tes, the diagnostic system stops after detecting an error. After the system reports the error, press the space bar to continue or [Esc] to end testing.

Echo to LPT1 Set to Yes or No. If set to Yes, the test result data is written to a printer attached to LPT1. This feature is useful if you set Continuous Test to Yes, Stop on Error to No, and run the test(s) unattended.

> **NOTE**
> Some of the submenu tests require you to respond to prompts. These are identified as interactive. If you are performing continuous unattended tests, do not select interactive tests.

3.2.7.4 System Board

This selection tests the processor, DMA registers, CMOS RAM, real time clock, timers, and interrupt controller. After the tests are completed, press [Esc] to Return to the Diagnostics Menu or the space bar to run the tests again.

3.2.7.5 Keyboard

After Keyboard test is selected, a menu appears that allows the keyboard and controller tests to be enabled or disabled. [F7] selects all tests; [F8] sets all tests to No.

After pressing [F10] to accept the selections, a keyboard map appears that is appropriate to the type of keyboard specified under Diagnostics Keyboard. Press [Ctrl+Y] if all keys are working correctly or [Ctrl+N] if there are keys that do not work.

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3.2.7.6 **System Memory**

This diagnostic tests the amount of read/write system memory.

3.2.7.7 **Extended Memory**

This diagnostic tests the amount of extended system memory. Separate tests for read/write and address lines are performed.

3.2.7.8 **Diskette Drives 0 and 1**

Choosing to test the diskette drives brings up a submenu that requests the drive to test. Certain test features can be set to Yes or No. The test will seek tracks, verify tracks, change the disk, and perform a read/write and format. The disk change is interactive, and read/write and format are destructive.

`[F7]` selects all tests; `[F8]` sets all tests to No.

Select test for diskette drive **A:**					
Seek tracks	**[Yes]**				
Verify tracks	**[Yes]**				
Disk change (interactive)	**[No]**				
Read / Write (destructive)	**[Yes]**				
Format (destructive)	**[Yes]**				
↑↓ Move		F5	Toggle	F7	All
F1 Help		F8	None		
Esc Abort		F10	Accept		

Figure 3-10. Diskette Drive Menu

3.2.7.9 **Fixed Disk Drives 0 and 1**

This selection brings up a menu that enables or disables controller, head select, and seek tests. The drive designation for the drive to be tested must be entered as 0 or 1.

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[F7] selects all tests; [F8] sets all tests to No.

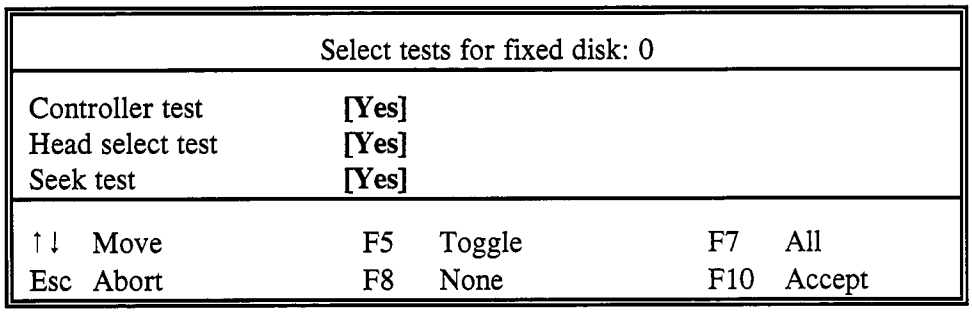


Figure 3-11. Fixed Disk Menu

CAUTION
Tests that are labeled destructive could destroy information. Use caution when testing floppy and hard disks.

3.2.7.10 **Monitor Type**

Set your monitor type to P and the other monitor types to N. Available selections are

- Monochrome Adapter (MDA)
- Color Graphics Adapter (CGA)
- Enhanced Graphics Adapter (EGA)
- Video Graphics Array (VGA)

If the video controller on the XVME-675 has not been disabled, select the VGA option.

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3.2.7.11 **Parallel Port Tests**

Set the primary, secondary, and monochrome parallel ports to (P) if present or (N) if not present in your system. When a parallel port test is selected, a menu similar to the one below appears:

Select Tests for Parallel					
Internal Loopback	**[Yes]**				
Printed Pattern (requires connected printer)	**[No]**				
External Loopback (requires loopback connector)	**[No]**				
↑↓ Move		F5	Toggle	F7	All
Esc Abort		F8	None	F10	Accept

Figure 3-12. Parallel Port Test Menu

The port(s) selected are tested for external loopback, internal loopback, and printer pattern.

If performing a parallel loopback test, there must be a loopback connector on the parallel port. The pinouts for this connector are shown in Figure 3-13, on the following page

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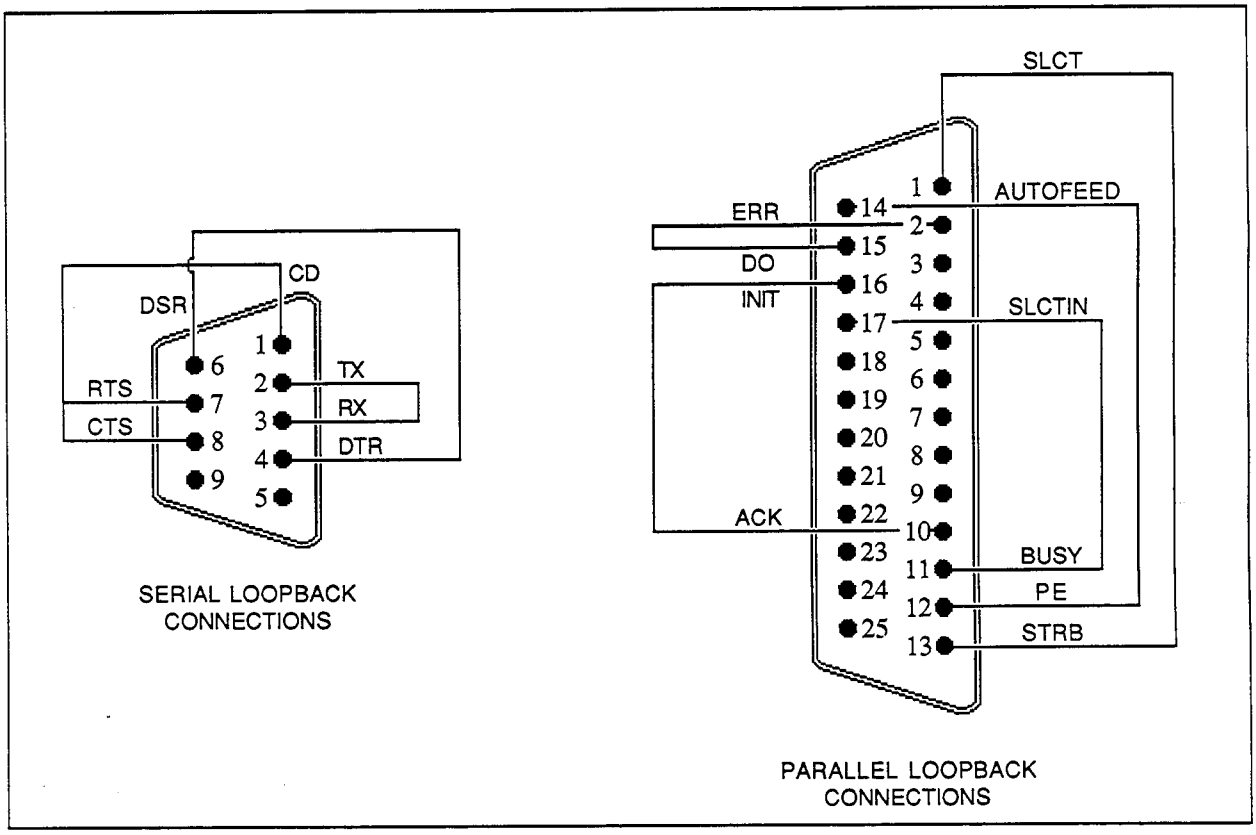


Figure 3-13. Serial and Parallel Loopback Connections

3.2.7.12 **Serial Port Tests**

Set the primary and secondary serial ports to (P) if present or (N) if not present in your system. A menu appears when you select the port(s) to test. Baud rate clock, internal transfer and receive data lines, and modem control data lines can be tested. A loopback connector is required to execute the external loopback test. Refer to Figure 3-13 above for the Serial and Parallel Loopback Connections diagram.

3.2.8 **Format Fixed Disk**

Select Format Fixed Disk from the Main Menu to format your fixed disk drive(s). A menu prompts you for which fixed disk (0 or 1) you wish to format. Use the arrow keys to select the disk and press `[Enter]`. A warning is displayed stating that this operation will destroy all data on the selected hard drive. You are prompted to continue. If you select (Y), the Format Fixed Disk Menu appears (shown in Figure 3-14 on the following page).

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Format Fixed Disk v1.02				
Drive: 0 Heads: 8 Cylinders: 1024				
Cyl Hd	Cyl Hd	Cyl Hd	Cyl Hd	Cyl Hd
Interlv: **[03]** Insert: Cyl [0] HD [0] Bad: 0				
↑↓ Move	Ins/Del	Bad Track	F5	Scan bad tracks
	F2	Clear Table	F6	Analyze Surface
	F3	Print Table	F7	Format Unformatted
Esc Escape	F4	Set Interleave	F8	Format Preformatted

Figure 3-14. Format Fixed Disk Menu

CAUTION
Most IDE drives should not be low-level formatted. Check your IDE drive manual for formatting procedures.

3.2.8.1 Using the Bad Track Table

Bad tracks are areas of the fixed disk that cannot properly store data. Bad tracks are displayed in the center of the menu. Use [F5], [F6], or [F8] to update this list.

To add a bad track manually, press [Insert] and use the arrow keys or [Enter] to select the cylinder and head fields. Enter the appropriate information and press [F10] or [Enter]. You are alerted if you enter an invalid head or cylinder. Use the arrow keys to position the cursor, press [Delete], then enter the new information.

To clear the entire bad track table, press [F2]. To print the table, press [F3]. If the drive has already been formatted, press [F5] to search for existing bad tracks.

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3.2.8.2 Setting the Interleave

The interleave is the value used by the format operation to interleave the fixed disk tracks. Press `[F4]` to set the interleave. Consult your disk drive manual to set the proper interleave.

> **NOTE**
> The interleave specified is the value which will be used to format, which is not necessarily the current value for your fixed disk.

If you do not set the interleave, a default of three is used.

3.2.8.3 Analyzing the Fixed Disk Surface

If you do not need to reformat the entire fixed disk, but want to perform a thorough media test to detect any bad or marginal areas, select `[F6]` to analyze the surface.

> **CAUTION**
> Analyzing the surface causes all data on the disk to be lost.

Any bad tracks found in the analysis are automatically added to the bad track table. As they are located, the bad tracks are reformatted as bad to prevent these areas from being used.

3.2.8.4 Formatting a New Fixed Disk Drive

Formatting the disk sets bad tracks with a special attribute so other programs (like DOS FORMAT) do not attempt to use these areas.

After installing a new fixed disk drive, enter the bad track information provided by the manufacturer into the bad track table. Next, press `[F7]` to begin formatting. The following operations are performed:

- Each track of the fixed disk is formatted using the current interleave.
- Each bad track is reformatted as bad so that it cannot be used.

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3.2.8.5 Formatting an Already Formatted Disk

If the fixed disk was previously formatted, select `[F8]` to begin formatting. The following operations are performed:

- The drive is scanned for bad tracks, which are added to the bad track table.
- Each track is reformatted using the current interleave.
- Each bad track is reformatted as bad so it cannot be used.
- A surface analysis is performed on the media and any additional bad tracks found are reformatted as bad and added to the bad track table.

3.2.8.6 Finishing the Formatting

The Fixed Disk Format commands perform low-level format operations on the fixed disk drive(s). After the format is complete, run the DOS FDISK command followed by DOS FORMAT to prepare the media for use under DOS (or the corresponding utilities for another operating system). Refer to the operating system manual for more information.

3.2.8.7 Error Codes

When the diagnostics system detects an error, a two-byte hexadecimal code is displayed. The first byte of this code is the class of error and the second byte is the subclass. The error code class generally corresponds to a specific hardware system or group of systems. For example, the first class (01) is used for the system board, so error 0108 indicates a system board error regarding the 8253 counters.

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Table 3-1. Error Codes

Code	Class	Failure Type
0101	System board	DMA registers
0102		DMA memory move
0103		Interrupt mask
0104		Hot interrupt line
0105		Stuck NMI
0106		Process registers
0107		System timer
0108		8253 counters
0109		System timer interrupts (1)
010A		System timer interrupts (2)
010B		Processor flags
0110		CMOS memory
0111		Real time clock
0120		BIOS checksum
0701	Keyboard	Controller
0702		Keyboard map
1001	Co-processor	Registers
1002		Calculations
1701	Video	Text attributes
1702		Background colors
1703		Character set
1704		Text page registration
1705		Text pages
1706		Graphics display
1707		EGA/VGA palette
1708		Memory
1709		VGA sequencer
170A		VGA controller registers
170B		VGA attribute controller
170C		VGA DAC
1730		Cannot initialize video
2001	Serial	Baud rate clock
2002		Internal loopback data
2003		Internal loopback control
2004		External loopback data

Table continued on the following page.

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Table 3-1. Error Codes (*continued*)

Code	Class	Failure Description
2701	Parallel	Registers read/write
2702		Control loopback
2703		Printed pattern
2704		Printer not ready
2705		Unknown error
2706		No paper / paper jam
2707		Printer timeout
2708		Printer busy
3001	Memory	Address lines
3002		Data patterns
3003		Walking bits
3701	Disk	Invalid parameter
3702		Address mark not found
3703		Write protect error
3704		Sector not found
3705		Reset failed
3706		Change line active
3707		Drive parameter error
3708		DMA overrun
3709		Attempt to DMA across 64 K
370A		Bad sector flag found
370B		Bad cylinder detected
370C		Media type not found
370D		Invalid format sectors count
370E		Control data mark detected
3710		CRC or ECC error detected
3711		ECC corrected error
3720		General controller failure
3740		Seek operation
3750		Change line test
3780		Drive not ready
37BB		Undefined error occurred
37CC		Write fault on selected drive
37EO		Status error
37FF		Sense operation failed

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4.1 MEMORY MAPS

The XVME-675 has two different memory maps, one for each of the two possible local memory configurations. VMEbus extended memory begins at address 40000000h, regardless of the memory size. The XVME-675 memory maps are outlined in tables 4-1 and 4-2.

XVME BIOS functions 01h and 02h (see Chapter 5) can be used to get the physical segment of the Real Mode Window and the protected mode addresses of the VMEbus IACK, short, standard, and extended address spaces.

> **NOTE**
> The I/O Channel designation refers to memory viewed as part of the PC/104 Bus.

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Table 4-1. 16 Mbyte Memory Map

Address Range	**Size**	**Usage**
FE000000 - FFFFFFFF	32 Mbytes	System BIOS EPROM
FD000000 - FDFFFFFF	16 Mbytes	VME standard space
FC0x0000 - FCFxFFFF x = 1,3,5,7,9,B,D,F	8 Mbytes	VME short I/O space
FC0x0000 - FCFxFFFF x = 0,2,4,6,8,A,C,E	8 Mbytes	VME IACK space
40000000 - FBFFFFFF	3008 Mbytes	VME extended space
01000000 - 3FFFFFFF	1008 Mbytes	Reserved (shadow on 128 Mbytes)
00100000 - 00FFFFFF	15 Mbytes	Dual-access DRAM
000F0000 - 000FFFFF	64 Kbytes	System BIOS EPROM
000E0000 - 000EFFFF	64 Kbytes	Real Mode Window or Diagnostics and SETUP
000D8000 - 000DFFFF	32 Kbytes	I/O channel memory or on-board BIOS
000D0000 - 000D7FFF	32 Kbytes	I/O channel memory or on-board BIOS
000C8000 - 000CFFFF	32 Kbytes	I/O channel memory or on-board BIOS
000C0000 - 000C7FFF	32 Kbytes	Video BIOS
000A0000 - 000BFFFF	128 Kbytes	Video memory DRAM
00000000 - 0009FFFF	640 Kbytes	Dual-access DRAM

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Table 4-2. 32 Mbyte Memory Map

Address Range	**Size**	**Usage**
FE000000 - FFFFFFFF	32 Mbytes	System BIOS EPROM
FD000000 - FDFFFFFF	16 Mbytes	VME standard space
FC0x0000 - FCFxFFFF x = 1,3,5,7,9,B,D,F	8 Mbytes	VME short I/O space
FC0x0000 - FCFxFFFF x = 0,2,4,6,8,A,C,E	8 Mbytes	VME IACK space
40000000 - FBFFFFFF	3008 Mbytes	VME extended space
02000000 - 3FFFFFFF	992 Mbytes	Reserved (shadow on 128 Mbytes)
00100000 - 01FFFFFF	31 Mbytes	Dual-access DRAM
000F0000 - 000FFFFF	64 Kbytes	System BIOS EPROM
000E0000 - 000EFFFF	64 Kbytes	Real Mode Window or Diagnostics and SETUP
000D8000 - 000DFFFF	32 Kbytes	I/O channel memory or on-board BIOS
000D0000 - 000D7FFF	32 Kbytes	I/O channel memory or on-board BIOS
000C8000 - 000CFFFF	32 Kbytes	I/O channel memory or on-board BIOS
000C0000 - 000C7FFF	32 Kbytes	Video BIOS
000A0000 - 000BFFFF	128 Kbytes	Video memory DRAM
00000000 - 0009FFFF	640 Kbytes	Dual-access DRAM

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4.1.1 **Dual-access DRAM**

The actual amount of DRAM installed on the XVME-675 can be determined via XVME-BIOS function 05h (Get Memory Size) in Chapter 5.

The 16 Mbyte version has 15.64 Mbytes of dual-access DRAM divided into 640 Kbyte and 15 Mbyte blocks. The additional 384 Kbytes of DRAM is dedicated for shadow RAM and cannot be relocated.

The 32 Mbyte version has 31.64 Mbytes of dual-access DRAM divided into 640 Kbyte and 31 Mbyte blocks. The additional 384 Kbytes of DRAM is dedicated for shadow RAM and cannot be relocated.

For all versions, the VMEbus views the dual-access DRAM as a contiguous block of memory.

4.1.2 **EPROM**

The XVME-675 has only one EPROM on board. It is a 256 Kbyte device that can represent the entire ROM BIOS range. The memory map appears in Table 4-3.

Table 4-3. EPROM Memory Map

Device Address*	**System Address****	**Size**	**Description**
30000-3FFFF	F0000-FFFFF	64 Kbytes	System BIOS
20000-2FFFF	E0000-EFFFF	64 Kbytes	Diagnostics and Setup
10000-1FFFF	D0000-DFFFF	64 Kbytes	User
08000-0FFFF	C8000-CFFFF	32 Kbytes	Reserved
00000-07FFF	C0000-C7FFF	32 Kbytes	Video BIOS

* The Device Address is the physical address viewed from an EPROM programmer.

** The System Address is the address where the code appears when plugged into the EPROM site on the XVME-675.

To add an on-board extended BIOS, the 32-pin EPROM has to be removed from the socket and the new BIOS must be burned into the D0000-DFFFF block (10000-1FFFF). Users should then enter the Setup Menu to enable the appropriate BIOS range.

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4.2 I/O MAPS

The XVME-675 I/O maps contain the I/O ports of the IBM AT architecture with some additions. The XVME-675 I/O Map appears in Table 4-4.

Table 4-4. Input/Output Map

Hex Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller 1, 8259 equivalent
022-023	Not used by XVME-675
024&028	AT chipset register set up
025-02F	Interrupt controller 1, 8259 equivalent
030-03F	VME interface control and status registers
040-05F	Timer, 8254-2 equivalent
060-06F	8742 equivalent keyboard
070-07F	Real time clock
080-09F	DMA page register
0A0-0BF	Interrupt controller 2, 8259 equivalent
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0E0-0EF	Not used by XVME-675
0F0	Clear math co-processor interrupt
0F1	N/A
0F2-0FF	Math co-processor
100-1EF	Available
1F0-1F7	IDE controller (AT drive)
1F8-1FF	Not used by XVME-675
200-218	Available
219	BIOS ROM enable/ IO remap
21A-21F	Not used by XVME-675
220-277	Available
278-27F	Parallel port 2
280-2F7	Available
2F8-2FF	Serial port 2
300-32F	Available
330-33F	Not used by XVME-675
340-36F	Available
370-377	VME interface control and status registers (alternate)
378-37F	Parallel port 1
380-3Bf	Available
3C0-3CF	VGA/EGA
3D0-3EF	Available
3F0-3F7	Primary floppy disk controller
3F8-3FF	Serial port 1

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5.1 OVERVIEW

The XVME BIOS contains a series of functions that are accessible to user programs, to assist in configuring and using the VMEbus Interface Control and Status Registers. The Xycom BIOS Information Block (XBIB) provides the interface that is used to access these functions.

This chapter contains detailed information about XBIB and the XVME BIOS functions.

5.2 XYCOM BIOS INFORMATION BLOCK

The BIOS contains a Xycom BIOS Information Block. Embedded within the XBIB is information that can be used to make decisions or interface with the BIOS. The XBIB contains the following information:

Table 5-1. XBIB Structure

Field	**Description**
Xycom Signature	Identifies the BIOS as a Xycom product.
XVME Model	Identifies the model number of the XVME board.
Processor Speed	Indicates the processor speed of the XVME board. If the BIOS is speed independent, the processor speed is zero.
BIOS Revision Level	Identifies the revision level of the BIOS.
XVME Attributes	Indicates support provided by this BIOS.
Entry Points	Provides access to XVME BIOS functions.
Checksum	Allows for an integrity check on XBIB information.

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The XBIB is located by searching the BIOS segment (i.e., physical segment F000h) for the Xycom signature. Once located, XBIB information can be extracted and used. The assembly code fragment on the following pages illustrates one way to do this.

> **NOTE**
> The XBIB location code fragment assumes operation in 16-bit real mode. The 16-bit and 32-bit (flat and segmented) protect mode models require operating system details. In these environments, the 16-bit real mode code fragment can serve as an example.

```
        .data
XBIB    struc
        product         db      10      dup (?)
        speed           db      4       dup (?)
        revision        db      7       dup (?)
        xvmeattrib      db      2       dup (?)
        oifattrib       db      2       dup (?)
        unused          db      9       dup (?)
        Offset32        dw      ?
        Offset16        dw      ?
        Checksum        db      ?
ends

Signature               db              "XYCOMSIG",0
SignatureSize           equ             $-Signature
Info                    XBIB            ?

        .code
; This code assumes that DS has been loaded correctly and
; that the static entries in the data segment have been set
; up properly.
```

> **NOTE**
> Code fragment continues on the following page.

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```
        ; Search BIOS segment for Xycom signature
        mov         ax,0F000h               ; Move BIOS segment
        mov         es,ax                   ;   into ES
        xor         di,di                   ; Start at offset 0000h
SearchMore:
        mov         si,offset Signature     ; Start of signature string
        mov         cx,SignatureSize        ; Size of signature string
        rep         cmpsb                   ; Compare
        je          Found                   ; Exit if signature located ?
        and         di,0FFF0h               ; Set offset to next
        add         di,010h                 ;   paragraph boundary
        jc          Not_Found               ; Exit if outside BIOS segment
        jmp         short SearchMore        ; Try new offset

        ; Extract information from XBIB and verify XBIB checksum
Found:
        mov         ah,073h                 ; Start with checksum of XYCOMSIG
        mov         si,offset Info          ; Start at beginning of Info
        mov         cx,size XBIB            ; Size of XBIB
XBIBMore:
        mov         al,es:[di]              ; Get XBIB data byte
        add         ah,al                   ; Add to checksum
        mov         ds:[si],al              ; Save XBIB data byte
        inc         di                      ; Next XBIB
        inc         si                      ;   data byte
        loop        XBIBMore                ; More XBIB data ?
        or          ah,ah                   ; Verify checksum
        jnz         Error                   ; Exit if checksum is bad
        ...
        ; XBIB checksum failed
Error:
        ...
        ; Xycom signature not found !!!
Not_Found:
        ...
```


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5.3 XVME BIOS FUNCTIONS

XVME BIOS functions spare the user from having to directly access and manipulate the XVME registers, and provide a compatibility buffer in case future XVME PC/AT I/O register maps and bit definitions change. It is recommended that these functions, rather than direct access to I/O registers, be used.

The XVME BIOS functions can be accessed via INT 15h function AFh (i.e., AH = AFh). The individual function to be performed is identified by an eight-bit function number in AL. Function numbers indicate the group (most significant hex digit of the function number) and the index (least significant hex digit of the function number).

The following assembly code fragment shows how to use the interrupt 15h interface. Load AH with AFh and AL with the function number of the desired function. Load the other registers with input data as required by the function. Then generate the interrupt. Upon return from the interrupt, DI should be checked for an "XY" to ensure that an XVME BIOS function was performed. Register AX should also be checked to see if an error occurred. If DI contains an "XY," no error occurred (AX=0), then the output data is valid. See Section 5.13 for more information on XVME BIOS function error codes.

```
        ; Invoke XVME BIOS function using the int15 interface
        mov   ah,0AFh                       ; Indicate XVME BIOS function
        mov   al,<Fn#>                      ; Indicate which function
        <load other registers as needed>    ; Provide function inputs
        int   015h                          ; Invoke XVME BIOS function
        cmp   di,"XY"                       ; Exit if the XVME BIOS
        jne   unknown                       ;   function was not invoked
        or    ax,ax                         ; Check for
        jnz   error                         ;   an error
        <use output registers as needed>    ; Function outputs are valid
        ...

        ; Handle XVME BIOS function error
error:
        <error code in register ax>

        ; XVME BIOS function not performed
unknown:
        <XVME function not performed>
```


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In addition to the INT 15h interface, the Xycom BIOS Information Block includes offsets for 16-bit and 32-bit call entry points to the XVME BIOS functions. All call entry points use a register structure for input and output data. Before using a call entry, the AL field is filled with the function number of the desired function; other fields are filled with input data required by the desired function. When using the call entry, it is not necessary to load the AH field with AFh. Once filled, the register structure is used as one of the parameters in a C style call (i.e., address is pushed onto the stack) to the call entry point. Upon return from the XVME BIOS function, the AX field contains an error code which indicates the type of error or zero if no error occurred. If no error occurred, the other fields contain valid output data.

Table 5-2. XVME BIOS Function Call Interface Register Structure

Byte Offset	**Fields in Structure**	
00h	AX	
	AL	AH
02h	BX	
	BL	BH
04h	CX	
	CL	CH
06h	DX	
	DL	DH
08h	SI	
0Ah	DI	
0Ch	FLAGS	

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The following assembly code fragment shows how to declare the register structure defined in Table 5-2.

```
regstruc    struc
      union                              ; General purpose registers
            struc
                  _al   db    ?     ;   can
                  _ah   db    ?     ;   be
                  _bl   db    ?     ;   accessed
                  _bh   db    ?     ;   as
                  _cl   db    ?     ;   high
                  _ch   db    ?     ;   and
                  _dl   db    ?     ;   low
                  _dh   db    ?     ;   bytes
            ends
            struc
                  _ax   dw    ?     ;   or
                  _bx   dw    ?     ;   as
                  _cx   dw    ?     ;   single
                  _dx   dw    ?     ;   words
            ends
      ends
      _si         dw    ?
      _di         dw    ?
      _flags      dw    ?
ends
```


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The following assembly code fragment shows how to use the 16-bit call interface. Fill the register structure, push the segment and offset of the register structure onto the stack, and then make a far call to the 16-bit call entry offset indicated in the Xycom BIOS Information Block. Upon return, the AX field should be checked to see if an error occurred. If no error occurred (AX field=0), any other output fields are valid. See Section 5.13 for more information on XVME BIOS function error codes.

```
        .data
Call16_Far          label dword
Call16_Offset       dw    ?
Call16_Segment      dw    0F000h
Info                XBIB        <>
Regs                regstruc    <>

        .code
; This code assumes that DS has been previously loaded, that the static
; entries in the data segment have been set up properly, and that the
; XBIB information has been correctly extracted.

        ; Generate 16-bit far call entry pointer
        ; (this section need only be performed once)
        mov   ax,Info.Offset16              ; Get offset from XBIB
        mov   Call16_Offset,ax              ; Fill in pointer

        ; Invoke XVME BIOS function using the 16-bit far call entry
        mov   Regs._al,<Fn#>                ; Indicate XVME BIOS function
        <fill registers fields as needed>   ; Provide function inputs
        push  seg Regs                      ; Put far address of register
        push  offset Regs                   ; structure on the stack
        call  Call16_Far                    ; Invoke XVME BIOS function
        add   sp,4                          ; Clean up the stack
        cmp   Regs._ax,0                    ; Check for
        jne   error                         ;   an error
        <use output fields as needed>       ; Function outputs are valid
        ...

        ; Handle XVME BIOS function error
error:
        <error code in Regs._ax>
```


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The following assembly code fragment shows how to use the 32-bit near call interface. Fill the register structure, push the 32-bit linear offset of the BIOS (physical address F000h:0000h—typically determined through an operating system call), and the 32-bit linear of the register structure onto the stack, and then make a near call to the 32-bit call entry offset indicated in the Xycom BIOS Information Block. Upon return, the AX field should be checked to see if an error occurred. If no error occurred (AX field=0), any other output fields are valid. See Section 5.13 for more information on XVME BIOS function error codes.

```
        .data
Call32_Near         dd          ?
Info                XBIB        <>
Regs                regstruc    <>

        .code
; This code assumes that DS has been previously loaded, that the static
; entries in the data segment have been set up properly, and that the
; XBIB information has been correctly extracted.

        ; Generate 32-bit near call entry pointer
        ; (this section need only be performed once)
        <get 32-bit offset of BIOS from OS (BIOS_Addr)>
        xor         eax,eax                 ; Start with offset zero
        mov         ax,Info.Offset32        ; Get offset from XBIB
        add         eax,<BIOS_Addr>         ; Add BIOS_Addr
        mov         Call32_Near,eax         ; Fill in pointer

        ; Invoke XVME BIOS function using the 32-bit near call entry
        mov         Regs._al,<Fn#>          ; Indicate XVME BIOS function
        <fill registers fields as needed>   ; Provide function inputs
        push        <BIOS_Addr>             ; Indicate BIOS location
        push        offset Regs             ;   structure on the stack
        call        Call32_Near             ; Invoke XVME BIOS function
        add         sp,8                    ; Clean up the stack
        cmp         Regs._ax,0              ; Check for
        jne         error                   ;   an error
        <use output fields as needed>       ; Function outputs are valid
        ...

        ; Handle XVME BIOS function error
error:
        <error code in Regs._ax>
```


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The following assembly code fragment shows how to use the 32-bit far call interface. Fill the register structure, push the 32-bit linear offset of the BIOS (physical address F000h:0000h—typically determined via an operating system call), and the 32-bit offset and descriptor of the register structure onto the stack. Then make a far call to the 32-bit call entry offset indicated in the Xycom BIOS Information Block plus 6. Upon return, the AX field should be checked to see if an error occurred. If no error occurred (AX field=0), any other output fields are valid. See Section 5.13 for more information on XVME BIOS function error codes.

```
        .data
Call32_Far          label       qword
Call32_Offset       dd          ?
Call32_Descriptor   dw          ?
Info                XBIB        <>
Regs                regstruc    <>

        .code
; This code assumes that DS has been previously loaded, that the static
; entries in the data segment have been set up properly, and that the
; XBIB information has been correctly extracted.

        ; Generate 32-bit far call entry pointer
        ; (this section need only be performed once)
        <get descriptor of BIOS from OS (BIOS_Desc))
        <get 32-bit offset of BIOS from OS (BIOS_Addr)>
        xor         eax,eax                 ; Start with offset zero
        mov         ax,Info.Offset32        ; Get offset from XBIB
        add         eax,6                   ; Adjust for far entry
        add         eax,<BIOS_Addr>         ; Add BIOS_Addr
        mov         Call32_Offset,eax       ; Fill in pointer offset
        mov         ax,<BIOS_Desc>          ; Fill in pointer
        mov         Call32_Descriptor,ax    ; descriptor

        ; Invoke XVME BIOS function using the 32-bit near call entry
        mov         Regs._al,<Fn#>          ; Indicate XVME BIOS function
        <fill registers fields as needed>   ; Provide function inputs
        push        <BIOS_Addr>             ; Indicate BIOS location
        push        seg Regs                ; Put far address of register
        push        offset Regs             ;   structure on the stack
        call        Call32_Far              ; Invoke XVME BIOS function
        add         sp,10                   ; Clean up the stack
        cmp         Regs._ax,0              ; Check for
        jne         error                   ;   an error
        <use output fields as needed>       ; Function outputs are valid

        ; Handle XVME BIOS function error
error:
        <error code in Regs._ax>
```


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5.4 MISCELLANEOUS FUNCTIONS

This group of functions accesses information about the module, including the module ID, front panel LEDs, amount of on-board memory, and Flash BIOS configurations.

5.4.1 Get XVME Information

This function returns information about the XVME CPU module. This information includes the module number, call entry point offsets, attributes, and I/O register information.

Function 00h

Call With: AL = 00h

Returns:

If error:	AX	=	Error code
If successful:	AX	=	0
	BX	=	XVME CPU model number
	CX	=	Offset of 16-bit call entry point (relative to physical address F000h:0000h)
	DX*	=	Offset of 32-bit near call entry point (relative to physical address F000h:0000h)
	SI	=	Offset of attribute table (relative to physical address F000h:0000h)

See Tables 5-3 and 5-4 for attribute table content and attribute bit descriptions.

***Note:**
The offset of 32-bit far call entry point equals the contents of DX+6.

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Information in the Attribute Table (Table 5-3) is organized into two groups—attribute bits and I/O registers. The first byte in the Attribute Table contains the number of attribute bits (NB). The size (SZ) of the attribute bits section (in bytes) is calculated in the following manner:

$$SZ = (NB+7) \text{ div } 8$$

Where div indicates a modulo divide.

The starting offset of the I/O register information is calculated in the following manner:

$$I/O = SZ+1$$

Table 5-3 illustrates the overall format of the Attribute Table. Offset 00h contains the number of attribute bits. Offsets 01h through SZ contain the actual attribute bits (see Table 5-4 for a detailed definition of each attribute bit). Offset I/O contains the number of I/O registers (NR) in the table (I/O registers are 16 bits in length). Offsets I/O+1 through I/O+2NR+1 contain a list of the I/O addresses used in the XVME BIOS functions.

Table 5-3. Attribute Table Contents

Offset	**Descriptor**
00h	Number of attribute bits (NB)
01h	Attribute bits 0-7
. . .	. . .
SZ	. . .
I/O	Number of I/O registers (NR)
I/O+1 I/O+2	I/O register number 1
I/O+3 I/O+4	I/O register number 2
. . .	. . .
I/O+2NR I/O+2NR+1	. . .

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Attribute bit definitions for offsets 01h through SZ are detailed in Table 5-4. Using the calculations from the previous page, software written to the current definition will be upwardly compatible (if additional attribute bits are defined in future releases of the XVME BIOS).

Table 5-4. Attribute Bit Descriptions

Offset	Bit	Definition
01h	0-7	VMEbus Master Interface Type Indicates the VMEbus master data width and whether VMEbus master byte-swapping can be controlled by hardware. **Type** / **Data Width** / **Byte-swapping** 0 / (No VMEbus master interface.) / (No VMEbus master interface.) 1 / D16 / Nonprogrammable 2 / D16 / Programmable 3 / D32 / Nonprogrammable 4 / D32 / Programmable **Note:** For types that return nonprogrammable, the polarity of the byte-swapping bit can be determined by calling the Get VMEbus Master Configuration function (30h).
02h	0-7	VMEbus Slave Interface Type Indicates the VMEbus slave data width and whether VMEbus slave byte-swapping can be controlled by hardware. **Type** / **Data Width** / **Byte-swapping** 0 / (No VMEbus slave interface.) / (No VMEbus slave interface.) 1 / D16 / Nonprogrammable 2 / D16 / Programmable 3 / D32 / Nonprogrammable 4 / D32 / Programmable **Note:** For types that return nonprogrammable, the polarity of the byte-swapping bit can be determined by calling the Get VMEbus Slave Configuration function (40h).

Table continued on the following page.

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Table 5-4. Attribute Bit Descriptions (*continued*)

Offset	Bit	Definition
03h	0	Watchdog timer 0 - Not supported 1 - Control, Status, Strobe supported
	1	Pass and Fail LEDS 0 - LEDS not supported 1 - Control, Status supported
	2	Auxiliary Non-maskable Interrupt (ANMI) signal 0 - Always mapped to NMI signal 1 - Can be mapped to IRQ10 signal
	3	ANMI group 0 - Not supported 1 - Control supported
	4	VMEbus BERR ANMI 0 - Not supported 1 - Control, Status supported
	5	VMEbus ACFAIL ANMI 0 - Not supported 1 - Control, Status supported
	6	VMEbus SYSFAIL ANMI 0 - Not supported 1 - Control, Status supported
	7	ABORT push button ANMI 0 - Not supported 1 - Control, Status supported

Table continued on the following page.

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Table 5-4. Attribute Bit Descriptions (*continued*)

Offset	Bit	Definition
04h	0	VMEbus ACFAIL signal 0 - Not supported 1 - Supported
	1	VMEbus SYSFAIL signal 0 - Not supported 1 - Supported
	2	Auxiliary Maskable Interrupt (AMI) group 0 - Not supported 1 - Control supported
	3	VMEbus interrupt levels (1-7) AMI 0 - Not supported 1 - Control, Status supported
	4	VMEbus interrupter 0 - Not supported 1 - Generate, Status
	5	PC/AT system memory size 0 - Not supported 1 - Status supported
	6	Flash BIOS write 0 - Not supported 1 - Control supported
	7	System resources flag 0 - Not supported 1 - Status supported

Table continued on the following page.

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Table 5-4. Attribute Bit Descriptions (*continued*)

Offset	Bit	Definition
05h	0	VMEbus BERR timeout 0 - Not supported 1 - Control supported
	1	VMEbus master interface 0 - Not supported 1 - Control, Ownership (with Status) supported
	2	Real Mode Window VMEbus master short I/O 0 - Not supported 1 - Control supported
	3	Real Mode Window VMEbus master standard 0 - Not supported 1 - Control, Address supported
	4	Real Mode Window VMEbus master extended 0 - Not supported 1 - Control, Address supported
	5	Real Mode Window VMEbus master IACK 0 - Not supported 1 - Control supported
	6	VMEbus master address modifier 0 - Not supported 1 - Control supported
	7	VMEbus master bus request level 0 - Not supported 1 - Control supported

Table continued on the following page.

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Table 5-4. Attribute Bit Descriptions (*continued*)

Offset	Bit	Definition
06h	0	VMEbus master release mechanism 0 - Always release when done 1 - Can be set to release on request
	1	VMEbus slave interface 0 - Not supported 1 - Control supported
	2	VMEbus slave standard addressing 0 - Not supported 1 - Control supported
	3	VMEbus slave extended addressing 0 - Not supported 1 - Control supported
	4	VMEbus slave sccess address modifier 0 - Not supported 1 - Control supported
	5	VMEbus slave privilege address modifier 0 - Not supported 1 - Control supported
	6	VMEbus slave size 0 - Not supported 1 - Control supported
	7	VMEbus slave address 0 - Not supported 1 - Control supported

Table continued on the following page.

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Table 5-4. Attribute Bit Descriptions (*continued*)

Offset	Bit	Definition
07h	0	Protect mode VMEbus master short I/O 0 - Not supported 1 - Supported
	1	Protect mode VMEbus master standard 0 - Not supported 1 - Supported
	2	Protect mode VMEbus master extended 0 - Not supported 1 - Supported
	3	Protect Mode VMEbus master IACK 0 - Not supported 1 - Supported
	4	Remap of I/O registers 0 - Not supported 1 - Supported
	5-7	Reserved (all bits set to 0)

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5.4.2 Get Real Mode Window Physical Segment

This function returns the physical segment of PC/AT memory occupied by the Real Mode Window.

Function 01h

Call With:	AL	=	01h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BX	=	Physical segment, in real mode, of Real Mode Window

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5.4.3 Get Protect Mode VMEbus Physical Addresses

This function returns the upper 16 bits of the base address for each of the VMEbus address spaces. This information is useful for programs that use protect mode to access the VMEbus.

Function 02h

Call With: AL = 02h

Returns:

If error:	AX	= Error code
If successful:	AX	= 0
	BX	= Upper 16 bits for physical address of VMEbus IACK space
	CX	= Upper 16 bits for physical address of VMEbus short address space
	DX	= Upper 16 bits for physical address of VMEbus standard address space
	SI	= Upper 16 bits for physical address of VMEbus extended address space

Note:
Zero is returned for all VMEbus spaces not supported in protect mode.

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5.4.4 Get LED Configuration

This function indicates which state the front panel LEDs are in. Possible LED states are

Passed	Pass/Green LED on, Fail/Red LED off
Testing	Pass/Green LED on, Fail/Red LED on
Other	Pass/Green LED off, Fail/Red LED off
Failed	Pass/Green LED off, Fail/Red LED on

Function 03h

Call With: AL = 03h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current LED configuration

0 - Passed

1 - Testing

2 - Other

3 - Failed

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5.4.5 Set LED Configuration

This function alters the state of the front panel LEDs. Possible LED states are

Passed	Pass/Green LED on, Fail/Red LED off
Testing	Pass/Green LED on, Fail/Red LED on
Other	Pass/Green LED off, Fail/Red LED off
Failed	Pass/Green LED off, Fail/Red LED on

Function 04h

Call With: AL = 04h
BL = Desired LED configuration
0 - Passed
1 - Testing
2 - Other
3 - Failed

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
The XVME CPU modules assert the VMEbus SYSFAIL signal when the fail LED is on (Fail and Testing LED configurations) and the SFAIL switch (SW1 position 3) is closed.

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5.4.6 Get Memory Size

This function returns the amount of system memory installed on the module.

Function 05h

Call With:	AL	=	05h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BX	=	Amount of system memory in Mbytes

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5.4.7 Get Flash BIOS Write Configuration

This function returns the state of the module's on-board Flash BIOS write logic.

Function 06h

Call With:	AL	=	06h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BL	=	Current Flash BIOS write configuration
			0 - Disabled
			1 - Enabled

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5.4.8 Set Flash BIOS Write Configuration

This function enables or disables the module's on-board Flash BIOS write logic.

Function 07h

Call With:
AL = 07h
BL = Desired Flash BIOS write configuration
0 - Disabled
1 - Enabled

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
The write logic should only be enabled when the XVME CPU module's BIOS socket contains a Flash memory device. Programming algorithms vary with manufacturers. Consult your Flash device manual for more information.

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5.5 REAL MODE WINDOW (RMW) FUNCTIONS

This group of functions obtains or sets the configuration of the XVME CPU module's Real Mode Window interface. The Real Mode Window can be configured to ROM or any 64 Kbyte region in the VMEbus address space supported by the XVME CPU module.

5.5.1 Get Real Mode Window Configuration

This function returns the 64 Kbyte portion of VMEbus address space to which the Real Mode Window is currently configured.

Function 10h

Call With: AL = 10h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current Real Mode Window address space
- 0 - ROM
- 1 - VMEbus short
- 2 - VMEbus standard
- 3 - VMEbus IACK
- 4 - VMEbus extended

CL = Current upper 8 bits of the Real Mode Window (if BL is 2, VMEbus standard)

CX = Current upper 16 bits of the Real Mode Window (if BL is 4, VMEbus extended)

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5.5.2 Set Real Mode Window Configuration

This function configures the Real Mode Window to a particular 64 Kbyte portion of VME address space.

Function 11h

Call With:	AL	= 11h
	BL	= Desired Real Mode Window address space
		0 - ROM
		1 - VMEbus short
		2 - VMEbus standard
		3 - VMEbus IACK
		4 - VMEbus extended
	CL	= Desired upper 8 bits of the Real Mode Window (if BL is 2, VMEbus standard)
	CX	= Desired upper 16 bits of the Real Mode Window (if BL is 4, VMEbus extended)
Returns:		
If error:	AX	= Error code
If successful:	AX	= 0

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5.6 XVME AUXILIARY NON-MASKABLE INTERRUPT (ANMI) FUNCTIONS

This group of functions obtains and sets the XVME CPU module's ANMI configuration. The XVME ANMI group configuration, ANMI source mask, and ANMI status can be accessed.

5.6.1 Get XVME ANMI Configuration

This function returns the current XVME ANMI group configuration. This configuration tells you if the XVME ANMI group is enabled and identifies which signal it uses.

Function 20h

Call With: AL = 20h

Returns:

If error: AX = Error code
If successful: AX = 0
BL = Current ANMI configuration
0 - Disabled
1 - Enabled on NMI signal
2 - Enabled on IRQ10 signal

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5.6.2 Set XVME ANMI Configuration

This function sets the XVME ANMI group configuration, allowing the group to be enabled or disabled and mapped to the NMI or IRQ10 interrupt signals.

Function 21h

Call With:
AL = 21h
BL = Desired ANMI configuration
0 - Disabled
1 - Enabled on NMI signal
2 - Enabled on IRQ10 signal

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
If the XVME ANMI group is to be enabled on the NMI signal, all XVME ANMIs will be reset first. This clears prior XVME ANMIs that may still be pending.

When enabled, XVME ANMIs come in on the selected signal (see XVME ANMI Interrupt functions 20h). It is the responsibility of users to ensure that IRQ10—if used—is enabled via the 8259 and that an appropriate interrupt handler or NMI handler is provided. MS-DOS allows users to directly manipulate the 8259 and the interrupt vector table. Other operating systems usually provide a service for attaching to and enabling specific PC/AT IRQs, but tend to be less flexible when dealing with NMIs. Check your operating system documentation for proper interrupt and NMI handling procedures.

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5.6.3 Get XVME ANMI Interrupt Mask

This function returns the current state of the XVME ANMI source mask.

Function 22h

Call With: AL = 22h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current ANMI source mask

- Bit 0 Reserved
- Bit 1 VMEbus BERR ANMI
  - 0 - Disabled
  - 1 - Enabled
- Bit 2 VMEbus SYSFAIL ANMI
  - 0 - Disabled
  - 1 - Enabled
- Bit 3 ABORT push button ANMI
  - 0 - Disabled
  - 1 - Enabled
- Bit 4 VMEbus ACFAIL ANMI
  - 0 - Disabled
  - 1 - Enabled
- Bit 5-7 Reserved

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5.6.4 Enable/Disable Specific XVME ANMI Interrupts

This function enables or disables individual XVME ANMI sources.

Function 23h

Call With:

AL = 23h
BL = Enable/disable mask
- Bit 0 Operation to perform
  - 0 - Disable
  - 1 - Enable
- Bit 1 VMEbus BERR ANMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 2 VMEbus SYSFAIL ANMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 3 ABORT push button ANMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 4 VMEbus ACFAIL ANMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 5-7 Reserved (all bits set to 0)

Returns:

If error: AX = Error code
If successful: AX = 0

Note:
If the ANMI group is enabled on the IRQ10 signal (see XVME ANMI Interrupt functions 20h and 21h), any ANMI sources enabled by this function are reset first. This clears prior XVME ANMIs that may still be pending.

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5.6.5 Get XVME ANMI Status

When an XVME ANMI is detected, a call to this function determines which XVME ANMI occurred. This function can also determine the current state of the VMEbus SYSFAIL and ACFAIL signals.

Function 24h

Call With: AL = 24h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current ANMI status signals

- Bit 0 Reserved
- Bit 1 VMEbus BERR ANMI
  - 0 - Not pending
  - 1 - Pending
- Bit 2 VMEbus SYSFAIL ANMI
  - 0 - Not pending
  - 1 - Pending
- Bit 3 ABORT push button ANMI
  - 0 - Not pending
  - 1 - Pending
- Bit 4 VMEbus ACFAIL ANMI
  - 0 - Not pending
  - 1 - Pending
- Bit 5 VMEbus SYSFAIL signal
  - 0 - Currently negated
  - 1 - Currently asserted
- Bit 6 VMEbus ACFAIL signal
  - 0 - Currently negated
  - 1 - Currently asserted
- Bit 7 Reserved

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5.7 VMEBUS MASTER FUNCTIONS

This group of functions obtains or sets the configuration of the XVME CPU module's VMEbus master interface. VMEbus master configuration parameters that can be accessed include VMEbus master interface enable/disable, byte-swapping, access type, request levels, VMEbus release mechanism, and VMEbus ownership.

5.7.1 Get VMEbus Master Configuration

This function returns the XVME CPU module's current VMEbus master interface configuration.

Function 30h

Call With: AL = 30h

Returns:

If error: AX = Error code

If successful: AX = 0

BX = Current VMEbus master interface configuration

Bit 0	VMEbus master interface
	0 - Disabled
	1 - Enabled
Bit 1	VMEbus master byte-swapping
	0 - Disabled
	1 - Enabled
Bit 2	VMEbus master access type
	0 - Non-privileged
	1 - Supervisory
Bit 3-4	VMEbus request level
	00 - Level 0
	01 - Level 1
	10 - Level 2
	11 - Level 3
Bit 5	VMEbus release mechanism
	0 - Release when done
	1 - Release on request
Bit 6-15	Reserved

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5.7.2 Set VMEbus Master Configuration

This function modifies the configuration of the XVME CPU module's VMEbus master interface.

Function 31h

Call With:

AL = 31h
BX = Desired VMEbus master interface configuration

Bit 0	VMEbus master interface
	0 - Disabled
	1 - Enabled
Bit 1	VMEbus master byte-swapping
	0 - Disabled
	1 - Enabled
Bit 2	VMEbus master access type
	0 - Non-privileged
	1 - Supervisory
Bit 3-4	VMEbus request level
	00 - Level 0
	01 - Level 1
	10 - Level 2
	11 - Level 3
Bit 5	VMEbus release mechanism
	0 - Release VMEbus when done
	1 - Release VMEbus on request
Bit 6-15	Reserved (set all set bits to 0)

CX = Mask indicating which fields of the desired VMEbus master interface configuration are to be used (set bits to indicate which fields in BX to use)

Returns:

If error: AX = Error code
If successful: AX = 0

Note:
VMEbus Request Level cannot be changed when system resources are enabled and should only be changed when the VMEbus is owned by the XVME CPU module. The VMEbus Release Mechanism should only be changed when the VMEbus is owned by the XVME CPU module. (See VMEbus Master functions 32h-34h.)

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5.7.3 Get VMEbus Ownership Configuration

This function returns the current state of the VMEbus ownership requestor, providing a way to determine if ownership of the VMEbus has already been requested.

Function 32h

Call With:	AL	= 32h
Returns:		
If error:	AX	= Error code
If successful:	AX	= 0
	BL	= Current VMEbus ownership request setting 0 - Not requested 1 - Requested

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5.7.4 Set VMEbus Ownership Configuration

Although exclusive ownership of the VMEbus is not required for all VMEbus transfers, there may be instances where time critical operations need to be performed on the VMEbus without interruptions. This function gains exclusive ownership of the VMEbus. A call to this function requests ownership of the VMEbus from the arbiter. Use the Get VMEbus Ownership Status function (34h) to determine when the arbiter has granted ownership of the VMEbus.

Function 33h

Call With:
AL = 33h
BL = Desired VMEbus ownership requestor setting
0 - Not requested
1 - Requested

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
The Get VMEbus Ownership Configuration function (32h) can be used to determine if ownership has already been requested.

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5.7.5 Get VMEbus Ownership Status

This function can be used after executing the Set VMEbus Ownership Configuration function (33h). Use this function to determine when the arbiter has granted exclusive use of the VMEbus to the XVME CPU module.

Function 34h

Call With:	AL	=	34h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BL	=	Current VMEbus ownership status
			0 - Granted
			1 - Not granted

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5.8 VMEBUS SLAVE FUNCTIONS

This group of functions obtains and sets the configuration of the XVME CPU module's VMEbus slave interface. VMEbus slave configuration parameters that can be accessed include slave interface enable/disable, byte-swapping, access type, and slave interface address space and size.

5.8.1 Get VMEbus Slave Configuration

This function returns the configuration of the VMEbus slave interface.

Function 40h

Call With: AL = 40h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current VMEbus slave configuration

Bit 0	VMEbus slave interface
	0 - Disabled
	1 - Enabled
Bit 1	VMEbus slave byte-swapping
	0 - Disabled
	1 - Enabled
Bit 2	VMEbus slave access type 1
	0 - Non-privileged
	1 - Supervisory
Bit 3	VMEbus slave access type 2
	0 - Data
	1 - Program
Bit 4	VMEbus slave address space
	0 - VMEbus Standard
	1 - VMEbus Extended
Bit 5	Reserved
Bit 6-15	VMEbus slave address bits A22-A31

CX = Current VMEbus slave size in Mbytes

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5.8.2 Set VMEbus Slave Configuration

This function modifies the slave configuration parameters reported in the Get VMEbus Slave Configuration function (40h).

Function 41h

Call With:

AL = 41h
BL = Desired VMEbus slave configuration
- Bit 0 — VMEbus slave interface
  - 0 - Disabled
  - 1 - Enabled
- Bit 1 — VMEbus slave byte-swapping
  - 0 - Disabled
  - 1 - Enabled
- Bit 2 — VMEbus slave access type 1
  - 0 - Non-privileged
  - 1 - Supervisory
- Bit 3 — VMEbus slave access type 2
  - 0 - Data
  - 1 - Program
- Bit 4 — VMEbus slave address space
  - 0 - VMEbus standard
  - 1 - VMEbus extended
- Bit 5 — Reserved
- Bit 6-15 — VMEbus slave address bits A22-A31

CX = Desired VMEbus slave size in Mbytes

Returns:

If error: AX = Error code
If successful: AX = 0

Note:
VMEbus slave configuration should only be changed when the VMEbus is owned by the XVME CPU module. VMEbus slave size cannot be greater than the total amount of memory on the board. (See VMEbus Master functions 32h-34h.)

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5.9 VMEBUS INTERRUPT HANDLER FUNCTIONS

This group of functions configures and processes VMEbus interrupts—also referred to as Auxiliary Maskable Interrupts (AMIs)—received on IRQ10. Each of the seven VMEbus levels can be enabled or disabled.

5.9.1 Get VMEbus Interrupt Group Configuration

This function returns the current XVME AMI group configuration.

Function 50h

Call With:	AL	=	50h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BL	=	Current VMEbus interrupt group configuration 0 - Disabled 1 - Enabled

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5.9.2 Set VMEbus Interrupt Group Configuration

This function enables or disables the current XVME AMI group.

Function 51h

Call With:
AL = 51h
BL = Desired XVME AMI group configuration
0 - Disabled
1 - Enabled

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
When enabled, VMEbus interrupt level AMIs come in on IRQ10. It is the responsibility of the user to ensure that IRQ10 is enabled via the 8259 and that an appropriate interrupt handler is provided. MS-DOS allows the user to directly manipulate the 8259 and the interrupt vector table. If you use an operating system other than MS-DOS, consult your operating system documentation regarding the use of IRQ10.

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5.9.3 Get VMEbus Interrupt Mask

This function returns VMEbus interrupt level AMIs which are enabled and disabled.

Function 52h

Call With: AL = 52h

Returns:
If error: AX = Error code
If successful: AX = 0
BL = Current VMEbus interrupt mask
Bit 0 Reserved
Bit 1 VMEbus interrupt level 1 AMI
0 - Disabled
1 - Enabled
Bit 2 VMEbus interrupt level 2 AMI
0 - Disabled
1 - Enabled
Bit 3 VMEbus interrupt level 3 AMI
0 - Disabled
1 - Enabled
Bit 4 VMEbus interrupt level 4 AMI
0 - Disabled
1 - Enabled
Bit 5 VMEbus interrupt level 5 AMI
0 - Disabled
1 - Enabled
Bit 6 VMEbus interrupt level 6 AMI
0 - Disabled
1 - Enabled
Bit 7 VMEbus interrupt level 7 AMI
0 - Disabled
1 - Enabled

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5.9.4 Enable/Disable Specific VMEbus Interrupt Mask Bits

This function allows specific VMEbus interrupt level AMIs to be enabled or disabled.

Function 53h

Call With:

AL = 53h
BL = Enable/disable mask
- Bit 0 Operation to perform
  - 0 - Disabled
  - 1 - Enabled
- Bit 1 VMEbus interrupt level 1 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 2 VMEbus interrupt level 2 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 3 VMEbus interrupt level 3 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 4 VMEbus interrupt level 4 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 5 VMEbus interrupt level 5 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 6 VMEbus interrupt level 6 AMI
  - 0 - Leave as is
  - 1 - Perform operation
- Bit 7 VMEbus interrupt level 7 AMI
  - 0 - Leave as is
  - 1 - Perform operation

Returns:

If error: AX = Error code
If successful: AX = 0

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5.9.5 Get VMEbus Interrupt Status

This function indicates which VMEbus interrupts are pending. A pending interrupt needs to be acknowledged. The calling program can select any VMEbus interrupt level AMI or just those currently enabled.

Function 54h

Call With:

AL = 54h
BL = VMEbus interrupt level type
0 - VMEbus interrupt level AMIs that are enabled
1 - Any VMEbus interrupt level AMIs

Returns:

If error:
AX = Error code

If successful:
AX = 0
BX = Current VMEbus interrupt level AMI status
Bit 0 Reserved
Bit 1 VMEbus interrupt level 1
0 - Not pending
1 - Pending
Bit 2 VMEbus interrupt level 2
0 - Not pending
1 - Pending
Bit 3 VMEbus interrupt level 3
0 - Not pending
1 - Pending
Bit 4 VMEbus interrupt level 4
0 - Not pending
1 - Pending
Bit 5 VMEbus interrupt level 5
0 - Not pending
1 - Pending
Bit 6 VMEbus interrupt level 6
0 - Not pending
1 - Pending
Bit 7 VMEbus interrupt level 7
0 - Not pending
1 - Pending

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5.9.6 Acknowledge VMEbus Interrupt

If an interrupt is pending on one of the VMEbus interrupt levels, an interrupt acknowledge cycle must be executed to retrieve the Status ID vector from the interrupter. This function performs an Interrupt Acknowledge (IACK) cycle on the interrupt level passed by the calling program.

Function 55h

Call With:
AL = 55h
BL = VMEbus interrupt level to acknowledge
1 - VMEbus interrupt level 1
2 - VMEbus interrupt level 2
3 - VMEbus interrupt level 3
4 - VMEbus interrupt level 4
5 - VMEbus interrupt level 5
6 - VMEbus interrupt level 6
7 - VMEbus interrupt level 7

Returns:
If error: AX = Error code
If successful: AX = 0
BL = Status ID vector obtained during VMEbus IACK

Note:
This function is currently unsupported, but should be used in case the current IACK mechanism changes in the future. If the unsupported error code is returned, then perform the VMEbus IACK manually. This is accomplished by reading the VMEbus IACK space at the following offset:

Offset=(Level*2) - 1

Level is the VMEbus interrupt level to be acknowledged (BL).

This manual IACK requires the VMEbus master interface to be enabled. (See VME Master functions 30h and 31h.)

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5.10 VMEBUS INTERRUPTER FUNCTIONS

This group of functions operates and determines the status of the XVME CPU module's VMEbus interrupter interface.

5.10.1 Generate VMEbus Interrupt

This function stores the vector supplied by the calling program, sets up the interrupt request level, and then generates a VMEbus interrupt.

Function 60h

Call With:
AL = 60h
BL = Level of VMEbus interrupt to be generated (1-7)
BH = Interrupt vector to respond with during VMEbus IACK cycle

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
Prior to calling this function, use the Get VMEbus Interrupt Acknowledge Status function (61h) to wait for previous VMEbus interrupts to complete.

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5.10.2 Get VMEbus Interrupt Acknowledge Status

This function checks the status of the VMEbus interrupter to determine if a generated interrupt has been acknowledged by a VMEbus interrupt handler.

Function 61h

Call With:	AL =	61h
Returns:		
If error:	AX =	Error code
If successful:	AX =	0
	BL =	Current VMEbus interrupt acknowledge status
		0 - Acknowledged
		1 - Pending

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5.11 SOFTWARE WATCHDOG TIMER FUNCTIONS

This group of functions accesses the watchdog timer. If enabled, the watchdog timer can expire, generating an ANMI to the CPU if it is not strobed once every 16 μsec.

5.11.1 Get Software Watchdog Timer Configuration

This function returns the current state of the watchdog timer.

Function 70h

Call With:	AL	=	70h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BL	=	Current watchdog timer configuration
			0 - Disabled
			1 - Enabled

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5.11.2 Set Software Watchdog Timer

This function enables or disables the watchdog timer.

Function 71h

Call With:
AL = 71h
BL = Desired watchdog timer configuration
0 - Disabled
1 - Enabled

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
The watchdog timer is always reset before it is enabled. This clears prior watchdog timer ANMIs that may still be pending. When enabled, the watchdog timer interrupt comes in as an NMI. It is the responsibility of the user to ensure that an appropriate NMI handler is provided. MS-DOS allows the user to directly manipulate the interrupt vector table. Other operating systems tend to be less flexible in this area. Check your operating system documentation for proper NMI handling.

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5.11.3 Get Software Watchdog Timer Status

This function determines if the watchdog timer has expired.

Function 72h

Call With:	AL	=	72h
Returns:			
If error:	AX	=	Error code
If successful:	AX	=	0
	BL	=	Current watchdog timer status
			0 - Watchdog timer has not expired
			1 - Watchdog timer has expired

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5.11.4 Strobe Software Watchdog Timer

The watchdog timer must be strobed once every 16 μsec to avoid expiration. A call to this function strobes the watchdog timer.

Function 73h

Call With: AL = 73h

Returns:
If error: AX = Error code
If successful: AX = 0

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5.12 VMEBUS SYSTEM RESOURCE FUNCTIONS

This group of functions reads the status of the module's system resources and sets the VMEbus BERR timeout.

5.12.1 Get VMEbus System Resource Flag

The System Resource Flag indicates if the system resources, VMEbus BERR, VMEbus arbiter, and VMEbus system clock are provided by the module. The System Resource Control (SRC) switch (SWI position 4) enables or disables system resources.

Function 80h

Call With:	AL	= 80h
Returns:		
If error:	AX	= Error code
If successful:	AX	= 0
	BL	= State of system resource flag
		0 - System resources disabled
		1 - System resources enabled

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5.12.2 Get VMEbus BERR Timeout System Resource Configuration

A call to this function returns the value of the VMEbus BERR timeout.

Function 81h

Call With: AL = 81h

Returns:

If error: AX = Error code

If successful: AX = 0

BL = Current VMEbus BERR timeout system resource configuration

Bit 0-1 Current VMEbus BERR timeout

00 - 8 μsec

01 - 16 μsec

10 - 32 μsec

11 - 64 μsec

Bit 2-7 Reserved

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5.12.3 Set VMEbus BERR Timeout System Resource Configuration

This function allows the selection of the on-board VMEbus BERR timeout value. Choices are 8 μsec, 16 μsec, 32 μsec, and 64 μsec.

Function 82h

Call With:
AL = 82h
BL = Desired VMEbus BERR timeout system resource configuration
Bit 0-1 Current VMEbus BERR timeout
00 - 8 μsec
01 - 16 μsec
10 - 32 μsec
11 - 64 μsec
Bit 2-7 Reserved (all bits set to 0)

Returns:
If error: AX = Error code
If successful: AX = 0

Note:
VMEbus BERR Timeout cannot be changed if system resources are disabled. Also, VMEbus system resources should only be changed when the VMEbus is owned by the XVME processor board. (See VMEbus Master functions 32h-34h.)

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5.13 XVME BIOS FUNCTION ERROR CODES

The error codes that can be returned by an XVME BIOS function are listed below.

5.13.1 0300h

Title: Invalid Value

Description: One or more of the input parameters passed to the requested function was invalid.

Solution: Correct the invalid input parameter values and try the function again. Some parameters may be valid on one XVME CPU module, but not on another. Consult your XVME CPU module manual for supported hardware features.

5.13.2 FE00h

Title: Unsupported Function

Description: The requested function is not supported.

Solution: Correct the function number and try the function again. Some functions may be valid on one XVME CPU module, but not on another. Consult your XVME CPU module manual for supported hardware features.

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A.1 VMEBUS SIGNALS

The XVME-675 PC/AT Processor Module is a single-board VMEbus-compatible module. On the rear edge of the board are two 96-pin bus connectors labeled P1 and P2. Connectors P1 and P2 carry the standard address, data, and control signals required for a P1 and P2 backplane interface, as defined by the VMEbus specification. Table A-1 identifies and defines the signals carried by the P1 and P2 connectors.

Table A-1. VMEbus Signal Identification

Signal Mnemonic	Connector, Row: Pin Number	Signal Name and Description
ACFAIL*	1B:3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	1A:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17 18,19 1C:1	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus such as size, cycle type, and/or DTB master identification.
AS*	1A:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A:24-30 1C:15-30	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.

Table continued on the following page.

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Table A-1. VMEbus Signal Identification (*continued*)

Signal Mnemonic	**Connector, Row: Pin Number**	**Signal Name and Description**
BBSY*	1B:1	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG3IN*	1B:4,6,8,10	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the arbiter or requestors. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*-BG3OUT*	1B:5,7,9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by requestors. These signals indicate that a DTB master in the daisy chain requires access to the bus.
BR0*-BR3*	1B:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by requestors. These signals indicate that a DTB master in the daisy chain requires access to the bus.
DS0*	1A:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DS1*	1A:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).

Table continued on the following page.

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Table A-1. VMEbus Signal Identification (*continued*)

Signal Mnemonic	**Connector, Row: Pin Number**	**Signal Name and Description**
DTACK*	1A:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D31	1A:1-8 1C:1-8 2B:1A-21 2B:23-30	DATA BUS (bits 0-31): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A:9,11,15, 17,19 1B:20,23 1C:9 2B:2,12,22,31	GROUND
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* to start the interrupt acknowledge daisy chain.
IRQ1*-IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERVED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B:21	A reserved signal that will be used as the clock for a serial communication bus protocol that is still being finalized.
SERDAT	1B:22	A reserved signal that will be used as the transmission line for serial communication bus messages.

Table continued on the following page.

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Table A-1. VMEbus Signal Identification (*continued*)

Signal Mnemonic	**Connector, Row: Pin Number**	**Signal Name and Description**
SYSCLK	1A:10	SYSTEM CLOCK: A constant 16 MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.
SYSFAIL*	1C:10	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	1C:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	1B:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5	1A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12V	1A:31	-12 VDC POWER: Used by system logic circuits.

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A.2 CONNECTORS

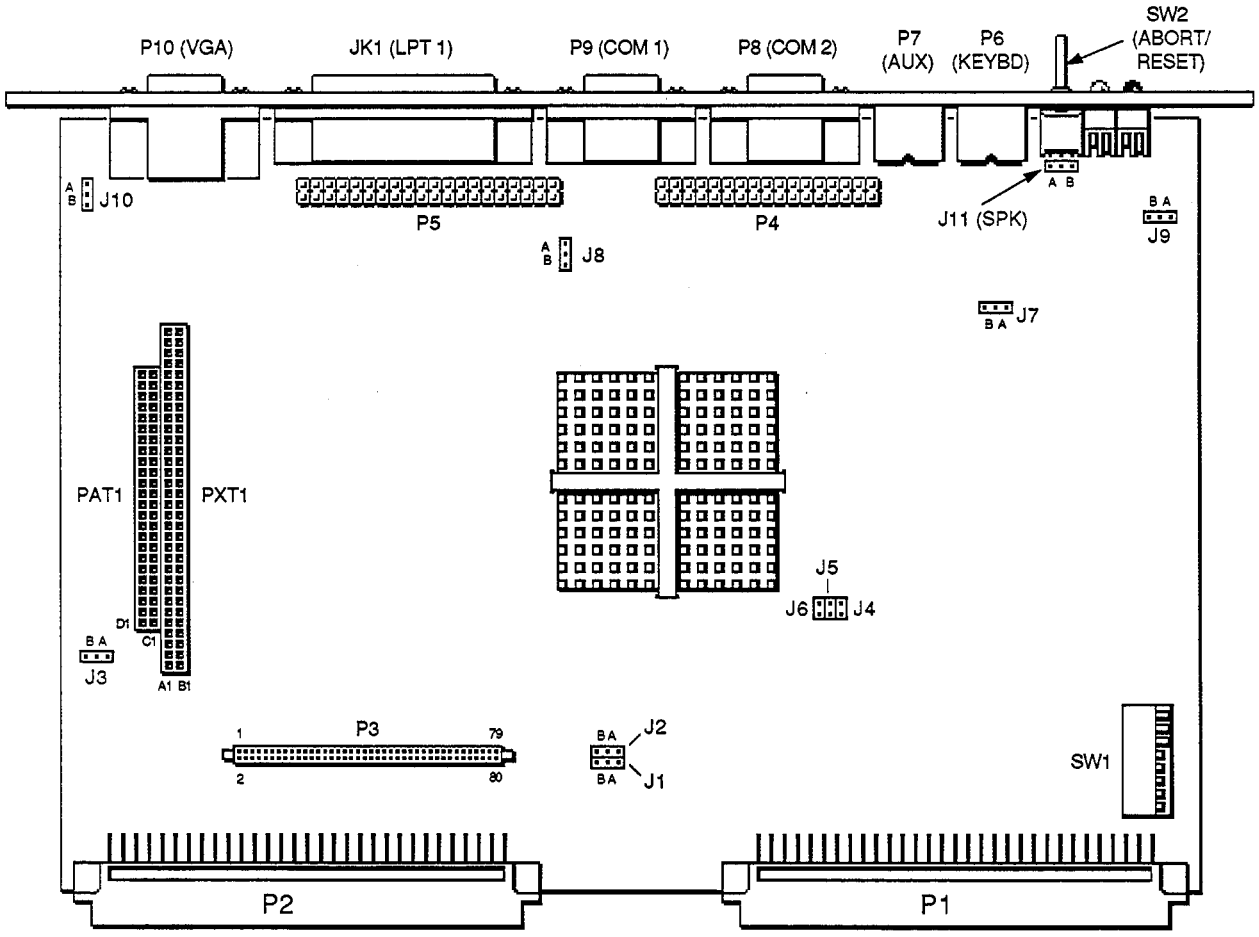


Figure A-1. XVME-675 Connectors and Jumpers

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A.2.1 **Keyboard Connector**

The keyboard connector, P6, is a six-pin MINI DIN connector.

Table A-2. Keyboard Connector (P6)

Pin	Description
1	DATA
2	N/C
3	GND
4	+5V
5	CLK
6	N/C

A.2.2 **Auxiliary Connector**

The auxiliary connector, P7, is a six-pin MINI DIN connector designed to be PS/2 compatible. This port accepts a PS/2-compatible mouse, track ball, etc.

Table A-3. Auxiliary Connector (P7)

Pin	Description
1	DATA
2	N/C
3	GND
4	+5V
5	CLK
6	N/C

A.2.3 **Speaker Connector**

The speaker connector, J11, is a three-pin header.

Table A-4. Speaker Connector (J11)

Pin	Description
1	Signal
2	+5V
3	N/C

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A.2.4 COM1 Serial Port Connector

The serial connector, located on the front panel, is a nine-pin D subminiature designated as P9.

Table A-5. COM1 Serial Port Connector (P9)

Pin	Description
1	DCD1
2	RXD1
3	TXD1
4	DTR1
5	GND
6	DSR1
7	RTS1
8	CTS1
9	R11

A.2.5 COM2 Serial Port Connector

The serial connector, located on the front panel, is a nine-pin D subminiature designated as P8.

Table A-6. COM2 Serial Port Connector (P8)

Pin	Description
1	DCD2
2	RXD2
3	TXD2
4	DTR2
5	GND
6	DSR2
7	RTS2
8	CTS2
9	R12

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A.2.6 **Parallel Port Connector**

The parallel port connector, JK1, is a 25-pin female D subminiature connector.

Table A-7. Parallel Port Connector (JK1)

Pin	Description
1	STROBE
2	PDOUT0
3	PDOUT1
4	PDOUT2
5	PDOUT3
6	PDOUT4
7	PDOUT5
8	PDOUT6
9	PDOUT7
10	PACK
11	PBUSY
12	PE
13	SELECT
14	AUTOFEED
15	PERROR
16	INIT
17	SELIN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

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A.2.7 **VGA Connector**

The VGA connector, P10, is a 15-pin D subminiature.

Table A-8. VGA Connector (P10)

Pin	Description
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	KEY
10	GND
11	NC
12	NC
13	HSYNC
14	VSYNC
15	NC

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A.2.8 **Floppy Drive Connector**

The floppy drive connector, P4, is a 34-pin header. The GND signals are grouped together to save space.

Table A-9. Floppy Drive Connector (P4)

Pin	Description
1	GND
2	FRWC*
3	GND
4	NC
5	KEY
6	NC
7	GND
8	IDX*
9	GND
10	MOI*
11	GND
12	FDS2*
13	GND
14	FDS1*
15	GND
16	MO2*
17	GND
18	FDIRC*
19	GND
20	FSTEP*
21	GND
22	FWD*
23	GND
24	FWE*
25	GND
26	FTKO*
27	GND
28	FWP*
29	GND
30	FRDD*
31	GND
32	FHS*
33	GND
34	DCHG*

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A.2.9 **IDE Drive Connector**

The IDE Drive Connector, P5, is a 40-pin connector.

Table A-10. IDE Drive Connector (P5)

Pin	Description
1	RESET*
2	GND
3	SD7
4	SD8
5	SD6
6	SD9
7	SD5
8	SD10
9	SD4
10	SD11
11	SD3
12	SD12
13	SD2
14	SD13
15	SD1
16	SD14
17	SD0
18	SD15
19	GND
20	N/C
21	N/C
22	GND
23	IOW*
24	GND
25	IOR*
26	GND
27	N/C
28	ALE
29	N/C
30	GND
31	IDINT
32	ATIOCS16*
33	SA1
34	N/C
35	SA0
36	SA2
37	HCS0*
38	HCS1*
39	N/C
40	GND

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A.2.10 **VMEbus Connectors**

The P1 and P2 VMEbus connectors are 96-pin DIN connectors.

Table A-11. VMEbus Connector (P1)

P1			
Pin	**A**	**B**	**C**
1	D00	BBBUSY	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5v STDBY	+12V
32	+5V	+5V	+5V

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Table A-12. VMEbus Connector (P2)

P2			
Pin	**A**	**B**	**C**
1	N/C	+5V	N/C
2	N/C	GND	N/C
3	N/C	N/C	N/C
4	N/C	A24	N/C
5	N/C	A25	N/C
6	N/C	A26	N/C
7	N/C	A27	N/C
8	N/C	A28	N/C
9	N/C	A29	N/C
10	N/C	A30	N/C
11	N/C	A31	N/C
12	N/C	GND	N/C
13	N/C	+5V	N/C
14	N/C	D16	N/C
15	N/C	D17	N/C
16	N/C	D18	N/C
17	N/C	D19	N/C
18	N/C	D20	N/C
19	N/C	D21	N/C
20	N/C	D22	N/C
21	N/C	D23	N/C
22	N/C	GND	N/C
23	N/C	D24	N/C
24	N/C	D25	N/C
25	N/C	D26	N/C
26	N/C	D27	N/C
27	N/C	D28	N/C
28	N/C	D29	N/C
29	N/C	D30	N/C
30	N/C	D31	N/C
31	N/C	GND	N/C
32	N/C	+5V	N/C

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A.2.11 PXT1 CONNECTOR (PC/104 Expansion Site)

PXT1 is a 32-pin connector that is used to add PC/104 expansion modules to the XVME-675.

Table A-13. PXT1 Connector

Pin	Row A Signal	Row B Signal
1	IOCHCHK*	GND
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	N/C
6	SD3	DRQ2
7	SD2	-12V
8	SD1	N/C
9	SD0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW*
12	SA19	SMEMR*
13	SA18	IOW*
14	SA17	IOR*
15	SA16	DACK3*
16	SA15	DRQ3
17	SA14	DACK1*
18	SA13	DRQ1
19	SA12	REF*
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2*
27	SA4	T/C
28	SA3	ALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND

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A.2.12 PAT1 CONNECTOR (PC/104 Expansion Site)

PAT1 is a 24-pin connector that is used to add PC/104 expansion modules to the XVME-675.

Table A-14. PAT1 Connector

Pin	Row C Signal	Row D Signal
0	GND	GND
1	SBHE*	MEMCS16*
2	LA23	IOCS16*
3	LA22	IRQ10
4	LA21	IRQ11
5	LA20	IRQ12
6	LA19	IRQ15
7	LA18	IRQ14
8	LA17	DACK0*
9	MEMR*	DRQ0
10	MEMW*	DACK5*
11	SD8	DRQ5
12	SD9	DACK6*
13	SD10	DRQ6
14	SD11	DACK7*
15	SD12	DRQ7
16	SD13	+5V
17	SD14	N/C
18	SD 15	GND
19	KEY	GND

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B.1 JUMPERS

The XVME-675 uses 10 jumpers to configure hardware options. All jumpers are shipped in position A. Jumpers are defined in Table B-1, below.

> **NOTE**
> Unless you wish to disable VGA or replace the BIOS EPROM with Flash, all jumpers should be left in the default position.

> **NOTE**
> Silk screened jumper definitions are located on the top of the CPU board.

Table B-1. Jumper Settings

Jumper	Setting	Description
J1	A✓	CPU option 80486
	B	CPU option 80486SX
J2	A✓	CPU option 80486
	B	CPU option 80486SX
J3	A✓	CMOS okay
	B	CMOS clear
J4, J5, J6	OUT	Install for +5 V P24T Pentium overdrive processor
J7	A✓	ROM or Flash non-writable +5 V
	B	Flash +12 V
J8	A✓	VGA enabled
	B	VGA disabled
J9	A✓	IRQ12 driven by auxiliary port
	B	IRQ12 not driven by auxiliary port
J10	A✓	IRQ9 driven by the VGA controller
	B	IRQ9 not driven by the VGA controller

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NOTE

Perform the following steps to clear the CMOS RAM configuration:

1. Change J3 to position B.
2. Power up the board until the BIOS sign-on message appears.
3. Turn off the power and switch J3 to position A.
4. Power up the board again.

B.2 SWITCH SW1

Switch SW1 allows critical options not in software control to be enabled in one common area.

NOTE

Silk screened switch definitions are located on the back of the CPU board.

Table B-2. Switch SW1 Settings

Position	Setting	Description
1	Open Closed✓	VME SYSRESET* not driven on power up VME SYSRESET* driven on power up
2	Open Closed✓	VME SYSRESET* not caused by toggle switch VME SYSRESET* caused by toggle switch
3	Open✓ Closed	VME SYSFAIL not driven on VMEbus VME SYSFAIL driven on VMEbus
4	Open Closed✓	System resources disabled System resources enabled
5	Open✓ Closed	Local reset disabled Local reset caused by toggle switch
6	Open✓ Closed	Reserved Reserved
7	Open✓ Closed	Keyboard enabled Keyboard inhibited
8	Open✓ Closed	Color enabled BW

✓ = default settings

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The XVME-675 supports standard VGA resolutions 0-13, as well as the following Super VGA resolutions:

- 640 x 480 x 256 colors
- 640 x 480 x 32K colors
- 640 x 480 x 64K colors
- 800 x 600 x 16 colors
- 800 x 600 x 256 colors
- 800 x 600 x 32K colors
- 800 x 600 x 64K colors
- 1024 x 768 x 16 colors (interlaced or non-interlaced)
- 1024 x 768 x 256 colors (interlaced or non-interlaced)

Because these resolutions are beyond the original IBM specification, an enhanced monitor and a video driver are needed to support these modes. The steps for ensuring that these are available are listed below.

- Make sure your monitor has the desired resolution capabilities. A generic IBM clone is not able to sync on the different frequencies required for extended modes. Refer to Table C-2 for the horizontal and vertical frequencies for each mode. If you want to run different extended modes at different times, a multisync monitor is recommended. If you are using a multisync monitor, make sure the maximum horizontal and vertical frequencies are not exceeded. Otherwise, the monitor will not sync.

- Make sure a video driver is available to run your application software. These video drivers are available from Xycom. The drivers are loaded as part of the setup for the application program. The environments and applications supported in this package are listed in Table C-1.

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Table C-1. Supported Environments/Applications

Product	**Supported Resolutions**
AutoCAD v10, v11	640x480, 800x600, 1024x768
Autoshade v2	640x480, 800x600, 1024x768 - 256 colors 640x480 - 65,536 colors
3D Studio v1, v2	640x480, 800x600, 1024x768 - 256 colors 640x480 - 65,536 colors
GEM v3.x	800x600, 1024x768 - 16 colors
Lotus 1-2-3 v2.x	132x25, 132x43 - 16 (text) 800x600 - 16 colors
Lotus 1-2-3 v3.x	800x600, 1024x768 - 16 colors
Lotus Symphony v2	132x25, 132x43 - 16 (text) 800x600 - 16 colors
Microsoft Windows	640x480, 800x600, 1024x768 640x480, 800x600, 1024x768 - 256 colors 640x480 - 65,536 colors
Microsoft Word v5.0	800x600 - 16 colors
Microsoft Word v5.1-v5.5	800x600, 1024x768 - 16 colors
OS/2 v2.0	800x600, 1024x768 - 16 colors
Ventura Publisher v2, v3	800x600, 1024x768 - 16 colors
WordPerfect v5.1	800x600, 1024x768 - 16 colors
WordStar v5.5-v7.0 & 2000	800x600, 1024x768 - 16 colors

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The Cirrus Logic VGA BIOS supports all standard VGA modes. These standard VGA modes are listed in Table C-2. Following is the legend for tables C-2 and C-3.

Legend	
i	interlaced mode
n	non-interlaced mode
*	EGA resolution
+	VGA resolution

Table C-2. Cirrus Logic VGA BIOS–Standard VGA Modes

Mode #	VESA Mode #	# of Colors	Col. x Row	Char. Cell	Pixels	Display Mode	Horiz. Freq. KHz	Vert. Freq. Hz
00/01	-	16	40x25	8x8	320x200	Text	31.5	70
00*/01	-	16	40x25	8x14	320x350	Text	31.5	70
00+/01+	-	16	40x25	9x16	360x400	Text	31.5	70
02/03	-	16	80x25	8x8	640x200	Text	31.5	70
02*/03*	-	16	80x25	8x14	640x350	Text	31.5	70
02+/03+	-	16	80x25	9x16	720x400	Text	31.5	70
04/05	-	4	40x25	8x8	320x200	Graphics	31.5	70
6	-	2	80x25	8x8	640x200	Graphics	31.5	70
07*	-	mono	80x25	9x14	720x350	Text	31.5	70
07+	-	mono	80x25	9x16	720x400	Text	31.5	70
0D	-	16	40x25	8x8	320x200	Graphics	31.5	70
0E	-	16	80x25	8x8	640x200	Graphics	31.5	70
0F	-	mono	80x25	8x14	640x350	Graphics	31.5	70
10	-	16	80x25	8x14	640x480	Graphics	31.5	70
11	-	2	80x30	8x16	640x480	Graphics	31.5	70
12	-	16	80x30	8x16	640x480	Graphics	31.5	70
13	-	256	40x25	8x8	320x200	Graphics	31.5	70

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The Cirrus Logic VGA BIOS supports standard VESA and extended modes. These modes are listed in the following table:

Table C-3. Cirrus Logic VGA BIOS–Super VGA Modes

Mode #	VESA Mode #	# of Colors	Col. x Row	Char. Cell	Screen Format	Display Mode	Dot Freq. MHz	Horiz. Freq. KHz	Vert. Freq. Hz
14	-	16	132x25	8x16	1056x400	Text	41.5	31.5	70
54	10A	16	132x43	8x8	1056x350	Text	41.5	31.5	70
55	109	16	132x25	8x14	1056x350	Text	41.5	31.5	70
58,6A	102	16	100x37	8x16	800x600	Graphics	36	35.2	56
58,6A	102	16	100x37	8x16	800x600	Graphics	40	37.8	60
58,6A	102	16	100x37	8x16	800x600	Graphics	50	48.1	72
5C	103	256	100x37	8x16	800x600	Graphics	36	35.2	56
5C	103	256	100x37	8x16	800x600	Graphics	40	37.9	60
5C	103	256	100x37	8x16	800x600	Graphics	50	48.1	72
5Di	104	16	128x48	8x16	1024x768	Graphics	44.9	35.5	87i
5D	104	16	128x48	8x16	1024x768	Graphics	65	48.3	60
5D	104	16	128x48	8x16	1024x768	Graphics	75	56	70
5D	104	16	128x48	8x16	1024x768	Graphics	77	58	72
5F	101	256	80x30	8x16	640x480	Graphics	25	31.5	60
5F	101	256	80x30	8x16	640x480	Graphics	31.5	37.9	72

Table continued on the following page.

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Table C-3. Cirrus Logic VGA BIOS–Super VGA Modes (*continued*)

Mode #	VESA Mode #	# of Colors	Col. x Row	Char. Cell	Screen Format	Display Mode	Dot Freq. MHz	Horiz. Freq. KHz	Vert. Freq. Hz
60i	105	256	128x48	8x16	1024x768	Graphics	44.9.	35.5	87i[2]
60	105	256	128x48	8x16	1024x768	Graphics	65	48.3	60
60	105	256	128x48	8x16	1024x768	Graphics	75	56	70
60	105	256	128x48	8x16	1024x768	Graphics	77	58	72
64	111	64K	-	-	640x480	Graphics	25	31.5	60
64	111	64K	-	-	640x480	Graphics	62.8	37.9	72
66	110	32K	-	-	640x480	Graphics	25	31.5	60
66	110	32K	-	-	640x480	Graphics	62.8	37.9	72
6F	10E	64K	40x25	8x8	320x200	Graphics	25	31.5	70

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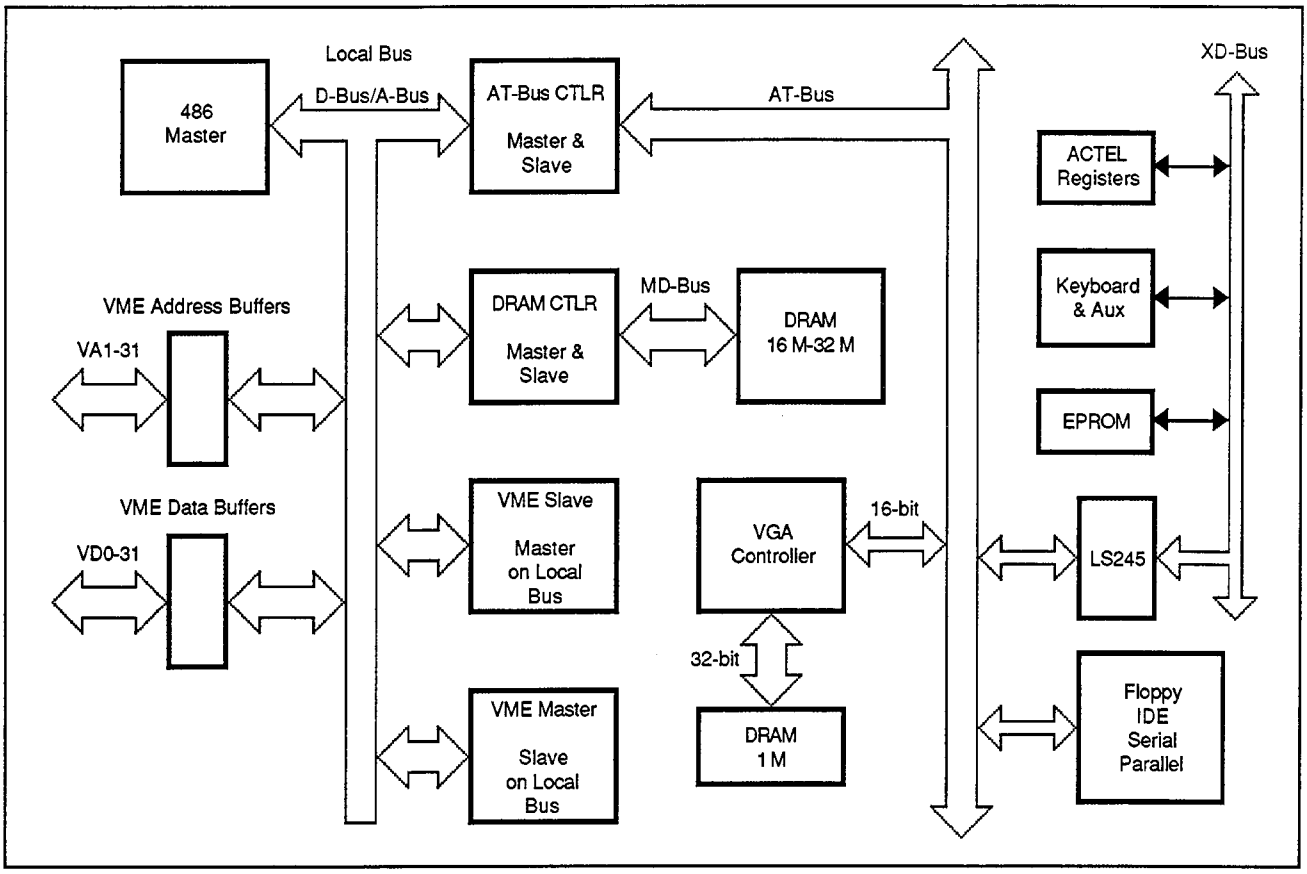


Figure D-1. XVME-675 CPU Board Block Diagram

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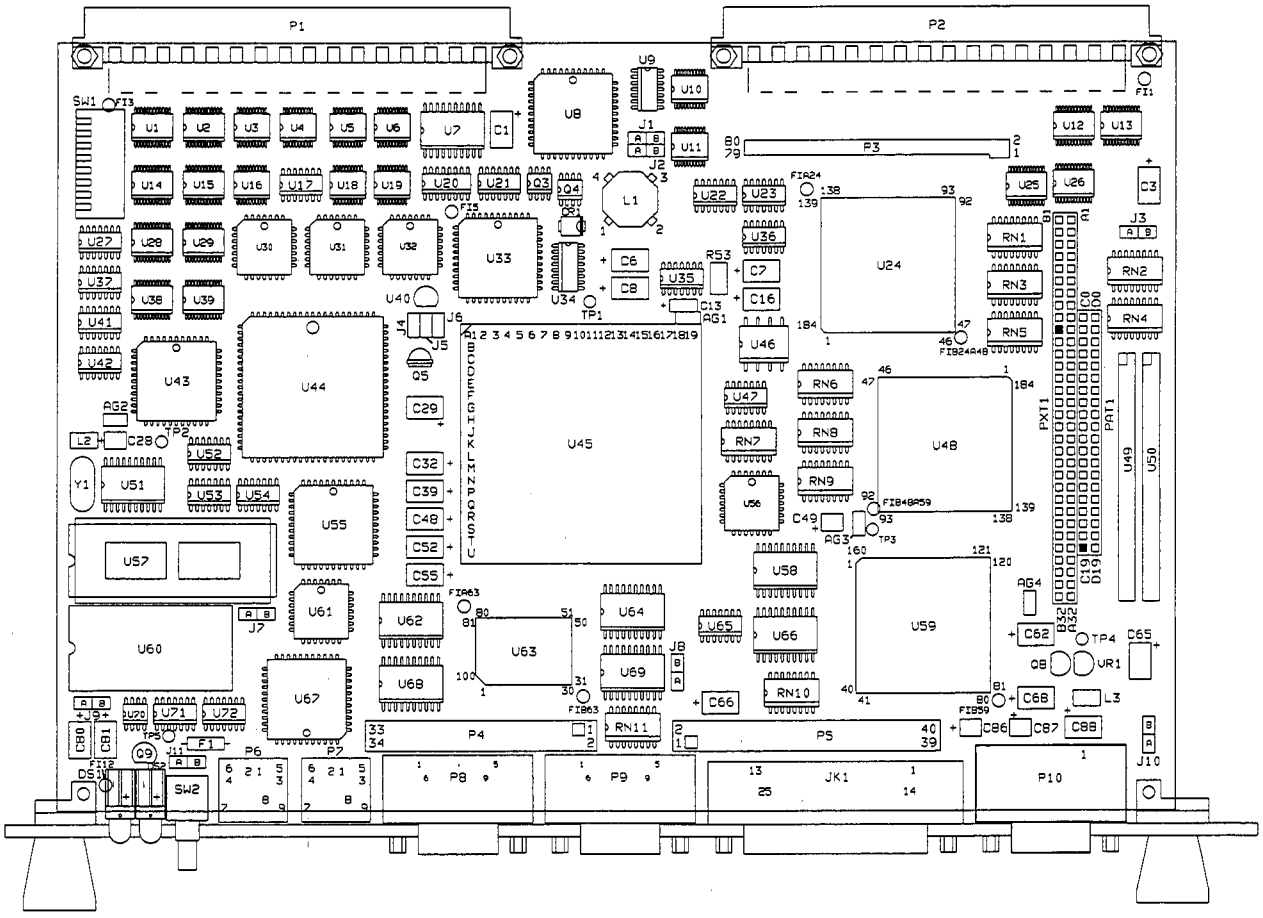


Figure D-2. XVME-675 CPU Board Assembly Drawing

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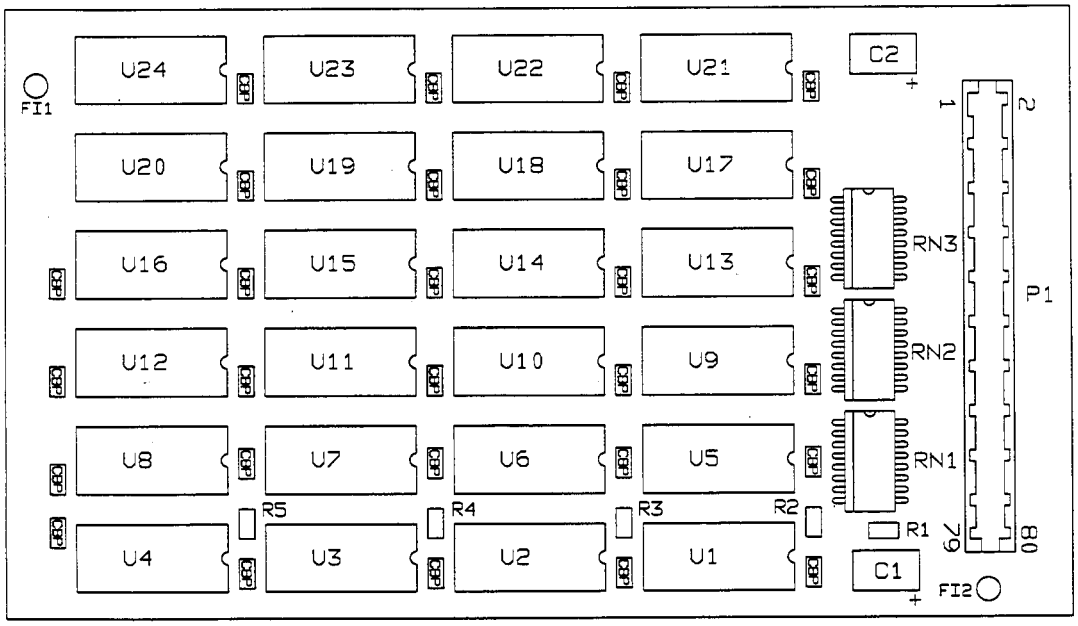
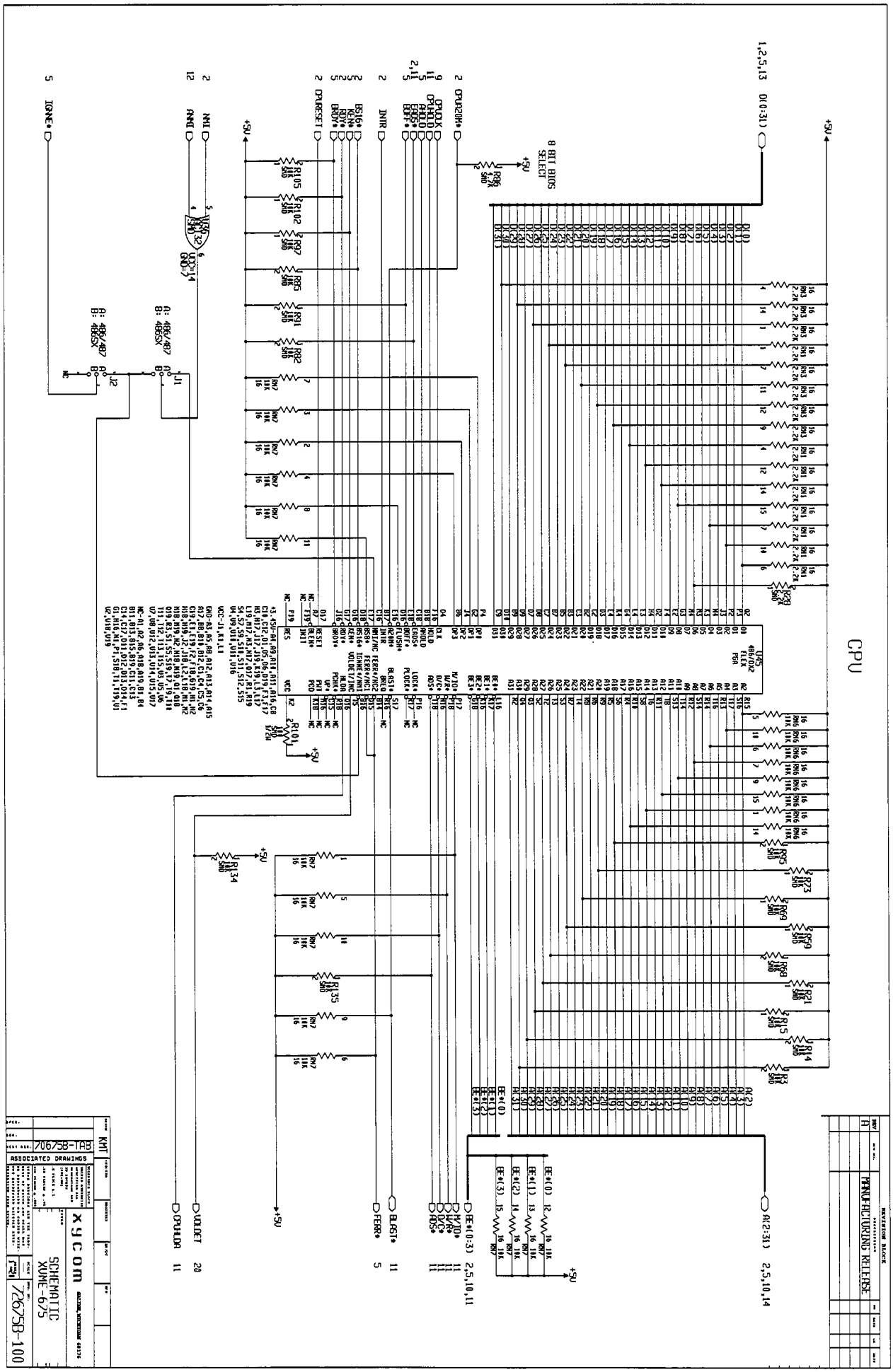


Figure D-3. XVME-675 Memory Board Assembly Drawing

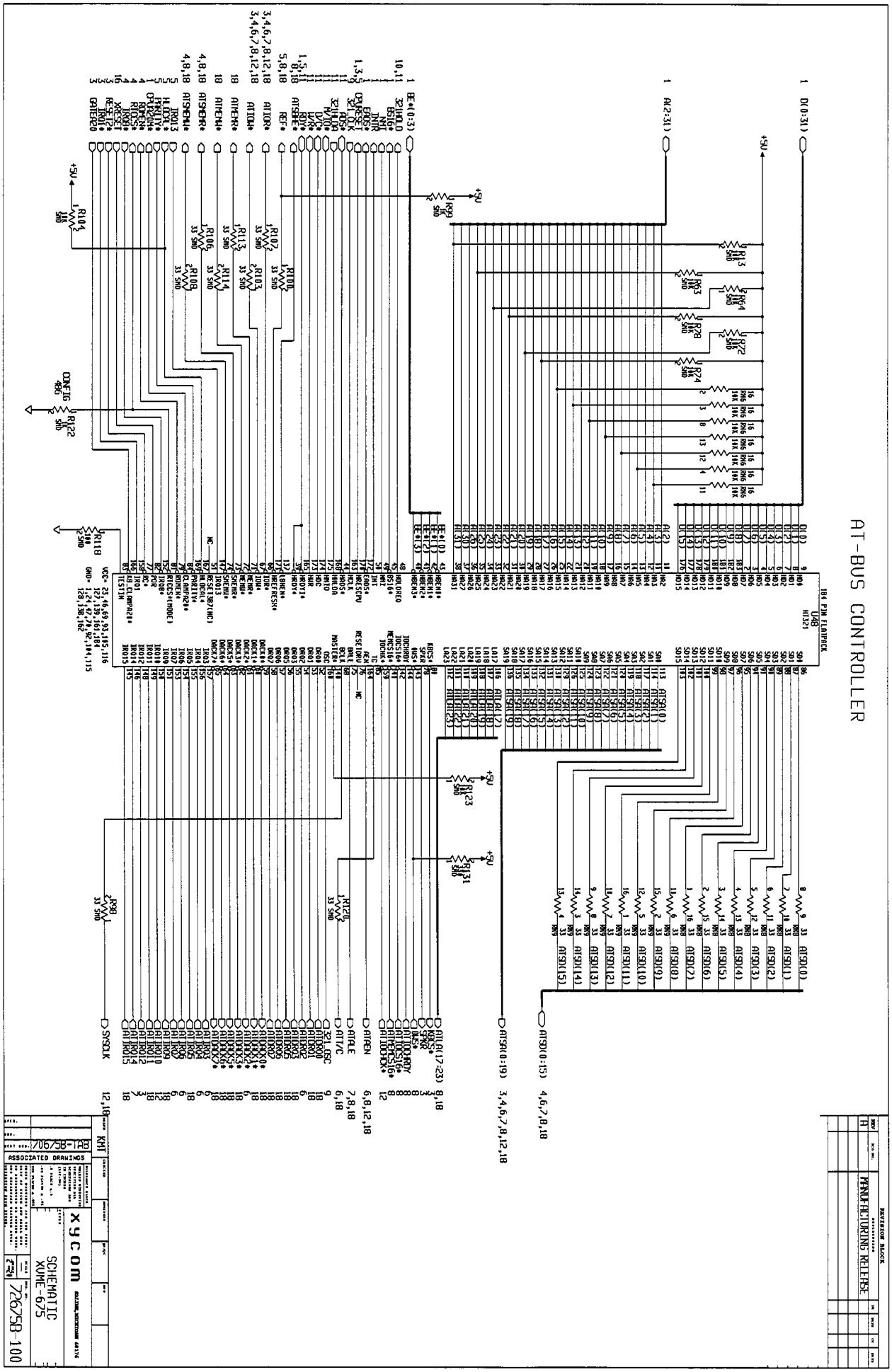
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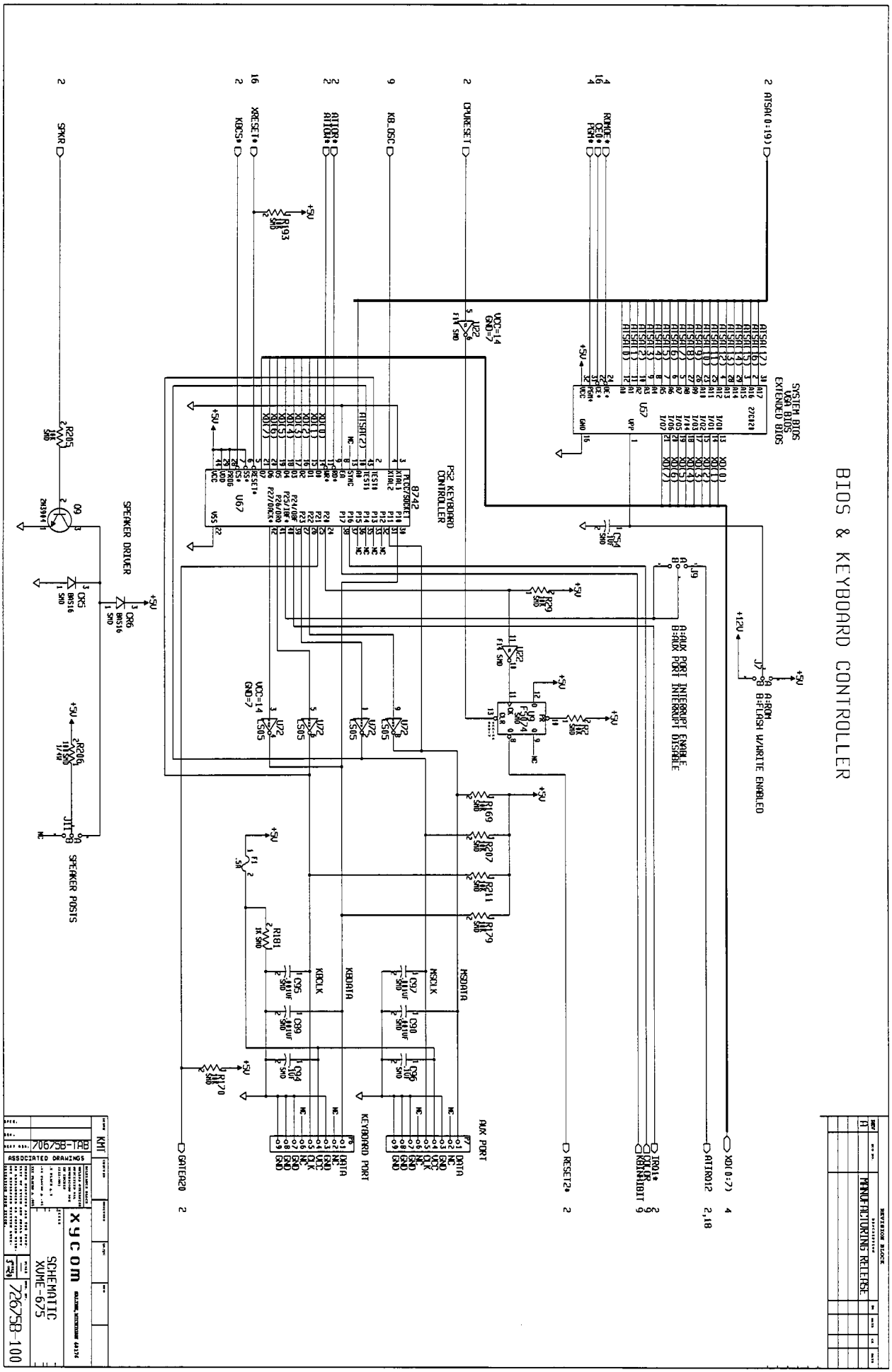
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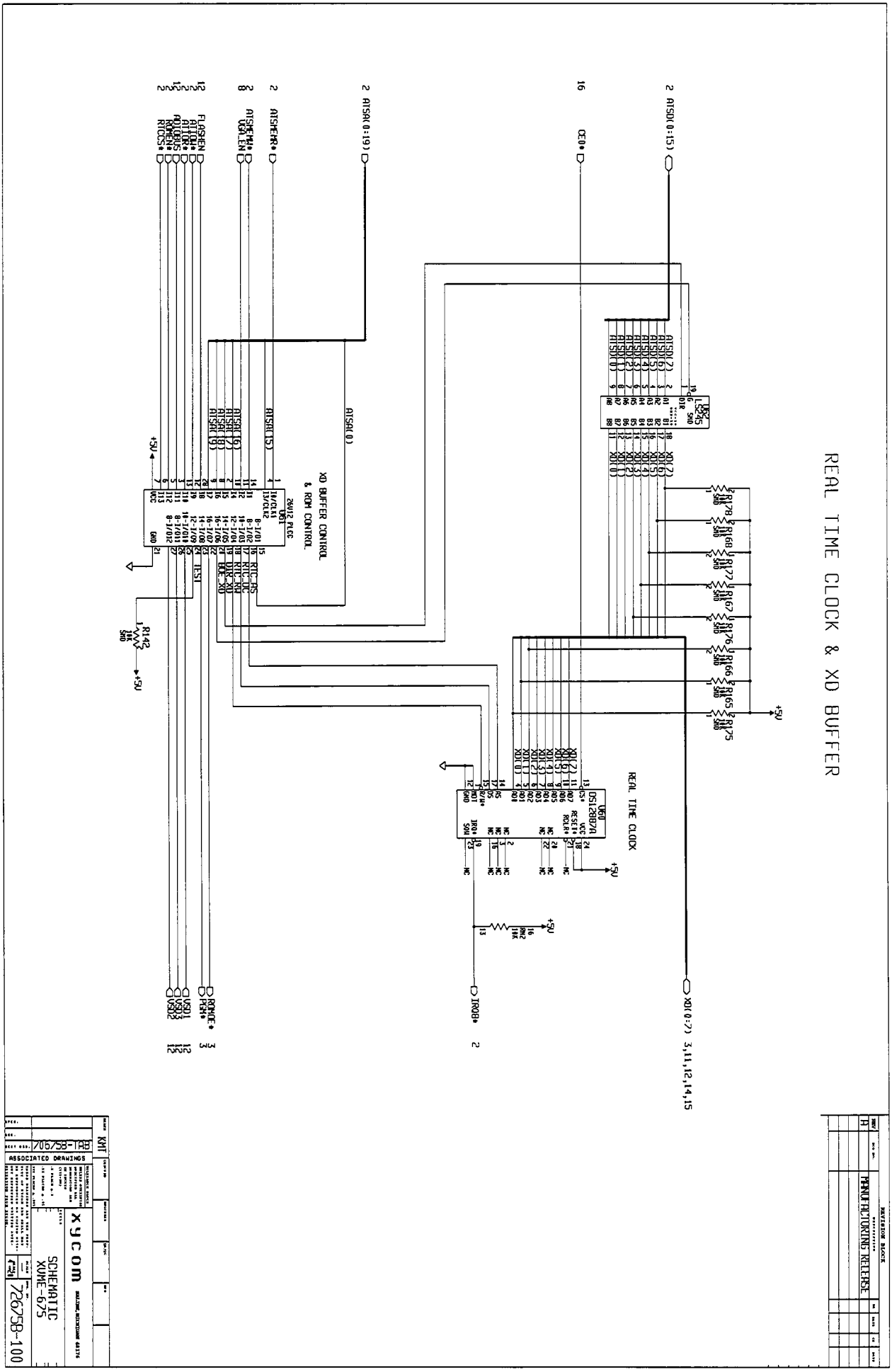
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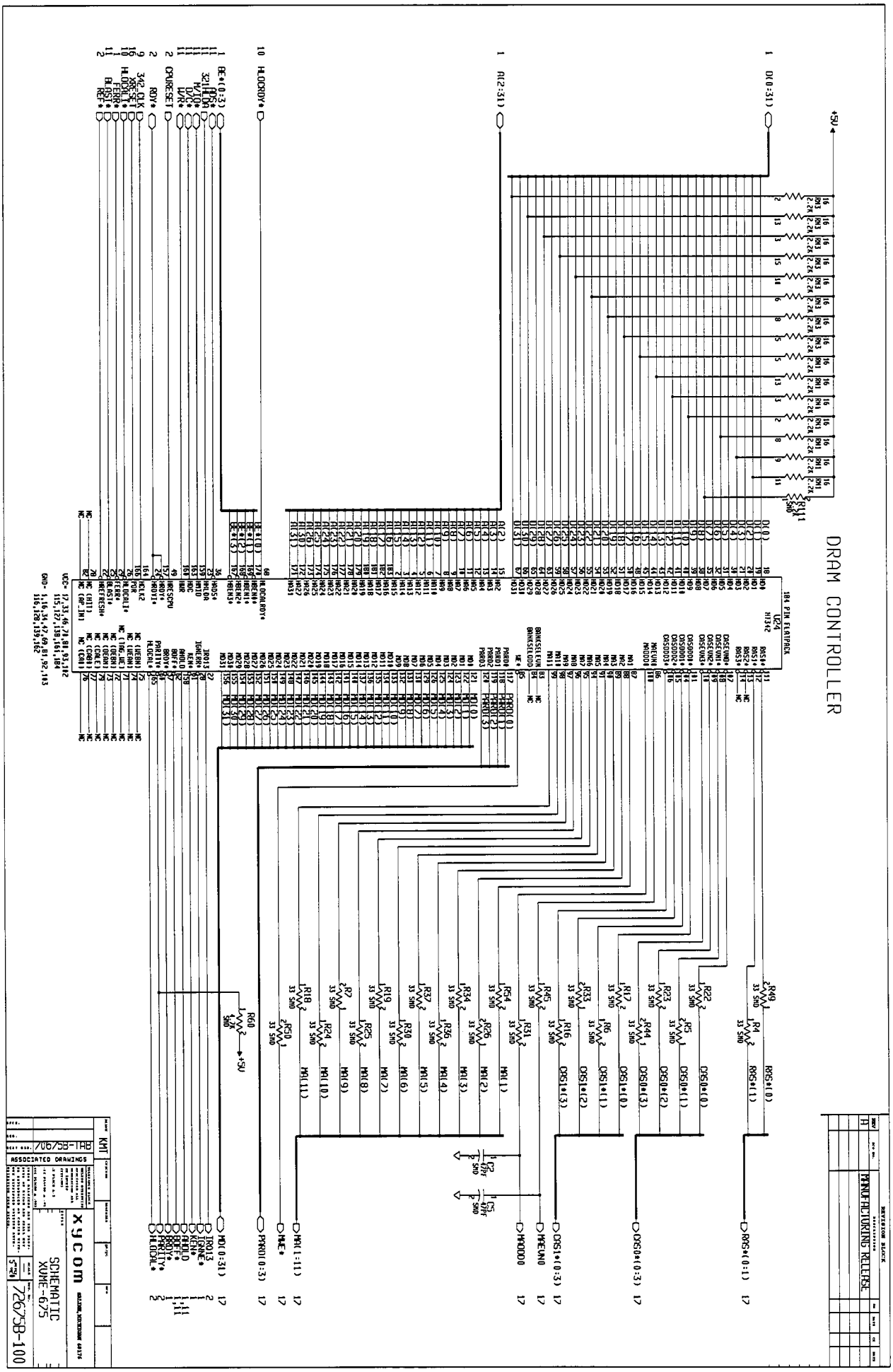
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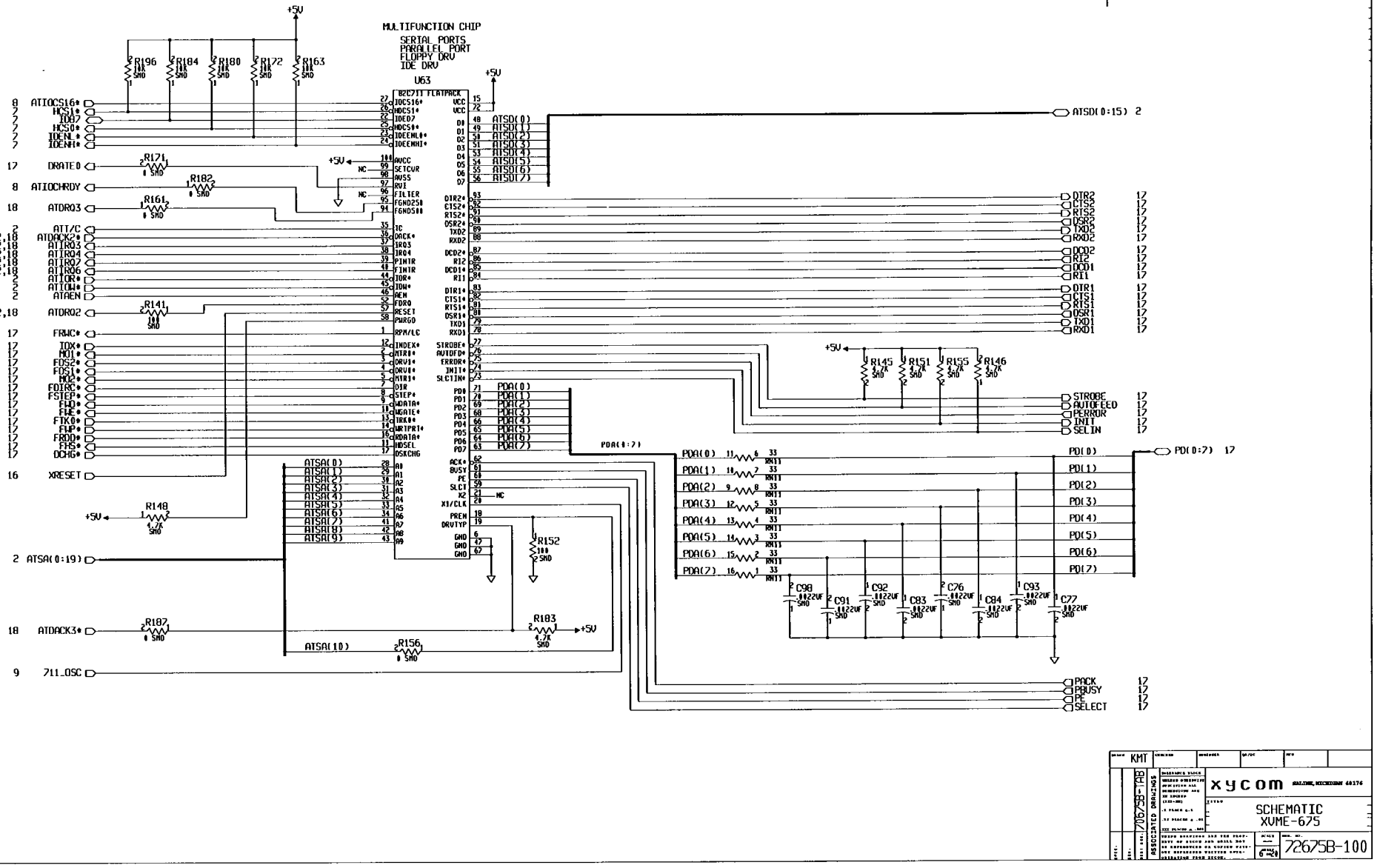


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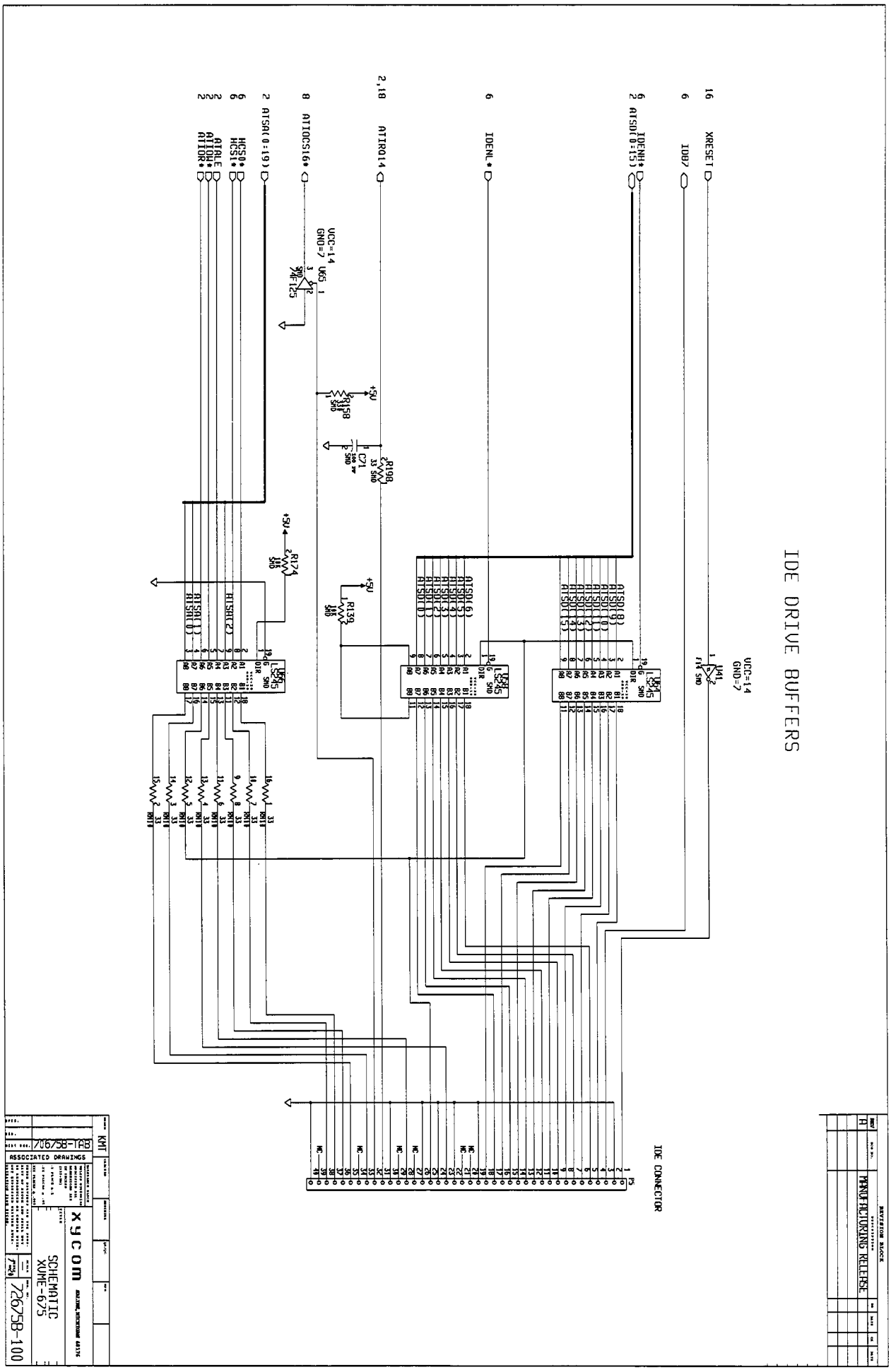
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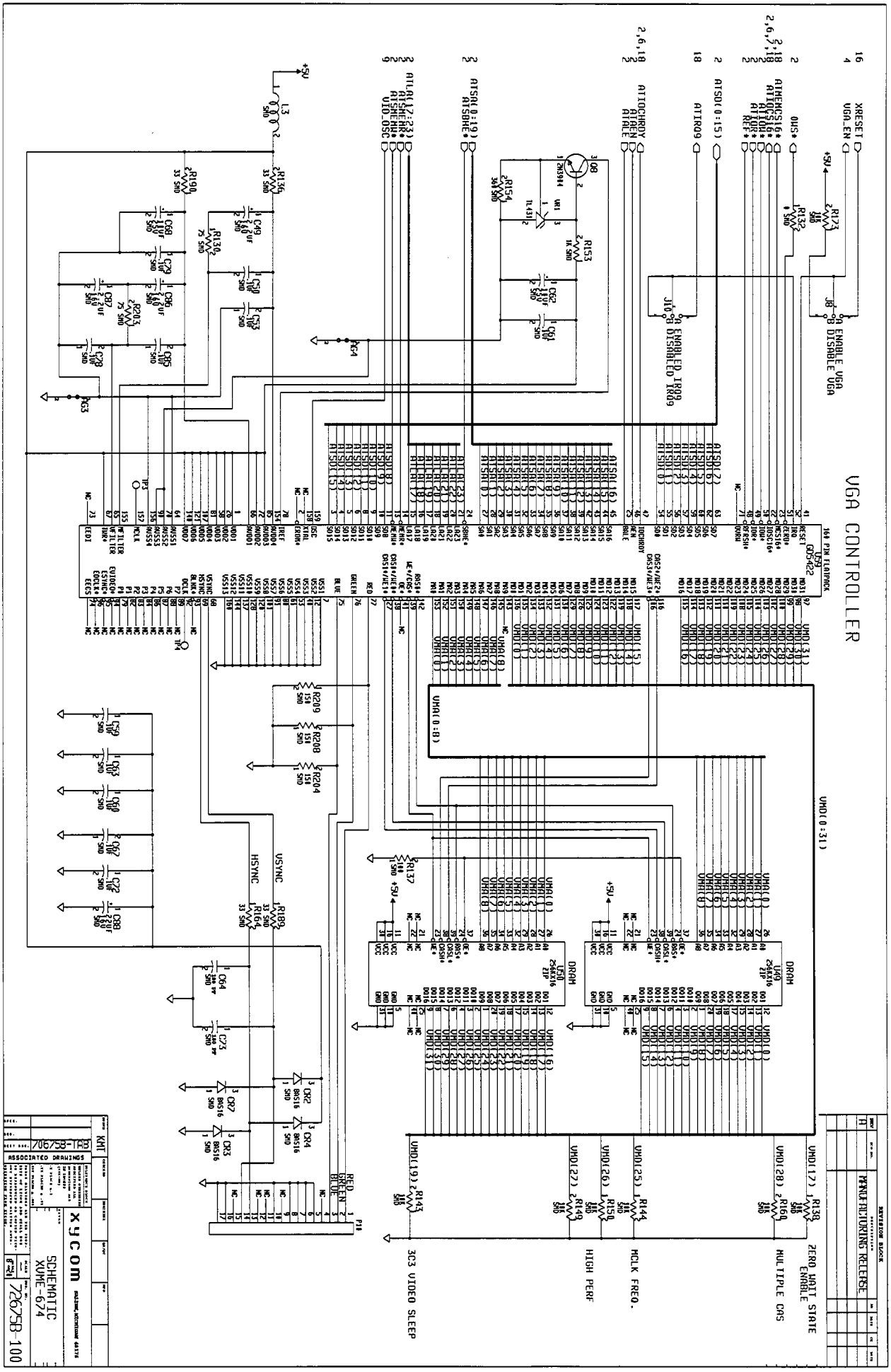


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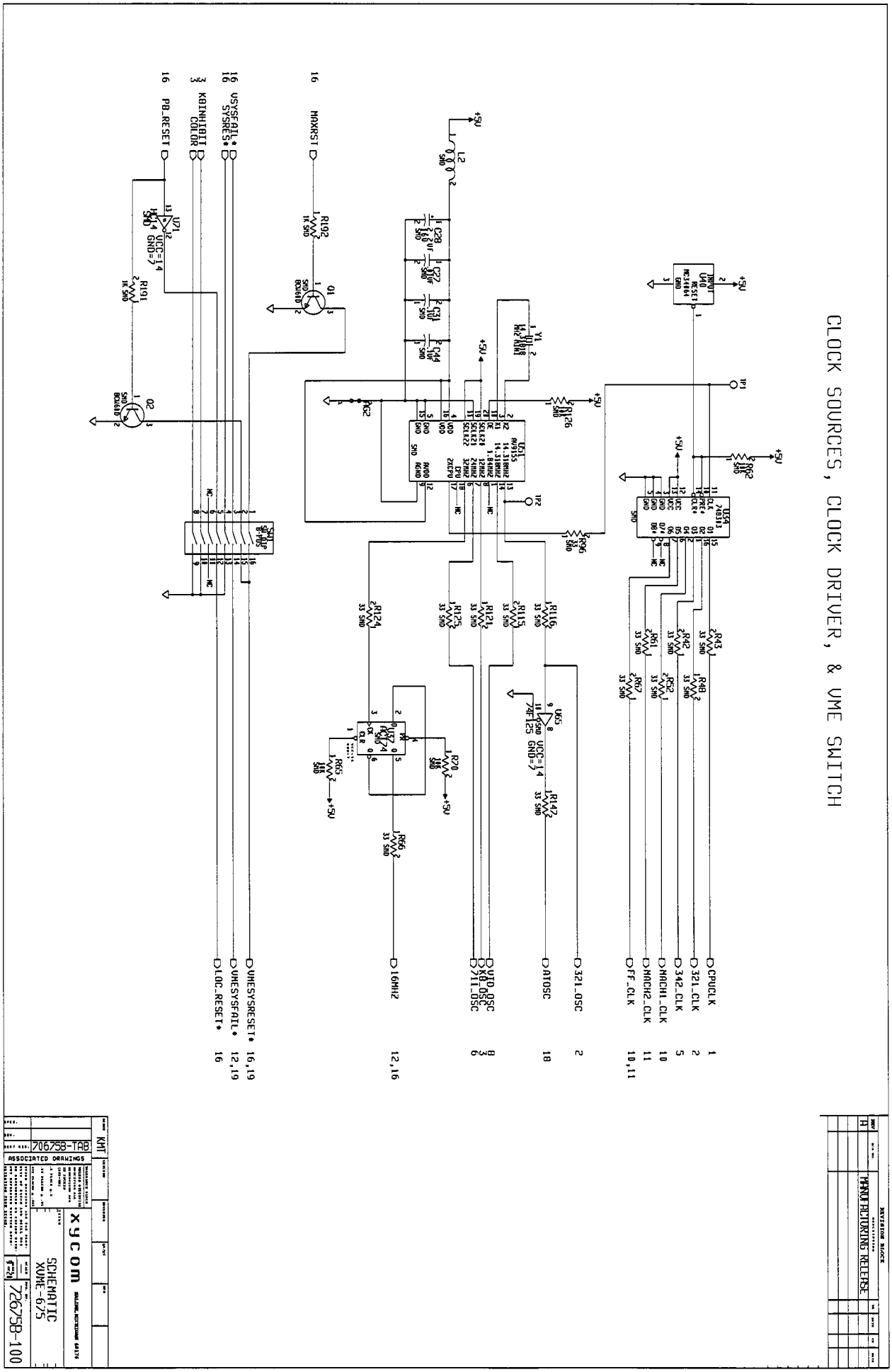
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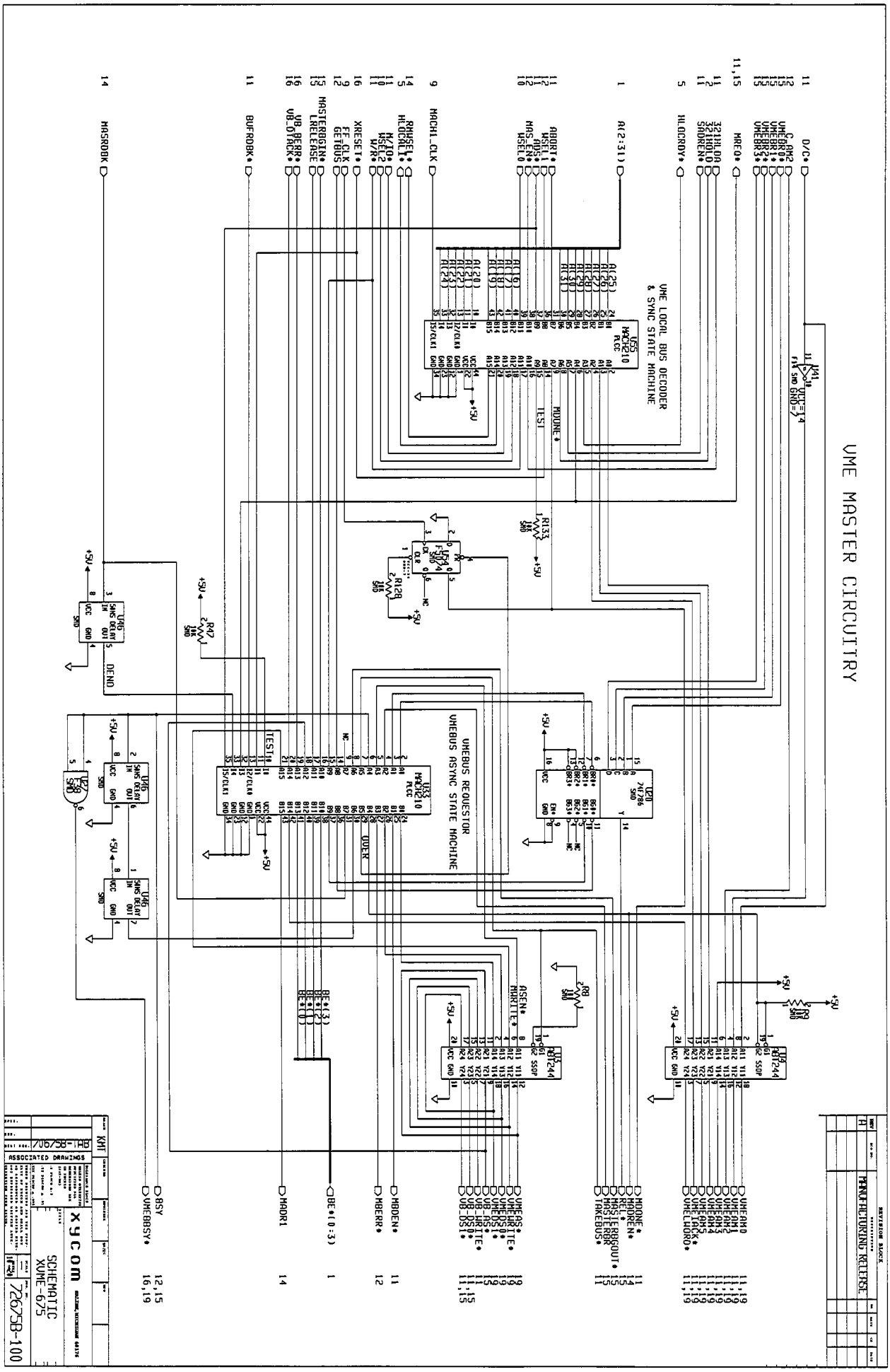
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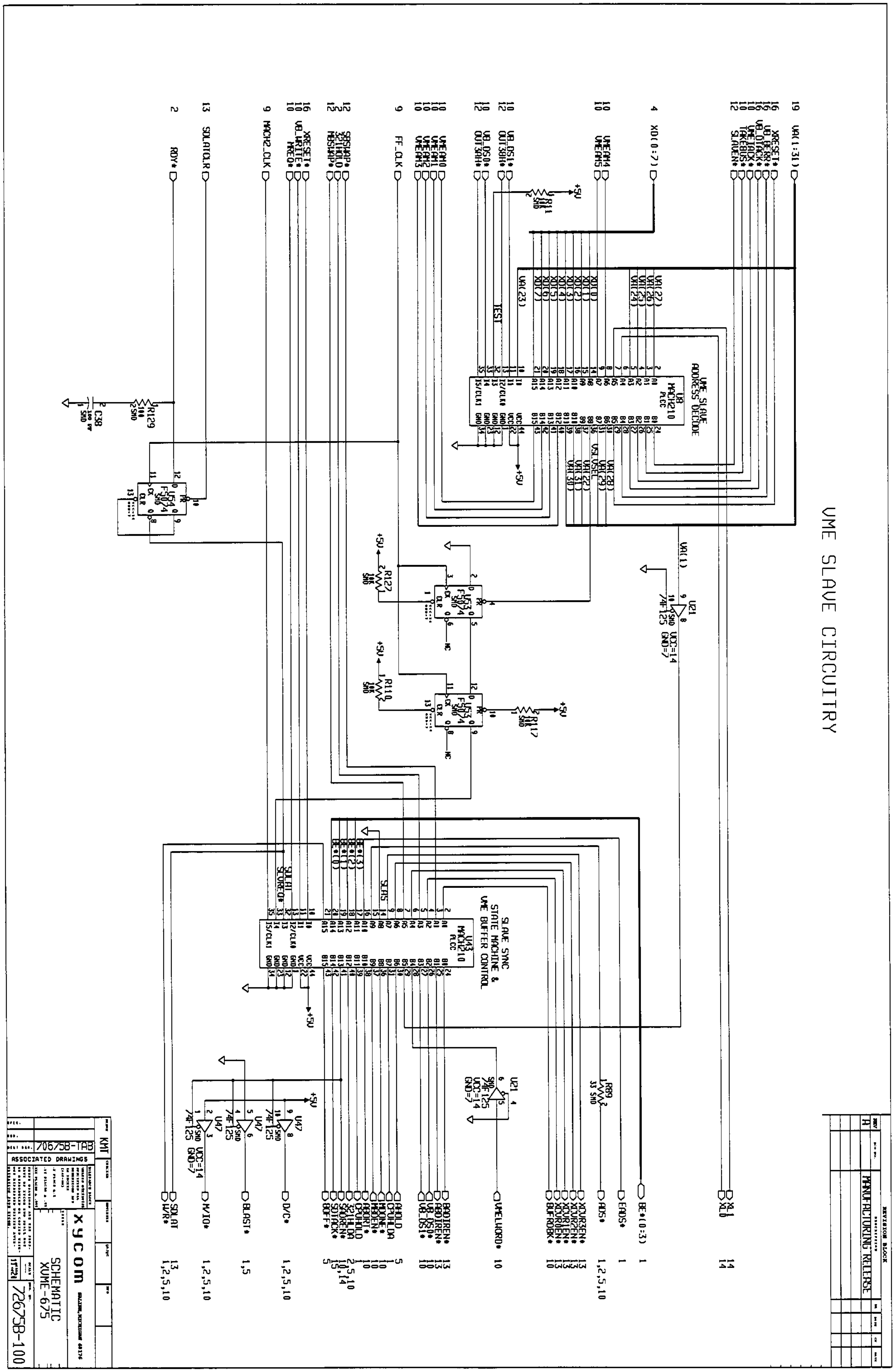
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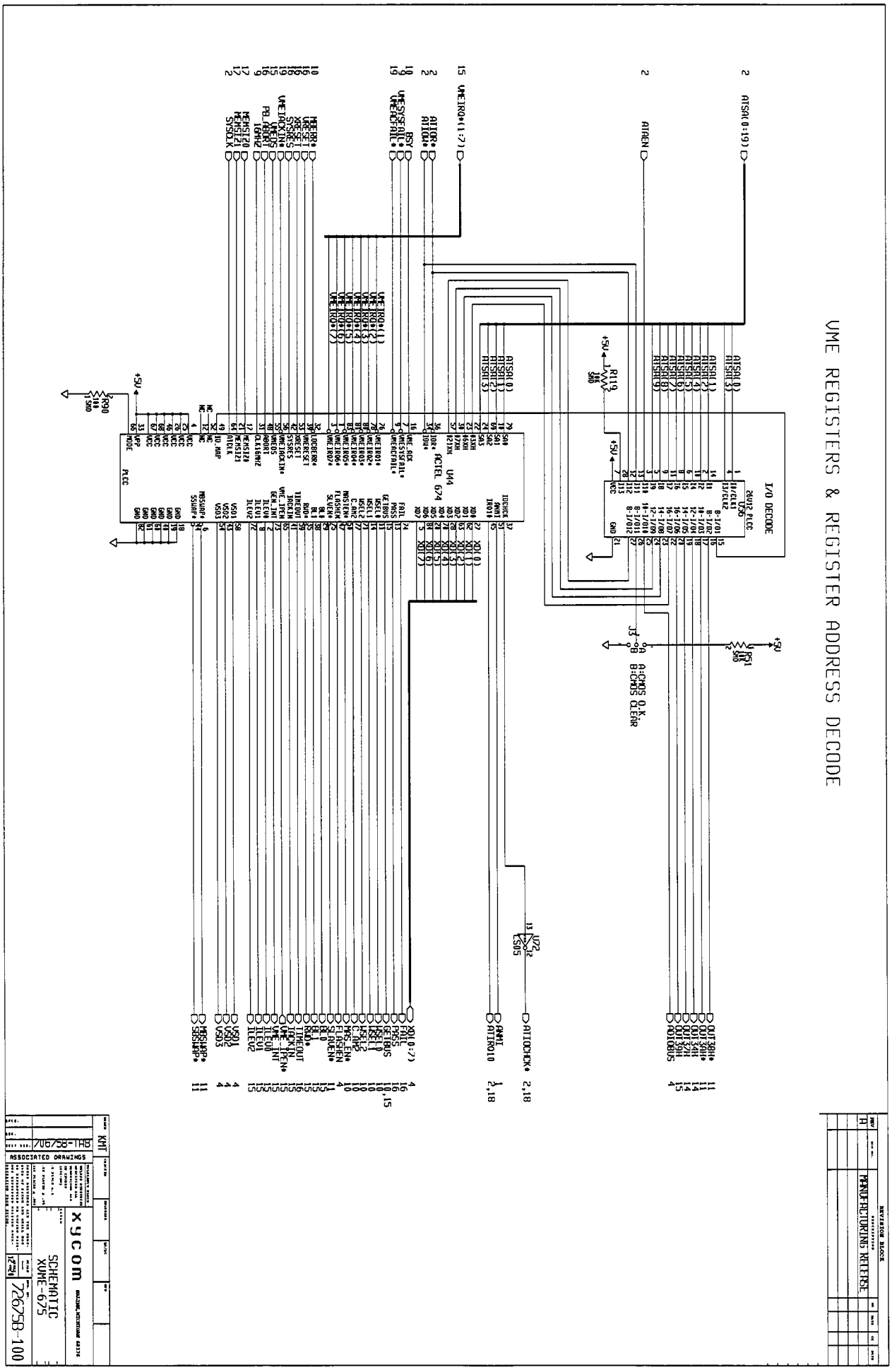
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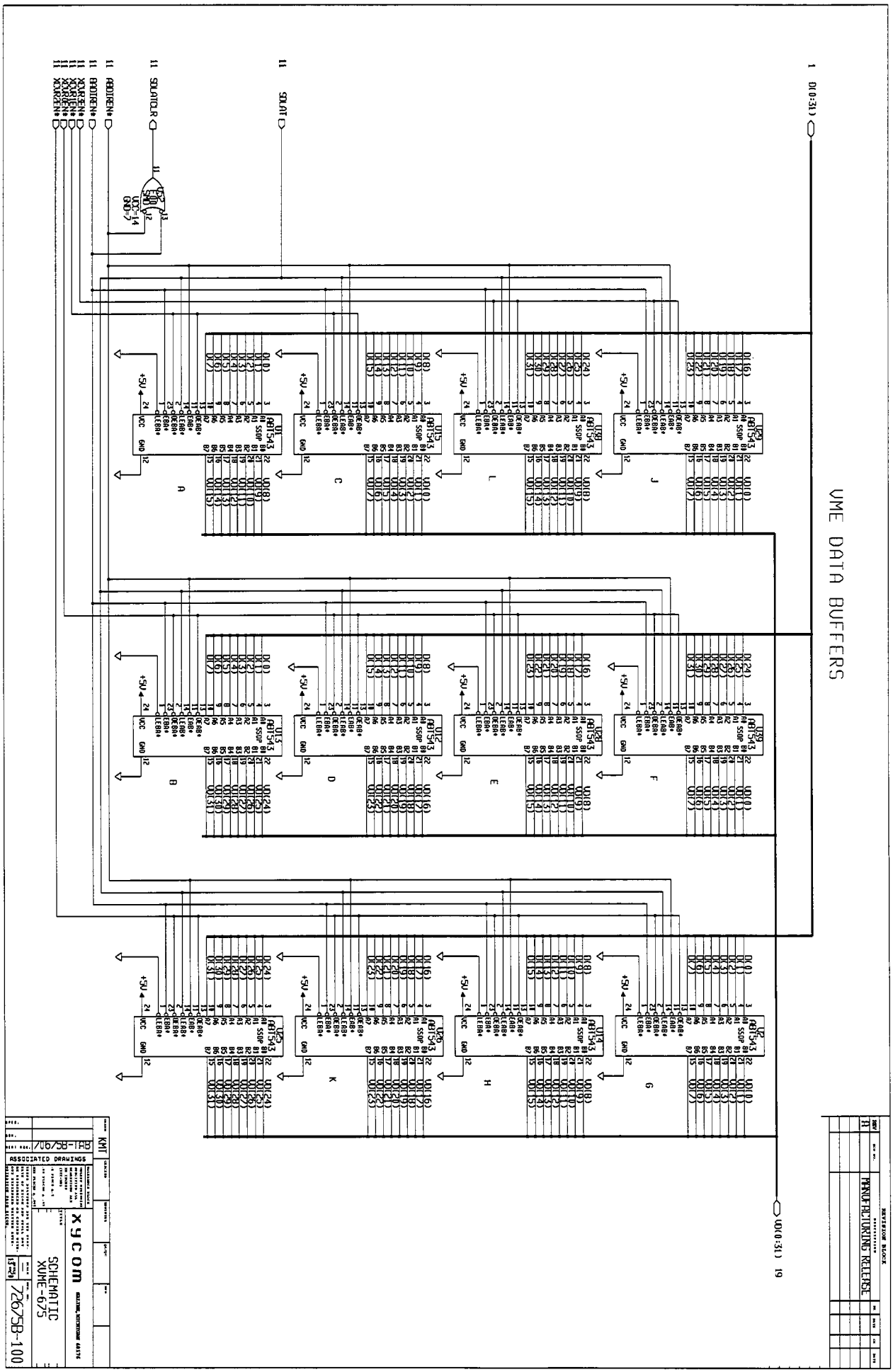
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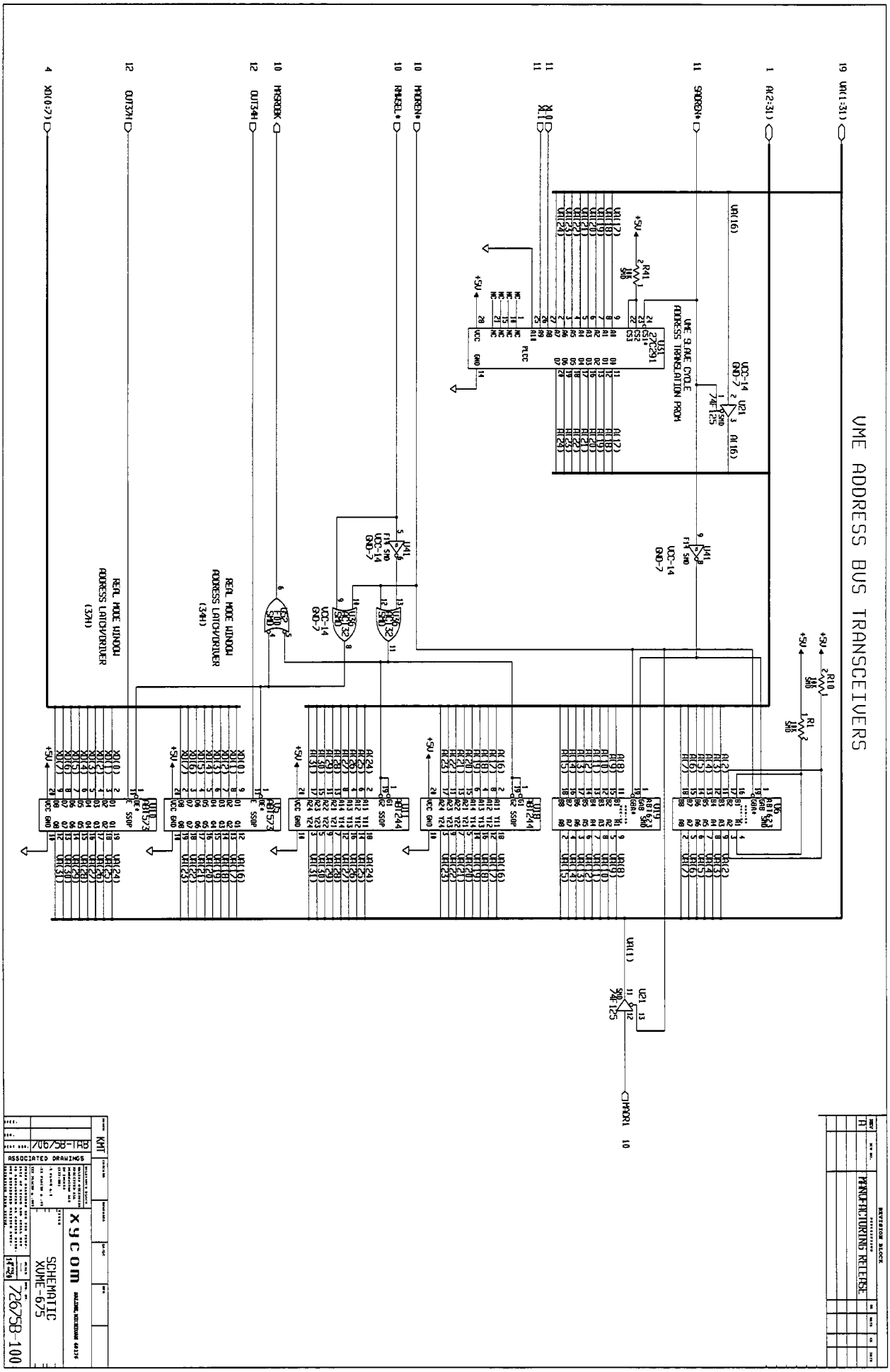
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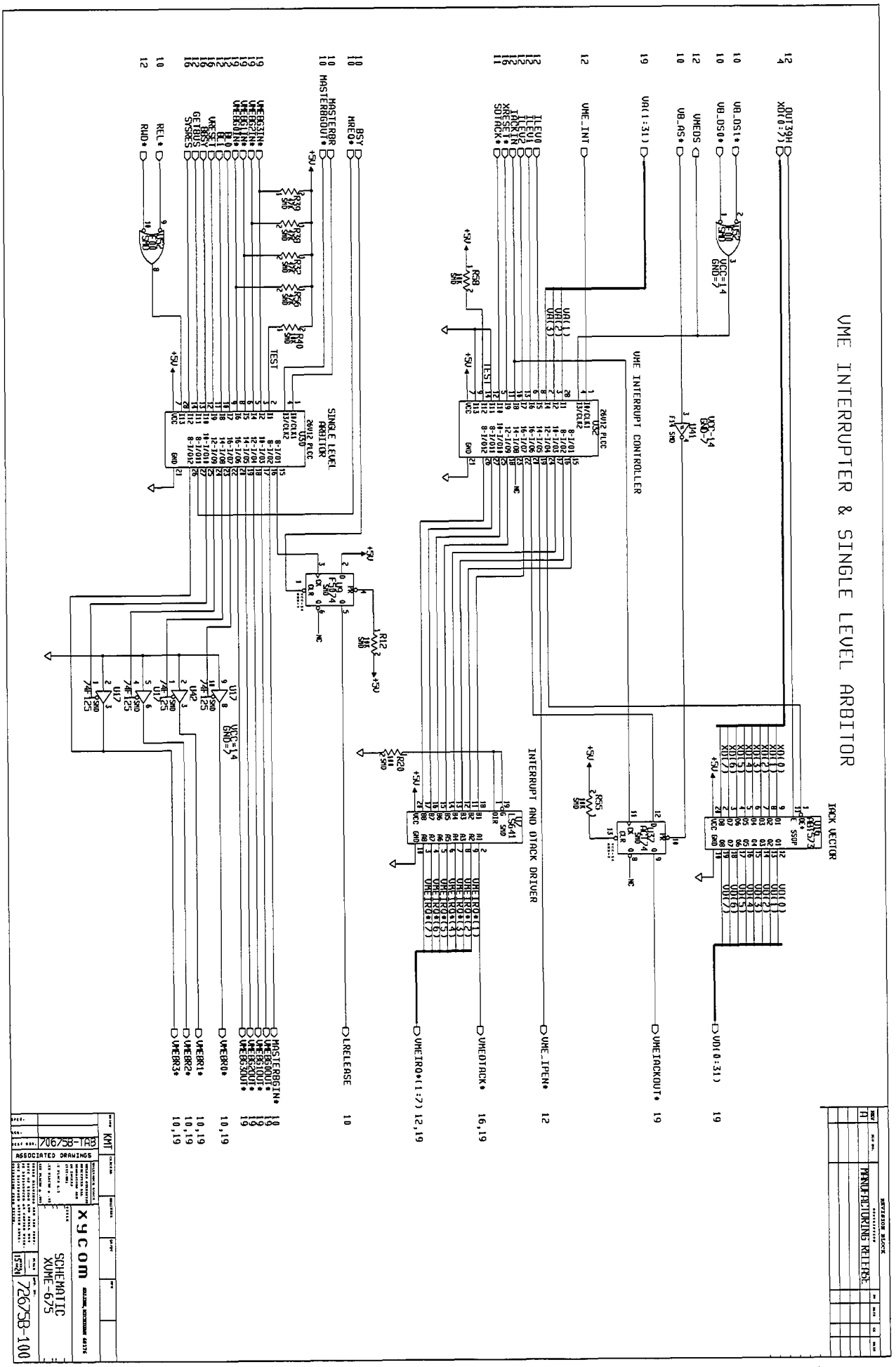
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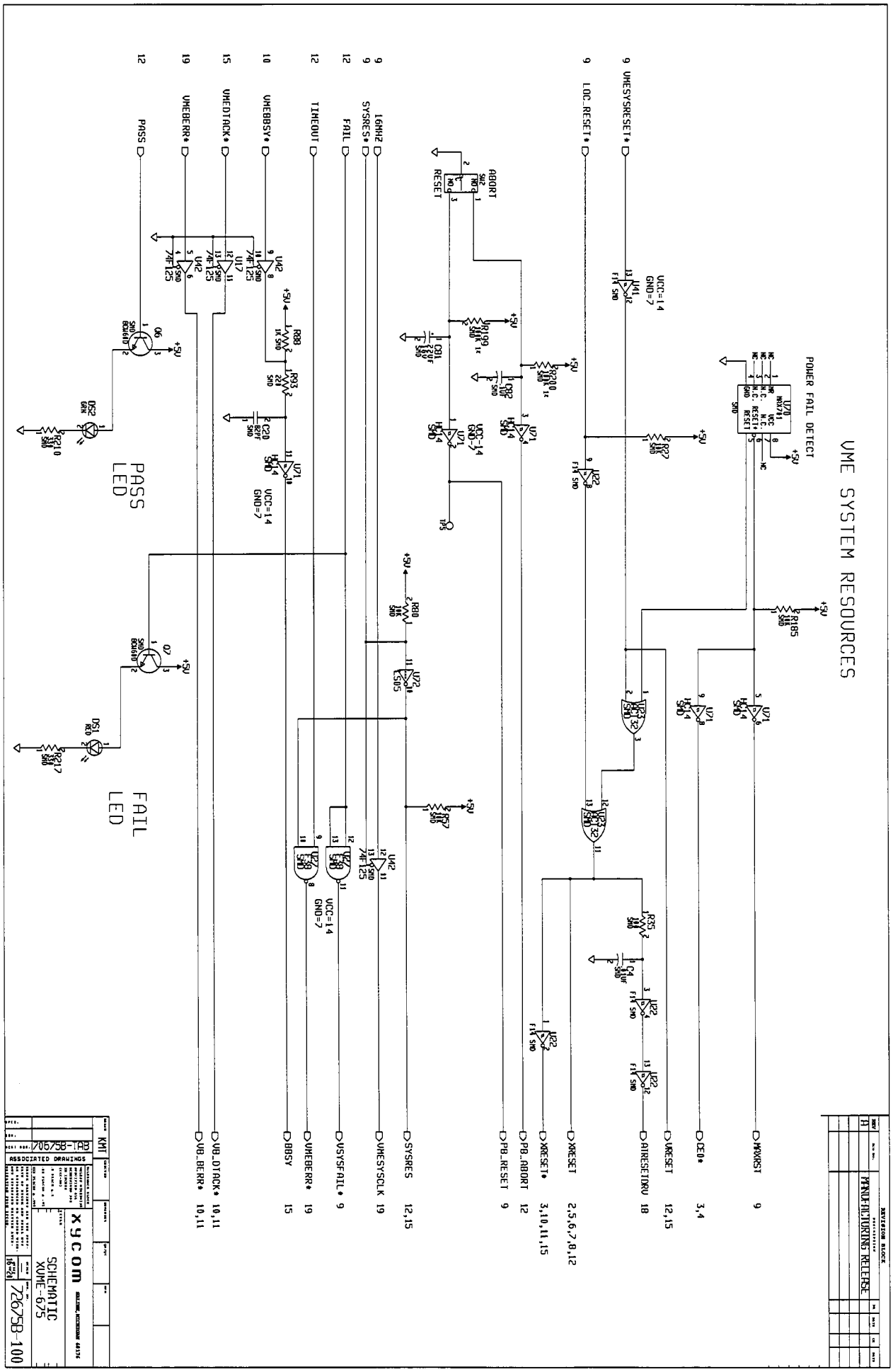
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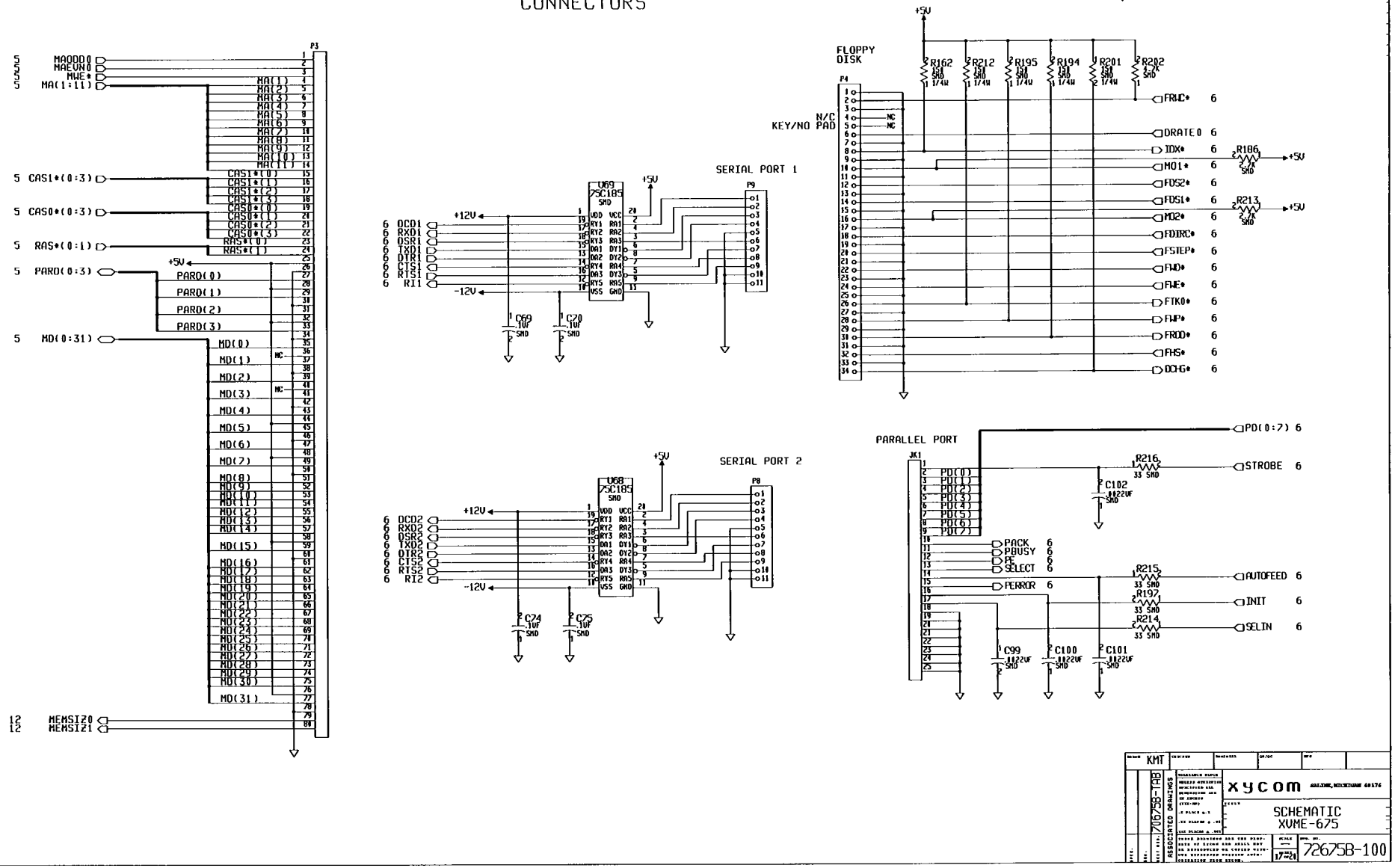


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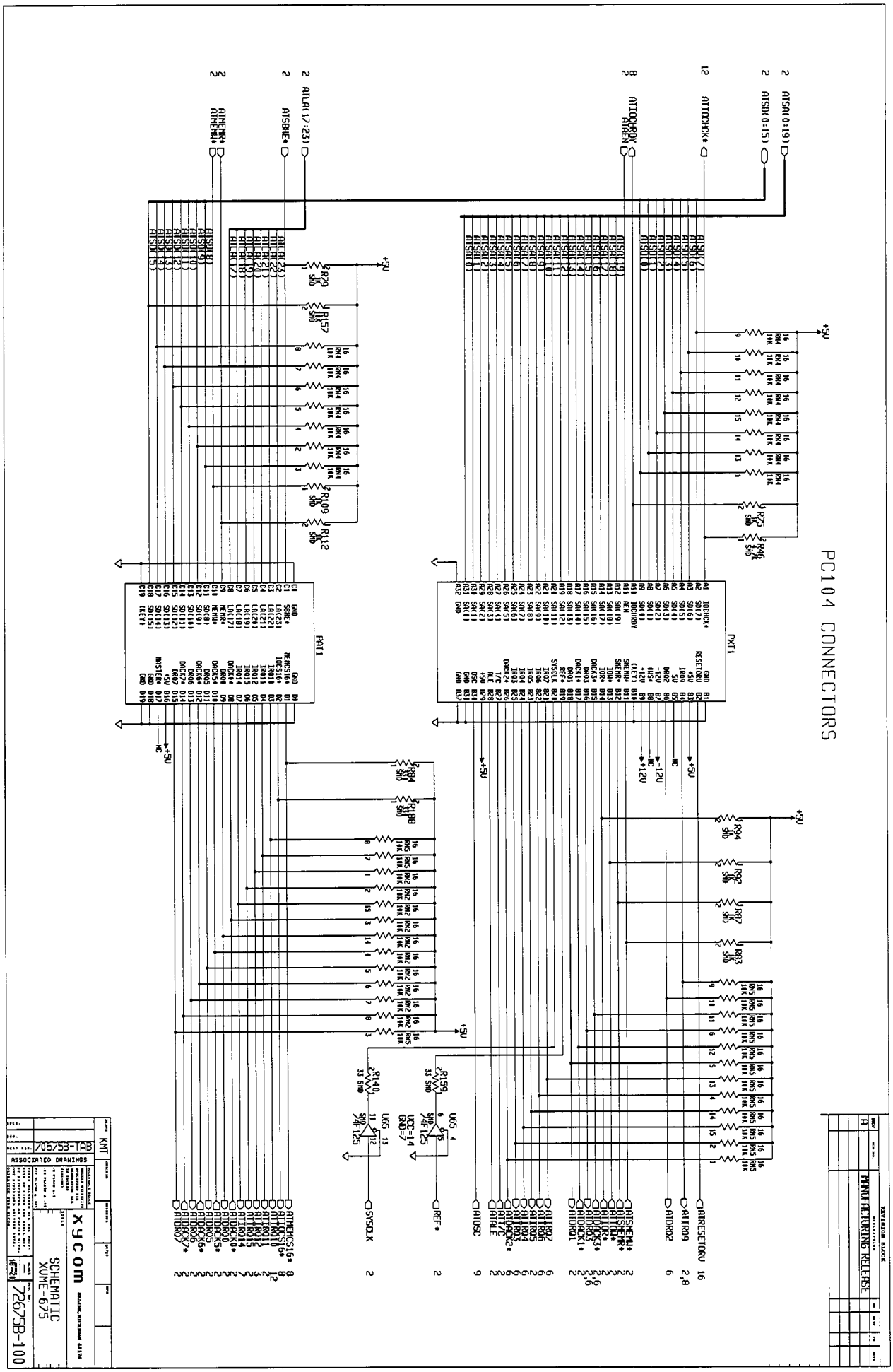
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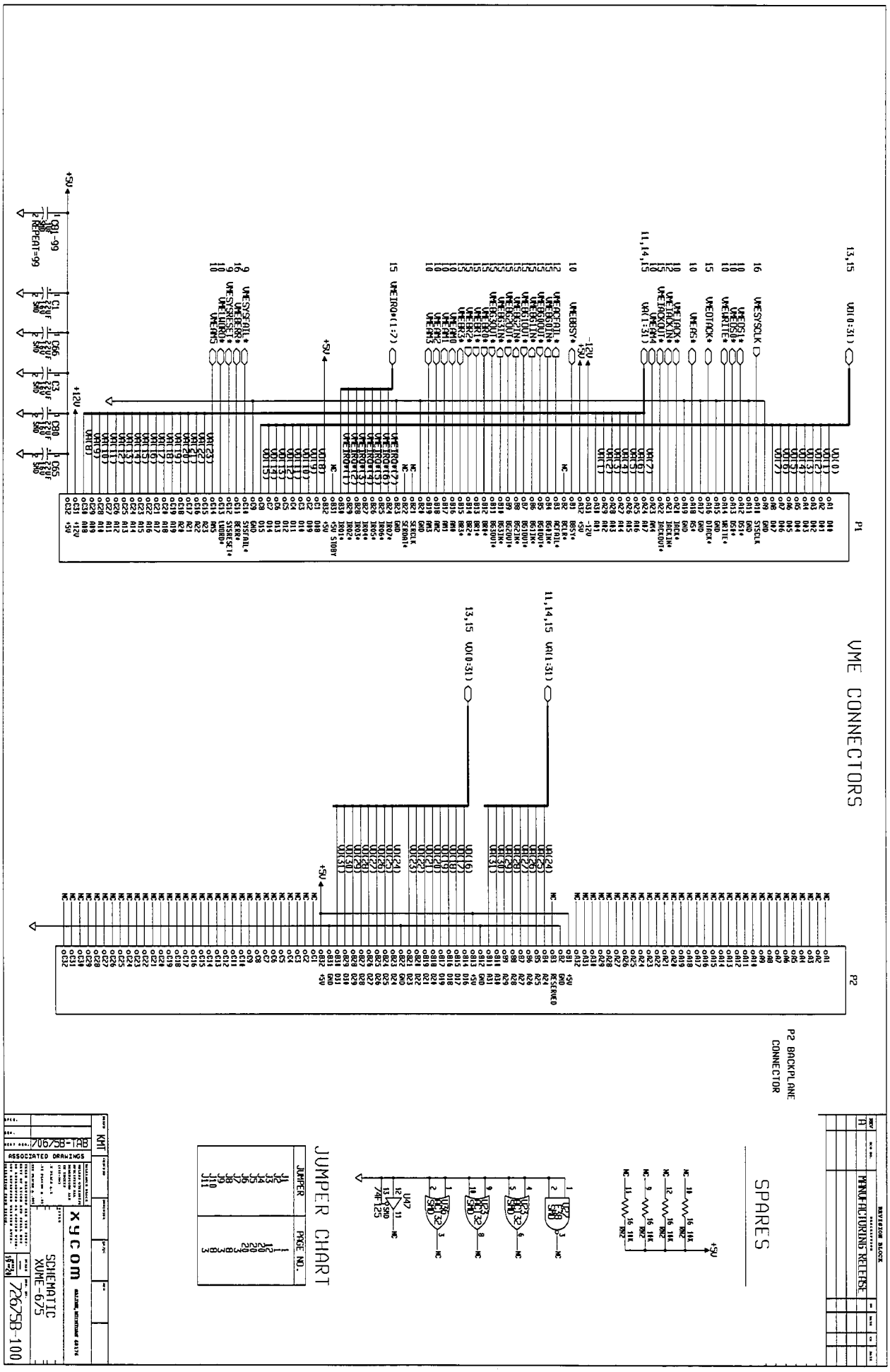


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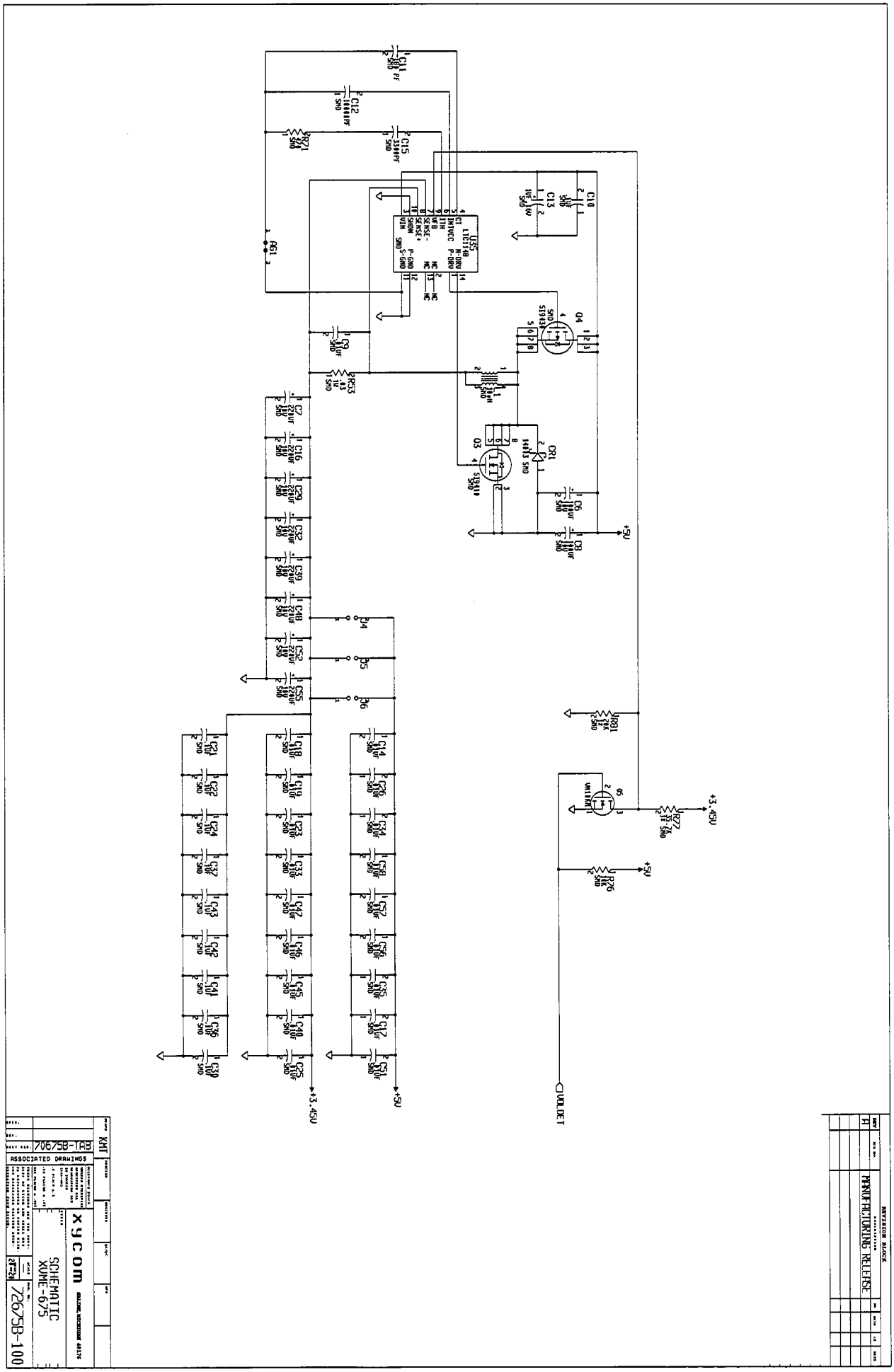
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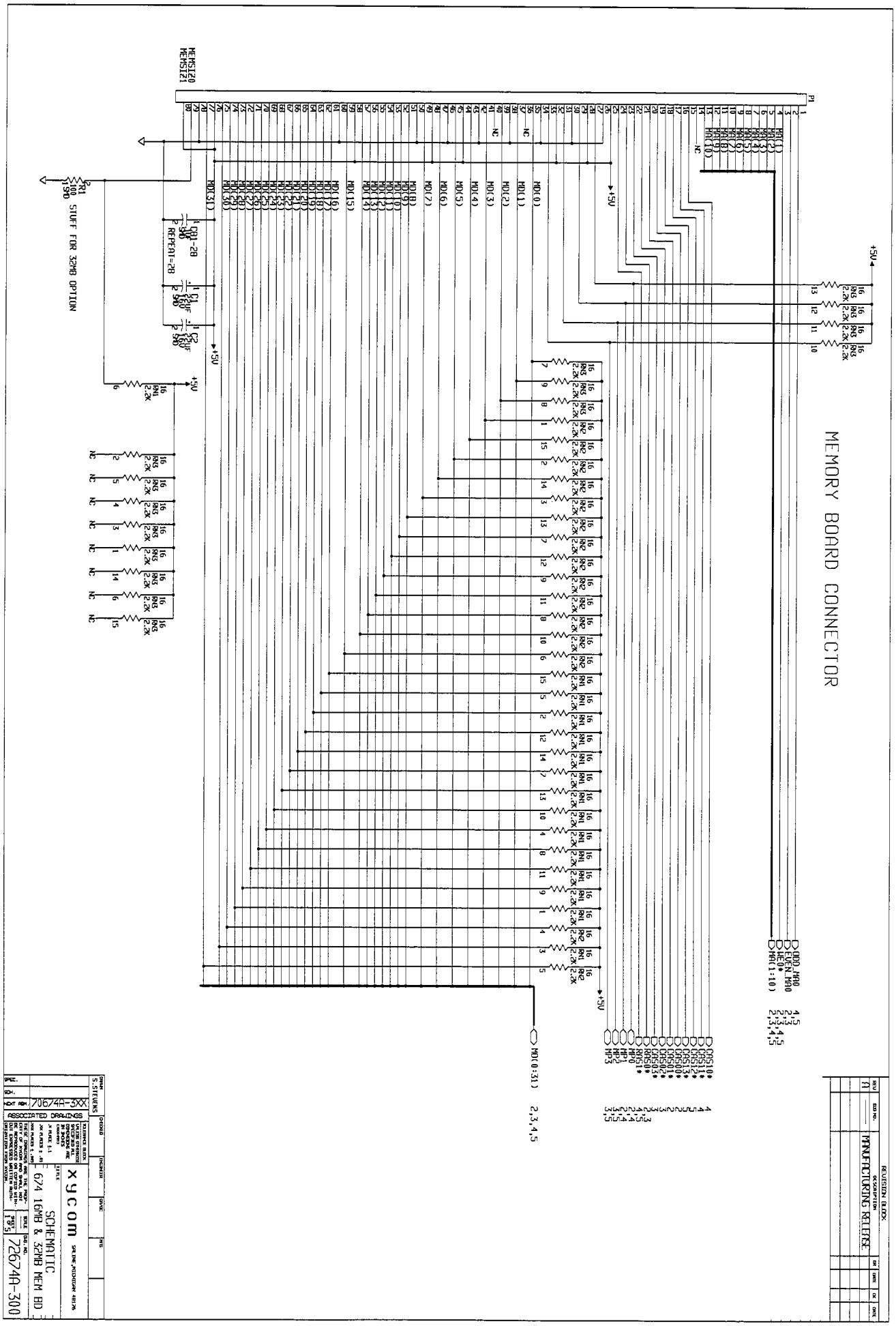
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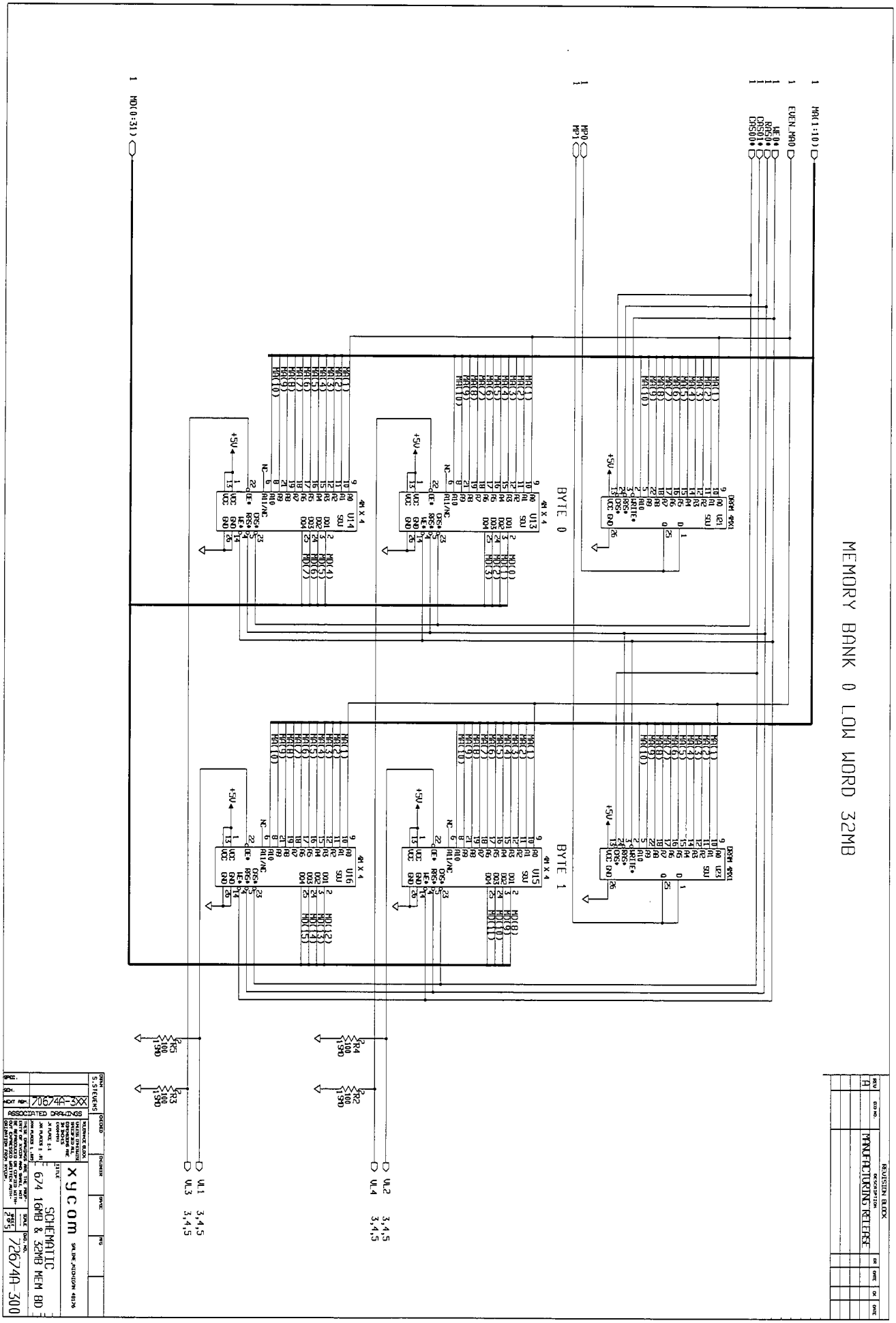
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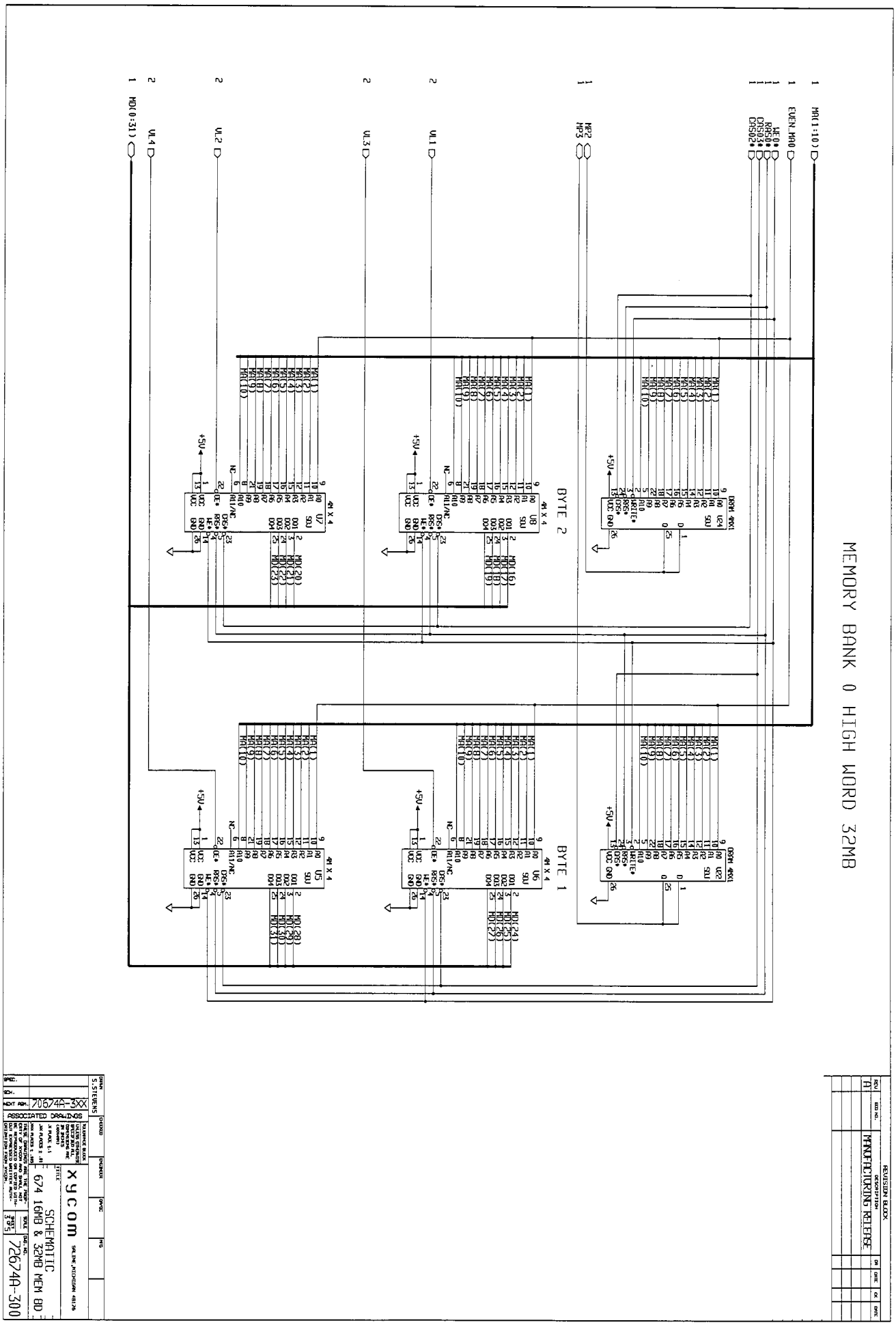
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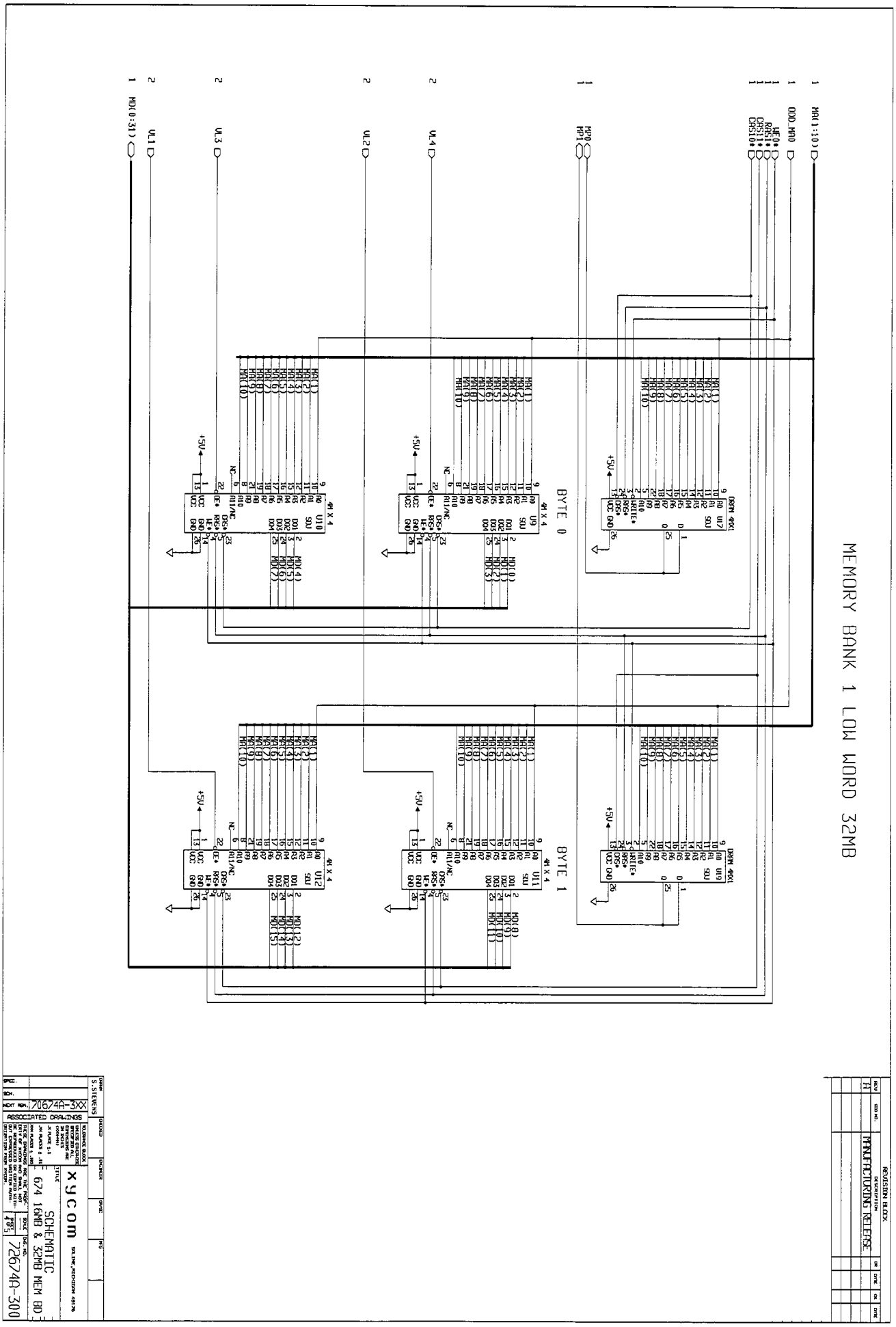
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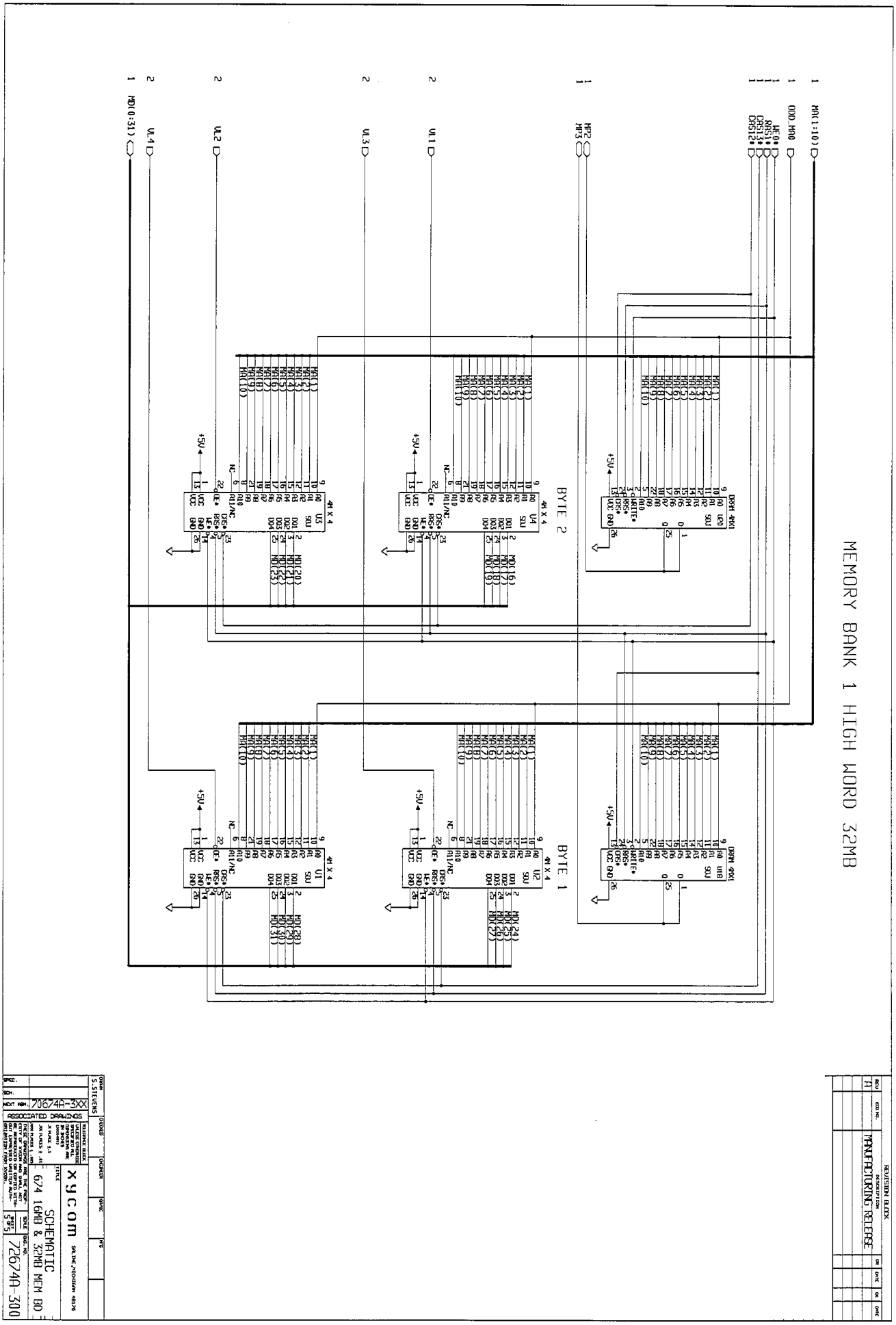
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