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Hardware User Guide

Cable Hardware

MutliLINX™ Cable

FPGA Design Demonstration Board

CPLD Design Demonstration Board

Glossary



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5,737,631; 5,742,178; 5,742,531; 5,744,974; 5,744,979; 5,744,995; 5,748,942; 5,748,979; 5,752,006; 5,752,035; 5,754,459; 5,758,192; 5,760,603; 5,760,604; 5,760,607; 5,761,483; 5,764,076; 5,764,534; 5,764,564; 5,768,179; 5,770,951; 5,773,993; 5,778,439; 5,781,756; 5,784,313; 5,784,577; 5,786,240; 5,787,007; 5,789,938; 5,790,479; 5,790,882; 5,795,068; 5,796,269; 5,798,656; 5,801,546; 5,801,547; 5,801,548; 5,811,985; 5,815,004; 5,815,016; 5,815,404; 5,815,405; 5,818,255; 5,818,730; 5,821,772; 5,821,774; 5,825,202; 5,825,662; 5,825,787; 5,828,230; 5,828,231; 5,828,236; 5,828,608; 5,831,448; 5,831,460; 5,831,845; 5,831,907; 5,835,402; 5,838,167; 5,838,901; 5,838,954; 5,841,296; 5,841,867; 5,844,422; 5,844,424; 5,844,829; 5,844,844; 5,847,577; 5,847,579; 5,847,580; 5,847,993; 5,852,323; 5,861,761; 5,862,082; 5,867,396; 5,870,309; 5,870,327; 5,870,586; 5,874,834; 5,875,111; 5,877,632; 5,877,979; 5,880,492; 5,880,598; 5,880,620; 5,883,525; 5,886,538; 5,889,411; 5,889,413; 5,889,701; 5,892,681; 5,892,961; 5,894,420; 5,896,047; 5,896,329; 5,898,319; 5,898,320; 5,898,602; 5,898,618; 5,898,893; 5,907,245; 5,907,248; 5,909,125; 5,909,453; 5,910,732; 5,912,937; 5,914,514; 5,914,616; 5,920,201; 5,920,202; 5,920,223; 5,923,185; 5,923,602; 5,923,614; 5,928,338; 5,931,962; 5,933,023; 5,933,025; 5,933,369; 5,936,415; 5,936,424; 5,939,930; 5,942,913; 5,944,813; 5,945,837; 5,946,478; 5,949,690; 5,949,712; 5,949,983; 5,949,987; 5,952,839; 5,952,846; 5,955,888; 5,956,748; 5,958,026; 5,959,821; 5,959,881; 5,959,885; 5,961,576; 5,962,881; 5,963,048; 5,963,050; 5,969,539; 5,969,543; 5,970,142; 5,970,372; 5,971,595; 5,973,506; 5,978,260; 5,986,958; 5,990,704; 5,991,523; 5,991,788; 5,991,880; 5,991,908; 5,995,419; 5,995,744; 5,995,988; 5,999,014; 5,999,025; 6,002,282; and 6,002,991; Re. 34,363, Re. 34,444, and Re. 34,808. Other U.S. and foreign patents pending. Xilinx, Inc. does not represent that devices shown or products described herein are free from patent infringement or from any other third party right. Xilinx, Inc. assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made. Xilinx, Inc. will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

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About This Manual

This manual describes the function and operation of Xilinx hardware devices, which include the following.

- Cables for downloading designs
- MultiLINX™ Cable specific information
- FPGA Design Demonstration board for design verification
- CPLD Design Demonstration board for design verification

Before using this manual, you should be familiar with the operations that are common to all Xilinx software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *2.1i Quick Start Guide.* Other publications you can consult for related information are the *Hardware Debugger Guide* and the *JTAG Programmer Guide.*

Manual Contents

This manual covers the following topics.

- Chapter 1, “Cable Hardware”provides specific information about using the MultiLINX™ Cable, Parallel Cable III and XChecker™ cables to configure CPLDs and FPGAs.
- Chapter 2, “MutliLINX™ Cable”provides detailed information about the MultiLINX Cable, Flying Wires and Operation Modes.
- Chapter 3, “FPGA Design Demonstration Board”describes the function and operation of the FPGA Demonstration Board.

- Chapter 4, “CPLD Design Demonstration Board”describes the function and operation of this board, which is used for demonstrating the In-system Programming (ISP) capabilities of the XC9500 CPLD family.
- “Glossary”defines all the terms you should understand to use Xilinx Hardware.

Additional Resources

For additional information, go to `http://support.xilinx.com`. The following table lists some of the resources you can access from this Web site. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging `http://support.xilinx.com/support/techsup/tutorials/index.htm`
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at `http://support.xilinx.com/support/searchtd.htm`
Application Notes	Descriptions of device-specific design techniques and approaches `http://support.xilinx.com/apps/appsweb.htm`
Data Book	Pages from *The Programmable Logic Data Book*, which contain device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging `http://support.xilinx.com/partinfo/databook.htm`
Xcell Journals	Quarterly journals for Xilinx programmable logic users `http://support.xilinx.com/xcell/xcell.htm`
Technical Tips	Latest news, design tips, and patch information for the Xilinx design environment `http://support.xilinx.com/support/techsup/journals/index.htm`

Conventions

This manual uses the following conventions. An example illustrates each convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: - 100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  ```
  rpt_del_net=
  ```

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *`design_name`*

  - References to other manuals

See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd *[option_name] design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={on|off}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={on|off}

- A vertical ellipsis indicates repetitive material that has been omitted.

  ```
  IOB #1: Name = QOUT'
  IOB #2: Name = CLKIN'
  .
  .
  .
  ```

- A horizontal ellipsis "...." indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.

- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

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Chapter 1

Cable Hardware

This chapter gives specific information about connecting and using the In System Programming (ISP) Download Cables. These cables can be used to configure FPGAs and CPLDs. The following sections are in this chapter.

- "Cable Overview"
- "Cable Baud Rates"
- "MultiLINX Cable and Flying Leads"
- "External Power for the MultiLINX Cable"
- "Parallel Cable III"
- "XChecker Cable"
- "Download Cable Schematic"

Cable Overview

There are three cables available for use with Xilinx Alliance and Foundation software. The MultiLINX Cable supports USB and RS-232 serial port connections, the Parallel Cable III supports parallel port, and the XChecker Cable supports RS-232 serial ports.

Selecting a Cable

Determine the most suitable cable to use, depending upon the tasks you wish to perform.

MultiLINX Cable

You can use the MultiLINX Cable to download and readback your Xilinx programmable logic device. The MultiLINX cable hardware

communicates with the host through the Universal Serial Bus (USB) port or an RS-232 interface. The additional flying wires support the various configuration modes available on Xilinx configuration cables.

Parallel Cable

The Parallel Cable III connects to the parallel printer port of a PC. This cable can be used to download and readback configuration data via JTAG.

XChecker Cable

The XChecker Cable connects to the serial port of both workstations and PCs. This cable can be used for design verification and debugging in addition to data download and readback.

Note Always set the configuration mode of the device being configured to slave serial, no matter which cable you use.

Table 1-1 Cable Support

Name	Function	Platform
MultiLINX Cable (Model: DLC6)	Download, Readback	PC, Workstation
Parallel Cable III (Model: DLC5)	Download Only	PC
XChecker Cable (Model: DLC4)	Download, Readback, and Debug	PC, Workstation

Software Support

Make sure that you use the appropriate configuration software for your device type.

- JTAG Programmer Software is used to configure FPGAs and CPLDs, and supports both the XChecker and the Parallel Cable III. This is a GUI based program.
- Hardware Debugger Software supports the MultiLINX, Parallel, and XChecker download cables and is used for FPGA configuration. This is a GUI based program with a waveform viewer.

Note All Hardware Debugger Software versions prior to 2.1i do not support the MultiLINX Cable. The Hardware Debugger Software only supports the MultiLINX Cable in the 2.1i release.

For specific information on using the download cables with the Hardware Debugger Software, see the *Hardware Debugger Guide*. Consult the *JTAG Programmer Guide* for more information about using this software.

Cable Limitations

The MultiLINX Cable is compatible in supporting Readback for all the FPGAs supported by the XChecker Cable. In addition to the supporting legacy devices, the MultiLINX Cable supports the devices that were not supported by the XChecker Cable. Supported devices include those devices in the 4000E, 4000XL, and SPARTAN families whose bitfile size is more than 256K bits. The MultiLINX Cable will also support readback for the new Virtex family.

Note Debug is not available with the MultiLINX Cable when using the Hardware Debugger Software in the 2.1i Xilinx release version.

XChecker Hardware Drawbacks

Following are the limitations of the XChecker cable.

- Cannot support readback for devices whose bitfile size is more than 256K bits.
- Only supports RS-232.
- Has less user control (only 2 sets of 8 flying wires each).

MultiLINX Hardware Advantages

Following are the advantages of the MultiLINX cable.

- Fast download, readback & verify using the USB port.
- More configuration modes are supported.
- Supports both RS-232 ports and USB ports.
- Compatible with the currently supported devices for Readback & Verify.
- Supports new devices that are not supported by XChecker due to RAM size limitation.

- Works at multiple supply voltages (5 V, 3.3 V, and 2.5 V).
- Supports JTAG configuration for all Xilinx devices.
- Supports SelectMAP configuration mode for Virtex.

Previous Cable Versions

This section details considerations for using previous download cables with the Hardware Debugger Software.

You can use Hardware Debugger software with all previous parallel and serial download cables. However, these previous cables can only be used to download a configuration bitstream, they cannot be used for readback.

If you do use Hardware Debugger with a previous parallel or serial download cable version, keep the following points in mind.

- Previous versions of the download cable were made to download XC3000 and XC2000 designs, not XC4000 designs. The basic limitation of the previous cables is that they do not have a PROG pin to initiate a re-program in XC4000 devices. They also do not have an INIT pin to check for Cyclical Redundancy Check (CRC) errors during configuration.

  Note To use a parallel download cable prior to the Parallel Cable III to download designs to the XC4000 family devices, you must manually toggle the PROG pin to low. PROG is active when it is low. (The Parallel Cable III has a wire for the PROG pin.)

- Previous download cables do not support readback or verification.
- For the PC, the download cable is a parallel cable, requiring connection to the parallel port. (The XChecker cable is serial.)

There are only two situations when you might prefer using previous download cables instead of the XChecker Cable or MultiLINX Cable.

- You have circuit boards with header connectors keyed to match the previous cable headers. However, you could use the XChecker Cable with its flying lead connectors. Simply match the labeled flying leads to the equivalent signals on your system.
- You have circuit boards where power consumption is a critical factor. (The XChecker Cable requires about 100 mA at 5 V and the MultiLINX Cable requires about 300mA at 5 V, 500mA at 3.3 V,

and 750mA at 2.5 V; the Parallel Cable used with PCs draws less power from the target LCA board.) In such cases, you may use the Hardware Debugger software to download the bitstream.

Cable Baud Rates

The supported Baud Rates for the MultiLINX, Parallel and XChecker Cables are shown in the following table.

Table 1-2 Cable Baud Rates

Cable	PC	Workstation
MultiLINX Cable (USB)	1M-12M (Currently USB is supported only on Win98.)	USB is currently not supported on WorkStations.
MultiLINX Cable (RS-232)	9600, 19200, 38400, and 57600	9600, 19200, and 38400
Parallel Cable	9600	Not supported on WorkStations.
XChecker Cable	9600, 19200, 38400, and 115200	9600, 19200, and 38400

MultiLINX Cable and Flying Leads

The MultiLINX Cable is a device for configuring and verifying Xilinx FPGAs and CPLDs.

The MultiLINX Cable is shipped with four sets of flying lead wires. A USB Cable and RS-232 Cable (with adapter) are also supplied.

For detailed information on the MultiLINX Flying Wires supported modes, refer to the “MutliLINX™ Cable” chapter.

The following figure shows the MultiLINX Cable hardware and flying lead connection wires.

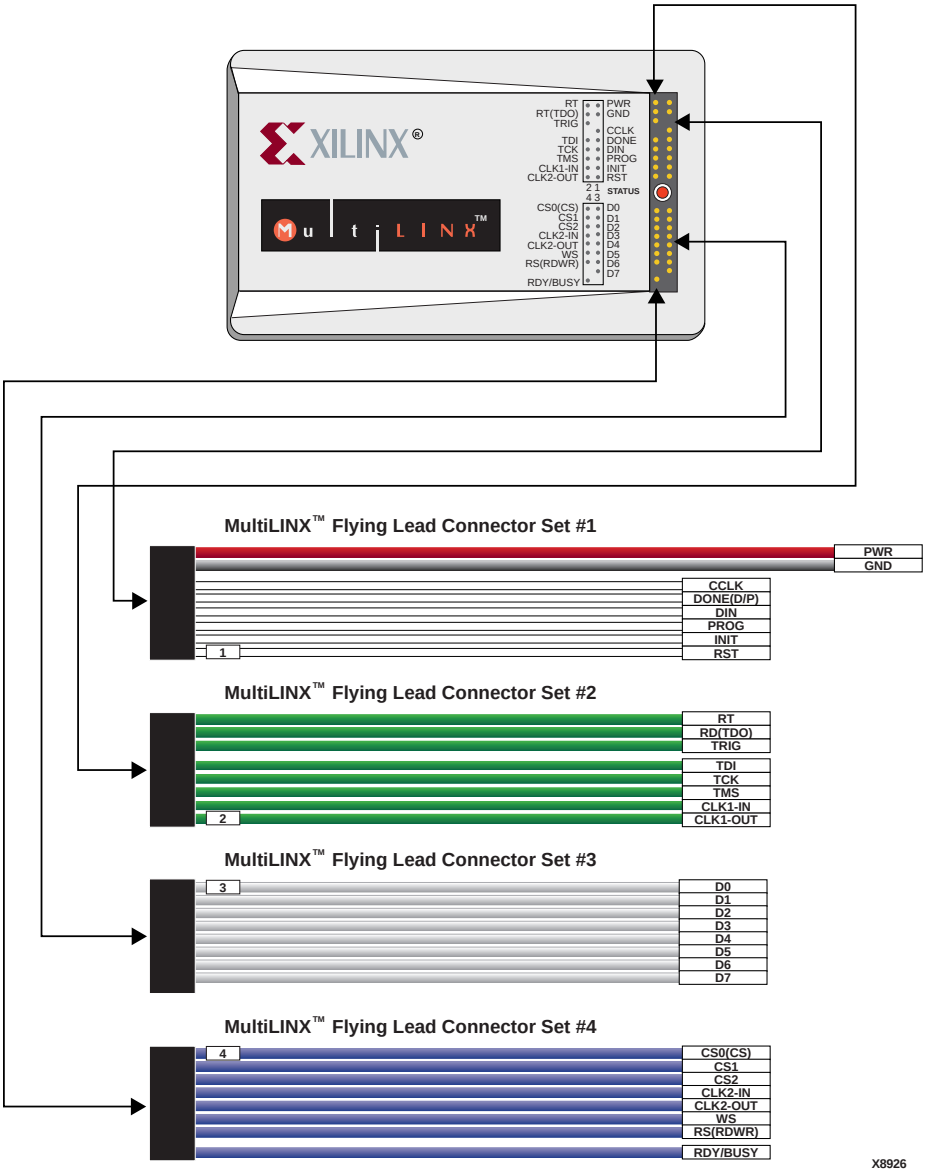


Figure 1-1 MultiLINX Cable and Flying Lead Connectors

The following figure shows the top and bottom view of the Multi-LINX Cable.



Figure 1-2 MultiLINX Cable

External Power for the MultiLINX Cable

The MultiLINX Cable gets its power from the User's circuit board an extended power supply. The cable power does not come from the USB port (nor the RS-232 port). The red (PWR) and black (GND) wires from Flying Wire Set #1 are connected to the VCC (red wire) and Ground (black wire) lines of the circuit board that is powering the Xilinx device. The external power for the MultiLINX Cable is shown in the following figure.

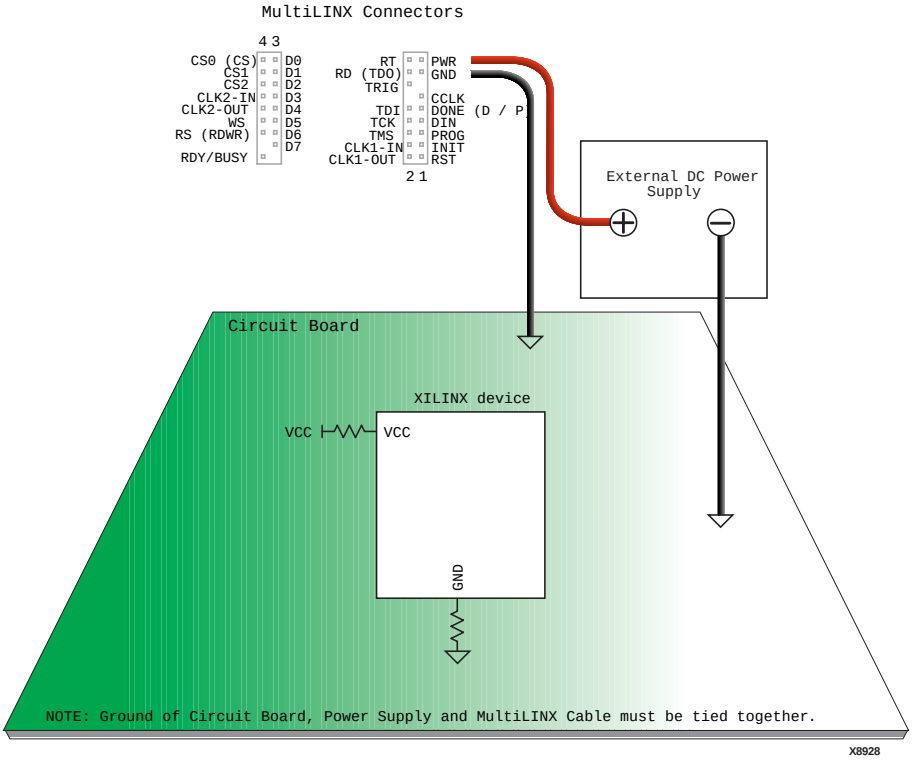


Figure 1-3 Optional External Power for the MultiLINX Cable

When using an external power supply, make sure that the ground of the supply, the MultiLINX Cable and the circuit board are all tied together. An advantage of the external DC power supply is that no power is taken away from the circuit board and the MultiLINX Cable can remain powered up and does not get powered down when the circuit board power is off.

Parallel Cable III

The Parallel Cable III is a cable assembly which contains a buffer to protect your PC's parallel port and a set of headers to connect to your target system.

The cable can be used with a single CPLD or FPGA device, or several devices connected in a daisy chain.

The transmission speed of the this cable is determined solely by the speed at which the host PC can transmit data through its parallel port interface.

Using the Parallel Cable III requires a PC equipped with an AT compatible parallel port interface and a DB25 standard printer connector.

Flying Leads

This cable is shipped with two sets of flying leads, one for FPGAs and one for CPLDs. The CPLD leads are labelled “JTAG” and the FPGA leads are labelled “FPGA”.

Each flying lead has a 9-pin (6 signals, 3 keys) header connector on one end. This connector fits onto one of the two cable headers. These header connectors are keyed to assure proper orientation to the cable assembly.

On the other end of each flying lead are six individual wires with female connectors. The female connectors fit onto standard 0.025 inch square male pins.

As an example, the following figure shows the Parallel Cable III and its FPGA flying lead wires.

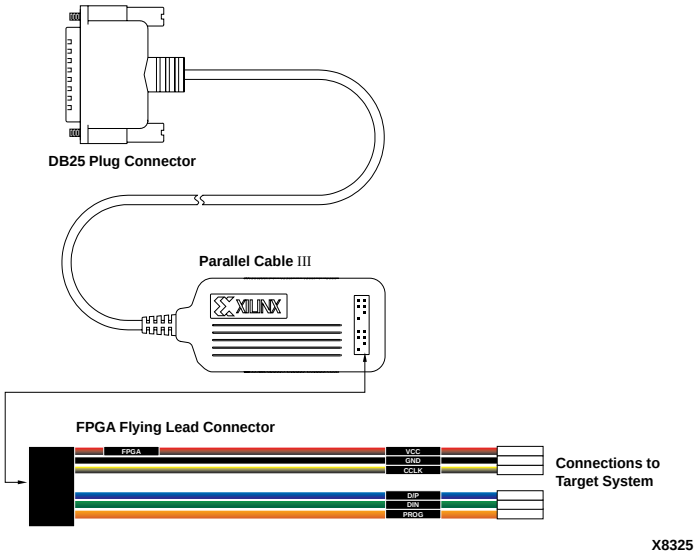


Figure 1-4 Parallel Cable III and FPGA Flying Leads

The following figure shows top and bottom views of the Parallel Cable III, including the FPGA and JTAG (CPLD) headers.

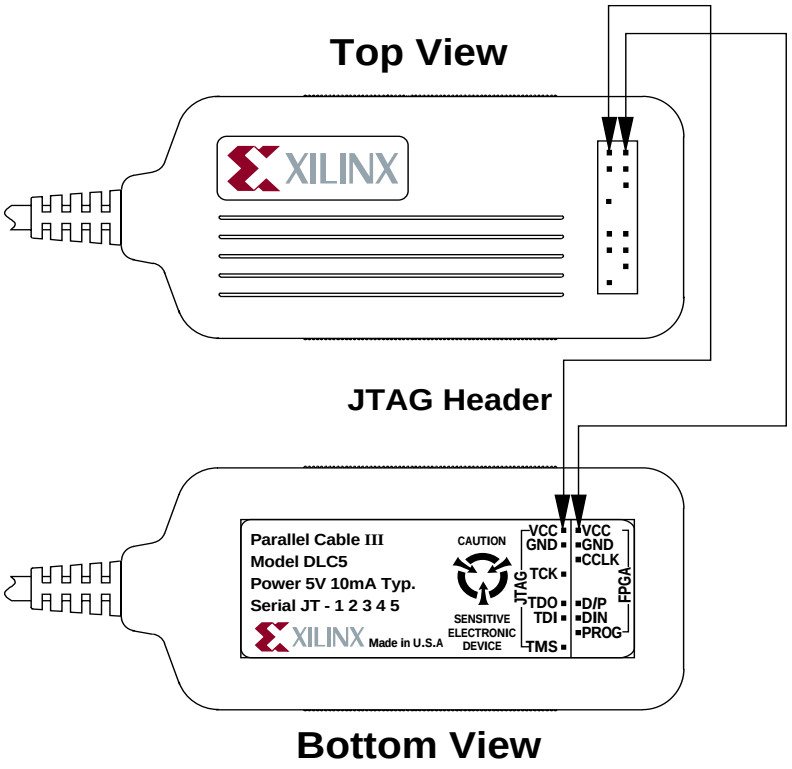


Figure 1-5 Parallel Cable III

Note The plastic cover of the Parallel Cable III is grey, while the XChecker Cable is beige.

Configuring CPLDs With the Parallel Cable III

When connecting the CPLD flying leads for configuration, make sure to use the “JTAG” header. The following figure shows the connections between the Parallel Cable III CPLD flying leads and a target system.

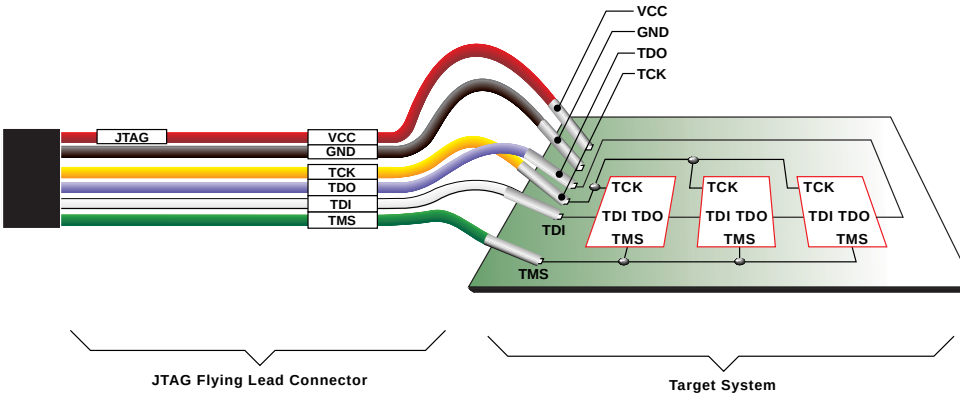


Figure 1-6 Parallel Cable III Connections to CPLD Device

The following table describes the pin functions and connections for configuring CPLDs with the Parallel Cable III.

Table 1-3 Parallel Cable III CPLD Pin Connections

Name	Function	Connections
VCC	Power – Supplies VCC (5 V, 10 mA, typically) to the cable.	To target system VCC
GND	Ground – Supplies ground reference to the cable.	To target system ground
TCK	Test Clock – Drives the test logic for all devices on a JTAG chain.	Connect to system TCK pin.
TDO	Test Data Output – data from the target system is read at this pin.	Connect to system TDO pin.

Table 1-3 Parallel Cable III CPLD Pin Connections

Name	Function	Connections
TDI	Test Data Input – this signal is used to transmit serial test instructions and data.	Connect to system TDI pin.
TMS	Test Mode Select – this signal is decoded by the JTAG state machine to control test operations.	Connect to system TMS pin.

Note TRST is an optional pin in the JTAG (IEEE 1149.1) specification, and is not used by XC9500 CPLDs. If any of your non-Xilinx parts have a TRST pin, the pin should be connected to VCC

Configuring FPGAs With the Parallel Cable III

This section details the connections needed to configure FPGAs with the Parallel Cable III.

The following figures show which pins to connect, depending on your chosen FPGA device. For descriptions of each pin, see Table 3-6and Table 3-7 of the “FPGA Design Demonstration Board” chapter.

Note If you are using the Xilinx FPGA Design Demonstration Board, see the “Mode Switch Settings” section of the “FPGA Design Demonstration Board” chapter for specific configuration information.

Connect the flying wires to XC4000 FPGAs as shown in the following figure.

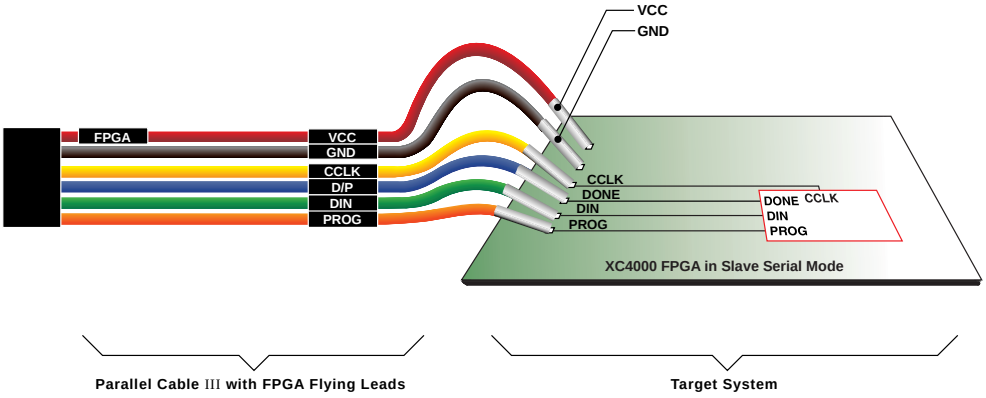


Figure 1-7 Parallel Cable III Connections to XC4000 Device

To configure XC3000 FPGAs, the PROG wire is not used as shown in the following figure. In both cases the FPGA must be in the Serial Slave Mode.

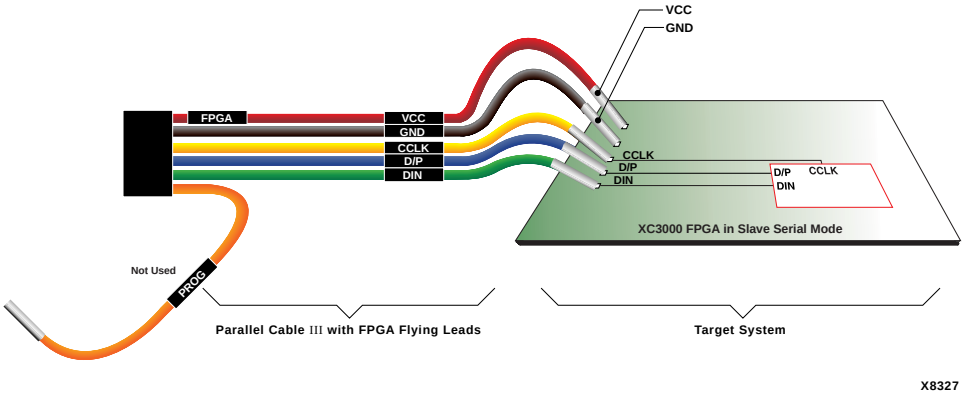


Figure 1-8 Parallel Cable III Connections to XC3000 Device

Note If you are using the Xilinx FPGA Demonstration Board, see the "Mode Switch Settings" section of the "FPGA Design Demonstration Board" chapter for specific configuration information.

XChecker Cable

The XChecker hardware consists of a cable assembly with internal logic, a test fixture, and a set of headers to connect the cable to your target system. The cable can be used with a single FPGA or CPLD, or several devices connected in a daisy chain.

Using the XChecker hardware requires either a standard DB-9 or DB-25 RS-232 serial port. If you have a different serial port connection, you need to provide a DB-9/DB-25 adapter.

Flying Leads

The XChecker Cable is shipped with two sets of flying lead wires. The flying lead connectors have a nine position header connector on one end. The other end has eight individual wires with female connectors that fit onto standard 0.025 inch square male pins.

You need appropriate pins on the target system for connecting to the download cable. The “XChecker Baud Rates” section details the necessary pins.

The following figure shows the XChecker Cable hardware and flying lead connection wires.

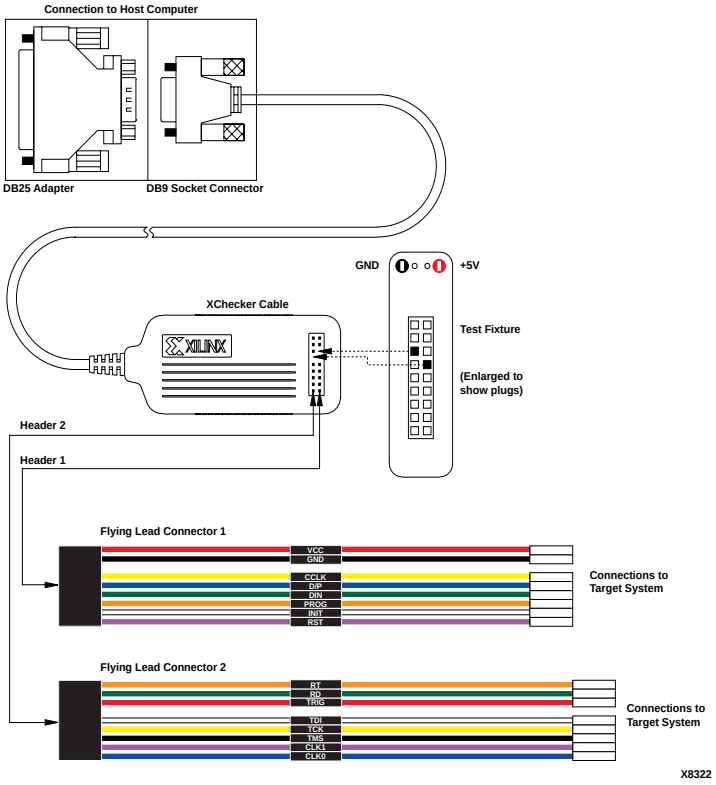


Figure 1-9 XChecker Cable and Flying Leads

The following figure shows top and bottom views of the XChecker Cable.

XChecker Cable

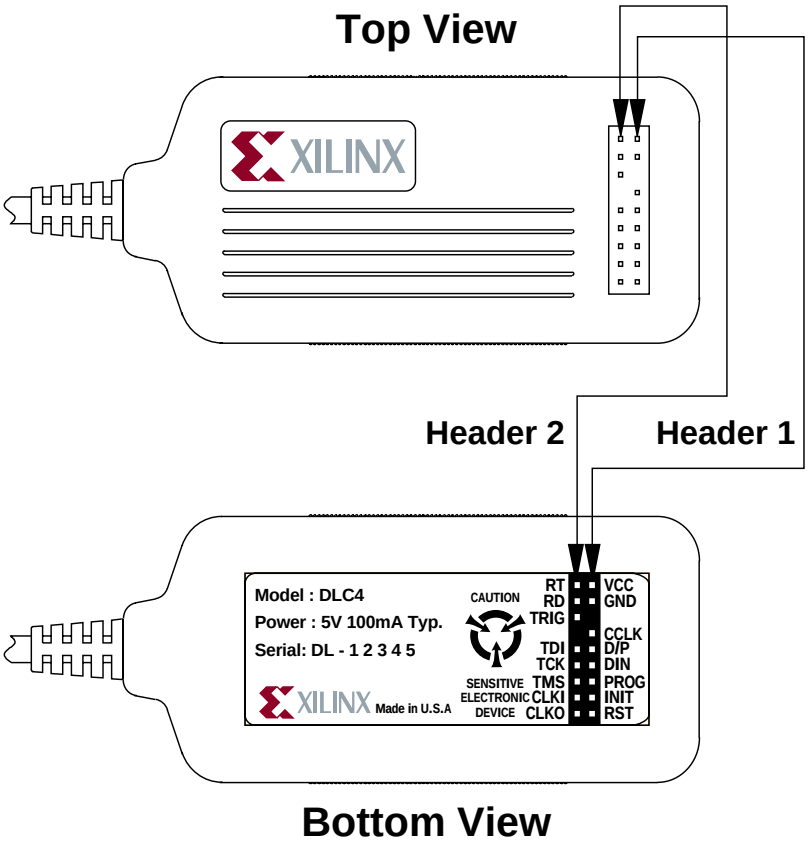


Figure 1-10 XChecker Cable

Note The plastic cover of the XChecker Cable is beige, while the cover for the Parallel Cable III is grey. The flying lead wires are keyed to fit into the appropriate cable header. Use Header 1 for FPGAs and Header 2 for CPLDs.

XChecker Baud Rates

Communication between your host system and the XChecker Cable is dependent on host system capability. The XChecker Cable supports several Baud rates and platforms, as shown in the following table.

Table 1-4 Valid Baud Rates

Platform	9600	19200	38400	115.2K
IBM® PC	X	X	X	X
NEC PC	X			
SUN®	X	X	X	
HP 700	X	X	X	X

X indicates applicable baud rate

Configuring CPLDs With the XChecker Cable

The JTAG Programmer should be used to program in JTAG mode. When you configure a CPLD with the XChecker Cable, connections between the cable assembly and the target system use only six of the sixteen leads. For connection to JTAG boundary-scan systems you need only ensure that the VCC, GND, TDI, TCK, TMS and RD (TDO) pins are connected.

Note TRST is an optional pin in the JTAG (IEEE 1149.1) specification, and is not used by XC9500 CPLDs (If any of your non-Xilinx parts have a TRST pin, the pin should be connected to VCC).

Once installed properly, the connectors provide power to the cable and allow download and readback of configuration data. The following table describes the CPLD pin connections to the target circuit board.

Table 1-5 XChecker Cable Pin Connections for CPLDs

Name	Function	Connections
VCC	Power – Supplies VCC (5 V, 100 mA, typically) to the cable	To target system VCC
GND	Ground – Supplies ground reference to the cable	To target system ground

Table 1-5 XChecker Cable Pin Connections for CPLDs

Name	Function	Connections
RD (TDO)	Read Data – Reads back data from the target system is read at this pin.	Connect to system TDO pin.
TDI	Test Data In – this signal is used to transmit serial test instructions and data.	Connect to system TDI pin.
TCK	Test Clock – this clock drives the test logic for all devices on boundary-scan chain.	Connect to system TCK pin.
TMS	Test Mode Select – this signal is decoded by the TAP controller to control test operations.	Connect to system TMS pin.
CLKI	Not used.	Unconnected.
CLKO	Not used.	Unconnected.
CCLK	Not used.	Unconnected.
D / P	Not used.	Unconnected.
DIN	Not used.	Unconnected.
PROG	Not used.	Unconnected.
INIT	Not used.	Unconnected.
RST	Not used.	Unconnected.
RT	Not used.	Unconnected.
TRIG	Not used.	Unconnected.

Configuring FPGAs With the XChecker Cable

This section details the connections needed to configure FPGAs with the XChecker Cable.

Note If you are using the Xilinx FPGA Design Demonstration Board, see the “Demonstration Board Operation” section of the “FPGA Design Demonstration Board” chapter for specific configuration information.

The following figures show which pins to connect, depending on your chosen FPGA device. For descriptions of each pin, see Table 3-6and Table 3-7 of the “FPGA Design Demonstration Board” chapter.

Use Header 1 (see Figure 1-9) to connect the XChecker Cable to the target system for configuring FPGAs. When configuring XC4000 FPGAs, the RST (Reset) wire is not used as shown in the following figure.

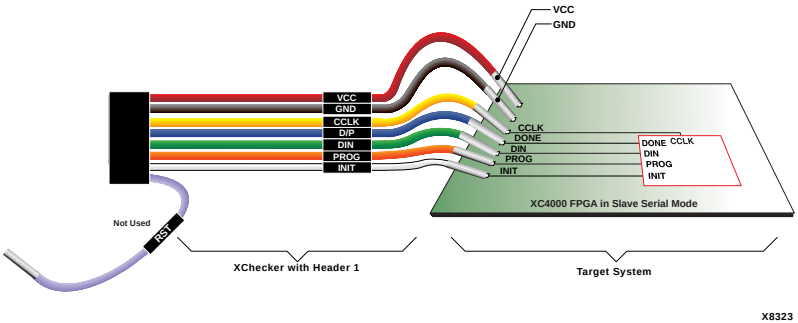


Figure 1-11 XChecker Connections to XC4000 Device

To configure XC3000 FPGAs, the PROG wire is not used. This is shown in the following figure. In both cases, the FPGA must be in the Serial Slave Mode.

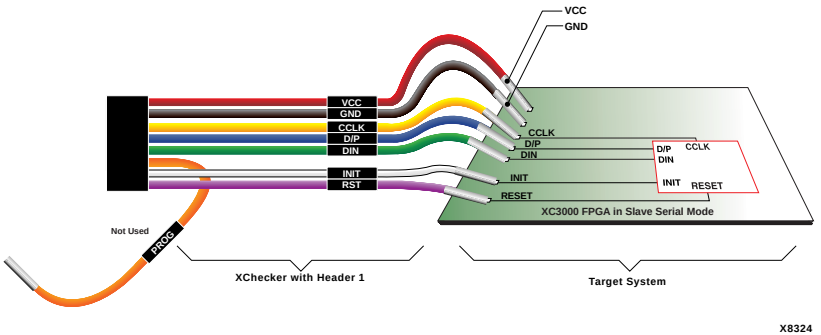


Figure 1-12 XChecker Connections to XC3000 Device

Pin Connection Considerations

The following adjustments will make the process of connecting and downloading easier.

- Provide appropriate pins on your printed circuit board for your device type.
- Place pins on board so that flying leads can reach them. The flying leads that are shipped with the cable are six inches long. While pins may be a couple inches apart, do not have any two pins more than six inches apart.
- Keep header pins on your board a minimum of 0.10 inches apart.

Cable Connection Procedure

The following steps are required for download cable operation.

1. Connect the cable to your host system. Make sure to use the appropriate port and adapter, if necessary.
2. Connect the cable to your target system or demonstration board. Always power up the host system before the target system. The power for the drivers is derived from the target system.
3. Connect the cable's GND wire to the corresponding signal on the target board. Next, connect VCC to the +5 V on the target board.
4. Connect the appropriate pins for device configuration.
5. Power up the target system.



Caution

Cable protection ensures that the host system port cannot be damaged through normal cable operation. For increased safety, please check that the power to the host computer is on before the target system is powered up.

6. Start the appropriate Xilinx software package and configure your device. The JTAG Programmer Software and Hardware Debugger Software will automatically identify the download cables when correctly connected. If you need to set up the cable manually, see the following section.

   Note The download cables will not operate if the target system's power is turned off before or during software operations. Make certain that this power connection is on and stable. Your system's power should be on during ISP operations. When powering down, turn off the target demonstration board first, and then the host machine.

Setting Up The Cable

If you are using the Hardware Debugger Software and a PC as a host system, manually select your cable as follows.

`Output > Cable Setup`

Select your cable type, then click **`OK`**. If you are using the XChecker cable, you may also select a BAUD rate. See Table 1-4.

If you are using the JTAG Programmer software, select the cable manually as follows.

`Output > Cable Auto Connect`

Select your cable type, then click **`OK`**.

Download Cable Schematic

The following figure is an internal schematic of the Parallel Cable III. You must use the recommended lengths for parallel cables. Xilinx cables are typically six feet (approximately two meters) in length between the connector and active circuitry. Keep the wires between the headers and target system as short as possible.

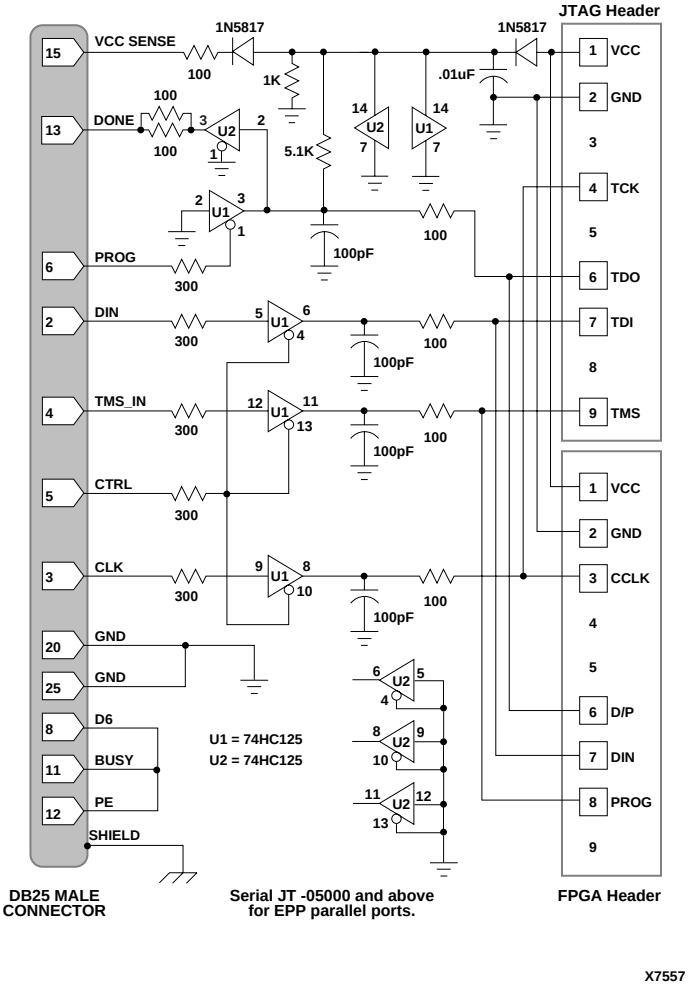


Figure 1-13 Parallel Cable III Schematic

Chapter 2

MutliLINX™ Cable

The MultiLINX™ Cable is the next generation configuration and readback tool for FPGA's and CPLD's. During the integration of Xilinx programmable logic into your design, the MultiLINX Cable can be used to troubleshoot your configuration setup, and diagnose configuration problems associated with Xilinx programmable logic.

The MultiLINX Cable uses either a serial or USB port on a host computer. Maximum throughput is available by using the USB interface.

This chapter contains the following sections.

- "Additional MultiLINX Documentation"
- "MultiLINX Platform Support"
- "MultiLINX Flying Wires"
- "Device Configuration Modes"

Additional MultiLINX Documentation

You can access the following mentioned application note with descriptions of device-specific design techniques and approaches from the support page at `http://support.xilinx.com/support/searchtd.htm`.

The "*Getting Started with the MultiLINX Guide*" application note is a quick reference to everything you need to know to use the MultiLINX Cable.

- Describes using a USB port, Mixed Voltage environments, connections for all the supported Modes.
- Describes how to setup a Prototype application for use with the MultiLINX Cable.

- Describes all the cables, their capabilities, and associated software tools.

MultiLINX Platform Support

The MultiLINX Cable supports the following platforms.

- Win 95
- Win 98
- Win NT 4.0
- Solaris 2.6
- HP 10.2

Table 2-1 MultiLINX Support

Supported Platforms	USB	RS-232
Win 95		X
Win 98	X	X
Win NT 4.0		X
Solaris 2.6		X
HP 10.2		X

X indicates applicable ports that can be used with the MultiLINX Cable on specified platforms.

MultiLINX Flying Wires

The MultiLINX Cable is shipped with four sets of flying lead wires. The following figure shows these four sets of MultiLINX flying lead connectors.

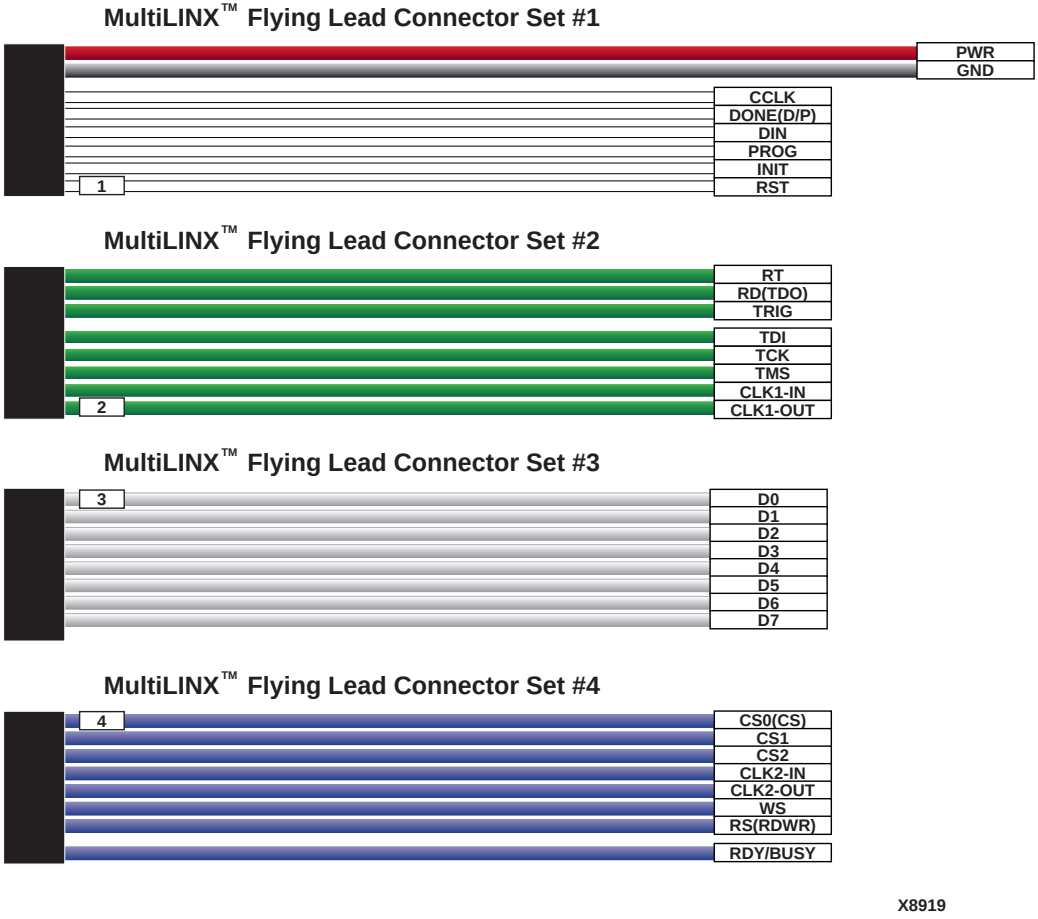


Figure 2-1 MultiLINX Flying Wires

The MultiLINX Flying wires are described in the following table.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
PWR	*Power* — Supplies VCC to cable (Works at multiple voltages 5V, 3.3V, and 2.5V).
GND	*Ground* — Supplies ground reference to cable.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
CCLK	*Configuration Clock* — is the configuration clock pin, and the default clock for readback operation.
DONE (D/P)	*Done/Program* — represents the D/~P pin for XC3000A/L and XC3100A devices, and DONE for XC4000, XC5200 and Spartan devices. This pin indicates that the configuration process is complete for XC4000, XC5200, and Spartan devices. This same pin initiates a reconfiguration, and indicates that the configuration process is complete on XC3000 FPGAs.
DIN	*Data In* — Provides configuration data to target system during configuration and is tristated at all other times.
PROG	*Program* — A Low indicates the device is clearing its configuration memory. Active Low signal to initiate the configuration process.
INIT	*Initialize* — Initialization sequencing pin during configuration (Indicates start of configuration). A logical zero on this pin during configuration indicates a data error.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
RST	*Reset* —Pin used to reset internal FPGA logic. Connection to this pin is optional during configuration. During configuration, a Low pulse causes XC3000A devices to restart configuration. After configuration, this pin can drive Low to reset target FPGA internal latches and flip-flops. RST is the active high for XC4000 / XC5200 devices.
RT	*Read Trigger* — Pin used to initiate a readback of target FPGA. MultiLINX output. Hardware Debugger provides Low-to-High transition on RT to initiate readback.
RD (TDO)	*Read Data* — MultiLINX input. Hardware Debugger receives the readback data through the RD pin after readback is initiated. Pin used to initiate a readback of target FPGA. TDO is for JTAG.
TRIG	*System Trigger* — MultiLINX input High on this pin signals the MultiLINX electronics to initiate a readback and causes the RT pin to go High.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
RD (TDO) TDI TCK TMS	These pins are used for JTAG Programmer device configuration. The JTAG/boundary scan pins function for FPGA and CPLD JTAG operations.
CLKI-IN	*Clock Input* — Transmits your system clock to the MultiLINX electronic. Clock must be between 120 kHz and 10 MHz. Connect this pin to target system clock to synchronize the read-back trigger with target system clock.
CLK1-OUT	*Clock Output* — Drives target system clock. Clock can come from either the CLKI-IN pin, or it can be internally generated by the MultiLINX Cable when CLKI-IN is unconnected.
D0-D7	*Data Bus* — This pin is used for Virtex SelectMAP Mode. An 8 bit data bus supporting the SelectMAP, and Express configuration modes.
CS0 (CS)	*Chip Select* — CS on the Virtex; and CS0 on the XC4000 and XC5200 FPGAs. The CS0/CS pin represents a chip select to the
CS1	*Chip Select* — The CS1 pin represents Chip Select to the XC4000 and XC5200 FPGAs during configuration.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
CS2	*Chip Select* — The CS2 pin represents Chip Select to the XC3000 FPGA while using the Peripheral configuration mode.
CLK2-IN	*Clock Input* — Transmits your system clock to the MultiLINX electronics. Clock must be between 120 kHz and 10 MHz. Connect this pin to target system clock to synchronize the readback trigger with target system clock.
CLK2-OUT	*Clock Output* — Drives target system clock. Clock can come from either the CLK2-IN pin, or it can be internally generated by the MultiLINX Cable when CLK2-IN is unconnected
WS	*Write Select* — The WS pin represents Write Select control for the Asynchronous Peripheral configuration mode on XC4000 and XC5200 FPGAs.

Table 2-2 MultiLINX Pin Descriptions

Signal Name	Function
RS (RDWR)	*Read Select* — The RS pin represents Read Select control for the Asynchronous Peripheral configuration mode on XC4000 and XC5200 FPGAs. *Read/Write* — The RDWR pin is used as an active high READ and an active low WRITE control signal to the Virtex FPGA.
RDY / BUSY	*Busy Pin* — Busy pin on the Virtex; and RDY / Busy pin on the XC3000, XC4000, and XC5200 FPGAs.

MultiLINX Baud Rates

Communication between your host system and the MultiLINX Cable is dependent on host system capability. The MultiLINX Cable supports several Baud rates.

With the USB interface, the MultiLINX Cable can run at 12 M bits / sec. With the PC RS-232 interface, the MultiLINX Cable can run from a 9600 baud rate to a 57.6 K baud rate.

MultiLINX Power Requirements

The MultiLINX Cable gets its power from the User's circuit board. The cable power does not come from the USB port (nor the RS-232 port). The red (PWR) and black (GND) wires from Flying Wire Set #1 are connected to the VCC (red wire) and Ground (black wire) lines of the circuit board that is powering the Xilinx device.

The minimum input voltage to the cable is 2.5 V (.8 A). The maximum input voltage is 5 V (.4 A).

External Power for the MultiLINX Cable

An optional method of powering the MultiLINX Cable is to use an external DC power supply (not supplied) as shown in the following

"Optional External Power for the MultiLINX Cable" figure.Typical current requirements are: 300 mA at 2.5 V.

Note The voltage supplied to the MultiLINX Cable does not need to be the same voltage powering the Xilinx device. The cable generates its own voltages from the power supplied to it.

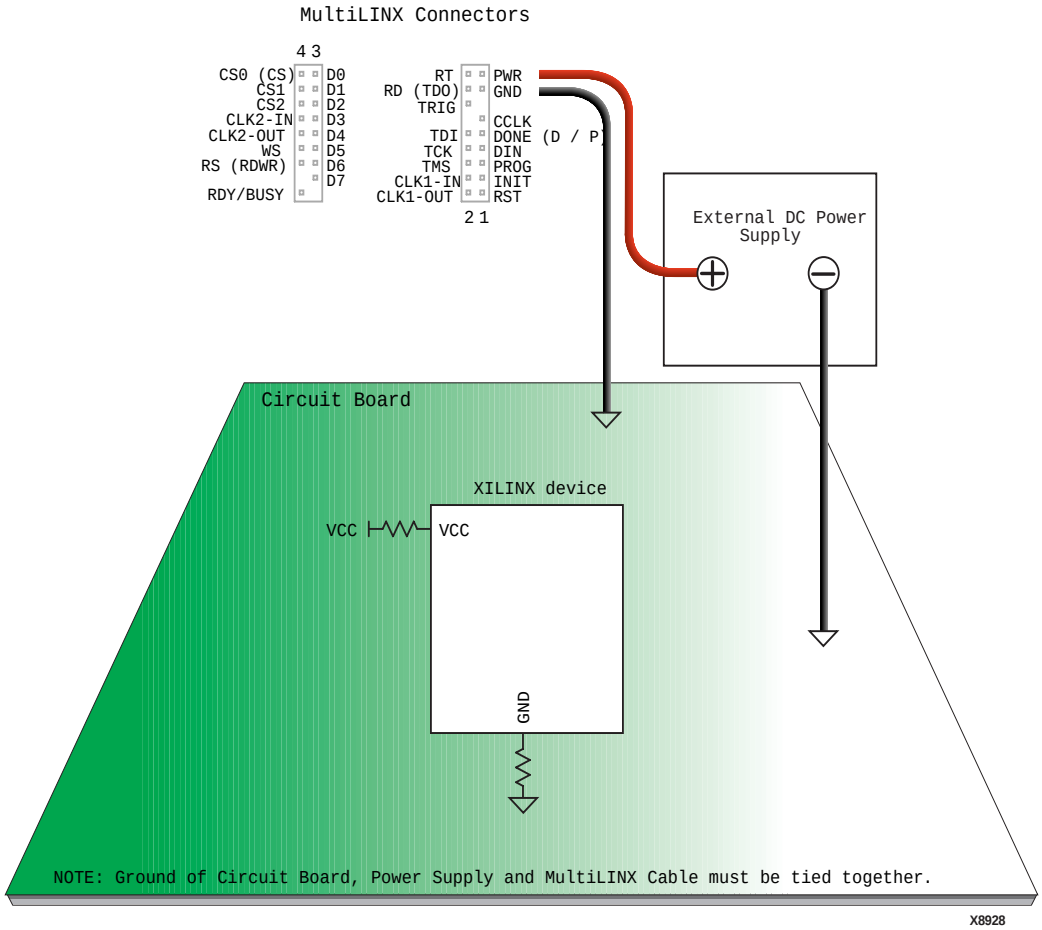


Figure 2-2 Optional External Power for the MultiLINX Cable

When using an external power supply, make sure that the ground of the supply, the MultiLINX Cable and the circuit board are all tied together. An advantage of the external DC power supply is that no power is taken away from the circuit board and the MultiLINX Cable

can remain powered up and does not get powered down when the circuit board power is off.

Device Configuration Modes

The various MultiLINX device configuration modes supported for each device are shown in the following table.

Table 2-3 MultiLINX Device Configuration Modes

Configuration Mode	Device					
	Virtex	Spartan	XC9500	XC5200	XC4000	XC3000
SelectMAP	X					
Slave Serial	X	X		X		X
JTAG	X	X	X	X	X	

Downloading Configuration Data

This section details the connections needed to download configuration data with the MultiLINX Cable.

Slave Serial Mode (XC3000)

The following figure shows in detail the Slave Serial Mode connections to a XC3000 device for Downloading Configuration Data.

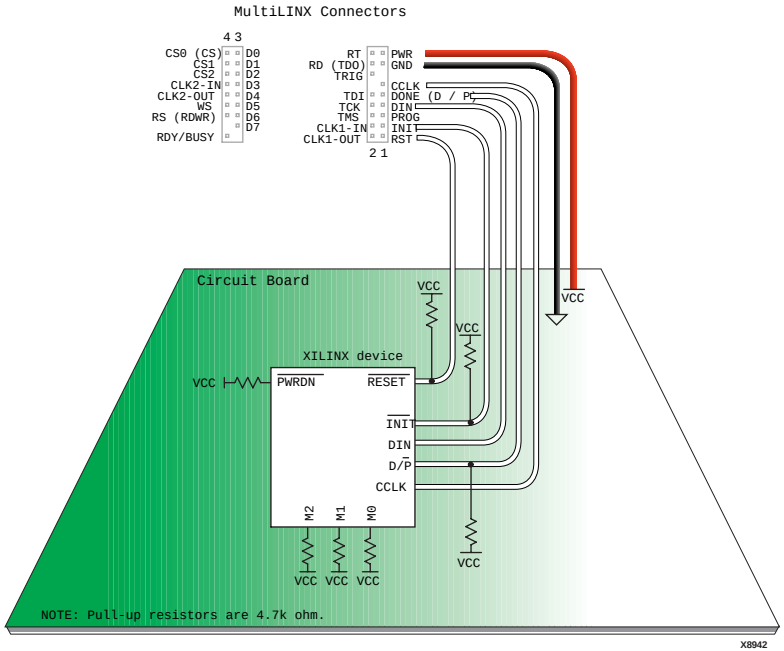


Figure 2-3 Slave Serial Mode (XC3000)

Slave Serial Mode (Virtex, Spartan, XC5200, XC4000)

The following figure shows in detail the Slave Serial Mode connections for Virtex, Spartan, XC5200, and XC4000 devices.

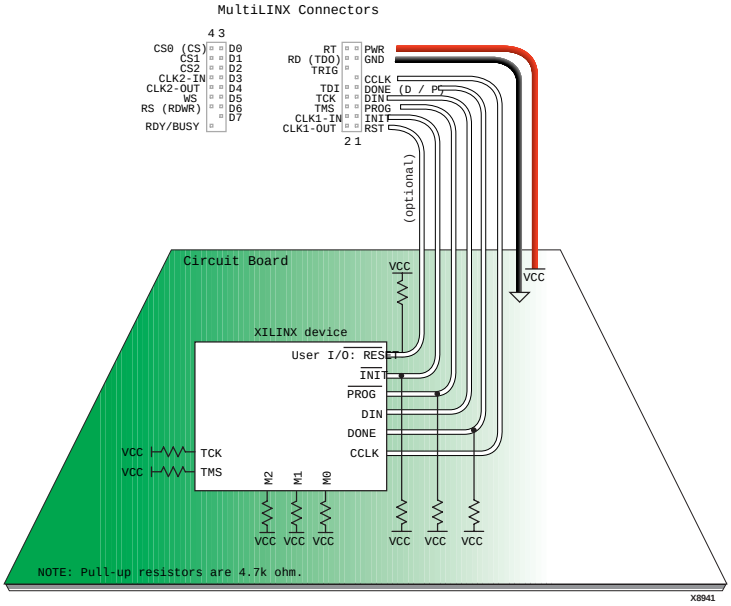


Figure 2-4 Slave Serial Mode (Virtex, Spartan, XC5200, XC4000)

Downloading Configuration Data or Verification of Data

This section details the connections needed for downloading configuration data or the verification of data with the MultiLINX Cable.

SelectMAP Mode (Virtex)

The following figure shows in detail the SelectMAP Mode connections for Virtex devices.

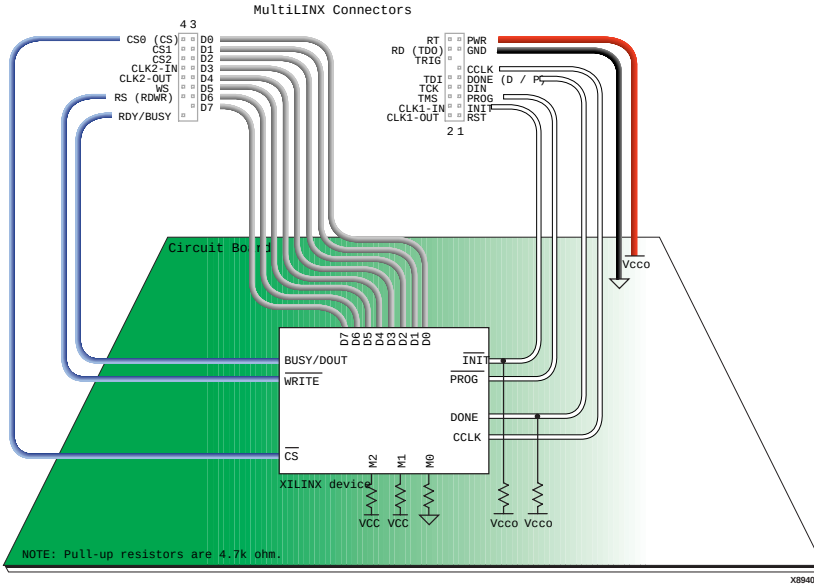


Figure 2-5 SelectMAP Mode (Virtex)

Downloading Configuration Data

This section details the connections needed for downloading configuration data with the MultiLINX Cable in JTAG Mode.

JTAG Mode (XC9000, Virtex, Spartan, XC5200, XC4000)

The following figure shows in detail the JTAG Mode connections for XC9000, Virtex, Spartan, XC5200, and XC4000 devices.

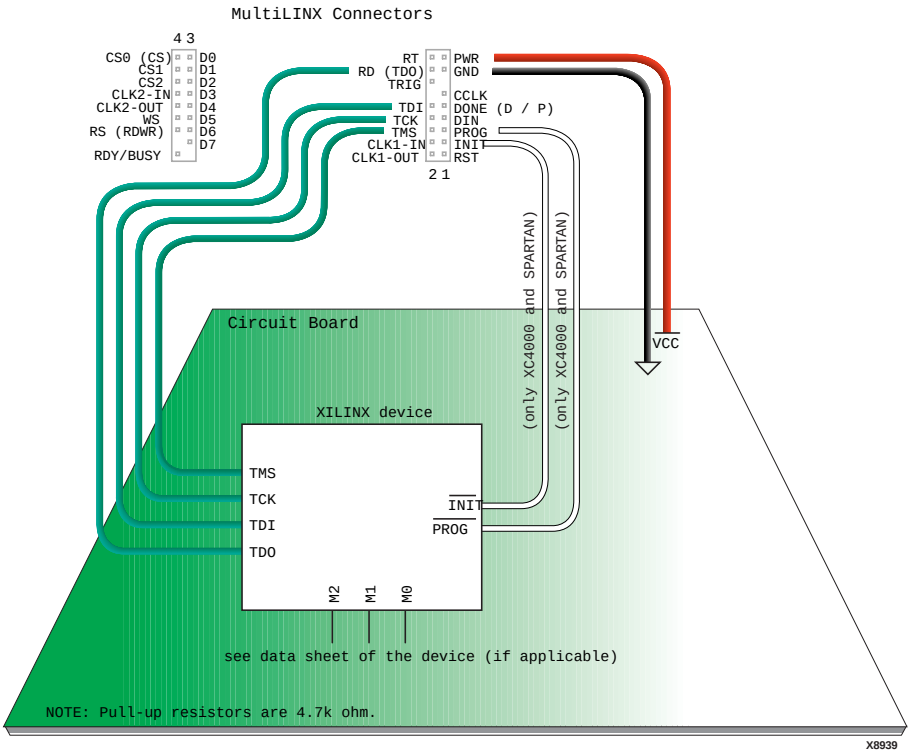


Figure 2-6 JTAG Mode (XC9000, Virtex, Spartan, XC5200, XC4000)

Downloading/Verification of Configuration Data

This section details the connections needed for downloading / verification of configuration data with the MultiLINX Cable in Slave Serial Mode.

Slave Serial Mode (XC3000)

The following figure shows in detail the Slave Serial Mode connections for the XC3000 device.

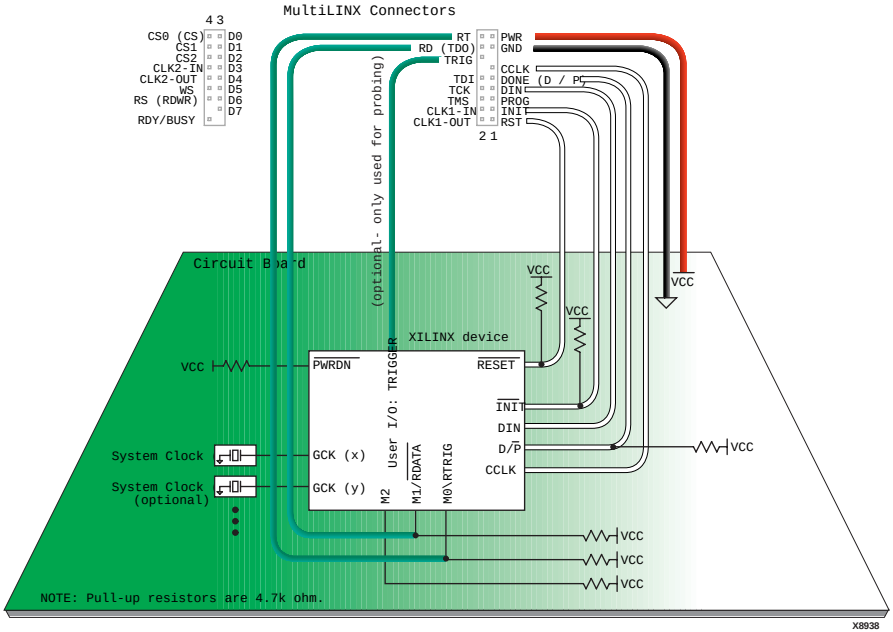


Figure 2-7 Slave Serial Mode (XC3000)

Slave Serial Mode (Spartan, XC5200, XC4000)

The following figure shows in detail the Slave Serial Mode connections for Spartan, XC5200, and XC4000 devices.

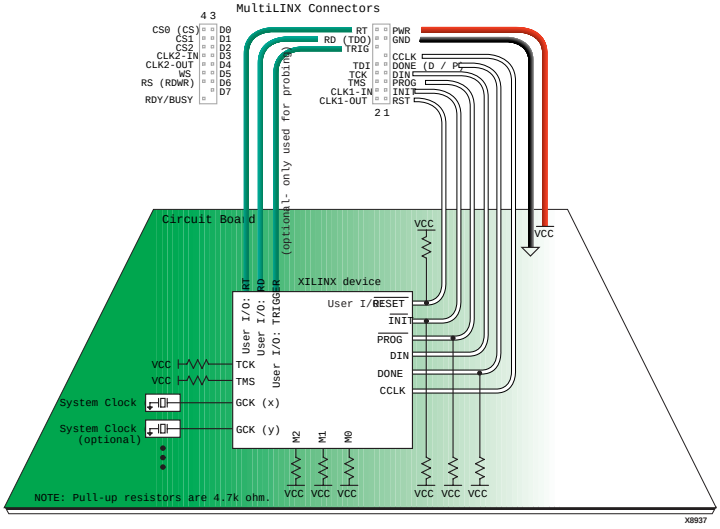


Figure 2-8 Slave Serial Mode (Spartan, XC5200, XC4000)

SelectMAP Mode (Virtex)

The following figure shows in detail the SelectMAP Mode connections for downloading / verification of configuration data with Virtex devices.

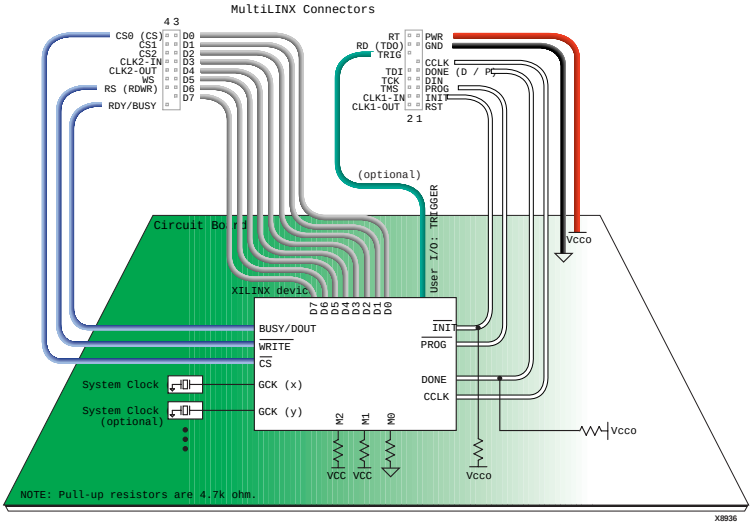


Figure 2-9 SelectMAP Mode (Virtex)

SelectMAP Mode (Virtex with Asynchronous Probing)

The following figure shows in detail the SelectMAP Mode connections for Virtex with Asynchronous Probing.

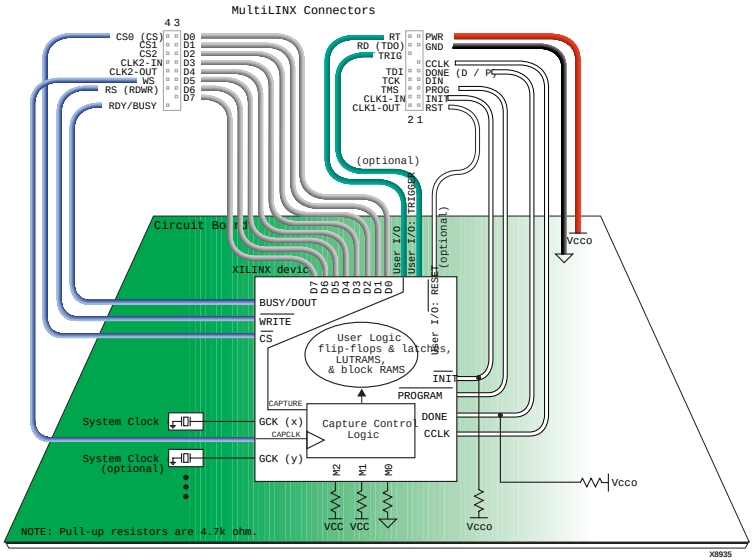


Figure 2-10 SelectMAP Mode (Virtex with Asynchronous Probing)

JTAG Mode (XC9000, Virtex, Spartan, XC5200, XC4000)

The following figure shows in detail the JTAG Mode connections for XC9000, Virtex, Spartan, XC5200, and XC4000 devices.

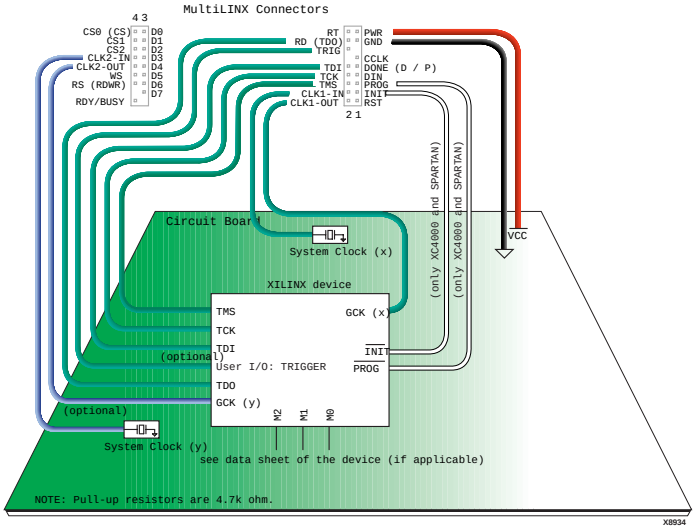


Figure 2-11 JTAG Mode (XC9000, Virtex, Spartan, XC5200, XC4000

Verification of Configuration Data Only

This section details the connections needed for verification of configuration data only using the MultiLINX Cable.

Verification of Configuration Data Only (Spartan, XC5200, XC4000)

The following figure shows in detail the connections for verification of configuration data only with Spartan, XC5200, and XC4000 devices.

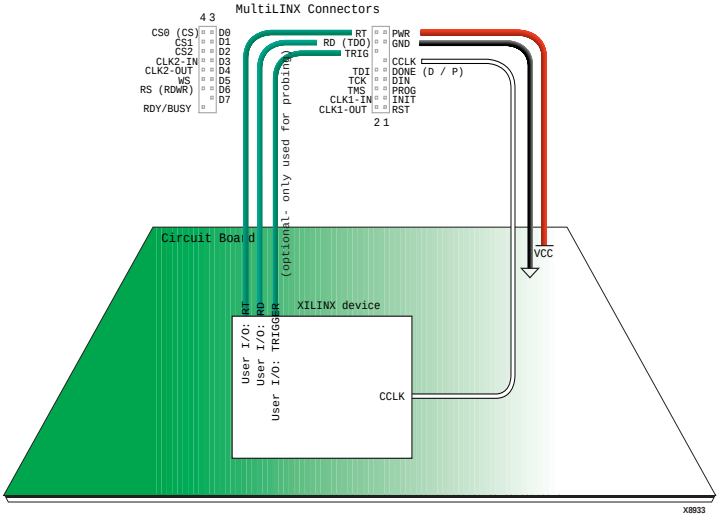


Figure 2-12 Verification of Configuration Data Only (Spartan, XC5200, XC4000)

Verification of Configuration Data Only (XC3000)

The following figure shows in detail the connections for verification of configuration data only with the XC3000 device.

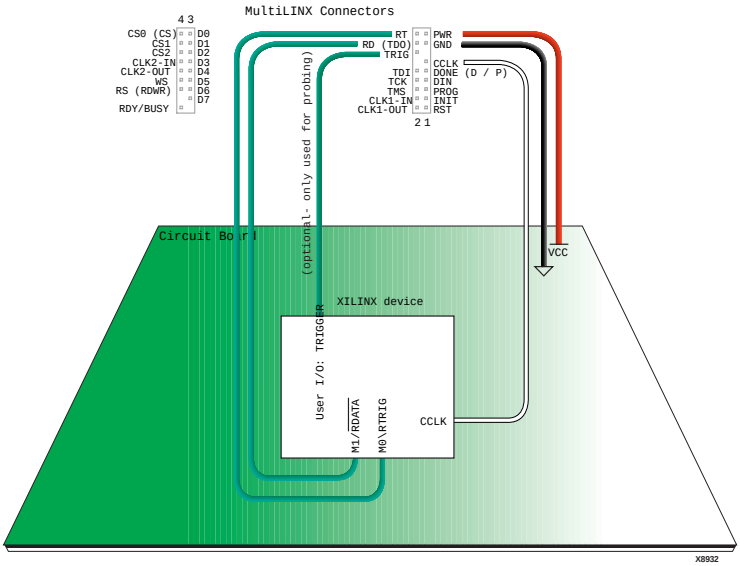


Figure 2-13 Verification of Configuration Data Only (XC3000)

Synchronous Probing

This section details the connections needed for synchronous probing using the MultiLINX Cable.

Slave Serial Mode (XC3000)

The following figure shows in detail the Slave Serial Mode connections for synchronous probing using the XC3000 device.

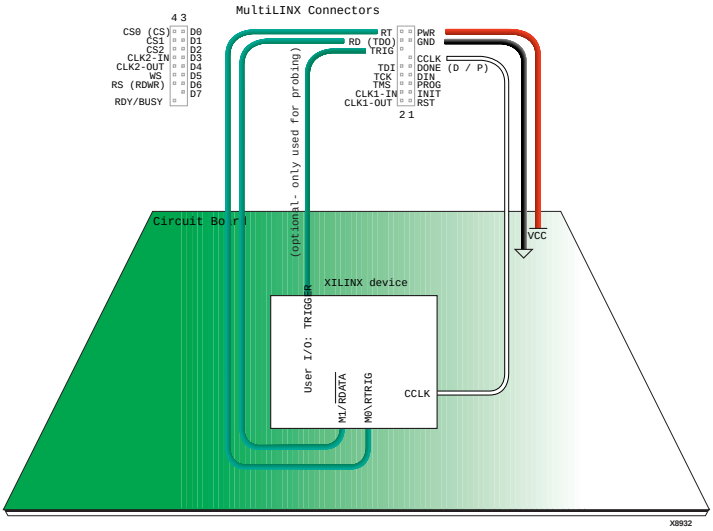


Figure 2-14 Slave Serial Mode (XC3000)

Slave Serial Mode (Spartan, XC5200, XC4000)

The following figure shows in detail the Slave Serial Mode connections for synchronous probing using Spartan, XC5200, and XC4000 devices.

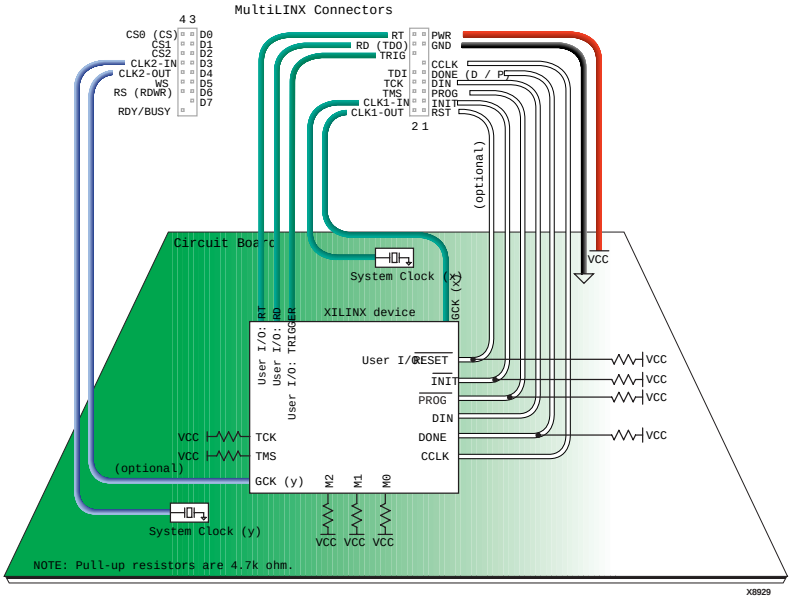


Figure 2-15 Slave Serial Mode (Spartan, XC5200, XC4000)

SelectMAP Mode (Virtex)

The following figure shows in detail the SelectMAP Mode connections for synchronous probing using Virtex devices.

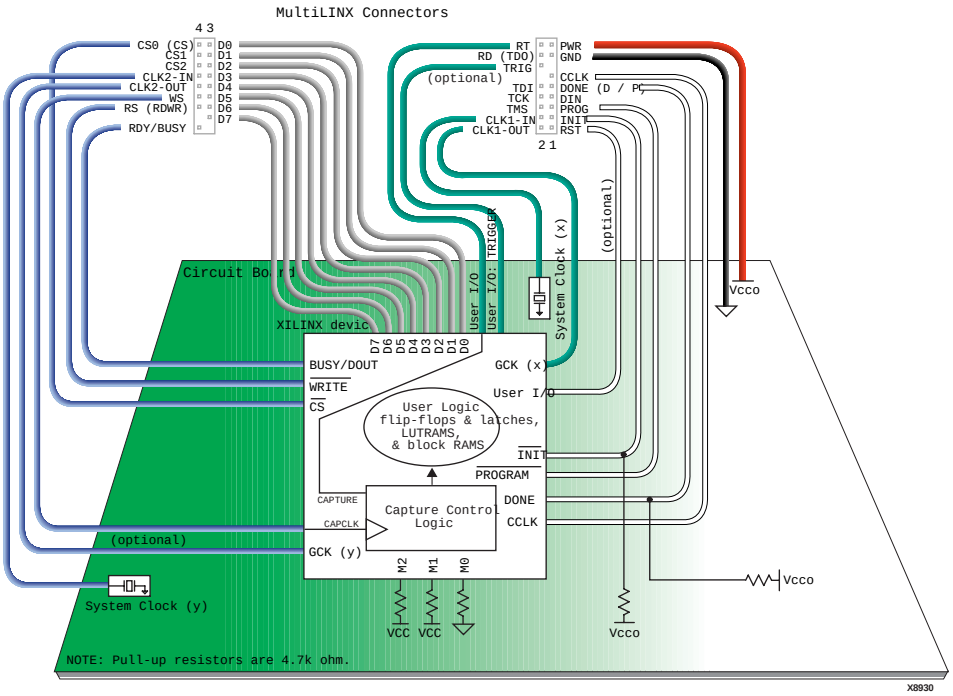


Figure 2-16 SelectMAP Mode (Virtex)

JTAG Mode

In JTAG mode Synchronous Probing is not available.

Chapter 3

FPGA Design Demonstration Board

The FPGA Demonstration Board (Part Number: HW-FPGABOARD) is a stand-alone board for experimenting and developing prototypes using the Xilinx FPGA architecture. The FPGA Demonstration Board allows you to become familiar with some of the Xilinx FPGA device families and the Xilinx software development system. This chapter contains the following sections.

- "Demonstration Board Overview"
- "General Components"
- "XC4003E Components"
- "XC3020A Components"
- "Mode Switch Settings"
- "Demonstration Board Operation"

Demonstration Board Overview

The following sections detail the device and software support for the FPGA Demonstration Board, as well as describing the board's general features.

Device Support

The FPGA Demonstration Board supports the following Xilinx FPGA families.

- XC3000A, XC3000L
- XC3100A
- XC4000E

- Spartan™ Product Families

Note: The Spartan series is a low-cost FPGA family, based on the XC4000 devices. See the Xilinx web site or the *1998 Xilinx Databook* for more information about Spartan.

Download Cable Support

The FPGA Demonstration Board is shipped with two short "ribbon" cables which can be used to configure FPGAs. You can also configure designs with the XChecker Cable (slave serial mode), the onboard XC1700PD8 PROM (master serial mode), or the Parallel Cable III, a JTAG Cable. For more information on connecting XChecker Cable or the Parallel Cable III, see the “Cable Hardware” chapter.

Software Support

Two Xilinx software packages can be used with this demonstration board.

- XChecker is a command line text-only program, available for both PC and Workstation platforms. The XChecker Software supports the XChecker Cable only.
- Hardware Debugger, a GUI-type program, is the recommended software for use with this demonstration board. For more information on using Hardware Debugger with the demonstration board, see the “Demonstration Board Operation” section.

Board Features

The FPGA Demonstration Board is shipped with two devices, the XC3020APC68 and XC4003EPC84. The board has the following features.

- One socket for an XC3000 PC68 device
- One socket for an XC4000 PC84 device
- One XC1700PD8 socket for each FPGA
- An XChecker / Parallel Cable III header for each FPGA
- Daisy-chain configuration with the XC4000 device at the head of the chain

- Total of three 8-pin DIP switches to set up the XC4000 and XC3000 FPGAs, as shown in the following table.

Table 3-1 DIP Switch Configuration

XC3000 SW1	XC4000 SW2	Switch
INP	1	PWR
MPE	MPE (multiple configurations)	2
SPE	SPE (single configuration)	3
M0	M0	4
M1	M1	5
M2	M2	6
MCLK	RST	7
DOUT	INIT	8

- 16 I/O lines that connect the two FPGAs
- An external relaxation oscillator circuit available to the user for the XC3000
- The XC4000 OSC4 library symbol, which uses pin 19 of the XC4003E to drive the XC3000 TCLKIN on pin 11 of the XC3020A
- The XC4000 OSC4, uses pin 13 to drive the XC3000 alternate clock buffer (BCLKIN) on pin 43
- Eight general purpose input switches to provide logic inputs to the FPGAs
- Program, Reset, and Spare Active Low push-button switches, which are common to both FPGAs
- An XC3000A display for the XC3000 device. The display uses eight LED bars in one row and one 7-segment LED, as shown in the following figure.
- An XC4000A display for the XC4000 device. The display uses eight LED bars in one row and two 7-segment LEDs, as shown in the following figure.
- Space for an optional +5 V regulator for battery operation
- Space for an optional crystal oscillator
- Headers for FPGA probe points

- A prototype area on the PC board

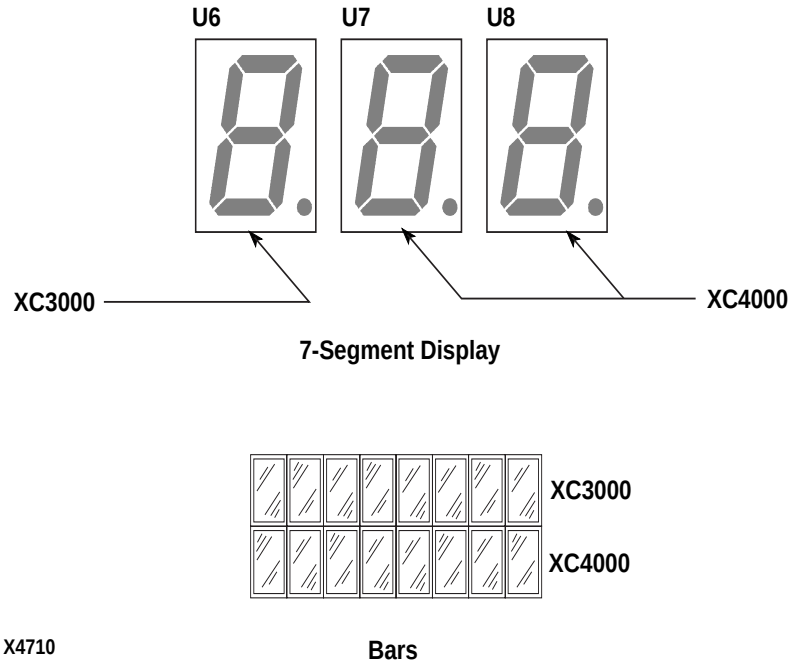


Figure 3-1 FPGA Demonstration Board Displays

General Components

This section describes the common components that are found on the FPGA Demonstration Board. The following figure shows the component layout of the FPGA Demonstration Board.

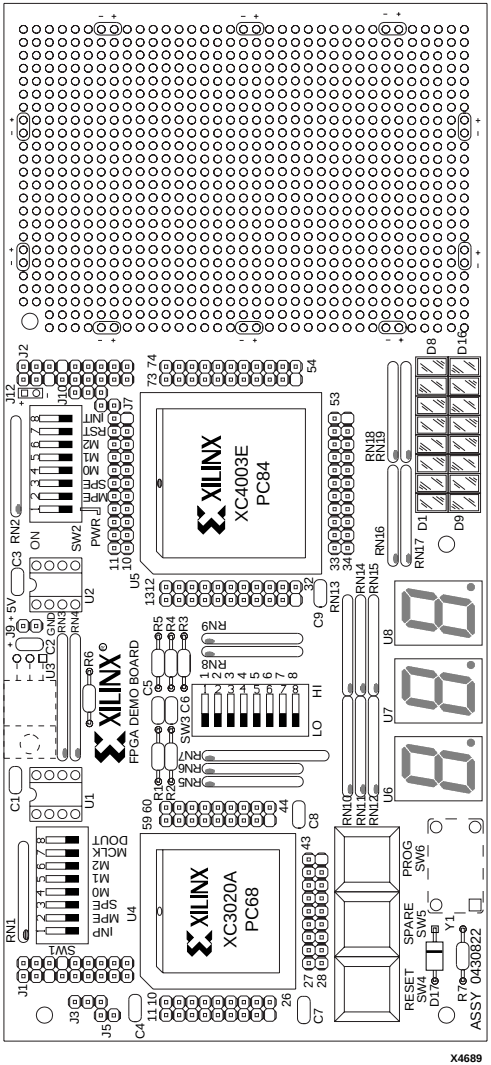


Figure 3-2 FPGA Demonstration Board

+5 V Power Connector (J9)

A regulated +5 volts and ground connected to the FPGA Demonstration Board through connector J9. Pin 1 (square pad) is +5 V and pin 2

is ground. The power supply should provide at least 250 mA of current to drive the LED displays.

Unregulated Power Input (J12)

This input provides a way to power the FPGA Demonstration Board from an unregulated source, such as a 9 V battery or an AC adapter. Typically, the input should be 7VDC - 12VDC at 250 mA. You must consider the power dissipation requirements of the U3 voltage regulator if the voltage input is greater than 9 V.

The J12 unregulated power input provides two holes to connect the unregulated power source. The hole with the square pad, marked with a "+" is the positive input. The other hole, marked with a "-" is circuit ground. The positive input is connected through the power on-off switch SW2–1 to U3–1, which is the optional +5 V regulator. U3 must be installed to use this input.

+5 V Regulator Option (U3)

You can install a three terminal +5 V regulator, such as the LM2940CT shown in the following figure. This regulator powers the demonstration board from an unregulated power supply, such as a +9 V battery. Pin 1 (square pad) is Vin, pin 2 is ground, and pin 3 is +5 V out.

Note Insulate the metal heat sink tab of the regulator from traces and vias on the PCB.

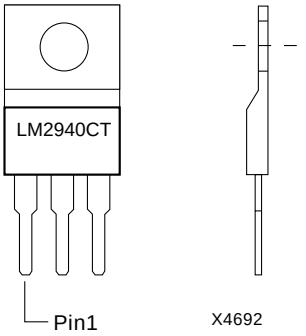


Figure 3-3 LM2940CT +5 V Regulator

RESET Pushbutton (SW4)

Depending on how the Reset signal routing is configured the RESET pushbutton switch can apply an active-Low Reset signal to the FPGAs and configuration PROMs. Reset is normally pulled High through a 27 kilohm resistor.

SPARE Pushbutton (SW5)

The SPARE pushbutton applies an active-Low signal to the XC3020A on pin 16, and to the XC4003E on pin 18. You can isolate these pins from the switch by using the trace-cut options on the solder side of the board. The trace-cut options appear as point-to-point triangles; the trace-cut option for the XC3020A is under its socket and the trace-cut option for the XC4003E is under R3. The SPARE signal is pulled High through a 27 kilohm resistor.

PROG Pushbutton (SW6)

The PROG pushbutton applies an active-Low signal to the DONE/PROGRAM input on the XC3020A FPGA socket at pin 45 and to the PROGRAM input on the XC4003E FPGA socket at pin 55. The PROG signal is normally pulled High through a 13.5 kilohm resistor.

Eight General-Purpose Input Switches (SW3)

Eight switches connect to eight general-purpose inputs on both the XC3020A and the XC4003E FPGAs. These switches provide logic input to the FPGAs. An FPGA input pin is set to a logic "1" when a switch is on, and a logic "0" when a switch is off. See the following figure for a diagram.

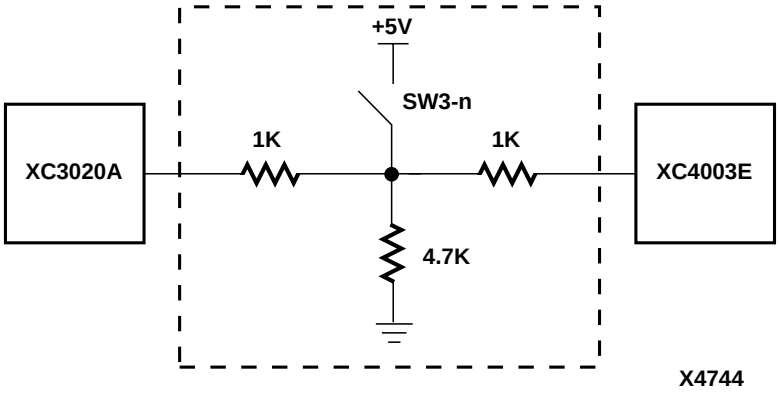


Figure 3-4 FPGA Demonstration Board General-Purpose Switch

The FPGA pins connected to this switch are intended for use as inputs. However, each FPGA pin has a 1 kilohm resistor that isolates it from the switch, so it is possible to define the pins as outputs. You can also drive the pins from an external source by connecting that signal to the FPGA probe point header. The following table lists the FPGA pin connections.

Table 3-2 Input Switch Pin Connections

Switch	XC3020A	XC4003E
SW3–1	11	19
SW3–2	13	20
SW3–3	15	23
SW3–4	17	24
SW3–5	19	25
SW3–6	21	26
SW3–7	23	27
SW3–8	24	28

Seven-Segment Displays (U6, U7, U8)

Three seven-segment displays are included with the leftmost display (U6) connect to the XC3020A FPGA. The rightmost two displays (U7 and U8) connect to the XC4003E device.

Each LED segment is turned on by driving the corresponding FPGA pin 'LOW' with a logic '0.' The decimal point on U8 connects to the INIT pin of the XC4003E (pin 41) and serves as a programming error indicator. The decimal point should be on while the FPGA is in its internal clearing state, then it should remain off during configuration. If the decimal point comes back on, a programming error has occurred.

The decimal points on U6 and U7 are tied to the Low During Configuration (LDC) pins of the XC3020A and XC4003E, respectively. The decimal points are on while the FPGAs wait to be configured.

The following table shows the I/O pin definitions. The following figure shows the seven-segment display of the FPGA demonstration board.

Table 3-3 Seven-Segment I/O Connections

Display Segment	XC3020A	XC4003E	XC4003E
	U6	U7	U8
a	38	39	49
b	39	38	48
c	40	36	47
d	56	35	46
e	49	29	45
f	53	40	50
g	55	44	51
decimal point	30	37	41

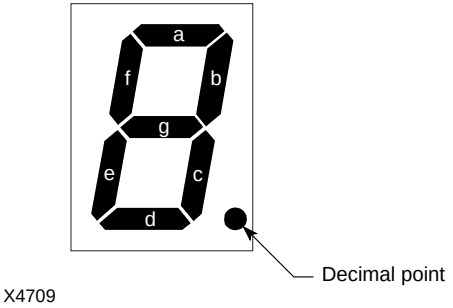


Figure 3-5 Seven-Segment Display

LED Indicators (D1-D8, D9-D16)

Eight LEDs are connected to the I/O pins of each FPGA. Pins D1 through D8 connect to the XC3020A, and D9 through D16 connect to the XC4003E. You can turn on an LED by driving its corresponding FPGA pin Low with a logic "0." The following table shows the pin connections for the LED indicators.

Table 3-4 LED Indicators for XC3020A and XC4003E

LED	XC3020A Pin	LED	XC4003E Pin
D1	37	D9	61
D2	36	D10	62
D3	41	D11	65
D4	33	D12	66
D5	32	D13	57
D6	31	D14	58
D7	28	D15	59
D8	29	D16	60

I/O Line Connections

There are 16 I/O lines that connect the XC3020A and XC4003E FPGAs. These are shown in the following table.

Table 3-5 I/O Line Connections for XC3020A and XC4003E Devices

I/O Line	XC3020A Pin	XC4003E Pin
0	61	10
1	62	9
2	63	8
3	64	7
4	65	6
5	66	5
6	67	4
7	68	3
8	2	84
9	3	83
10	4	82
11	5	81
12	6	80
13	7	79
14	8	78
15	9	77

Optional Crystal Oscillator (Y1)

You can add a standard 4-pin crystal oscillator to the FPGA Demonstration Board. The oscillator output drives the XC3020A XTL2 input at pin 43 and the XC4003E PGCK1 input at pin 13.

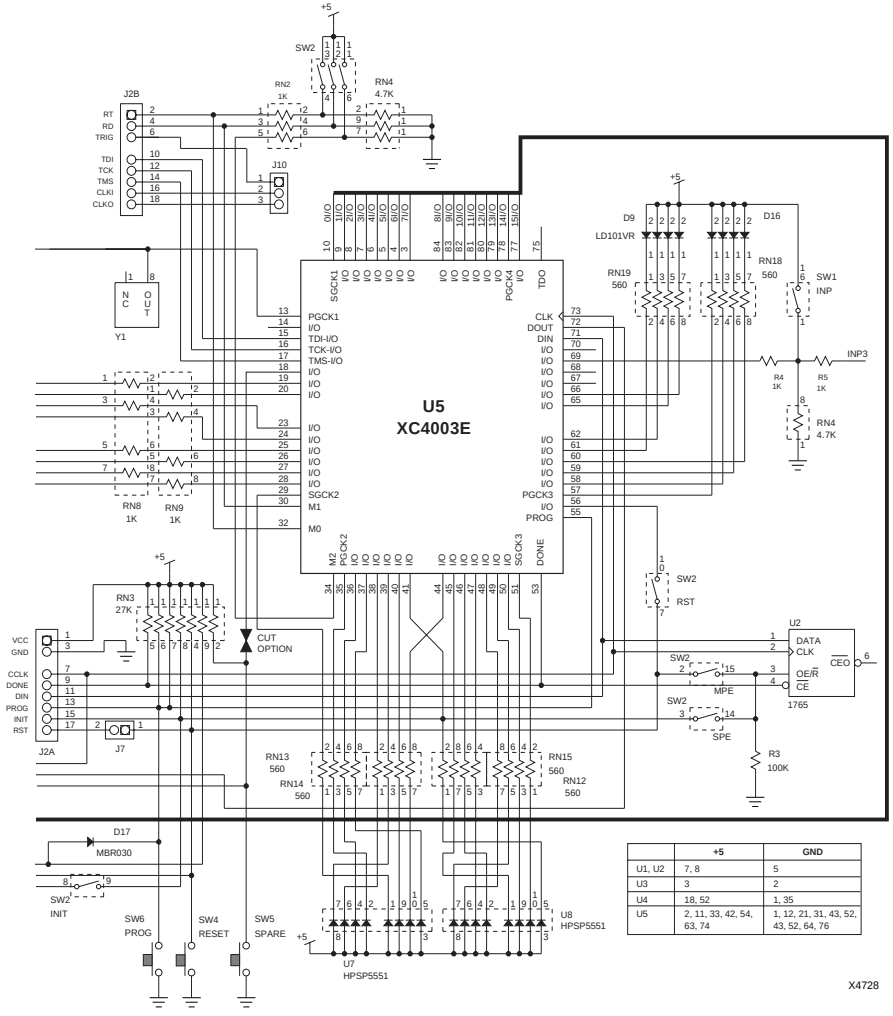
Prototype Area

The Prototype area is a 0.1-inch grid of holes where you can add additional circuitry to the demonstration board. A +5 V bus (compo-

nent side) and a ground bus (solder side) are available on the perimeter of this area. There are also locations for filter capacitors.

XC4003E Components

This section describes the components on the FPGA Demonstration Board which are used with the XC4003E device. The following schematic shows this device.



	+5	GND
U1, U2	7, 8	5
U3	3	2
U4	18, 52	1, 35
U5	2, 11, 33, 42, 54, 63, 74	1, 12, 21, 31, 43, 52, 43, 52, 64, 76

Figure 3-6 XC4003E Schematic

XC4003E FPGA and Socket (U5)

The XC4003E FPGA occupies socket U5 on the demonstration board.

XC4003E Probe Points

All pins of the XC4003E connect to the headers that surround the FPGA socket. These pins provide convenient points for probing signals or making wirewrap connections to other circuitry, including the prototype area. Pin numbering increases from the inside row to the outside, counterclockwise. See the corners of each header for the starting number of that header.

XC4003E Configuration Switches (SW2)

The following sections describe each of the SW2 switches. For more information on configuring the XC40003E device, see the "Mode Switch Settings" section.

PWR-Power (SW2–1)

This switch turns the unregulated power input on or off to the +5 V regulator U3.

MPE-Multiple Program Enable (SW2-2)

With MPE turned on and SPE turned off, the configuration PROM (U2) is reset by the RESET pushbutton (SW4). Configuration mode must be set to master-serial. After a Reset or powerup, the first bitstream stored in the serial PROM is loaded into the XC4003E. Pressing RESET resets the serial PROM address pointer. Pressing PROG (SW6) loads the XC4003E with the first bitstream again. If you press PROG without pressing RESET, the XC4003E is loaded with the next bitstream that is stored in the serial PROM. The size of the serial PROM limits the number of bitstreams that can be sequentially loaded.

SPE-Single Program Enable (SW2-3)

With SPE turned on and MPE turned off, the configuration PROM (U2) is reset by the XC4003E's INIT output, which is driven Low whenever you press PROG (SW6). The first bitstream stored in the serial PROM is loaded into the XC4003E.

Note MPE and SPE must not be on at the same time, one must be off when the other is on. MPE and SPE are only used in conjunction with

the serial PROMs. The serial PROMs must be configured as OE / Reset to allow MPE and SPE to function properly.

M0, M1, M2-Mode Pins (SW2-4,5,6)

These three switches must be on to configure the XC4003E using the XChecker / Parallel Cable III. When these switches are on, the FPGA is in slave serial mode. To configure the XC4003E from the onboard serial PROM, these three switches must be off. This places the FPGA in master serial mode.

RST-Reset (SW2-7)

When this switch is on, it connects the RESET pushbutton (SW4) to XC4003E pin 56.

INIT-Initialize (SW2-8)

When this switch is on, it connects the XC3020A INIT pin to the XC4003E INIT pin. This connection is used to configure FPGAs in a daisy chain with the XC4003E at the head of the chain.

Note INIT should only be used to configure FPGAs in a daisy chain.

XChecker/Parallel Cable III Connector J2

The following table provides a detailed description of the J2 XChecker / Parallel Cable III connector.

Table 3-6 XChecker/Parallel Cable III Connector J2

Pin	Name	Function	Pin	Name	Function
J2-1[a]	VCC	Supplies +5 V to the cable.	J2-2	RT	Read Trigger allows XChecker Cable to trigger a readback of the XC4003E. Connects to XC4003E pin 32.
J2-3[a]	GND	Supplies ground reference to the cable.	J2-4	RD	Used by XChecker Cable for readback data. Connects to XC4003E pin 30.

Table 3-6 XChecker/Parallel Cable III Connector J2

Pin	Name	Function	Pin	Name	Function
J2-5	N.C.[b]		J2-6	TRIG	XChecker Cable input that allows an external event to trigger readback of the XC4003E or output a burst of clocks to the XC4003E. Connects to tiepoint J10–1.
J2-7[a]	CCLK	Provides the clock during configuration or readback. Connects to XC4003E input pin 73.	J2-8	N.C.[b]	
J2-9[a]	DONE	Indicates when configuration is complete. Connects to XC4003E output pin 53.	J2-10	TDI	Inputs boundary-scan data to the XC4003E. Connects to XC4003E pin 15.
J2-11[a]	DIN	Provides configuration data during configuration. Connects to XC4003E DIN input pin 71.	J2-12	TCK	Input boundary scan clock to the XC4003E. Connects to pin 16.
J2-13[a]	PROG	Provides program pulse causing the FPGA to configure. Connects to XC4003E PROG input pin 55.	J2-14	TMS	Boundary scan mode input to the XC4003E. Connects to pin 17.

Table 3-6 XChecker/Parallel Cable III Connector J2

Pin	Name	Function	Pin	Name	Function
J2-15	INIT	Goes Low if CRC error occurs during configuration. Connects to XC4003E INIT pin 41.	J2-16	CLK1	A system clock input to XChecker Cable to be controlled and output on CLK0. Connects to tiepoint J10-2.
J2-17	RST	Connects to jumper J7. If connected, allows XChecker Cable to provide a Reset input (same as pressing the Reset button).	J2-18	CLK0	A system clock output controlled by XChecker Cable. Used to single-step or burst clocks to the XC4003E. Connects to tiepoint J10-3.

a. Denotes pins supported by the Parallel Cable III

b. No pin connection

The D/P wire from the FPGA header on the Parallel Cable III is connected to J2-9 DONE pin.

Jumper J7 and Tiepoints J10 (1-3)

Jumper J7 allows the XChecker signal RST on J2-17 to drive the reset line on the demonstration board. Tiepoint pins jumper the following XChecker signals into the circuit. Tiepoint J10-1 connects to TRIG on J2-6; Tiepoint J10-2 connects to CLK1 on J2-16; and, Tiepoint J10-3 connects to CLK0 on J2-18. See the preceding table for more details on the cable and pin connections.

Serial PROM Socket (U2)

This serial PROM configures the XC4003E or the XC4003E and XC3020A connected in a daisy chain. The configuration mode must be in the master serial mode to configure from the serial PROM.

XC3020A Components

This section describes the components on the FPGA Demonstration Board which are for the XC3020A device. The following figure is a schematic of the FPGA Demonstration Board utilizing this device.

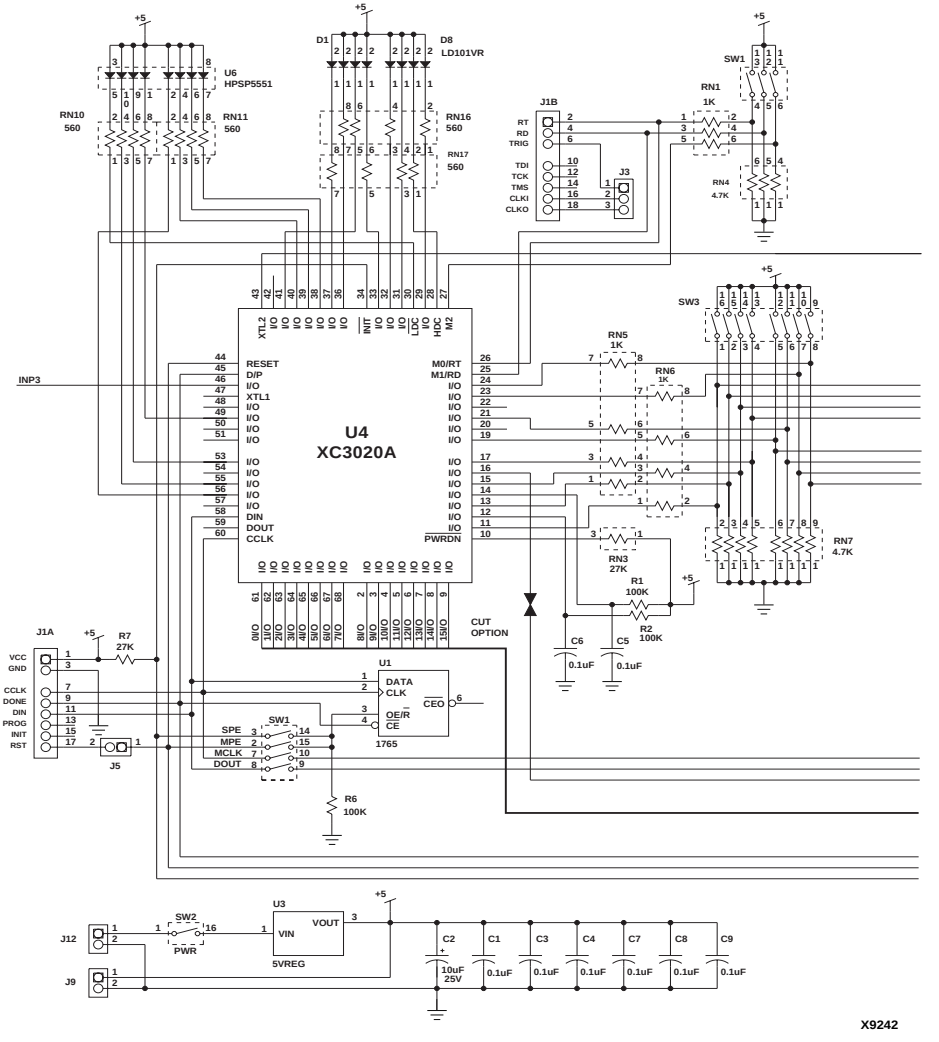


Figure 3-7 XC3020A Schematic

XC3020A FPGA and Socket (U4)

The XC3020A FPGA occupies socket U4 on the demonstration board.

XC3020A Probe Points

All pins of the XC3020A FPGA connect to the headers that surround the FPGA socket. These pins provide convenient points for probing signals or making wirewrap connections to other circuitry, such as the prototype area. Pin numbering increases from the inside row to the outside, counterclockwise. See the corners of each header for the starting number of that header. Refer to Table 3-5 for information.

The XC3020A I/O pins 2 through 9 and 61 through 68 connect to XC4003E pins 3 through 10 and 77 through 84, respectively. The XC3020A pins share the XC4003E probe points header.

XC3020A Configuration Switches (SW1)

The following sections describe each of the SW1 switches. For more information on configuring the XC3020A device, see the “Mode Switch Settings” section.

INP-Input Switch (SW1-1)

INP is an extra switch, which you can connect to provide an extra logic input to the XC3020A pin 46 and the XC4003E pin 69. The FPGA input pins are set to a logic "1" when the switch is on and a logic "0" when the switch is off.

The FPGA pins connected to this switch are intended for use as inputs. However, the pins have a 1 kilohm resistor that isolates them from the switch. Therefore, the pins can be defined as outputs. It is also possible to drive the pins from an external source by connecting the source signal to the FPGA probe point header. See the following figure for details.

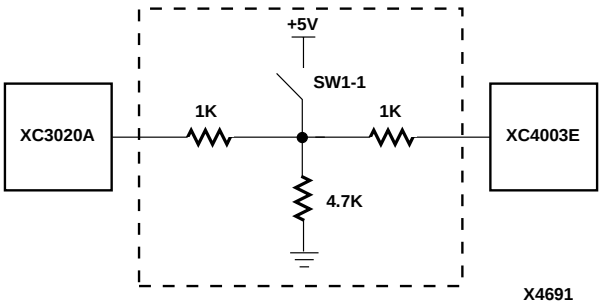


Figure 3-8 Configuration Switch SW1

MPE-Multiple Program Enable (SW1-2)

When MPE is on and SPE is off, the configuration PROM (U1) is reset by the RESET pushbutton (SW4). Configuration must be set to the master serial mode. After a Reset or powerup, the first bitstream stored in the serial PROM is loaded into the XC3020A FPGA. IF you press RESET, the serial PROM address pointer is reset. If you press PROG (SW6), the XC3020A is loaded with the first bitstream again. If you press PROG, and do not press RESET, the XC3020A is loaded with the next bitstream stored in the serial PROM. The number of bitstreams that can be sequentially loaded is limited by the size of the serial PROM.

SPE-Single Program Enable (SW1-3)

When SPE is on and MPE is off, the configuration PROM (U1) is reset by the XC3020A's INIT output, which is driven Low whenever you press PROG (SW6). The first bitstream stored in the serial PROM is loaded into the XC3020A FPGA.

Note MPE and SPE must not be on at the same time. MPE and SPE are only used in conjunction with the serial PROMs. The serial PROMs must be configured as OE/RESET to allow MPE and SPE to function properly.

M0, M1, M2-Mode Pins (SW1-4,5,6)

To configure the XC3020A using the XChecker/Parallel Cable III these switches must be on. This places the FPGA in slave serial mode.

To configure from the onboard serial PROM, these switches must be off. This places the FPGA in master serial mode.

MCLK-Master Clock (SW1-7)

When this switch is on, it connects the XC4003E configuration clock (pin 73) to the configuration clock on the XC3020A (pin 60). This connection is used to configure FPGAs in a daisy chain with the XC4003E at the head.

DOUT-Data Out (SW1–8)

When this switch is on, it connects the XC4003E data out line (pin 72) to the data in line of the XC3020A. This connection configures FPGAs in a daisy chain with the XC4003E at the head.

Note MCLK and DOUT should only be used to configure the FPGAs in a daisy chain.

XChecker/Parallel Cable III Connector J1

The following table describes the pins and functions of the XChecker / Parallel Cable III J1 connector.

Table 3-7 XChecker/Parallel Cable III Connector J1

Pin	Name	Function	Pin	Name	Function
J1–1[a]	VCC	Supplies +5 V to the XChecker Cable.	J1–2	RT	Allows XChecker Cable to trigger a read-back of the XC3020A. Connects to XC3020A pin 26.
J1–3[a]	GND	Supplies ground reference to XChecker Cable.	J1–4	RD	Used by XChecker Cable for readback data. Connects to XC3020A pin 25.

Table 3-7 XChecker/Parallel Cable III Connector J1

Pin	Name	Function	Pin	Name	Function
J1–5	N.C.[b]		J1–6	TRIG	XChecker Cable input that allows an external event to trigger read-back of the XC3020A or outputting a burst of clocks to the XC3020A. Connects to tiepoint J3–1.
J1–7[a]	CCLK	Provides clock during configuration or readback. Connects to XC3020A input pin 50.	J1–8	N.C.[b]	
J1–9[a]	D / P	Starts configuration and indicates completion. Connects to XC3020A DONE / PROGRAM pin 45.	J1–10	N.C.[b]	
J1–11[a]	DIN	Provides configuration data during configuration. Connects to XC3020A DIN input pin 58.	J1–12	N.C.[b]	
J1–13	N.C.[b]		J1–14	N.C.[b]	

Table 3-7 XChecker/Parallel Cable III Connector J1

Pin	Name	Function	Pin	Name	Function
J1–15	N.C.b[b]		J1–16	CLKI	System clock input to XChecker Cable to be controlled and output on CLKO. Connects to tiepoint J3–2.
J1–17	RST	Connects to jumper J5. If connected, allows XChecker Cable to provide a Reset input (same as pressing Reset button).	J1–18	CLKO	System clock output controlled by XChecker Cable; used to single-step or burst clocks to the XC3020A. Connects to tiepoint J3–3.

a. Denotes pins supported by the Parallel Cable III

b. No pin connection

Jumper J5 allows the XChecker Cable signal RST on J1-17 to drive the reset line on the demonstration board. Tiepoint pins jumper the following XChecker Cable signals into your circuit. Tiepoint J3-1 connects to TRIG on J1-6; Tiepoint J3-2 connects to CLK1 on J1-16; and, Tiepoint J3-3 connects to CLK0 on J1-18. See the preceding table for more information on cable connections.

Serial PROM Socket (U1)

This serial PROM configures the XC3020A. You must use the master serial mode to configure from the serial PROM.

Relaxation Oscillator Components (R1 C5, R2 C6)

R1, C5 and R2, C6 are two RC networks that connect to the XC3020A at pins 12 and 14. These RC networks are for use in a relaxation oscillator such as the circuit is shown in the following figure.

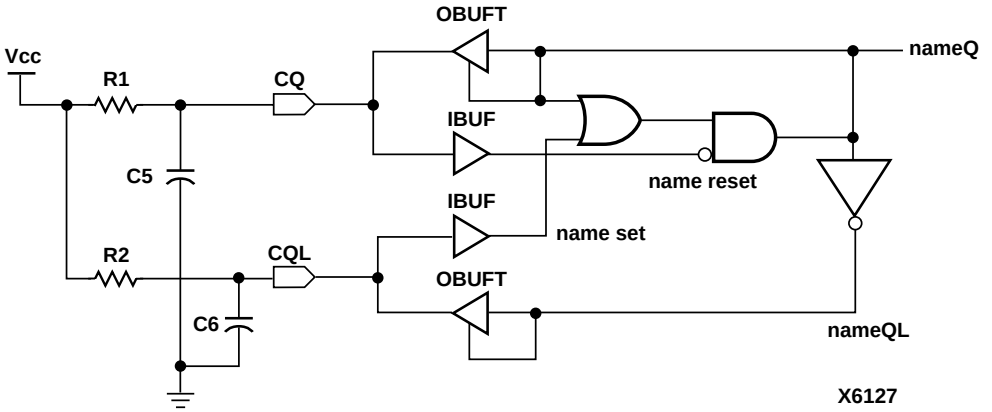


Figure 3-9 Relaxation Oscillator Schematic

With the components provided, R1 = R2 = 100 kilohms and C5 = C6 = 0.1uF, the oscillator generates an output frequency of approximately 100 Hz.

The following figure shows the RC Network waveforms.

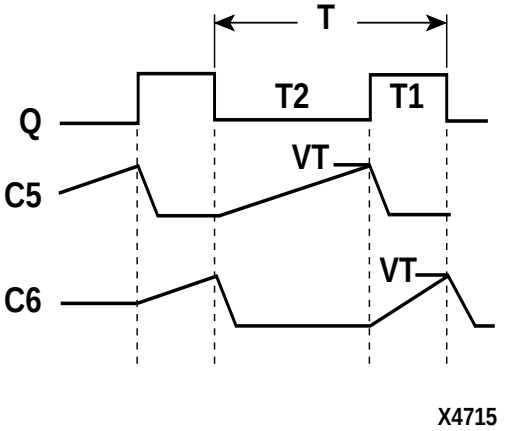


Figure 3-10 RC Network Waveforms

The formula for calculating the RC network is as follows.

T = T1 + T2 = N ((R1C5) + (R2C6))

where:

N = approximately 0.35 for TTl threshold

= approximately 0.75 for CMOS threshold

when the FPGA allows each capacitor to discharge during the opposite timing phase.

Mode Switch Settings

This section describes the SW1 and SW2 switch settings for configuring the XC3020A and XC4003E devices.

- From the XChecker / Parallel Cable III
- From the serial PROM (single program)
- From the serial PROM (multiple program)
- In a daisy chain

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A FPGA from the XChecker or Parallel Cable III.

Table 3-8 Configuring the XC3020A from the XChecker/Parallel Cable III

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	OFF	SW2–2	MPE	X
SW1–3	SPE	OFF	SW2–3	SPE	X
SW1–4	M0	ON	SW2–4	M0	X
SW1–5	M1	ON	SW2–5	M1	X
SW1–6	M2	ON	SW2–6	M2	X
SW1–7	MCLK	OFF	SW2–7	RST	
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don‘t care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC4003E FPGA from the XChecker / Parallel Cable III.

Table 3-9 Configuring the XC4003E from the XChecker/Parallel Cable III

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	X	SW2–2	MPE	OFF
SW1–3	SPE	X	SW2–3	SPE	OFF
SW1–4	M0	X	SW2–4	M0	ON
SW1–5	M1	X	SW2–5	M1	ON
SW1–6	M2	X	SW2–6	M2	ON
SW1–7	MCLK	OFF	SW2–7	RST	X
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don't care

When you configure both the XC3020A and XC4003E devices using the XChecker / Parallel Cable III, configure the XC4003E FPGA first. If you configure the XC3020A first, its configuration is lost when the XC4003E FPGA configures because the PROG signal connects directly to the XC4003E PROG input and through a diode to the XC3020A DONE / PROG input.

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A FPGA from the serial PROM.

Table 3-10 Configuring the XC3020A from the Serial PROM (Single Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	OFF	SW2–2	MPE	X
SW1–3	SPE	ON	SW2–3	SPE	X
SW1–4	M0	OFF	SW2–4	M0	X
SW1–5	M1	OFF	SW2–5	M1	X
SW1–6	M2	OFF	SW2–6	M2	X

Table 3-10 Configuring the XC3020A from the Serial PROM (Single Program)

Switch	Name	Position	Switch	Name	Position
SW1–7	MCLK	OFF	SW2–7	RST	X
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don't care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC4003E FPGA from the serial PROM.

Table 3-11 Configuring the XC4003E from the Serial PROM (Single Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	X	SW2–2	MPE	OFF
SW1–3	SPE	X	SW2–3	SPE	ON
SW1–4	M0	X	SW2–4	M0	OFF
SW1–5	M1	X	SW2–5	M1	OFF
SW1–6	M2	X	SW2–6	M2	OFF
SW1–7	MCLK	OFF	SW2–7	RST	X
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don't care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A FPGA from the serial PROM (multiple program).

Table 3-12 Configuring the XC3020A from the Serial PROM (Multiple Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	ON	SW2–2	MPE	X
SW1–3	SPE	OFF	SW2–3	SPE	X
SW1–4	M0	OFF	SW2–4	M0	X
SW1–5	M1	OFF	SW2–5	M1	X

Table 3-12 Configuring the XC3020A from the Serial PROM (Multiple Program)

Switch	Name	Position	Switch	Name	Position
SW1–6	M2	OFF	SW2–6	M2	X
SW1–7	MCLK	OFF	SW2–7	RST	X
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don‘t care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC4003E FPGA from the serial PROM (multiple program).

Table 3-13 Configuring the XC4003E from the Serial PROM (Multiple Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	X	SW2–2	MPE	ON
SW1–3	SPE	X	SW2–3	SPE	OFF
SW1–4	M0	X	SW2–4	M0	OFF
SW1–5	M1	X	SW2–5	M1	OFF
SW1–6	M2	X	SW2–6	M2	OFF
SW1–7	MCLK	OFF	SW2–7	RST	X
SW1–8	DOUT	OFF	SW2–8	INIT	OFF

X indicates don’t care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A and XC4003E FPGAs in a daisy-chain from the XChecker / Parallel Cable III.

Table 3-14 Configuring the XC3020A and XC4003E in a Daisy Chain from the XChecker/Parallel Cable III

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	OFF	SW2–2	MPE	OFF
SW1–3	SPE	OFF	SW2–3	SPE	OFF

Table 3-14 Configuring the XC3020A and XC4003E in a Daisy Chain from the XChecker/Parallel Cable III

Switch	Name	Position	Switch	Name	Position
SW1–4	M0	ON	SW2–4	M0	ON
SW1–5	M1	ON	SW2–5	M1	ON
SW1–6	M2	ON	SW2–6	M2	ON
SW1–7	MCLK	ON	SW2–7	RST	X
SW1–8	DOUT	ON	SW2–8	INIT	ON

X indicates don‘t care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A and XC4003E FPGAs in a daisy-chain from the serial PROM (single program).

Table 3-15 Configuring the XC3020A and XC4003E in a Daisy Chain from the Serial PROM (Single Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	OFF	SW2–2	MPE	OFF
SW1–3	SPE	OFF	SW2–3	SPE	ON
SW1–4	M0	ON	SW2–4	M0	OFF
SW1–5	M1	ON	SW2–5	M1	OFF
SW1–6	M2	ON	SW2–6	M2	OFF
SW1–7	MCLK	ON	SW2–7	RST	X
SW1–8	DOUT	ON	SW2–8	INIT	ON

X indicates don‘t care

The following table lists the names and positions of the SW1 and SW2 switches for configuring the XC3020A and XC4003E FPGAs in a daisy-chain from the serial PROM (multiple program).

Table 3-16 Configuring the XC3020A and XC4003E in a Daisy Chain from the Serial PROM (Multiple Program)

Switch	Name	Position	Switch	Name	Position
SW1–1	INP	X	SW2–1	PWR	X
SW1–2	MPE	OFF	SW2–2	MPE	ON
SW1–3	SPE	OFF	SW2–3	SPE	OFF
SW1–4	M0	ON	SW2–4	M0	OFF
SW1–5	M1	ON	SW2–5	M1	OFF
SW1–6	M2	ON	SW2–6	M2	OFF
SW1–7	MCLK	ON	SW2–7	RST	X
SW1–8	DOUT	ON	SW2–8	INIT	ON

X indicates don‘t care

Demonstration Board Operation

This section describes how to use the XChecker download cable with the FPGA Demonstration Board and Hardware Debugger software for device configuration. Explicit cable connection information is included in the “Cable Hardware” chapter.

The information in this section applies to both the XC3020A and the XC4003E devices. However, for clarity references are only made to the XC4003E FPGA.

Note The Parallel Cable III can also be used for FPGA configuration. For Parallel Cable III connection information, refer to the “External Power for the MultiLINX Cable” section of the “Cable Hardware” chapter.

Demonstration Designs

Demonstration designs are supplied with Xilinx Foundation™ and Alliance™ Series software. You can view or edit the demonstration designs. Before editing, you must compile the input files with your design implementation software.

These example designs incorporate the ability of the XC4003E to build ROM out of function generators. The ROM macros store a sequence of patterns that are displayed on the 7-segment displays and the LED bar graphs of the FPGA Demonstration board.

Please read the text files that accompany these designs. Design schematics are available by calling the Xilinx Technical Support Hotline. You can also access schematics through the Xilinx web site, located at http://www.xilinx.com.

Design Downloading Checklist

You must follow the recommended design flow to assure proper operation. Make backups before making changes to any demonstration design files.

1. Produce a routed design, design_name using a design entry tool and the appropriate place and route tool.

   If you want a global Reset signal in your XC4000 designs, you must include the Startup symbol in your design and select the location of the RESET pin. Attach pin 56 to an inverter and the GSR pin on the Startup symbol. GSR is active-High so you must include an inverter between the pad and the Startup symbol.

2. Generate a bitstream for the design, design_name.bit with the appropriate configuration options using the BitGen program.

3. Optionally, create a PROM File.

4. Generate a PROM file (design_name.mcs, design_name.tek, or design_name.exo) using the PROMGen program. This step is optional since the XChecker and Hardware Debugger software can use the design.bit file as input.

5. Connect the XChecker Cable to your host system.

6. Connect the XChecker Cable to your target system.

   The XChecker Cable draws its power from the target system through the VCC and GND wires. Therefore, power to the XChecker Cable and the target FPGA must be stable. Do not connect the XChecker Cable pins to any signals before connecting VCC and ground to the FPGA Demonstration Board.

   When you use the XChecker Cable to download, only one of the two-keyed connectors are needed.

7. Connect XChecker to J1 (for the XC3020A) and J2 (for the XC4003E) on the FPGA Demonstration Board.
8. Set the mode switches.

   When you use the XChecker Cable, the M0, M1, and M2 switches must be on. This setting causes the device to be in the serial slave mode. Refer to the Table 3-14 for the switch settings necessary to configure a daisy chain.
9. Power up the target system.
10. Start your software package.

For information on starting the Hardware Debugger software, see the"Starting Hardware Debugger" section.

Loading with a Configuration PROM

If you already have a design programmed in a PROM, skip to step 5. You can also view or edit the demonstration designs supplied with the Xilinx software tools.

Note Make backups before making changes to any demonstration design files.

1. Place and route the design.

   Produce a routed design, *design_name* using a design entry tool and the appropriate place and route tool.
2. Generate a configuration bitstream for the design, design_name.bit with the appropriate configuration options using the BitGen program.
3. Create a PROM file.

   Generate a PROM file (design_name) using the PROMGen program. See the PROMGen documentation in the Development System Reference Guide to create a PROM file.

   Note The XC1700 series of configuration serial PROMs must be programmed with the reset polarity set for active-Low.
4. Place the PROM on the FPGA Demonstration Board.

   After you have a PROM that has a configuration bitstream programmed into it, place it into the FPGA Demonstration Board

with power off. Use the appropriate demonstration board socket for your device.

- U2 socket: XC4003E devices
- U2 socket: XC4003E and XC3020A devices in a daisy chain with the XC4003E at the head of the chain
- U1 socket: XC3020A devices

5. Set the mode switches.

   When you use the serial PROMs, the M0, M1, and M2 switches must be off. This setting causes the device to be in the active master serial mode. Set the MPE, SPE, and RST switches to the desired positions. Refer to theTable 3-15 and the Table 3-16 for switch settings required to configure a daisy chain.

6. Load the FPGA.
7. After you insert the PROM into the socket and set the configuration switches, apply power to the FPGA Demonstration Board.

   This step configures the FPGA; when the DONE pin goes High, it indicates that the design logic is active.

8. Start your configuration software.

For information on starting the Hardware Debugger software, see the following section.

Starting Hardware Debugger

The following section includes a checklist for opening the Hardware Debugger software. For further information, consult the *Hardware Debugger Guide*.

1. Open your Alliance or Foundation software.
2. From within Xilinx Design Manager (version M1.0 or later), select Hardware Debugger from the tools menu. You can also start the Hardware Debugger from the operating system prompt by entering the following command.

   `hwdebugr` *`design_name`*

   When you start the Hardware Debugger, the port where the cable is plugged in is located, and the baud rate is set to the maximum allowed by the platform.

3. A message window indicates that the FPGA design is loading. When loading is complete, the Hardware Debugger indicates that the DONE pin went High. At this point, the loaded bit file functions as designed.

Tutorials

Tutorials are available from the Xilinx Web site and on the AppLINX CD. (The Web site location is http://support.xilinx.com/support/techsup/tutorials/index.htm). Please contact your local Sales Representative for a copy of the AppLINX CD.

Calculator tutorial designs for Mentor® and Cadence are available on the Xilinx CAE Interface CD-ROM at the following locations.

- Mentor Tutorial on a Workstation

  <CD DRIVE or server>

  `/mentor/tutorial/calc_4ke/calc.bit`

- Cadence Tutorial on a Workstation

  <CD DRIVE or server>

  `/cadence/tutorial/calc_4ke/xilinx.run/calc.bit`

Chapter 4

CPLD Design Demonstration Board

The CPLD Design Demonstration Board (Part Number : HW-CPLD-DEMOBD) is a tool used for demonstrating the In-System Programming (ISP) capabilities of the XC9500 CPLD family. Using this board, you can easily program, erase, verify, and functionally test any XC9500 device.

This chapter contains the following sections:

- “Demonstration Board Overview”
- “Demonstration Board Schematics”
- “Foundation Design Tutorial”

Demonstration Board Overview

The following section details the features and support for the CPLD Demonstration Board.

The demonstration board uses a surface-mounted 555 timer, with resistor and capacitor values set for 14 Hz operation. This oscillator clocks a simple test design (a Johnson counter) implemented in the XC9536; this counter drives LEDs used to verify operation.

Software and Download Cable Support

The CPLD Demonstration Board is shipped with two short "ribbon" style cables for device configuration. The board also supports the Parallel Cable III and the XChecker (serial) cables.

Make sure to connect the cables properly to your host and target system. For information on connecting cables and powering up the demonstration board, refer to the “Cable Hardware” chapter.

This demonstration board is supported by the JTAG Programmer Software. For more information about using this software, refer to the *JTAG Programmer Guide.*

Printed Circuit Board (PCB)

The Printed Circuit Board is shipped with a 44-pin VQFP XC9536 device with two bypass capacitors, 8 LEDs with current limiting resistors, and a header for attaching the download cable.

The PCB will accept a DPDT switch or a permanent jumper at location SW1. The switch is used to connect or disconnect an external DC voltage from the +5V regulator.

Prototyping Area

A prototyping area is included on the PCB. This area has 299 holes (13 columns x 23 rows) for attaching additional circuitry. The holes are 0.038 inch diameter on 0.10 inch centers. Two pairs of these holes are connected to + 5V and GND along the left side of the prototyping area.

Power Supply

The Demonstration Board allows the attachment of an external regulated +5V power supply via the pads at J2. If a +5V regulator is installed at location U2 with a 22uF (or larger) filter capacitor at C4, an external DC voltage of 7V to 12V can be applied at location J3.

You can also install an outer case, battery, 5V regulator, filter capacitor, and on-off switch on the demonstration board. These power supply components can be purchased from Digi-Key, as shown in the following table.

Table 4-1 Digi-Key Parts List

Quantity	Descriptions	References	Digi-Key Part Number
1	DPDT Switch, right angle.	SW1	EG1909

Table 4-1 Digi-Key Parts List

Quantity	Descriptions	References	Digi-Key Part Number
1	5V, 1A, low dropout reg.	U2	LM2940CT-5.0
1	22uf, 16V, Tantalum cap.	C4	P2040

- Digi-Key Corporation is located at 701 Brooks Ave. South, Thief River Falls, MN 56701-0677, Tel: 800-344-4539, Fax: 218-681-3380, (http://www.digikey.com).
- The PCB is designed to fit into a SERPAC plastic case, Model H-65 AC. This case can be purchased from SERPAC, 619 Commercial Ave., Covina, CA 91723, Tel: 818-331-0517, Fax: 818-331-8584 (http://www.serpac.com).

Demonstration Board Schematics

A schematic of this demonstration board is shown in the following figure.

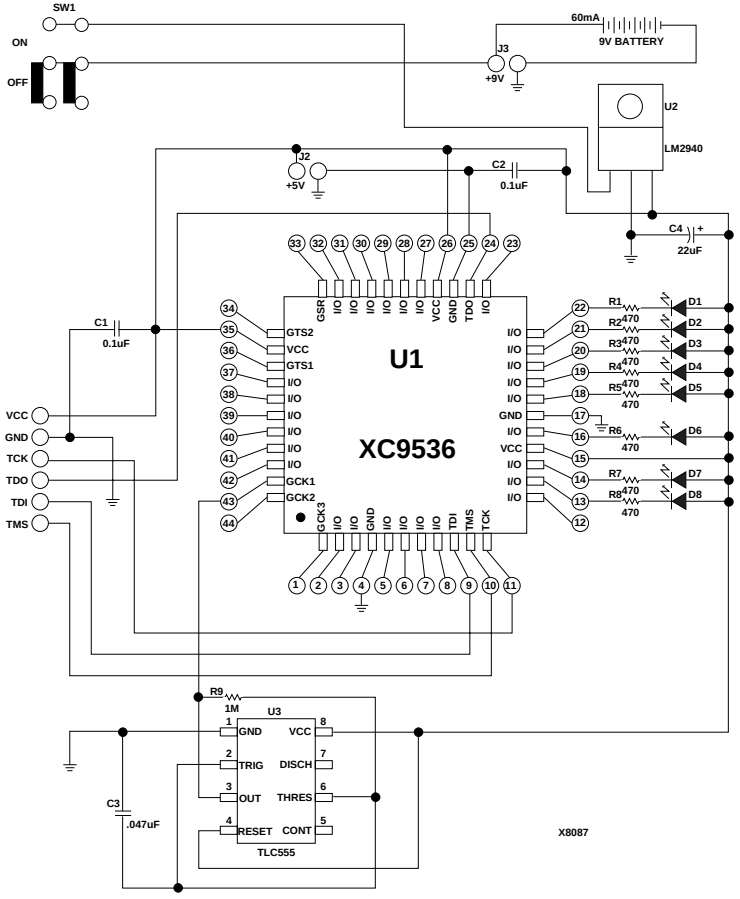


Figure 4-1 XC9536 Device Schematic

The following figure shows the pin layout and components of the ISP Demonstration Board.

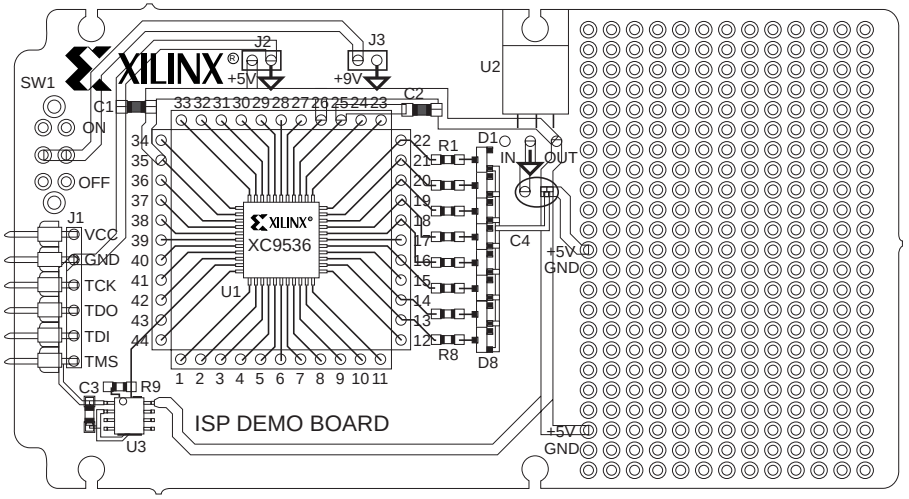


Figure 4-2 CPLD ISP Demonstration Board

All pins of the XC9536 device are connected to through-hole pads on the PCB, numbered 1 to 44. Header Rows of 0.025 inch square posts (on 0.10 inch centers) can be installed at these locations to provide connection points for application circuitry.

Foundation Design Tutorial

The Xilinx Foundation Software Series contains the CPLD Jcounter tutorial, which includes the following five design entry methods.

- **JCT_SCH** (schematic only)
- **JCT_ABL** (ABEL only)
- **JCT_SABL** (schematic with ABEL macro)
- **JCT_VHD** (VHDL only)
- **JCT_SVHD** (schematic with VHDL macro)

Example I: Schematic Design Entry

Example 1 shows the readme.txt file that is located in the project directories of the Jcounter tutorial designs in the Xilinx Foundation

Series™ software. Use these tutorial designs to learn the ISP design flow.

Schematic With VHDL Macro Design

```
JCT_SVHD is a simple 8-bit Johnson counter

DESIGN FLOW: Schematic (JCT_SVH1.SCH) with XVHDL
   macro (JCOUNTER.VHD)

TARGET DEVICE: XC9536-VQ44 (any speed)

I/O Pins:
 CLK   : input free-running clock
 Q0-Q7 : counter outputs

OPERATION:
The counter is triggered on rising edge of the
   clock(CLK).
The following is the sequence of states on outputs
Q Q7-Q0:
 00000000
 00000001
 00000011
 00000111
 00001111
 00011111
 00111111
 01111111
 11111110
 11111110
 11111100
 11111000
 11110000
 11100000
 11000000
 10000000
 00000000  (repeats)

SIMULATION WAVEFORMS:
```

```
JCT_FUNC : functional simulation of design before
implementation.

JCT_TIME : timing simulation results after
implementation.

TUTORIAL:
 This project is used as one of the example designs
 described in the CPLD Design Flow tutorial in the
 Foundation Series On-Line Help System.

DEMO BOARD:
 The JEDEC programming file produced by this
   project
 can be downloaded into the CPLD Demo Board
(HW-CPLD-DEMOBD).
```

Example 2: VHDL Design Entry

Example 2 shows the same design, done in VHDL while using Xilinx Foundation software.

```
library IEEE;

use IEEE.std_logic_1164.all

library metamor;

use metamor.attributes.all;


entity jcounter is
 port  (

   clk:in STD_LOGIC;
 Dout: buffer STD_LOGIC_VECTOR (7 downto 0)


);
```

```
-- Can use attributes to assign pin locations in
   -
-- Foundation VHDL
attribute pinnum of Dout:signal is
"p13,14,16,18,19,20,21,22";

end jcounter;


architecture jcounter_arch of jcounter is

begin

 if CLK' event and CLK='1' then--CLK rising edge

 Dout (7 downto 1) <= Dout (6 downto 0);--shift -
Dout (7 downto 1) <= Dout (6 downto 0);--shift -

 Dout (0) <= not Dout (7);--Last bit inverted --
-- back into first bit

 end if;

end process;


end jcounter_arch;
```

Glossary

Baud Rates

Baud rates refer to your host system communication capabilities.

Configuration Modes

Configuration Modes are the modes available on the Xilinx configuration cables. They include JTAG, SelectMAP and Slave Serial.

CPLD

Complex Programmable Logic Device (CPLD) is an erasable programmable logic device that can be programmed with a schematic or a behavioral design.

Daisy Chain

A daisy chain is a series of bitstream files concatenated in one file. It can be used to program several FPGAs connected in a daisy chain board configuration.

Download

Dowloading is the process of configuring or programming a device by sending bitstream data to the device.

FPGA Flying Lead Connector

FPGA flying lead connectors connect your target FPGA to the FPGA demonstration board.

FPGA Lead Wires

FPGA lead wires connnect to the Parallel Cable III.

GUI Based Program

A graphical program used for accessing the implementation tools.

In System Programming (ISP)

A programmable logic device that can be programmed after it has been connected to the system pc-board.

JTAG Mode

JTAG Mode is a MultiLINX configuration mode supported by the following MultiLINX devices: Virtex, Spartan, XC9500, XC5200, and XC4000.

MultiLINX Cable

The MultiLINX cable is a device for configuring and verifying Xilinx FPGAs and CPLDs.

MultiLINX Flying Wires

The MultiLINX flying wires consist of four sets that are included with the MultiLINX Cable.

Parallel Cable III

Parallel Cable III is a cable assembly which contains a buffer to protect your PCs parallel port and a set of headers to connect to your target system.

Readback

Readback is the process of reading the logic downloaded to an FPGA device.

RS-232 Port

The RS-232 Port is where the MultiLINX cable connects to on the host computer. This is how the MultiLINX cable hardware communicates with the host.

SelectMAP Mode

SelectMAP mode is a MultiLINX configuration mode supported by the MultiLINX device, Virtex.

Slave Serial Mode

Slave Serial Mode is a MultiLINX configuration mode supported by the following MultiLINX devices: Virtex, Spartan, XCS5200, and XC3000.

Universal Serial Buss (USB) Port

The USB Port is where the MultiLINX cable connects to on the host computer.

XChecker Cable

The XChecker hardware consists of a cable assembly with internal logic, a test fixture, and a set of headers to connect the cable to your target system.

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