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Parallel Cable III

The Parallel Cable III is a cable assembly which contains a buffer to protect your PC's parallel port and a set of headers to connect to your target system.

The cable can be used with a single CPLD or FPGA device, or several devices connected in a daisy chain.

The transmission speed of the this cable is determined solely by the speed at which the host PC can transmit data through its parallel port interface.

Using the Parallel Cable III requires a PC equipped with an AT compatible parallel port interface and a DB25 standard printer connector.

Flying Leads

This cable is shipped with two sets of flying leads, one for FPGAs and one for CPLDs. The CPLD leads are labelled "JTAG", and the FPGA leads are labelled "FPGA".

Each flying lead has a 9-pin (6 signals, 3 keys) header connector on one end. This connector fits onto one of the two cable headers. These header connectors are keyed to assure proper orientation to the cable assembly.

On the other end of each flying lead are six individual wires with female connectors. The female connectors fit onto standard 0.025 inch square male pins.

As an example, the following figure shows the Parallel Cable III and its FPGA flying lead wires.

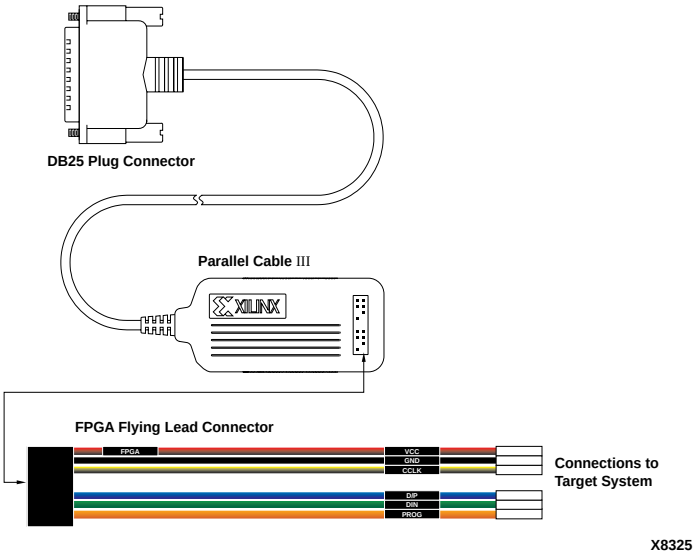


Figure 1-4 Parallel Cable III and FPGA Flying Leads

The following figure shows top and bottom views of the Parallel Cable III, including the FPGA and JTAG (CPLD) headers.

Parallel Cable III

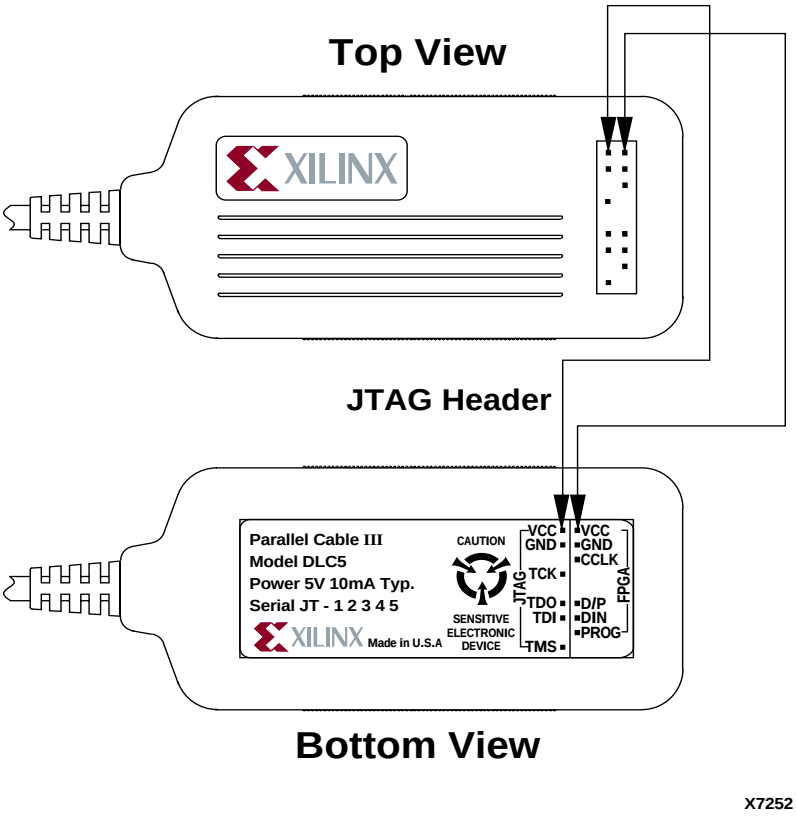


Figure 1-5 Parallel Cable III

Note: The plastic cover of the Parallel Cable III is grey, while the XChecker Cable is beige.

Configuring CPLDs With the Parallel Cable III

When connecting the CPLD flying leads for configuration, make sure to use the “JTAG” header. The following figure shows the connections between the Parallel Cable III CPLD flying leads and a target system.

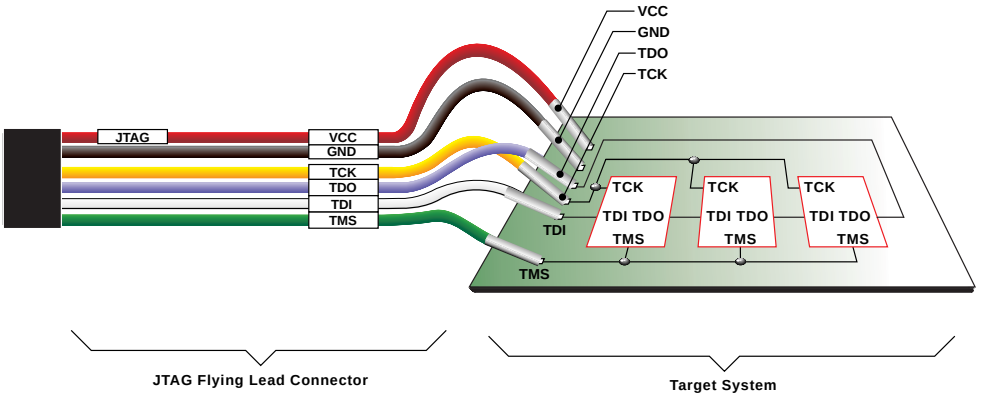


Figure 1-6 Parallel Cable III Connections to CPLD Device

The following table describes the pin functions and connections for configuring CPLDs with the Parallel Cable III.

Table 1-3 Parallel Cable III CPLD Pin Connections

Name	Function	Connections
VCC	Power – Supplies VCC (5 V, 10 mA, typically) to the cable.	To target system VCC
GND	Ground – Supplies ground reference to the cable.	To target system ground
TCK	Test Clock – Drives the test logic for all devices on a JTAG chain.	Connect to system TCK pin.
TDO	Test Data Output – data from the target system is read at this pin.	Connect to system TDO pin.

Table 1-3 Parallel Cable III CPLD Pin Connections

Name	Function	Connections
TDI	Test Data Input – this signal is used to transmit serial test instructions and data.	Connect to system TDI pin.
TMS	Test Mode Select – this signal is decoded by the JTAG state machine to control test operations.	Connect to system TMS pin.

Note: TRST is an optional pin in the JTAG (IEEE 1149.1) specification, and is not used by XC9500 CPLDs. If any of your non-Xilinx parts have a TRST pin, the pin should be connected to VCC.

Configuring FPGAs With the Parallel Cable III

This section details the connections needed to configure FPGAs with the Parallel Cable III.

The following figures show which pins to connect, depending on your chosen FPGA device. For descriptions of each pin, see the "XChecker / Parallel Cable III Connector J2" table and the "XChecker / Parallel Cable III Connector J1" table.

Note: If you are using the Xilinx FPGA Design Demonstration Board, see the "Mode Switch Settings" section of the "FPGA Design Demonstration Board" chapter for specific configuration information.

Connect the flying wires to XC4000 FPGAs as shown in the following figure.

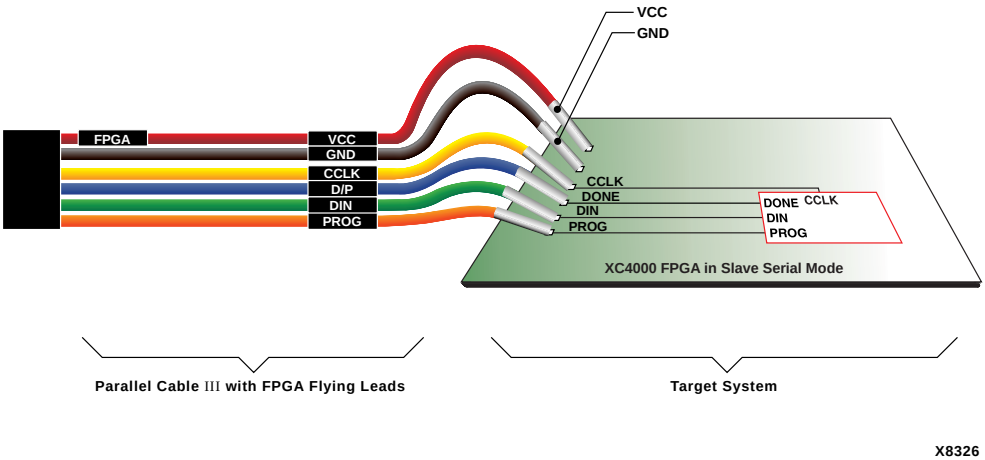


Figure 1-7 Parallel Cable III Connections to XC4000 Device

To configure XC3000 FPGAs, the PROG wire is not used as shown in the following figure. In both cases the FPGA must be in the Serial Slave Mode.

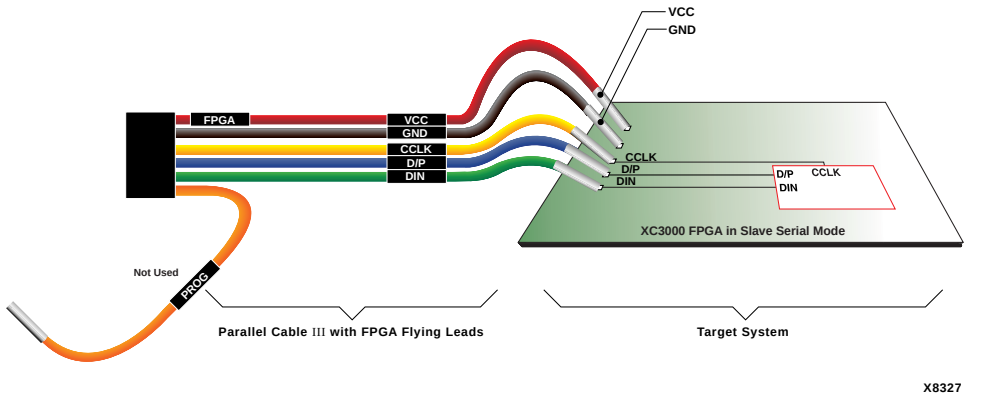


Figure 1-8 Parallel Cable III Connections to XC3000 Device

Note: If you are using the Xilinx FPGA Demonstration Board, see the "Mode Switch Settings" section of the "FPGA Design Demonstration Board" chapter for specific configuration information.

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