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SmartLynq Data Cable

User Guide

UG1258 (v1.2) March 6, 2019

XILINX

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/06/2019	1.2	Added a Caution regarding temperature to Physical Description. Updated pin assignments in Figure 1-10. Added SmartLynq Cable Operating Characteristics including DC electrical and switching characteristics and Figure 1-11. Added a note about backward compatibility to Firmware Updates. Added how to reset IP settings in Static IP Address for USB or Ethernet Connection on Linux.
09/14/2017	1.1	Replaced PMOD with GPIO in text and graphics. Updated Figure 1-13. Changed GPIO interface to 3.3V only.
09/07/2017	1.0	Initial Xilinx release.

Table of Contents

Revision History 2

Chapter 1: SmartLynq Data Cable

Features 4
Description 4
Setup 6

Appendix A: Regulatory and Compliance Information

Declaration of Conformity 23

Appendix B: Additional Resources and Legal Notices

Xilinx Resources 24
Solution Centers 24
Documentation Navigator and Design Hubs 24
References 25
Please Read: Important Legal Notices 25

SmartLynq Data Cable

Features

The SmartLynq Data Cable is a complete, all-in-one solution for programming and debugging Xilinx devices. The cable includes these features:

- Supports JTAG rates up to 40 Mb/s with a voltage range of 1.2V to 3.3V.
- Offers Ethernet and USB host-side connections.
- Leverages industry standards, including JTAG boundary-scan *IEEE Standard 1149.1 - Test Access Port and Boundary-Scan Architecture* [Ref 1].
- Supports all UltraScale™, UltraScale+™, and 7 series families as well as Zynq®-7000 SoCs and Zynq UltraScale+ MPSoCs.
- Indirectly programs selected serial peripheral interface (SPI) flash memory or parallel flash memory devices via the device's JTAG port.
- Offers a 3.3V 8-bit general purpose I/O (GPIO) port.
- Optimized for use with Xilinx® Vivado® design tools.

Note: Xilinx Vivado design tools are required for programming and configuration. See the design tool release notes for supported devices. The cable is not supported by Xilinx ISE® tools.

Description

Figure 1-1 shows the contents of the SmartLynq Data Cable kit.

The SmartLynq Data Cable provides a high-speed connection through Ethernet or USB to a JTAG chain for configuring and debugging Xilinx devices. The cable supports debugging and indirect flash programming of third-party parallel and serial NOR devices through a JTAG port when used with Vivado Hardware Manager, and for debugging embedded software when used with the Xilinx SDK development environment.

The SmartLynq Data Cable supports JTAG data transfer bursts at JTAG clock (TCK) frequencies, selectable from 125 kHz to 40 MHz, and provides a separate 8-bit GPIO port for 8-bit read and write operations to external logic.



Figure 1-1: **Xilinx SmartLynq Data Cable**

Physical Description

The SmartLynq Data Cable circuitry is housed in a recyclable, fire-retardant plastic case with a display (Figure 1-2). An internal EMI shield attenuates internally generated emissions and protects against susceptibility to radiated emissions.

CAUTION! *The SmartLynq Data Cable is designed to operate in the temperature range of 10°C to 26°C (50°F to 80°F). The storage temperature range is 0°C to 55°C (32°F to 131°F). Operating outside of this range might cause malfunction or permanent damage to the device.*



Figure 1-2: **SmartLynq Module**

Setup

This section describes how to set up the SmartLynq Data Cable and how to connect to the cable using Vivado design tools.

Minimum Host System Requirements

You can access the SmartLynq Data Cable through a USB port on a host computer or through an Ethernet connection that is accessible from your network. To connect using USB, the host computer must contain a USB host controller with one or more USB ports. The controller can reside on the PC motherboard or can be added using an expansion or PCMCIA card. The SmartLynq Data Cable is a bus-powered device drawing less than 150 mA from the host USB port under all operating conditions.

The SmartLynq Data Cable is designed to take full advantage of the bandwidth of USB 3.0 ports and is backward-compatible with USB 2.0 and USB 1.1.

SmartLynq Data Cable Connectors

The JTAG and GPIO 2x6 cable connectors are on the right side of the SmartLynq Data Cable module (see Figure 1-3).

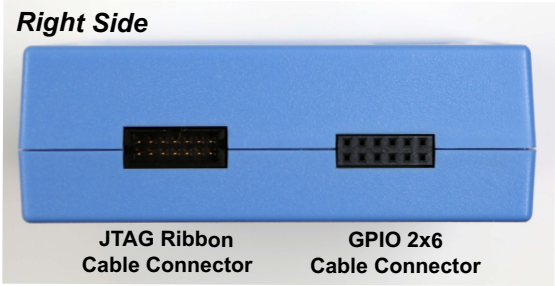


Figure 1-3: **JTAG Ribbon Cable and GPIO 2x6 Cable Jacks**

The DC power, USB Type-B, and Ethernet jacks are on the left side of the SmartLynq Data Cable module (see Figure 1-4).

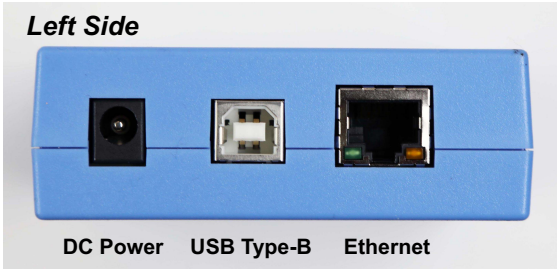


Figure 1-4: **DC Power, USB Type-B, and Ethernet Jacks**

When connecting to the SmartLynq Data Cable through Ethernet, the default for the SmartLynq Data Cable is to receive its IP address from a DHCP server. To manually set up a static IP address on SmartLynq Data Cable, see Assigning a Static IP Address.

Setup—Connect through Ethernet

1. Connect the power and Ethernet cables to the SmartLynq Data Cable module.
   a. Plug the power adapter barrel plug into the power jack on the side of the module.
   b. Plug the Ethernet cable into the Ethernet jack on the SmartLynq module and a user network tap.
   c. Plug the power adapter into a 120-VAC outlet.

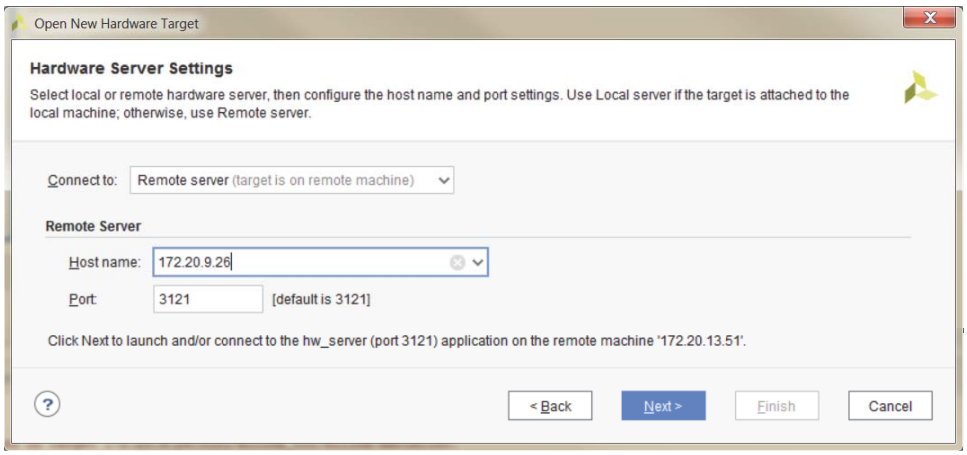
The SmartLynq Data Cable powers up and the display shows self-checks. The SmartLynq Data Cable then acquires and displays an IP address, as shown in Figure 1-5.



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Figure 1-5: **IP Address on the Display**

2. Connect the SmartLynq Data Cable to the target board.
   a. Connect the SmartLynq Data Cable to the JTAG interface on the target board.
   b. To connect to the board through SmartLynq Data Cable, open the **Hardware Manager** in the Vivado tool.
   c. In the **Connect To** field, pull-down **Remote Server**.
   d. In the **Host Name** field, specify the IP address shown on the SmartLynq Data Cable display. See Figure 1-6. Click **Next**.



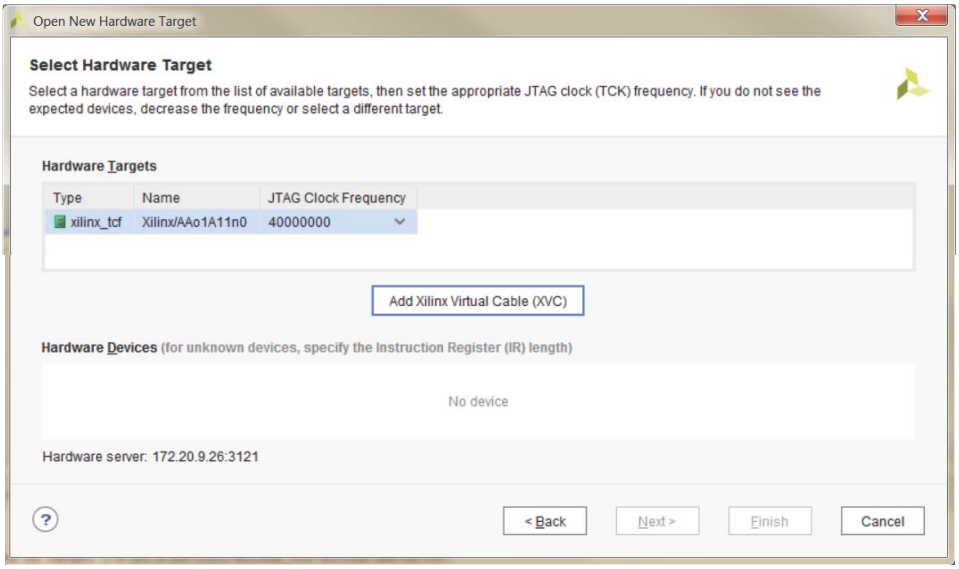
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Figure 1-6: **Hardware Server Settings**

On the SmartLynq Data Cable display, VREF ON appears if the target board is powered up, and VREF OFF appears if the target board does not have power.

Note: The target board must be powered on to connect with the Vivado Hardware Manager. With the board powered on, you can connect using the Open New Hardware Target wizard.

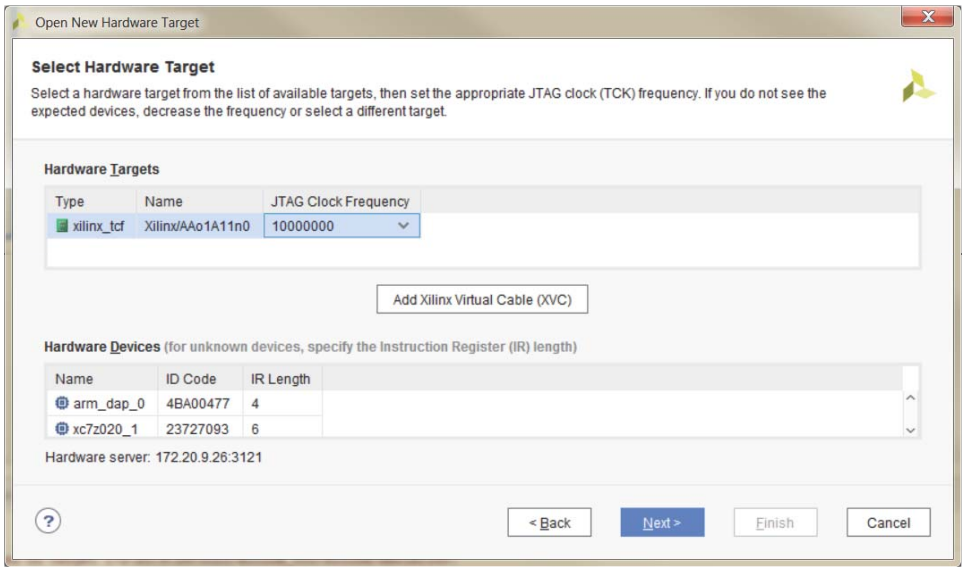
The SmartLynq Data Cable defaults to a TCK frequency of 40 MHz. See Figure 1-7.



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Figure 1-7: **Default TCK Frequency of 40 MHz**

If no devices on the target board are listed under **Hardware Devices**, this might indicate the clock speed is too high. Lower the JTAG clock frequency (to 10 MHz for example) to detect devices. See Figure 1-7.



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Figure 1-8: **Example of Frequency Lowered to 10 MHz**

Setup—Connect through USB (Windows Systems)

1. Connect the USB cable to the SmartLynq Data Cable module.
   a. Plug a USB cable with a type-B connector into the SmartLynq module USB port and the other end into the Windows system.

      Note: The USB port supplies power to SmartLynq Data Cable module so the power adapter is not required.

   b. When the SmartLynq Data Cable is connected to the Windows system the first time, Windows automatically installs the device driver. When complete, a message appears:

      ```
      Smart JTAG Cable installed
      ```

   c. After the driver is installed, unplug and plug back in the SmartLynq model to reinitialize.
   d. After initializing, an IP address appears on the display.
2. Connect the SmartLynq Data Cable to the target board using the Hardware Manager.
   a. Start Vivado tools on the same Windows machine.
   b. Open the **Hardware Manager** and connect to the target.
   c. In the **Connect to** field, pull-down **Remote server** and specify the IP address shown on the SmartLynq Data Cable display.

      Note: From a Vivado Hardware Manager session, you cannot remotely interface with a SmartLynq Data Cable connected to a Windows System via USB.

Setup—Connect through USB (Linux Systems)

1. Connect the USB cable to SmartLynq Data Cable module.
   a. Plug a USB cable with a Type-B connector into the SmartLynq Data Cable USB port and the other end into the Linux host system.

      Note: The USB port supplies power to the SmartLynq Data Cable module so the power adapter is not required.

   b. The SmartLynq Data Cable module powers up. Self-check information appears on its display.
   c. An IP address appears on the display.

2. **Optional**: Connect the SmartLynq Data Cable to the target board.

   This optional step shows how to set up the network interface for the SmartLynq Data Cable, if required. (This section is optional because you do not need to connect a target immediately after plugging in the cable.)

   a. Connect the SmartLynq Data Cable module to the JTAG interface on the target board.

   b. Open the **Hardware Manager** in the Vivado tool.

   c. In the **Connect to** field, pull-down **Remote Server**.

   d. In the **Host Name** field, specify the IP address shown on the SmartLynq Data Cable display. Click **Next**.

      Note: The remaining sub-steps are optional. For most users, the remaining steps are not used.

   e. To connect to the SmartLynq Data Cable from a Vivado tools session running on a different machine, run the **`setting64.csh`** file from the Xilinx Vivado installation directory.

   f. Run the command from a shell:

      ```
      tcflog TCP:<IP address>:3121
      ```

      For example, if the SmartLynq Data Cable display shows **`10.0.0.2`**, run **`tcflog TCP:10.0.0.2:3121`**.

   g. Open the Vivado **Hardware Manager** on the other machine.

   h. In the **Connect to** field, pull-down **Remote server.**

   i. In the **Host Name** field, enter the name of the remote machine that the SmartLynq Data Cable is plugged into.

   j. In the Port field, enter **1534**.

   k. Click **Next** to connect to the remote SmartLynq Data Cable setup.

   If **Hardware Manager** cannot connect to SmartLynq Data Cable, run the **`ifconfig`** command to set up the network interface (see step 3) and then run step 2 again.

3. Setup the network interface for the SmartLynq Data Cable (if required).

   a. Run the ifconfig command to configure the network interface depending on the IP address Linux assigned to the SmartLynq Data Cable.

For example: Linux assigns the IP address 10.0.0.2 to the SmartLynq Data Cable. Run **ifconfig** to view the currently active network interfaces on this system. For example:

```
eth0      Link encap:Ethernet HWaddr D7:45:89:22:88:97
          inet addr:172.19.3.148 Bcast:172.19.3.255 Mask:255.255.252.0
          UP BROADCAST RUNNING MULTICAST MTU:1500 Metric:1
          RX packets:2278375690 errors:0 dropped:307 overruns:0 frame:0
          TX packets:2305014867 errors:0 dropped:22 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:1026403610964 (955.9 GiB) TX bytes:1048839754879 (976.8 GiB)
          Interrupt:17

lo        Link encap:Local Loopback
          inet addr:127.0.0.1 Mask:255.0.0.0
          UP LOOPBACK RUNNING MTU:16436 Metric:1
          RX packets:41586323 errors:0 dropped:0 overruns:0 frame:0
          TX packets:41586323 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:107897957583 (100.4 GiB) TX bytes:107897957583 (100.4 GiB)
```

If none of the interface names have an Internet address that is part of the protocol address family that covers the assigned SmartLynq Data Cable address, then use **ifconfig** to configure a new interface.

In the preceding example, the Linux system has two interfaces defined: **eth0** and **lo**. Neither interface has an Internet address format 10.0.x.x that includes the address 10.0.0.2 assigned to SmartLynq Data Cable. Set up the interface by running **ifconfig** with the following arguments:

```
sudo ifconfig eth1 10.0.0.1 netmask 255.255.0.0
```

Running **ifconfig** again shows the new interface:

```
eth0      Link encap:Ethernet HWaddr D7:45:89:22:88:97
          inet addr:172.19.3.148 Bcast:172.19.3.255 Mask:255.255.252.0
          UP BROADCAST RUNNING MULTICAST MTU:1500 Metric:1
          RX packets:2278375690 errors:0 dropped:307 overruns:0 frame:0
          TX packets:2305014867 errors:0 dropped:22 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:1026403610964 (955.9 GiB) TX bytes:1048839754879 (976.8 GiB)
          Interrupt:17

eth1      Link encap:Ethernet HWaddr 00:5D:03:00:00:01
          inet addr:10.0.0.1 Bcast:10.0.255.255 Mask:255.255.0.0
          UP BROADCAST RUNNING MULTICAST MTU:1500 Metric:1
          RX packets:10 errors:0 dropped:0 overruns:0 frame:0
          TX packets:2 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:2396 (2.3 KiB) TX bytes:345 (345.0 b)

lo        Link encap:Local Loopback
          inet addr:127.0.0.1 Mask:255.0.0.0
          UP LOOPBACK RUNNING MTU:16436 Metric:1
          RX packets:41586323 errors:0 dropped:0 overruns:0 frame:0
          TX packets:41586323 errors:0 dropped:0 overruns:0 carrier:0
```

```
collisions:0 txqueuelen:0
RX bytes:107897957583 (100.4 GiB) TX bytes:107897957583 (100.4 GiB)
```

Firmware Updates

The SmartLynq Data Cable cable contains a controller that might need firmware upgrades periodically distributed by Xilinx with the Vivado software releases. After connecting to the SmartLynq Data Cable, the Vivado Hardware Manager displays the following notification if it detects that the SmartLynq Data Cable firmware version in the current version of Vivado is newer than the version in the SmartLynq Data Cable cable:

```
INFO: [Labtools 27-2285] Connecting to hw_server url
TCP:xxx.xxx.xxx.xxx:3121

INFO: [Labtools 27-3350] There is an update available for the
SmartLynq Data Cable cable. Call 'update_hw_firmware -reset' TCL
command to update.
```

Run the command **`update_hw_firmware -reset`** in the Vivado Hardware Manager Tcl console to update the SmartLynq Data Cable firmware. The Hardware Manager automatically disconnects from the cable after updating the firmware.



CAUTION! *This operation can take up to 40 seconds. Do not stop the process or disconnect power to the cable before the operation completes!*

Power-cycle the SmartLynq Data Cable by disconnecting and reconnecting the power supply and the USB cable to boot the controller with the new firmware.

Note: The SmartLynq Data Cable is backward-compatible with older releases of Vivado tools, regardless of the firmware version used to program the cable. There is no need to downgrade the firmware version if you want to use an older release of Vivado tools.

SmartLynq Data Cable Status Display

The 4-line SmartLynq Data Cable display (Figure 1-5) provides the following information:

1. Connection status
   a. Displays NO CONNECTION if the SmartLynq Data Cable is not connected to Ethernet or USB.
   b. Displays IP address on the first two lines if connected to Ethernet or USB.
   ◦ The character at the end of line 3 indicates the type of connection:
      - E for Ethernet
      - U for USB

2. VREF status
    a. Displays VREF OFF or VREF ON to indicate VREF status on the target board.
3. Number of clients connected to the SmartLynq Data Cable
    a. The number at the end of the third line indicates number of clients connected to the SmartLynq Data Cable.

Target Interface Connectors

The SmartLynq Data Cable has two target interface connectors:

- JTAG 7x2 connector for the 4-bit IEEE JTAG interface
- GPIO 2x6 connector for the 8-bit GPIO interface

SmartLynq Data Cable JTAG Connector

Xilinx recommends using the provided 6-inch ribbon cable to connect the SmartLynq Data Cable JTAG connector to the JTAG port on the target board.

To take advantage of the ribbon cable, a mating connector must be incorporated into the target board, as is implemented on Xilinx evaluation boards. This connector is normally installed only during prototype checkout. When the production hardware is functional and the JTAG devices can be configured from alternate sources, the connector can be eliminated to reduce cost. Maintaining the footprint for this connector is recommended if space permits.

The connector has a 2-mm shrouded, keyed header. See Table 1-2 for vendor part numbers and pin assignments.

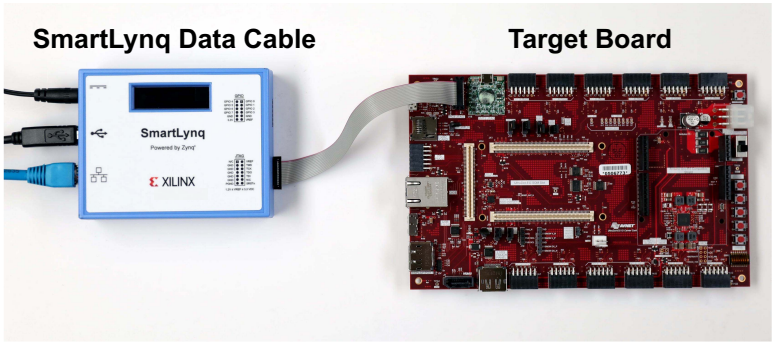


Figure 1-9: **SmartLynq Data Cable JTAG Connection to the JTAG Interface on a Target Board**

Mating connectors for attaching the high-performance ribbon cable to the JTAG port on a target board are available in both through-hole and surface-mount configurations

(Figure 1-10). Shrouded and keyed versions should always be used to guarantee proper orientation when inserting the cable. The connector requires 105 mm^2 of board space.

The target board voltage applied to pin 2 of the JTAG connector is used as a power source for the output buffers that drive the output pins (see Table 1-1).

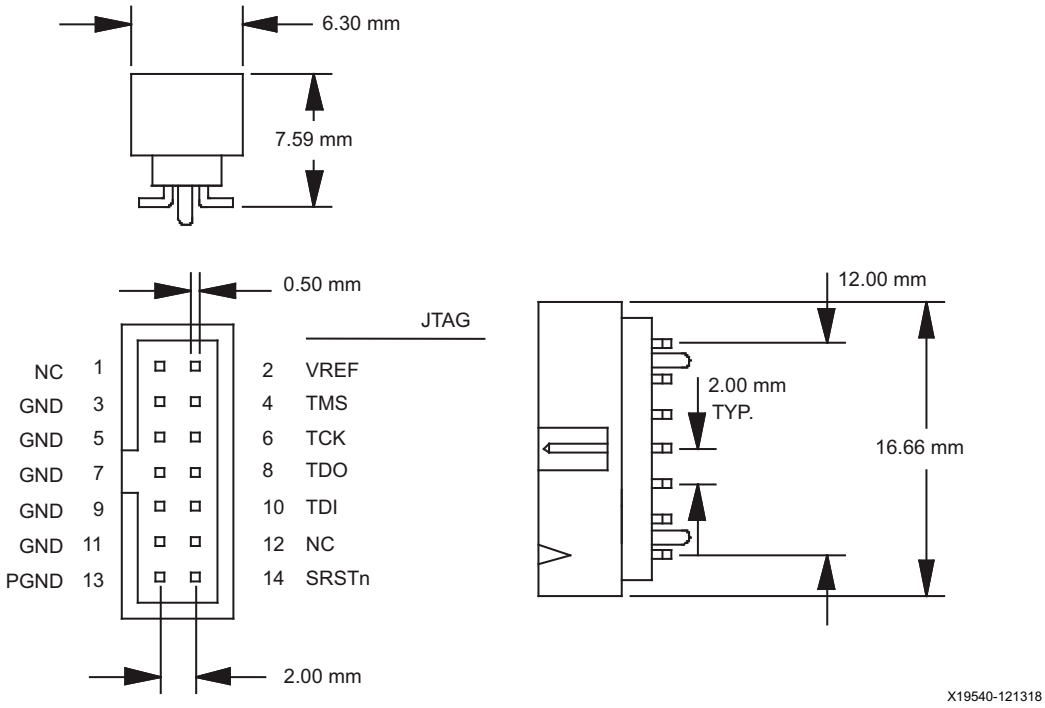


Figure 1-10: **Target Interface Connector Dimensions and Signal Assignments**

Table 1-1: **Target Board Interface Pin Descriptions**

Pin Number	Pin Name	Direction	Description
2	V_{REF}	In	**Target Reference Voltage**. This pin should be connected to a voltage bus on the target board that serves the JTAG interface.
4	TMS	Out	**JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions on all target JTAG devices.
6	TCK	Out	**JTAG Test Clock.** This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target JTAG devices sharing the same data stream.
8	TDO	In	**JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.
10	TDI	Out	**JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

Table 1-1: **Target Board Interface Pin Descriptions *(Cont'd)***

Pin Number	Pin Name	Direction	Description
13	PGND	Out	**JTAG Pseudo Ground**. Use of this pin is optional. PGND is LOW during JTAG operation.
14	SRST	Out	Use of this pin is optional. Host applications can customize the behavior of this signal.

Table 1-2 provides a third-party source for mating connectors that are compatible with the SmartLynq Data Cable JTAG interface.

Table 1-2: **Mating Connectors for 2 mm pitch, 14-Conductor Ribbon Cable**

Manufacturer(1)	SMT, Vertical	Through-Hole, Vertical	Through-Hole, Right Angle	Website
Molex	87832-1420	87831-1420	87833-1420	www.molex.com

Notes:

1. Some manufacturer pin assignments do not conform to Xilinx pin assignments. Refer to the manufacturer's data sheet for more information

SmartLynq Cable Operating Characteristics

Table 1-3: **DC Electrical Characteristics of the SmartLynq Cable JTAG Signals**

Symbol	Description	Conditions	Min	Max	Units
V_{OH}	High-level output voltage	V_{REF} = 1.65V, I_{OH} = –8 mA	1.2	—	V
		V_{REF} = 2.3V, I_{OH} = –9 mA	1.7	—	
		V_{REF} = 3V, I_{OH} = –12 mA	2.3	—	
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	—	0.4	V
		I_{OL} = 9 mA	—	0.5	
		I_{OL} = 12 mA	—	0.7	
V_{IH}	High-level input voltage	V_{REF} = 1.2V to 1.35V	0.78	—	V
		V_{REF} = 1.35V to 1.65V	0.88		
		V_{REF} = 1.65V to 1.95V	1.1		
		V_{REF} = 1.95V to 2.7V	1.6		
		V_{REF} = 2.7V to 3.3V	2		
V_{IL}	Low-level input voltage	V_{REF} = 1.2V to 1.95V	—	0.4	V
		V_{REF} = 1.95V to 2.7V	—	0.7	
		V_{REF} = 2.7V to 3.3V	—	0.8	
I_{CC}	Dynamic current	—	—	110	mA

Table 1-4: **Switching Characteristics of the SmartLynq Cable**

Symbol	Description	Conditions	Min	Max	Units
T_{CLK}	Clock period with 50% duty cycle	125 kHz to 40 MHz	25	8000	ns
TCPD	Cable Propagation Delay Time (TDI or TMS relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	—	1	ns
TCSU	Cable Setup Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	12	—	ns
TCHU	Cable Hold Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	0.50	—	ns

Figure 1-11 illustrates SmartLynq Data Cable timing.

The sample point is automatically selected based on an algorithm run by the SmartLynq module.

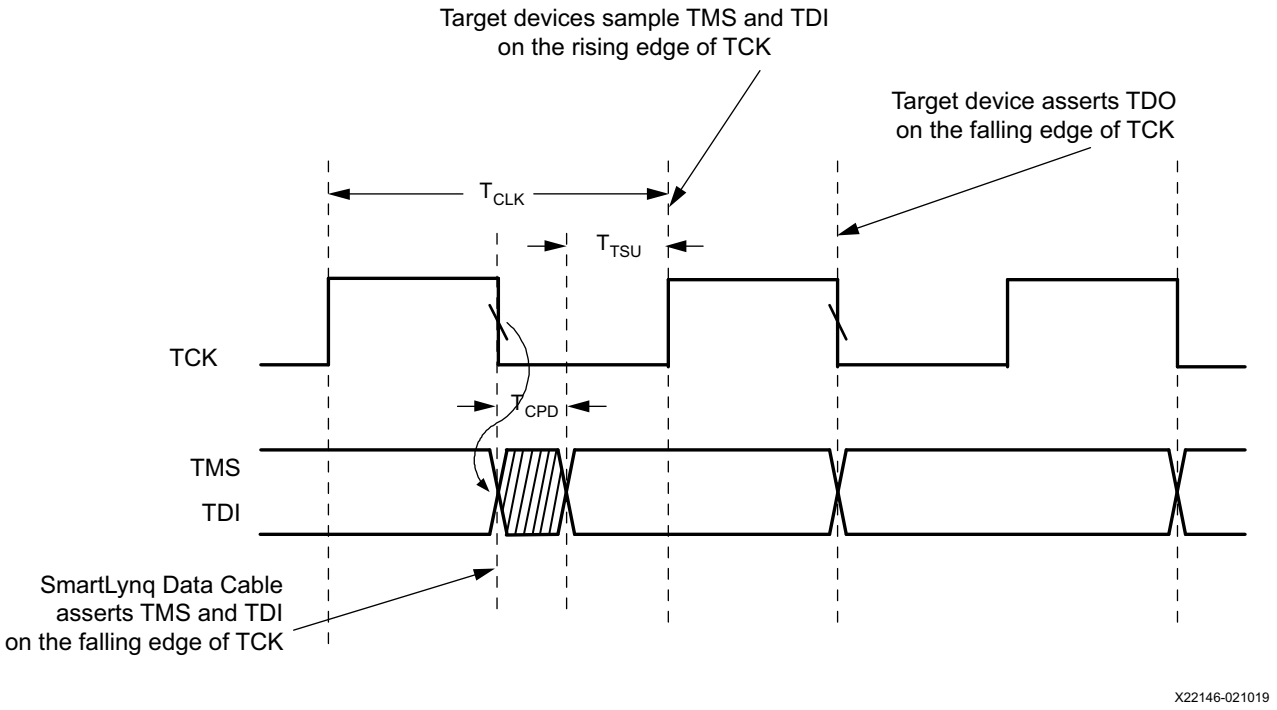


Figure 1-11: **SmartLynq Data Cable Timing Diagram**

Additional notes pertaining to Figure 1-11:

- The SmartLynq Data Cable samples TDO at either 0, 90, 180, or 270 degrees of TCK, with 0 degrees being the rising edge of TCK and 180 being the falling edge.

- Propagation delays associated with buffers on the target system must be taken into account to satisfy the minimum setup times.

GPIO 8-Bit 3.3V Interface

The SmartLynq Data Cable GPIO can be used for a variety of basic input/output operations on the target board. Figure 1-12 shows a sample setup where the SmartLynq Data Cable is connected to an oscilloscope, power supply, and a target board. In this setup, the SmartLynq Data Cable uses an output from the GPIO pins to drive a trigger input to the oscilloscope. The oscilloscope drives an input to the SmartLynq cable to allow monitoring a trigger event from the oscilloscope. With this oscilloscope arrangement, it is possible to take analog measurements with the oscilloscope and synchronize trigger events with the SmartLynq Data Cable. Figure 1-12 also shows how a power supply or relay could be controlled through the GPIO port so as to power on or off the target board. Thus, through the GPIO ports, it is possible to simplify the driving and sensing of additional instruments connected to the target system.

The latency of such a trigger is unpredictable because these are software-driven triggers.

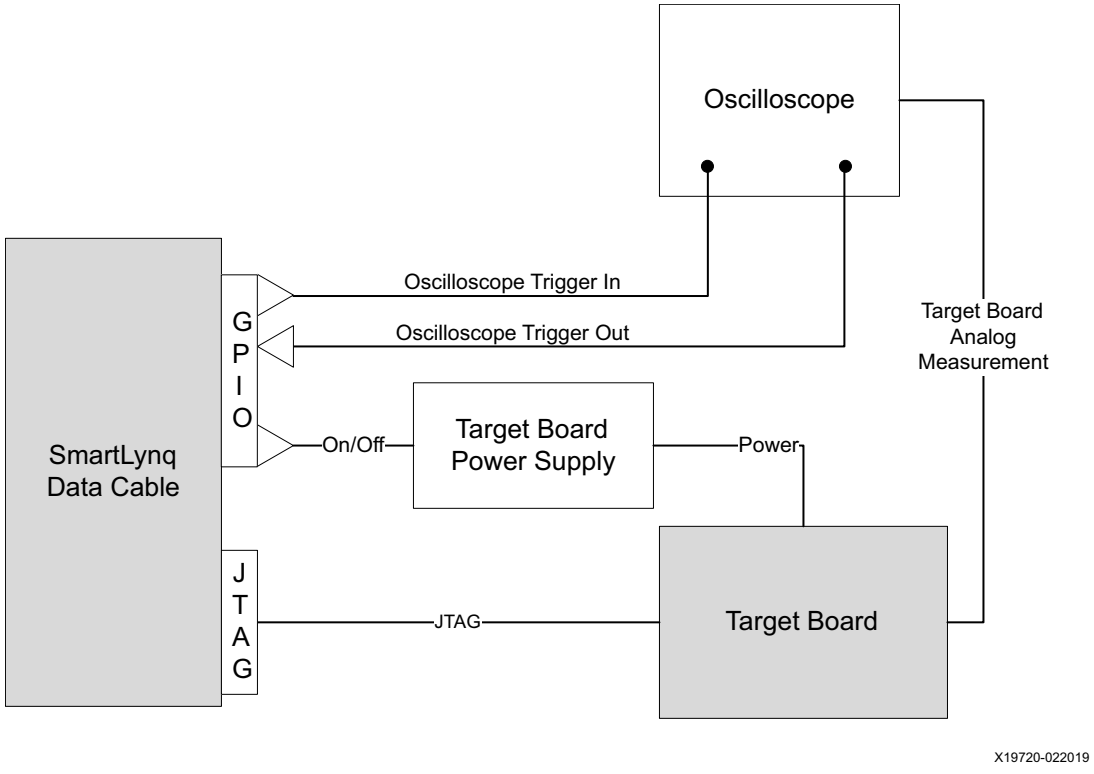


Figure 1-12: **Sample Setup—Cable H to an Oscilloscope**

The GPIO 2x6 connector is available for 8-bit static read/write operations (see Figure 1-13). The 8-bit GPIO interface does not turn on until the GPIO_VREF pin 11 on the GPIO 2x6 interface is powered by 3.3V.

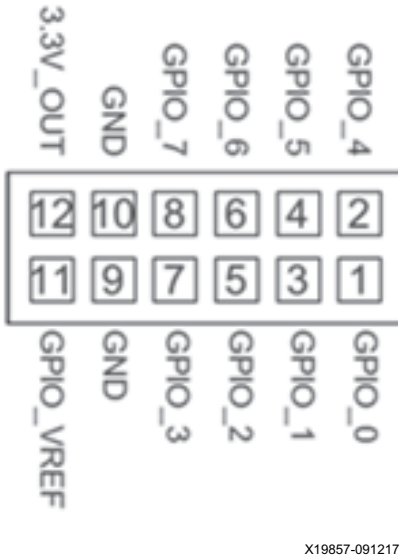


Figure 1-13: **GPIO 2x6 Pin Assignments**

You can attach flying leads to any of the standard 0.1-inch headers (2x6 pins) in Table 1-5 to connect to the GPIO interface.

Table 1-5: **Header Manufacturer and Part**

Manufacturer	Part Number
Samtec	TSW-106-23-S-D
Amphenol FCI	67997-212HLF
3M	929836-01-06-RK
Hirose	A1-12PA-2.54DSA(71)
Sullins	PBC06DAAN

The 8-bit general purpose read/write interface is controlled by the **update_hw_gpio** Tcl command. The GPIO interface defaults to read mode on power on reset.

To define a bit as input or output, specify a byte after the **update_hw_gpio** command:

```
update_hw_gpio <direction byte>
```

where:

- 1 in the direction byte specifies the pin in that bit position as an output pin.
- 0 defines the pin as an input pin.

For example:

```
update_hw_gpio A3
```

where:

0xA3 = binary **1010_0011** defines the following bits and pins as:

- outputs: 0, 1, 5, 7
- inputs: 2, 3, 4, 6

The command **update_hw_gpio** initializes the bits defined as outputs to 0.

To drive a value onto the output pins, specify a second byte argument to **update_hw_gpio** with the corresponding bit positions set to 0 or 1.

For example:

```
update_hw_gpio 3F e7
```

where:

0x3F = binary **0011_1111**, which defines the following bits and pins as:

- 0 to 5 as outputs
- 6 and 7 as inputs

0xE7 = **1110_0111**, which drives the following values on output bits 0 to 5:

- bit 0 = 1
- bit 1 = 1
- bit 2 = 1
- bit 3 = 0
- bit 4 = 0
- bit 5 = 1

Note: Bits 6 and 7 are defined as inputs.

Running **update_hw_gpio** with no arguments returns the values detected on the bits and pins defined as inputs, and returns the values driven on the output pins.

Assigning a Static IP Address

Static IP Address for USB or Ethernet Connection on Linux

You can assign a static IP address to the SmartLynq Data Cable to enable scripted Vivado and XSDK tool operations to always detect the cable at the same IP address. The steps provided assume you have already attached your SmartLynq Data Cable to a Windows or Linux host system through either USB or Ethernet.

Create a configuration file called `config.ini` with the information in Table 1-6.

Table 1-6: **Content of the Config.ini File**

	USB	Ethernet (2)

Content	`set always-open-jtag 1`
	`set usb-address <static IP address>` (1)
	`set usb-netmask 255.255.255.0`
	`set usb-gateway 10.0.0.1`
		`set always-open-jtag 1`
		`set ip-address <static IP address>`
		`set ip-netmask 255.255.255.0`
		`set ip-gateway 10.0.0.1`

Notes:

1. The usb-address line is the static IP address to use when connected through USB (e.g., 10.0.0.25).
2. Obtain valid ip-address, ip-netmask, and ip-gateway information from your network administrator.

Configure the SmartLynq Data Cable with the `config.ini` file information by running the command from the Hardware Manager Tcl console:

```
update_hw_firmware -skip_update -config_path config.ini -reset
```

The `-reset` option disconnects the Hardware Manager from the SmartLynq Data Cable.

Unplug the SmartLynq Data Cable and then reconnect it to apply the IP address change.

To reset the old IP settings:

```
update_hw_firmware -format -reset
```

Reconnect Hardware Manager to the SmartLynq Data Cable:

If the Vivado Hardware Manager is running on the same machine as the SmartLynq Data Cable USB connection:

1. In the **Connect to** field, pull-down **Remote Server**.
2. For **Host Name**, specify the new IP address.
3. For **Port**, specify the default port value of **3121**.
4. Click **Next** to connect to the SmartLynq Data Cable.

If the Vivado Hardware Manager is running on a different machine than the remote machine with the SmartLynq Data Cable USB setup:

1. On the machine with the SmartLynq Data Cable USB setup, run `tcflog TCP:<new IP address>:3121`
2. In the **Connect to** field, pull-down **Remote Server**.
3. For the **Host Name**, specify the name or URL of the remote machine.
4. For **Port**, specify the value **1534**.
5. Click **Next** to connect to the SmartLynq Data Cable.

Static IP Address for Ethernet Connection on Linux

The steps to set up a static IP address for Ethernet are similar to the steps to set up a Static IP Address for USB Connection on Linux, except the **config.ini** file keywords are different:

```
set always-open-jtag 1
set ip-address <static IP address>
set ip-netmask 255.255.255.0
set ip-gateway xxx.xxx.xxx.xxx
```

Obtain valid ip-address, ip-netmask, and ip-gateway information from your network administrator.

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Appendix A

Regulatory and Compliance Information

Declaration of Conformity

The SmartLynq Data Cable Declaration of Conformity is online.

Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up-to-date information for this cable is available on these websites:

SmartLynq Data Cable

SmartLynq Data Cable Master Answer Record 69590

This document provides supplemental material:

1. *IEEE Standard 1149.1 - Test Access Port and Boundary-Scan Architecture*
   standards.ieee.org/standard/1149_1-2013.html

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