

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

ML405 Evaluation Platform

User Guide

UG210 (v1.5.1) March 10, 2008

XILINX®

Xilinx is disclosing this user guide, manual, release note, and/or specification (the "Documentation") to you solely for use in the development of designs to operate with Xilinx hardware devices. You may not reproduce, distribute, republish, download, display, post, or transmit the Documentation in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Xilinx expressly disclaims any liability arising out of your use of the Documentation. Xilinx reserves the right, at its sole discretion, to change the Documentation without notice at any time. Xilinx assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information.

THE DOCUMENTATION IS DISCLOSED TO YOU “AS-IS” WITH NO WARRANTY OF ANY KIND. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

© 2006–2008 Xilinx, Inc. All rights reserved.

XILINX, the Xilinx logo, the Brand Window, and other designated brands included herein are trademarks of Xilinx, Inc. PowerPC is a trademark of IBM Corp. and is used under license. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/23/06	1.0	Initial Xilinx release.
06/30/06	1.0.1	Release to Web.
01/31/07	1.1	Updated jumper information for 2.5V and 3.3V operation (Table 1-1, page 12).
03/21/07	1.2	Updated Table 1-19, page 31 (see table notes).
05/02/07	1.3	Added Appendix A, “Board Revisions” and information for RoHS-compliant boards.
06/28/07	1.4	Updated Table 1-19, page 31 for XAUI/SRIO support.
08/13/07	1.5	Corrected J5 pinout for HDR2_8 in Table 1-8, page 17 (U19).
03/10/08	1.5.1	Minor edits to Table A-1, page 35.

Table of Contents

Preface: About This Guide

Additional Resources 5
Conventions 5
Typographical 5
Online Document 6
Introduction 7
Features 7
Package Contents 8
Additional Information 8
Block Diagram 9
Detailed Description 10
1. Virtex-4 FPGA 12
2. DDR SDRAM 13
3. Differential Clock Input and Output with SMA Connectors 14
4. Oscillator Sockets 14
5. LCD Brightness and Contrast Adjustment 14
6. DIP Switches (Not Installed) 14
7. User and Error LEDs (Active-High) 15
8. User Pushbutton Switches (Active-High) 16
9. CPU Reset Pushbutton Switch (Active-Low) 16
10. Expansion Headers 17
11. Stereo AC97 Audio Codec 21
12. RS-232 Serial Port 21
13. 16-Character x 2-Line LCD 21
14. IIC Bus with 4 Kb EEPROM 22
15. VGA Output 22
16. PS/2 Mouse and Keyboard Ports 22
17. System ACE Controller 23
18. ZBT Synchronous SRAM 23
19. Linear Flash 24
20. Xilinx XC95144XL CPLD 24
21. 10/100/1000 Tri-Speed Ethernet PHY 25
22. USB Controller with Host and Peripheral Ports 26
23. Xilinx XCF32P Platform Flash Configuration Storage Device 26
24. JTAG Configuration Port 26
25. Onboard Power Supplies 27
26. AC Adapter and Input Power Switch/Jack 27
27. Power Indicator LED 27
28. INIT LED 28
29. DONE LED 28
30. Program Switch 28
31. Configuration Address and Mode DIP Switches 28
32. Encryption Key Battery 28
33. Configuration Source Selector Switch 28
34. SFP Connector 29
35. Differential MGT Input and Output With SMA Connectors 29
36. Serial-ATA Host Connectors 30

37. MGT Clocking Circuitry 30
38. Mini-SMP Connectors for Power Supply Analysis 32
39. IIC Fan Controller and Temperature Monitor 33
Configuration Options 33
JTAG (Parallel Cable IV Cable and System ACE Controller) 33
Platform Flash Memory 34
Linear Flash and CPLD 34

About This Guide

The ML405 evaluation platform enables designers to investigate and experiment with features of the Virtex™-4 family of FPGAs. This user guide describes features and operation of the ML405 evaluation platform.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "ML405 Evaluation Platform" provides an overview of the evaluation platform and details the components and features of the ML405 board
- Appendix A, "Board Revisions" details the differences between board revisions in the ML405 series

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*

Convention	Meaning or Use	Example
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**ngdbuild** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr =**{**on**|**off**}
Vertical bar |	Separates items in a list of choices	**lowpwr =**{**on**|**off**}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

XILINX®

Chapter 1

ML405 Evaluation Platform

Introduction

The ML405 evaluation platform enables designers to investigate and experiment with features of the Virtex™-4 family of FPGAs. This user guide describes features and operation of the ML405 evaluation platform.

Features

- Virtex-4 FPGA:
  - XC4VFX20-FF672
  - SFP connector for SFP module
  - SMA connectors connected to one RocketIO™ multi-gigabit transceiver (MGT)
  - Two serial ATA (SATA) host connectors
  - High-performance, low-jitter LVDS clock synthesizer for SMA/SFP MGT clocks
  - Low-jitter, 75/150-MHz LVDS clock for SATA MGTs
  - Low-jitter, LVDS clock for SGMII MGTs
    - 125 MHz for non-RoHS-compliant boards
    - 250 MHz for RoHS-compliant boards
- 128-MB DDR SDRAM, 32-bit interface running up to 400-MHz data rate
- One differential clock input pair and differential clock output pair with SMA connectors
- One 100-MHz clock oscillator (socketed) plus one extra open 3.3V clock oscillator socket
- General-purpose LEDs and pushbutton switches
- Expansion header with 32 single-ended I/Os, 16 LVDS capable differential pairs, 14 spare I/Os shared with pushbutton switches and LEDs, power, JTAG chain expansion capability, and IIC bus expansion
- Stereo AC97 audio codec with line-in, line-out, 50-mW headphone, and microphone-in (mono) jacks
- RS-232 serial port
- 16-character x 2-line LCD display
- 4-Kb IIC EEPROM
- VGA output with 330-MHz /15-bit video DAC
- PS/2 mouse and keyboard connectors

- System ACE™ CompactFlash configuration controller with Type I/II CompactFlash connector
- ZBT synchronous SRAM (9 Mb) on 32-bit data bus with four parity bits
- Intel StrataFlash (or compatible) linear flash chips (8 MB)
- 10/100/1000 tri-speed Ethernet PHY transceiver
- USB interface chip (Cypress CY7C67300) with host and peripheral ports
- Xilinx XC95144XL CPLD to allow linear flash chips to be used for FPGA configuration
- Xilinx XCF32P Platform Flash configuration storage device
- JTAG configuration port for use with Parallel Cable III, Parallel Cable IV, or Platform USB cable
- IIC fan controller
- Onboard power supplies for all necessary voltages
- 5V @ 6A AC adapter
- Power indicator LED

Package Contents

- Xilinx Virtex-4 ML405 evaluation platform
- System ACE CompactFlash card
- Power supply with power cord
- Carrying case with anti-static foam
- Xilinx serial ATA crossover cable

Additional Information

For current information about your ML405 evaluation platform, see:
http://www.xilinx.com/ml405

The information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-4 features and technology
- Demonstration hardware and software configuration files for the System ACE controller, Platform Flash configuration storage device, CPLD, and linear flash chips
- MicroBlaze™ and PowerPC® 405 EDK reference design files
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in `*.pho` and `*.pdf` for the PC board (There are many free or shareware Gerber file viewers available on the internet for viewing and printing these files)
- Additional documentation, errata, frequently asked questions, and the latest news

For information about the Virtex-4 family of FPGA devices, including product highlights, data sheets, user guides, and application notes, visit the Virtex-4 website at http://www.xilinx.com/virtex4.

Additional information is available from the data sheets and application notes from the component manufacturers.

Block Diagram

Figure 1-1 shows a block diagram of the ML405 evaluation platform (board).

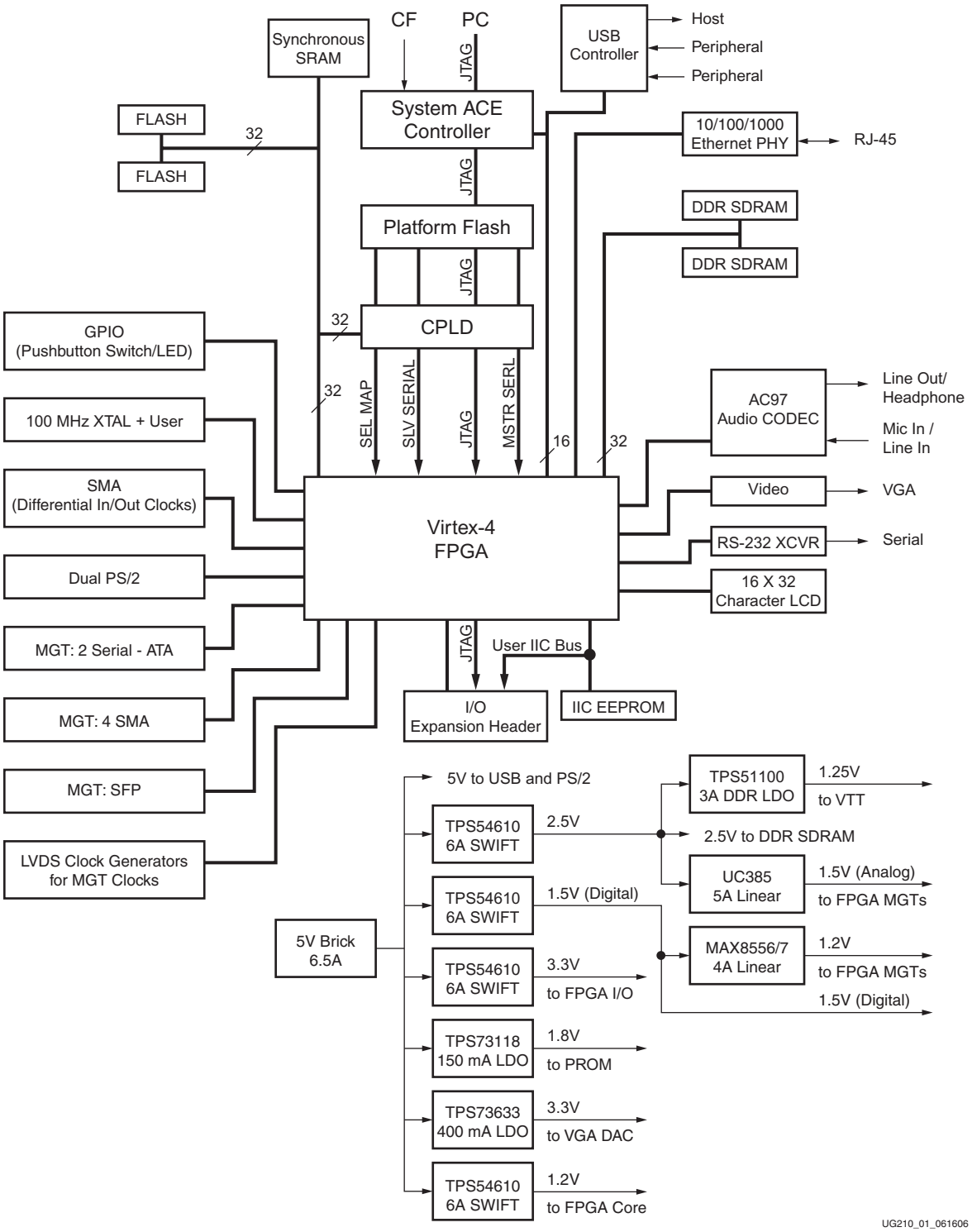


Figure 1-1: **Virtex-4 ML405 Evaluation Platform Block Diagram**

Detailed Description

The ML405 evaluation platform (board) is shown in Figure 1-2 (front) and Figure 1-3, page 11 (back). Each feature is detailed in the corresponding numbered sections that follow.

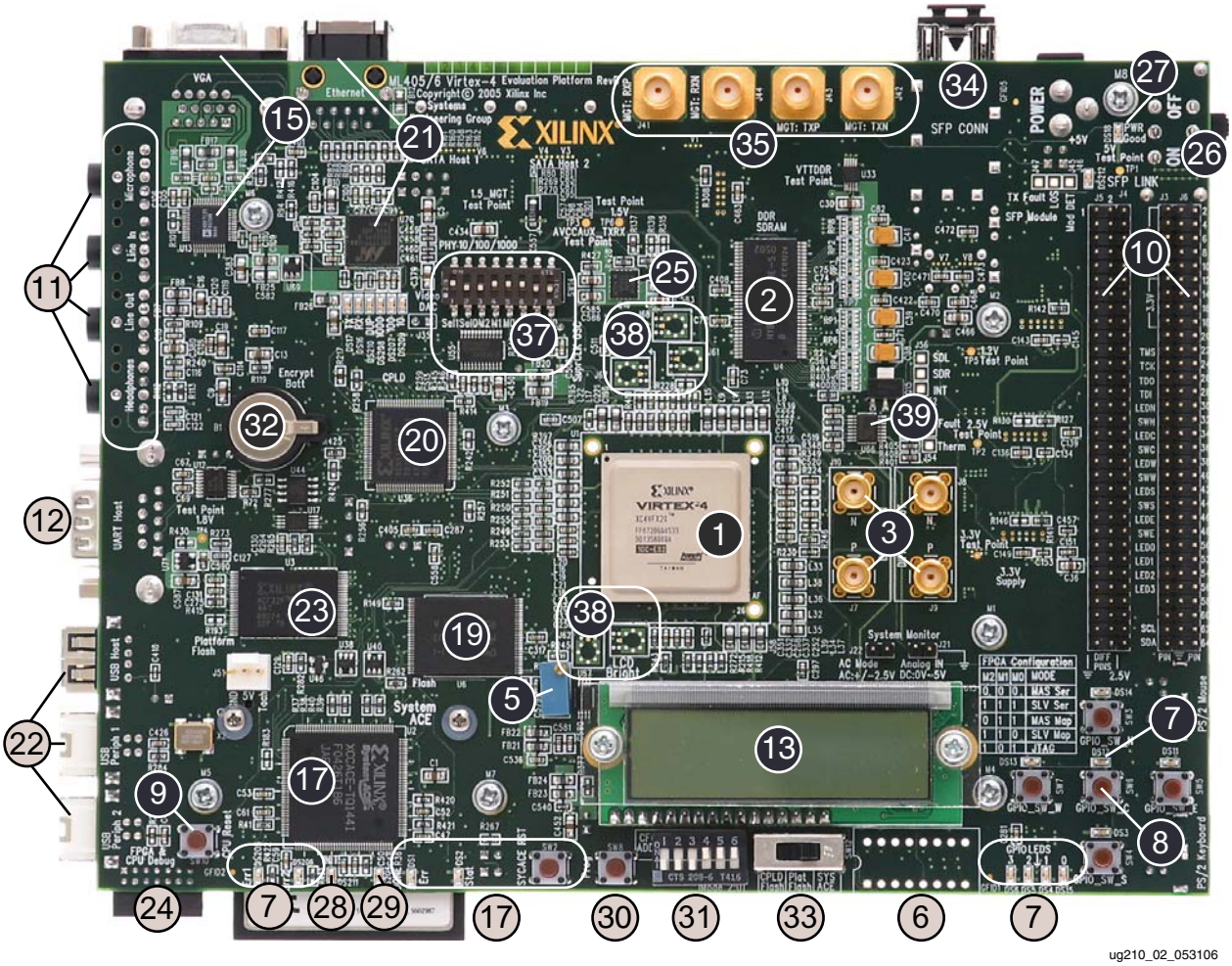


Figure 1-2: **Detailed Description of Virtex-4 ML405 Evaluation Platform Components (Front)**

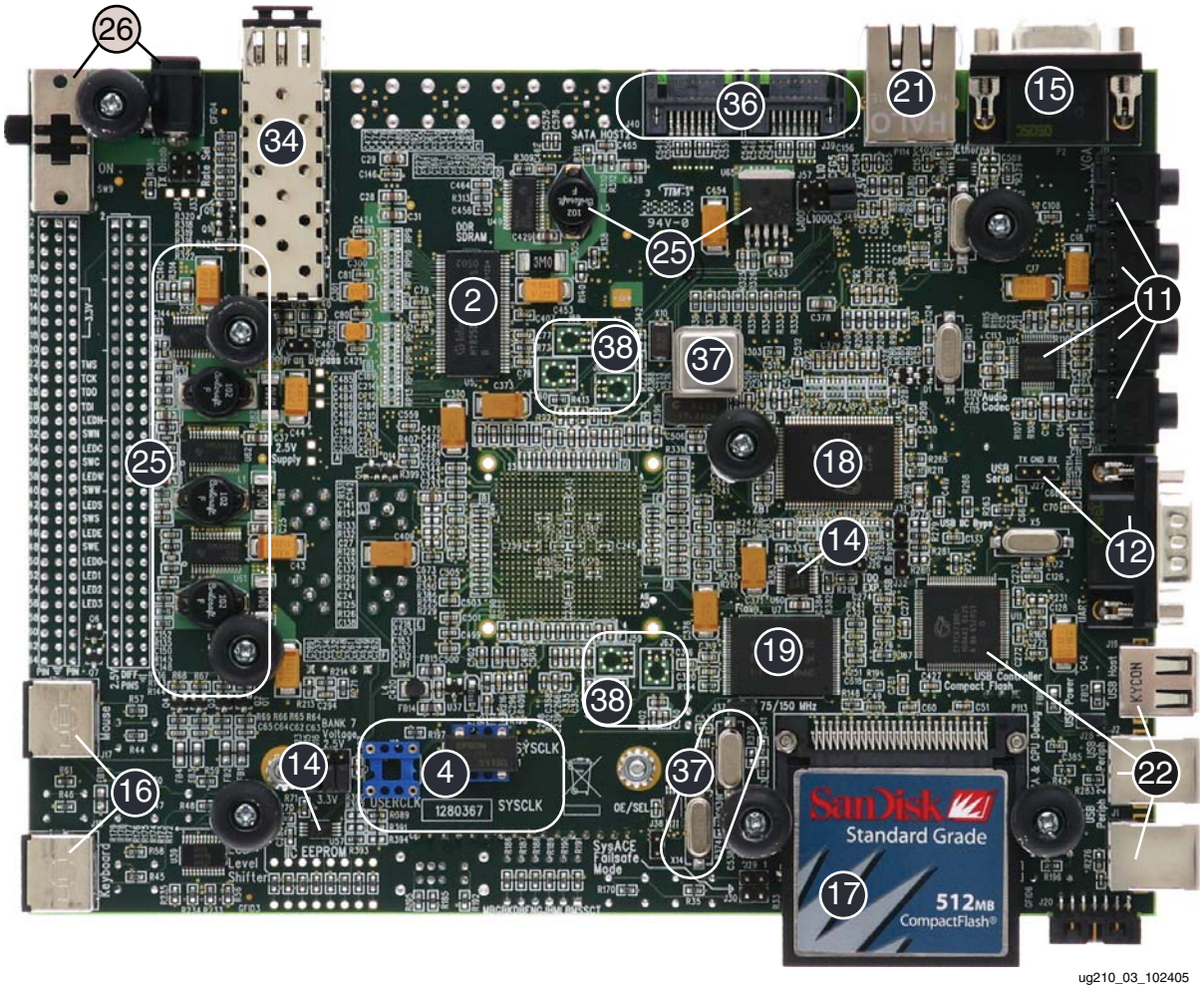


Figure 1-3: **Detailed Description of Virtex-4 ML405 Evaluation Platform Components (Back)**

Note: The label on the CF card shipped with your board might differ from the one shown.

1. Virtex-4 FPGA

A Xilinx Virtex-4 FPGA, XC4VFX20-FF672-10, is installed on the evaluation platform (the board).

Configuration

The board supports configuration in all modes: JTAG, Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP modes. See "Configuration Options," page 33 for more information.

I/O Voltage Rails

The FPGA has 9 banks. The I/O voltage applied to each bank is summarized in Table 1-1. See the *Virtex-4 Data Sheet* for more information regarding I/O standards.

Table 1-1: **I/O Voltage Rail of FPGA Banks**

FPGA Bank	I/O Voltage Rail
0	3.3V
1	3.3V
2	3.3V
3	2.5V
4	3.3V
5	2.5V
6	2.5V
7	User selectable as 2.5V or 3.3V using jumpers J15, J16, and J23.
8	3.3V

Digitally Controlled Impedance (DCI)

Some FPGA banks can support the DCI feature in Virtex-4 FPGAs. Support for DCI is summarized in Table 1-2.

Table 1-2: **DCI Capability of FPGA Bank**

FPGA Bank	DCI Capability
1	Not supported.
2	Not supported.
3	Optional: User must remove resistors R234 and R235 and must install resistors R222 and R221.(1)
4	Not supported.
5	Optional: User must install resistors R224 and R225 to use DCI. In bitgen, the switch "-g DCIUpdateMode:Quiet" must also be used.(2)
6	Not supported.
7	Optional: User must install resistors R289 and R290.(3)
8	Yes, 49.9Ω resistors are installed.

Notes:

1. Use of DCI disables the use of GPIO LED [2] and [3].
2. Use of DCI disables user control of the DDR_CS_N and DDR_CKE signals.
3. This disables the use of two I/O pins on the expansion connector J5 (pin 38 and 40).

2. DDR SDRAM

The board contains 128 MB of DDR SDRAM divided between two Infineon HYB25D512160BT-5 (or compatible) devices (U4 and U5). Each device is 16 bits wide and together form a 32-bit data bus capable of running up to 400 MHz. All DDR SDRAM signals are terminated through 47Ω resistors to a 1.25V VTT reference voltage. The board is designed for matched length traces across all DDR control and data signals except clocks and the DDR loop trace (see "DDR Clock Signal" and "DDR Loop Signal").

The board can support up to 256 MB of total DDR SDRAM memory if larger chips are installed. An extra address pin is present on the board to support up to 1-Gb DDR chips.

DDR Clock Signal

The DDR clock signal is broadcast from the FPGA as a single differential pair that drives both DDR chips. The delay on the clock trace is designed to match the delay of the other DDR control and data signals. The DDR clock is also fed back to the FPGA to allow for clock deskew using Virtex-4 DCMs. The board is designed so that the DDR clock signal reaches the FPGA clock feedback pin at the same time as it arrives at the DDR chips.

DDR Loop Signal

The DDR loop signal is a trace that is driven and then received back at the FPGA with a delay equal to the sum of the trace delays of the clock and DQS signals. This looped trace can be used in high-speed memory controllers to help compensate for the physical trace delays between the FPGA and DDR chips.

3. Differential Clock Input and Output with SMA Connectors

High-precision clock signals can be input to the FPGA using differential clock signals brought in through 50Ω SMA connectors. This allows an external function generator or other clock source to drive the differential clock inputs that directly feed the global clock input pins of the FPGA. The FPGA can be configured to present a 100Ω termination impedance.

A differential clock output from the FPGA is driven out through a second pair of SMA connectors. This allows the FPGA to drive a precision clock to an external device, such as a piece of test equipment. Table 1-3 summarizes the differential SMA clock pin connections.

Table 1-3: **Differential SMA Clock Connections**

Label	Clock Name	FPGA Pin
J10	SMA_DIFF_CLK_IN_N	B12
J7	SMA_DIFF_CLK_IN_P	A12
J8	SMA_DIFF_CLK_OUT_N	H6
J9	SMA_DIFF_CLK_OUT_P	G7

4. Oscillator Sockets

The ML405 evaluation platform has two crystal oscillator sockets, each wired for standard LVTTL-type oscillators. (A 100-MHz oscillator is pre-installed in the X1 SYSCLK socket.) These connect to the FPGA clock pins as shown in Table 1-4. The oscillator sockets accept half-sized oscillators and are powered by the 3.3V supply.

Table 1-4: **Oscillator Socket Connections**

Label	Clock Name	FPGA Pin
X1	SYSCLK	AB14
X6	USERCLK	AB12

5. LCD Brightness and Contrast Adjustment

Turning potentiometer R1 adjusts the image contrast of the character LCD.

6. DIP Switches (Not Installed)

These DIP switches are not installed on the ML405 board.

7. User and Error LEDs (Active-High)

There are 10 active-High LEDs directly controllable by the FPGA (Table 1-5 summarizes the LED definitions and connections):

- Four green LEDs are general-purpose LEDs arranged in a row
- Five green LEDs are positioned next to the north-east-south-west-center oriented pushbutton switches (only the *center* one is cited in Figure 1-2, page 10)
- One red LED is intended to be used for signaling error conditions, such as bus errors, but can also be used for any other purpose. On the ML405 board, the Error 2 LED is not accessible by the FPGA

Table 1-5: **User and Error LED Connections**

Reference Designator	Label/Definition	Color	FPGA Pin
DS14	LED North	Green	G4
DS11	LED East	Green	L7
DS3	LED South	Green	L9
DS13	LED West	Green	G12
DS12	LED Center	Green	E6
DS15	GPIOLEDS 0	Green	A10
DS4	GPIOLEDS 1	Green	B10
DS5	GPIOLEDS 2	Green	F13
DS6	GPIOLEDS 3	Green	F14
DS205	Error 1	Red	L4

8. User Pushbutton Switches (Active-High)

There are five active-High user pushbutton switches available for general-purpose usage and arranged in a north-east-south-west-center orientation (only the *center* one is cited in Figure 1-2, page 10). Table 1-6 summarizes the user pushbutton switch connections.

Table 1-6: **User Pushbutton Switch Connections**

Reference Designator	Label/Definition	FPGA Pin
SW3	GPIO_SW_N	G11
SW5	GPIO_SW_E	M6
SW4	GPIO_SW_S	L10
SW7	GPIO_SW_W	K8
SW6	GPIO_SW_C	D6

9. CPU Reset Pushbutton Switch (Active-Low)

The CPU reset pushbutton switch is active-Low and is used as a system or user reset button. This pushbutton switch is wired only to an FPGA I/O pin so it can also be used as a general-purpose pushbutton switch (Table 1-7).

Table 1-7: **CPU Reset Pushbutton Switch Connections**

Reference Designator	Label/Definition	FPGA Pin
SW10	CPU Reset	M5

10. Expansion Headers

The board contains expansion headers (U3, U4, U5, and U6) for easy expansion or adaptation of the board for other applications. The expansion connectors use standard 0.1-inch headers. The expansion connectors contain connections to single-ended and differential FPGA I/Os, ground, 2.5V/3.3V/5V power, JTAG chain, and the IIC bus. All signals on connectors U5 and U6 have matched length traces that are matched to each other.

Differential Expansion I/O Connectors

Header J5 contains 16 pairs of differential signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed differential signals, such as LVDS data. All differential signals are routed with 100Ω differential trace impedance. Matched length traces are used across all differential signals on U5. Consequently, these signals connect to the FPGA I/O and they can be used as independent single-ended nets. The V_{CCIO} of these signals can be set to 2.5V or 3.3V by setting jumpers J15, J16, and J23. Table 1-8 summarizes the differential connections on this expansion I/O connector.

Table 1-8: **Expansion I/O Differential Connections (J5)**

J5 Differential Pin Pair		Schematic Net Name		FPGA Pin	
Pos	**Neg**	**Pos**	**Neg**	**Pos**	**Neg**
4	2	HDR2_4	HDR2_2	Y22	AA22
8	6	HDR2_28	HDR2_26	AC19	AC18
12	10	HDR2_20	HDR2_18	AA18	Y18
16	14	HDR2_12	HDR2_10	AD16	AC16
20	18	HDR2_8	HDR2_6	U19	T18
24	22	HDR2_60	HDR2_58	AB20	AB19
28	26	HDR2_56	HDR2_54	W20	W19
32	30	HDR2_52	HDR2_50	W18	V18
36	34	HDR2_36	HDR2_34	AB22	AB21
40	38	HDR2_16	HDR2_14	W21	Y20
44	42	HDR2_64	HDR2_62	AB24	AC24
48	46	HDR2_48	HDR2_46	AD24	AD23
52	50	HDR2_24	HDR2_22	AA24	AA23
56	54	HDR2_44	HDR2_42	AA20	AA19
60	58	HDR2_32	HDR2_30	V21	U21
64	62	HDR2_40	HDR2_38	AC23	AC22

Single-Ended Expansion I/O Connectors

Header J6 contains 32 single-ended signal connections to the FPGA I/Os. This permits the signals on this connector to carry high-speed single-ended data. All single-ended signals on connector J6 are matched length traces. The V_{CCIO} of these signals can be set to 2.5V or 3.3V by setting jumpers J15, J16, and J23. Table 1-9 summarizes the single-ended connections on this expansion I/O connector.

Table 1-9: **Expansion I/O Single-Ended Connections (J6)**

J6 Pin	Schematic Net Name	FPGA Pin
2	HDR1_28	Y16
4	HDR1_42	R20
6	HDR1_36	W24
8	HDR1_2	T20
10	HDR1_52	R21
12	HDR1_32	U20
14	HDR1_26	Y15
16	HDR1_12	T22
18	HDR1_50	P24
20	HDR1_38	U17
22	HDR1_40	T17
24	HDR1_22	R23
26	HDR1_10	T24
28	HDR1_60	T23
30	HDR1_24	U24
32	HDR1_4	V23
34	HDR1_30	V22
36	HDR1_6	W23
38	HDR1_34	V24
40	HDR1_18	Y23
42	HDR1_16	AD20
44	HDR1_54	AD21
46	HDR1_56	AC21
48	HDR1_46	AD19
50	HDR1_20	Y17
52	HDR1_14	AD18
54	HDR1_48	AA17

Table 1-9: **Expansion I/O Single-Ended Connections (J6) *(Continued)***

J6 Pin	Schematic Net Name	FPGA Pin
56	HDR1_44	AC17
58	HDR1_58	AB17
60	HDR1_8	AB16
62	HDR1_62	AB15
64	HDR1_64	AA15

Other Expansion I/O Connectors

In addition to the high-speed I/O paths, additional I/O signals and power connections are available to support expansion cards plugged into the ML405 board. The 14 I/O pins from the general-purpose pushbutton switches and LEDs on the board are connected to expansion connector J3. This permits additional I/Os to connect to the expansion connector if the pushbutton switches and LEDs are not used. The connection also allows the expansion card to utilize the pushbutton switches and LEDs on the board.

The expansion connector also allows the board's JTAG chain to be extended onto the expansion card by setting jumper J26 accordingly.

The IIC bus on the board is also extended onto the expansion connector to allow additional IIC devices to be bused together. If the expansion IIC bus is to be utilized, the user must have the IIC pull-up resistors present on the expansion card. Bidirectional level shifting transistors allow the expansion card to utilize 2.5V to 5V signaling on the IIC bus.

Power supply connections to the expansion connectors provide ground, 2.5V, 3.3V, and 5V power pins. If the expansion card draws significant power from the ML405 board, ensure that the total power draw can be supplied by the board.

The ML405 expansion connector is backward compatible with the expansion connectors on the ML32X and ML42X boards, thereby allowing their daughter cards to be used with the ML405 evaluation platform. Table 1-10, page 20 summarizes the additional expansion I/O connections.

Table 1-10: **Additional Expansion I/O Connections (J3)**

J3 Pin	Label	FPGA Pin	Description
1	VCC5	–	5V Power Supply
2	VCC5	–	5V Power Supply
3	VCC5	–	5V Power Supply
4	VCC5	–	5V Power Supply
5	NC	–	Not Connected
6	VCC3V3	–	3.3V Power Supply
7	VCC3V3	–	3.3V Power Supply
8	VCC3V3	–	3.3V Power Supply
9	VCC3V3	–	3.3V Power Supply
10	NC	–	Not Connected
11	TMS	–	Expansion TMS
12	TCK	–	Expansion TCK
13	TDO	–	Expansion TDO
14	TDI	–	Expansion TDI
15	DS14	E2	LED North
16	SW3 (GPIO_SW_N)	E7	GPIO Switch North
17	DS12	C6	LED Center
18	SW6 (GPIO_SW_C)	B6	GPIO Switch Center
19	DS13	F9	LED West
20	SW7 (GPIO_SW_W)	E9	GPIO Switch West
21	DS3	A5	LED South
22	SW4 (GPIO_SW_S)	A6	GPIO Switch South
23	DS11	E10	LED East
24	SW5 (GPIO_SW_E)	F10	GPIO Switch East
25	GPIOLED 0	G5	GPIO LED 0
26	GPIOLED 1	G6	GPIO LED 1
27	GPIOLED 2	A11	GPIO LED 2
28	GPIOLED 3	A12	GPIO LED 3
29	NC	–	Not Connected
30	NC	–	Not Connected
31	EXP_IIC_SCL	A17	Expansion IIC SCL
32	EXP_IIC_SDA	B17	Expansion IIC SDA

11. Stereo AC97 Audio Codec

The ML405 evaluation platform has an AC97 audio codec (U14) to permit audio processing. The National Semiconductor LM4550 Audio Codec supports stereo 16-bit audio with up to 48-kHz sampling. The sampling rate for record and playback can be different.

Note: The reset for the AC97 codec is shared with the reset signal for the flash memory chips and is asserted at power-on or upon system reset.

Separate audio jacks are provided for Microphone, Line In, Line Out, and Headphone. All jacks are stereo except for Microphone. The Headphone jack is driven by the audio codec's internal 50-mW amplifier. Table 1-11 summarizes the audio jacks.

Table 1-11: **ML405 Audio Jacks**

Reference Designator	Description	
	Function	Stereo/Mono
J11	Microphone - In	Mono
J12	Analog Line - In	Stereo
J13	Analog Line - Out	Stereo
J14	Headphone - Out	Stereo

12. RS-232 Serial Port

The ML405 board contains one male DB-9 RS-232 serial port, allowing the FPGA to communicate serial data with another device. The serial port is wired as a host (DCE) device. Therefore, a null modem cable is normally required to connect the board to the serial port on a PC. The serial port is designed to operate up to 115200 Bd. An interface chip is used to shift the voltage level between FPGA and RS-232 signals.

Note: The FPGA is connected only to the TX and RX data pins on the serial port. Therefore, other RS-232 signals, including hardware flow-control signals, are not used. Flow control should be disabled when communicating with a PC.

A secondary serial interface is available by using header J27 to support debug of the USB controller chip. Header J27 brings out RS-232 voltage level signals for ground, TX data, and RX data.

13. 16-Character x 2-Line LCD

The ML405 board has a 16-character x 2-line LCD (Lumex LCM-S01602DTR/M) on the board to display text information. Potentiometer R1 adjusts the contrast of the LCD. The data interface to the LCD is connected to the FPGA to support 4-bit mode only. A level translator chip is used to shift the voltage level between the FPGA and the LCD.

Note: Care should be taken not to scratch or damage the surface of the LCD window.

14. IIC Bus with 4 Kb EEPROM

An IIC EEPROM (Microchip Technology 24LC04B-I/ST) is provided on the ML405 board to store non-volatile data such as an Ethernet MAC address. The EEPROM write protect is disabled on the ML405 board. The IIC bus uses 2.5V signaling and can operate at up to 400 kHz. IIC bus pull-up resistors are provided on the board.

The IIC bus is extended to the expansion connector so that the user can add additional IIC devices and share the IIC controller in the FPGA. If the expansion IIC bus is used, the user must have additional IIC pull-up resistors present on the expansion card. Bidirectional level shifting transistors allow the expansion card to use 2.5V to 5V signaling on the IIC bus.

A dual 1-of-4 FET multiplexer/demultiplexer chip (U60) allows the FPGA to independently access multiple IIC buses without concern for IIC device address overlap. See Table 1-12 for summary of IIC Mux options.

Table 1-12: **IIC Mux Options**

IIC Bus Connection	IIC_SEL_1	IIC_SEL_0
IIC EEPROM and expansion connector (1)	0	0
SFP Module	0	1
VGA Connector (to read monitor configuration parameters, for example: plug-and-play support)	1	0
USB Controller's IIC EEPROM	1	1

Notes:

1. Pull-down resistors default the IIC Mux to this connection

15. VGA Output

A VGA output port (P2) is present on the board to support an external video monitor. On ML405, the VGA circuitry utilizes a 330-MHz, 15-bit color video DAC (Analog Devices ADV7125JST330). The FPGA can drive only five bits of data per color (red, green, and blue).

The VGA connector supports the IIC protocol to allow the board to read the monitor's configuration parameters (for example, plug and play support. See "14. IIC Bus with 4 Kb EEPROM" for more information.

16. PS/2 Mouse and Keyboard Ports

The ML405 evaluation platform contains two PS/2 ports: one for a mouse (J17) and the other for a keyboard (J18). Bidirectional level shifting transistors allow the FPGA's 2.5V I/O to interface with the 5V I/O of the PS/2 ports. The PS/2 ports on the board are powered directly by the main 5V power jack; this jack also powers the rest of the board.

Caution! The power load of any attached PS/2 device must not overload the AC adapter.

17. System ACE Controller

The Xilinx System ACE CF configuration controller allows a Type I or Type II CompactFlash card to program the FPGA through the JTAG port. Both hardware and software data can be downloaded through the JTAG port. The System ACE controller can support up to eight configuration images on a single CompactFlash card. The configuration address pushbutton switches allow the user to choose which of the eight configuration images to use.

System ACE error and status LEDs indicate the operational state of the System ACE controller:

- A blinking red error LED indicates that no CompactFlash card is present
- A solid red error LED indicates an error condition during configuration
- A blinking green status LED indicates a configuration operation is ongoing
- A solid green status LED indicates a successful download

Every time a CompactFlash card is inserted into the System ACE socket, a configuration operation is initiated. Pressing the System ACE reset pushbutton switch reprograms the FPGA.

The board also features a System ACE *failsafe* mode. In this mode, if the System ACE controller detects a failed configuration attempt, it automatically reboots back to a predefined configuration image. The failsafe mode is enabled by inserting two jumpers across J29 and J30 (in horizontal or vertical orientation).

> ***Caution!*** Insert or remove the CompactFlash card only when the board power is off. Use caution when inserting a CompactFlash card with exposed metallic surfaces. Inserting the card incorrectly can cause a short with the traces or components on the board.

The System ACE MPU port is connected to the FPGA. This allows the FPGA to control the System ACE chip and use it to reconfigure the system or access the CompactFlash card as a generic FAT file system. The data bus for the System ACE MPU port is shared with the USB controller.

For configuration through the System ACE controller, the configuration selector switch (SW12) must be set to the SYS ACE position.

18. ZBT Synchronous SRAM

The ZBT synchronous SRAM (Cypress CY7C1354B or compatible) provides high-speed, low-latency external memory to the FPGA. The memory is organized as 256K x 36 bits. This provides for a 32-bit data bus with support for four parity bits.

The SRAM and FLASH memory share the same data bus. The parity bits are not available on the ML405 board.

19. Linear Flash

Two 32-Mb linear flash devices (Micron MT28F320J3RG-11 ET) are installed on the board for a total of 8 MB of flash memory. These flash memory devices are Intel StrataFlash compatible. This memory provides non-volatile storage of data, software, or bitstreams. Each flash device is 16 bits wide and together forms a 32-bit data bus that is shared with SRAM. Each flash device is 16 bits wide, and the two devices together form a 32-bit data bus that is shared with SRAM.In conjunction with a CPLD, the flash memory can also be used to program the FPGA.

Note: The reset for the AC97 Codec is shared with the reset signal for the flash memory chips and is designed to be asserted at power-on or upon system reset.

20. Xilinx XC95144XL CPLD

A Xilinx XC95144XL CPLD is connected to the flash memory and the FPGA configuration signals. This supports applications where flash memory programs the FPGA. The CPLD is programmed from the main JTAG chain of the board. The CPLD is wired so that it can support master or slave configuration in serial or parallel (SelectMAP) modes. For FPGA configuration via the CPLD and flash, the configuration selector switch (SW12) must be set to the CPLD Flash position. See the "Configuration Options," page 33 section for more information.

21. 10/100/1000 Tri-Speed Ethernet PHY

The ML405 evaluation platform contains a Marvell Alaska PHY device (88E1111) operating at 10/100/1000 Mb/s (Table 1-13). The board supports MII, GMII, RGMII, and SGMII interface modes with the FPGA. The PHY is connected to a Halo HFJ11-1G01E RJ-45 (or compatible) connector with built-in magnetics. A 25-MHz crystal supplies the clock signal to the PHY. The PHY is configured to default at power-on or reset to the settings shown in Table 1-19, page 31. These settings can be overwritten via software, except PHYADR[4:0].

Table 1-13: **Board Connections for PHY Configuration Pins**

Config Pin	Connection on Board	Bit[2] Definition and Value	Bit[1] Definition and Value	Bit[0] Definition and Value
CONFIG0	VCC 2.5V	PHYADR[2] = 1	PHYADR[1] = 1	PHYADR[0] = 1
CONFIG1	Ground	ENA_PAUSE = 0	PHYADR[4] = 0	PHYADR[3] = 0
CONFIG2	VCC 2.5V	ANEG[3] = 1	ANEG[2] = 1	ANEG[1] = 1
CONFIG3	VCC 2.5V	ANEG[0] = 1	ENA_XC = 1	DIS_125 = 1
CONFIG4	VCC 2.5V	HWCFG_MODE[2] = 1	HWCFG_MODE[1] = 1	HWCFG_MODE[0] = 1
CONFIG5	VCC 2.5V	DIS_FC = 1	DIS_SLEEP = 1	HWCFG_MODE[3] = 1
CONFIG6	LED_RX	SEL_BDT = 0	INT_POL = 1	75/50Ω = 0

Jumpers J48, J49, and J57 allow the user to select the default interface that the PHY uses (Table 1-14). The interface can also be changed via MDIO commands.

Table 1-14: **PHY Default Interface Mode**

Mode	Jumper Settings		
	J48	J49	J57
GMII/MII to copper (default)	Jumper over pins 1-2	Jumper over pins 1-2	No jumper
SGMII to copper, no clock	Jumper over pins 2-3	Jumper over pins 2-3	No jumper
RGMII	Jumper over pins 1-2	No jumper	Jumper on

22. USB Controller with Host and Peripheral Ports

A Cypress CY7C67300 embedded USB host controller provides USB connectivity for the board. The USB controller supports host and peripheral modes of operation. The USB controller has two serial interface engines (SIE) that can be used independently. SIE1 is connected to the USB Host 1 connector (J19) and the USB Peripheral 1 connector (J2). SIE2 is connected only to the USB Peripheral 2 connector.

When using SIE1, the port can only be configured at boot-up to use either the host or peripheral connector, but not both at the same time.

The USB controller has an internal microprocessor to assist in processing USB commands. The firmware for this processor can be stored in its own dedicated IIC EEPROM (U17) or downloaded from a host computer via a peripheral connector. The USB controller's serial port is connected to J27 through an RS-232 transceiver to assist with debug.

23. Xilinx XCF32P Platform Flash Configuration Storage Device

Xilinx XCF32P Platform Flash configuration storage device offers a convenient and easy-to-use configuration solution for the FPGA. The Platform Flash memory holds up to four separate configuration images that can be accessed through the configuration address switches. To use the Platform Flash memory to configure the FPGA, the configuration selector switch (SW12) must be set to the Plat Flash position.

The Platform Flash memory can be used to program the FPGA using master or slave configuration in serial or parallel (SelectMap) modes. The Platform Flash memory is programmed using Xilinx iMPACT software through the board's JTAG chain. See "Configuration Options," page 33 for more information.

24. JTAG Configuration Port

The JTAG configuration port (J20) allows for device programming and FPGA debug. The JTAG port supports the Xilinx Parallel Cable III, Parallel Cable IV, or Platform Cable USB products. Third-party configuration products might also be available. The JTAG chain can be extended to an expansion board by setting jumper J26 accordingly. See "Configuration Options," page 33 for more information.

25. Onboard Power Supplies

Power supply circuitry on the board generates 1.2V, 1.25V, 1.2V (MGT), 1.5V, 1.8V, 2.5V, and 3.3V voltages to power the components on the board. The 1.2V, 1.5V (digital), 2.5V, and 3.3V supplies are driven by switching power regulators. When these switching regulators report they are running at their nominal voltages, the PWR Good LED turns on.

The diagram in Figure 1-4 shows the power supply architecture and maximum current handling on each supply. The typical operating currents are significantly below the maximum capacity. The ML405 board normally ships with a 30W power supply that should be sufficient for most applications.

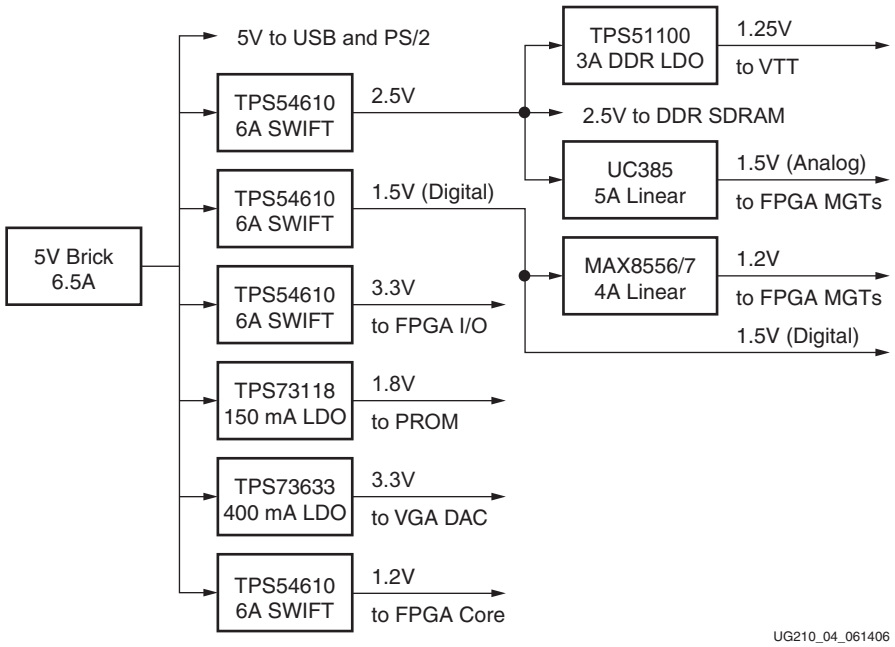


Figure 1-4: **Power Supply Diagram**

Special analog voltage regulators on the board produce a clean 1.2V and 1.5V (analog) supply circuitry for the MGT. A separate 3.3V analog regulator produces a clean analog 3.3V power supply for the video DAC.

26. AC Adapter and Input Power Switch/Jack

The ML405 board ships with a 30W (5V @ 6A) AC adapter. The power connector is a 2.1 mm x 5.5 mm barrel type plug (center positive). For applications requiring additional power, such as the use of expansion cards drawing significant power, a larger AC adapter might be required. If a different AC adapter is used, its load regulation should be less than 10% or better than ± 10%. The power switch turns the board on and off by controlling the supply of 5V to the board.

27. Power Indicator LED

The PWR Good LED lights when the 1.2V, 1.5V, 2.5V, and 3.3V power supplies are all at their nominal operating conditions. If the PWR Good LED is off, blinking, or glowing lightly, a fault condition, such as a short or overload condition, might exist.

28. INIT LED

The INIT LED lights upon power-up to indicate that the FPGA has successfully powered up and completed its internal power-on process.

29. DONE LED

The DONE LED indicates the status of the DONE pin on the FPGA. It illuminates when the FPGA is successfully configured.

30. Program Switch

This switch grounds the FPGA's Program pin when pressed and clears the FPGA.

31. Configuration Address and Mode DIP Switches

This 6-position DIP switch controls the configuration address and FPGA configuration mode.

The three leftmost switches choose one of eight possible configuration addresses. It provides the System ACE controller and the CPLD the possibility of using up to eight different configuration images as set by these three switches. The Platform Flash memory supports up to four different images.

The three rightmost DIP switches set the FPGA configuration mode pins M2, M1, and M0 as shown in Table 1-15.

Table 1-15: **Configuration Mode DIP Switch Settings**

M2	M1	M0	Mode
0	0	0	Master Serial
1	1	1	Slave Serial
0	1	1	Master Parallel (SelectMAP)
1	1	0	Slave Parallel (SelectMAP)
1	0	1	JTAG

32. Encryption Key Battery

An onboard battery holder is connected to the VBATT pin of the FPGA to hold the encryption key for the FPGA. Use a 12-mm lithium coin battery (3V), such as Panasonic part numbers BR1216, CR1216, and BR1225, or any other appropriate 12-mm lithium coin battery (3V).

33. Configuration Source Selector Switch

The configuration source selector switch (SW12) selects between System ACE CF, Platform Flash, and linear flash/CPLD methods of programming the FPGA. Whichever method is selected to program the FPGA, make sure the FPGA configuration mode switches are set appropriately for the desired method of configuration. The PC4 connector allows JTAG download and debug of the board regardless of the setting of the configuration source selector switch.

34. SFP Connector

The board contains a small form-factor pluggable (SFP) connector and cage assembly (U54) that accepts SFP modules. The SFP interface is connected to MGT 102B on the FPGA. The SFP module serial ID interface is connected to the IIC mux on the board (See "14. IIC Bus with 4 Kb EEPROM," page 22 for more information). The control and status signals for the SFP module are connected to jumpers, test points, and LEDs as described in Table 1-16.

Table 1-16: **Configuration for SEP Module Control and Status Signals**

SFP Control/Status Signal	Board Connection
SFP TX FAULT	Test Point J47 • High = Fault • Low = Normal Operation
SFP TX DISAB	Jumper J34 • Jumper Off = SFP Enabled • Jumper On = SFP Disabled
SFP MOD DETECT	Test Point J46 • High = Module Not Present • Low = Module Present
SFP RT SEL	Jumper J33 • Jumper Off = Full Bandwidth • Jumper On = Reduced Bandwidth
SFP LOS	Test Point J45 • High = Loss of Receiver Signal • Low = Normal Operation LED DS212 • LED Off = Loss of Receiver Signal • LED On = Normal Operation

35. Differential MGT Input and Output With SMA Connectors

Four SMA connectors (Rosenberger 32K153-400E3) along the top edge of the board connect to MGT 102A on the FPGA. The SMA connectors provide a convenient and easily accessible method of interfacing to MGTs for general-purpose connectivity. The SMAs are designed and laid out to provide high-quality MGT connections for speeds up to 3.125 Gb/s.

The transmit pair is connected directly from the FPGA to the SMA connectors while the receive pair is connected to the FPGA via series AC coupling capacitors. If a DC-coupled receive-side connection is desired, these capacitors can be replaced with 0Ω 0402-size resistors.

36. Serial-ATA Host Connectors

Serial-ATA (SATA) is the next generation of the ATA interface used for storage devices such as hard disks. The board contains two SATA host connectors that can be connected to a SATA device (such as a hard disk) using a standard SATA cable. The SATA connectors are connected to MGTs on the FPGA (Table 1-17).

Table 1-17: **SATA Connection Configuration**

SATA Connector	FPGA Connection
SATA Host 1 Connector (J39)	MGT 113B
SATA Host 2 Connector (J40)	MGT 113A

SATA can also be used as a convenient and low cost medium for connecting MGTs. The SATA physical interface can carry MGT signals up to 1.5 Gb/s for general-purpose usage. The board ships with a special Xilinx SATA crossover cable that is used as a loopback connection between the two SATA host connectors for:

- Loopback testing
- Bit error rate testing (BERT)

The SATA crossover cable can also be used to connect MGTs between two boards.

Note: The special SATA crossover cable cannot be used to connect a SATA host to a SATA device (that is, PC to hard disk). It is only intended for host-to-host loopback connections.

37. MGT Clocking Circuitry

Overview

Low jitter LVDS clock sources on the board provide high-quality reference clocks for the MGTs. Different clock sources are provided to support each of the MGT interfaces on the board. Table 1-18 provides a summary of the MGT clock sources.

Table 1-18: **MGT CLock Sources**

Clock Source	Frequency	MGT Clock Input	FPGA Differential Pair Pin	
			Positive	Negative
SFP/SMA MGT	Variable	MGT 102 Clock	F26	G26
SATA MGT	75 or 150 MHz	MGT 113 Clock	K1	L1
SGMII/Loopback MGT	250 MHz(1)	MGT 105 Clock	AF21	AF20

Notes:

1. All non-RoHS-compliant boards use a 125-MHz clock. See Appendix A, "Board Revisions" for details.

Frequency Synthesizer for SFP/SMA MGT Clocking

An Integrated Circuit Systems ICS843001-21 frequency synthesizer chip offers flexible, low-jitter clock generation for the MGT pair connected to SFP and SMA interfaces. The ICS843001-21 is connected to a 19.44-MHz crystal and a socketed 25-MHz oscillator (X7).

DIP switches (SW14) enable the user to select clock source and frequency synthesis options to generate a number of commonly used frequencies for applications, such as Gigabit Ethernet and SONET (Table 1-19). For other frequencies, consult the ICS843001-21 data sheet for more information. The 25-MHz oscillator is socketed to allow the user to change the oscillator frequency and use the entire range of possible synthesized frequency outputs.

Table 1-19: **Configurations for Clock Source and Frequency Options**

DIP Switch SW14 [1:8] Value								Input Ref Clock (MHz)	M Divider Value	N Divider Value	V_{CO} (MHz)	Output Frequency (MHz)	Application
SEL1	SEL0	M2	M1	M0	N2	N1	N0						
0	1	1	0	0	0	1	1	19.44	32	4	622.08	155.52	SONET
0	1	1	0	0	1	1	0	19.44	32	8	622.08	77.76	SONET
0	1	1	0	0	0	0	0	19.44	32	1	622.08	622.08	SONET
0	1	1	0	0	0	0	1	19.44	32	2	622.08	311.04(1)	SONET
1	0	0	1	1	1	0	0	25	25	5	625	125	Gigabit Ethernet
1	0	0	1	1	1	1	1	25	25	10	625	62.5	Gigabit Ethernet
1	0	0	1	0	1	0	1	25	24	6	600	100	PCI Express
1	0	0	1	0	0	1	1	25	24	4	600	150	SATA
1	0	0	1	1	0	1	1	25	25	4	625	156.25	XAUI/SRIO

Notes:

1. Factory default setting.
2. A 1 equates to the DIP switch in the on position.
3. For Fibre Channel support, see Answer Record 24921.

The native output of the ICS843001-21 is LVPECL, so a resistor network is present to change the voltage swing to LVDS levels. The LVDS output is then multiplexed out through Series AC coupling capacitors to allow the clock input of the FPGA to set the common mode voltage.

SATA MGT Clock Generation

An Integrated Circuit Systems ICS844051-1 chip generates a high-quality, low-jitter, 75-MHz or 150-MHz LVDS clock from an inexpensive 25-MHz crystal oscillator. This clock is sent to the MGT driving the SATA connectors. Jumper J37 sets the SATA MGT clock frequency (Table 1-20). Series AC coupling capacitors are also present to allow the clock input of the FPGA to set the common mode voltage.

Table 1-20: **Configuration for SATA MGT Clock Signals**

SATA Clock Signal	Board Connection
SATA Clock Frequency	Jumper J37 • Jumper Off = 75 MHz • Jumper On = 150 MHz

SGMII / Loopback MGT Clock Generation

An Integrated Circuit Systems ICS844031I chip generates a high-quality, low-jitter, 250-MHz LVDS clock from an inexpensive 20-MHz crystal oscillator on all RoHS-compliant boards. For non-RoHS-compliant boards, an ICS844021I chip generates a high-quality, low-jitter, 125-MHz LVDS clock from an inexpensive 25-MHz crystal oscillator. See Appendix A, "Board Revisions" for details on MGT clocking. The SGMII clock is sent to the MGTs driving the SGMII or onboard loopback interfaces. Series AC coupling capacitors are also present to allow the clock input of the FPGA to set the common mode voltage.

38. Mini-SMP Connectors for Power Supply Analysis

The Mini-SMP connector (Rosenberger 18S101-40ME4) is a small, form-factor, surface-mount, 50Ω coaxial connector suitable for high-frequency signal analysis.

The board supports having a pair of Mini-SMP connectors attached to each of the main power supplies. This permits the user to perform spectrum analysis of the behavior of the power supply during board operation. This can help the user tune the power supply decoupling network for optimal performance. Because two Mini-SMP connectors are attached to a given power supply, the user can also use one Mini-SMP connector to inject a high frequency signal into the power plane while the second Mini-SMP is connected to test equipment that measures the response of the board.

By default, the Mini-SMP connectors are not soldered on. Contact Rosenberger of North America (www.rosenbergerna.com) to order the Mini-SMP connector. Rosenberger also manufactures adapter cables that allow SMA-based test equipment or cables to be connected to the Mini-SMP connectors.

Note: Xilinx is not responsible for damage caused by a user attempting to solder the Mini-SMP connectors onto the board.

39. IIC Fan Controller and Temperature Monitor

The board contains an IIC controlled fan controller chip and fan connector. The Maxim MAX6653 fan controller (U66) contains on-chip and remote temperature monitors. The on-chip temperature measures the ambient temperature near the surface of the board. The remote temperature monitoring pins are connected to the FPGA TDP/TDN pins that access a temperature diode in the FPGA.

The MAX6653 also offers other features such as fan speed control, tachometer, and programmable speed control based on temperature trip points.

Connector J51 is a keyed three-pin fan header similar to those found in PCs. It is designed to support a 5V DC fan. To bypass the fan controller chip and operate the fan at full speed, the user can populate connector J50.

For high-power operating conditions, a heatsink and/or fan can be accommodated on the board. The ML405 does not ship with a heatsink/fan unit but can accommodate one (for example, Calgreg Electronics Smart-CLIP family of heatsink/fan assemblies).

Configuration Options

The FPGA on the ML405 evaluation platform can be configured by four major devices:

- Parallel Cable IV or other download cable (JTAG)
- System ACE controller (JTAG)
- Platform Flash memory
- Linear flash + CPLD

The following section provides an overview of the possible ways the board can be configured.

JTAG (Parallel Cable IV Cable and System ACE Controller)

The FPGA, Platform Flash memory, and CPLD can be configured through the JTAG port. The JTAG chain of the board is illustrated in Figure 1-5.

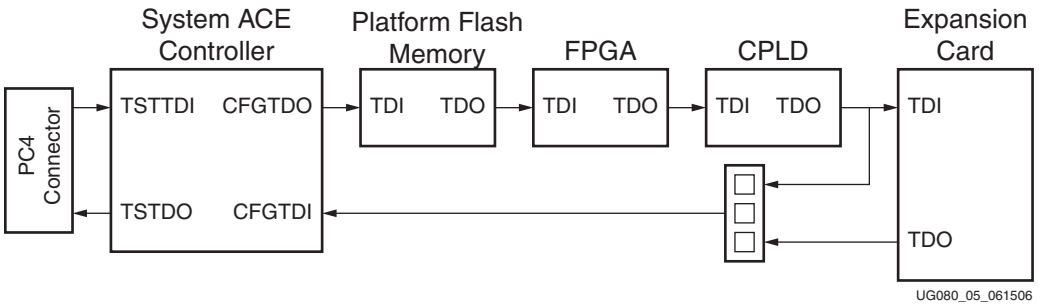


Figure 1-5: **JTAG Chain**

The chain starts at the PC4 connector and goes through the System ACE controller, the Platform Flash memory, the FPGA, the CPLD, and an optional extension of the chain to the expansion card. Jumper J26 determines if the JTAG chain should be extended to the expansion card.

The JTAG chain can be used to program the FPGA and access the FPGA for hardware and software debug. The JTAG chain is also used to program the Platform Flash memory and the CPLD.

The PC4 JTAG connection to the JTAG chain allows a host PC to download bitstreams to the FPGA using the iMPACT software tool. PC4 also allows debug tools such as the ChipScope™ Pro Analyzer or a software debugger to access the FPGA.

The System ACE controller can also program the FPGA through the JTAG port. Using an inserted CompactFlash card or Microdrive storage device, configuration information can be stored and played out to the FPGA. The System ACE controller supports up to eight configuration images that are selected via the three configuration address DIP switches. Under FPGA control, the System ACE chip can be instructed to reconfigure to any of the eight configuration images.

The configuration source selector switch should be in the SYS ACE program setting if the use of the System ACE controller is desired.

When the switch is set to the SYS ACE position, the System ACE controller programs the FPGA from the image on the CompactFlash card at power-up. Pressing the System ACE reset pushbutton switch also causes the System ACE controller to program the FPGA if a CompactFlash card is present.

Platform Flash Memory

The Platform Flash memory can also be used to program the FPGA. The Platform Flash memory can hold up to four configuration images, which are selectable by the two least significant bits of the configuration address DIP switches.

The board is wired so the Platform Flash memory can download bitstreams in Master Serial, Slave Serial, Master SelectMAP (parallel), or Slave SelectMAP (parallel) modes. Using the iMPACT tool to program the Platform Flash memory, the user has the option to select which of the four modes to use for programming the FPGA. The configuration mode DIP switches on the board must be set to match the programming method being used by the Platform Flash memory.

The configuration source selector switch should be set to Plat Flash if the use of Platform Flash memory is desired.

When set correctly, the Platform Flash memory programs the FPGA upon power-up or whenever the Prog pushbutton switch is pressed.

Linear Flash and CPLD

Data stored in the linear flash can be read by the CPLD and used to program the FPGA. Depending on the logic design in the CPLD, up to eight configuration images can theoretically be supported.

The board is wired so the CPLD can download bitstreams via Master Serial, Slave Serial, Master SelectMAP (parallel), or Slave SelectMAP (parallel) modes. The configuration mode DIP switches on the board must be set to match the programming method being used by the CPLD.

The configuration source selector switch should be in the CPLD Flash setting if the use of CPLD and Platform Flash is desired.

When set correctly, the CPLD programs the FPGA upon power-up or whenever the Prog pushbutton switch is pressed.

Appendix A

Board Revisions

This appendix describes the major differences in revisions of the ML405 platform. Table A-1 shows the features unique to each ML405 platform.

Table A-1: **Differences in Board Revisions**

	Board P/N		
	HW-V4-ML405-US/UK/EU	**HW-V4-ML405-UNI-G**	
Build number	All	–01 and –02	–03
RoHS-compliant	No	Yes	Yes
Virtex-4 FX FPGA	FF672	FFG672	FFG672
SGMII Clock(1)	125 MHz U52 - ICS844021 X14 - 25 MHz	125 MHz U52 - ICS844021 X14 - 25 MHz	250 MHz U52 - ICS844031 X14 - 20 MHz

Notes:

1. X14 and U52 are located on the back side of the PCB near the CompactFlash connector, P113. Pin-compatible replacement devices are used on X14 and U52.

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP