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XVME 505/595

Analog Output Module

P/N 74505-001

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Chapter 1

MODULE DESCRIPTION

1.1 INTRODUCTION

The XVME-505 and the XVME-595 are powerful VMEbus compatible Analog Output Modules. Both Modules are capable of performing digital to analog conversions, with I2-bit resolution. The XVME-505 is a single-high, single-wide (3U) module, while the XVME-595 is a double-high, single-wide (6U) module. Both the XVME-505 and XVME-595 Analog Output Modules are available in either of two versions:

1) XVME-505/595-l: Providing 4 voltage output channels (either unipolar or bipolar) in the ranges 0-5V, 0-I0V, ±5V, or ±10V.

OR

2) XVME-505/595-2: Providing 4 channels which may be configured for either voltage output (in the same ranges as the above option) or current loop output (in the range 4 to 20mA).

1.2 MANUAL STRUCTURE

It is the aim of this first chapter to introduce the user to the general specifications and functional capabilities of the XVME-505/595 Analog Output Modules. Successive chapters will develop the various aspects of module specification and operation in the following progression:

Chapter One - A general description of the Analog Output Module, including complete functional and environmental specifications, VMEbus compliance information, and a detailed block diagram.

Chapter Two - Module installation information, covering module specific system requirements, jumpers, and connector pinouts.

Chapter Three - Presents information required to operate the Modules in standard analog output applications.

Chapter Four - A short chapter covering the procedures for analog output circuit calibration.

The appendices at the rear of this manual are designed to introduce and reinforce a variety of module-related topics including: backplane signal/pin descriptions, a block diagram and schematics, and a quick reference section.

1.3 MODULE OPERATIONAL DESCRIPTION

Figure l-l shows an operational block diagram of the XVME-505/595 Analog Output Modules.

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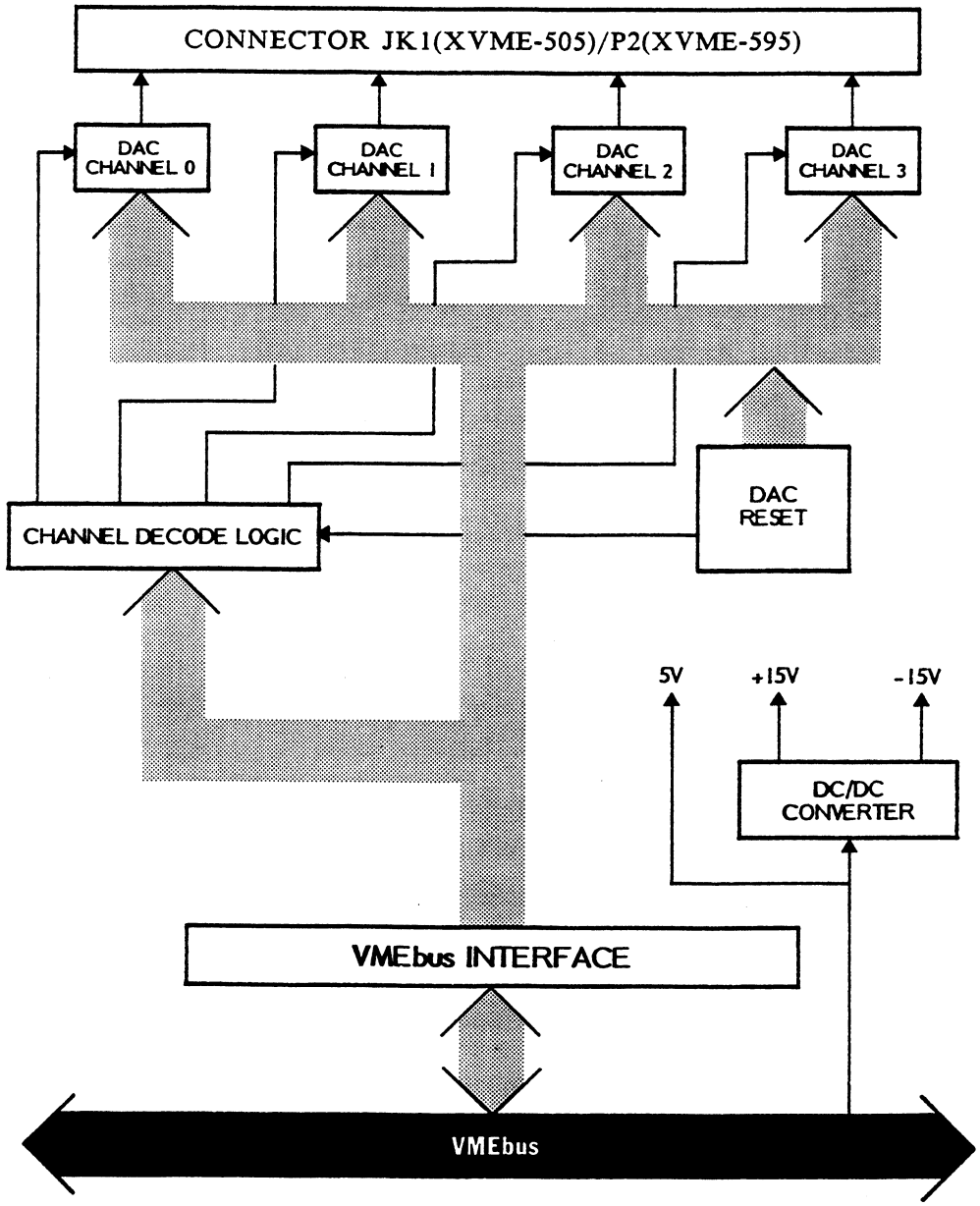


Figure 1-1. XVME-505/595 Operational Block Diagram

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1.3.1 Application Circuitry

As Figure l-1 shows, the digital to analog conversion circuitry consists of the following parts:

- VMEbus interface circuitry.
- 4 D/A converters which perform with 12-bit resolution.
- Channel decode circuitry which selects the converters based on the address offset received by the module.
- A converter reset circuit which causes the D/A converters on all four channels to be loaded with either all logic l's or all logic O's at system power-up or reset (this is a jumper-selectable user option).

1.3.2 General Operation

The Analog Output Modules are designed to be addressed within the VMEbus defined 64K Short I/O Address Space. The module base address is jumper selectable to any of the 64 - 1K boundaries within the Short I/O Address Space. When the module is installed it will occupy a 1K block of the Short I/O Address Space. There are 4 16-bit digital to analog conversion registers located at consecutive word addresses within the 1K block occupied by the module. Thus, the address of each D/A conversion register is simply an offset from the module base address.

Data can be transferred to the D/A conversion registers in either the byte word format. If the data is transferred to the conversion registers via the byte format (i.e., one byte at a time), the low order byte is always transferred prior to the high order byte. This is due to the fact that the transfer of the high order byte initiates the conversion process. Of course, this convention has a bearing if data is transferred in the word format.

As was previously mentioned, the Analog Output Modules are available in two versions (XVME-505/595-l and XVME-505/595-2). Both versions are able to provide voltage outputs, while the XVME-505/595-2 has the additional capability of providing current outputs. The voltage outputs can be configured in either unipolar or bipolar format over the specified ranges (see Table l-l), and the conversion circuitry is able to deal with digital encoded in straight binary, offset binary, and two's compliment. The current output feature on the XVME-505/595-2 provides outputs in the range 4 - 20mA, and because the 4 channels are individually configurable (for either voltage or current output), the XVME-505/595 is capable of a variety of output combinations.

1.4 SPECIFICATIONS

Table 1-1 lists the XVME-505/595 Module Specifications in detail.

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Table l-1. XVME-505/595 Analog Output Module Specifications

Characteristic	Specification
Number of Channels	4
Supply Voltage	+5VDC ±5%
Supply Current	
XVME-505/595-l	1.6A maximum
XVME-505/595-2	1.9A maximum
Accuracy	
Resolution	12 bits
Overall Error	± 1/2 LSB
Differential Linearity	± 1 LSB
Voltage Output Characteristics	
Ranges	0-5V, 0-l0V, ±2.5V, +5V, +10V
Output Current	5mA minimum @ ±10V
Settling Time	7uS
Offset T.C.	75ppm/°C
Gain T.C.	100ppm/°C
Current Loop Characteristics	
Range	4-20mA, Non-isolated
Compliance Voltage	10V @ 20mA
Loop Supply Voltage	+15v to +30v
Settling Time	5ous
Load Resistance Range	50 - 500 Ohms
Offset T.C.	75ppm/°C
Gain I.C.	100ppm/°C
Digital Input Coding	Binary, Offset Binary, or Two's Complement
Temperature	
Operating	0 to 65°C (32 to 149°F)
Non-operating	-40 to 85°C (-40 to 185°F)
Humidity	5 to 95% RH non-condensing (Extremely low humidity may require protection against static discharge.)
Altitude	
Operating	Sea-level to 10,000 ft. (3048m)
Non-operating	Sea-level to 50,000 ft. (15240m)

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Table l-l. Analog Output Module Specifications (Cont'd)

Characteristic	Specification
Vibration	
Operating	5 to 2000Hz .015 in. peak-to-peak 2.5g maximum
Non-operating	5 to 2000Hz .030 in. peak-to-peak 5.0g maximum
Shock	
Operating	30 g peak acceleration 11 mSec duration
Non-operating	50 g peak acceleration 11 mSec duration
VMEbus Compliance	
• Complies with VMEbus Specification Revision C.l • A 16:D 16/D08(E0) DTB Slave • Form Factor (XVME-505) - SINGLE • Form Factor (XVME-595) - DOUBLE	

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Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter explains how to configure the XVME-505/595 Analog Output Module prior to installation in a VMEbus backplane. Included in this chapter is information on module base address selection jumpers, module interrupt level selection jumpers, connector pinouts, and a brief outline of the physical installation procedure.

2.2 SYSTEM REQUIREMENTS

The XVME-505/595 Modules are VMEbus compatible modules. To operate, they must be properly installed in a VMEbus backplane.

The minimum system requirements for the operation of an XVME-505/595 Modules are one of the following:

A) A host processor module properly installed on the same backplane as the XVME-505/595; and a controller subsystem module which employs a Data Transfer Bus Arbiter, a System Clock driver, a System Reset driver, and a Bus timeout module. (The XYCOM XVME-010 System Resource Module provides a controller subsystem with the components listed.)

-- OR --

B) A host processor module which incorporates ,an on-board controller sub-system (such as XYCOM's XVME-600 or XVME-601).

2.3 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers, calibration potentiometers, and connectors on the XVME-505 Analog Output Module are illustrated in Figure 2-1. The jumpers, calibration potentiometers, and connectors on the XVME-595 Analog Output Module are illustrated in Figure 2-2.

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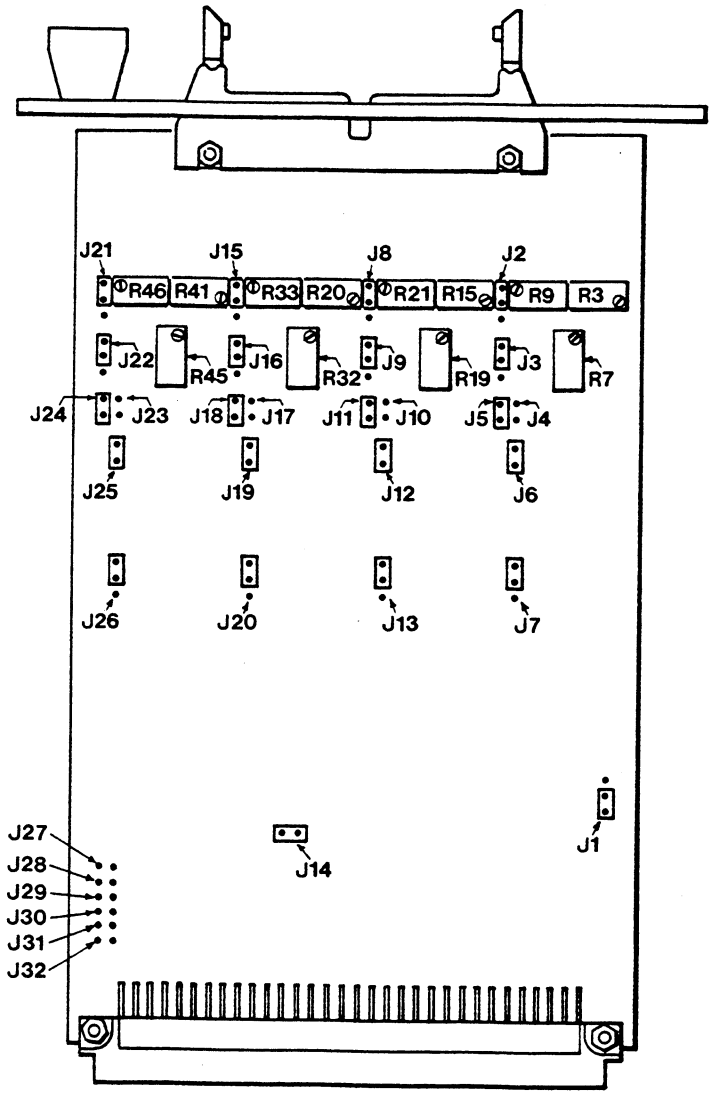


Figure 2-1. Location of Relevant Components (XVME-505)

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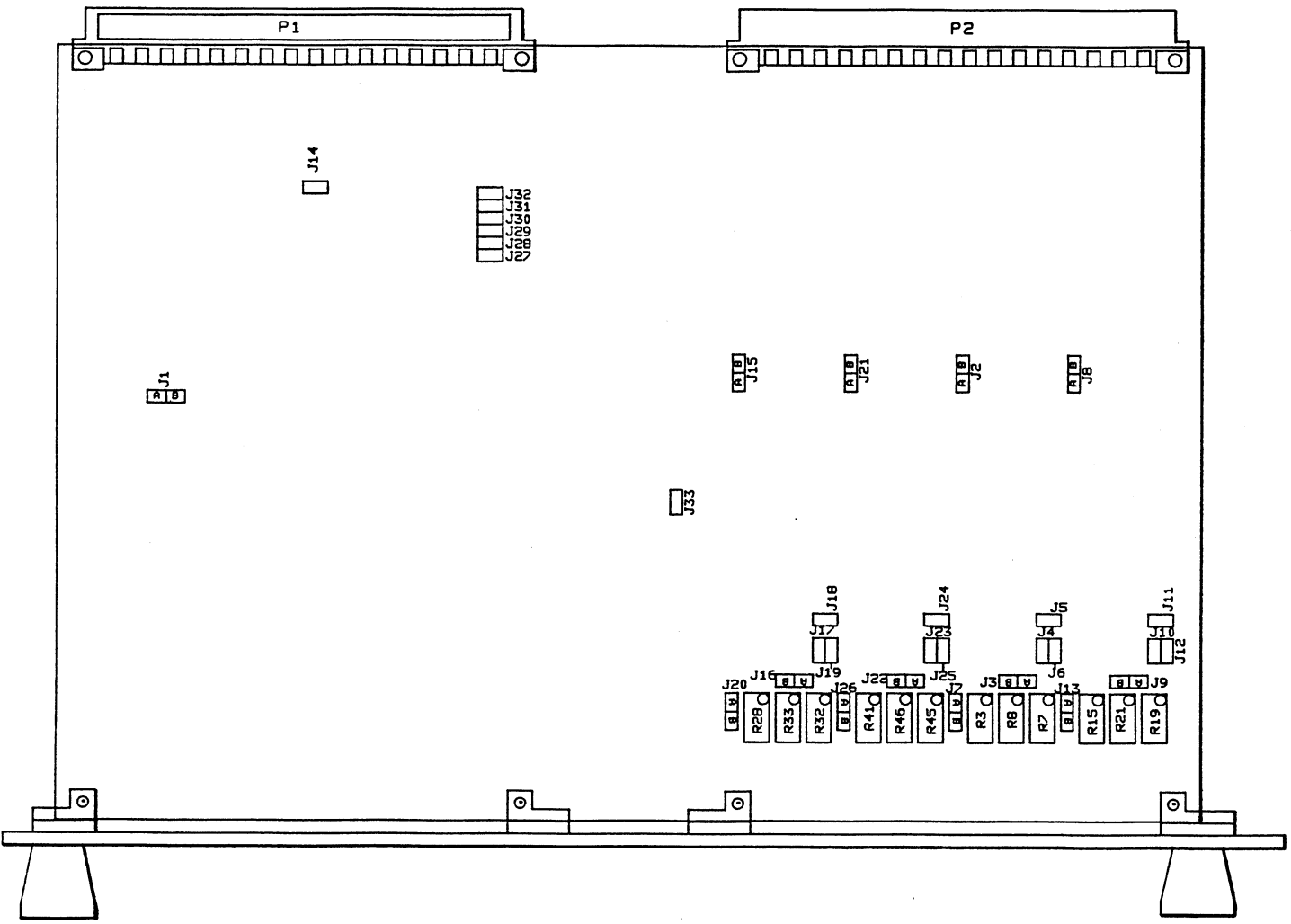


Figure 2-2. Location of Relevant Components (XVME-595)

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2.4 JUMPERS

Prior to installing the Analog Output Module, it will be necessary to configure several jumper options. The configuration of the jumpers is dependent upon which of the module operational capabilities are required for a given application. The jumper options can be divided into two' catagories: VMEbus-related options, and digital to analog conversion options.

VMEbus Options

Jumper	Use
J27-J32	Module base address select jumpers (refer to Section 2.5.1).
J14	This jumper determines whether the module will respond to only supervisory accesses or to both supervisory and non-privileged accesses (refer to Section 2.5.2).

Digital to Analog Conversion Options

Jumper	Use
Jl	This jumper will automatically load the D/A converters on all channels with either all logic "l's" or all logic "O's" during system reset or power-up (refer to Section 2.6.1).
J7, J13, J20, J26	These jumpers provide the option to individually configure each output channel to convert either straight binary to analog, or to convert two's complement binary to analog (refer to Section 2.6.2).
J2, J15, J8, J21	On the these jumpers configure the four output channels to convert data to either an analog voltage format or an analog current format (refer to Section 2.6.3).
J16-J17, J22-J25, J8, J4, J5, J6, J9-J12	These groups of jumpers select one of five output voltage ranges for each output channel. Four of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar offset or for the adjustment of bipolar offset voltage.
J33	(XVME-595 Only.) Connects analog to digital ground. This jumper is installed will foil and may be removed by the user to separate the grounds.

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2.5 VMEbus OPTIONS

2.5.1 Base Address Selection Jumpers (J27-J32)

The XVME-505/595 Analog Output Module is designed to be addressed within the VMEbus Short I/O Memory Space. Since each module connected to the bus must have its own unique address, the base addressing scheme for XVME I/O modules has been designed to be jumper selectable. When the XVME-505/595 Analog Output Module is installed in the system, it will occupy a 1K byte block of Short I/O Memory Space.

The base address decoding scheme for XYCOM I/O modules is such that the starting address for a module will always reside on a 1K boundary. Thus, the module base address may be set to any of one of 64 possible 1K boundaries within the Short I/O Address Space.

The module base address is selected by using the jumpers labeled J27-J32 (see Figure 2-1 (XVME-505) for the location on the board, or Figure 2-2 (XVME-595) for the location on the board). Figure 2-3 shows the base address jumpers, and how each jumper relates to the address lines.

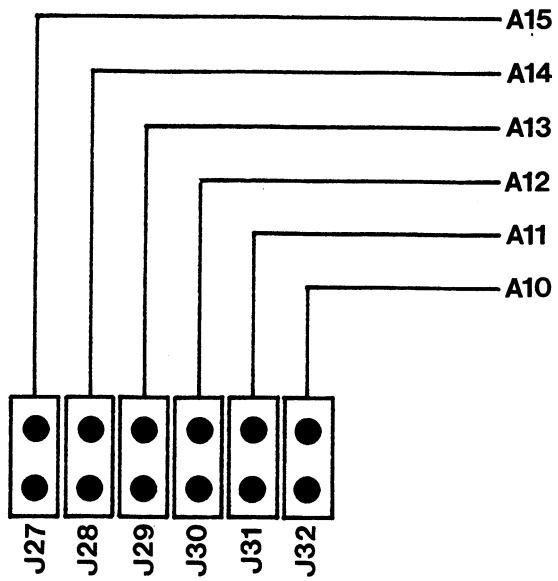


Figure 2-3. Base Address Jumpers

When a jumper is installed, the corresponding base address bit will be logic "0". When a jumper is removed, the corresponding base address bit will be logic "1".

Table 2-1 shows a list of the 64 1K boundaries which can be used as module base addresses in the Short I/O Address Space, as well as the corresponding jumper settings for each address.

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Table 2-1. Base Address Options

J27	J28	J29	J30	J31	J32	Base Address of Module
In	In	In	In	In	In	0000H
In	In	In	In	In	Out	0400H
In	In	In	In	Out	In	0800H
In	In	In	In	Out	Out	0C00H
In	In	In	Out	In	In	1000H
In	In	In	Out	In	Out	1400H
In	In	In	Out	Out	In	1800H
In	In	In	Out	Out	Out	1C00H
In	In	Out	In	In	In	2000H
In	In	Out	In	In	Out	2400H
In	In	Out	In	Out	In	2800H
In	In	Out	In	Out	Out	2C00H
In	In	Out	Out	In	In	3000H
In	In	Out	Out	In	Out	3400H
In	In	Out	Out	Out	In	3800H
In	In	Out	Out	Out	Out	3C00H
In	Out	In	In	In	In	4000H
In	Out	In	In	In	Out	4400H
In	Out	In	In	Out	In	4800H
In	Out	In	In	Out	Out	4C00H
In	Out	In	Out	In	In	5000H
In	Out	In	Out	In	Out	5400H
In	Out	In	Out	Out	In	5800H
In	Out	In	Out	Out	Out	5C00H
In	Out	Out	In	In	In	6000H
In	Out	Out	In	In	Out	6400H
In	Out	Out	In	Out	In	6800H
In	Out	Out	In	Out	Out	6C00H
In	Out	Out	Out	In	In	7000H
In	Out	Out	Out	In	Out	7400H
In	Out	Out	Out	Out	In	7800H
In	Out	Out	Out	Out	Out	7C00H
Out	In	In	In	In	In	8000H
Out	In	In	In	In	Out	8400H
Out	In	In	In	Out	In	8800H
Out	In	In	In	Out	Out	8C00H
Out	In	In	Out	In	In	9000H
Out	In	In	Out	In	Out	9400H
Out	In	In	Out	Out	In	9800H
Out	In	In	Out	Out	Out	9C00H
Out	In	Out	In	In	In	A000H
Out	In	Out	In	In	Out	A400H
Out	In	Out	In	Out	In	A800H
Out	In	Out	In	Out	Out	AC00H
Out	In	Out	Out	In	In	B000H
Out	In	Out	Out	In	Out	B400H
Out	In	Out	Out	Out	In	B800H
Out	In	Out	Out	Out	Out	BC00H
Out	Out	In	In	In	In	C000H
Out	Out	In	In	In	Out	C400H
Out	Out	In	In	Out	In	C800H
Out	Out	In	In	Out	Out	CC00H
Out	Out	In	Out	In	In	D000H
Out	Out	In	Out	In	Out	D400H
Out	Out	In	Out	Out	In	D800H
Out	Out	In	Out	Out	Out	DC00H
Out	Out	Out	In	In	In	E000H
Out	Out	Out	In	In	Out	E400H
Out	Out	Out	In	Out	In	E800H
Out	Out	Out	In	Out	Out	EC00H
Out	Out	Out	Out	In	In	F000H
Out	Out	Out	Out	In	Out	F400H
Out	Out	Out	Out	Out	In	F800H
Out	Out	Out	Out	Out	Out	FC00H

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2.5.2 Supervisor/Non-Privileged Mode Selection (J14)

The XVME-505/595 Analog Output Module can be configured to respond to only Supervisory accesses, or to both Non-privileged and Supervisory accesses by installing or removing jumper 514. Table 2-2 shows the access options controlled by jumper J14.

Table 2-2. Access Options

Jumper J14	Access Mode Selection	Address Modifier Code
Installed	Supervisory Only	2DH
Removed	Supervisory or Non-Privileged	2DH or 29H

2.6 DIGITAL TO ANALOG CONVERSION OPTIONS

2.6.1 Analog Output Reset Jumper (Jl)

Depending on how jumper Jl is configured, the four digital to analog converters will be loaded with either logic '1s" or logic 'Os" at reset or power-up. The two configuration possibilities are:

Jumper	Digital State Converted to Analog on All Outputs
JlA	Logic 1
JIB	Logic 0

This option allows the user to configure a "predetermined" output state on all outputs at reset or power-up. In most applications this jumper would be configured (to JlB) so that the outputs would all be at 0 volts (or at 4mA for a current loop application on the XVME-505/595-2) at reset or power-up. However, depending on the mode of the output range selected (i.e., unipolar or bipolar) and the output conversion format selected (i.e., straight binary, offset binary, or two's complement), this jumper can also be used to "force' the outputs to the full scale limit for the range and format chosen.

Table 2-3 shows the output state corresponding to each of the two jumper settings for both types of voltage output ranges and for all three data conversion formats.

Table 2-3. Reset/Power-up Output States

Jumper Setting	Output States		
	Bipolar		Unipolar
	Offset Binary	Two's Comp.	Straight Binary
JlA	+FSR	0 - 1 LSB	+FSR (20mA)
JlB	-FSR	0 v	OV (4mA)

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NOTE

FSR = Full Scale Range, and LSB = Least Significant Bit These terms are defined in more detail in Section 3.3.1.

2.6.2 Output Conversion Format Jumpers (J20, J26, J7, J13)

This jumper option provides a means of configuring the D/A conversion circuitry to handle digital data in either the straight/offset binary formats, or in the two's complement binary format. The use of this option is entirely dependent up the data format which is provided by the output control program being employed by the user. Each of the four output channels can be configured independently as shown in Table 2-4.

Table 2-4. Output Conversion Format Jumpers

output Channel	Digital Data Conversion Formats	
	Straight/Off set Binary	Twos' Complement
0	J20A	J20B
1	J26A	J26B
2	J7A	J7B
3	J13A	J13B

2.6.3 Voltage/Current Output Selection Jumpers (J15, J21, J2, J8)

In the case of the XVME-505/595-2, each of the four analog output channels is capable of providing an output which can be used as either a voltage applied source or a current applied source (refer to Section 1.1 of Chapter 1 for information on the difference between the XVME-505/595-l and the XVME-505/595-2). Prior to configuring any other channel specific criteria, it should be determined whether the output will be used as an analog voltage source or as an analog current source. Table 2-5 show which jumpers configure the channels as current outputs, and which jumpers configure the channels as voltage outputs.

Table 2-5. Voltage/Current Output Selection Jumpers (XVME-505/595-2 Option Only)

Output Channel	Output	
	Voltage	Current
0	J15A	J15B
1	J21A	J21B
2	J2A	J2B
3	J8A	J8B

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When a channel is to be configured for voltage output, a corresponding voltage range must be selected and jumpered (refer to Section 2.6.4). Depending on whether the voltage range selected is unipolar or bipolar, a channel specific potentiometer is jumper selected (refer to Section 2.6.4) and voltage offset calibration can be performed (refer to Chapter 4 for calibration information).

On the XVME-505/595-2, when the channel is configured for current output, the voltage range selection jumpers which correspond to that particular channel must be configured for the 0-I0V range (see the note in Section 2.6.4). The specified current loop range for each output channel is 4-20mA.

2.6.4 Output Voltage Range Selection Jumpers (J16-J19, J22-J25, J3-J6, J9-J12)

All four output channels can be jumper-configured to provide analog output voltages in any one of five voltage ranges. There are three bipolar output voltage ranges and two unipolar output voltage ranges. The bipolar ranges are:

±2.5V
±5V
±10V

The unipolar ranges are:

0 to +5v
0 to +l0V

Each output channel has its own group of three jumpers which determine which of the five output voltage ranges will apply to that channel. In addition, each output channel has a corresponding jumper which activates an offset voltage calibration potentiometer, and thus, allows offset adjustment for either bipolar or unipolar operation. Table 2-6 shows the various jumper combinations used to configure the output channels for the specific voltage ranges. Note that the last jumper in each group (i.e., J16, J22, J3, J9) is the jumper which activates the offset voltage calibration potentiometer for either unipolar or bipolar adjustment on each channel (refer to Chapter 4 for the calibration procedure).

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Table 2-6. Output Voltage Range Configurations

Channel	Jumper	Output Voltage Ranges				
		±2.5V	±5V	±10V	0-5V	0-10V
0	J19	OUT	IN	IN	OUT	IN
0	J18	IN	IN	OUT	IN	IN
0	J17	IN	OUT	OUT	IN	OUT
0	J16	B	B	B	A	A
1	J25	OUT	IN	IN	OUT	IN
1	J24	IN	IN	OUT	IN	IN
1	J23	IN	OUT	OUT	IN	OUT
1	J22	B	B	B	A	A
2	J6	OUT	IN	IN	OUT	IN
2	J5	IN	IN	OUT	IN	IN
2	J4	IN	OUT	OUT	IN	OUT
2	J3	B	B	B	A	A
3	J12	OUT	IN	IN	OUT	IN
3	Jll	IN	IN	OUT	IN	IN
3	Jl0	IN	OUT	OUT	IN	OUT
3	J9	B	B	B	A	A

NOTE

On the XVME-505/595-2, when using a channel in the current output mode (refer to Section 2.6.3), the voltage- output jumpers for that channel must be configured for the 0-I0V range.

Before the XVME-505/595 Analog Output Module is shipped from the factory, they are configured and calibrated for the following output ranges:

XVME-505/595-l - Unipolar 0-10V Voltage Output
XVME-505/595-2 - Unipolar 4-20mA Current Output

2.7 EXTERNAL CONNECTOR JKl (XVME-505 Only)

The analog output channels are accessible on the front panel of the module in the form of a single mass termination header (labeled JKl). Connector JKl is a 34-pin header with pins l-26 devoted to voltage output, and pins 27-34 devoted to current outputs (XVME-505/595-2 Option Only). Jumper J33 connects analog to digital ground and is installed with foil which may be removed by the user to separate the grounds. Figure 2-4 shows the module (XVME-505) front panel and how the pins are situated in the connector.

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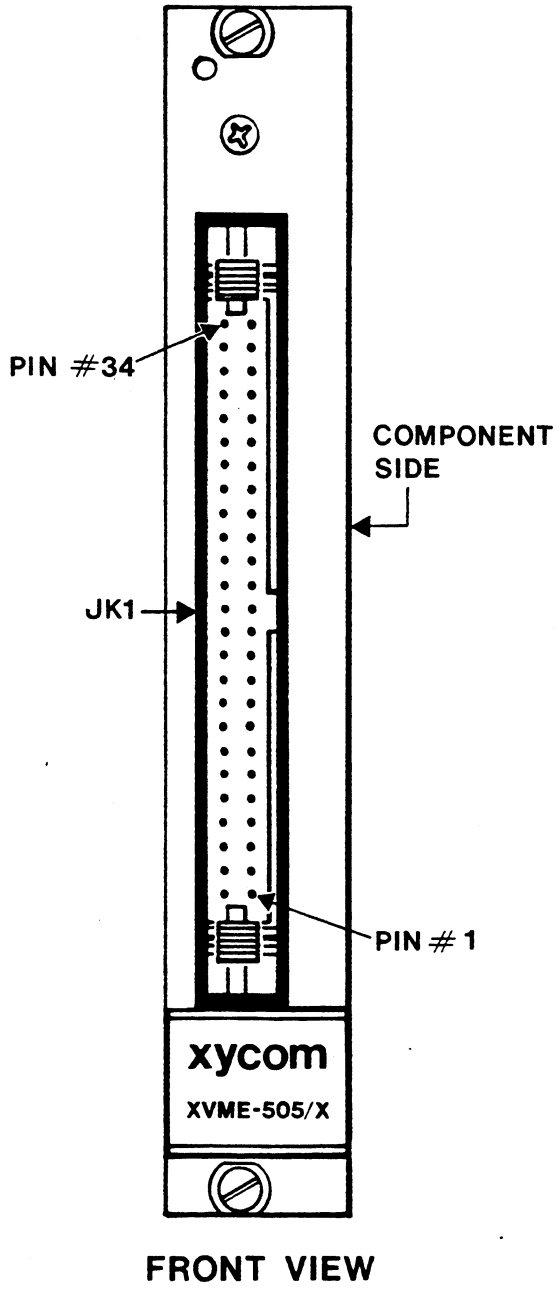


Figure 2-4. Connector JK1

NOTE

Pins 1 through 26 of connector JK1 are fully compatible with Analog Devices 3B Series Universal Signal Conditioning System.

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Table 2-7 shows the pin designations for connector JKl.

Table 2-7. Output Connector JKl

Pin	Pin Description	
1	Channel 0 Vout	
2	NC	
3	Analog Ground	
4	NC	
5	Channel 1 Vout	
6	Analog Ground	
7	Channel 2 Vout	
8	NC	
9	Analog Ground	
10	NC	
11	Channel 3 Vout	
12	Analog Ground	
13	NC	
14	NC	
15	Analog Ground	
16	NC	
17	NC	
18	Analog Ground	
19	NC	
20	NC	
21	Analog Ground	
22	NC	
23	NC	
24	Analog Ground	
25	NC	
26	NC	
27	Channel 0 Iout+	XVME-505/595-2 Option Only
28	Iout-	
29	Iout-	
30	Channel 1 Iout+	
31	Channel 2 Iout+	
32	Iout-	
33	Iout-	
34	Channel 3 Iout+	

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2.8 EXTERNAL CONNECTORS Pl and P2

2.8.1 Pl Connector

Connector Pl is mounted at the rear edge of the board (see Figure 2-2). The pin connections for Pl (a 96-pin, 3-row connector) contains the standard address, data, and control signals necessary for the operation of VMEbus-defined NEXP modules. (The signal definitions and pin-outs for the connector are found in Appendix A of this manual.) The Pl connector is designed to mechanically interface with a VMEbus defined Pl backplane.

2.8.2 P2 Connector (XVME-595 Only)

The P2 connector is mounted on the rear edge of the XVME-595 module and is a 96-pin, 3 row connector. Only 34 pins are used, pins 1-13 (rows A and C) are devoted to voltage output, and pins 14-17 (rows A and C) are devoted to current outputs (XVME-505/595-2 Option Only). This connector functionally the same as the JKl, only the signals are routed out the back of the module. Row B is used as power and ground as per VMEbus specifications. Table 2-8 shows the pin designations for the P2 connector.

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Table 2-8. Pin Assignment for P2 (XVME-595 Only)

ROW A		ROW B		ROW C		
Pin #	Signal	Pin #	Signal	Pin #	Signal	
P2A-1	NO CONNECT	P2B-1	+5V	P2C-1	Channel 0 Vout	
P2A-2	NO CONNECT	P2B2	GND	P2C-2	Analog Ground	
P2A-3	Analog Ground	NO CONNECT		P2C-3	Channel 1 Vout	
P2A-4	NO CONNECT	NO CONNECT		P2C-4	Channel 2 Vout	
P2A-5	NO CONNECT	NO CONNECT		P2C-5	Analog Ground	
P2A-6	NO CONNECT	NO CONNECT		P2C-6	Channel 3 Vout	
P2A-7	NO CONNECT	NO CONNECT		P2C-7	NO CONNECT	
P2A-8	NO CONNECT	NO CONNECT		P2C-8	NO CONNECT	
P2A-9	Analog Ground	NO CONNECT		P2C-9	NO CONNECT	
P2A-10	NO CONNECT	NO CONNECT		P2C-10	NO CONNECT	
P2A-11	NO CONNECT	NO CONNECT		P2C-11	Analog Ground	
P2A-12	Analog Ground	P2B-12	GND	P2C-12	NO CONNECT	
P2A-13	NO CONNECT	P2B-13	+5V	P2C-13	NO CONNECT	
P2A-14	Iout-	NO CONNECT		P2C-14	Channel 0 Iout+	(505/595-2) Option Only
P2A-15	Channel 1 Iout+	NO CONNECT		P2C-15	Iout-	
P2A-16	Iout-	NO CONNECT		P2C-16	Channel 2 Iout+	
P2A-17	Channel 3 Iout+	NO CONNECT		P2C-17	Iout-	
P2A-18	NO CONNECT	NO CONNECT		P2C-18	NO CONNECT	
P2A-19	NO CONNECT	NO CONNECT		P2C-19	NO CONNECT	
P2A-20	NO CONNECT	NO CONNECT		P2C-20	NO CONNECT	
P2A-21	NO CONNECT	NO CONNECT		P2C-21	NO CONNECT	
P2A-22	NO CONNECT	P2B-22	GND	P2C-22	NO CONNECT	
P2A-23	NO CONNECT	NO CONNECT		P2C-23	NO CONNECT	
P2A-24	NO CONNECT	NO CONNECT		P2C-24	NO CONNECT	
P2A-25	NO CONNECT	NO CONNECT		P2C-25	NO CONNECT	
P2A-26	NO CONNECT	NO CONNECT		P2C-26	NO CONNECT	
P2A-27	NO CONNECT	NO CONNECT		P2C-27	NO CONNECT	
P2A-28	NO CONNECT	NO CONNECT		P2C-28	NO CONNECT	
P2A-29	NO CONNECT	NO CONNECT		P2C-29	NO CONNECT	
P2A-30	NO CONNECT	NO CONNECT		P2C-30	NO CONNECT	
P2A-31	NO CONNECT	P2B-31	GND	P2C-31	NO CONNECT	
P2A-32	NO CONNECT	P2B-32	+5V	P2C-32	NO CONNECT	

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2.9 MODULE INSTALLATION

XYCOM XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-505 Analog Output Module is a single-high VMEbus module, and as such, only requires the Pl backplane. The XVME-595 Analog Output Module is a Double-high VMEbus module, it also requires the PI backplane and can use the P2 backplane.

CAUTION

Never attempt to install or remove any boards before turning off the . power to the bus, and all related external power supplies.

Prior to installing a module, you should determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. (Please check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2) Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage (XVME-505 Only).

3) Push the card slowly toward the rear of the chassis until the connectors engage (the card should slide freely in the plastic guides).

4) Apply straight-forward pressure to the handles located on the front panel of the module until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excessive pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, it should be secured to the chassis by tightening the two machine screws at the extreme top and bottom of the board.

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2.9.1 Installing a 6U Front Panel Kit

XYCOM Model Number XVME-942 is an optional 6U (if you have purchased the XVME-595 Module it is already a 6U board, therefore you may skip this section) front panel kit designed to replace the existing 3U front panel on the XVME-505. The 6U front panel facilitates the secure installation of single-high modules in those chassis which are designed to accommodate only double-high modules. The following step-by-step procedure for installing the 6U front panel on an XVME-505 Module (refer to Figure 2-5 for a graphic depiction of the installation procedure).

1) Disconnect the module from the bus.

2) Remove the screw and plastic collar assemblies (labeled #6 and #7) from the extreme top and bottom of the existing 3U front panel (#11), and install the screw assemblies in their corresponding locations on the 6U front panel.

3) Slide the module identification plate (labeled #13) from the handle (#9) on the 3U front panel. By removing the screw/nut found inside the handle, the entire handle assembly will separate from the 3U front panel. Remove the counter-sunk screw labeled #8 to separate the 3U front panel from the printed circuit board (#12).

4) Line-up the plastic support brackets on the printed circuit board with the corresponding holes in the 6U front panel (i.e., the holes at the top and top-center of the panel). Install the counter-sunk screw (#8) in the hole near the top-center of the 6U panel, securing it to the lower support bracket on the printed circuit board.

5) Install the handle assembly (which was taken from the 3U panel) at the top of the 6U panel, using the screw and nut previously attached inside the handle. After securing the top handle, slide the module identification plate in place.

6) Finally, install the bottom handle (i.e., the handle that accompanies the kit - labeled #2) using the screw and nut (#3 and #5) provided. Slide the XYCOM VMEbus I.D. plate (#4) in place on the bottom handle.

The module is now ready to be re-installed in the backplane.

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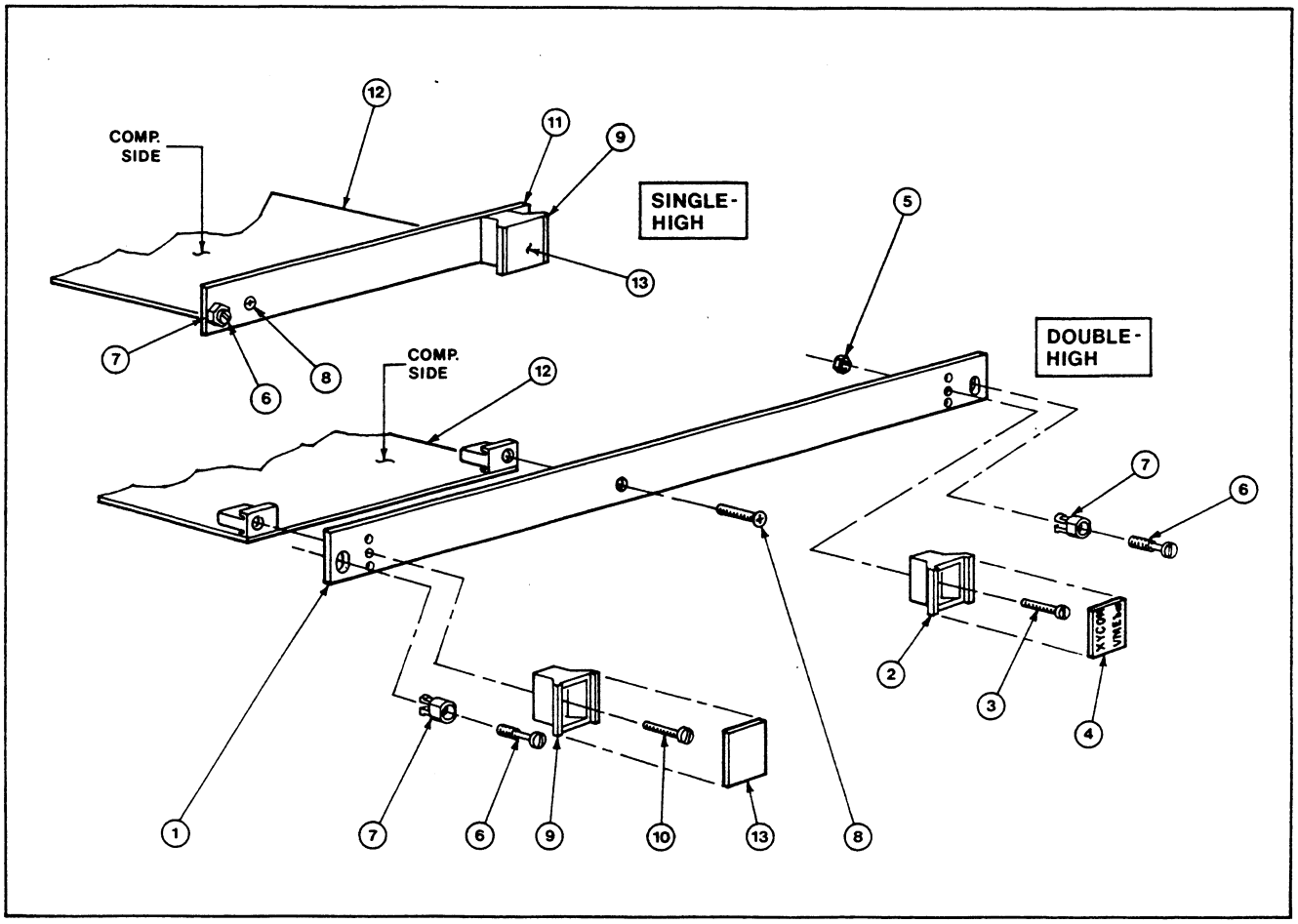


Figure 2-5. Installing the 6U Front Panel Kit (XVME-505 Only)

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Chapter 3

PROGRAMMING

3.1 INTRODUCTION

This chapter provides the information required to program the XVME-505/595 Analog Output Module for digital to analog signal conversions. The programming information is presented in the following fashion:

- A discussion of base addressing and how the conversion registers are accessed. .
- D/A conversion principles.

3.2 BASE ADDRESSING

The XVME-505/595 Analog Output Module is designed to be addressed within the VMEbus-defined 64K Short I/O Address Space. When the module is installed in a system, it will occupy a 1K byte block of the Short I/O Address Space. The base address decoding scheme for the XVME I/O modules is such that the starting address for each board resides on a IK boundary. Thus, there are 64 possible locations (1K boundaries) in the Short I/O Address Space which could be used as the base address for the XVME-505/595 Analog Output Module (refer to Section 2.5.1 for the list of base addresses and their corresponding list of jumper configurations).

The logical registers utilized for the conversion of data on the XVME-505/595 Analog Output Module are given specific addresses within the 1K block of address space occupied by the module. These addresses are offset from the module base address. Figure 3-1 shows a representative memory map for the Analog Output Module.

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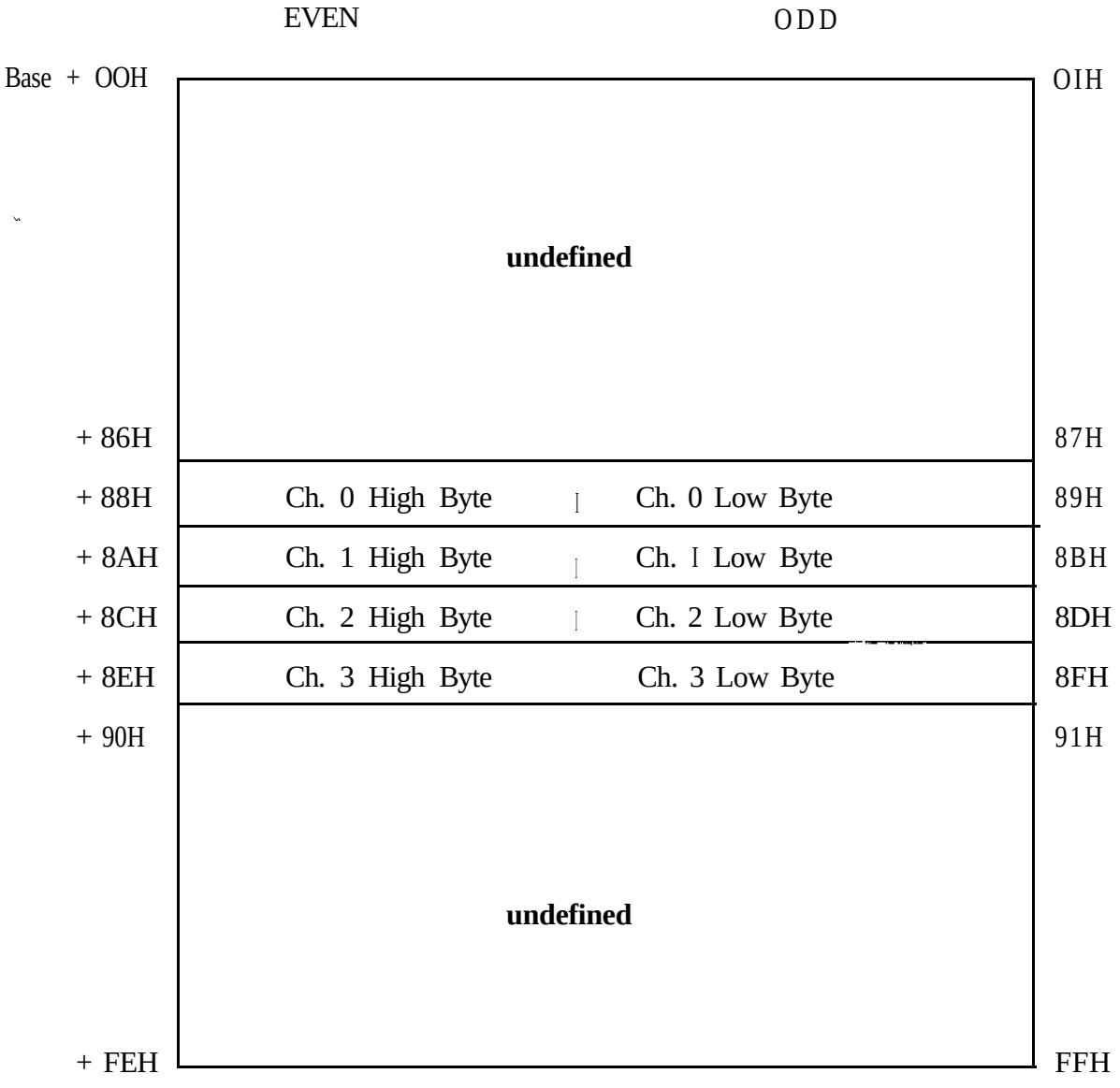


Figure 3-1. Analog Output Module Memory Map

NOTE
The defined locations are Write ONLY. Any attempt to Read data will simply return invalid data.

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A specific conversion register on the module can be accessed by simply adding the specific register offset to the module base address. For example, the channel 0 conversion register is located at offset address 88H, and if the module base address is jumpered to l000H, then data to be converted on channel 0 would be addressed to 1088H (i.e., assuming the data is sent via the word mode).

(Module base address)		(Register off set)		(Actual Address)
1000H	+	88H	=	1088H

For memory-mapped CPU modules (such as 68000 CPU modules), the Short I/O Address Space is memory-mapped to begin at a specific address. For such modules, the register offset is an offset from the start of this memory-mapped Short I/O Address Space. For example, if the Short I/O Address Space of a 68000CPU module starts at F9000H, and if the base address of the XVME-505/595 Analog Output Module is set at l000H, the actual module base address would be F91000H.

3.3 D/A CONVERSION REGISTERS (Base + 88H, SAH, 8CH, and 8EH) (Write Only)

The D/A converters can produce a voltage output (and/or a current output on the XVME-505/2) for any of four available output channels. On the XVME-505/2 the output channels are independently jumper-configured for the type of output required (refer to Section 2.6.3). The value of the analog output will be a fraction of the converters "full scale" output, defined by the digital code sent to the converter.

The data to be converted is sent to one of the four D/A conversion channels by writing to the module base + the offset of the desired channel. Refer to Figure 3-1 to see the relative positions of the four output channel registers within the IK block of Short I/O Address Space occupied by the Analog Output Module.

The digital to analog conversion process begins when data is written to the high order byte of an output channels conversion register. For this reason, either the data should be moved via a word transfer, or if a byte transfer is used, the low order byte will have to be written prior to the high order byte. Whenever a low order byte is written, the last high order byte written to the same channel will be treated as data for the D/D conversion.

3.3.1 Digital Output Data Format

The digital data written to the D/A conversion registers corresponds to the magnitude of the analog output signal in a relation that is different for each of the two digital data formats (i.e., Straight Binary Encoding, or Offset Binary Encoding).

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The analog output signals can be divided into two general groups:

Unipolar Output - where the output has only a positive polarity (e.g., 0-5V or 4-20mA).

and

Bipolar Output - where the output magnitude can have a negative or positive polarity (e.g., ±5V).

NOTE

When an output is used in current mode (on the XVME-505/595-2 version only), it is classified as a unipolar output.

In the unipolar formats, the data to be converted is usually encoded in the Straight Binary form. The following table (Table 3-1) shows the data encoding format for Straight Binary in the Unipolar mode.

Table 3-1. Unipolar Mode
(Straight Binary Encoding)

X= Don't Care Voltage Mode: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	Vfsr - 1 LSB Vfsr/2 0V
Current Mode (XVME-505/595-2 Only): D_{15} D_0	Analog Output 4-20mA
X X X X 1 1 1 1 1 1 1 1 1 1 1 1 X X X X 1 0 0 0 0 0 0 0 0 0 0 0 X X X X 0 0 0 0 0 0 0 0 0 0 0 0	19.996mA (20mA - 1 LSB) 12mA 4mA

In the bipolar mode, the digital value converted to analog is encoded in either Offset Binary or Two's Complement form. In Offset Binary, the negative full scale voltage (-Vmax) is represented by all binary zeros. The positive full scale voltage (minus one LSB) is represented by all binary ones. Thus, the voltage represented is "offset" by a factor of one half of the full scale voltage "swing" (+Vmax to -Vmax).

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In Two's Complement mode, the most significant bit is simply inverted. This provides for direct mapping between the Two's Complement numbers used by the microprocessor and the voltage output of the digital to analog convertor. Table 3-2 shows the offset and two's complement encoding formats.

Table 3-2. Bipolar Modes

X= Don't Care Offset Binary Encoding: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1 LSB
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	Vfsr/2
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	-Vfsr/2
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	-Vfsr
Two's Complement Encoding: **D_{15} D_0**	**Analog Output 4-20mA**
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1 LSB
X X X X 0 1 0 0 0 0 0 0 0 0 0 0	1/2 (+Vfsr)
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	1/2 (-Vfsr)
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	-Vfsr

NOTE

The "LSB" (least Significant Bit) represents the change in output voltage (or current) that is the result of an increase or decrease of the binary code by one count. The "LSB" is derived from the full range (fsr) of either current or voltage divided by the maximum conversion resolution (i.e., 12 bits or 4096 in binary equivalent). Thus, the value of one LSB can be determined by the following:

$$\text{Unipolar LSB} = \frac{\text{Vfsr}}{4096} \qquad \text{Bipolar LSB} = \frac{(+\text{Vfsr}) - (-\text{Vfsr})}{4096}$$

$$\text{Current LSB} = \frac{20\text{mA} - 4\text{mA}}{4096}$$

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The following list shows the value of 1 LSB for each range:

+2.5V	= 1.2207mV
+5V	= 2.4414mV
+10V	= 4.8828mV
0 - 5 v	= 1.2207mV
0 - 10V	= 2.4414mV
4 - 20mA	= 3.906uA

3.4 D/A CONVERSION PRINCIPLES

A general procedure for configuring the XVME-505/595 Analog Output Module to convert digital data to analog outputs must include the following elements:

1) Configure jumpers (refer to Chapter 2) for the output voltage range (unipolar or bipolar), digital data conversion format (straight binary of offset binary), D/A converter reset state at power-up or system reset (i.e., the converters are loaded with either all logic "0's" or all logic "l's" at power-up or reset), and in the case of the XVME-505/595-2 the output type (i.e., voltage or current).

2) Perform Calibration (see Chapter 4).

3) Write the data to be converted to the desired 16 bit D/A output register in the byte or word mode. If the data is transferred to the register in the byte mode, the high order byte must be written prior to the low order byte.

   When the low order byte is written, the D/A conversion is initiated and the output will change state.

Thus, initiating a conversion on the output channels is simply a matter of writing the binary conversion data to the module base address + (word locations) 88H, 8AH, 8CH, and 8EH.

3.4.1 Current Loop Outputs on the XVME-505/595-2

When the outputs on the XVME-505/595-2 are configured for current loop operation (see Section 2.6.3), the loop supply voltage is provided by an on-board 15V DC-DC converter circuit. This converter not only generates +15V from the VMEbus supplied +5V, but it also serves to separate analog ground-from the digital ground. In addition, the module has its own precision voltage source to provide an internal reference voltage. The D/A outputs are capable of handling current loop configurations in the 4-20mA range with a loop resistance range of 50-500 ohms.

When used in the current output mode, the output channels on the XVME-505/595-2 must be jumpered for the 0-10V output range.

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Chapter 4

CALIBRATION

4.1 INTRODUCTION

Calibration facilities have been provided on the XVME-505/595 Analog Output Module for the analog output circuits. The module is calibrated in the O-10V (4 to 20mA range on the XVME-505/595-2) voltage output range prior to leaving the factory, however, it is recommended that if the module is configured to operate in ranges other than 0-l0V, the calibration should be checked and adjusted if necessary. As a general rule, the output circuitry should 'be recalibrated whenever the output range jumpers ar changed.

The output calibration procedure entails offset and gain adjustment for each output channel in either the unipolar or the bipolar modes of operation. Table 4-1 provides a list of the potentiometers and their applications for the output circuit calibration. Relative locations of the calibration potentiometers can be found in Figure 2-1.

Table 4-1. D/A Calibration Potentiometers

Potentiometer No.	Type of Adjustment
R15	Gain adjustment for output channel 3
R3	Gain adjustment for output channel 2
R41	Gain adjustment for output channel 1
R28	Gain adjustment for output channel 0
R21	Channel 3 bipolar off set adjustment
R8	Channel 2 bipolar offset adjustment
R46	Channel 1 bipolar offset adjustment
R33	Channel 0 bipolar offset adjustment
RI9	Channel 3 unipolar offset adjustment
R7	Channel 2 unipolar offset adjustment
R45	Channel 1 unipolar offset adjustment
R32	Channel 0 unipolar offset adjustment

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4.2 OUTPUT CALIBRATION

Equipment required:

1) A 5-digit volt meter capable of reading ±30uV

2) A small f lat-bladed screwdriver

Output calibration entails voltage offset adjustment, and gain adjustment for each channel, in both the unipolar and bipolar configurations. For unipolar operation, potentiometers R32, R45, R7, and R19 are adjusted for channels 0 through 3 respectively. Bipolar operation requires that potentiometers R33, R46, R8, and R21 be adjusted for channels 0 through 3 respectively. Potentiometers R28, R41, R3, and R15 are used to adjust channel gain for both the unipolar and bipolar modes.

The following is the calibration procedure for the unipolar output mode:

Unipolar Off set/Gain Ad iustment

1) Set jumpers J16, J22, J8 or J9 to the "A" position, dependent upon which channels are to be offset adjusted.

2) Turn all bits off (load binary zeros) to the channel being calibrated.

3) Make sure that the channels are jumpered for voltage output (J15A, J2lA, J2A, or J8A).

4) Adjust the (unipolar) potentiometer that corresponds with the. channel being calibrated until the output reads 0.0000 volts ±30uV.

5) Turn all bits on (FFFH) to the channel being calibrated.

6) Adjust the corresponding gain potentiometer until the output is 9.9976 volts (i.e., 1 LSB less than the nominal full scale of 10.000 volts).

On the XVME-505/595-2 steps 2, 3, 4, 5, and 6 may also be executed with the channels configured for current output (step three would set the voltage/current jumpers in the "B" current position). In this case, the channel offset potentiometer is adjusted for an output of 4mA (or l.000V ±30uV across a 250 Ohm, .0l% resistor returned to the -1out pin on connector JKl (XVME-505/2) or P2 (XVME-595/2)), and the gain potentiometer should be adjusted for an output of 20mA (or 5.000 volts).

NOTE

Make certain that the resistor used for current mode calibration does not change value due to self-heating.

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The following is the calibration procedure for the bipolar output mode:

Bipolar Offset/Gain Ad iustments

1) Set jumpers J16, J22, J8, or J9 to the "B" position, dependent upon which channel(s) are to be calibrated.

2) Turn all bits off (load binary zeros) to the output channel being calibrated.

3) Ad just the (bipolar) potentiometer that corresponds with the channel being calibrated until the output reads -5.00V ±30uV.

4) Turn all bits on (load FFFH) to the output channel being calibrated.

5) Adjust the gain potentiometer until the output reads +4.9976V.

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Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

Connectors Pl and P2 are mounted at the rear edge of the board (see Figure 2-2). The pin connections for Pl (a 96-pin, 3-row connector) contains the standard address, data, and control signals necessary for the operation of VMEbus-defined NEXP modules. The Pl connector is designed to mechanically interface with a VMEbus defined Pl backplane.

Table A-1. P1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	lA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 lB:16,17, 18,19 lC:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	IA:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A01-A23	1A:24-30 lC:15-30	ADDRESS BUS (bits l-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:l	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	IB:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:ll	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,l0	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BGOOUT*- BG30UT*	1B:5,7, 9,ll	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	lA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSl*	lA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).
DTACK*	lA:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
G N D	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22,31	GROUND

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQl*-IRQ7*	1B:24-30	INTERRUPT REQUEST (l-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	IC:I3	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	lA:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5v	1A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12v	lC:31	+12 VDC POWER: Used by system logic circuits.
-12v	lA:31	-12 VDC POWER: Used by system logic circuits.

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BACKPLANE CONNECTOR Pl

The following table lists the Pl pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DO0	BBSY*	DO8
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	Dl0
4	DO3	BGOIN*	Dll
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG20UT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

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The analog output channels are accessible on the front panel of the module in the form of a single mass termination header (labeled JKl). Connector JKl is a 34-pin header with pins 1-26 devoted to voltage output, and pins 27-34 devoted to current outputs (XVME-505/595-2 Option Only). Figure 2-4 shows the module (XVME-505) front panel and how the pins are situated in the connector.

NOTE

Pins 1 through 26 of connector JKl are fully compatible with Analog Devices 3B Series Universal Signal Conditioning System.

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Table A-3 shows the pin designations for connector **JKl.**

Table A-3. Output Connector JKI

Pin	Pin Description	
1	Channel 0 Vout	
2	NC	
3	Analog Ground	
4	NC	
5	Channel 1 Vout	
6	Analog Ground	
7	Channel 2 Vout	
8	NC	
9	Analog Ground	
10	NC	
11	Channel 3 Vout	
12	Analog Ground	
13	NC	
14	NC	
15	Analog Ground	
16	NC	
17	NC	
18	Analog Ground	
19	NC	
20	NC	
21	Analog Ground	
22	NC	
23	NC	
24	Analog Ground	
25	NC	
26	NC	
27	Channel 0 Iout+	XVME-505/595-2 Option Only
28	Iout-	
29	Iout-	
30	Channel 1 Iout+	
31	Channel 2 Iout+	
32	Iout-	
33	Iout-	
34	Channel 3 Iout+	

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The P2 connector is mounted on the rear edge of the XVME-595 module and is a 96-pin, 3 row connector. Only 34 pins are used, pins 1-13 (rows A and C) are devoted to voltage output, and pins 14-17 (rows A and C) are devoted to current outputs (XVME-505/595-2 Option Only). This connector functionally the same as the JK1, only the signals are routed out the back of the module. Row B is used as power and ground as per VMEbus specifications. Table A-4 shows the pin designations for the P2 connector.

Table A-4. Pin Assignment for P2 (XVME-595 Only)

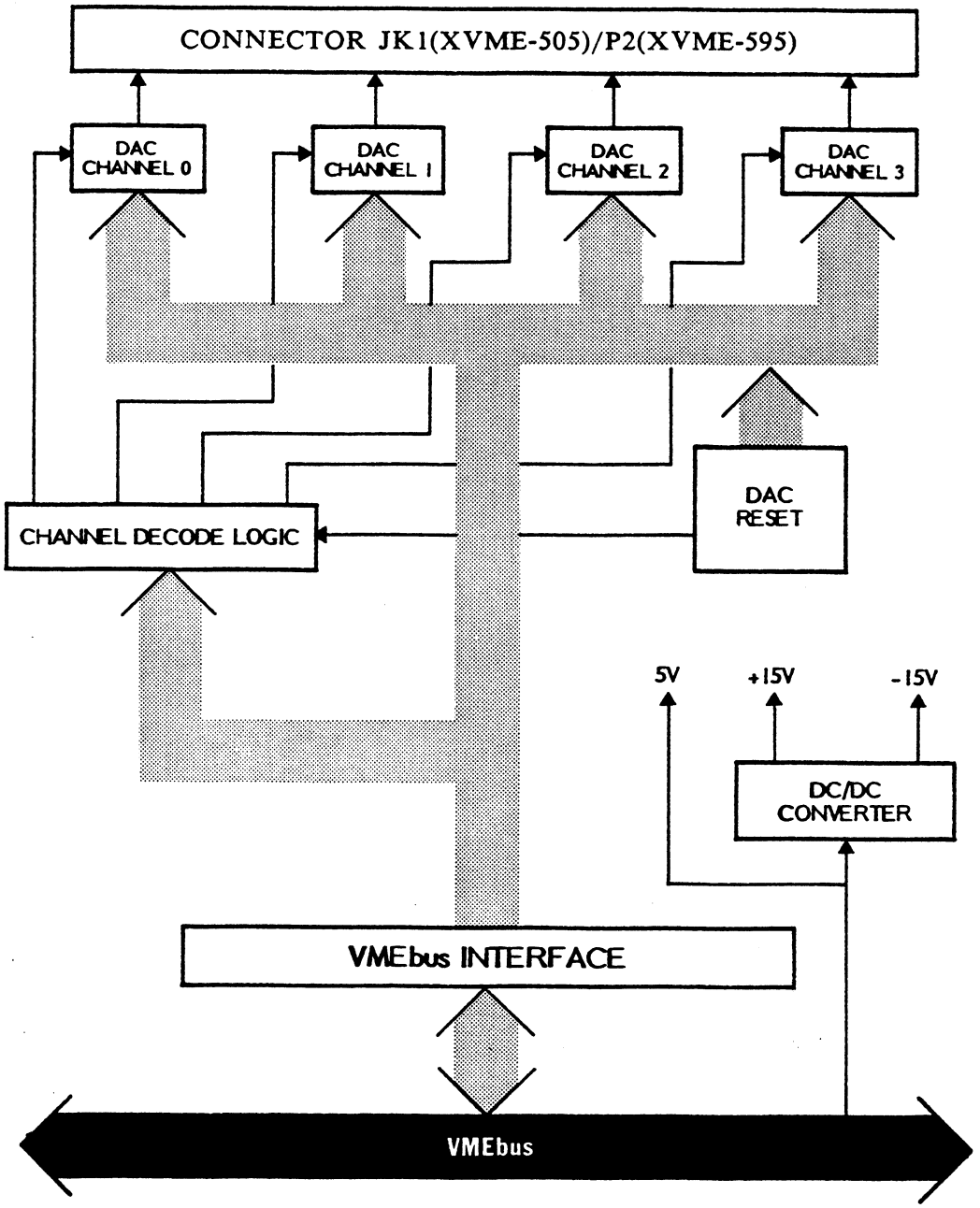
ROW A		ROW B		ROW C		
Pin #	Signal	Pin #	Signal	Pin #	Signal	
P2A-1	NO CONNECT	P2B-1	+5V	P2C-1	Channel 0 Vout	
P2A-2	NO CONNECT	P2B2	GND	P2C-2	Analog Ground	
P2A-3	Analog Ground	NO CONNECT		P2C-3	Channel 1 Vout	
P2A-4	NO CONNECT	NO CONNECT		P2C-4	Channel 2 Vout	
P2A-5	NO CONNECT	NO CONNECT		P2C-5	Analog Ground	
P2A-6	NO CONNECT	NO CONNECT		P2C-6	Channel 3 Vout	
P2A-7	NO CONNECT	NO CONNECT		P2C-7	NO CONNECT	
P2A-8	NO CONNECT	NO CONNECT		P2C-8	NO CONNECT	
P2A-9	Analog Ground	NO CONNECT		P2C-9	NO CONNECT	
P2A-10	NO CONNECT	NO CONNECT		P2C-10	NO CONNECT	
P2A-11	NO CONNECT	NO CONNECT		P2C-11	Analog Ground	
P2A-12	Analog Ground	P2B-12	GND	P2C-12	NO CONNECT	
P2A-13	NO CONNECT	P2B-13	+5V	P2C-13	NO CONNECT	
P2A-14	Iout-	NO CONNECT		P2C-14	Channel 0 Iout+	(505/595-2) Option Only
P2A-15	Channel 1 Iout+	NO CONNECT		P2C-15	Iout-	
P2A-16	Iout-	NO CONNECT		P2C-16	Channel 2 Iout+	
P2A-17	Channel 3 Iout+	NO CONNECT		P2C-17	Iout-	
P2A-18	NO CONNECT	NO CONNECT		P2C-18	NO CONNECT	
P2A-19	NO CONNECT	NO CONNECT		P2C-19	NO CONNECT	
P2A-20	NO CONNECT	NO CONNECT		P2C-20	NO CONNECT	
P2A-21	NO CONNECT	NO CONNECT		P2C-21	NO CONNECT	
P2A-22	NO CONNECT	P2B-22	GND	P2C-22	NO CONNECT	
P2A-23	NO CONNECT	NO CONNECT		P2C-23	NO CONNECT	
P2A-24	NO CONNECT	NO CONNECT		P2C-24	NO CONNECT	
P2A-25	NO CONNECT	NO CONNECT		P2C-25	NO CONNECT	
P2A-26	NO CONNECT	NO CONNECT		P2C-26	NO CONNECT	
P2A-27	NO CONNECT	NO CONNECT		P2C-27	NO CONNECT	
P2A-28	NO CONNECT	NO CONNECT		P2C-28	NO CONNECT	
P2A-29	NO CONNECT	NO CONNECT		P2C-29	NO CONNECT	
P2A-30	NO CONNECT	NO CONNECT		P2C-30	NO CONNECT	
P2A-31	NO CONNECT	P2B-31	GND	P2C-31	NO CONNECT	
P2A-32	NO CONNECT	P2B-32	+5V	P2C-32	NO CONNECT	

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Appendix B

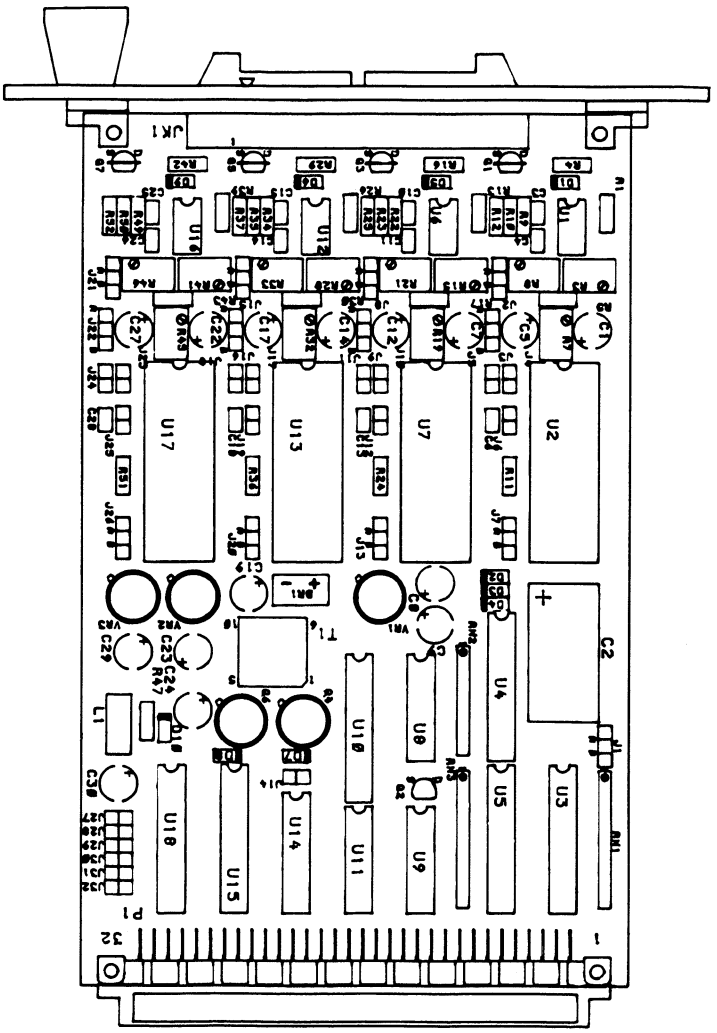
BLOCK DIAGRAM, ASSEMBLY DRAWING, & SCHEMATICS

BLOCK DIAGRAM



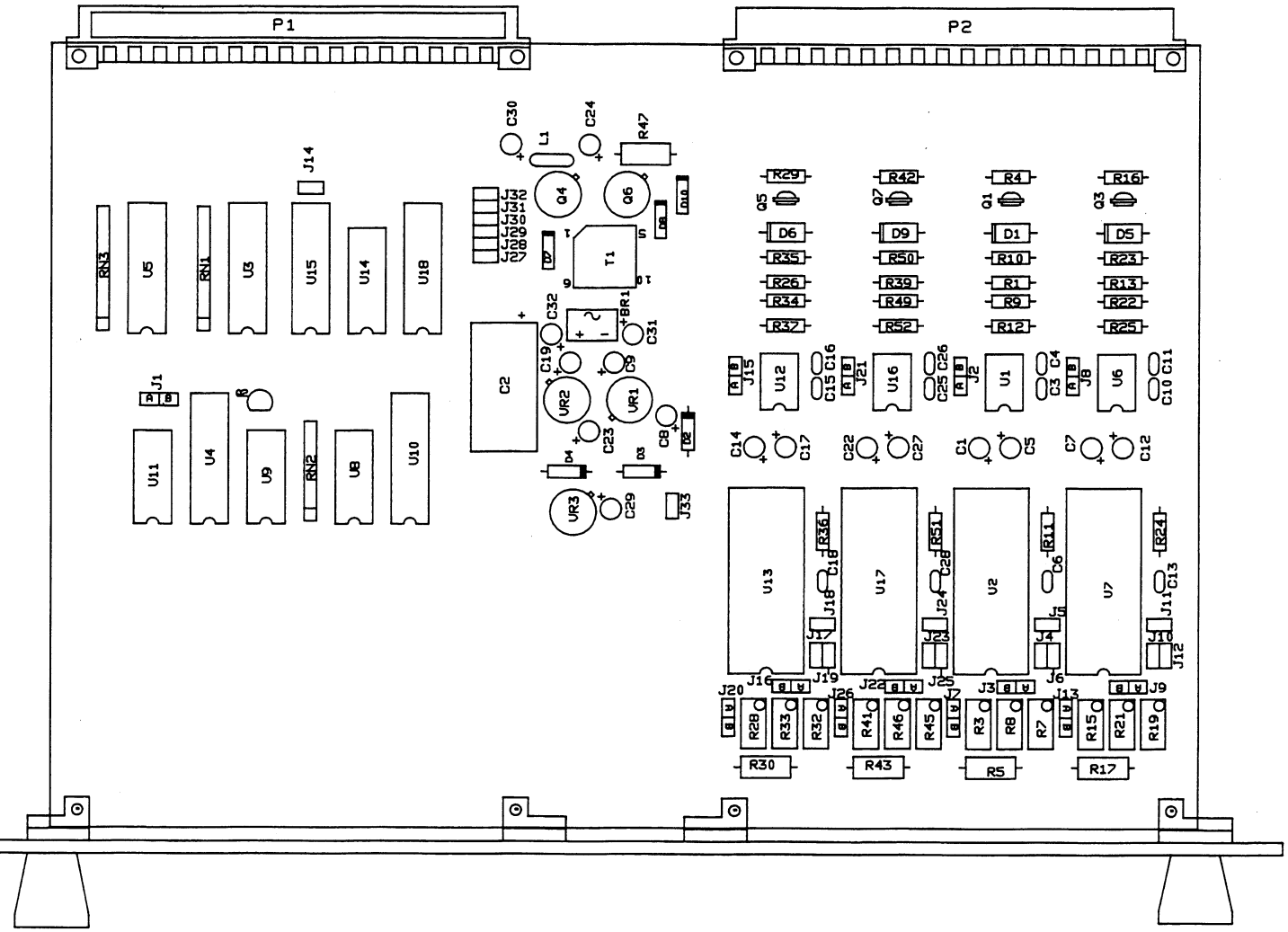
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XVME-505 ASSEMBLY DRAWING



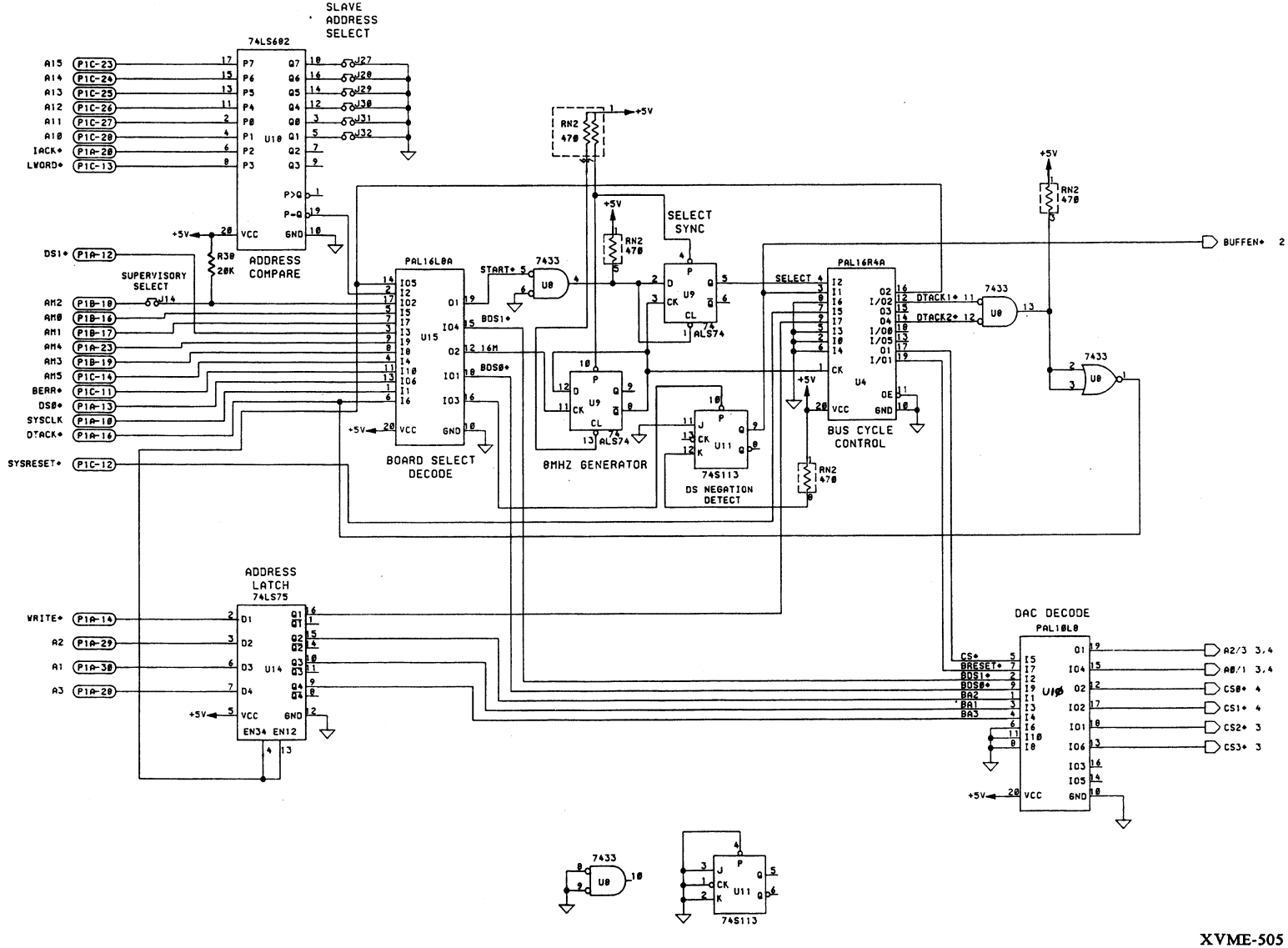
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XVME-595 ASSEMBLY DRAWING

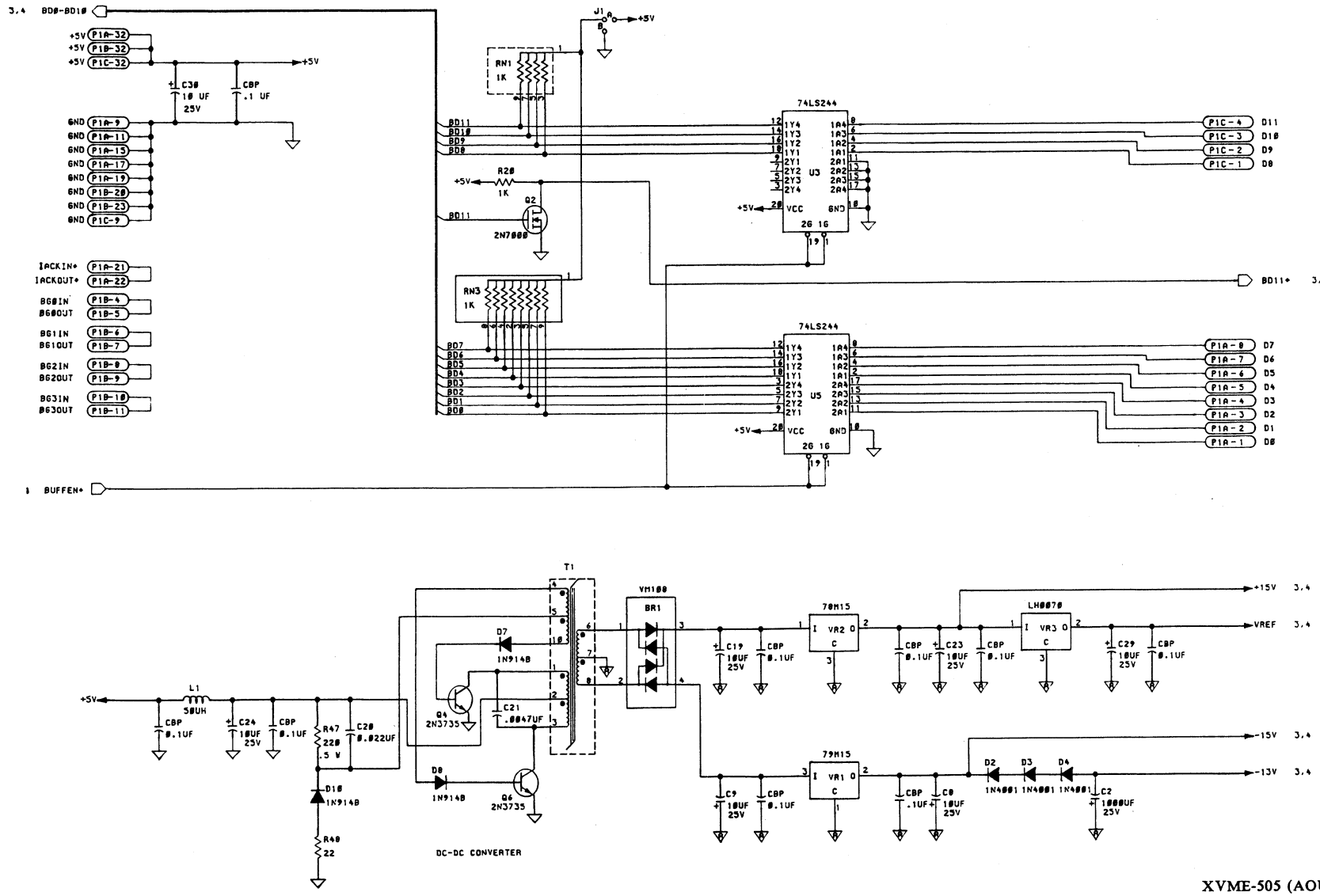


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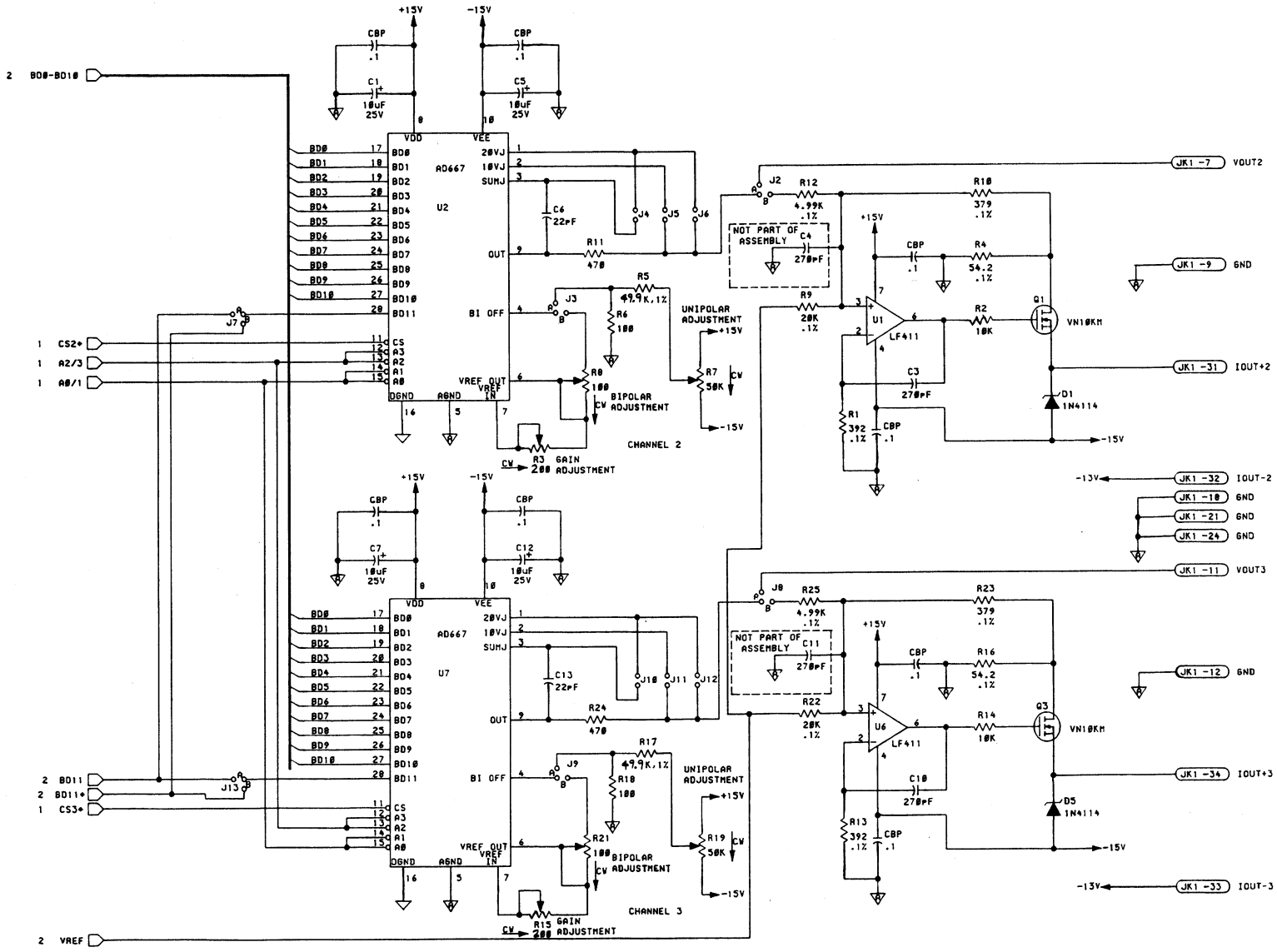
XVME-505 (AOUT) Schematic, Sheet 1 of 4



XVME-505 (AOUT) Schematic,
Sheet 2 of 4

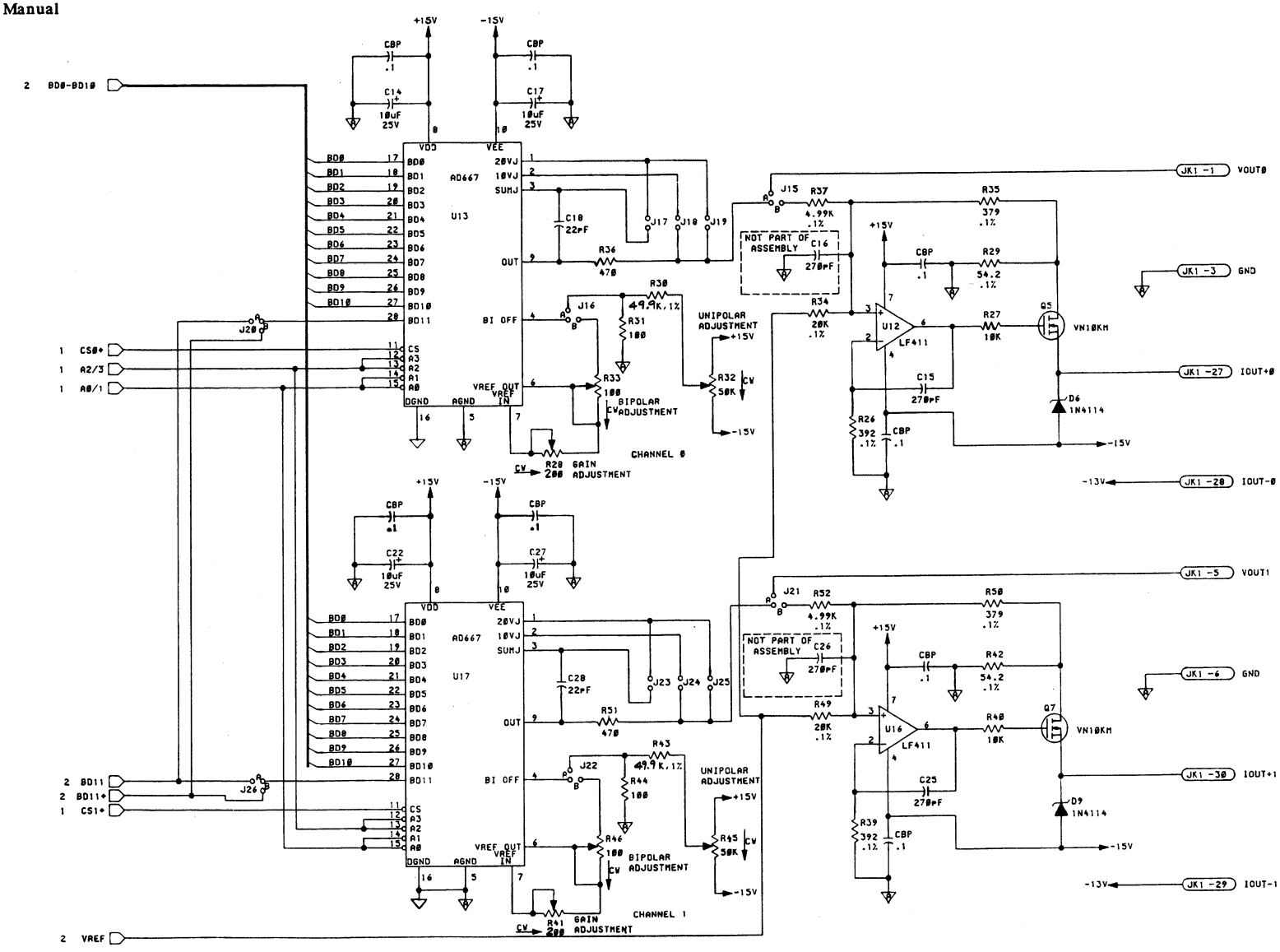
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RANGE	0 - 5V	±2.5V	0 - 10V	±5V	±10V
CHANNEL 2 JUMPER	J3-A J5,J4	J3-B J5,J4	J3-A J6,J5	J3-B J6,J5	J3-B J6
CHANNEL 3 JUMPER	J9-A J11,J10	J9-B J11,J10	J9-A J12,J11	J9-B J12,J11	J9-B J12

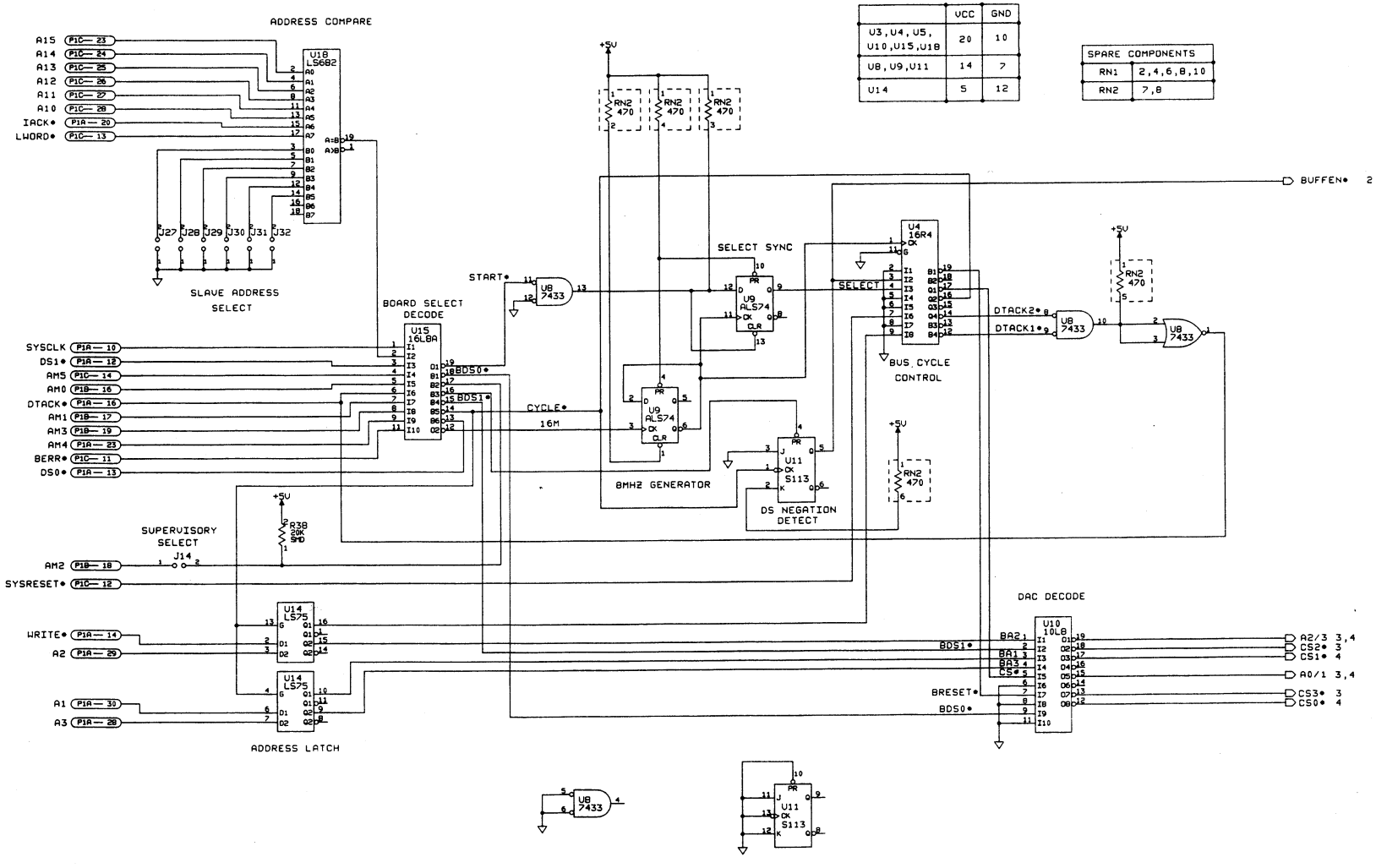
XVME-505 (AOUT) Schematic,
Sheet 3 of 4



RANGE	0 - 5V	±2.5V	0 - 10V	±5V	±10V
CHANNEL 0 JUMPER	J16-A J18,J17	J16-B J18,J17	J16-A J19,J18	J16-B J19,J18	J16-B J19
CHANNEL 1 JUMPER	J22-A J24,J23	J22-B J24,J23	J22-A J25,J24	J22-B J25,J24	J22-B J25

XVME-505 (AOUT) Schematic, Sheet 4 of 4

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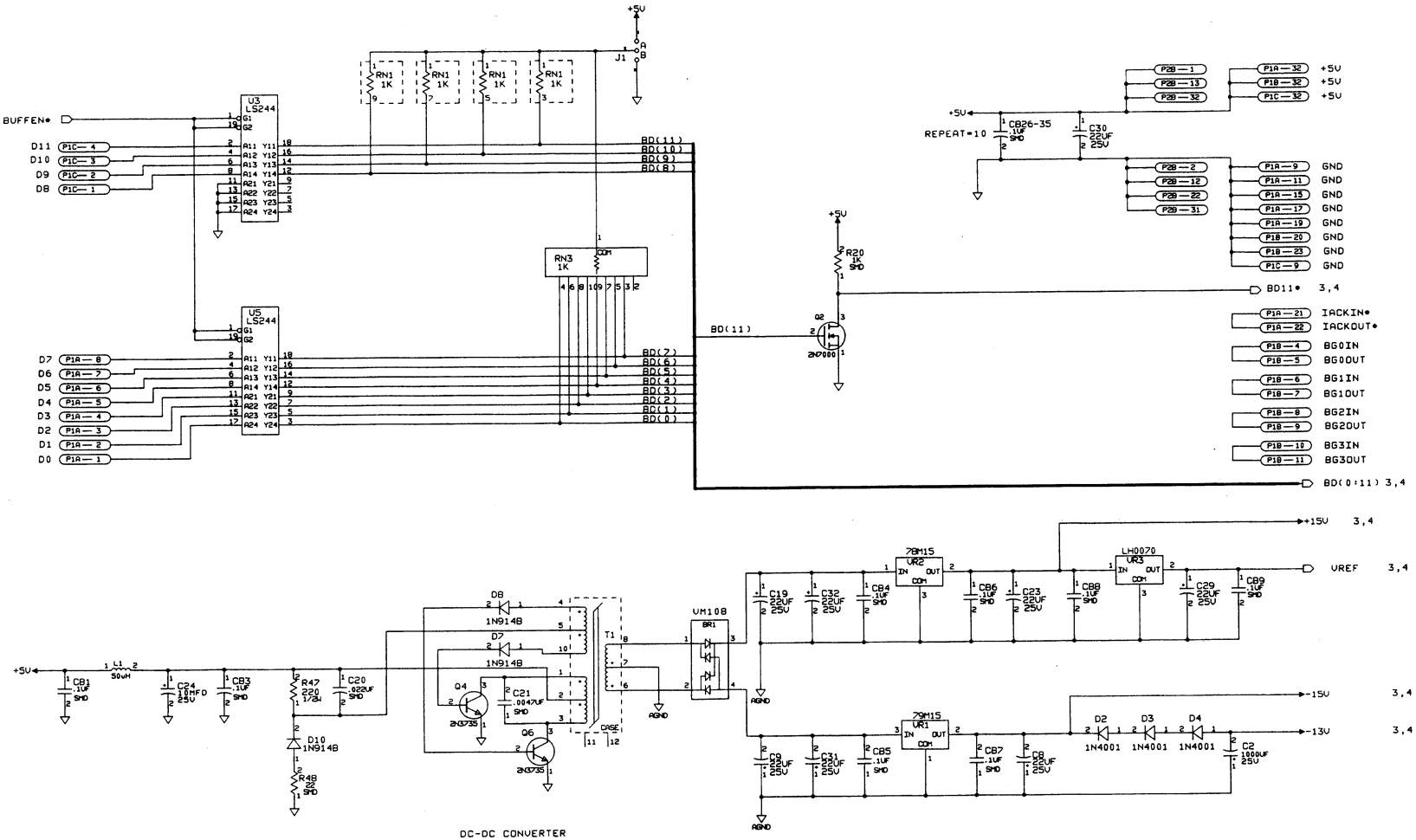
	VCC	GND
U3,U4,U5, U10,U15,U18	20	10
U8,U9,U11	14	7
U14	5	12

SPARE COMPONENTS	
RN1	2,4,6,8,10
RN2	7,8

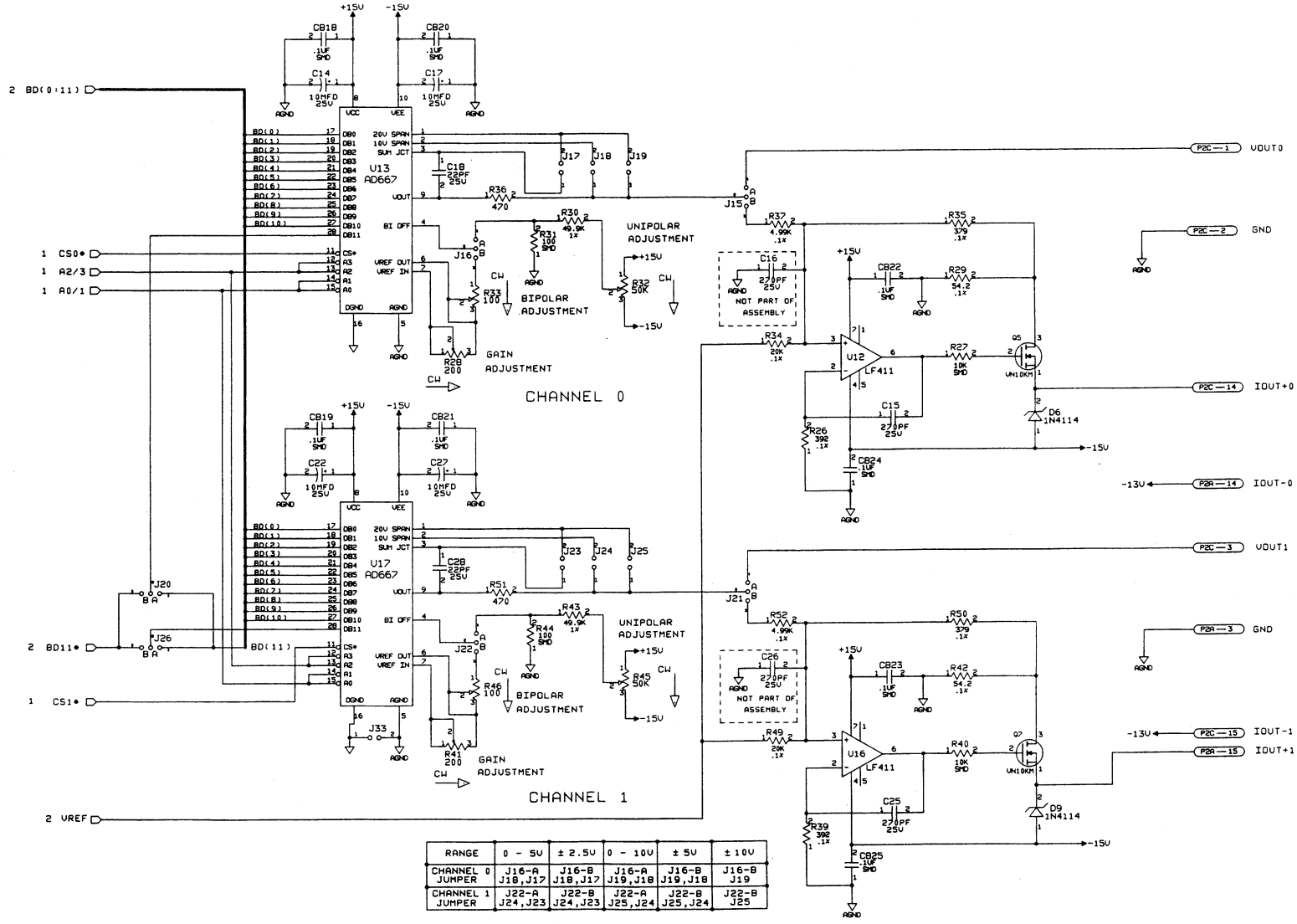
XVME-595 (AOUT) Schematic,
Sheet 1 of 4

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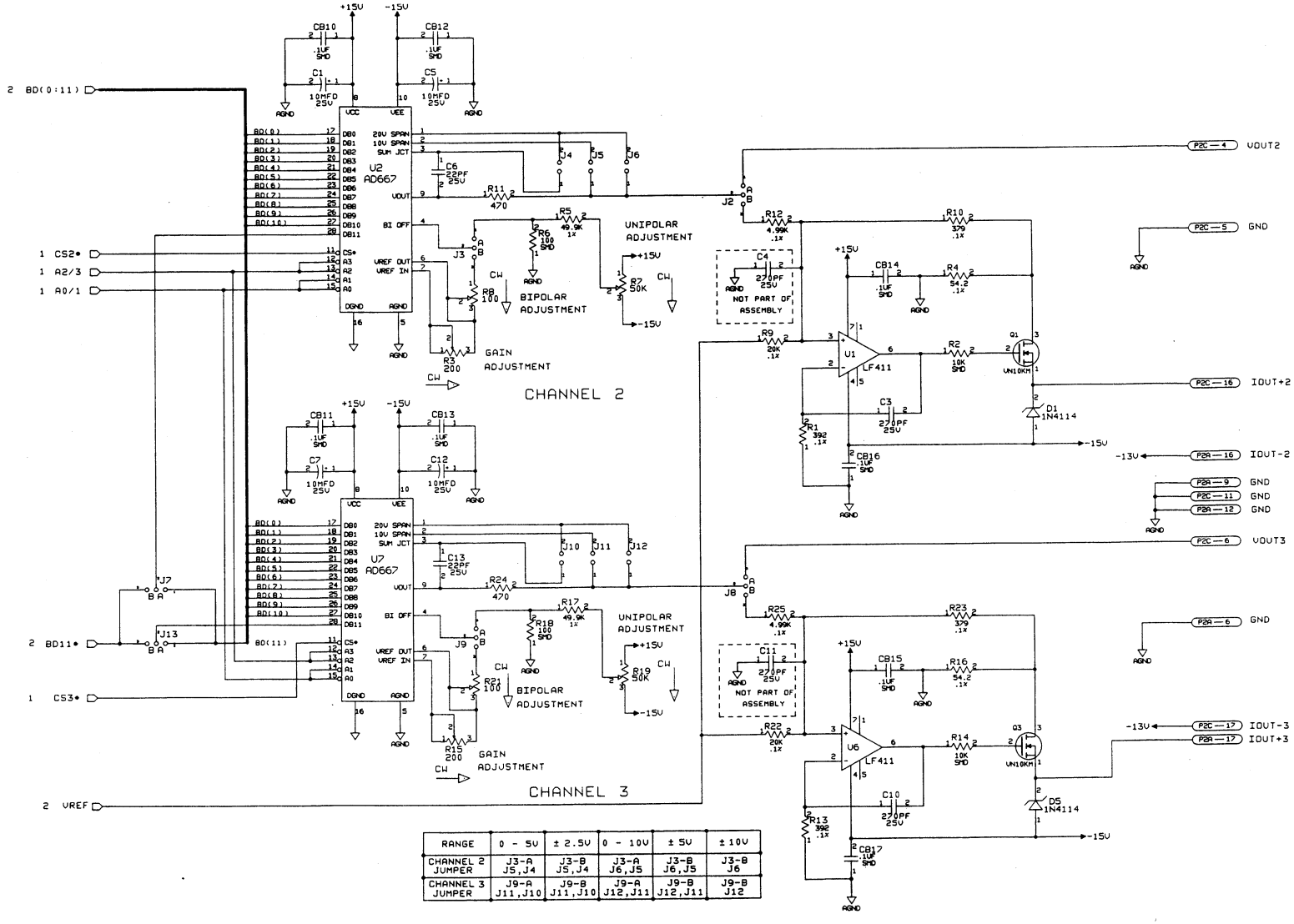
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RANGE	0 - 5V	± 2.5V	0 - 10V	± 5V	± 10V
CHANNEL 0 JUMPER	J16-A J18,J17	J16-B J18,J17	J16-A J19,J18	J16-B J19,J18	J16-B J19
CHANNEL 1 JUMPER	J22-A J24,J23	J22-B J24,J23	J22-A J25,J24	J22-B J25,J24	J22-B J25

XVME-595 (AOUT) Schematic,
Sheet 3 of 4

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RANGE	0 - 5V	± 2.5V	0 - 10V	± 5V	± 10V
CHANNEL 2 JUMPER	J3-A J5,J4	J3-B J5,J4	J3-A J6,J5	J3-B J6,J5	J3-B J6
CHANNEL 3 JUMPER	J9-A J11,J10	J9-B J11,J10	J9-A J12,J11	J9-B J12,J11	J9-B J12

XVME-595 (AOUT) Schematic,
Sheet 4 of 4

Appendix C

QUICK REFERENCE GUIDE

VMEbus Options

Jumper	Use
J27-J32	Module base address select jumpers (refer to Section 2.5.1).
J14	This jumper determines whether the module will respond to only supervisory accesses or to both supervisory and non-privileged accesses (refer to Section 2.5.2).

Digital to Analog Conversion Options

Jumper	Use
Jl	This jumper will automatically load the D/A converters on all channels with either all logic "l's" or all logic "O's" during system reset or power-up (refer to Section 2.6.1).
J7,J13, J20,J26	These jumpers provide the option to individually configure each output channel to convert either straight binary to analog, or to convert two's complement binary to analog (refer to Section 2.6.2).
J2,J15, J8,J21	On the XVME-505/595-2, these jumpers configure the four output channels to convert data to either an analog voltage format or an analog current format (refer to Section 2.6.3).
(J16-J17) (J22-J25) (J8,J4, J5,J6) (J9-J12)	These groups of jumpers select one of five output voltage ranges for each output channel. Four of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar offset or for the adjustment of bipolar off set voltage.
J33	(XVME-595 Only.) Connects analog to digital ground. This jumper is installed will foil and may be removed by the user to separate the grounds.

Table C-l. Access Options

Jumper J14	Access Mode Selection	Address Modifier Code
Installed	Supervisory Only	2DH
Removed	Supervisory or Non-Privileged	2DH or 29H

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Table C-2. Reset/Power-up Output States

Jumper Setting	Output States		
	Bipolar		Unipolar
	Off set Binary	Two's Comp.	Straight Binary
JlA	+FSR	0 - 1 LSB	+FSR (20mA)
JIB	-FSR	0 v	0V (4mA)

NOTE

FSR = Full Scale Range, and LSB = Least Significant Bit These terms are defined in more detail in Section 3.3.1.

Table C-3. Output Conversion Format Jumpers

output Channel	Digital Data Conversion Formats	
	Straight/Offset Binary	Twos' Complement
0	J20A	J20B
1	J26A	J26B
2	J7A	J7B
3	J13A	J13B

Table C-4. Voltage/Current Output Selection Jumpers (XVME-505/595-2 Option Only)

output Channel	Output	
	Voltage	Current
0	J15A	J15B
1	J21A	J2lB
2	J2A	J2B
3	J8A	J8B

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Table C-5. Output Voltage Range Configurations

Channel	Jumper	Output Voltage Ranges				
		±2.5V	±5V	±10V	0-5v	0-10V
0	J19	OUT	IN	IN	OUT	IN
0	J18	IN	IN	OUT	IN	IN
0	J17	IN	OUT	OUT	IN	OUT
0	J16	B	B	B	A	A
1	J25	OUT	IN	IN	OUT	IN
1	J24	IN	IN	OUT	IN	IN
1	J23	IN	OUT	OUT	IN	OUT
1	J22	B	B	B	A	A
2	J6	OUT	IN	IN	OUT	IN
2	J5	IN	IN	OUT	IN	IN
2	J4	IN	OUT	OUT	IN	OUT
2	J3	B	B	B	A	A
3	J12	OUT	IN	IN	OUT	IN
3	J11	IN	IN	OUT	IN	IN
3	Jl0	IN	OUT	OUT	IN	OUT
3	J9	B	B	B	A	A

NOTE

On the XVME-505/595-2, when using a channel in the current output mode (refer to Section 2.6.3), the voltage output jumpers for that channel must be configured for the 0-10V range.

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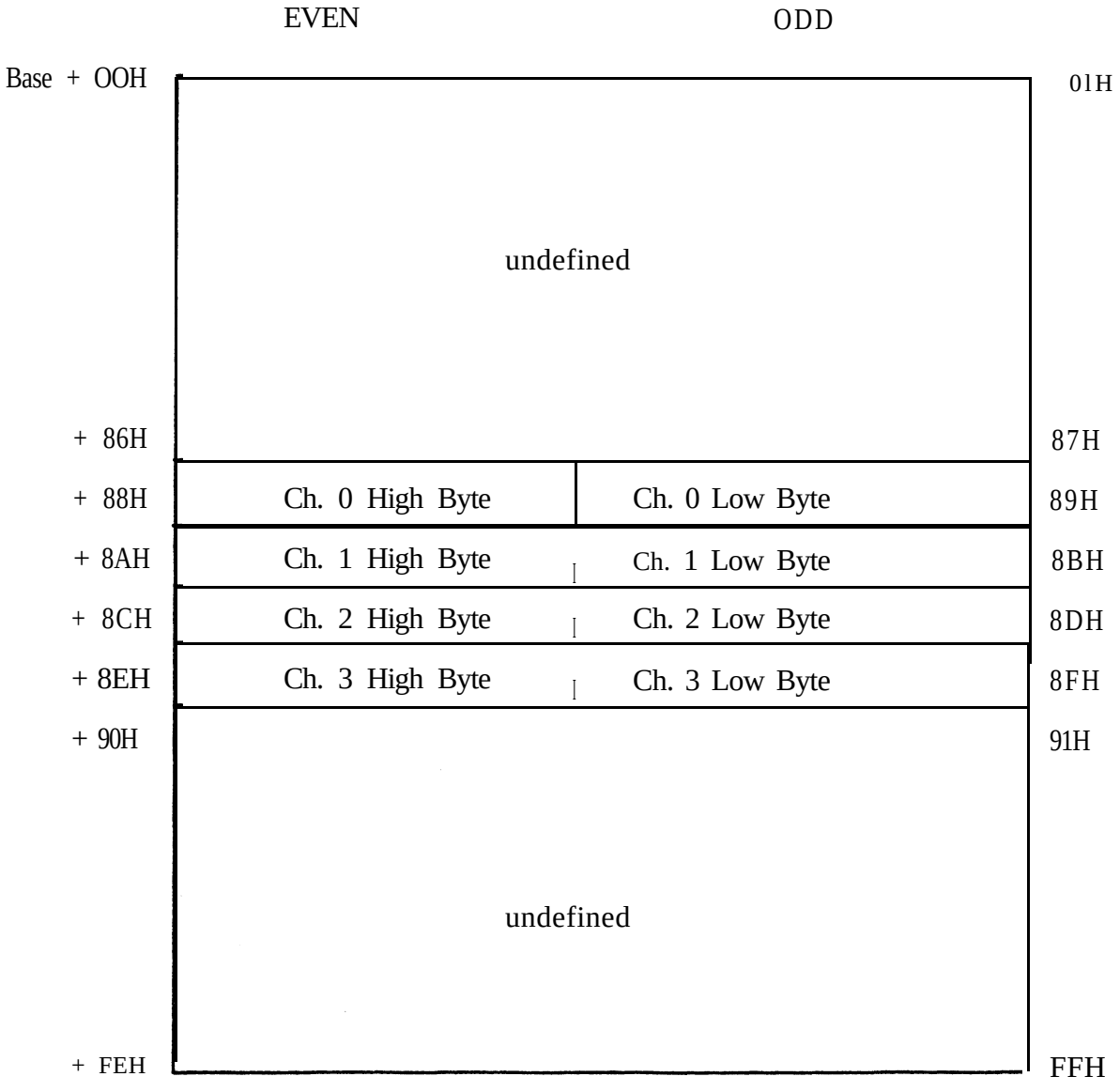


Figure C-l. XVME-505/595 Analog Output Module Memory Map

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Table C-6. Unipolar Mode
(Straight Binary Encoding)

X= Don't Care Voltage Mode: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	Vfsr - 1 LSB
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	Vfsr/2
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	0V
Current Mode (XVME-505/595-2 Only): D_{15} D_0	Analog Output 4-20mA
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	19.996mA (20mA - 1 LSB)
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	12mA
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	4mA

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Table C-7. Bipolar Modes

X= Don't Care Offset Binary Encoding: D_{15} D_0	Analog Output
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1 LSB
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	Vfsr/2
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	-Vfsr/2
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	-Vfsr
Two's Complement Encoding: D_{15} D_0	**Analog Output 4-20mA**
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1 LSB
X X X X 0 1 0 0 0 0 0 0 0 0 0 0	1/2 (+Vfsr)
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	1/2 (-Vfsr)
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	-Vfsr

NOTE

The "LSB" (least Significant Bit) represents the change in output voltage (or current) that is the result of an increase or decrease of the binary code by one count. The "LSB" is derived from the full range (fsr) of either current or voltage divided by the maximum conversion resolution (i.e., 12 bits or 4096 in binary equivalent). Thus, the value of one LSB can be determined by the following:

$$\text{Unipolar LSB} = \frac{\text{Vfsr}}{4096} \qquad \text{Bipolar LSB} = \frac{(+\text{Vfsr}) - (-\text{Vfsr})}{4096}$$

$$\text{Current LSB} = \frac{20\text{mA} - 4\text{mA}}{4096}$$

The following list shows the value of 1 LSB for each range:

±2.5V	= 1.2207mV
±5V	= 2.4414mV
±10V	= 4.8828mV
0 - 5V	= 1.2207mV
0 - 10V	= 2.4414mV
4 - 20mA	= 3.906uA

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Table C-8. D/A Calibration Potentiometers

Potentiometer No.	Type of Adjustment
R15	Gain adjustment for output channel 3
R3	Gain adjustment for output channel 2
R41	Gain adjustment for output channel 1
R28	Gain adjustment for output channel 0
R21	Channel 3 bipolar offset adjustment
R8	Channel 2 bipolar offset adjustment
R46	Channel 1 bipolar offset adjustment
R33	Channel 0 bipolar offset adjustment
R19	Channel 3 unipolar offset adjustment
R7	Channel 2 unipolar offset adjustment
R45	Channel 1 unipolar offset adjustment
R32	Channel 0 unipolar offset adjustment

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