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XVME 200/290

Digital I/O Modules

P/N 74200-002B

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Chapter 1

INTRODUCTION

1.1 OVERVIEW

The XVME-200 and XVME-290 are Digital I/O VMEbus compatible boards (also referred to as DIO Modules). The XVME-200 is a single-high (3U), single-wide module, and the XVME-90 is a double-high (6U), single-wide form factored modules. The DIO Module provides a VME system with 32 digital (TTL) I/O channels, full VMEbus interrupt capability, and port handshake control features. The DIO Module utilizes two 68230 Parallel Interface/Timer Integrated Circuit devices (also referred to as PI/T devices) to provide and control its parallel interface functions (with 16 I/O channels per PI/T device). In addition, the 68230 devices also provide two 240 bit, software-configurable timers (1 timer per PI/T device), which can be used to generate periodic interrupts, a single interrupt after a specified time period, or a square wave. The specific features of the DIO Module are listed below:

- Direct compatibility with OPT0 22 -- 24 point subsystems, of either single or quad density, with no transition interface required (XVME-290/2).
- Fully buffered TTL outputs, and hysteresis on TTL Inputs.
- Software-configurable port direction (i.e., ports may be configured to either input or output TTL level data).
- Complete VMEbus interrupt capability (I(1)-I(7) interrupts - STAT).
- Programmable IACK vector (with vector alteration based on the source of the interrupt.
- Port handshake signals are available to coordinate port data transfers.
- **TWO** 24=bit, software-configurable, timers.

The XVME-200 provides 32 digital I/O channels plus port handshake and timer control signals through the VMEbus P2 connector. The XVME-290/2 places all signals on OPT0 22 compatible connectors (JKI and JK2) located in the P2 area.

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1.2 MANUAL STRUCTURE

This manual consists of three chapters which divide the various aspects of module specification and operation into three distinct areas. The three chapters develop these aspects in the following progression:

Chapter One - A general description of the XVME-200/290 Digital I/O Module, including complete functional and environmental specifications, VMEbus compliance information, and a block diagram.

Chapter Two - DIO Module installation information covering module specific system requirements, jumpers, and connector pinouts.

Chapter Three - Details covering functional addressing, interrupt enabling, and programming considerations/requirements.

The Appendices are designed to provide additional information in terms of the backplane signal/pin descriptions, a block diagram and assembly drawing, and module schematics.

NOTE

In order to fully document the complex versatility of the XVME-200/290 and the 68230 PI/T device, a manual kit is being shipped with the XVME-200/290 DIO Module (the manual kit is referenced as XYCOM Part #74200-001). This kit consists of two parts: a *Motorola MC68230 Manual (c) (referenced as XYCOM Part #74200-003), and an XVME-200/290 Manual (referenced as XYCOM Part #74200-002.

It is recommended that the user read (completely) the 68230 Manual prior to reading further in the XVME-200/290 Manual. After becoming familiar with the 68230 and how it is programmed, the user should then read the remainder of the XVME-200/290 Manual to become acquainted with module base addressing, register access offsets, interrupt control, handshake control, and operational mode/programming constraints.

* MC68230 Parallel Interface/Timer Manual, (c)Motorola Inc., 1983

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1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows the operational block diagram of the XVME-200 and the XVME-290/2 DIO Modules. Figure 1-2 shows an operational block diagram of the XVME-290/1. The XVME-290/2 is identical to the XVME-200 DIO operational block diagram, however, the JK1 and JK2 connectors are located on the back of the module near the VMEbus P2 connector instead of on the module front panel.

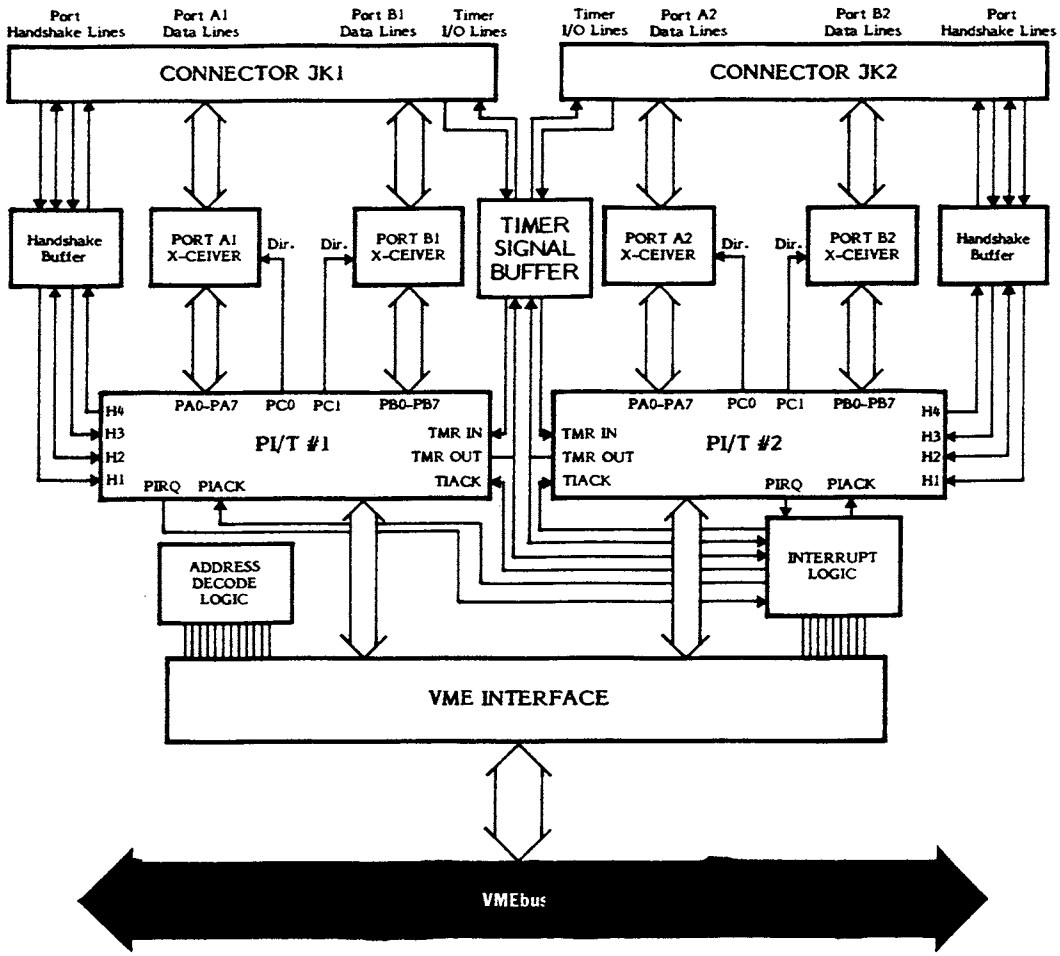


Figure 1-1. XVME-200 and 290/2 DIO Module Operational Block Diagram

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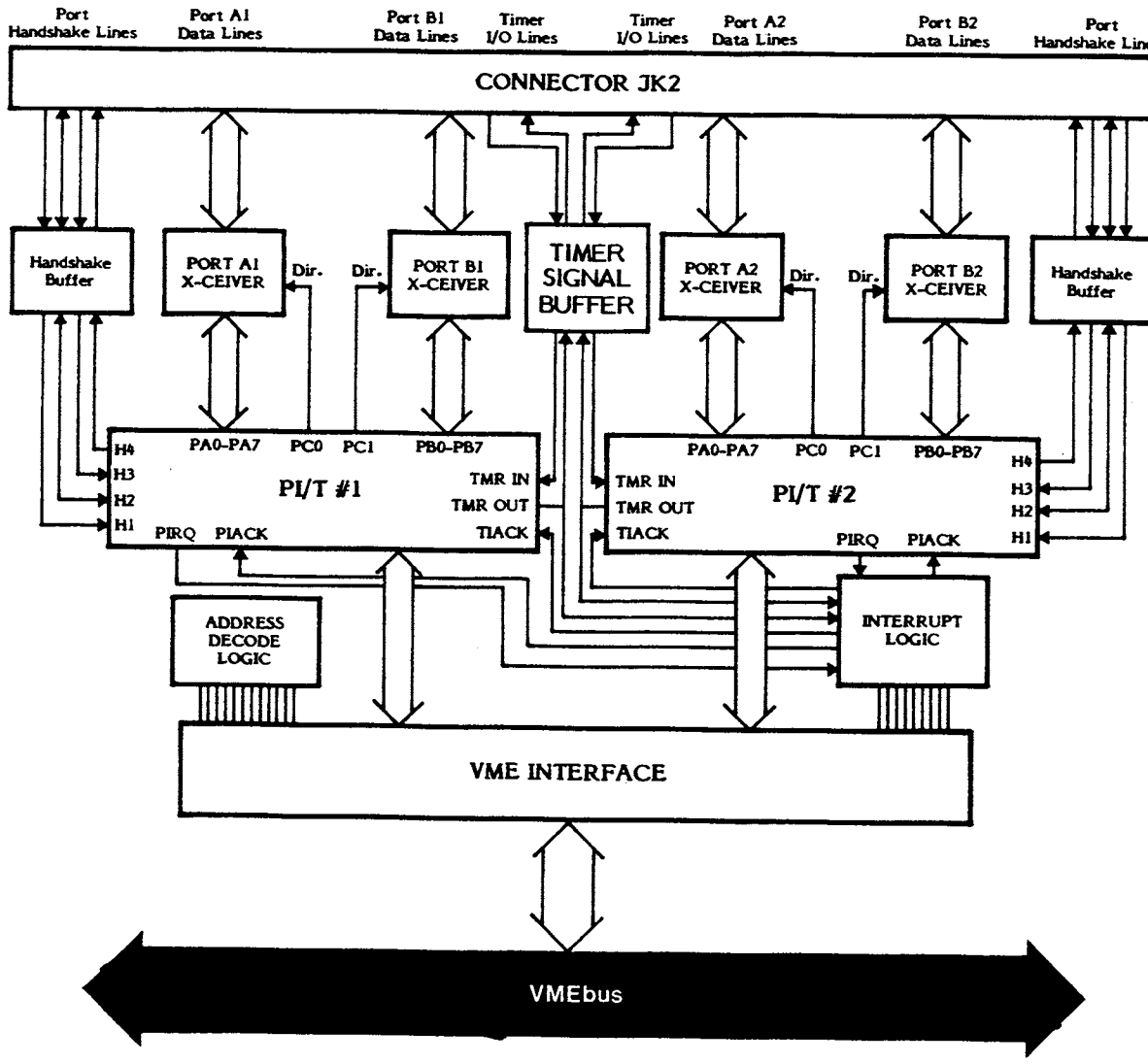


Figure 1-2. XVME-290/1 DIO Module Operational Block Diagram

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The DIO Module uses two 68230 Parallel Interface/Timer devices to provide a total of 32 parallel I/O lines (16 lines per chip) arranged as four I/O ports (two 8 line ports per chip), as well as 2 programmable timers (1 timer per chip). Several different operating modes can be programmed for the parallel ports and timers, to provide a high degree of versatility and flexibility.

Each 68230 chip has two (8 line) I/O ports labeled as Port Al and Port Bl for PI/T #l, and Port A2 and Port B2 for PI/T #2. The third Port on each PI/T chip (Port C/Alternate Function) is configured as a group of dedicated control lines for interrupt handling, timer operation, and data port direction.

Each of the four I/O ports is independently buffered by its own 8-bit data transceiver. The data transceivers are all bidirectional, with their direction being independently controlled by PC0 and PC1 of the Port D/Alternate Function lines on each PI/T. The 8 data lines within each of the four PI/T I/O ports Al, A2, Bl, and B2 must always be programmed for the same direction (i.e., because transceiver data direction is programmed individually for each port and cannot be done on a line-by-line basis). In order to avoid signal direction contention between a PI/T Port and its data transceiver, the direction of the ports and transceivers must be programmed in the proper order (documented in Chapter 2).

The DIO Module design allows each of the PI/T ports Al, Bl, A2, or B2 to be individually programmed in either Port Mode 0 or Port Mode 1 (refer to the 68230 Manual for a description of Port Modes). In addition, any of the submodes within Port Modes 0 and 1 may be utilized. There are 4 buffered handshake lines for each PI/T chip which (depending on the operation mode selected and the position of jumpers Jl and J3) can be used to provide interlocked handshake, pulsed handshake, interrupt input (independent of data transfer), or general purpose single-line I/O.

Each PI/T chip also contains its own 24-bit timer capable of signaling event occurrence by generating a periodic interrupt, an interrupt after timeout, or a square wave output. The timer interrupt capability is enabled by using three of the Port C/Alternate Function pins programmed to carry the Timer Interrupt functions (i.e., Timer Interrupt enable, Timer input, and Timer output).

The module address decode logic allows the user to select (via 6 jumpers) any one of 64 of the 1K boundaries in the Short I/O Address Space to be used as the module base address. The PI/T Internal Registers are accessible at specific addresses offset from the selected module base address. Any of the 7 VMEbus interrupt levels may be selected (via 3 jumpers) to facilitate interrupt generation, and handling from any one of 4 interrupt sources on the module (i.e., PI/T #l port interrupts, PI/T #2 port interrupts, PI/T #l timer interrupts, and PI/T #2 timer interrupts). Each of the two PI/T chips is capable of producing 5 different IACK vectors (one for the timer and four for the ports) for a total of ten different IACK vectors per module.

On the XVME-200/290 the configuration of the PI/Ts differ only in whether their I/O signals interface to JKl or JK2 (XVME-200, XVME-290/2) or which P2 pins the I/O signals connect to (XVME-290/l), and the jumper number which controls the direction of H2, which must be distinct.

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1.4 MODULE SPECIFICATIONS

The following is a list of the operational and environmental specifications for the XVME-200/290 DIO Module.

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Table 1-1. Digital I/O Module Specifications

Characteristic	Specification
Number of Channels	32
Parallel Interface Device	68230 (2 per module)
Input Characteristics	Vil = 0.8V max., Iil = -750 uA max. Vih = 2.0v min., lil= -325 uA max.
Output Characteristics	Vol = 0.4V max., Iol = 12 mA Vol = 0.5V max., Iol = 24 mA Voh = 2.4V min., Ioh = -3 mA Voh = 2.0v min., Ioh = -15 mA
Power Requirements	+5V, 1.3 A typ., 1.5 A max.
Board Dimensions	Single-height size (150 x 116.7 mm)(XVME-200) Double-height size (160 x 233.4 mm)(XVME-290)
Temperature	
Operating	0" to 32'C (32° to 149°F)
Non-Operating	-40° to 85°C (-40° to 158°F)
Humidity	5 to 95% RH non-condensing (Extremely low humidity may require protection against static discharge.)
Altitude	
Operating	Sea-level to 10,000 ft. (3048m)
Non-Operating	Sea-level to 50,000 ft. (15240m)
Vibration	
Operating	5 to 2000 Hz 0.015" peak-to-peak displacement 2.5 g peak acceleration
Non-Operating	5 to 2000 Hz 0.030" peak-to-peak displacement 5.0 g peak acceleration
Shock	
Operating	30 g peak acceleration 11 msec duration
Non-Operating	50 g peak acceleration 11 msec duration

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VMEbus Compliance

- Complies with VMEbus Standard Rev. C.l
- A 16:D8(0) DTB Slave
- I(1) to I(7) interrupter (STAT) with programmable interrupt vector
- Size - Single (XVME-200
- Size - Double (XVME-290)
- Base address jumper-selectable on 1K boundaries within the VMEbus short I/O address space

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Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter explains how to configure the XVME-200/290 DIO Module prior to installation in a VMEbus backplane. Included in this chapter is information on module base address selection jumpers, module interrupt level selection jumpers, the handshake line H2 direction jumpers, connector pinouts, and a brief outline of the physical installation procedure.

2.2 SYSTEM REQUIREMENTS

The XVME-200/290 DIO Modules are VMEbus compatible modules. To operate, they must be properly installed in a VMEbus backplane.

The minimum system requirements for the operation of an XVME-200/290 DIO Modules are one of the following:

A) A host processor module properly installed on the same backplane as the XVME-200/290; and a controller subsystem module which employs a Data Transfer Bus Arbiter, a System Clock driver, a System Reset driver, and a Bus timeout module. (The XYCOM XVME-010 System Resource Module provides a controller subsystem with the components listed.)

-- OR --

B) A host processor module which incorporates an on-board controller subsystem (such as XYCOM's XVME-600 or XVME-601).

Prior to installing the XVME-200/290 DIO Modules, it will be necessary to configure several jumper options. These options are:

1) Module base address within the short I/O address space.
2) Address Modifier codes to which the DIO Module will respond.
3) Interrupt level.
4) Direction of handshake line H2 on the 68230 PI/T chip.

2.3 XVME-200/290 DIO MODULE JUMPER/CONNECTOR LOCATIONS

The jumpers and connectors relevant to the installation of the XVME-200 DIO Module are shown in Figure 2-1, and the jumpers and connectors relevant to the installation of the XVME-290/2 DIO Module are shown in Figure 2-2, and Figure 2-3 shows the XVME-290/l.

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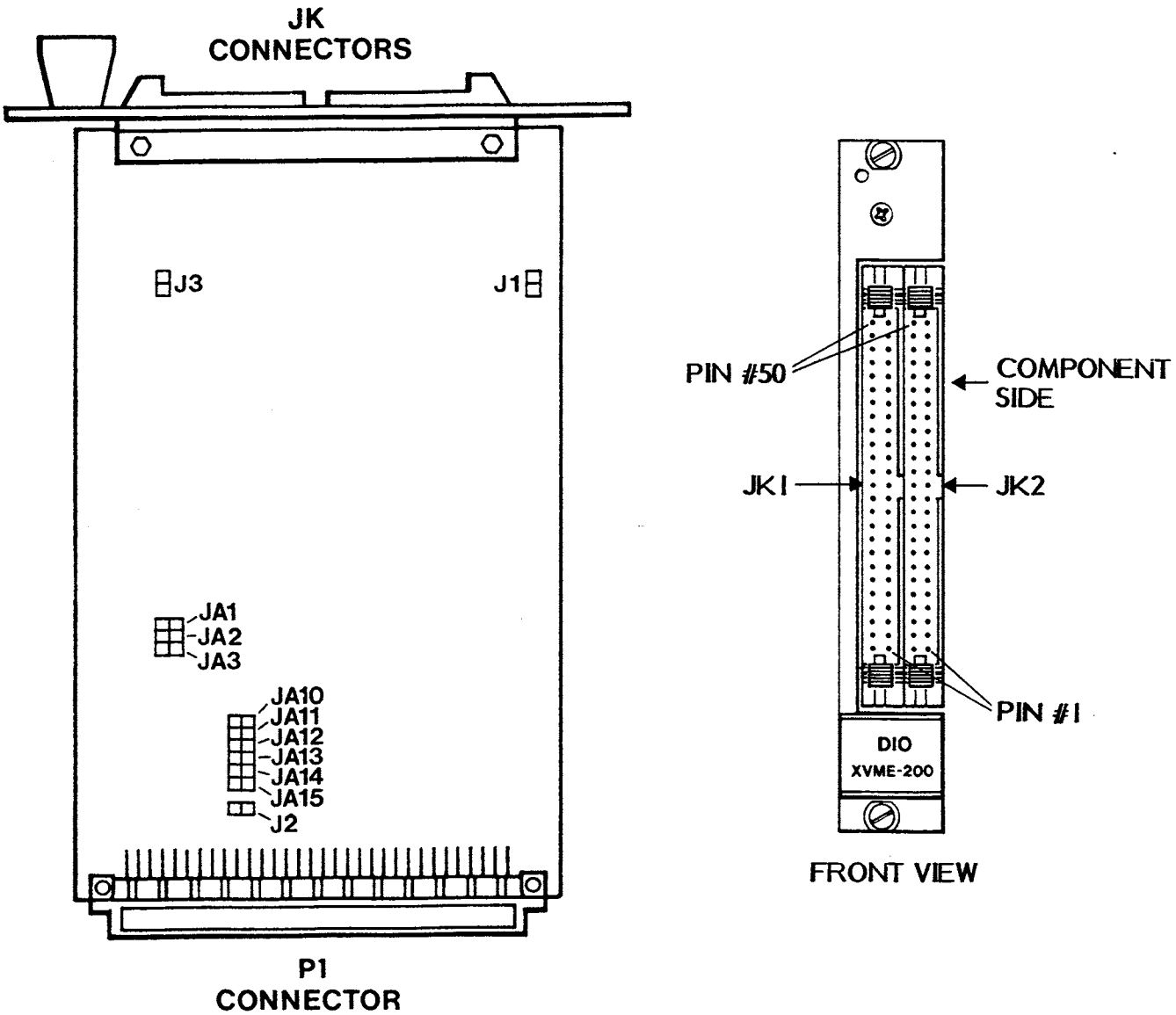


Figure 2-1. Jumper/Connector Locations on the XVME-200 DIO Module

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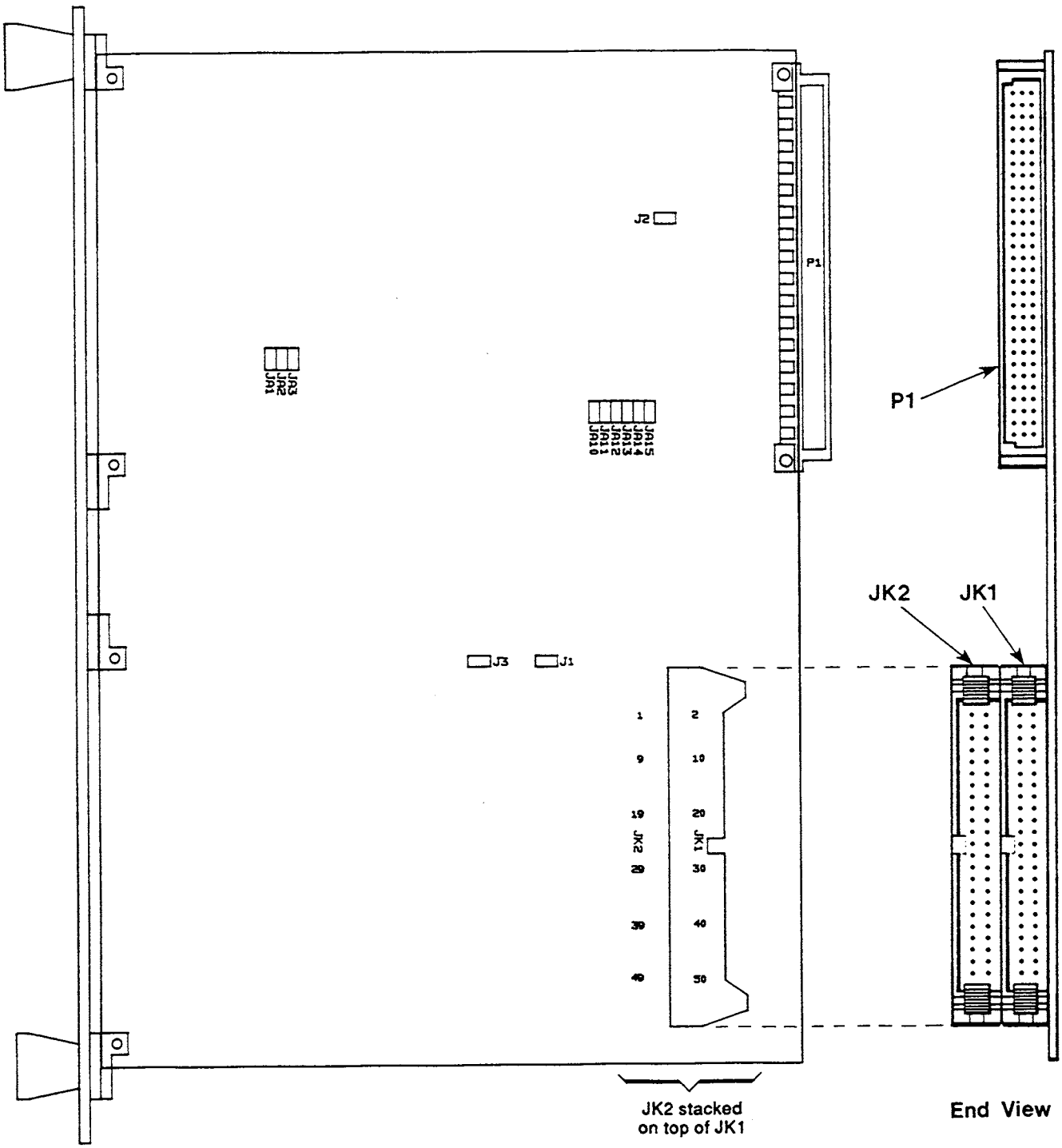


Figure 2-2. Jumper/Connector Locations on the XVME-290/2 DIO Module

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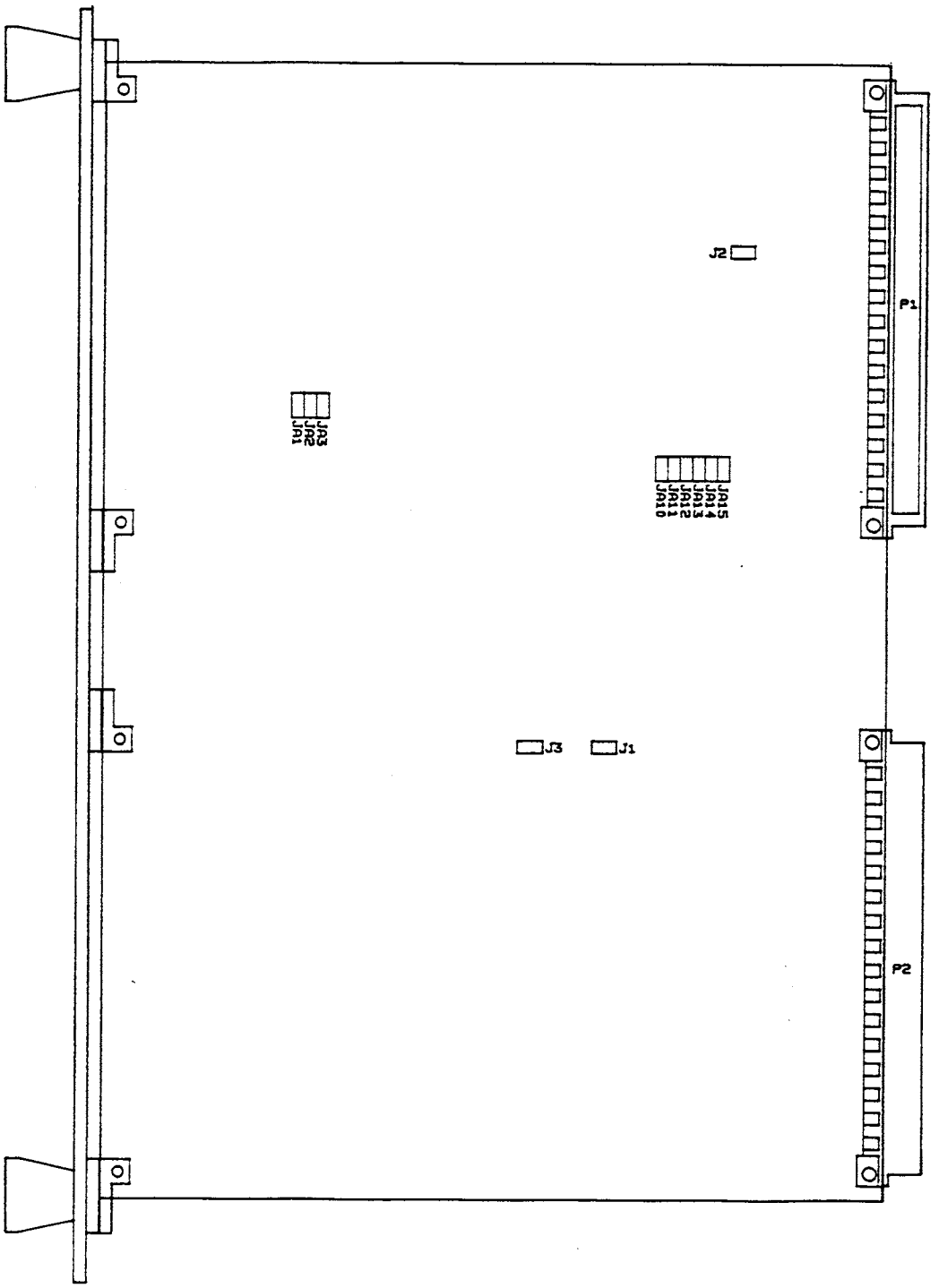


Figure 2-3. Jumper/Connector Locations on the XVME-290/1 DIO Module

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2.4 XVME-200/290 DIO MODULE JUMPER LIST

Table 2-1. DIO Module Jumper List

Jumper	Use
Jl and J3	Determine the direction of handshake line H2 for both of the PI/T chips (refer to Section 2.4.5 of this manual).
J2	Determines whether the module will respond to supervisory or non-privileged short I/O VMEbus cycles (refer to Section 2.4.2 of this manual).
JAl0-JAI5	Select module base address on any one of the 64 1K boundaries within the short I/O address space (refer to Section 2.4.1 of this manual).
JA1-JA3	Select the VMEbus interrupt level for the module (refer to Section 2.4.3 of this manual).

2.4.1 Base Address Jumpers

The DIO Module can be configured to be addressed at any one of the 64 IK boundaries within the VME Short I/O Address space by using jumpers JAI0 through JA15 (see Figure 2-1 (XVME-200), or Figure 2-2 (XVME-290) for the location of the jumpers on the board) as shown below:

Table 2-2. Base Address Jumper Options

JA15	JA14	JA13	JA12	JAI1	JAI0	Base Address of Module
IN	IN	IN	IN	IN	IN	0000H
IN	IN	IN	IN	IN	OUT	0400H
IN	IN	IN	IN	OUT	IN	0800H
IN	IN	IN	IN	OUT	OUT	0C00H
IN	IN	IN	OUT	IN	IN	1000H
IN	IN	IN	OUT	IN	OUT	1400H
IN	IN	IN	OUT	OUT	IN	1800H
IN	IN	IN	OUT	OUT	OUT	1C00H
IN	IN	OUT	IN	IN	IN	2000H
IN	IN	OUT	IN	IN	OUT	2400H
IN	IN	OUT	IN	OUT	IN	2800H
IN	IN	OUT	IN	OUT	OUT	2C00H
IN	IN	OUT	OUT	IN	IN	3000H

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Table 2-2. Base Address Jumper Options (Cont'd)

JA15	JA14	JA13	JA12	JAll	JAlO	Base Address of Module
IN	IN	OUT	OUT	IN	OUT	3400H
IN	IN	OUT	OUT	OUT	IN	3800H
IN	IN	OUT	OUT	OUT	OUT	3COOH
IN	OUT	IN	IN	IN	IN	4000H
IN	OUT	IN	IN	IN	OUT	4400H
IN	OUT	IN	IN	OUT	IN	4800H
IN	OUT	IN	IN	OUT	OUT	4COOH
IN	OUT	IN	OUT	IN	IN	5000H
IN	OUT	IN	OUT	IN	OUT	5400H
IN	OUT	IN	OUT	OUT	IN	5800H
IN	OUT	IN	OUT	OUT	OUT	5COOH
IN	OUT	OUT	IN	IN	IN	6OOOH
IN	OUT	OUT	IN	IN	OUT	6400H
IN	OUT	OUT	IN	OUT	IN	6800H
IN	OUT	OUT	IN	OUT	OUT	6COOH
IN	OUT	OUT	OUT	IN	IN	7000H
IN	OUT	OUT	OUT	IN	OUT	7400H
IN	OUT	OUT	OUT	OUT	IN	7800H
IN	OUT	OUT	OUT	OUT	OUT	7COOH
OUT	IN	IN	IN	IN	IN	8OOOH
OUT	IN	IN	IN	IN	OUT	8400H
OUT	IN	IN	IN	OUT	IN	8800H
OUT	IN	IN	IN	OUT	OUT	8COOH
OUT	IN	IN	OUT	IN	IN	9000H
OUT	IN	IN	OUT	IN	OUT	9400H
OUT	IN	IN	OUT	OUT	IN	9800H
OUT	IN	IN	OUT	OUT	OUT	9COOH
OUT	IN	OUT	IN	IN	IN	AOOOH
OUT	IN	OUT	IN	IN	OUT	A400H
OUT	IN	OUT	IN	OUT	IN	A800H
OUT	IN	OUT	IN	OUT	OUT	ACOOH
OUT	IN	OUT	OUT	IN	IN	BOOOH
OUT	IN	OUT	OUT	IN	OUT	B400H
OUT	IN	OUT	OUT	OUT	IN	B800H
OUT	IN	OUT	OUT	OUT	OUT	BCOOH
OUT	OUT	IN	IN	IN	IN	COOOH
OUT	OUT	IN	IN	IN	OUT	C4OOH
OUT	OUT	IN	IN	OUT	IN	C8OOH
OUT	OUT	IN	IN	OUT	OUT	CCOOH
OUT	OUT	IN	OUT	IN	IN	DOOOH
OUT	OUT	IN	OUT	IN	OUT	D400H
OUT	OUT	IN	OUT	OUT	IN	D800H
OUT	OUT	IN	OUT	OUT	OUT	DCOOH
OUT	OUT	OUT	IN	IN	IN	EOOOH
OUT	OUT	OUT	IN	IN	OUT	E400H

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Table 2-2. Base Address Jumper Options (Cont'd)

JA15	JA14	JAI3	JA12	JAI1	JAI0	Base Address of Module
OUT	OUT	OUT	IN	OUT	IN	E800H
OUT	OUT	OUT	IN	OUT	OUT	EC00H
OUT	OUT	OUT	OUT	IN	IN	F000H
OUT	OUT	OUT	OUT	IN	OUT	F400H
OUT	OUT	OUT	OUT	OUT	IN	F800H
OUT	OUT	OUT	OUT	OUT	OUT	FC00H

2.4.2 Address Modifier Jumper

The DIO Module has one jumper that determines which Address Modifier Codes it will respond to. This jumper is labeled as J2 (see Figure 2-1 for the jumper location). Jumper J2 determines whether the module will respond to supervisory or to non-privileged short I/O VMEbus cycles. When jumper J2 is in, the module will respond to supervisory short I/O bus cycles only. When jumper J2 is out, the module will respond to both non-privileged and supervisory short I/O bus cycles. Table **2-3** shows the relationship between jumper J2 and the Address Modifiers.

Table 2-3. Addressing Options

Jumper J2	Address Modifier that the DIO Module will respond to
In	(2DH) Supervisory Only
out	(2DH) Supervisory or (29H) Non-privileged

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2.4.3 Interrupt Level Selection Jumpers

The DIO Module can either be configured to generate VMEbus interrupts at levels 1-7 or the module interrupt capability can be completely disabled. Table 2-4 shows how jumpers JAI-JA3 are used to determine the interrupt level status for the DIO Module.

Table 2-4. Interrupt Level Jumper Positions

JA3	JA2	JAl	Interrupt Level Selected
In	In	In	None, VMEbus Interrupter disabled
In	In	Out	Level 1
In	Out	IN	Level 2
In	Out	Out	Level 3
Out	In	In	Level 4
Out	In	Out	Level 5
Out	Out	In	Level 6
Out	Out	Out	Level 7

The modules are shipped from the factory with jumpers JAI, JA2, and JA3 installed.

NOTE

When the module is never required to generate interrupts, JAl, JA2, and JA3 should all be installed to ensure that a programming bug will not generate a VMEbus interrupt.

2.4.4 BGIN*/BGOUT*-IACKIN*/IACKOUT* Daisy Chain

The Data Bus Arbitration signals BGIN*/BGOUT* are not used by the DIO Module and are hardwired together on the module to allow the Bus Arbitration Daisy Chain to pass through the backplane slot occupied by the DIO Module. In each slot of the VMEbus backplane there are set of jumpers which short the "IN" lines to the "OUT" lines. Since the BGIN*/BGOUT* signals are already hardwired on the DIO Module, it is not necessary to insert the corresponding jumper on the slot occupied by the DIO Module. However, the IACKIN*/IACKOUT* signals are used by the DIO Module and thus, the backplane jumper for these signals must not be installed in the backplane slot occupied by the DIO Module.

2.4.5 Handshake Line H2 Direction Jumpers

The 68230 PI/T chips on the DIO Module can be programmed to operate in Modes 0 and 1 (refer to the 68230 Manual for mode explanation). Data transfers in these modes can be controlled via the four handshake pins on each chip. These handshake pins are designed to be used in any of several different programmable protocols (a thorough understanding of Modes 0 and 1, and their associated submodes presented in the 68230 Manual is necessary in order to fully understand the variety of protocols).

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In these modes, the direction of two of the handshake pins (H2 and H4) should be programmable. However, due to constraints in hardware design, pin H4 must always be programmed as an output. Thus, pin H2 may be programmed as either an input or an output depending on what type of handshake protocol is to be used. Jumpers Jl and J3 (refer to Figure 2-1 (XVME-200) or Figure 2-2 (XVME-290) for the location of these jumpers) are used in conjunction with the programmed direction of pin H2 to determine whether the buffered handshake line H2 will be used as an input or an output. Jumper Jl is used to control the direction of the PI/T #l - H2 line and Jumper J3 is used to control the direction of the PI/T #2 - H2 line.

NOTE

In order to prevent the possibility of signal contention when using handshake protocol, pin H4 of a 68230 chip must always be programmed as an output with the H4 interrupt disabled, and the programmed direction of pin H2 must be consistent with the position of the corresponding jumper (J1 or J3).

Table 2-5 shows the relationship between the position of jumpers Jl and J3 and the direction of the buffered handshake line H2 for each of the PI/T chips.

Table 2-5. Handshake Line H2 Direction Jumpers

PI/T #I Jumper JI	PI/T #2 Jumper J3	Direction of the corresponding H2 handshake lines.
In Out	In Out	Input Output

CAUTION

The module is factory-shipped with Jl and J3 installed. Therefore, it will be necessary to remove the jumpers if the PI/T H2 lines are to be programmed as outputs. Failure to do so will result in signal contention.

2.5 CONNECTOR PIN ASSIGNMENTS

2.5.1 JKl and JK2 Connectors

The PI/T port data lines, port handshake lines, and timer I/O lines are all available to the user at two 50-pin connectors located on the module front panel (refer to Figure 2-1 (XVME-200) or Figure 2-2 (XVME-290)). The connectors are labeled JKl and JK2. The two connectors have identical pinouts and differ only as to which PI/T device they interface with. Connector JKl carries the signals pertaining to PI/T #l and Connector JK2 carries the signals pertaining to PI/T #2.

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The XVME-290 Module I/O interconnect is done via P2 of the VMEbus backplane (XVME-290/l) or through two 50-pin connectors (JKl and JK2) mounted in the P2 area (XVME-290/2). On the XVME-290/l, P2 carries all the signals for both PI/T #1 and PI/T #2, while for the XVME-290/2, JKl carries signals for PI/T #l and JK2 carries signals for PI/T #2.

NOTE

Connectors JKl and JK2 are directly compatible with OPT0 22 24-point subsystems, flat cables can be connected directly from the XVME-200 and XVME-290/2 to the OPT0 22 system without the need for a transition interface.

Table 2-6 shows the pin assignments for Connectors JKl and JK2, the signal direction with respect to the XVME-200 and the XVME-290/2 Modules, and the corresponding OPT0 22 channel number.

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Table 2-6. Pin Assignments for Connectors JK1 and JK2

Pin #	JK1 Signal	JK2 Signal	OPTO 22 Channel #	Signal Direction
1	--------- Not Connected		----------	----------
2	GND	GND		
3	H4 OUT-1	H4 OUT-2	22	OUTPUT
4	GND	GND		
5	H2 OUT-1	H2 OUT-2	21	OUTPUT
6	GND	GND		
7	TMR OUT-1	TMR OUT-2	20	OUTPUT
8	GND	GND		
9	H2 IN-1	H2 IN-2	19	INPUT
10	GND	GND		
11	H2 IN-1	H3 IN-2	18	INPUT
12	GND	GND		
13	H1 IN-1	H1 IN-2	17	INPUT
14	GND	GND		
15	TMR IN-1	TMR IN-2	16	INPUT
16	GND	GND		
17	PB7-1	PB7-2	15	
18	GND	GND		
19	PB6-1	PB6-2	14	
20	GND	GND		
21	PB5-1	PB5-2	13	
22	GND	GND		
23	PB4-1	PB4-2	12	INPUT or OUTPUT as a group
24	GND	GND		
25	PB3-1	PB3-2	11	
26	GND	GND		
27	PB2-1	PB2-2	10	
28	GND	GND		
29	PB1-1	PB1-2	9	
30	GND	GND		
31	PB0-1	PB0-2	8	
32	GND	GND		
33	PA7-1	PB7-2	7	
34	GND	GND		
35	PA6-1	PB6-2	6	
36	GND	GND		
37	PA5-1	PB5-2	5	
38	GND	GND		
39	PA4-1	PB4-2	4	INPUT or OUTPUT as a group
40	GND	GND		
41	PA3-1	PB3-2	3	
42	GND	GND		
43	PA2-1	PB2-2	2	
44	GND	GND		
45	PA1-1	PB1-2	1	
46	GND	GND		
47	PA0-1	PB0-2	0	
48	GND	GND		
49	--------- Not Connected		----------	----------
50	GND	GND		

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2.5.2 Pl and P2 Connectors

Connectors PI and P2 are mounted at the rear edge of the board (see Figure 2-1). The pin connections for Pl (a 96-pin, 3-row connector) contains the standard address, data, and control signals necessary for the operation of VMEbus-defined NEXP modules. (The signal definitions and pin-outs for the connector are found in Appendix A of this manual.) The Pl connector is designed to mechanically interface with a VMEbus defined Pl backplane.

2.5.3 P2 Connector XVME-290/l

The P2 connector is a standard VMEbus P2 backplane connector with 96-pins (3 rows). (The pin-outs for the connector P2 are found in Appendix A of this manual.) The P2 connector is designed to interface with a VMEbus defined P2 backplane. The P2 connector has been modified slightly for the XVME-290/l (see Table 2-7).

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Table 2-7. Pin Assignment for P2 (XVME-290/l Only)

ROW A		ROW B		ROW C	
Pin #	Signal	Pin #	Signal	Pin #	Signal
P2A-1	H4 OUT-1	P2B-1	v c c	P2C-1	GND
P2A-2	TMR OUT-1	P2B-2	GND	P2C-2	H2 OUT-l
P2A-3	H2 IN-l	NO	CONNECT	P2C-3	GND
P2A-4	Hl IN-1	NO	CONNECT	P2C-4	H3 IN-l
P2A-5	TMR IN-1	NO	CONNECT	P2C-5	GND
P2A-6	PB6- 1	NO	CONNECT	P2C-6	PB7-1
P2A-7	PB5-1	NO	CONNECT	P2C-7	GND
P2A-8	PB3- 1	NO	CONNECT	P2C-8	PB4- l
P2A-9	PB2-1	NO	CONNECT	P2C-9	GND
P2A-IO	PBO- 1	NO	CONNECT	P2C-10	PBI-1
P2A-I 1	PA7-1	NO	CONNECT	P2C-11	GND
P2A-12	PAS-1	P2B-12	**GND**	P2C-12	PA6- 1
P2A-13	PA4- 1	P2B-13	v c c	P2C-13	GND
P2A-14	PA2- 1	NO	CONNECT	P2C-14	PA3-1
P2A-I 5	PAL1	NO	CONNECT	P2C-15	GND
P2A-16	GND	NO	CONNECT	P2C-16	PAO- l
P2A-17	H4 OUT-2	NO	CONNECT	P2C-17	GND
P2A-18	TMR OUT-2	NO	CONNECT	P2C-18	H2 OUT-2
P2A-19	H2 IN-2	NO	CONNECT	P2C-19	GND
P2A-20	Hl IN-2	NO	CONNECT	P2C-20	H3 IN-2
P2A-2 1	TMR IN-2	NO	CONNECT	P2C-2 1	GND
P2A-22	PB6-2	P2B-22	GND	P2C-22	PB7-2
P2A-23	PB5-2	NO	CONNECT	P2C-23	GND
P2A-24	PB3-2	NO	CONNECT	P2C-24	PB4-2
P2A-25	PB2-2	NO	CONNECT	P2C-25	GND
P2A-26	PBO-2	NO	CONNECT	P2C-26	PBl-2
P2A-27	PA7-2	NO	CONNECT	P2C-27	GND
P2A-28	PA5-2	NO	CONNECT	P2C-28	PA6-2
P2A-29	PA4-2	NO	CONNECT	P2C-29	GND
P2A-30	PA2-2	NO	CONNECT	P2C-30	PA3-2
P2A-3 1	PAl-2	P2B-3 1	GND	P2C-3 I	GND
P2A-32	GND	P2B-32	v c c	P2C-32	PAO-2

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2.6 MODULE INSTALLATION

XYCOM XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-200 DIO Module is a single-high, single-wide VMEbus module, and as such, only requires the Pl backplane. The XVME-290/l DIO Module uses the P2 of the VMEbus backplane, or through the two 50 pin connectors (JKl and JK2) mounted in the P2 area (XVME-290/2). In the XVME-290/l version, P2 carries all the signals for both PI/T #I and PI/T #2, while the XVME-290/2 version, JKl carries the signals for PI/T #l and JK2 carries the signals for PI/T #2.

CAUTION

Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.

Prior to installing a module, you should determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. (Please check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessable.

2) Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage.

3) Push the card slowly toward the rear of the chassis until the connectors engage (the card should slide freely in the plastic guides).

4) Apply straight-forward pressure to the handle located on the front panel of the module until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excessive pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

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5) Once the board is properly seated, it should be secured to the chassis by tightening the two machine screws at the extreme top and bottom of the board.

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Chapter 3

MODULE PROGRAMMING

3.1 INTRODUCTION

This chapter will briefly examine the addressing, and initialization procedures and constraints required when programming the XVME-200 and XVME-290 DIO Modules. In order to demonstrate the correct sequence of initialization for the ports and registers contained in the 68230 PI/T chips, two programming examples (with comments) have been incorporated in this chapter. For a complete explanation on how to program and maximize the functionality of the 68230 PI/T chip, refer to the accompanying 68230 Manual.

3.2 MODULE ADDRESSING

The XVME-200 and XVME-290 DIO Modules are designed to be addressed within the VMEbus-defined 64K short I/O address space. When the DIO Module is installed in the system it will occupy a 1K byte block of the short I/O address space. The base address decoding scheme for the XVME I/O modules is such that the starting address for each board resides on a 1K boundary. Thus, there are 64 possible locations (1K boundaries) in the short I/O address space which could be used as the base address for the DIO Module (refer to Section 2.4.1 for the list of base addresses and their corresponding jumper configurations).

The logical registers/ports utilized for the transfer of data on the XVME-200 and XVME-290 Modules are all contained within the 68230 PI/T devices. All register locations within the 68230 devices are given specific addresses which are offset from the module base address (Table 3-1 lists the offsets specified for the registers used in the 68230 chips).

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Table 3-l. Register Offsets From the Module Base Address

68230 PI/T Register Offsets from Module Base Address				
PI/T #1		PI/T #2		
DEC	HEX	DEC	HEX	PI/T Register Name
1	1	65	41	Port General Control Register
3	3	67	43	Port Service Request Register
5	5	69	45	Port A Data Direction Register
7	7	71	47	Port B Data Direction Register
9	9	73	49	Port C Data Direction Register
11	B	75	4B	Port Interrupt Vector
13	D	77	4D	Port A Control Register
15	F	79	4F	Port B Control Register
17	11	81	51	Port A Data Register
19	13	83	53	Port B Data Register
21	15	85	55	Port A Alternate Register
23	17	87	57	Port B Alternate Register
25	19	89	59	Port C Data Register
27	1B	91	5B	Port Status Register
29	1D	93	5D	Null
31	1F	95	5F	Null
33	21	97	61	Timer Control Register
35	23	99	63	Timer Interrupt Vector
37	25	101	65	Null
39	27	103	67	Counter Preload High
41	29	105	69	Counter Preload Middle
43	2B	107	6B	Counter Preload Low
45	2D	109	6D	Null
47	2F	111	6F	Count Register High
49	31	113	71	Count Register Middle
51	33	115	73	Count Register Low
53	35	117	75	Timer Status Register
55	37	119	77	Null — Null Registers Always
57	39	121	79	Null — Read Zero. Writing
59	3B	123	7B	Null — To A Null Register
61	3D	125	7D	Null — Has No Effect On
63	3F	127	7F	Null — The Module.

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A specific register address in one of the 68230 chips can be accessed by simply adding the specific register offset to the module base address. For example, the offset specified for the Port General Control Register for PI/T #2 is 41H, and if the module base address is jumpered to 1000H, the register can be accessed at 1041H.

Module Base Address	Register Offset		PCG Register #2
1000H	41H	=	1041H

NOTE

The XVME-200/290 are an odd byte only slave, and as such, the module will not respond to even address, single-byte accesses. However, word accesses may be used, with the understanding that only the odd byte of the word is used to exchange data. If word accesses are used, the register offsets listed in Table 3-l would all be decremented by 1.

Figure 3-l shows a simple map of the 1K block of the short I/O address space which is occupied by the XVME-200/290 Modules.

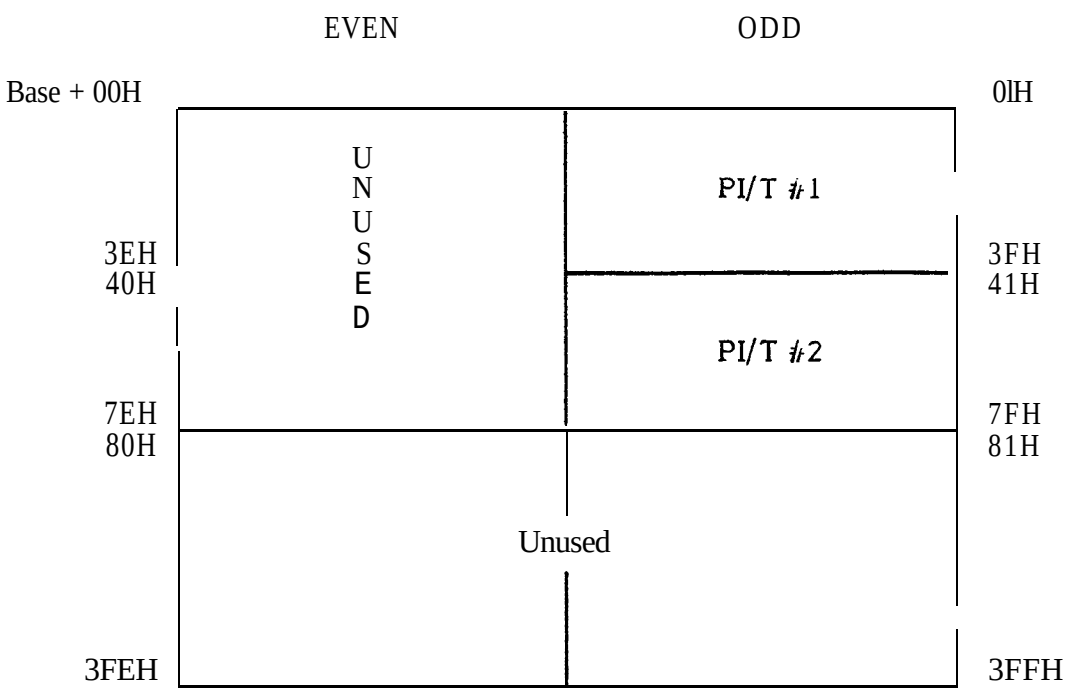


Figure 3-1. Memory Map of the XVME-200 and XVME-290 Modules

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Figure 3-2 is a model of the registers internal to each 68230 PI/T chip. Notice that the register model includes a "register value after reset" for each register, as well as "register select bits" for each register (see the **NOTE** immediately following Figure 3-2).

Register Select Bits 5 4 3 2 1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
0 0 0 0 0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	0 0	Port General Control Register
0 0 0 0 1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			0 0	Port Service Request Register
0 0 0 1 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port A Data Direction Register
0 0 0 1 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port B Data Direction Register
0 0 1 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port C Data Direction Register
0 0 1 0 1	Interrupt Vector Number						*	*	0 F	Port Interrupt Vector Register
0 0 1 1 0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	0 0	Port A Control Register
0 0 1 1 1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	0 0	Port B Control Register
0 1 0 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0 1 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0 1 0 1 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0 1 0 1 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0 1 1 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0 1 1 0 1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0 1 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
0 1 1 1 1	*	*	*	*	*	*	*	*	0 0	(Null)

*Unused, read as zero
**Value before RESET
***Current value on pins
****Undetermined value

Register Select Bits 5 4 3 2 1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
1 0 0 0 0	TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable	0 0	Timer Control Register
1 0 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 F	Timer Interrupt Vector Register
1 0 0 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 0 0 1 1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Counter Preload Register (High)
1 0 1 0 0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Counter Preload Register (Mid)
1 0 1 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Counter Preload Register (Low)
1 0 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 0 1 1 1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Count Register (High)
1 1 0 0 0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Count Register (Mid)
1 1 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Count Register (Low)
1 1 0 1 0	*	*	*	*	*	*	*	ZDS	0 0	Timer Status Register
1 1 0 1 1	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 0 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 0 1	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 1 1	*	*	*	*	*	*	*	*	0 0	(Null)

*Unused, read as zero
**Value before RESET

Figure 3-2. 68230 Register Model

NOTE

The "register select bits" values shown in Figure 3-2 are intended for the 68230 chip in a stand-alone perspective, and are not representative of the addressing logic included on the XVME-200 and XVME-290 DIO Modules. All registers are accessed on the XVME-200 and XVME-290 Modules by using the offsets shown in Table 3-1 added to the module base address (refer to the example on page 3-3).

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3.3 MODULE VMEbus INTERRUPT CAPABILITY

Four sources of interrupts exist on the XVME-200 and the XVME-290. These are the timer and port interrupt sources from both PI/T #l and PI/T #2. When enabled, each of the four interrupt sources can generate VMEbus interrupts on the level selected by jumpers JAI-JA3 (refer to Section 2.4.3 of this manual). The four local interrupt sources are prioritized during the VMEbus IACK cycle. Table 3-2 shows the priority of the four local interrupt sources.

Table 3-2. Priority of Local Interrupt Sources

PI/T #l Port Interrupt	Highest Priority
PI/T #2 Port Interrupt	
PI/T #l Timer Interrupt	
PI/T #2 Timer Interrupt	Lowest Priority

When the module responds to a VMEbus IACK cycle, the IACK vector is acquired from the corresponding PI/T vector register (refer to the 68230 Manual for location and operation) and driven onto the VMEbus. Each PI/T device produces 5 different vectors, 4 from the ports and 1 from the timer. Thus, ten different VMEbus IACK vectors can be provided by the XVME-200 and XVME-290 Modules. The appropriate PI/T IACK vector registers must be initialized before interrupts are enabled (refer to 68230 Manual).

3.3.1 Module VMEbus Interrupt Enabling

As mentioned in the previous section, the ports and timer of both PI/T devices have the capability of generating VMEbus interrupts. The following subsections explain the general procedure for enabling the port and timer interrupts.

3.3.1.1 Port C/Alternate Function Initialization

Basically, the interrupt initialization procedures begin by programming the Port C/Alternate function lines on the PI/T devices to carry the interrupt control functions. The operation of the Port C/Alternate function lines is covered in depth in the 68230 Manual, however, for the sake of clarity Figure 3-3 is included in this manual. Figure 3-3 defines the Port C/Alternate function lines and their programmed direction for primary module use. Notice that some of the pins retain the possibility of being used as Port C single-bit inputs/outputs if the module interrupt and timer capabilities are not being used (i.e., pins 1 and 3), while others must be dedicated to module control functions (i.e., pins 0 and 1 should always be programmed as outputs to control the direction of the Port A and B data buffers, and pins 4, 5, 6, and 7 are dedicated to timer and port interrupt control).

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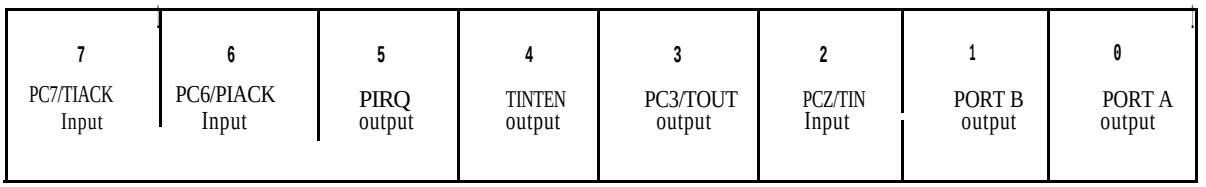


Figure 3-3. Port C/Alternate Function Signal Definitions

The following is a brief explanation of each PORT C bit:

Bits 0 and 1 are used to control the direction of the 8-bit data transceivers which are used to buffer the Port A and Port B data lines. After start-up or reset, these bits should be programmed as outputs.

Bit 2 is used as a timer input line if the 68230 timer function is being utilized. If the timer function is not being used, this bit could be employed as a general purpose input line.

Bit 3 is used as a timer output line if the 68230 timer function is being utilized. If the timer function is not being used, this bit could be employed as a general purpose output line.

Bit 4 is used as a timer interrupt enable line of the 68230 timer function is being utilized. This bit can only be used for the timer interrupt function.

Bit 5 is used as a port interrupt request line if the 68230 port interrupts are enabled. This bit can only be used for the port interrupt function.

Bit 6 is used as a port interrupt acknowledge line if the 68230 port interrupts are enabled. This bit can only be used for the port interrupt function.

Bit 7 is used as a timer interrupt acknowledge line if the 68230 timer functions are being utilized. This bit can only be used for the timer interrupt function.

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During a VMEbus reset, all three PI/T ports (A, B, & C) assume an input direction. Pull-up resistors present on bits PC0 and PC1 cause the port A and B data line transceivers to assume an input direction. Pull-up resistors also cause PORT C pins 3, 4, and 5 to go high at reset, thereby preventing the possibility of unintentional interrupts (port or timer). After reset, PORT C can be configured to conform to the users needs (i.e., Port A and B transceiver direction, port and timer interrupt control signals and timer I/O lines, and/or single-bit general purpose I/O). Figure 3-2 shows the direction for each PORT C pin as dictated by hardware configuration. Some attention should be given to the possibility of generating unintentional interrupts when configuring the direction of the PORT C pins. The following procedure is an example of how PORT C could be initialized to appear as it does in Figure 3-2.

1) Write FFH to the PORT C Data register. This ensures that all PORT C pins will be high when the direction of the pins is switched, thereby preventing the possibility of unintentional interrupts (both port and timer) being generated.

2) Write 1BH to the PORT C Direction register. This will configure the direction of PORT C as shown in Figure 3-2, with the exception of pin 5 (PIRQ), which remains an input to ensure that port interrupts will not be generated unintentionally.

3) Individual PORT C bits can now be programmed to conform to the user's needs. At this point, port interrupts could be enabled by merely programming the PC6/PIACK and PC5/PIRQ pins to support the interrupt and acknowledge functions.

3.3.1.2 PI/T Port Interrupt Enabling

In order to enable the PI/T port interrupt capability PORT C must be programmed so that pins PC5/PIRQ and PC6/PIACK serve the port interrupt request and acknowledge functions. As such, the individual internal enable bits for Hl, H2, and H3 determine whether a particular port function will generate a VMEbus interrupt.

NOTE

Handshake line H4 must be programmed as an output, and H4 interrupts must always be disabled.

When H2 interrupts are to be used, input pin H2 must be physically jumpered to configure the line for inputs (refer to Section 2.4.5 of this manual for H2 jumper definitions). During the interrupt service routine, the "Direct Method" of clearing the Hl, H2, or H3 status bits must be used to negate the interrupt (refer to the 68230 Manual for the "Direct Method" of clearing status bits).

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3.3.1.3 PI/T Timer Interrupt Enabling

68230 timer interrupts are enabled/disabled via PORT C output pin PC4. When PC4 is negated (logic 'l"), the timer cannot generate VMEbus interrupts. When PC4 is asserted (logic "0"), the timer will generate VMEbus interrupts.

When the timer interrupts are to be used, PORT C pins PC3/TOUT and PC7/TIACK must be programmed to serve the timer interrupt request and acknowledge functions. Pin PC4 is then used to determine whether timer interrupts are enabled or disabled. All interrupt related PORT C pins are connected to pull-up resistors, so that when the module is reset all PORT C lines will be configured as inputs and thus, all module interrupts will be disabled.

During the interrupt service routine, the 'Direct Method" must be used for clearing the timer zero detect status bit in order to negate the interrupt (refer to the 68230 Manual for information on the "Direct Method" of clearing the timer).

When the timer interrupts are not going to be used, pin PC4 must be negated (logic "1') in order to disable timer interrupts. In these cases, pin PC3/TOUT can be programmed either as a simple timer output or as a general purpose PORT C output line.

3.4 PI/T PORT A AND PORT B DATA LINES

The I/O lines connected to the PI/T I/O pins are labeled PA0-PA7 and PB0-PB7 (refer to Figure 1-1 of this manual). The PORT A and B data lines are independently buffered by 8-bit transceivers. The 8 I/O lines assigned to each port must all assume the same direction. Thus, all I/O lines in PORT A must assume the same direction, and all the data lines in PORT B must assume the same direction. PORTS A and B may however, assume different directions.

The direction of the 8-bit data transceivers which buffer each port is programmed independent of the direction of the PORT I/O lines on the PI/T chips. The direction of the data transceivers is programmed via the PORT C outputs PCO and PCl. The state of the PCO and PC1 outputs should be programmed to be consistent with the programmed direction of the PI/T ports.

When programming a port for output the direction of the transceiver and the port should be set in the following sequence:

1) Set the direction of the data transceiver.
2) Set the direction of the PI/T Port.

When programming a port for input the direction of the port and transceiver should be set in the following sequence:

1) Set the direction of the PI/T Port.
2) Set the direction of the data transceiver.

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Table 3-3 shows how pins PC0 and PC1 affect the direction of the PORT A and B data transceivers. Remember, each PI/T chip has its own PORT A and B, and thus there is a total of 4 lines which are used to control the direction of the four data transceivers (refer to the Module Block Diagram, Figure l-l).

Table 3-3. PORT A and B Data Transceiver Direction Control *

PC0 output	PC1 output	Data Line Transceiver Direction
0	--	PA0-PA7 are OUTPUTS
1	--	PA0-PA7 are INPUTS
--	0	PB0-PB7 are OUTPUTS
--	1	PB0-PB7 are INPUTS

* These directions are the same for both PI/T chips.

CAUTION

PI/T pins PA0-PA7 must all be programmed to assume the same direction, this direction must be consistent with PC0 as shown in Table 3-3. PI/T pins PBO-PB7 must all be programmed to assume the same direction, this direction must be consistent with PC1 as shown in Table 3-3. Failure to observe these conventions will cause signal contention.

3.4.1 Port A and B Reset State

During a VMEbus reset, PI/T PORTS A, B, and C all assume an input direction. Therefore, I/O signals PAO-PA7 and PBO-PB7 all assume an input direction during a reset. This means that if the I/O signals are being used in an application as outputs, they will have a "high" reset state. Thus, active "low" outputs would have to be used on lines which must be negated on power-up or system reset. The receivers of these active "low" outputs should limit their I_{ih} value below 250uA to guarantee that they will be negated upon reset.

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3.5 PROGRAMMKNG EXAMPLES

The two 68000 CPU code programming examples which follow, demonstrate general methods of initialization of the 68230 PI/T devices on the XVME-200 and XVME-290 Modules. The following equates will be used in both examples:

```
; Interrupt vectors.

PVCTR   EQU $___; Port interrupt vector.
TVCTR   EQU $___; Timer interrupt vector.


; Values to preload counter.
CHIGH   EQU $___ ; High byte.
CMID    EQU $___ ; Middle byte.
CLOW    EQU $___ ; Low byte.

; 68230 Base Address and Register Offsets.

BASE200 EQU $_______ ; XVME-200 Module base address
                     (jumper selectable).
PI/TlBASEQU  BASE200 + $00; 68230 PI/T #l base address.
PI/T2BASEQU  BASE200 + $40; 68230 PI/T #2 base address.

PCGR    EQU $01  ; Port general control register.
PSRR    EQU $03  ; Port service request register.
PADDR   EQU $05  ; Port A data direction register.
PBDDR   EQU $07  ; Port B data direction register.
PCDDR   EQU $09  ; Port C data direction register.
PIVR    EQU $0B  ; Port interrupt vector register.
PACR    EQU $OD  ; Port A control register.
PBCR    EQU $0F  ; Port B control register.
PADR    EQU $ll  ; Port A data register.
PBDR    EQU $13  ; Port B data register.
PAAR    EQU $15  ; Port A alternate register
PBAR    EQU $17  ; Port B alternate register.
PCDR    EQU $19  ; Port C data register.
PSR     EQU $lB  ; Port status register.
TCR     EQU $21  ; Timer control register.
TIVR    EQU $23  ; Timer interrupt vector register.
CPRH    EQU $27  ; Counter preload register - high byte.
CPRM    EQU $29  ; Counter preload register - mid byte.
CPRL    EQU $2B  ; Counter preload register - low byte.
CNTRH   EQU $2F  ; Count register - high byte.
CNTRM   EQU $31  ; Count register - mid byte.
CNTRL   EQU $33  ; Count register - low byte.
TSR     EQU $35  ; Timer status register.
```


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Example #1

Basic Set Up:

PI/T #1
Mode 0 = Unidirectional 8-bit Mode
Submode 1X = Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

Goals:

1) Port A, all bits = non-latched inputs.
2) Port B, all bits = single buffered outputs.
3) Port C, bit 0 = single buffered output (controls the direction of the transceiver connected to Port A).
4) Port C, bit 1 = single buffered output (controls the direction of the transceiver connected to Port B).
5) Port C, bit 2 = non-latched input.
6) Port C, bit 3 = single-buffered output (high).
7) Port C, bit 4 = single-buffered output (programmed high to disable timer interrupts).
8) Port C, bit 5 = PIRQ* function.
9) Port C, bit 6 = PIACK* function.
10) Port C, bit 7 = non-latched input (will always read as one).
11) The handshake pins (H1,H2,H3,H4) are at a low voltage level when negated, and at a high voltage level when asserted.
12) H1 is an edge-sensitive status input, H1S is set by an asserted edge of H1.
13) H2 is a negated output pin and H2S is always cleared.
14) H3 is an edge-sensitive status input, H3S is set by an asserted edge of H3.
15) H4 is an asserted output pin and H4S is always cleared.
16) All interrupts are disabled.
17) The timer is disabled.

CODE:

```
M0VEA.L  # PI/T1BASE,AO      ; A0 = base address of PI/T #1

M0VE.B   #$FF,PCDR(AO)       ; Initialize Port C control
M0VE.B   #$1 B,PCDDR(AO)     ; functions
                             ; Port A '& B transceivers = output
                             ; PC3/TOUT = high
                             ; PC4 = high (timer interrupts disabled)
                             ; PC7,6,5,2 = inputs

M0VE.B   #$OF,PGCR(AO)       ; Port mode = 0
                             ; H34,H12 interrupts disabled
                             ; Handshake pins = active high

MOVE.B   #$AO,PACR(AO)       ; Initialize Port A
                             ; Submode 1X
                             ; H2 = negated output
                             ; HI & H2 interrupts disabled
```


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```
M0VE.B    #$AS,PBCR(AO)        ; Initialize Port B
                               ; Submode 1X
                               ; H4 = asserted output
                               ; H3 & H4 interrupts disabled

M0VE.B    #$18,PSRR(AO)        ; PC4 = Port C function
                               ; PCS/PIRQ = PIRQ function
                               ; PC6/PIACK = PIACK function

                               ; Set Port A & B direction
M0VE.B    #O,PADDR(AO)         ; Port A = input mode
M0VE.B  #$FF,PBDDR(AO)         ; Port B = output mode
BCLR      #O,PCDR(AO)          ; Port A transceiver = input mode

M0VE.B    #O,TCR(AO)           ; PC2, PC3 & PC7 = Port C function
                               ; timer disabled
```

After this initialization code is executed, PI/T #1 Port A data register will reflect the state of PA7-1 through PAO-I. Data written to PI/T #I Port B will appear on PB7-1 through PBO-I.

Example #2

Basic Set Up:

PI/T #2
Mode 1 = Unidirectional 16-bit Mode
Submode X1 = Pin-Definable Double-Buffered Output or Non-Latched Input

Goals:

1) Port A and B, all bits = double buffered outputs.
2) Port C, bit 0 = single buffered output (controls the direction of the transceiver connected to Port A).
3) Port C, bit 1 = single buffered output (controls the direction of the transceiver connected to Port B).
4) Port C, bit 2 = TIN function. The prescaler will not be used. The signal TIN will be used to decrement the counter.
5) Port C, bit 3 = TOUT function.
6) Port C, bit 4 = single-buffered output (controls the timer interrupt enable).
7) Port C, bit 5 = PIRQ* function.
8) Port C, bit 6 = PIACK* function.
9) Port C, bit 7 = TIACK* function.
10) The handshake pins (Hl,H2,H3,H4) are at a low voltage level when negated, and at a high voltage level when asserted.
11) Hl is an edge-sensitive input, HIS is set by an asserted edge of Hl, and Hl interrupt is enabled.
12) H2 is an edge-sensitive input, and H2S is set by an asserted edge of H2, and H2 interrupt is disabled.
13) H3 and H4 set up for interlocked output handshake protocol.
14) H4 interrupt is disabled.
15) Timer is set up to interrupt after timeout (and started).

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16) Vectored interrupts are supported.
17) When zero is detected, the counter will generate a VMEbus interrupt, reload the counter, and continue counting.
18) Hl, H2, H3, and timer interrupts are enabled.

CODE:

```
M0VEA.L  #PI/T2BASE,AO      ; A0 = base address of PI/T #l

M0VE.B   #O,TCR(  AO)       ; Disable timer

M0VE.B   #$FF,PCDR(AO)      ; Initialize Port C functions
M0VE.B   #$l B,PCDDR(AO)    ; Port A & B transceivers = output
                            ; PC3/TOUT = high
                            ; PC4 = high (timer interrupts disabled)
                            ; PC7,6,5,2 = inputs

M0VE.B   #$4F,PGCR(AO)      ; Port mode = 1
                            ; H34,H12 interrupts disabled
                            ; Handshake pins = active high

M0VE.B   #$06,PACR(AO)      ; Initialize Port A
                            ; Submode Xl
                            ; H2 = edge sensitive input
                            ; Hl & H2 interrupts enabled

M0VE.B   #$32,PBCR(AO)      ; Initialize Port B
                            ; Submode X1
                            ;       = port handshake function
                              H4 interrupts disabled
                              H3 interrupts enabled

M0VE.B   #$18,PSRR(AO)      ; PC4 = Port C function
                            ; PCS/PIRQ = PIRQ function
                            ; PC6/PIACK = PIACK function

MOVE.B   #$FF,PADDR(AO)     ; Port A = output
M0VE.B   #$FF,PBDDR(AO)     ; Port B = output

M0VE.B  #PVCTR,PIVR(AO)     ; Set up port IACK vector

 ORI.B   #$30,PGCR(A0)      ; H34 & H12 interrupts enabled

                            ; Timer setup
M0VE.B     #$A6,TCR(AO)     ; PC3/TOUT = TOUT function
                            ; PC7/TIACK = TIACK function
                            ; Counter reloads on zero detect
                            ; PC2/TIN = TIN function
                            ; Timer disabled
```


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```
M0VE.B   #CHIGH,CPRH(AO)  ; Initialize counter preload registers
M0VE.B   #CMID,CPRM(AO)
M0VE.B   #CLOW,CPRL(AO)

M0VE.B   #TVCTR,TIVR(AO)  ; Initialize timer IACK vector

BCLR#4,PCDR(AO)           ; Set PC4 = 0 to enable timer interrupts

BSET#O,TCR(AO)            ; Enable timer
```


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Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-200 and XVME-290 Modules are VMEbus compatible boards. There is one 96-pin bus connector on the rear edge of the board labeled Pl (refer to Chapter 2, Figure 2-1 for the location) and the XVME-290/l also uses the P2 connector. The signals carried by connector Pl are the standard address, data, and control signals required for a Pl backplane interface, as defined by the VMEbus specification. Table A-1 identifies and defines the signals carried by the Pl connector. Table A-3 shows the pin-outs for the P2 connector.

Table A-l. Pl - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	lA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AMO-AM5	1A:23 lB:16,17, 18,19 lC:14	ADDRESS MODIFIER (bits O-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	lA:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A0l-A23	1A:24-30 lC:15-30	ADDRESS BUS (bits l-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:l	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	lB:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:ll	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BGOIN*- BG3IN*	1B:4,6, 8,l0	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	1B:5,7, 9,ll	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	lA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSl*	lA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).
DTACK*	IA:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-Dl5	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22,31	GROUND

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQl*-IRQ7*	1B:24-30	INTERRUPT REQUEST (l-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	lC:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	1A:l0	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

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Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:l4	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5v	l.A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12v	lC:31	+12 VDC POWER: Used by system logic circuits.
-12v	lA:31	-12 VDC POWER: Used by system logic circuits.

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BACKPLANE CONNECTOR Pl

The following table lists the Pl pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DO0	BBSY *	DO8
2	D01	BCLR*	DO9
3	DO2	ACFAIL*	Dl0
4	DO3	BGOIN*	D11
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG20UT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

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Table A-3. Pin Assignment for P2 (XVME-290/l Only)

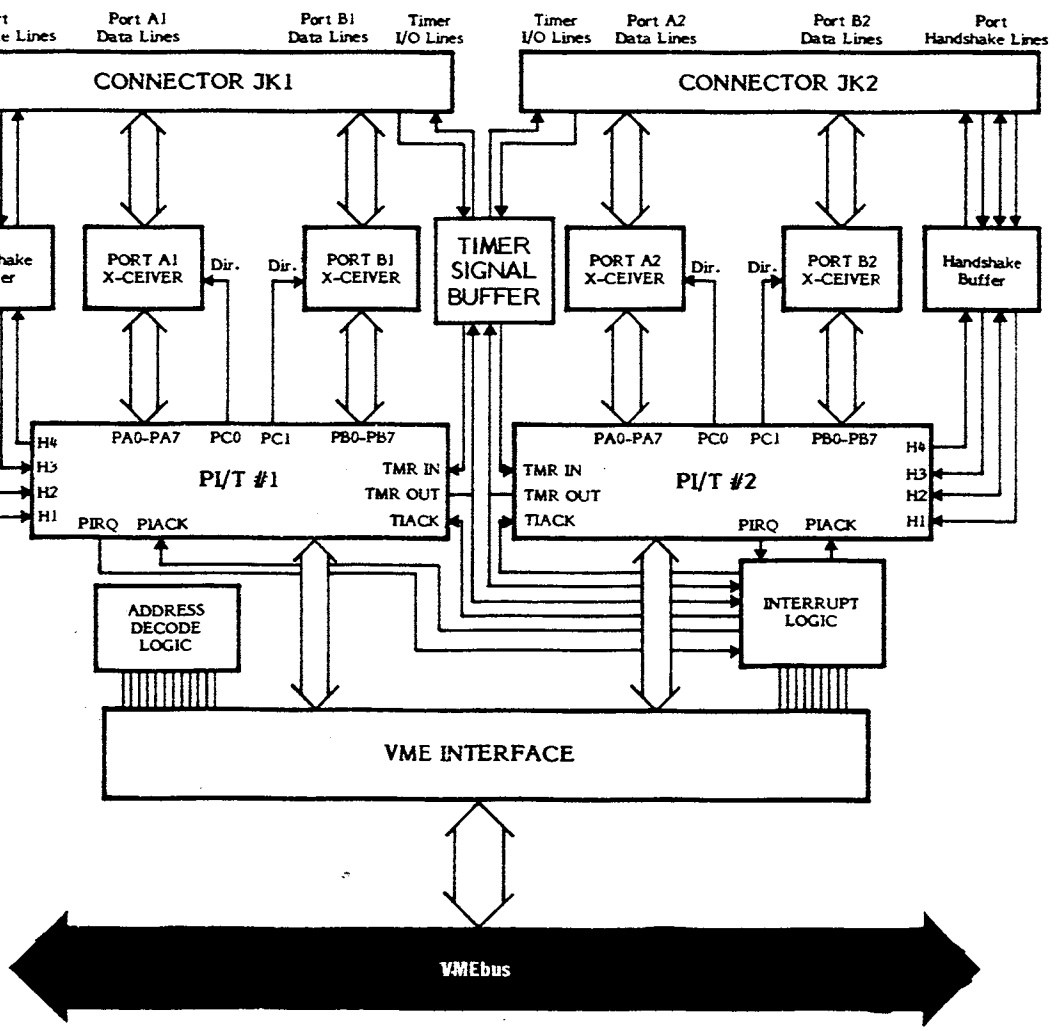
ROW A		ROW B		ROW C	
Pin #	Signal	Pin #	Signal	Pin #	Signal
P2A-1	H4 OUT-l	P2B-1	v c c	P2C-1	GND
P2A-2	TMR OUT-1	P2B2	GND	P2C-2	H2 OUT-l
P2A-3	H2 IN-l		NO CONNECT	P2C-3	GND
P2A-4	Hl IN-l		NO CONNECT	P2C-4	H3 IN-l
P2A-5	TMR IN-l		NO CONNECT	P2C-5	GND
P2A-6	PB6-1		NO CONNECT	P2C-6	PB7-1
P2A-7	PB5-1		NO CONNECT	P2C-7	GND
P2A-8	PB3-1		NO CONNECT	P2C-8	PB4-1
P2A-9	PB2- 1		NO CONNECT	P2C-9	GND
P2A-10	PBO- 1		NO CONNECT	P2C-10	PBl-I
P2A-11	PA791		NO CONNECT	P2C-11	GND
P2A-12	PA5- 1	P2B-12	GND	P2C-12	PA6-1
P2A-13	PA4- 1	P2B-13	v c c	P2C-13	GND
P2A-14	PA2- 1		NO CONNECT	P2C-14	PA3-1
P2A-15	PAl-1		NO CONNECT	P2C-15	GND
P2A-16	GND		NO CONNECT	P2C-16	PAO-1
P2A-17	H4 OUT-2		NO CONNECT	P2C-17	GND
P2A-18	TMR OUT-2		NO CONNECT	P2C-18	H2 OUT-2
P2A-19	H2 IN-2		NO CONNECT	P2C-19	GND
P2A-20	Hl IN-2		NO CONNECT	P2C-20	H3 IN-2
P2A-2 1	TMR IN-2		NO CONNECT	P2C-2 1	GND
P2A-22	PB6-2	P2B-22	GND	P2C-22	PB7-2
P2A-23	PB5-2		NO CONNECT	P2C-23	GND
P2A-24	PB3-2		NO CONNECT	P2C-24	PB4-2
P2A-25	PB2-2		NO CONNECT	P2C-25	GND
P2A-26	PB0-2		NO CONNECT	P2C-26	PBl-2
P2A-27	PA7-2		NO CONNECT	P2C-27	GND
P2A-28	PA5-2		NO CONNECT	P2C-28	PA6-2
P2A-29	PA4-2		NO CONNECT	P2C-29	GND
P2A-30	PA2-2		NO CONNECT	P2C-30	PA3-2
P2A-3 1	PAL2	P2B-3 1	GND	P2C-3 1	GND
P2A-32	GND	P2B-32	v c c	P2C-32	PA0-2

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Appendix B

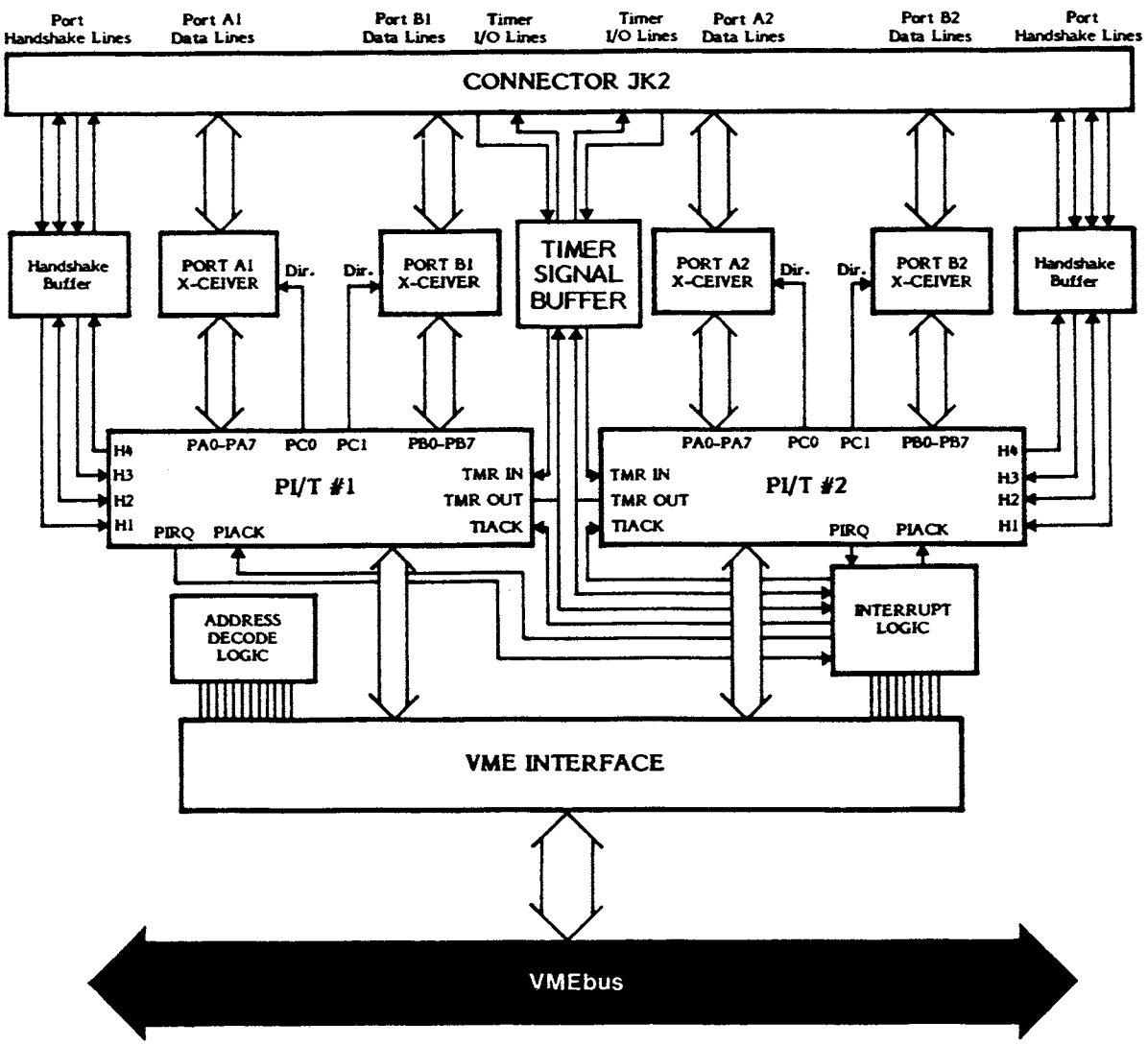
BLOCK DIAGRAM, ASSEMBLY DRAWING, & SCHEMATICS

Block Diagram (XVME-200 and XVME-290/2)



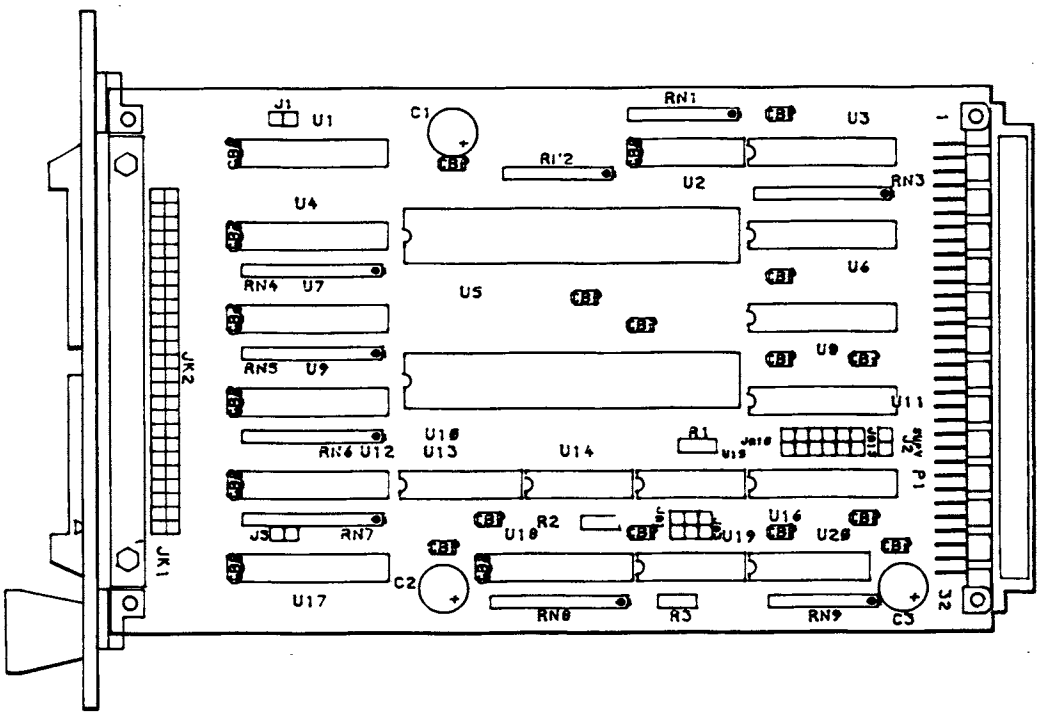
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Block Diagram (XVME-290/1)



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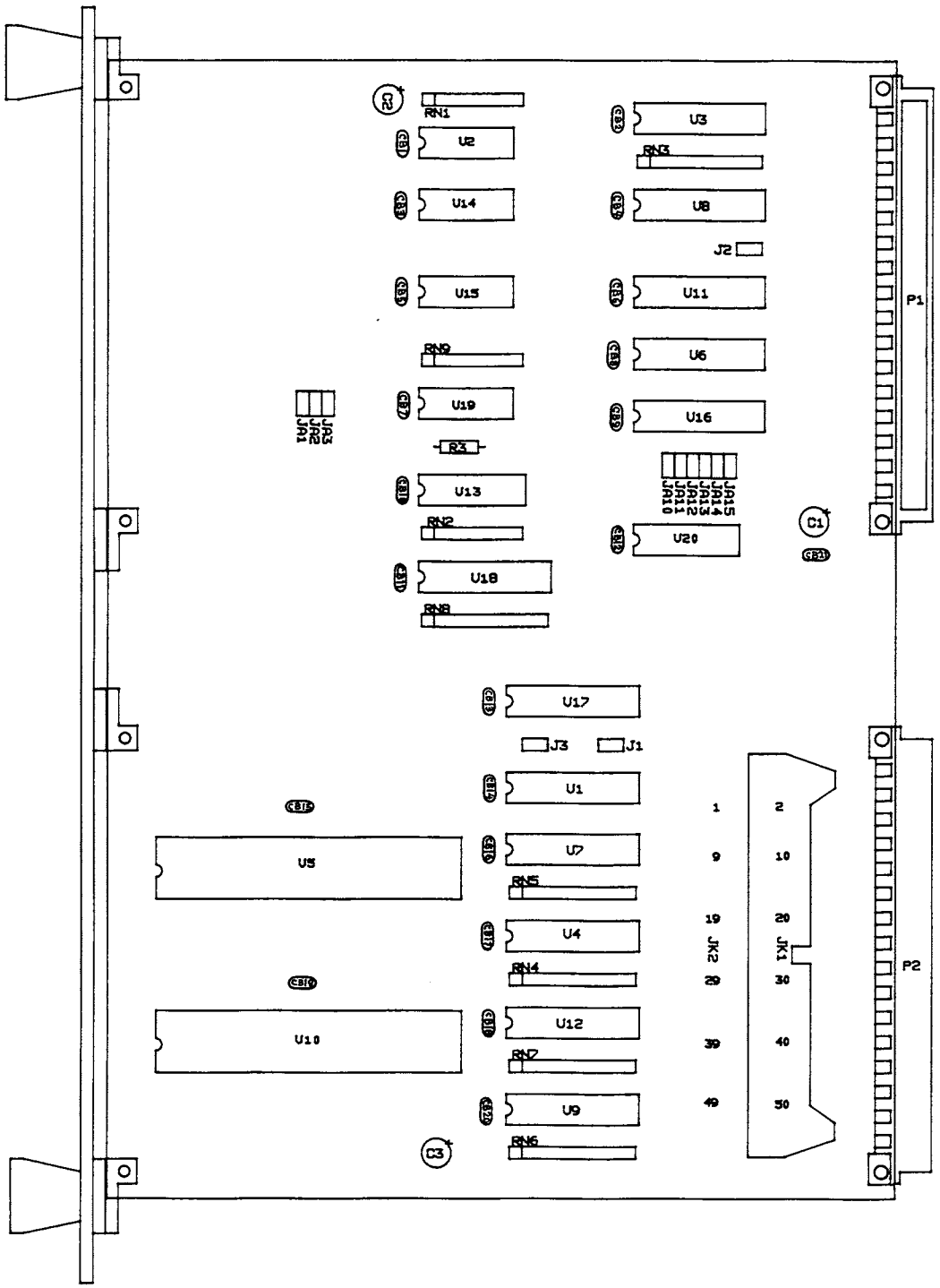
Assembly Drawing



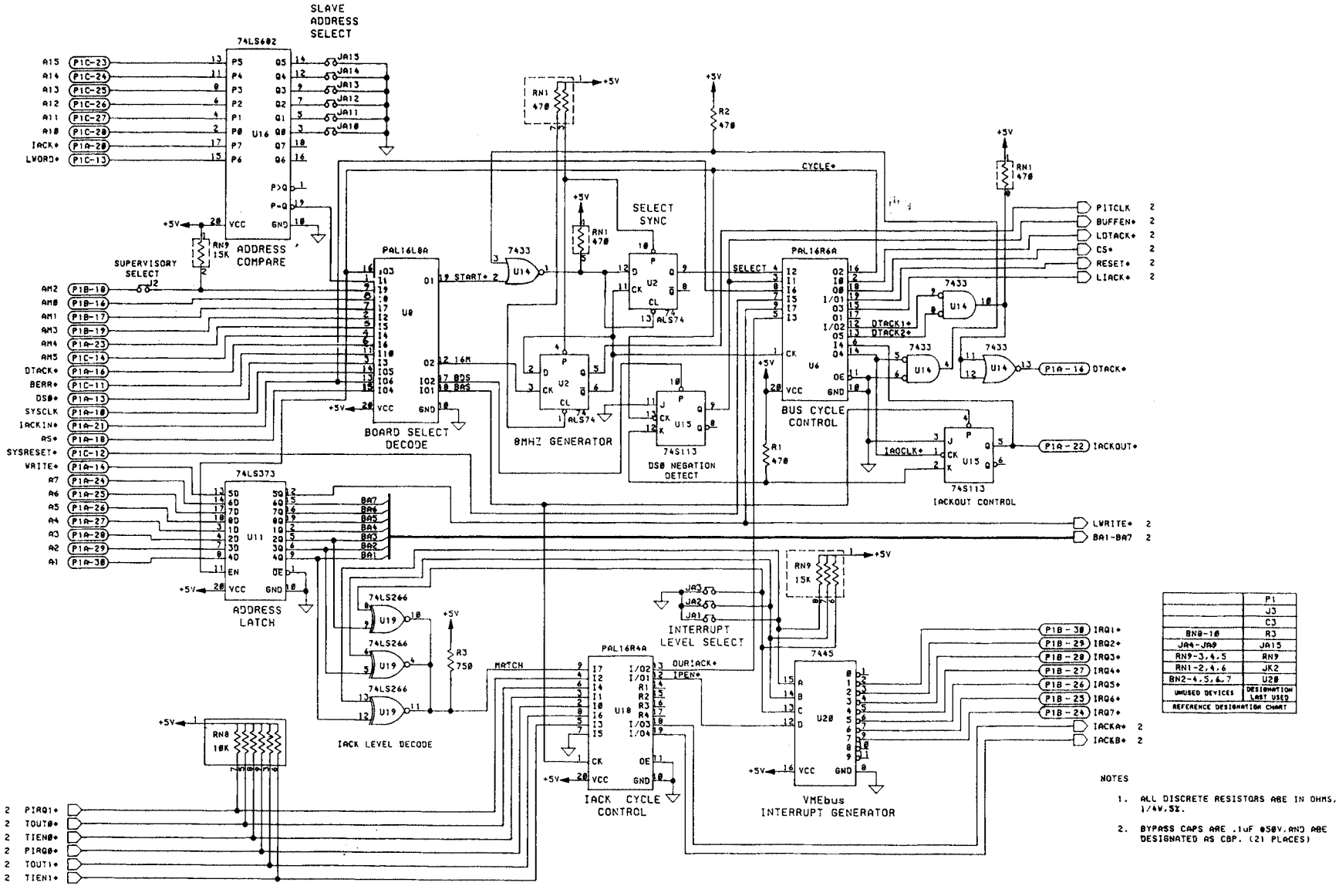
XVME-200

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Assembly Drawing



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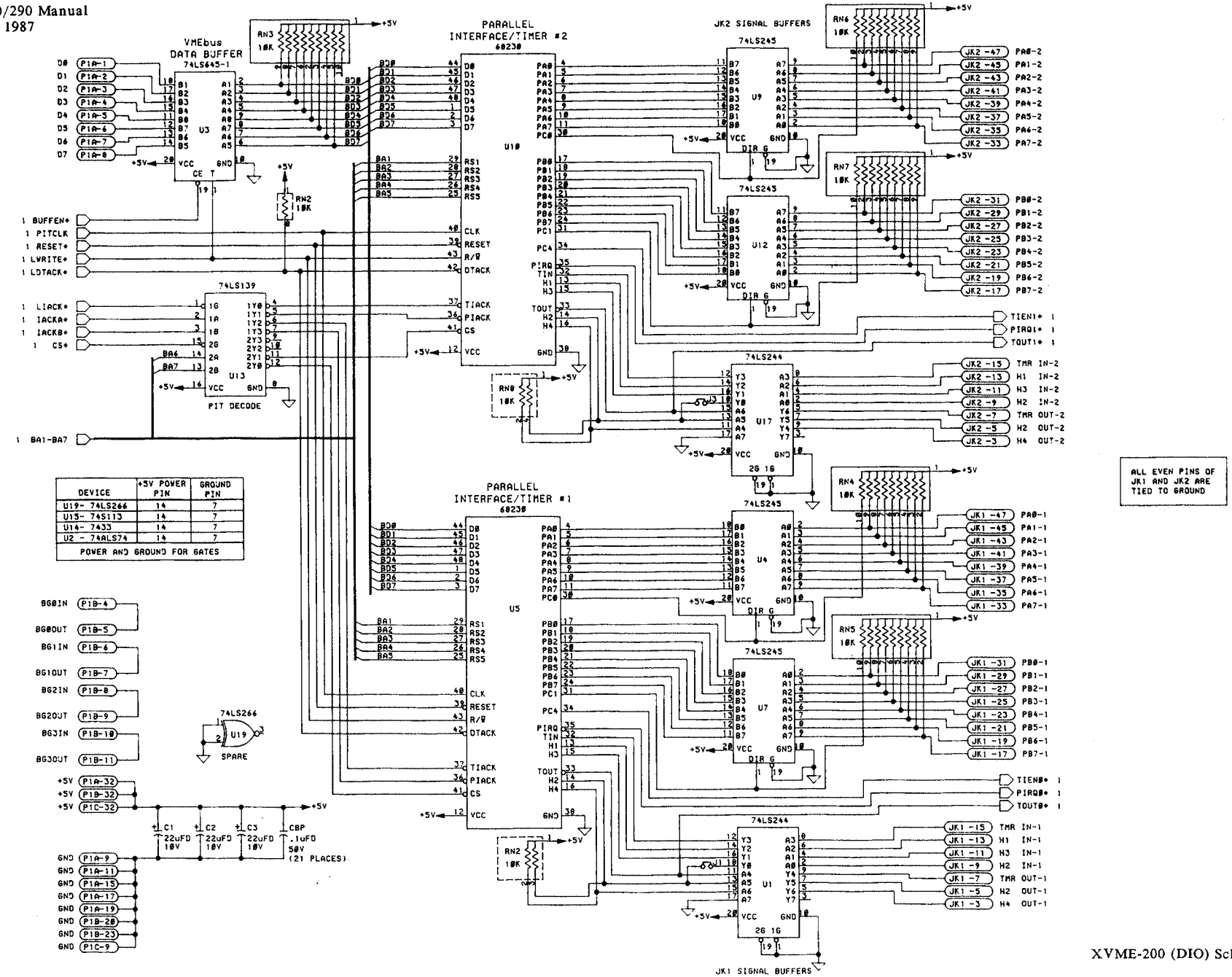


	P1
	J3
	C3
RN0-10	R3
JA4-JA9	JA15
RN9-3,4,5	RN9
RN1-2,4,6	JK2
RN2-4,5,6,7	U28
UNUSED DEVICES	DESIGNATION LAST USED
REFERENCE DESIGNATION CHART	

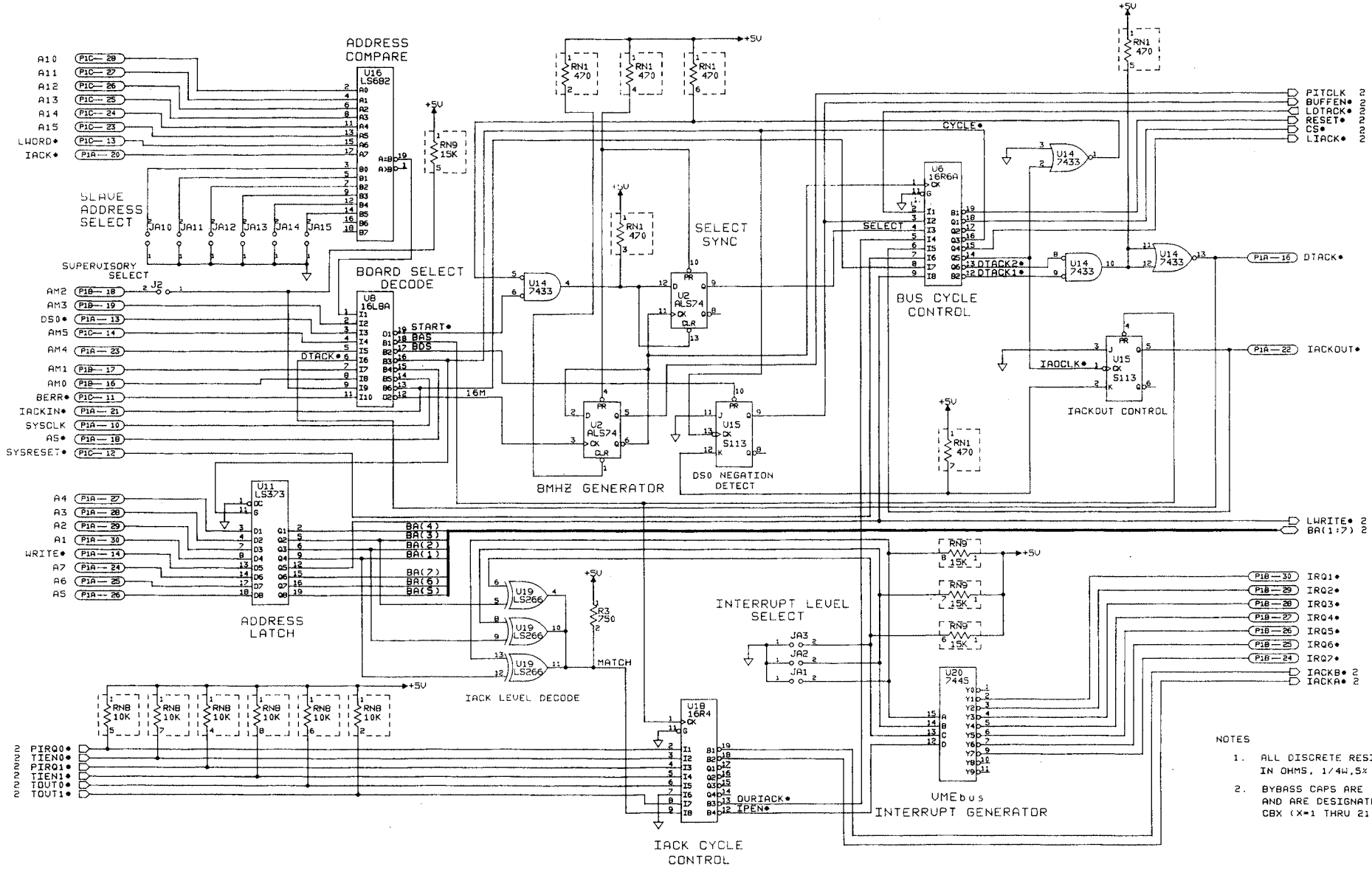
NOTES

1. ALL DISCRETE RESISTORS ARE IN OHMS, 1/4W,5%.
2. BYPASS CAPS ARE .1uF @50V,AND ARE DESIGNATED AS CBP. (21 PLACES)

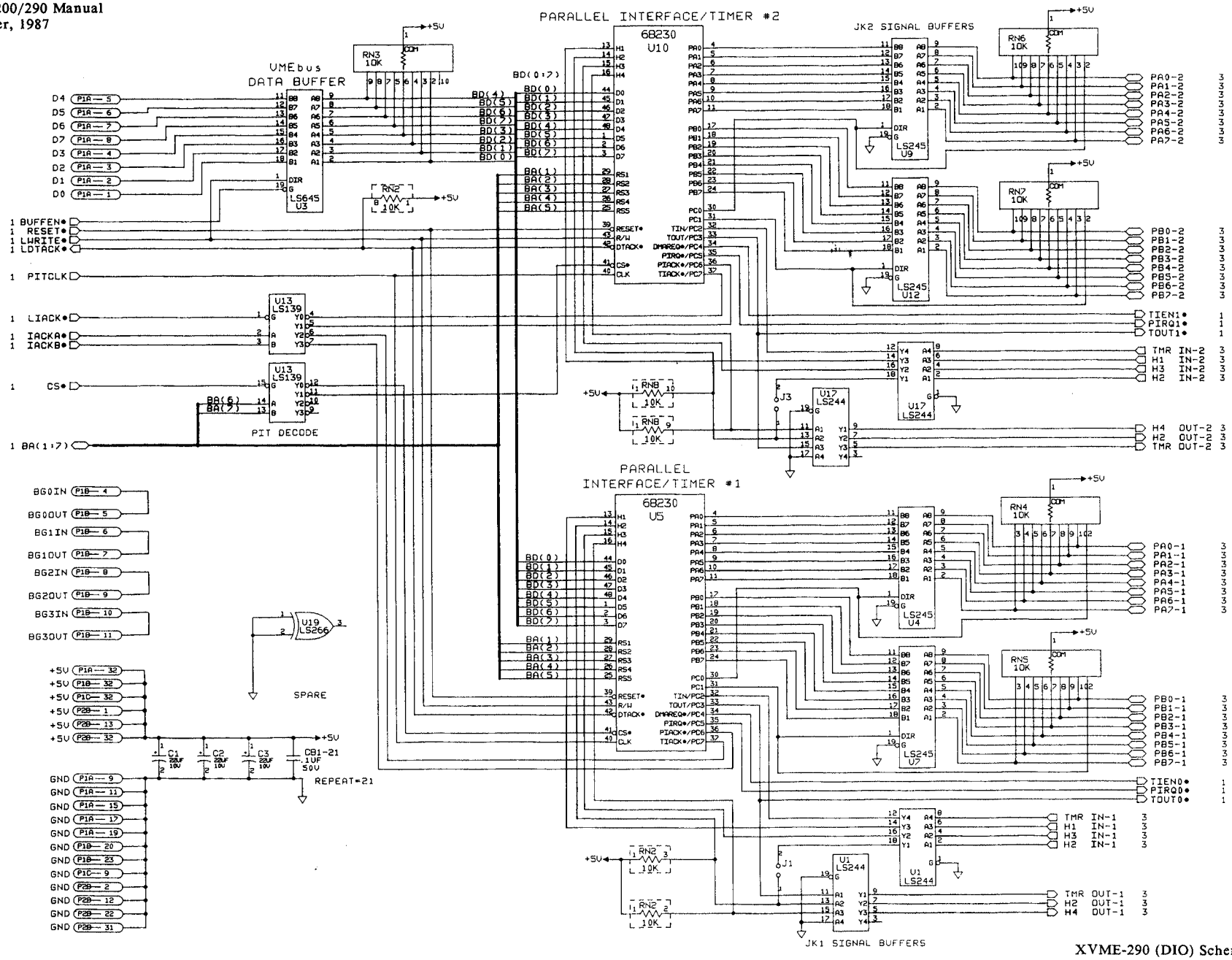
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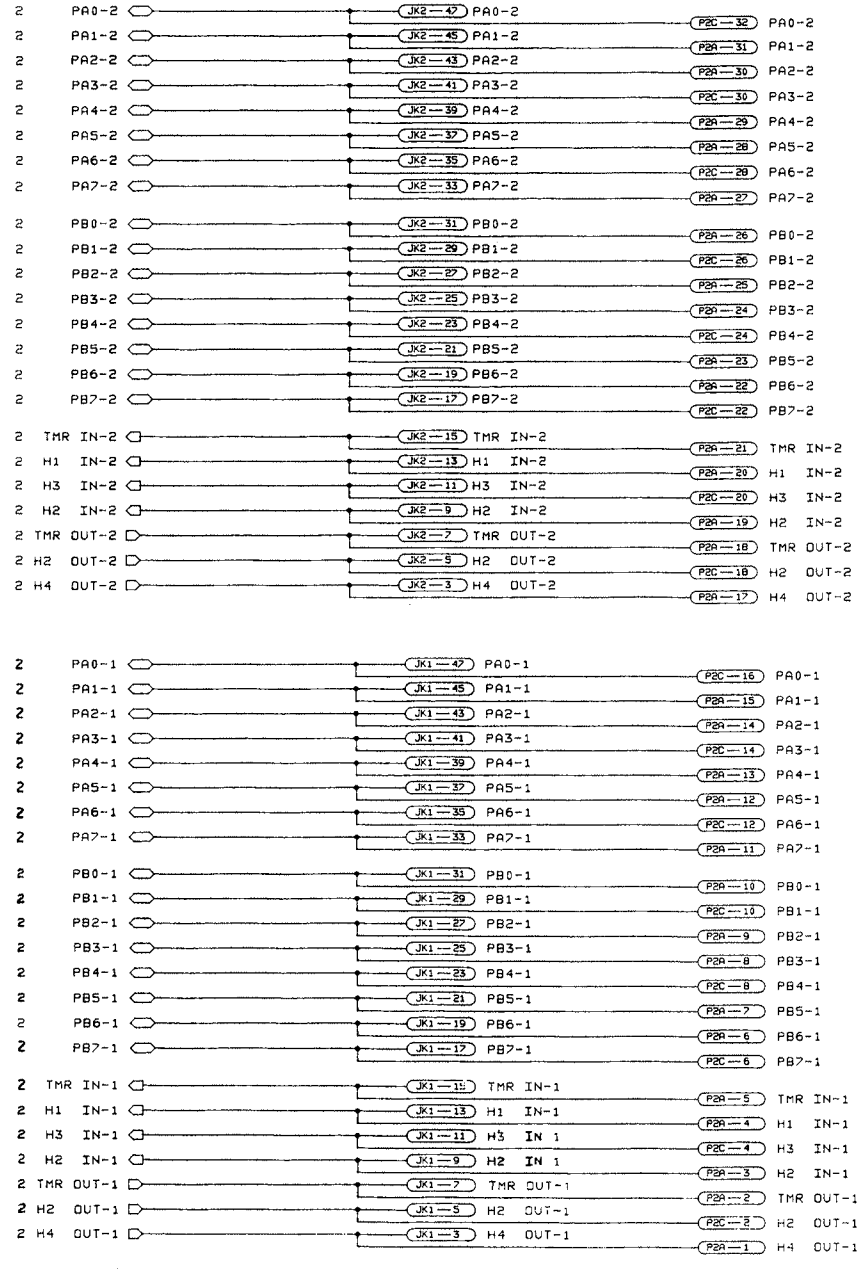


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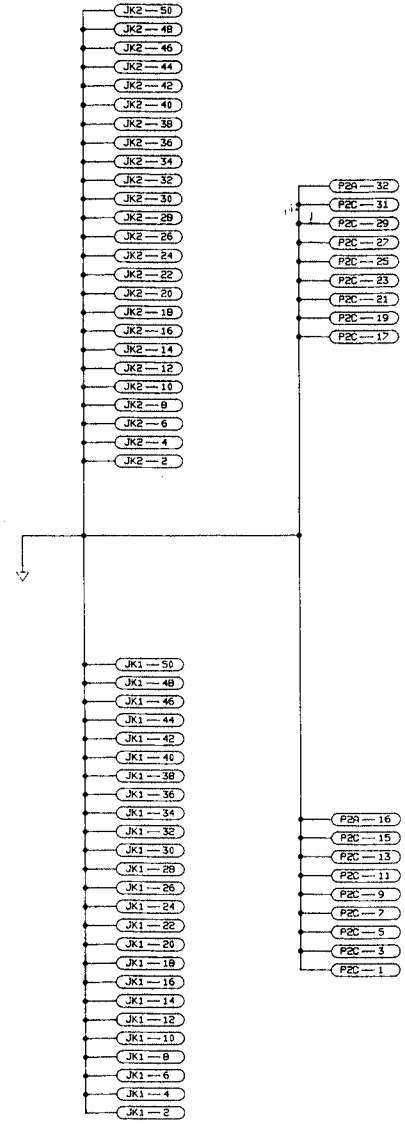


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290/1



290/2



DEVICE	+5V POWER PIN	GROUND PIN
U19-74LS266	14	7
U15- 74S113	14	7
U14- 7433	14	7
U2- 74ALS74	14	7
U16- 74LS682	20	10
U8- 16L8A	20	10
U11- 74LS373	20	10
U18- 16R4A	20	10
U6- 16R6A	20	10
U20- 7445	16	8
U3- 74LS645-1	20	10
U13- 74LS139	16	8
U5,U10- 68230	12	38
U1,U17- 74LS244	20	10
U4,U7,U9,U12- 74LS245	20	10

	CB21
	P2
RN3-10	J3
R1,R2	C3
RN8-3	R3
JA4-JA9	JA15
RN9-2,3,4	RN9
RN1-8	JK2
RN2-4,5,6,7	U20
UNUSED DEVICES	DESIGNATION LAST USED

REFERENCE DESIGNATION CHART

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