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XVME-530

ANALOG OUTPUT MODULE

74530-001 B

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Part Number 74530-001 B

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The XVME-530 Analog Output Module (hereafter referred to as AOUT) is a powerful D/A module which can generate eight 12-bit resolution analog signals. Output can be either voltage or current. The following output voltage ranges are jumper-selectable: 0-5V, 0 to 10V, ±2.5V, ±5V, ±10V. The jumper-selectable current range is 4-20 mA. The eight output channels are optically isolated (300V) from the digital logic.

The gain and offset errors are both adjustable to zero, and the maximum overall error is 0.5 LSB.

1.2 HOW THIS MANUAL IS ORGANIZED

This chapter provides a functional overview of the AOUT and presents the features of XYCOM's Standard I/O Architecture. Operational aspects of the AOUT are then explained in the following fashion:

Chapter 2 - Installation -- Presents information required to position the jumpers and switches on the AOUT, and then install it on a VMEbus chassis.

Chapter 3 - Programming -- Presents information required to program the AOUT and output analog signals.

The appendices at the rear of this manual provide information on XYCOM's Standard I/O Architecture, VMEbus connector/pin description, module schematics, and a quick reference guide to the AOUT's jumpers and registers.

1.3 OVERVIEW

Figure 1-1 shows an operational block diagram of the VMEbus compatible Analog Output module (AOUT).

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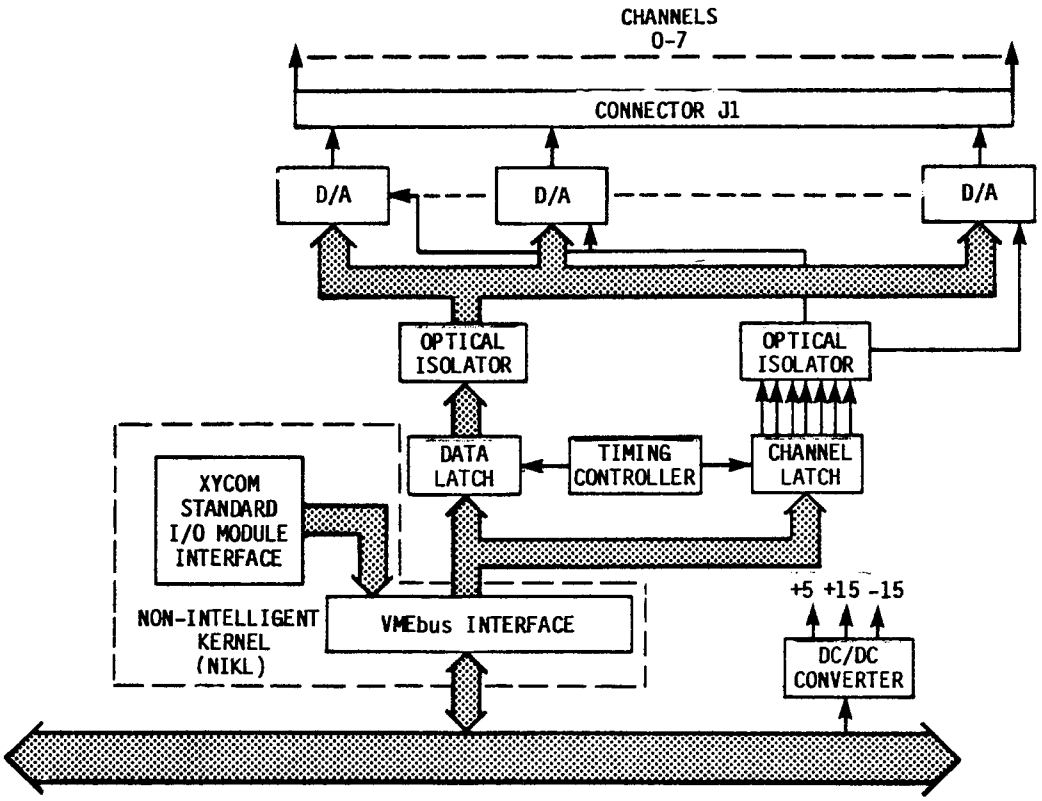


Figure 1-1. Block Diagram of the Analog Output Module

As can be seen from Figure 1-1, the AOUT consists of the Non-Intelligent Kernel which is standard for XYCOM's non-intelligent VMEbus modules, and application circuitry specific to the AOUT.

1.3.1 XYCOM Non-Intelligent Kernel

The Non-Intelligent Kernel is basically the interface to the VMEbus. It provides all the necessary circuitry to receive and generate the signals required by the VMEbus specification for a 16-bit slave. By simply adding the application circuitry (in this

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case D/A circuitry), a VMEbus module is complete. The Non-Intelligent Kernel has the following features:

- Control and Address Buffers
- Address Decode circuitry
- Control/Status Register
- Module identification information
- Pass and Fail LED indicators

The XYCOM Non-Intelligent Kernel is described in further detail in Appendix A.

1.3.2 Application Circuitry

As Figure 1-1 shows, the application circuitry consists primarily of the following:

- 8 D/A converters which perform 12-bit resolution D/A conversions
- Data latch to store the digital data to be converted to analog
- Channel latch to select the output channel over which the data will be output
- Optical isolator to isolate between the digital and analog circutry
- Timing controller to transfer digital information across the optical isolation boundary to the D/A's

1.4 FEATURES OF XYCOM'S STANDARD I/O ARCHITECTURE

The AOUT and all XYCOM I/O modules conform to the unique XYCOM VMEbus Standard I/O Architecture. This architecture is intended to make the programming of XYCOM VMEbus I/O modules simple and consistent. The following features apply to the operation of the AOUT.

- Module Address Space - The AOUT and all VMEbus modules are controlled by writing to addresses within the 64K Short I/O Address space. A VMEbus module can be jumpered to occupy any of the 64 available 1K blocks. This block, known as the I/O Interface Block, contains all of the module's programming registers, and ID data. Within the I/O Interface Block, the offsets are standardized so that the user may expect to find the same registers and data at the same offsets across the entire XYCOM VMEbus line.
- Module Identification - The AOUT has I.D. information which provides its name, model number, manufacturer and revision level at a location that is consistent with other XYCOM I/O modules.
- Status/Control Register - This register is always located at address Base+81H, and the lower four bits (two Test Status bits, and a red and green LED bit) are standard from module to module.

A detailed description of XYCOM I/O Architecture is presented in Appendix A at the rear of this manual.

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1.5 SPECIFICATIONS

Table 1-1. Analog Output Module Specifications

Characteristic	Specification
ANALOG OUTPUTS	
Number Available	8
Optical Isolation	300V
Monotonicity	Guaranteed
Accuracy	
Resolution	12 bits
Overall Error(1)	±0.5 LSB ±.0122%
Conversion Time(2)	42 usec
Settling Time (to .01%, into resistive load)	30 usec. max. (current mode) 8 usec. max. (voltage mode)
Voltage Output Characteristics	
Ranges	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Output Current	5mA min @ ±10V
Offset T.C.	30 ppm/°C (bipolar voltage mode) 15 ppm/°C (unipolar voltage mode)
Gain T.C.	50 ppm/°C
Current Loop Characteristics	
Range	4-20mA
Offset T.C.	30 ppm/°C
Gain T.C.	50 ppm/°C
Load Resistance Range	50 to 525 ohms
Load Regulation	.808 ppm/Ohm
Digital Input Coding	BIN, OBN
Reset	All DACs are reset to 0000H at power-up or system reset
Electrical	
Power Requirements	5V ±5%, Typ. 2.6 A (with outputs at full scale in 4-20mA mode)
Board Dimensions	NEXP Board Size (160mm x 233.4mm)
Temperature	
Operating	0 to 65°C (32° to 149°F)
Non-Operating	-40° to 85°C (-40° to 158°F)

(1) Overall error is specified with gain and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range. It is expressed in terms of bits and in terms of the deviation as a percent of the full scale range (i.e., ±.5 LSB is ±0.0122% FSR of a -10V to +10V range).

(2) Conversion time is defined as the time required to transfer 12 bits of data across the optically-coupled interface. It is measured from the time the low byte is written to when the analog output first starts to change.

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Table 1-1. Analog Output Module Specifications (continued)

Characteristic	Specification
Humidity	5 to 95% RH non-condensing (Extreme low humidity conditions may require special protection against static discharge.)
Altitude	
Operating	Sea-level to 10,000 ft. (3048 m)
Non-Operating	Sea-level to 50,000 ft. (15240 m)
Vibration	
Operating	5 to 2000 Hz .015 in peak-to-peak displacement 2.5 g peak (maximum) acceleration
Non-Operating	5 to 2000 Hz .030 in peak-to-peak displacement 5.0 g peak (maximum) acceleration
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-Operating	50 g peak acceleration, 11 msec duration

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Chapter 2

INSTALLATION

2.1 GENERAL

This chapter provides the information to configure the AOUT prior to installation in a VMEbus backplane card cage, and presents the installation procedure.

2.2 SYSTEM REQUIREMENTS

The AOUT is a double-height VMEbus compatible module. To operate it must be properly installed in a VMEbus backplane cardcage. The minimum system requirements for operation of the AOUT are one of the following:

A)
- A host processor properly installed on the same backplane.
- A properly installed controller subsystem. An example of such a controller subsystem is the XYCOM XVME-010 System Resource Module (SRM).

-- OR --

B)
- A host processor which incorporates an on-board controller subsystem.

2.3 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers, Address Switches, and connectors on the AOUT are illustrated in Figure 2-1.

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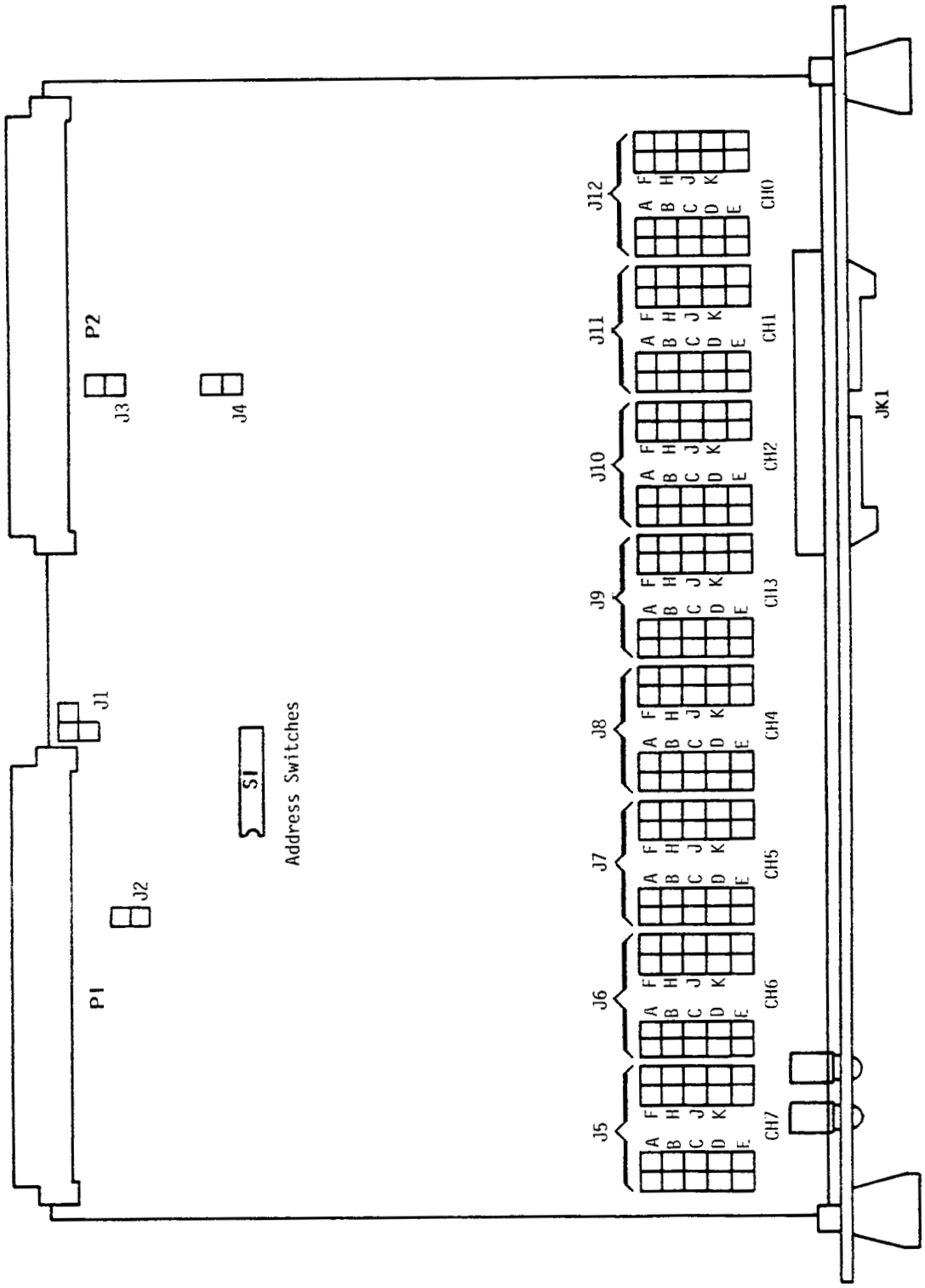


Figure 2-1. AOUT Jumpers, Address Switches, and Connectors

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2.4 JUMPERS/SWITCHES

Prior to installing the AOUT, it will be necessary to configure several jumper/switch selectable options. These options fall into two categories: VMEbus-related options and Analog-to-Digital conversion options.

VMEbus Options

- Module base address, selected by switches 1-6 of the Address Switches.
- Privilege level required to access the module, selected by switch 8 of the Address Switches.

Analog to Digital Conversion Options

- 8 jumper blocks (labeled J5 through J12). Each jumper bank selects from the following available output voltage and current ranges:

  4-20mA current loop
  0-10V
  0-5V
  ±10V
  ±5V
  ±2.5V

Table 2-1. AOUT Jumper/Switch List

Jumper/Switch	Use
J1	Not used on the AOUT.
J2B	Jumper J2 must be in the "B" position for proper module operation.
J3, J4	Not used on the AOUT.
J5 J6 J7 J8 J9 J10 J11 J12	One jumper block per output channel.
Address Switches	Address and Address Modifier compare switches.

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2.4.1 Base Address Switches

The AOUT has been constructed in accordance with XYCOM's Standard I/O Architecture (see Appendix A for a detailed description). As such, it can occupy any one of 64 1K blocks of memory within the 64K VMEbus Short I/O Address Space. The particular 1K block it shall reside in is selected by configuring the AOUT's "Base Address" equal to the beginning address of that block. The Base Address is selected by configuring switches 1-6 of the Address Switches (see Figure 2-2), as shown in Table 2-2.

NOTE

Switch position 8 must be set to the "Closed" position. Switch 7 is described in Section 2.4.2.

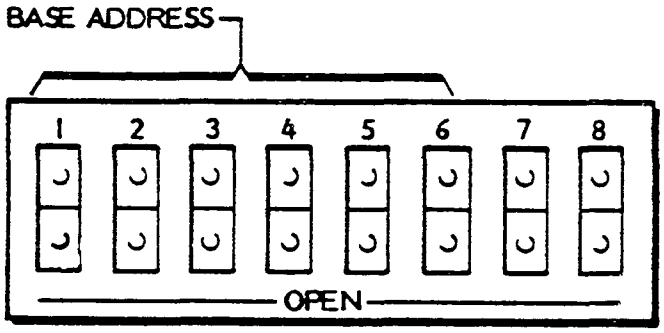


Figure 2-2. Address Switches

Table 2-2. Base Address Switches

Switch	Address Bit
6	A15
5	A14
4	A13
3	A12
2	A11
1	A10

NOTE

"OPEN" position equals logic 1, closed equals logic 0.

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2.4.2 Supervisor/Non-Privileged Mode Selection

The AOUT can respond only to Short I/O accesses. However, it can be configured to respond to only Supervisory access, or to both Non-Privileged and Supervisory accesses, by selecting the position of Switch 7 (see Figure 2-3), as shown in Table 2-3 below. Available AM codes are all Short I/O codes.

Table 2-3. Privilege Options

Switch 7	Privilege Mode Selected
Closed	Supervisory or Non-Privileged
Open	Supervisory Only

2.4.3 Address Modifier Reference

The following table (Table 2-4) indicates the actual VMEbus Address Modifier code that the AOUT will respond to based on the position of the two options discussed in the previous two sections.

Table 2-4. Address Modifier Code Options

	Switches 7	8	Jumper J2	Address Modifier Code AOUT will respond to
Short I/O	Closed	Closed	B	29H or 2DH
	Open	Closed	B	2DH only

2.4.4 BGxIN/BGxOUT and IACKIN/IACKOUT Daisy Chains

The Data Bus Arbitration signals BGxIN and BGxOUT (where "x" can be a number 0-3 to represent the three levels of arbitration) are not used by the AOUT, and are hardwired together on the module to allow the BGxIN/BGxOUT Daisy Chain to pass through the backplane slot occupied by the AOUT. In each slot of the VMEbus backplane, there are four sets of jumpers shorting the signal BGxIN to BGxOUT (x=0 thru 3). Since these signals are already hardwired on the AOUT, it is not necessary to insert these VMEbus jumpers on the slot occupied by the AOUT.

In addition, IACKIN/IACKOUT are hardwired together on the AOUT module.

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2.4.5 Output Jumpering

The AOUT's 8 outputs can each be individually configured in one of 6 different modes by jumpering the operational amplifier buffer on the output of each channel into different configurations. Eacn configuration is selected by placing jumpers across certain points labeled A, B, C, D, E, F, H, J, K, and L, on the AOUT circuit board. The diagram format below will be used to represent the jumper banks J5-J12. The jumper configurations for each analog output option are listed in Table 2-5.

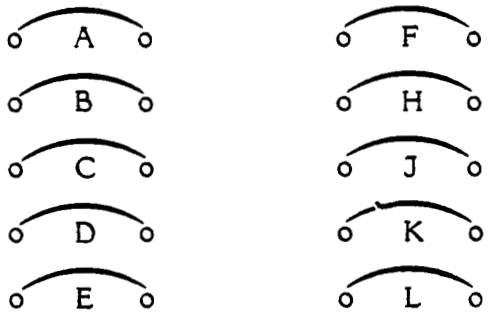


Figure 2-3. Output Jumper Configuration Diagram

The following table lists the jumper configuration unique to each mode.

Table 2-5. Jumper Configurations for Output Mode Options

Mode Chosen	Jumpers (all other output jumpers should be removed)
4 - 20mA	F, H, J, K, L
0 - 10V	A, C
0 - 5V	A, C, E
±10V	A, B, D
±5V	A, B, C
±2.5V	A, B, C, E

NOTE

The AOUT will be shipped to the customer in the 4-20mA output mode.

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2.5 ANALOG OUTPUT CONNECTIONS

The module is capable of providing 8 separate analog outputs. The outputs are accessible on the front edge of the board in the form of one 34 pin mass termination header. The connector is labeled JK1 (see Figure 2-1). The following table shows the pin designations for JK1.

Table 2-6. Output Connector JK1

JK1			
Pin	Signal	Pin	Signal
1	Chan. 0 Gnd	26	Chan. 6 Vout
2	Chan. 0 Vout	27	Chan. 6 IOUT-
3	Chan. 0 IOUT-	28	Chan. 6 IOUT+
4	Chan. 0 IOUT+	29	Chan. 7 Gnd
5	Chan. 1 Gnd	30	Chan. 7 Vout
6	Chan. 1 Vout	31	Chan. 7 IOUT-
7	Chan. 1 IOUT-	32	Chan. 7 IOUT+
8	Chan. 1 IOUT+	33	Gnd
9	Chan. 2 Gnd	34	Gnd
10	Chan. 2 Vout		
11	Chan. 2 IOUT-		
12	Chan. 2 IOUT+		
13	Chan. 3 Gnd		
14	Chan. 3 Vout		
15	Chan. 3 IOUT-		
16	Chan. 3 IOUT+		
17	Chan. 4 Gnd		
18	Chan. 4 Vout		
19	Chan. 4 IOUT-		
20	Chan. 4 IOUT+		
21	Chan. 5 Gnd		
22	Chan. 5 Vout		
23	Chan. 5 IOUT-		
24	Chan. 5 IOUT+		
25	Chan. 6 Gnd		

2.6 MODULE INSTALLATION

The XYCOM VMEbus modules can accommodate typical VMEbus backplane construction. Figure 2-4 shows a standard VME chassis and a typical backplane configuration. There are two rows of backplane connectors depicted (i.e., the P1 backplane and the P2 backplane).

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2.6.1 Installation Procedure

CAUTION

Do not attempt to install or remove any boards before turning off the power to the bus and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations and all connections to external devices or power supplies. (Please check the jumper configuration with the diagram and lists in the manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot you are going to use is clear and accessible.

2) Center the board on the plastic guides so that the solder side is facing to the left and the component side is facing to the right (refer to Figure 2-4).

3) Push the card slowly toward the rear of the chassis until the connectors engage (the board should slide freely in the plastic guides).

4) Apply straight-forward pressure to the two handles on the outer edge of the board until the connectors are fully engaged and properly seated.

NOTE

It should not be necessary to use excess pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, it should be secured by tightening the two machine screws at the extreme top and bottom of the board.

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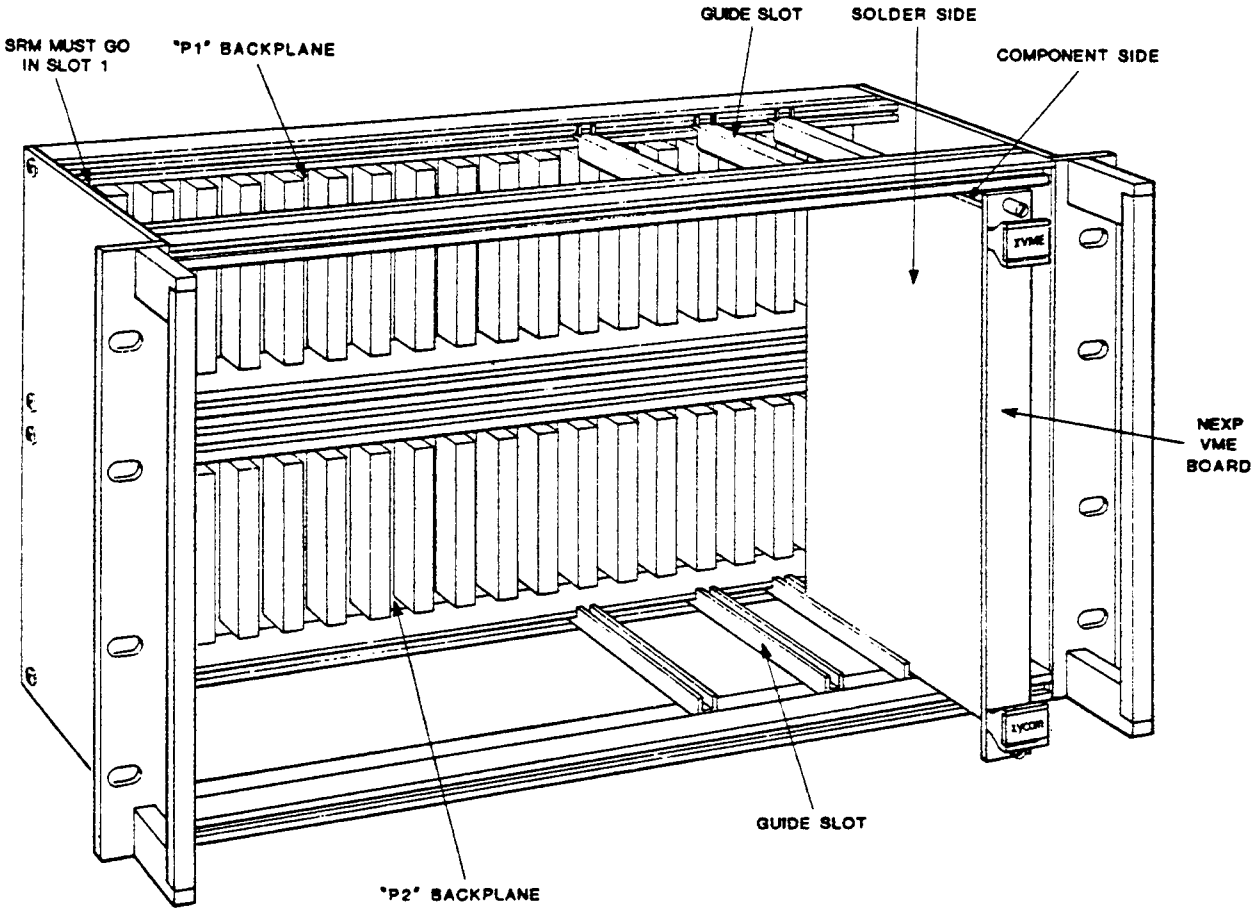


Figure 2-4. VMEbus Chassis

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Chapter 3

PROGRAMMING

3.1 INTRODUCTION

This chapter provides the information required to program the AOUT, access conversion data and perform calibration. This information is presented in the following fashion:

- Discussion of base addressing and I/O module address space
- Presentation of module address map showing programming locations
- Generating analog signals
- Reading the status of a D/A conversion
- Calibration

3.2 BASE ADDRESSING

The AOUT operates as an I/O module in VMEbus systems and is therefore located in the 64K VMEbus Short I/O Address Space. It can be located at any one of 64 Base Addresses at 1K intervals within this address space. The base address is selected via the switches described in Section 2.4.1.

When located at its base address, the AOUT is alloted a 1K block of short I/O address space for its own use. This 1K block of short I/O address space is termed the I/O Interface Block, and contains all of the module's programming locations. Figure 3-1 shows the AOUT's I/O Interface Block and its relation to the Short I/O Address space.

When a host processor is addressing locations in the I/O Interface Block, the location's address is added to the module's base address.

For example, if the AOUT is located at Short I/O Base Address 0400H, the address of the Control/Status register is 0481H (base+81H).

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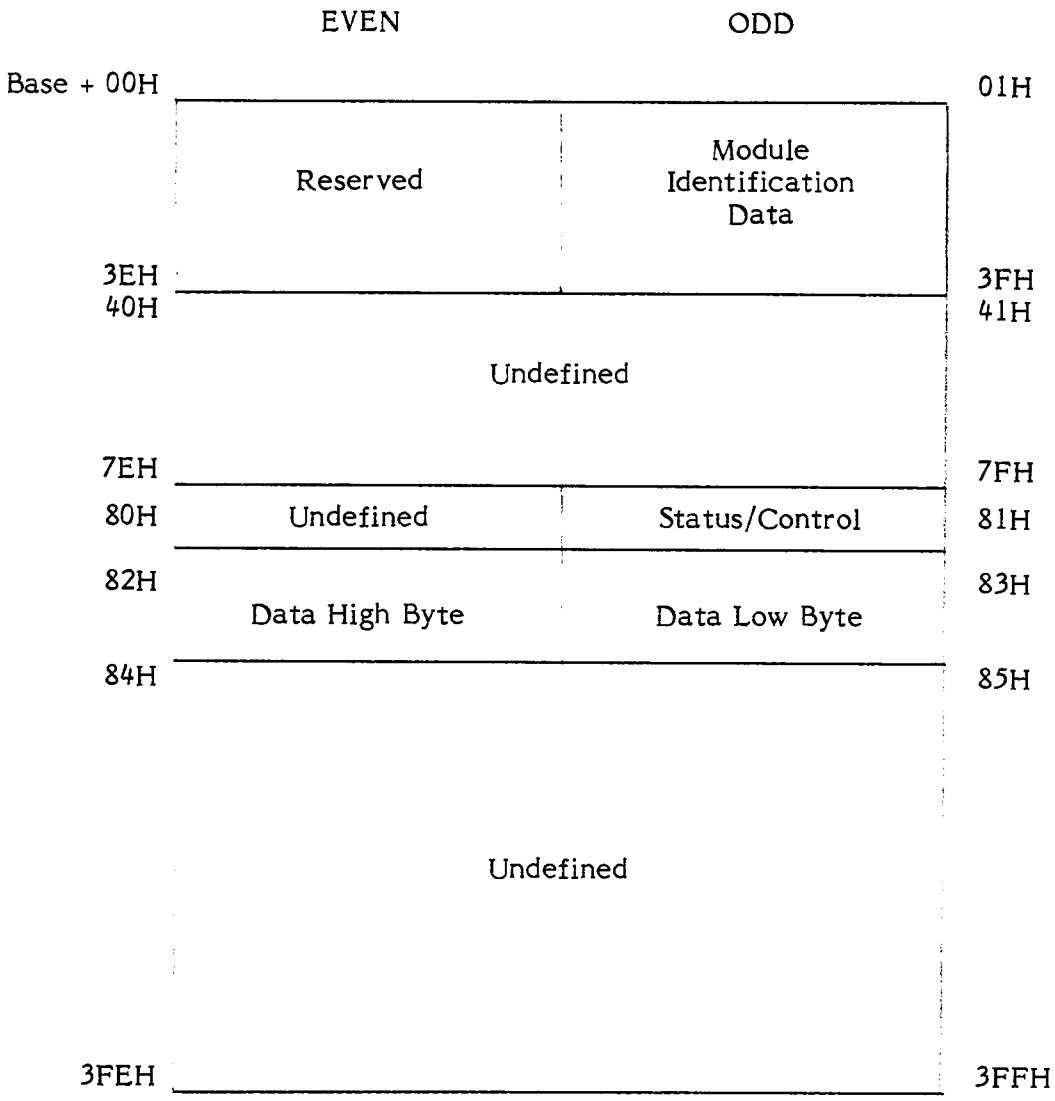


Figure 3-1. AOUT I/O Interface Block and its Possible Locations in Short I/O Address Space

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3.3 I/O INTERFACE BLOCK

The AOUT I/O Interface Block contains the following programming locations (as shown in Figure 3-1) which are defined in greater detail in their section of this chapter.

- I.D. information (base+01H to base+3FH): These locations provide information specifying model number, manufacturer and revision level.
- Status/Control register (base+81H): This location returns the status of a D/A conversion, controls the red and green LEDs, and provides board reset.
- Data High Byte (base+82H) and Data Low Byte (base+83H): These locations contain the digital data to be converted to analog. Conversion is automatically triggered by writing to the Data Low Byte.

NOTE

Reading or writing to undefined locations may make application software incompatible with future versions of this module.

3.4 STATUS/CONTROL REGISTER (base+81H)

Writing to the Status/Control register can reset the AOUT and/or control the red or green LEDs. By reading from the Status/Control register, the user can determine whether a conversion is still in progress (i.e., not completed).

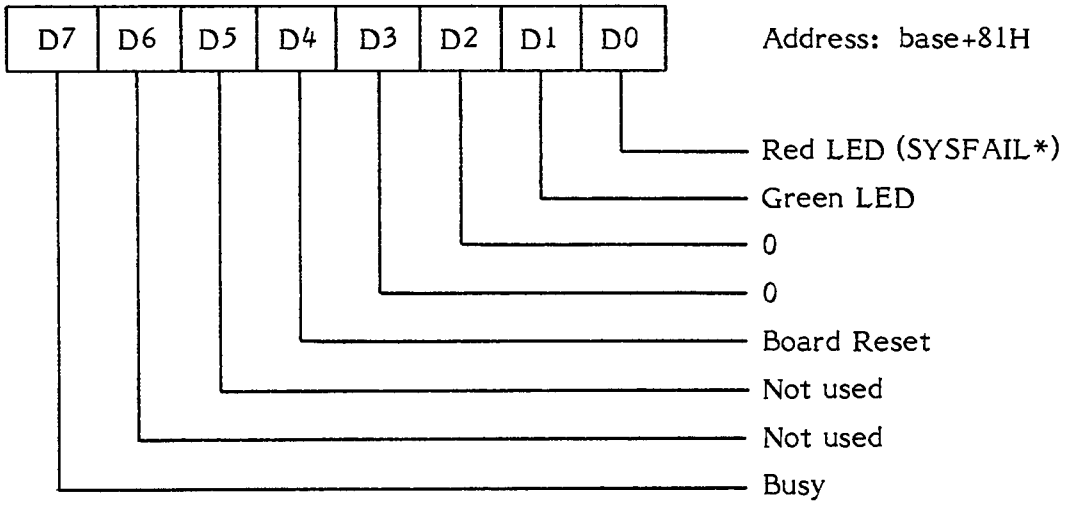


Figure 3-2. Status/Control Register

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3.4.1 Status/Control Register Bit Definitions

D7: Busy bit: A logic "1" in this bit indicates that the AOUT is in the process of making an D/A conversion. The level of this bit must be known or checked prior to starting another D/A conversion, or the D/A conversion in progress could be corrupted.

D6,D5: Not used.

D4: Reset bit. This bit is a software module reset. Setting this bit to "1" resets each analog channel to 000H. (This bit must be held high for a minimum of 4 us.) Note that setting this bit does not reset the Status/Control register. This bit must be reset back to "0" to release the AOUT from the reset state. If the AOUT is jumpered for unipolar mode, a reset will cause the analog output to go to 0V. If the AOUT is jumpered for bipolar mode, a reset will cause the analog output to go to -V max. (4mA in current mode).

D3: Not used.

D2: Not used.

D1,D0: These bits control the red and green LEDs. The red and green LEDs provide visual indication of a module status.

- o A logic "0" turns on the Red LED (D0)
- o A logic "1" turns on the Green LED (D1)

The LEDs should be used to indicate the following status (Table 3-1) as set forth by the XYCOM architecture (described in Appendix A).

Table 3-1. LED Status

Status Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

NOTE

The AOUT is a non-intelligent module so all diagnostics must be performed by the system host.

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3.5 DATA REGISTER (base+82H)

3.5.1 D/A Conversions

The D/A converter (DAC) can produce a voltage or current analog output. The value of the analog output will be a fraction of the DAC's "full scale" output defined by the digital code sent to the DAC.

The data to be converted is written to one of the eight A/D conversion channels. The channel selected is encoded in the data word written to the data port address, as shown below:

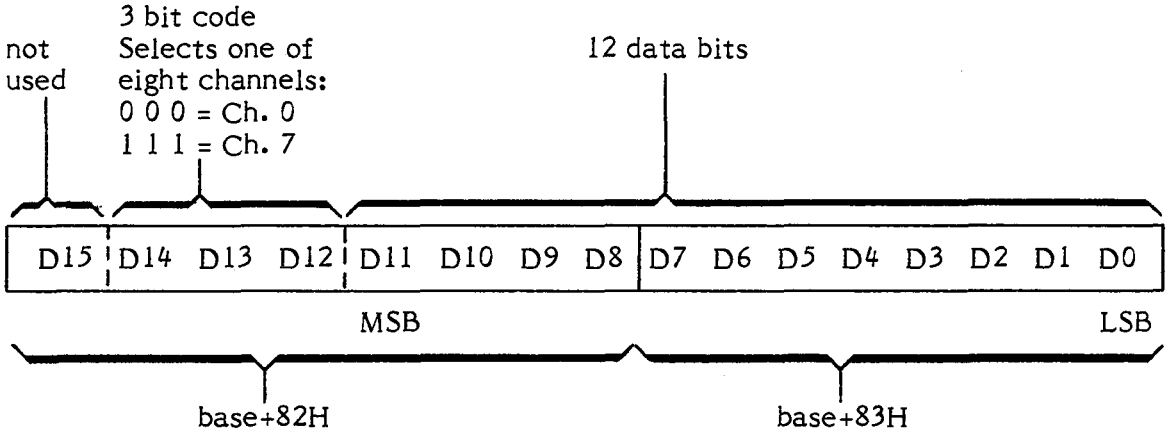


Figure 3-3. Data Port (Write Only)
(address = base+82H)

The Digital to Analog Conversion process will begin when the LSB is written to the address Base+083H of the Data Port. For this reason either the entire word must be written to the data port, or, if one byte is written at a time, the MSB must be written before the LSB. Whenever the LSB is written, the last MSB written will be used as data for the D/A conversion.

3.5.2 Digital Data Format

The AOUT individual channel output can be represented in one of six different analog formats, depending on how the channel output buffer is jumper configured (see Section 2.4.5). The digital data written to the data port corresponds to the magnitude of the analog output signal in a relation that is different for each of the two digital data formats.

The analog output signals can be divided into two general groups; Unipolar output, where the output has only positive polarity (e.g., 0-5V), and Bipolar output, where the output magnitude can have a negative or positive polarity (e.g., $\pm$5V). Current mode is unipolar. The formats are listed in the following tables.

In the unipolar mode the number to be converted must be encoded in straight binary form (see Table 3-2).

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Table 3-2. Unipolar Modes
(Straight Binary Encoding)

Voltage Mode:	
D11 D0	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	Vmax * (4095/4096)
1 0 0 0 0 0 0 0 0 0 0 0	Vmax * (2048/4096)
0 0 0 0 0 0 0 0 0 0 0 0	0V
Current Mode:	
D11 D0	ANALOG OUTPUT 4-20mA
1 1 1 1 1 1 1 1 1 1 1 1	4 + 16 * (4095/4096)mA
1 0 0 0 0 0 0 0 0 0 0 0	4 + 8 = 12mA
0 0 0 0 0 0 0 0 0 0 0 0	4mA

In the bipolar mode the digital value converted to analog must be encoded in offset binary form. In offset binary encoding the negative full scale voltage (-Vmax) is represented by binary zero. The notation is then represented by binary counting from zero up to the maximum binary representation of all one's which will represent the positive full scale voltage minus one LSB.

Table 3-3. Bipolar Voltage Mode
Offset Binary Encoding)

Voltage Mode:	
D11 D0	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	+Vmax * (2047/2048)
1 0 0 0 0 0 0 0 0 0 0 1	+Vmax * (1/2048)
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	-Vmax * (1/2048)
0 0 0 0 0 0 0 0 0 0 0 0	-Vmax

3.6 CALIBRATION

Each channel on the AOUT has two potentiometers used to calibrate its digital to analog conversion. One potentiometer is called the "zero adjust" potentiometer, and the other is called the "gain adjust" potentiometer. The calibration is done by adjusting the zero adjust potentiometer and then adjusting the gain adjust potentiometer. Calibration ensures that the analog output responds properly to the digital input throughout the operating range of the digital to analog conversion (for the chosen output buffer jumper configuration). Refer to Section 2.4.5 for possible output configurations. Note each time the configuration is changed the channel must be recalibrated.

The zero adjust potentiometers for each channel are listed in Table 3-4.

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Table 3-4. Zero Adjust Potentiometers

R41	Channel 0
R39	Channel 1
R37	Channel 2
R35	Channel 3
R33	Channel 4
R31	Channel 5
R29	Channel 6
R27	Channel 7

The channel's zero adjust potentiometer must be adjusted first as follows:

Unipolar Operation

1) Load the data port with the channel number and with all 12 data bits set to zero (see Figure 3-3).

2) Adjust the channel's corresponding zero adjust potentiometer for the lowest value of voltage or current allowed by the output buffer jumper configuration (0V or 4mA).

Bipolar Operation

1) Load the data port with the channel number and with all 12 data bits set to zero (see Figure 3-4).

2) Adjust the channel's corresponding zero adjust potentiometer for an output of negative full scale (-FS). Table 3-5 lists the zero potentiometers for each channel.

Table 3-5. Channel Gain Adjust Potentiometers

R40	Channel 0
R38	Channel 1
R36	Channel 2
R34	Channel 3
R32	Channel 4
R30	Channel 5
R28	Channel 6
R26	Channel 7

The negative full scale value will depend on the output buffer jumper configuration (see Table 3-6).

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Table 3-6. Potentiometer Adjustments

	Zero Adjust Potentiometer Setting	Gain Adjust Potentiomenter Setting (pos. full scale minus 1 LSB)
4-20mA	4.0000 mA	+19.9961 mA
0-10V	0.0000 V	+9.9975 V
0-5V	0.0000 V	+4.9988 V
±10V	-10.0000 V	9.9951 V
±5V	-5.0000 V	4.9975 V
±2.5V	-2.5000 V	2.4988 V

In bipolar or unipolar operation the gain adjust potentiometers should be adjusted as follows:

1) Load the data port register with the channel number and with all 12 data bits set to one (see Figure 3-3).

2) Adjust the channel's corresponding gain adjust potentiometer for an output of the positive full scale value minus one LSB (see Table 3-6).

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Appendix A

XYCOM STANDARD I/O ARCHITECTURE

INTRODUCTION

The purpose of this Appendix is to define XYCOM's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all XVME I/O modules in order to provide a simpler and more consistent method of programming for the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the XYCOM I/O Architecture are the following:

1. Module Addressing -- Where a module is positioned in the I/O address space and how software can read from it or write to it.

2. Module Identification -- How software can identify which modules are installed in a system.

3. Module Operational Status -- How the operator can (through software) determine the operational condition of specific modules within the system.

4. Interrupt Control -- How software is able to control and monitor the capability of the module to interrupt the system.

5. Communication between Modules -- How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the I/O modules.

6. The I/O Kernel -- How intelligent and non-intelligent "kernels" facilitate the operation of all XYCOM I/O modules.

MODULE ADDRESSING

All XYCOM I/O modules are designed to be addressed within the VMEbus-defined 64K short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while at the same time providing 64K of address space for I/O modules.

Base Addressing

Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for XYCOM VME I/O modules has been designed to be switch-selectable. Each XVME I/O module installed in the system requires at least a 1K byte block of the short I/O memory. This divides the 64K short I/O address space into 64 1K segments. Thus, each I/O module has a base address which starts on a 1K boundary. As a result, the XYCOM I/O modules have all been implemented to decode

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base addresses in 1K (400H) increments. On an intelligent XVME module, address signals A10-A13 are decoded, while A14 and A15 must be zero. (This implies that only the lowest 16 of the possible 64 1K segments are used for intelligent modules.) On non-intelligent XVME modules, the six highest order short I/O address bits are decoded, while the remaining lower order bits are ignored. This arrangement provides the correct address configuration to allow each module address to begin on a 1K boundary. Non-intelligent XVME modules allow the use of six base address jumpers (representing bits A10-A15), and thus, they are able to reside on any of the 64 1K boundaries available in the short I/O address space. Intelligent XVME modules will only allow the use of four base address jumpers (representing bits A10-A13) which limits their selection of 1K boundaries to one of 16 possible choices.

Figure A-1 shows an abbreviated view of the short I/O memory. The list shown next to the figure provides the 16 possible addresses which could be used as base addresses by XVME intelligent I/O modules.

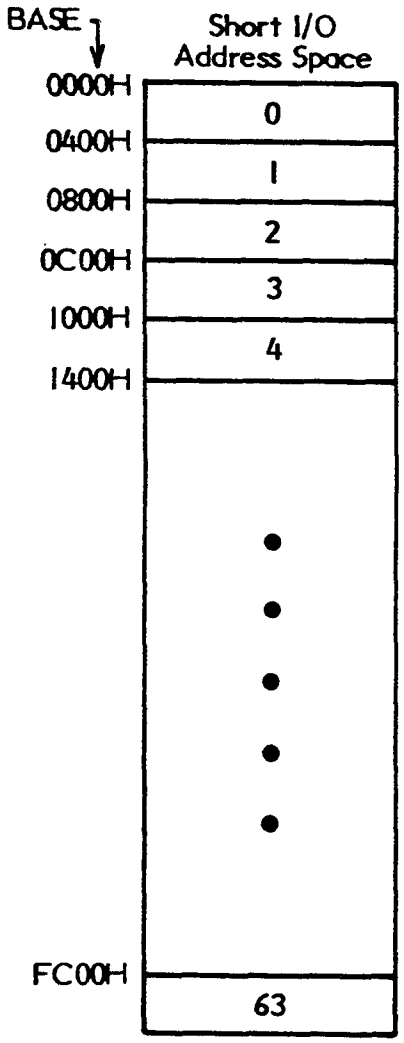


Figure A-1. 64K Short I/O Address Space

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Standardized Module I/O Map

The 1K block of short I/O addresses (called the I/O Interface Block) allocated to each XVME module is mapped with a standardized format in order to simplify programming and data access. The locations of frequently used registers and module-specific identification information are uniform. For example, the module identification information is always found in the first 32 odd bytes of the module memory block -- with these addresses being relative to the jumpered base address (i.e., Module I.D. data address = base address + odd bytes 1H - 3FH). The byte located at base address+81H on each module contains a Status/Control register which provides the results of diagnostics for verification of the module's operational condition. The next area of the module I/O Interface Block (base address + 82H - roughly 120H) is module-specific and it varies in size from one module to the next. It is in this area that the module holds specific I/O status, data, and pointer registers for use with IPC protocol. All intelligent XVME I/O modules have an area of their I/O Interface Blocks defined as "dual access RAM." This area of memory provides the space where XVME "slave" I/O modules access their command blocks and where XVME "master" modules could access their command blocks (i.e., "master" modules can also access global system memory).

The remainder of the I/O Interface Block is then allocated to various module-specific tasks, registers, buffers, ports, etc.

Figure A-2 shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. Notice that any location in the I/O Interface Block may be accessed by simply using the address formula:

Module Base Address + Relative Offset = Desired Location

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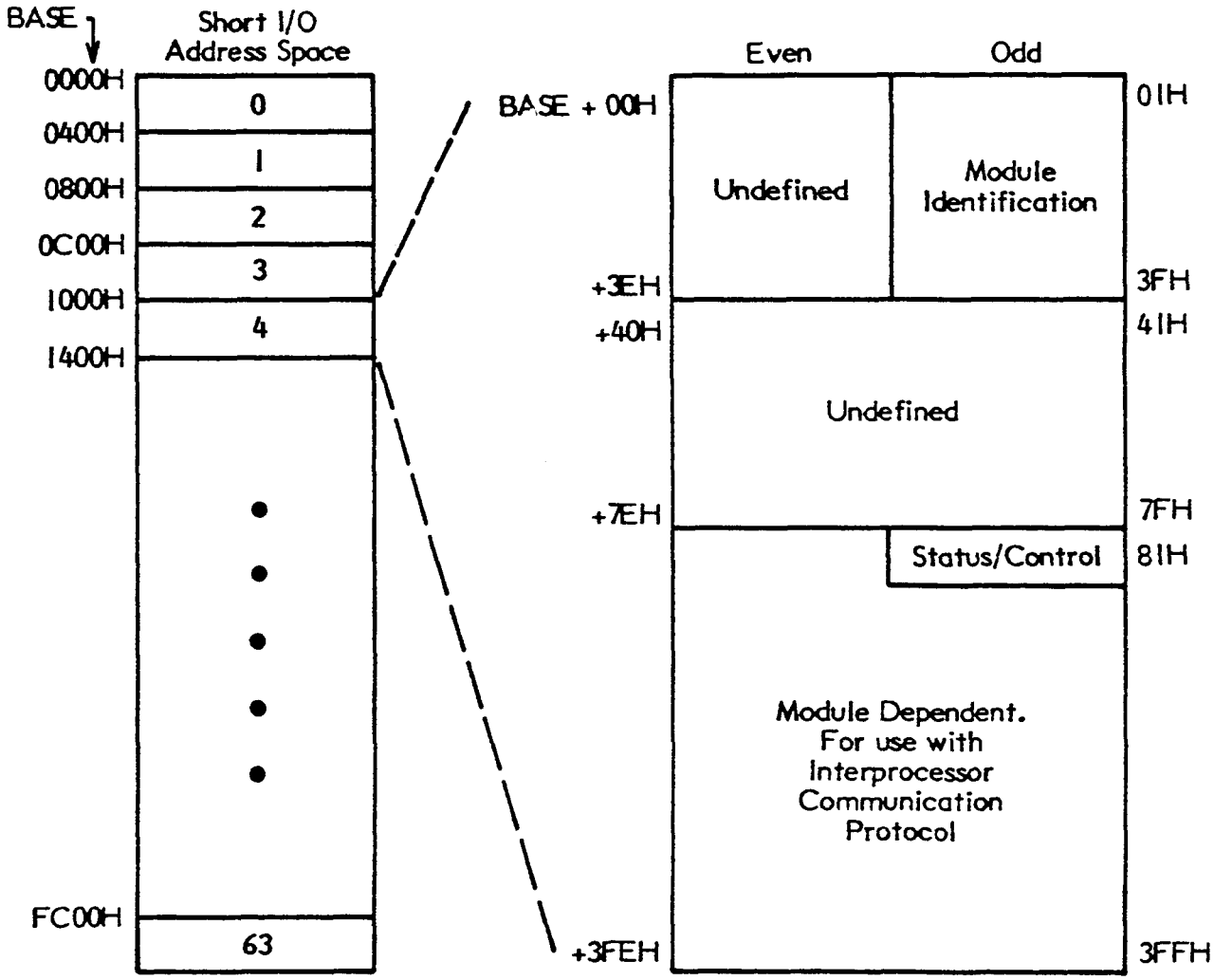


Figure A-2. XVME I/O Module Address Map

MODULE SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K-byte blocks occupied by the module, and model functional revision level information. This information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1 defines the Identification information locations.

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Table A-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier,
5	E	45	always "VMEID"
7	I	49	(5 characters)
9	D	44	
B	X	58	Manufacturers I.D.,
D	Y	59	always "XYC" for XYCOM
F	C	43	Modules (3 characters)
11	5	35	
13	3	33	Module Model Number
15	0	30	(3 characters and
17		20	4 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision
23	3	33	level with leading blank (if single digit)
25	1	31	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer
37	"		Dependent Information,
39	"		Reserved for Future Use
3B	"		
3D	"		
3F	"		

The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1H-3FH).

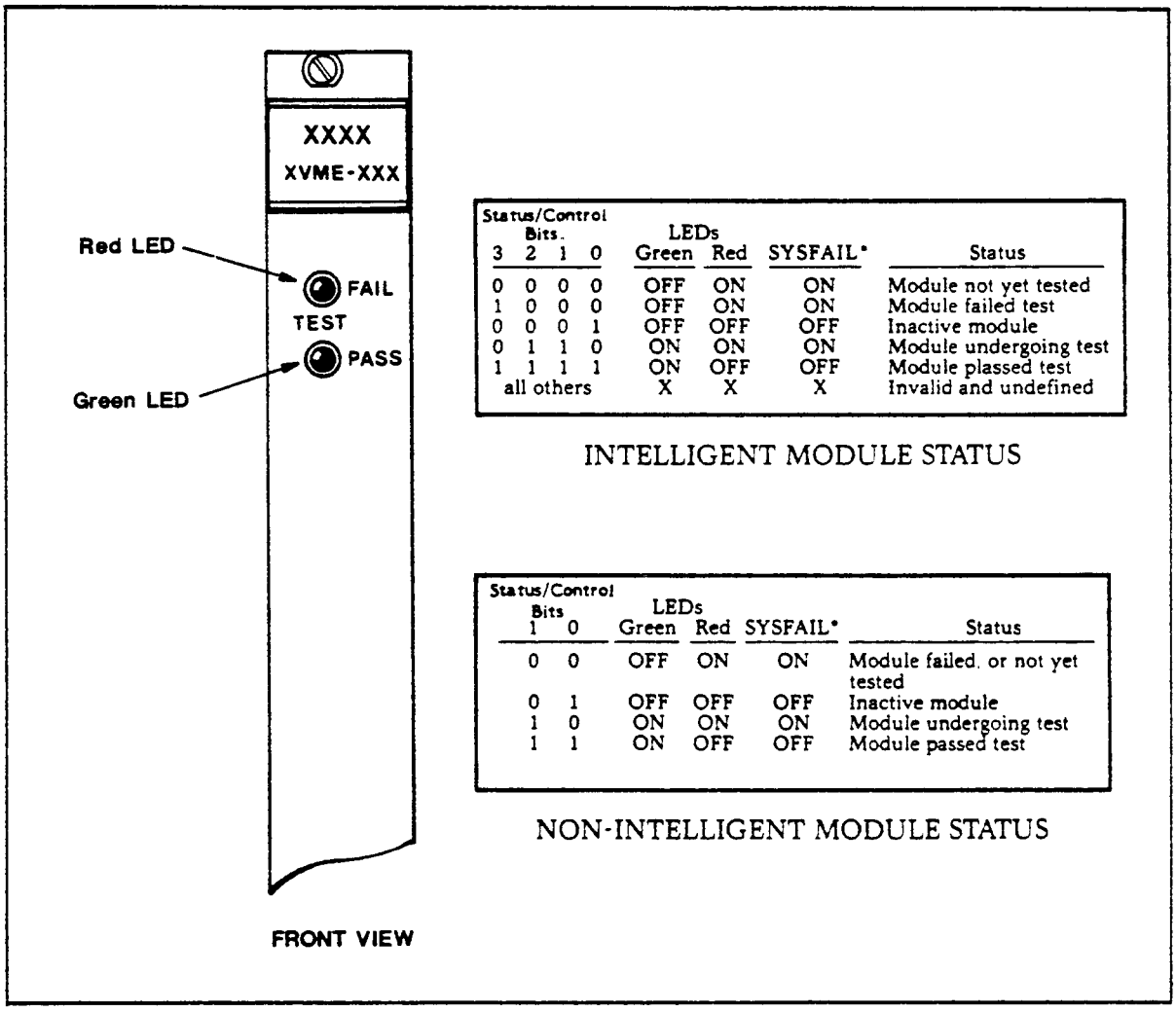
I.D. information can be accessed simply by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex-coded ASCII value at each location. Thus, in this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH within the system's short I/O address space.

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MODULE OPERATIONAL STATUS/CONTROL

All XVME intelligent I/O modules are designed to perform diagnostic self-tests on power-up or reset. For non-intelligent modules, the user must provide the diagnostic program. The self-test provision allows the user to verify the operational status of a module by either visually inspecting the two LEDs which are mounted on the module front panel (see Figure A-3), or by reading the module status byte (located at module base address + 81H).

Figure A-3 shows the location of the status LEDs on the module front panel. The two tables included with Figure A-3 define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status/Control Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module plassed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status/Control Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

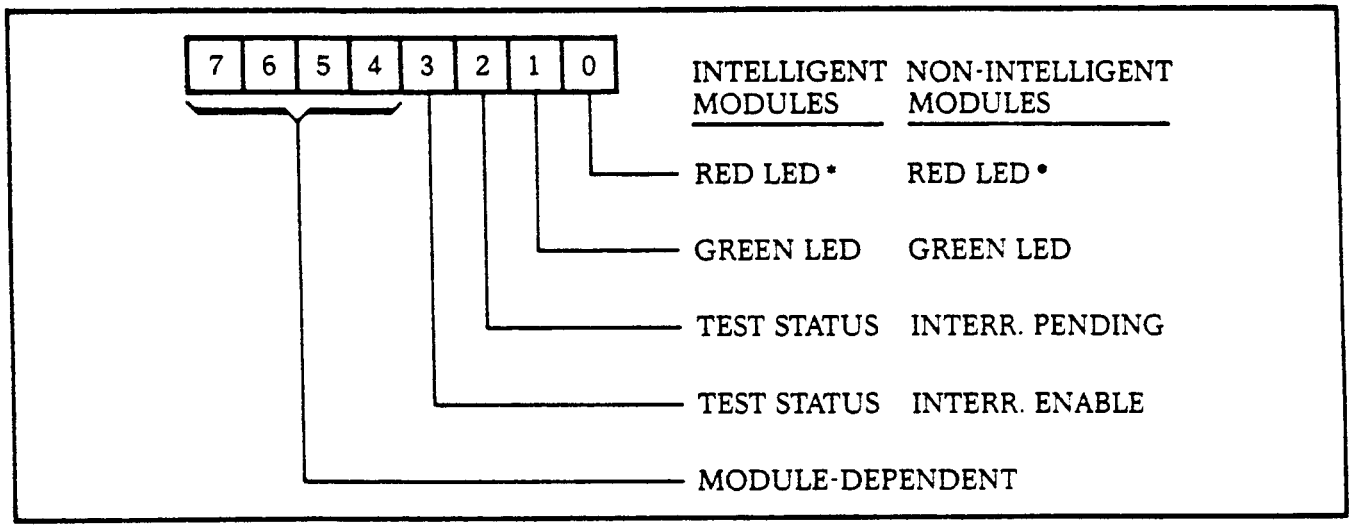
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The module status/control register (found at module base address + 81H) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent modules is a "Read Only" register and it can be read by software to determine if the board is operating properly.

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module-generated interrupts. The LED status bits are "Read/Write" locations which provide the user with the indicators to accomodate diagnostic software. The Interrupt Enable bit is also a Read/Write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a "Read Only" bit which indicates a module-generated pending interrupt.

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Figure A-4 shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules
0	Read/Write - Red LED* 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Bit	Intelligent Modules
0	Read Only - Red LED* 0 = Red LED On 1 = Red LED Off
1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2 & 3	Read Only - Test Status Indicators Bit 3 / Bit 2 0 / 0 = Self-test not started 0 / 1 = Self-test in progress 1 / 0 = Self-test failed 1 / 1 = Self-test passed
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Figure A-4. Status Register Bit Definitions

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INTERRUPT CONTROL

Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status of pending on-board interrupts can also be read from this register. Interrupt control for intelligent modules is handled by the Interprocessor Communications Protocol.

Communications Between Processors

Communications between an intelligent "master" and an intelligent "slave" I/O module is governed by XYCOM's Interprocessor Communication (IPC) Protocol. This protocol involves the use of 20-byte Command Block data structures, which can be located anywhere in shared global RAM or dual-access RAM on an I/O module, to exchange commands and data between a host processor and an I/O module. Interprocessor Communication Protocol is thoroughly explained in Chapter 3 of this manual.

THE KERNEL

To standardize its XVME I/O modules, XYCOM has designed them around "kernels" common from module to module. Each different module type consists of a standard kernel, combined with module-dependent application circuitry. Module standardization results in more efficient module design and allows the implementation of the Standard I/O Architecture. The biggest benefit of standardization for intelligent modules is that it allows the use of a common command language or protocol (Interprocessor Communication Protocol in this case).

The intelligent kernel is based around a 68000 microprocessor. This design provides the full complement of VMEbus Requester and Interrupter options for master/slave interfacing, as well as all of the advantages provided by the various facets of the XYCOM Standard I/O Architecture (as covered earlier in this appendix).

The non-intelligent kernel provides the circuitry required to receive and generate all of the signals for a VMEbus defined 16-bit "slave" module. The non-intelligent kernel also employs the features of the XYCOM Standard I/O Architecture (as described earlier in this appendix).

The simplified diagrams below show the features of both the intelligent and the non-intelligent kernels.

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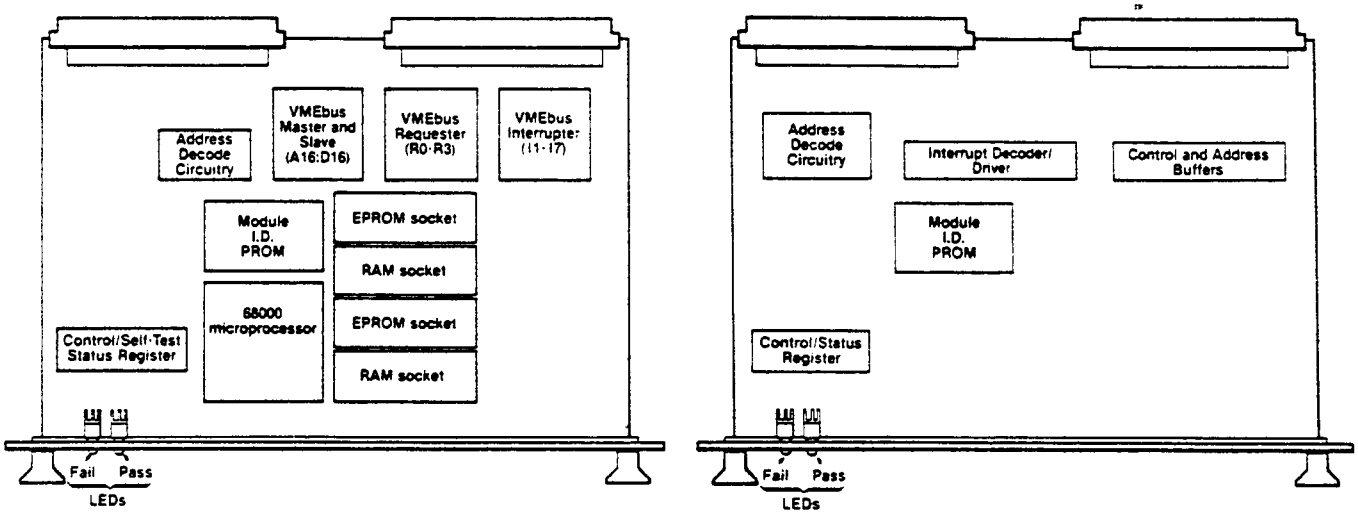


Figure A-5. Intelligent and Non-Intelligent Kernels

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Appendix B

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-530 Analog Output module is physically configured as a non-expanded (NEXP), double-height, VMEbus compatible board. There is one 96 pin bus connector on the rear edge of the board labeled P1, and one 96 pin bus connector labeled P2 (refer to Chapter 2, Figure 2-1 for the locations). The pin connections for P1 contain the standard address, data, and control signals necessary for the operation of NEXP modules. P2 contains additional +5 volt and ground connections for the module. The following tables identify the VMEbus signals by signal mnemonic, connector and pin number, and signal characteristic.

Table B-1. P1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B: 3	AC FAILURE - open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
IACKIN*	1A: 21	INTERRUPT ACKNOWLEDGE IN - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress. (Refer to Section 2.4.5.)
IACKOUT*	1A: 22	INTERRUPT ACKNOWLEDGE OUT - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress. (Refer to Section 2.4.5.)
AM0-AM5	1A: 23 1B: 16,17, 18,19 1C: 14	ADDRESS MODIFIER (bits 0-5) - Three-state driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification.
AS*	1A: 18	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A: 24-30 1C: 15-30	ADDRESS bus (bits 1-23) - Three-state driven address lines that specify a memory address.

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Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BBSY*	1B: 1	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B: 2	BUS CLEAR - Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.
BERR*	1C: 11	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG3IN**	1B: 4,6, 8,10	BUS GRANT (0-3) IN - Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals from a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master. (Refer to Section 2.4.7.)
BG0OUT*-BG3OUT*	1B: 5,7, 9,11	BUS GRANT (0-3) OUT - Totem-pole driven signals generated by Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant Out signal indicates to the next board that it may become the next bus master. (Refer to Section 2.4.7.)
BR0*-BR3*	1B: 12-15	BUS REQUEST (0-3) - Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A: 13	DATA STROBE 0 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DS1*	1A: 12	DATA STROBE 1 - Three state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).

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Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
DTACK*	1A: 16	DATA TRANSFER ACKNOWLEDGE - Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A: 1-8 1C: 1-8	DATA BUS (bits 0-15) - Three-state driven bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A: 9,11, 15,17,19 1B: 20,23 1C: 9 2B: 2,12 22,31	GROUND
IACK*	1A: 20	INTERRUPT ACKNOWLEDGE - Open-collector or three-state driven signal from any Master processing an interrupt request. Routed via the backplane to Slot 1, where it is looped back to become Slot 1 IACKIN* to start the interrupt acknowledge daisy-chain.
IRQ1*- IRQ7*	1B: 24-30	INTERRUPT REQUEST (1-7) - Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C: 13	LONGWORD - Three-state driven signal to indicate that the current transfer is a 32-bit transfer.
(RESERVED)	2B: 3	RESERVED - Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B: 21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B: 22	A reserved signal which will be used as the transmission line for serial communication bus messages.

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Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSCLK	1A: 10	SYSTEM CLOCK - A constant 16-MHz clock signal that is independent of processor speed or timing. This signal is used for general system timing use.
SYSFAIL*	1C: 10	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VMEbus.
SYSRESET*	1C: 12	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A: 14	WRITE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation; a low level indicates a write operation.
+5V STDBY	1B: 31	+5 Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
+5V	1A: 32 1B: 32 1C: 32	+5 Vdc Power - Used by system logic circuits.
+12V	1C: 31	+12 Vdc Power - Used by system logic circuits.
-12V	1A: 31	-12 Vdc Power - Used by system logic circuits.

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BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table B-2. P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GDN
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK (1)	A17
22	IACKOUT*	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

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Table B-3. P2 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
+5V	2B: 1,32	+5 Vdc Power - Used by system logic circuits.
GND	2G: 2,12 22,31	Ground
	ALL OTHER PINS NOT USED	

BACKPLANE CONNECTOR P2

The following table lists the P2 pin assignments by pin number order. (The connector consists of three rows of pins labeled A, B, and C.)

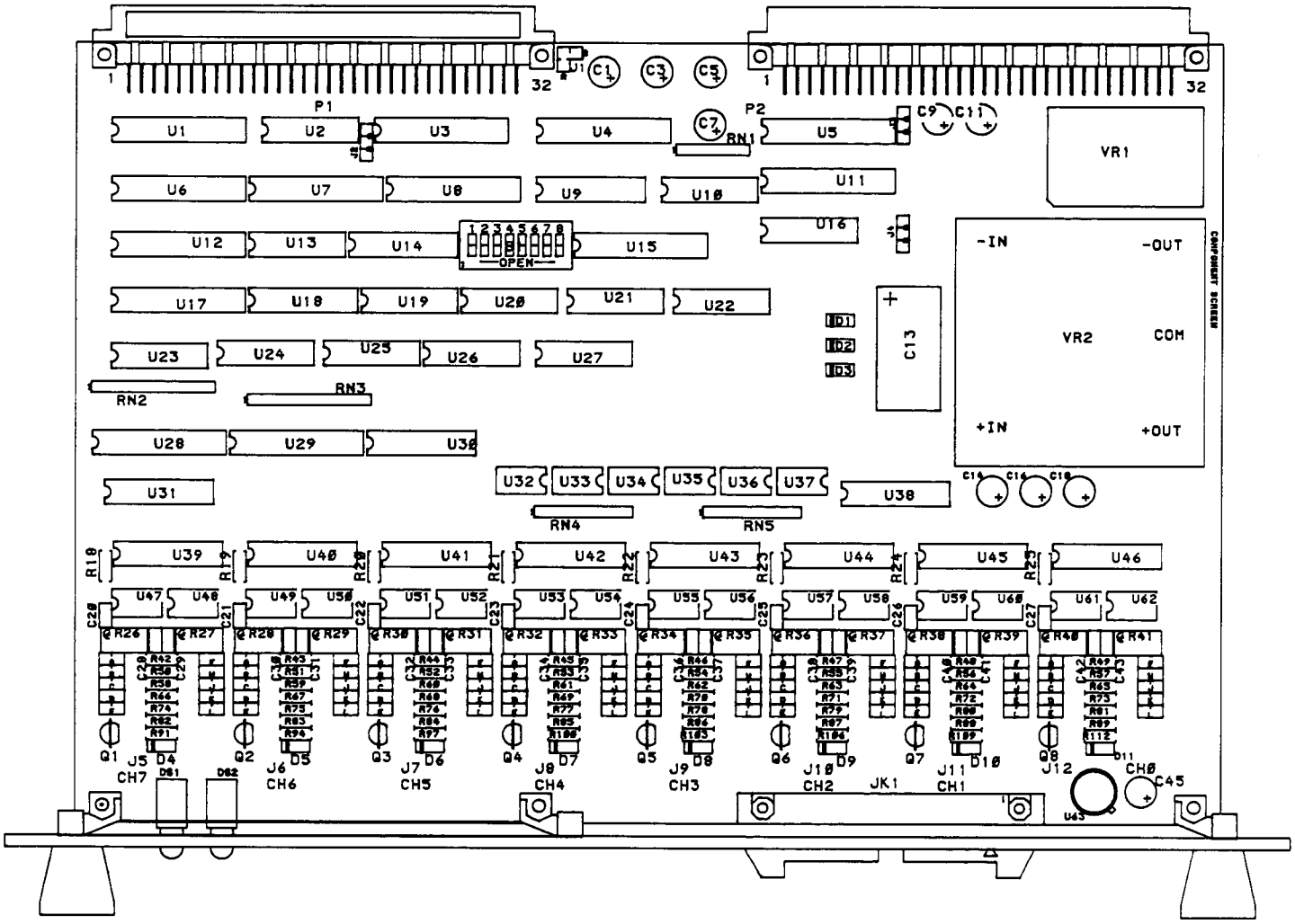
Table B-4. P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	- -	+5V	- -
2	- -	GND	- -
12	- -	GND	- -
22	- -	GND	- -
31	- -	GND	- -
32	- -	+5V	- -

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Appendix C

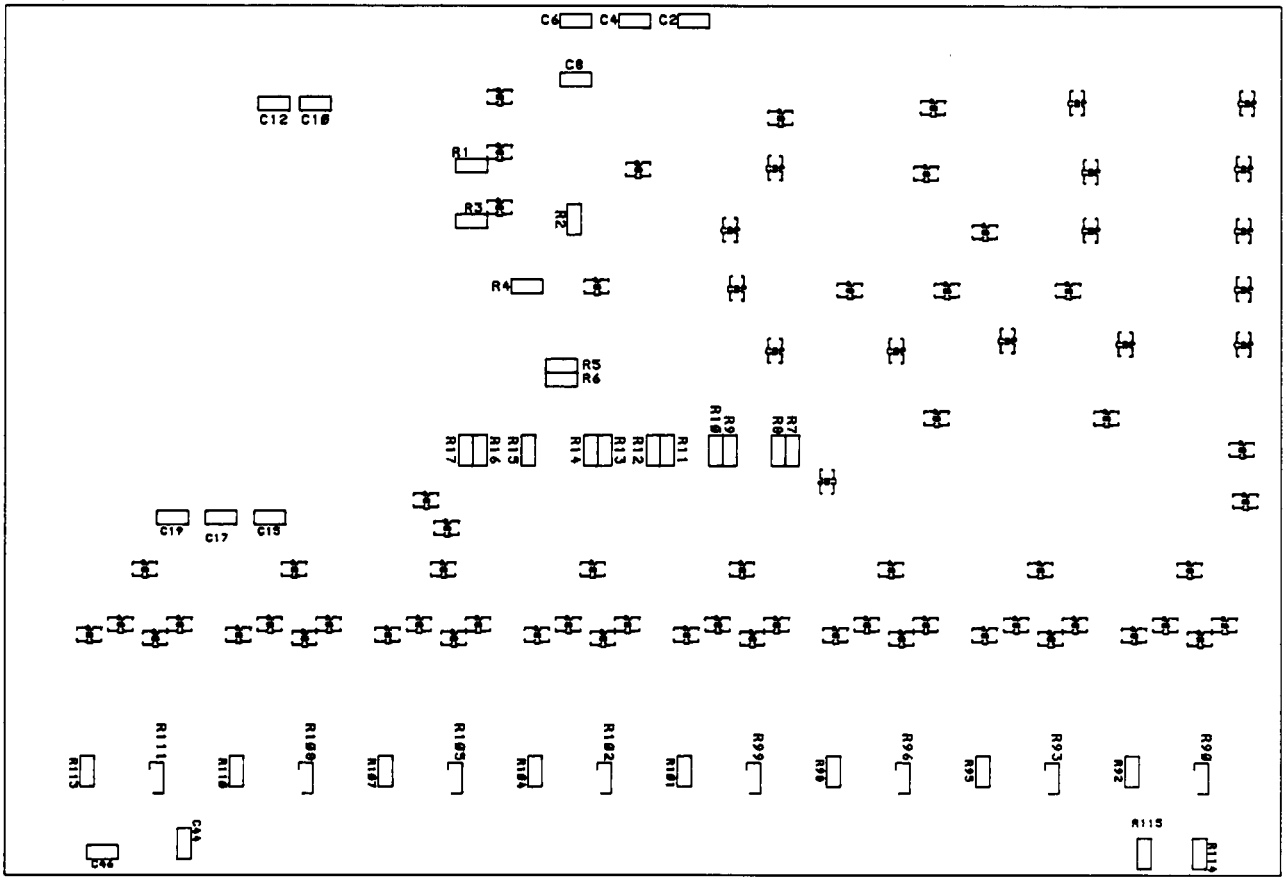
SCHEMATICS AND DIAGRAMS



XVME-530 (Rev. C) Assembly Drawing, Sheet 1 of 2

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SOLDER SIDE COMPONENTS



XVME-530 (Rev. C) Assembly Drawing, Sheet 2 of 2

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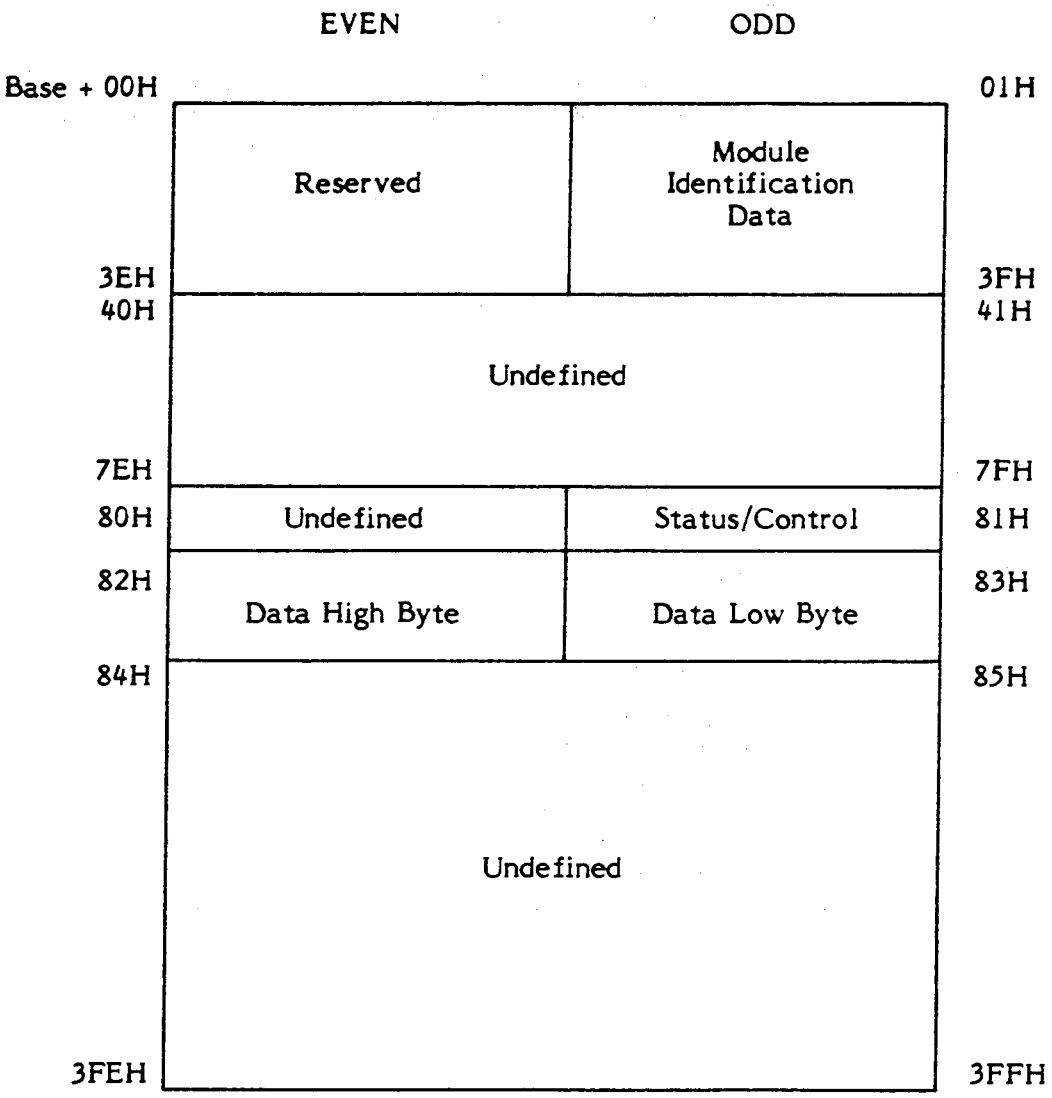
Insert Schematic Sheet Here

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Appendix D

QUICK REFERENCE GUIDE



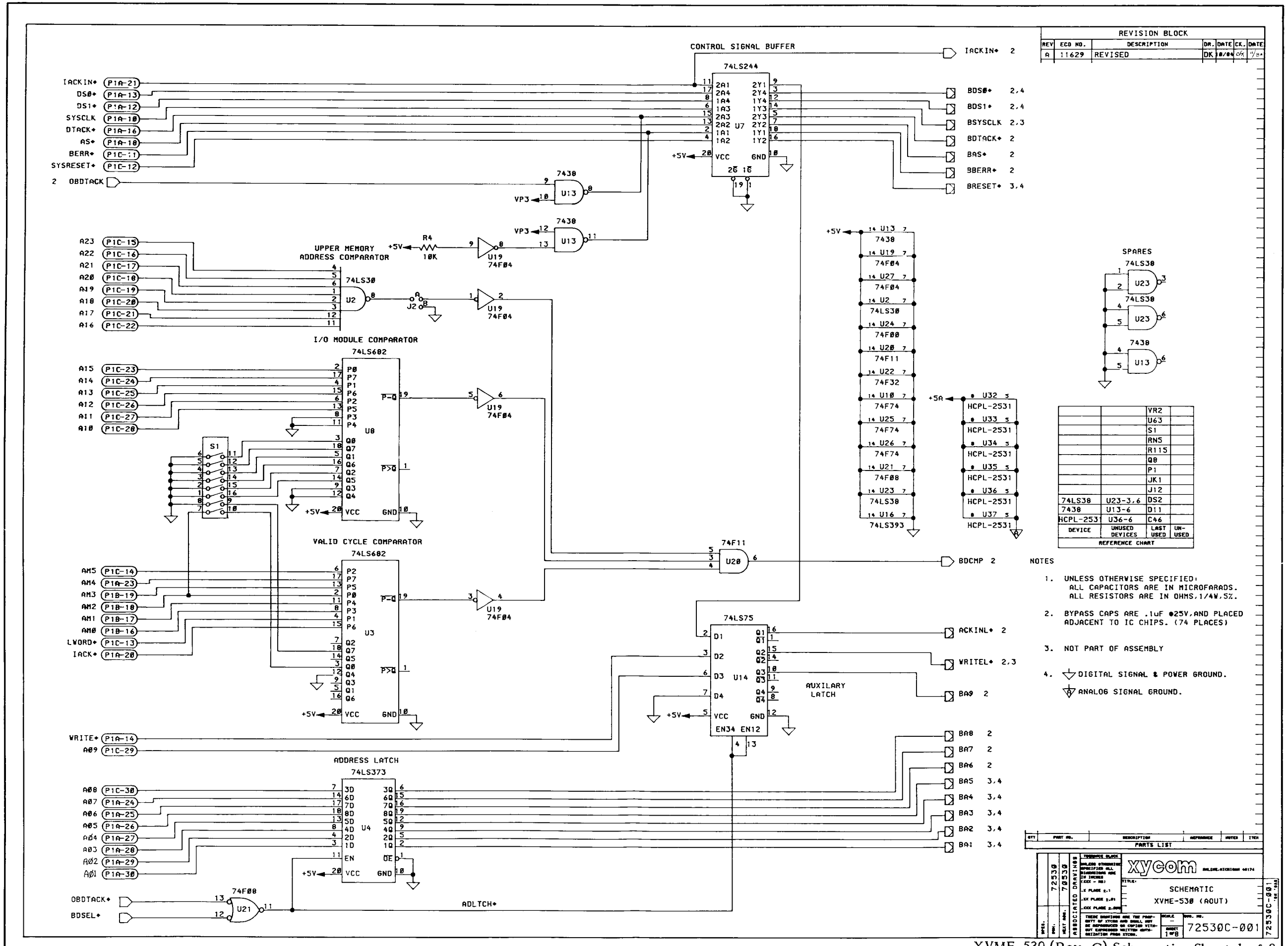
AOUT I/O Interface Block and its Possible Locations in Short I/O Address Space

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Table D-1. AOUT Jumper/Switch List

Jumper/Switch	Use
J1,J3,J4	Not used.
J2B	Jumper J2 must be in the "B" position.
J5-J12	Each jumper selects output voltage ranges for each of the 8 output ranges (J5=Ch. 7, J6=Ch. 6, J12=Ch. 0). Mode — Jumpers 4-20mA — F, H, J, K, L 0-10V — A, C 0-5V — A, C, E ±10V — A, B, D ±5V — A, B, C ±2.5V — A, B, C, E
Address Switches	
Switch 8	Always closed
Switch 7	Closed = both 29 and 2D Open = only 2D
Switches 0-6	Sets base address of AOUT: Switch 6: A15 Switch 5: A14 Switch 4: A13 Switch 3: A12 Switch 2: A11 Switch 1: A10

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XVME-530 (Rev. C) Schematic, Sheet 1 of 8

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ADDRESS DECODE AND
CYCLE TIMING GENERATOR

SEE NOTE 3
R6
+5V
10K

PAL16R4
U15

4 BUSY
1 BA9
1 BA8
1 BA7
1 BA6
1 WRITEL*
3 8MHZ
R2
+5V
10K
+5V

I6 I3 I2 I1 I0 I5 I7 I4 CK OE VCC
O0 O1 R3 R2 R1 R0 O2 O3 GND

(ST0*)
(ST1*)

U27
74F04

PROM* 3
RDSTB* 4
WRSTB* 4
OBDTACK* 1
OBDTACK 1
START 4

1 ACKINL*
74F00
U24
IOSEL*

74F08
U21

BOARD SELECT SAMPLER

BOARD SELECT TRAILING
EDGE SYNCHRONIZER

1 BDCMP
1 BBERR*
1 BDTACK*
74F32
U22
74F11
U20

P D CK CL Q
U26 U25
74F74
VP2
VP3

1 BSYSCLK
1 BDS0*
1 BDS1*
74F00
U24
U27
74F04

74F00
U24
U27
74F04
BDSEL* 1

RN1
+5V
10K

74F32
U22
74F08
U21
74F32
U22
BUFEN* 3

IACKOUT FF
VP2
P D CK CL Q
U10
74F74

74F08
U21
74F32
U22

J1
A
B
IACKIN* 1
P1A-22 IACKOUT*

U27
74F04

1 BAS*

REVISION BLOCK						
REV	ECO NO.	DESCRIPTION	DR.	DATE	CK.	DATE
A		SEE SHEET 1				

PARTS LIST

QTY	PART NO.	DESCRIPTION	REFERENCE	NOTES	ITEM

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XX = .01) .X PLACE ±.1 .XX PLACE ±.01 .XXX PLACE ±.005

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TITLE: SCHEMATIC
XVME-530 (AOUT)

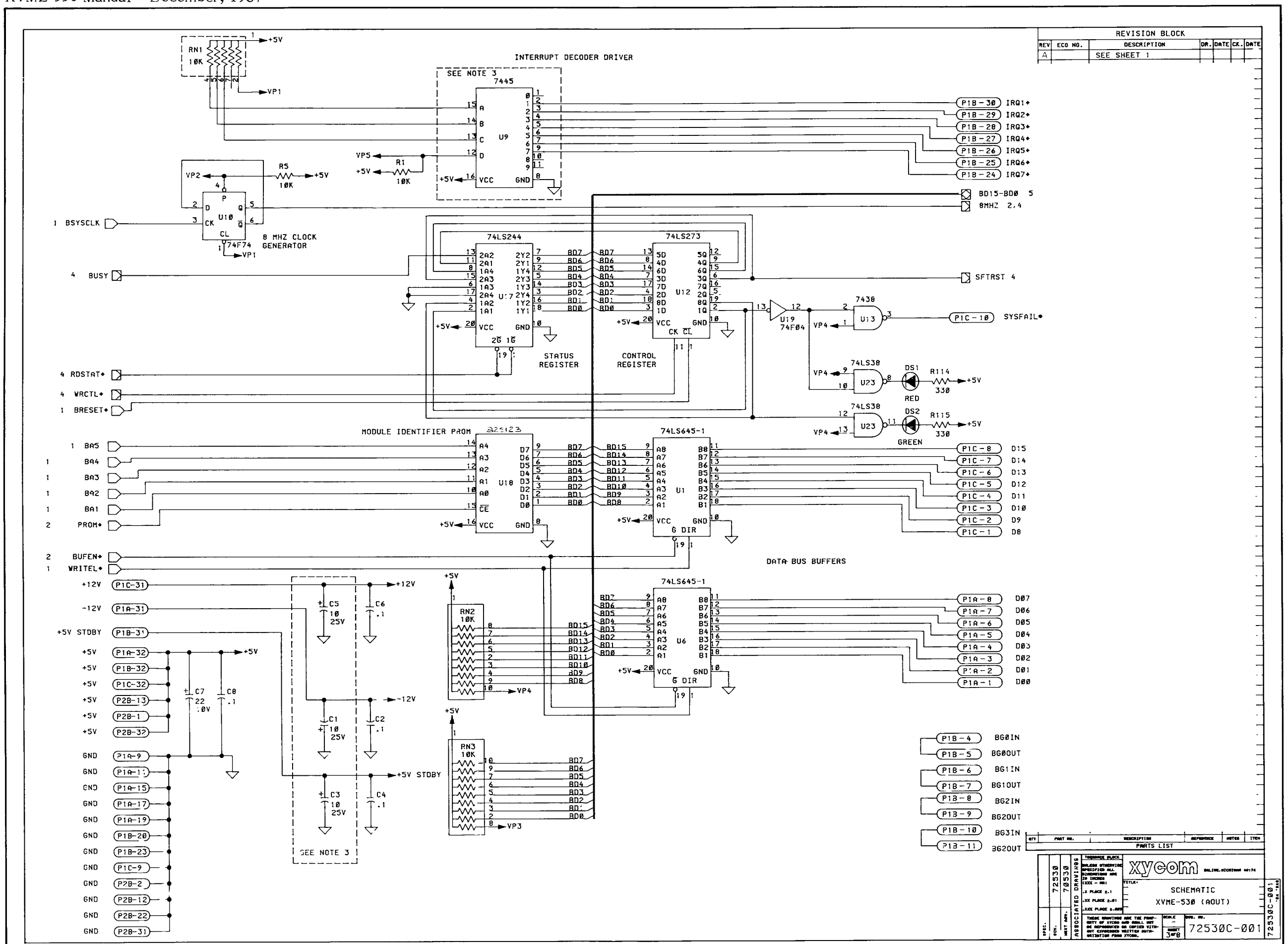
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72530 ASSOCIATED DRAWINGS
72530

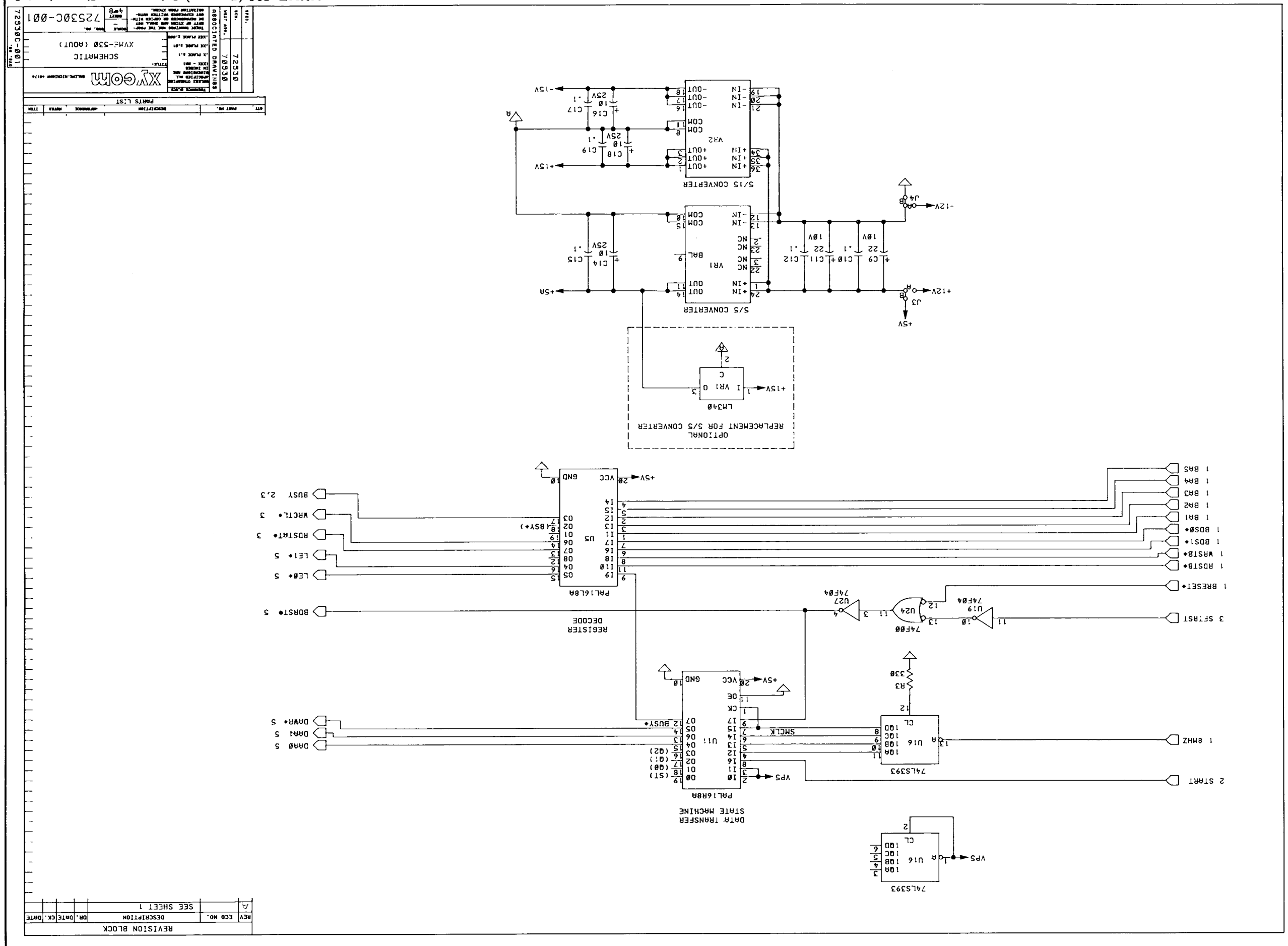
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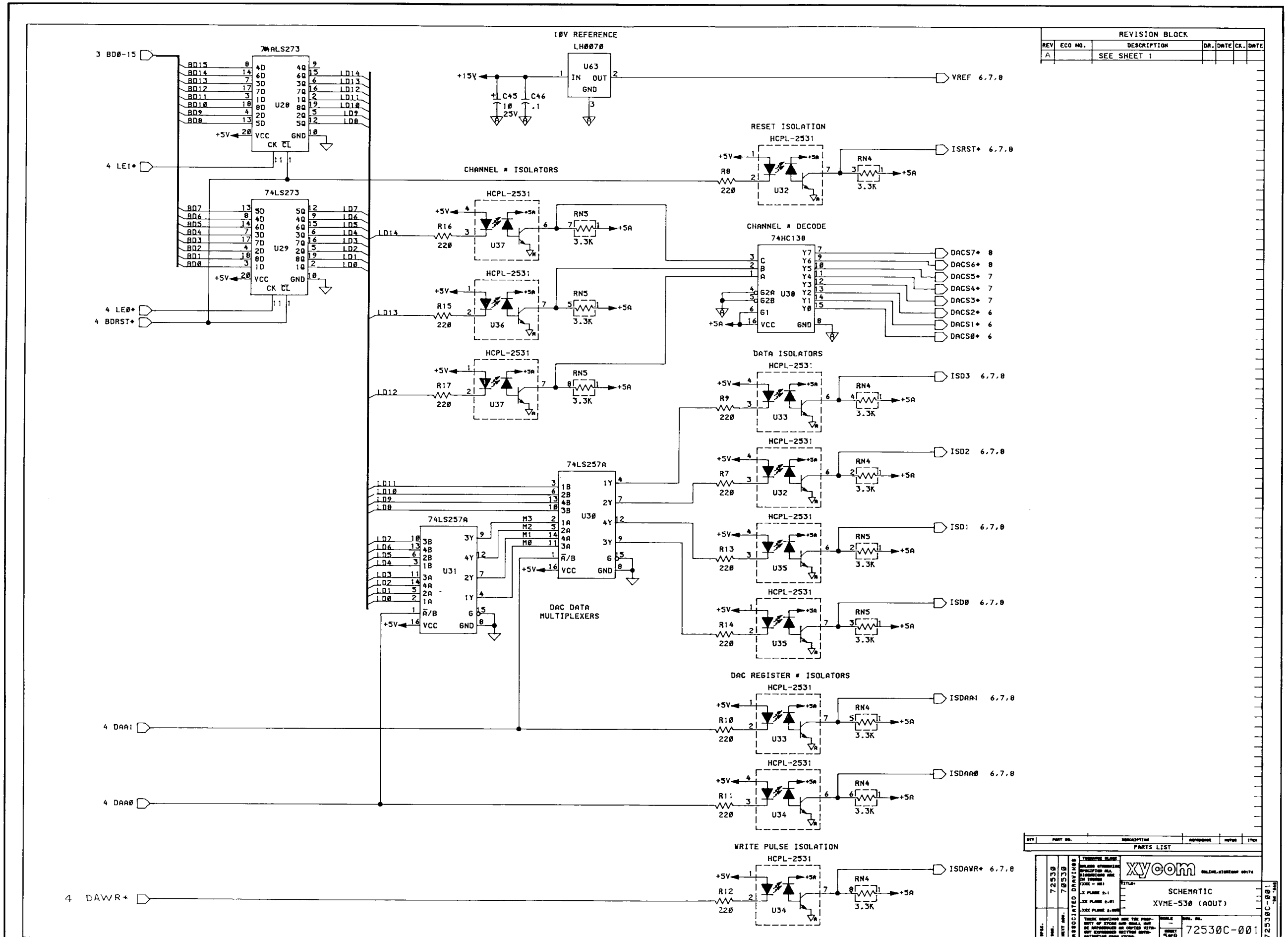
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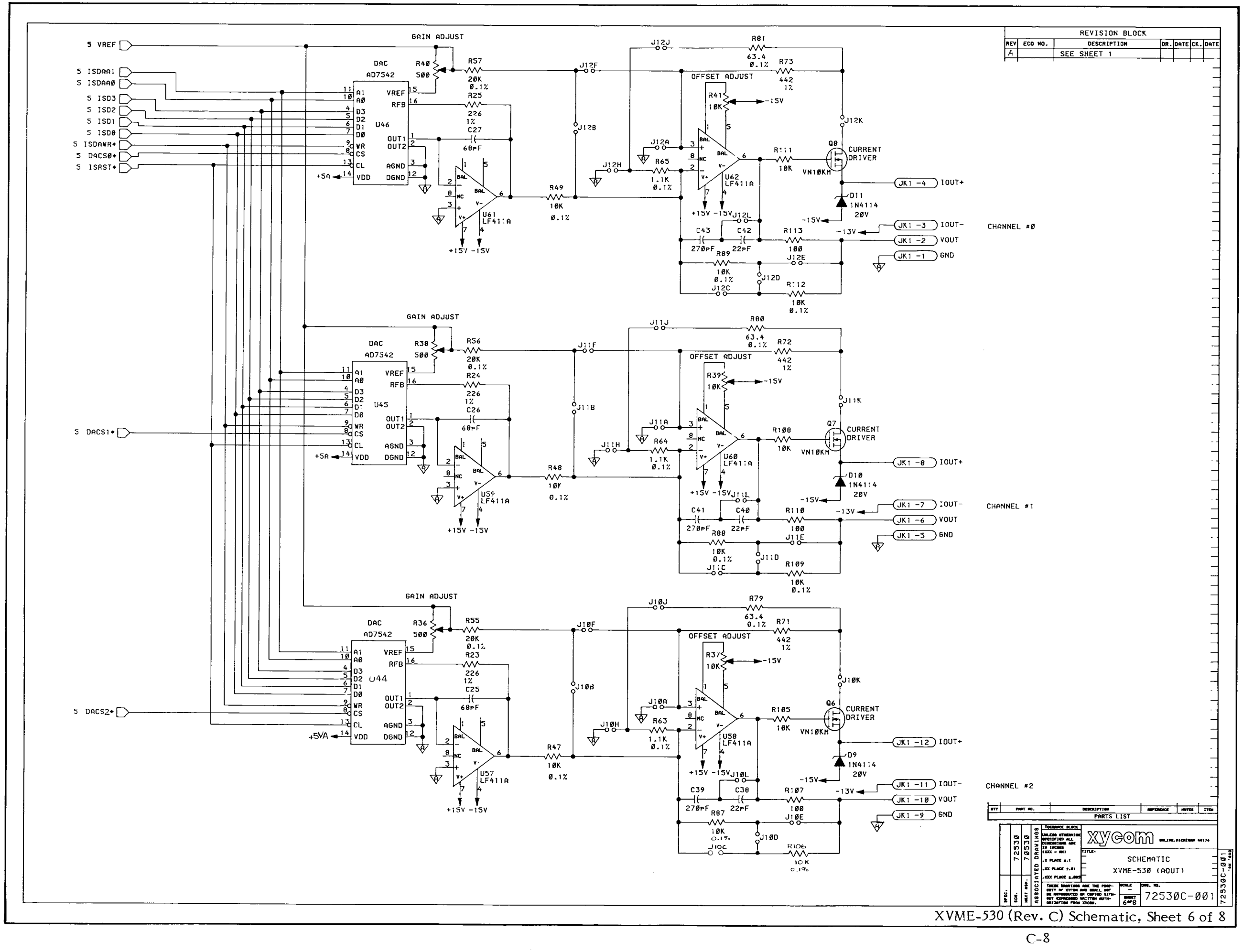
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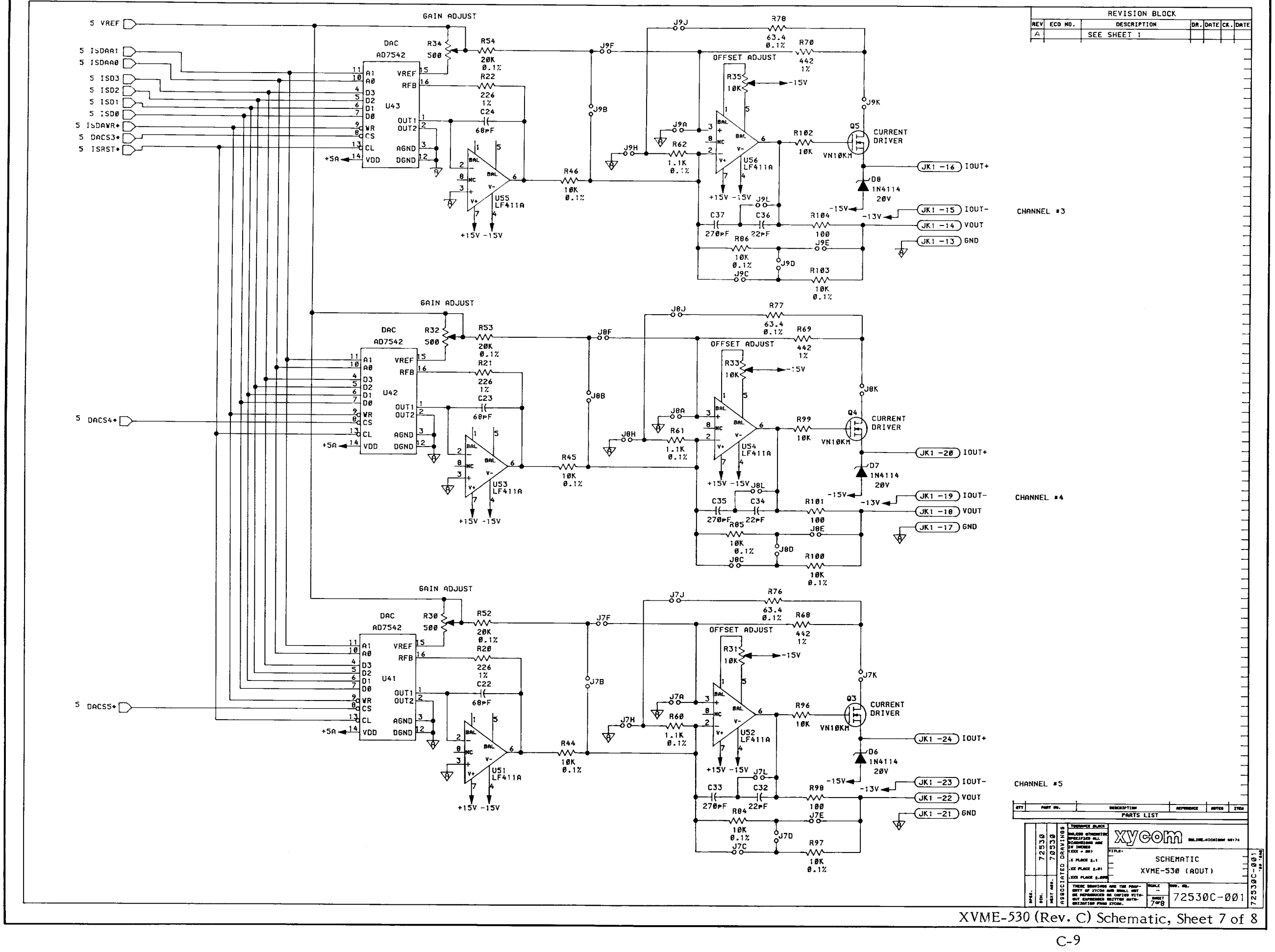


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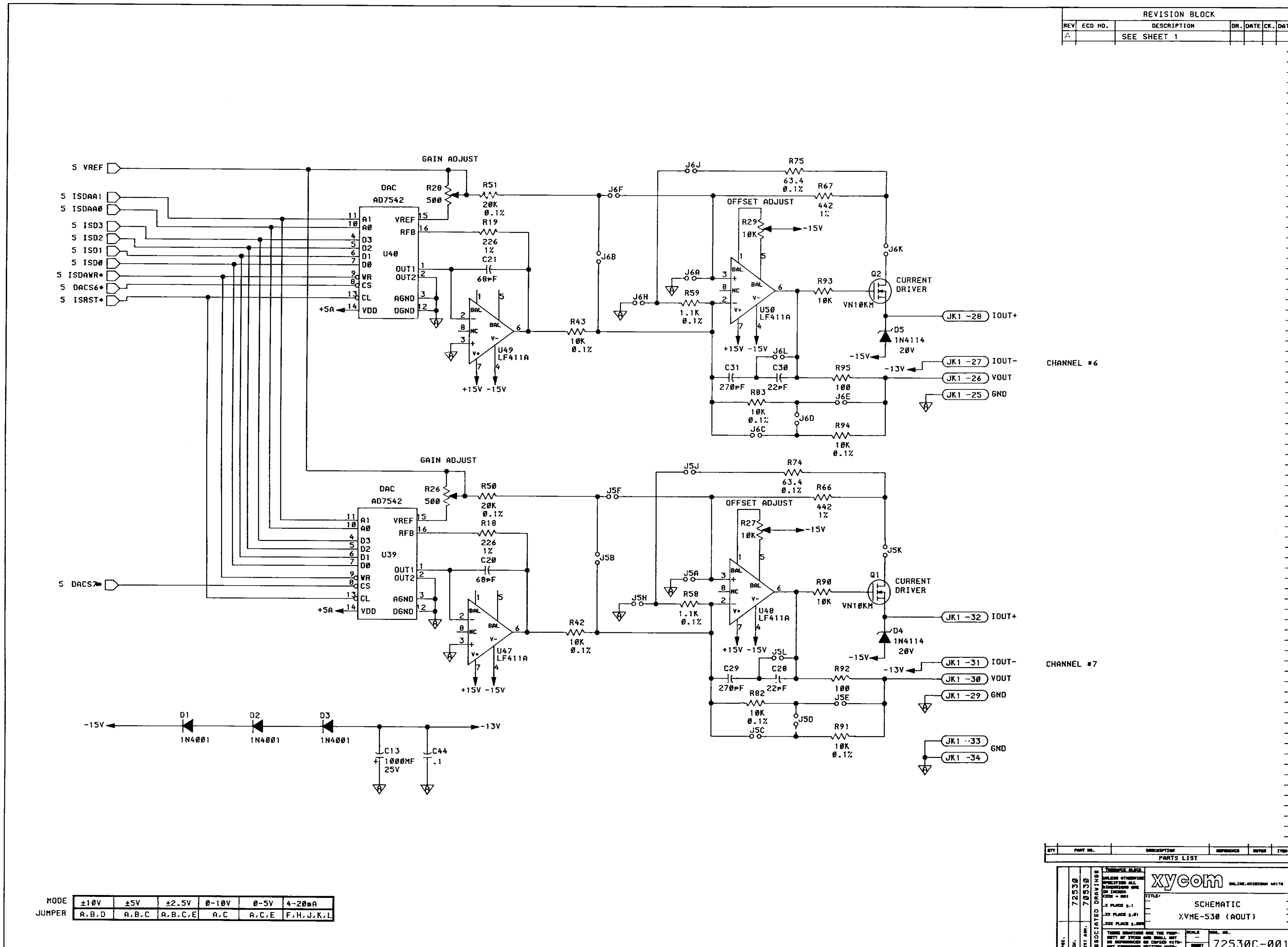
XVME-530 (Rev. C) Schematic, Sheet 6 of 8

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XVME-530 (Rev. C) Schematic, Sheet 7 of 8

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MODE	±10V	±5V	±2.5V	0-10V	0-5V	4-20mA
JUMPER	A,B,D	A,B,C	A,B,C,E	A,C	A,C,E	F,H,J,K,L

XVME-530 (Rev. C) Schematic, Sheet 8 of 8

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