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XVME-560

Analog Input Module

P/N 74560-001D

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The XVME-360 Analog Input Module (hereafter referred to as the AIN) is a VMEbus compatible module which can perform 12-bit resolution A/D conversions on up to 64 different input channels. The AIN can be programmed to operate in the following four different modes:

- single channel conversion
- repeated conversions on one channel
- conversions on sequential channels
- external triggering of conversion

Other features of the AIN include:

- Jumper selectable voltage input ranges of ±10V, ±2.5V, 0-I0V, ±5V, o-5v
- Programmable gain of 1,2,4 or 8
- Can interrupt at any VMEbus level (11-17) (STAT)
- 20 KHz conversion rate

Possible applications for the AIN are:

- Data acquisition
- Closed loop process control
- Pressure sensing
- Temperature sensing

1.2 HOW THIS MANUAL IS ORGANIZED

This chapter provides a functional overview of the AIN and presents the features of XYCOM's Standard I/O Architecture. Operational aspects of the AIN are then explained in the following fashion:

Chapter Two - Installation -- Presents information required for module installation.

Chapter Three - Programming -- Presents information required to program operating modes, access data, and perform module calibration.

The appendices at the rear of this manual provide information on XYCOM's Standard I/O Architecture, VMEbus connector/pin description, module schematics and a quick reference of module addresses and jumpers.

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1.3 FUNCTIONAL OVERVIEW

The XVME-AIN is a 64 channel (single ended input), 32 channel (differential input), analog input module designed to operate on the VMEbus backplane. It is comprised of two sections: an analog section containing circuitry needed to perform the analog to digital conversion, and the XYCOM Non-Intelligent Kernel section, which interfaces the analog circuitry to the VMEbus. An operational block diagram showing these sections is presented in Figure 1-1 below.

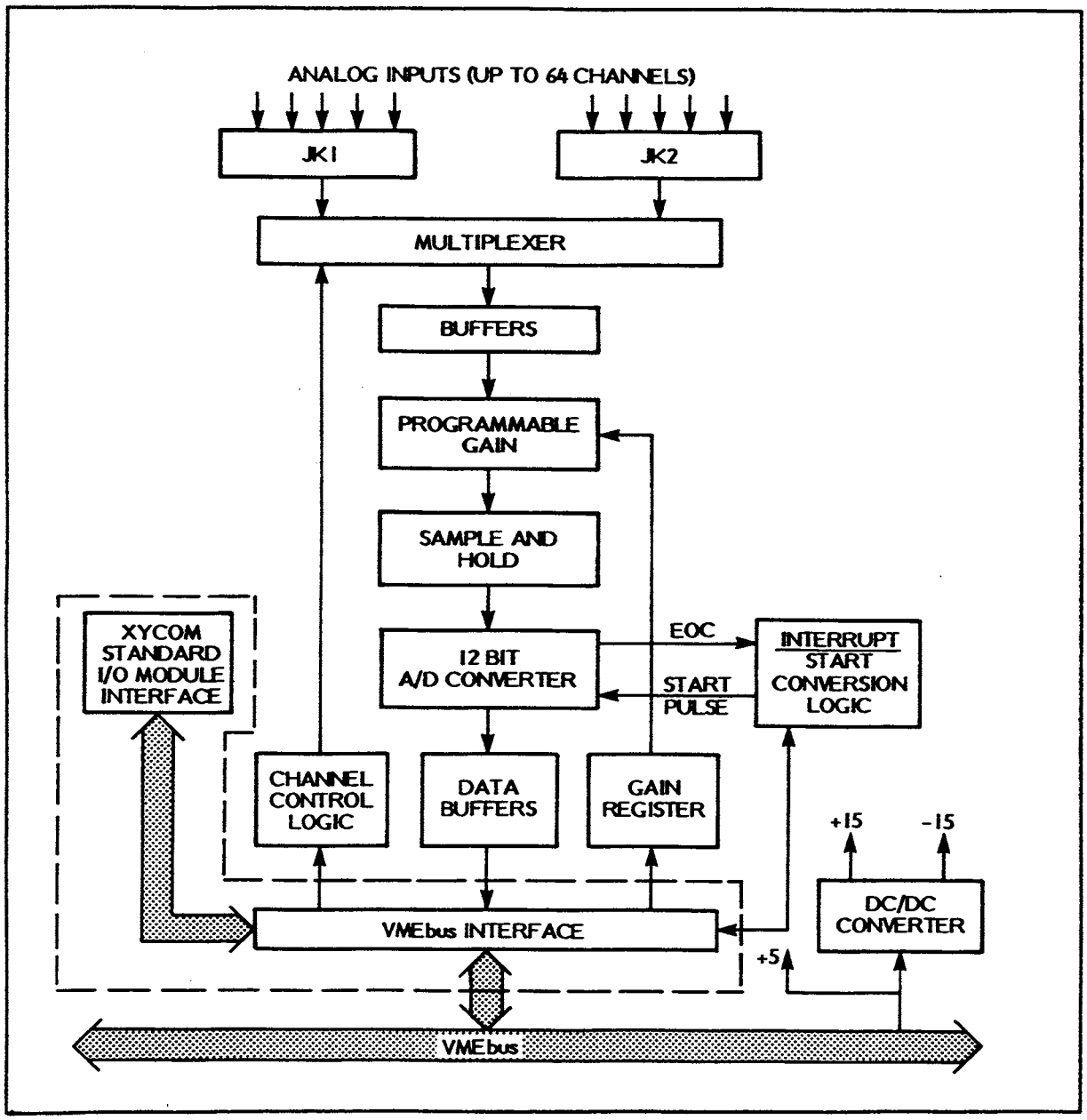


Figure 1-1. Operational Block Diagram of XVME-560

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1.3.1 Analog Circuitry

As can be seen from Figure l-1, the application circuitry consists primarily of the 12-bit A/D converter and its related signal conditioning components listed below:

Multiplexer: directed by software (see Chapter 3) to select one channel for data conversion.

Buffer (Instrumentation Amplifier): provides a high impedance front end to the analog signal coming out of the multiplexer.

Programmable Gain: allows a gain of 1, 2, 4 or 8 to be selected for increased conversion resolution on smaller input signals.

Sample and hold: samples the input signal for 23 usec to allow for "settling time" in the Instrumentation Amplifier and gain circuitry. This signal is then "held" until the conversion is completed.

Interrupt circuitry: allows a conversion completion to generate an interrupt (see Section 3.8).

1.3.2 XYCOM Non-Intelligent Kemel

The Non-Intelligent Kernel is basically the interface to the VMEbus. It provides all the necessary circuitry to receive and generate the signals required by the VMEbus specification for a 16-bit slave. By simply adding the application circuitry (in this case A/D circuitry), a VMEbus module is complete. The Non-Intelligent Kernel has the following features:

Control and Address Buffers

- Address Decode circuitry
- Interrupt Decoder/Driver
- Control/Status Register
- Module identification information
- Pass and Fail LED indicators

The XYCOM Non-Intelligent Kernel is described in further detail in Appendix A.

1.4 FEATURES OF XYCOM'S STANDARD I/O ARCHITECTURE

The AIN and all XYCOM I/O modules conform to the unique XYCOM VMEbus Standard I/O Architecture. This architecture is intended to make the programming of XYCOM VMEbus I/O modules simple and consistent. The following features apply to the operation of the AIN.

- Module Address - The AIN can be located at any one of 64 base addresses in VMEbus Short I/O memory.

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- Module Address Space - The AIN occupies 1K of Short I/O Address Space known as the I/O Interface Block which contains all of its programming registers.

- Module Identification - The AIN has I.D. information which provides its name, model number, manufacturer and revision level at a location that is consistent with other XYCOM I/O modules.

A detailed description of XYCOM I/O Architecture is presented in Appendix A at the rear of this manual.

1.5 SPECIFICATIONS

MODULE SPECIFICATIONS	
Analog Inputs	
No. of Analog Inputs	
Single-ended	64
Differential	32
Input Voltage Ranges (jumper-selectable)	
Unipolar	0-5V, 0-I0V
Bipolar	±2.5V, ±5V, ±10V
Software Programmable Gain	1, 2, 4, 8
Effective Full Scale Input Ranges	
Unipolar	0-625mV to 0-I0V w/Gain value
Bipolar	±312.5mV to ±10V w/Gain value
Maximum Input Voltage (without damage)	
Power on	44v
Power off	30v
Input Impedance	
with 22 Mohm resistor	17 M (min.)
without 22 Mohm resistor	100 M (min.)
Bias Current	±100NA max.
Input Capacitance	225pf max.
Operating Common Mode Voltage	+14v

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Accuracy	
Resolution	12 bits
Linearity	±1/2 LSB
Differential Linearity	±1/2 LSB
System Accuracy	
with Gain = 1	±0.025% of FSR
with Gain = 8	±0.05% of FSR
System Accuracy Temperature Drift	
±10V at Gain = 1	40 ppm/°C
±2.5V at Gain = 8	75 ppm/°C
CMRR	74db min.
Monotonicity	guaranteed
Speed	
Conversion time	50 uSec
Throughput	20K conversions/sec
Delay from External Trigger to Sampling	23 us
Power Requirements	+5V Typ. - 2.00A Max. - 2.50A
Environmental	
Temperature	
Operating	0 to 65°C
Non-Operating	-40 to 85°C
Humidity	5 to 95% RH non-condensing
Altitude	
Operating	Sea-level to 20,000 ft.
Non-Operating	Sea-level to 50,000 ft.
Vibration	
Operating	5 to 2000 Hz .015 inches peak-to-peak displacement 2.5 g peak (maximum) acceleration
Non-Operating	5 to 2000 Hz .030 inches peak-to-peak displacement 5.0 g peak (maximum) acceleration

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Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-Operating	50 g peak acceleration, 11 msec duration
Physical Specifications	
Double Height VME board 233.35 mm x 160 mm (9.2" x 6.3")	

VMEbus COMPLIANCE

Fully compatible with VMEbus standard

Al 6:D16 Data Transfer Bus slave

I(1) - I(7) (STAT) (Programmable Vector)

Base address jumper-selectable within VMEbus Short I/O or Memory-Mapped Address Space

Occupies 1K consecutive byte locations

Includes XYCOM's standard I/O module interface

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Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter provides the information necessary to configure the AIN for installation in a VMEbus backplane cardcage. The components relevant to installation are discussed and the installation procedure is presented.

2.2 SYSTEM REQUIREMENTS

The AIN is a double-height VMEbus compatible module. To operate it must be properly installed in a VMEbus backplane cardcage. The minimum system requirements for operation of the AIN are one of the following:

A) ● A host processor properly installed on the same backplane.

l A properly installed controller subsystem with the following features:

-- Data Transfer Bus Arbiter
-- System Clock driver
-- System Reset driver
-- Bus time-out module

An example of such a controller subsystem is the XYCOM XVME-010 System Resource Module (SRM).

-- OR --

B) l A host processor which incorporates an on-board controller subsystem.

2.3 JUMPERS/SWITCHES

Prior to installing the AIN, it will be necessary to configure several jumper/switch selectable options. These options fall into two categories: VMEbus-related options and Analog-to-Digital conversion options.

VMEbus Options

- Module base address, selected by switches 1-6 on Switch Bank 2.
- l Address space used by the module, selected by J2 and switch 7 on Switch Bank 2.
- l Privilege level required to access module, selected by switch 8 on Switch Bank 2.
- l The interrupt level used by the module, selected by switches l-3 on Switch Bank 1.

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Analog to Digital Conversion Options

- The channel configuration, either single-ended inputs or differential inputs. Selected by jumpers J10, Jll, J13, J14.
- One of the five different input scaling ranges. Selected by jumpers J5, J6, J7, J8, and J9.
- The digital data format for the digital value produced as a result of an A/D conversion, either straight binary, offset binary or two's complement. Selected by jumpers J3 and J4.
- If Channel zero is to be used as a ground reference. Selected by jumpers J15 and Jl6.

Table 2-l. AIN Jumper/Switch List

Jumper/Switch	Use
JlB	Enables IACKIN*/INACKOUT* daisy chain (this is a hardwired jumper and is always installed).
J2A J2B	Memory mapped operation. Short I/O operation.
J3A J3B J4A J4B	These jumpers select the kind of digital code that will be produced as a result of reading an analog signal (see Table 2-V).
J5 J6 J7 J8 J9	These jumpers select one of the five input scaling ranges used (see Table 2-8).
Jl0A Jl0B Jll J13 Jl4A Jl4B	These jumpers select between single-ended or differential input (see Table 2-7).
J12	Test purposes only - J12B always installed.
J15 J16	Used in grounding channel zero for a ground reference (see Table 2-10).
Switch Bank 1	Interrupt Level Select switches.
Switch Bank 2	Base Address address space and privilege level select switches (see Tables 2-2, 2-3 and 2-4).

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2.4 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers and connectors to be configured on the AIN are shown in Figure 2-1 below.

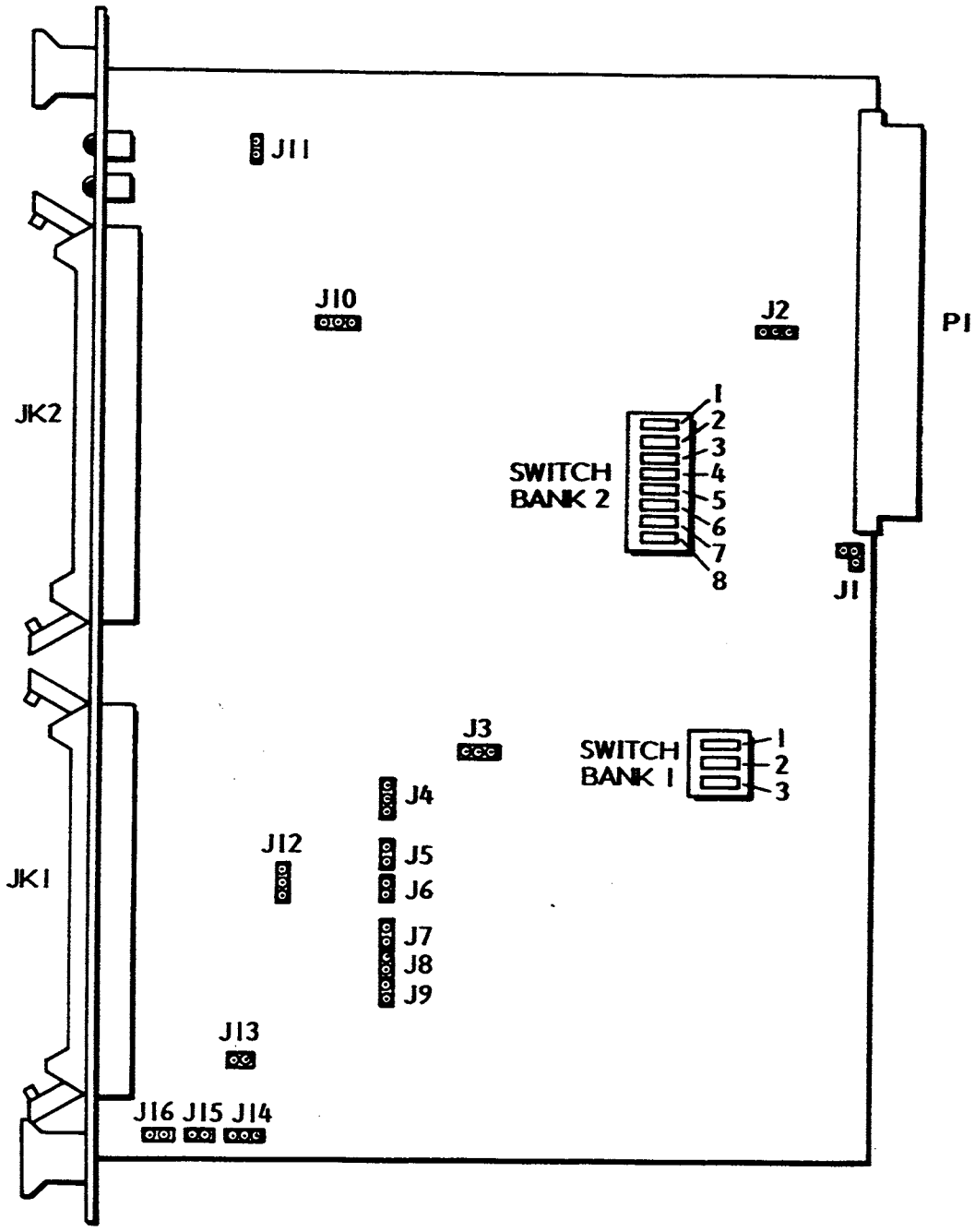


Figure 2-1. AIN Jumpers, Switches, and Connectors

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2.4.1 Base Address Switches

The AIN has been constructed in accordance with XYCOM's Standard I/O Architecture (see Appendix A for a detailed description). As such, it can occupy any one of 64 1K blocks of memory within the 64K VMEbus Short I/O Address Space. The particular 1K block it shall reside in is selected by configuring the AIN's "Base Address" equal to the beginning address of that block. The Base Address is selected by configuring switches 1-6 in Switch Bank 2 (see Figure 2-2), as shown below in Table 2-2.

Table 2-2. Base Address Switch Options

Switches						VME base address in VME Short I/O Address space
6(A15)	5(A14)	4(A13)	3(A12)	2(A11)	1(A10)	
0	0	0	0	0	0	0000H
0	0	0	0	0	1	0400H
0	0	0	0	1	0	0800H
0	0	0	0	1	1	0C00H
0	0	0	1	0	0	1000H
0	0	0	1	0	1	1400H
0	0	0	1	1	0	1800H
0	0	0	1	1	1	1C00H
0	0	1	0	0	0	2000H
0	0	1	0	0	1	2400H
0	0	1	0	1	0	2800H
0	0	1	0	1	1	2C00H
0	0	1	1	0	0	3000H
0	0	1	1	0	1	3400H
0	0	1	1	1	0	3800H
0	0	1	1	1	1	3C00H
0	1	0	0	0	0	4000H
0	1	0	0	0	1	4400H
0	1	0	0	1	0	4800H
0	1	0	0	1	1	4C00H
0	1	0	1	0	0	5000H
0	1	0	1	0	1	5400H
0	1	0	1	1	0	5800H
0	1	0	1	1	1	5C00H
0	1	1	0	0	0	6000H
0	1	1	0	0	1	6400H
0	1	1	0	1	0	6800H
0	1	1	0	1	1	6C00H
0	1	1	1	0	0	7000H
0	1	1	1	0	1	7400H
0	1	1	1	1	0	7800H
0	1	1	1	1	1	7C00H
1	0	0	0	0	0	8000H
1	0	0	0	0	1	8400H
1	0	0	0	1	0	8800H
1	0	0	0	1	1	8C00H
1	0	0	1	0	0	9000H
1	0	0	1	0	1	9400H
1	0	0	1	1	0	9800H
1	0	0	1	1	1	9C00H
1	0	1	0	0	0	A000H
1	0	1	0	0	1	A400H
1	0	1	0	1	0	A800H
1	0	1	0	1	1	AC00H
1	0	1	1	0	0	B000H
1	0	1	1	0	1	B400H
1	0	1	1	1	0	B800H
1	0	1	1	1	1	BC00H
1	1	0	0	0	0	C000H
1	1	0	0	0	1	C400H
1	1	0	0	1	0	C800H
1	1	0	0	1	1	CC00H
1	1	0	1	0	0	D000H
1	1	0	1	0	1	D400H
1	1	0	1	1	0	D800H
1	1	0	1	1	1	DC00H
1	1	1	0	0	0	E000H
1	1	1	0	0	1	E400H
1	1	1	0	1	0	E800H
1	1	1	0	1	1	EC00H
1	1	1	1	0	0	F000H
1	1	1	1	0	1	F400H
1	1	1	1	1	0	F800H
1	1	1	1	1	1	FC00H

NOTE

Open = Logic "1"
Closed = Logic "0"

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2.4.2 Address Space Selection

The user is given the option of placing the AIN in VMEbus Short I/O or Standard Memory Space. The selection is made by configuring jumper J2 and Switch 8 of Switch Bank 2 (see Figure 2-2) as shown in Table 2-3 below.

Table 2-3. Addressing Options

Jumper	Switch 8	Option Selected
J2A J2B	Open Closed	Standard Data Access Operation Short I/O Access Operation

If jumper J2A is installed, Switch 8 must be set to open.

If jumper J2B is installed, Switch 8 must be set to closed.

The Standard I/O Architecture recommends that the AIN operate within the Short I/O Address Space, in order to take advantage of the Standard I/O Architecture's various features, which are described in Appendix A.

If required, the AIN can operate in the Standard Address Space. The user should note that in this mode, the AIN will always reside within the last 64K byte segment of the Standard Memory Address Space (i.e., the address range FFOOOOH through FFFFFFH).

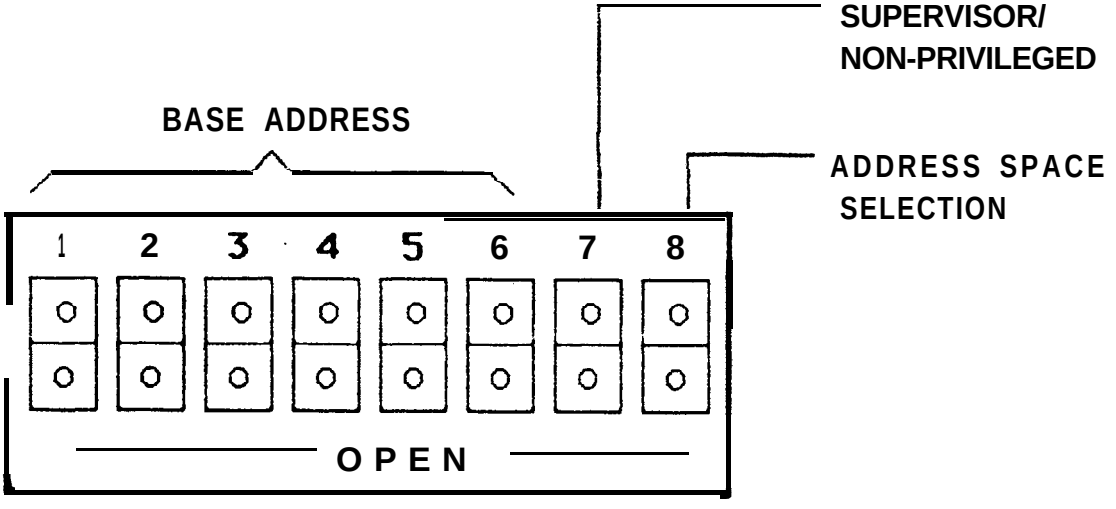


Figure 2-2. Switch Bank Two

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2.4.3 Supervisor/Non-Privileged Mode Selection

The AIN can be configured to respond to only Supervisory access, or to both Non-Privileged and Supervisory accesses, by selecting the position of Switch 7 (located in Switch Bank 2, see Figure 2-2), as shown in Table 2-4 below.

Table 2-4. Privilege Options

Switch 7	Privilege Mode Selected
Closed	Supervisory or Non-Privileged
Open	Supervisory Only

2.4.4 Address Modifier Reference

The following table (Table 2-5) indicates the actual VMEbus Address Modifier code that the AIN will respond to based on the position of the two options discussed in the previous two sections.

Table 2-5. Address Modifier Code Options

	Switches 7	8	Jumper J2	Address Modifier Code AIN will respond to
Short I/O	Closed	Closed	B	29H or 2DH
	Open	Closed	B	2DH only
Standard Address	Closed	Open	A	39H or 3DH
	Open	Open	A	3DH only

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2.405 IACKIN/IACKOUT Daisy Chain

The AIN has the ability to generate a VMEbus interrupt. Therefore, jumper J1 is hardwired in position "B" to enable the IACKIN/IACKOUT daisy chain.

CAUTION

The jumper shorting IACKIN to IACKOUT for the AIN's slot in the backplane must be removed, or the AIN may be damaged.

2.4.6 Interrupt Level Switches

Figure 2-3 shows Switch Bank 1 with its three interrupt level select switches. Table 2-6 illustrates their use.

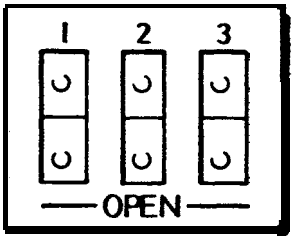


Figure 2-3. Switch Bank 1 Interrupt Level Select Switches

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Table 2-6. Interrupt Level Options

Switches 3	2	1	Level
0	0	0	No Level selected
0	0	1	Level 1
0	I	0	Level 2
0	1	1	Level 3
1	0	0	Level 4
1	0	1	Level 5
1	1	0	Level 6
1	1	1	Level 7

NOTE

Open = Logic "1"
Closed = Logic " 0 "

2.4.7 BGxIN/BGxOUT Daisy chain

The Data Bus Arbitration signals BGxIN and BGxOUT (where " x " can be a number 0-3 to represent the three levels of arbitration) are not used by the AIN, and are hardwired together on the module to allow the BGxIN/BGxOUT Daisy Chain to pass through the backplane slot occupied by the AIN. In each slot of the VMEbus backplane, there are four sets of jumpers shorting the signal BGxIN to BGxOUT (x=0 thru 3). Since these signals are already hardwired on the AIN, it is not necessary to insert these VMEbus jumpers on the slot occupied by the AIN.

2.4.8 Miscellaneous Jumpers

Jumper J12 enables the output of the Instrumentation amplifier for test purposes only and is left fixed in the "A" position.

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Analog to Digital Conversion Options

2.4.9 Channel Configuration Jumpers

The AIN can operate in either single-ended or differential mode. In differential mode, the AIN converts the analog voltage difference between two inputs. In single-ended mode, the AIN converts the analog voltage on one channel with respect to Analog Ground. If the AIN functions in single-ended mode, 64 input channels are available; if it functions in differential mode, 32 channels are available.

Table 2-7 describes how jumpers Jl0, Jll, J13, and J14 select the input mode.

Table 2-7. Analog Input Options

Option	Jumpers Inserted
Single-ended Input	JI0B, J13, JI4A
Differential Input	Jl0A, Jll, Jl4B

2.4.10 Analog Input Range

The AIN provides five different input scaling ranges which are selected by jumpers J5, J6, J7, J8 and J9 (see Figure 2-4). Any voltage above the specified range will be given the maximum (+ full scale) 12-bit value; any voltage below the specified range will be given the minimum value (or - full scale) (see also Section 3.6.l). Table 2-8 demonstrates how these options are selected.

Table 2-8. Input Scaling Options

Input Range	Jumpers Inserted	Jumpers Removed
±2.5 volts	J6,J7,J8	J5,J9
±5 volts	J6, J8	J5,J7,J9
+10 volts	J6, J9	J5,J7,J8
0 to +5 volts	J5,J7,J8	J6,J9
0 to +lOvolts	J5, J8	

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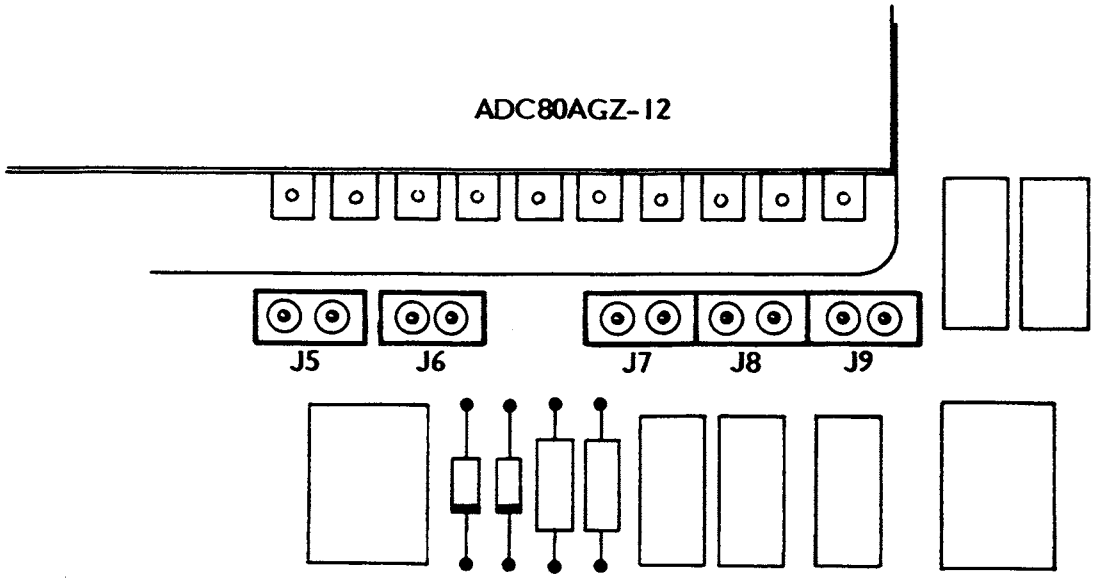


Figure 2-4. Input Scaling Jumpers

2.4.11 Digital Data Format Option Jumpers

Jumpers J3 and J4 select the kind of digital data format that will represent the result of an Analog to Digital conversion as shown in Table 2-9 below. See Section 3.6.1 for a description of the various digital data formats.

Table 2-9. Digital Data Format Option Jumpers

Digital Data Format	Jumpers Inserted	Jumpers Removed
Offset binary or straight binary	J3A J4A	J3B J4B
Two's complement	J3B J4B	J3A J4A

2.4.12 Grounding for Channel Zero

Jumpers J15 and J16 ground Channel Zero for calibration purposes. When Channel Zero is grounded, your program can read it to determine the offset drift from a true zero digital output. Calibration is described in Chapter 3, Section 3.9. Table 2-10 shows how these jumpers are used.

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Table 2-10. Grounding Jumper Options

Input Mode	Jumpers Inserted	Jumpers Removed
Single-ended	J16	J15
Differential		

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2.5 CONNECTORS

The AIN has two 50-pin connectors on its front panel labeled JK1 and JK2 (see Figure 2-5).

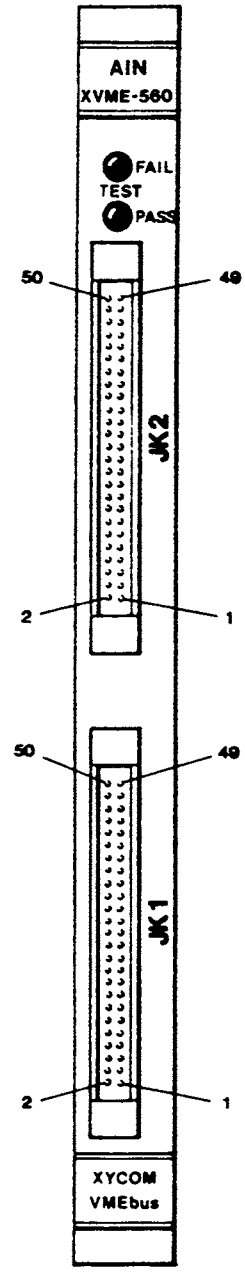


Figure 2-5. JK1 and JK2 Connector Diagram

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2.5.1 Signal Interface Data

The inputs have been designed so that they will not be damaged if connected to long signal leads which are left open circuited. The inputs are also protected against damage if power is removed while signals are still present.

2.5.2 Signal Location on Pin Connectors

The signals for each of the channels and corresponding analog grounds are available on JK 1 and JK2. Tables 2-11 and 2-12 show the signals and their corresponding pins for single-ended and different ial operation.

Table 2-l 1. Signal Location On JK1 and JK2 for Single-Ended Input

JKl				JK2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Channel 0	26	Channel 24	1	Channel 32	26	Channel 56
2	Channel 8	27	Analog gnd	2	Channel 40	27	Analog gnd
3	Analog gnd	28	Channel 25	3	Analog gnd	28	Channel 57
4	Channel 9	29	Channel 17	4	Channel 41	29	Channel 49
5	Channel 1	30	Analog gnd	5	Channel 33	30	Analog gnd
6	Analog gnd	31	Channel 18	6	Analog gnd	31	Channel 50
7	Channel 2	32	Channel 26	7	Channel 34	32	Channel 58
8	Channel 10	33	Analog gnd	8	Channel 42	33	Analog gnd
9	Analog gnd	34	Channel 27	9	Analog gnd	34	Channel 59
10	Channel 11	35	Channel 19	10	Channel 43	35	Channel 51
11	Channel 3	36	Analog gnd	II	Channel 35	36	Analog gnd
12	Analog gnd	37	Channel 20	12	Analog gnd	37	Channel 52
13	Channel 4	38	Channel 28	13	Channel 36	38	.Channel 60
14	Channel 12	39	Analog gnd	14	Channel 44	39	Analog gnd
15	Analog gnd	40	Channel 29	15	Analog gnd	40	Channel 6 1
16	Channel 13	41	Channel 21	16	Channel 45	41	Channel 53
17	Channel 5	42	Analog gnd	17	Channel 37	42	Analog gnd
18	Analog gnd	43	Channel 22	18	Analog gnd	43	Channel 54
19	Channel 6	44	Channel 30	19	Channel 38	44	Channel 62
20	Channel 14	45	Analog gnd	20	Channel 46	45	Analog gnd
21	Analog gnd	46	Channel 3 1	21	Analog gnd	46	Channel 63
22	Channel 15	47	Channel 23	22	Channel 47	47	Channel 55
23	Channel 7	48	Analog gnd	23	Channel 39	48	Analog gnd
24	Analog gnd	49	No connection	24	Analog gnd	49	Digital gnd
25	Channel 16	50	No connection	25	Channel 48	50	Ext Trigger

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Table 2-12. Signal Location On JKl and JK2 for Differential Input

JKl				JK2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Chan. 0 Lo	26	Chan. 8 Hi	1	Chan. 16 Lo	26	Chan. 24 Hi
2	Chan. 0 Hi	27	Analog gnd	2	Chan. 16 Hi	27	Analog gnd
3	Analog gnd	28	Chan. 9 Hi	3	Analog gnd	28	Chan. 25 Hi
4	Chan. 1 Hi	29	Chan. 9 Lo	4	Chan. 17 Hi	29	Chan. 25 Lo
5	Chan. 1 Lo	30	Analog gnd	5	Chan. 17 Lo	30	Analog gnd
6	Analog gnd	31	Chan. 10 Lo	6	Analog gnd	31	Chan. 26 Lo
7	Chan. 2 Lo	32	Chan. 10 Hi	7	Chan. 18 Lo	32	Chan. 26 Hi
8	Chan. 2 Hi	33	Analog gnd	8	Chan. 18 Hi	33	Analog gnd
9	Analog gnd	34	Chan. 11 Hi	9	Analog gnd	34	Chan. 27 Hi
10	Chan. 3 Hi	35	Chan. 11 Lo	10	Chan. 19 Hi	35	Chan. 27 Lo
11	Chan. 3 Lo	36	Analog gnd	11	Chan. 19 Lo	36	Analog gnd
12	Analog gnd	37	Chan. 12 Lo	12	Analog gnd	37	Chan. 28 Lo
13	Chan. 4 Lo	38	Chan. 12 Hi	13	Chan. 20 Lo	38	Chan. 28 Hi
14	Ghan. 4 Hi	39	Analog gnd	14	Chan. 20 Hi	39	Analog gnd
15	Analog gnd	40	Chan. 13 Hi	15	Analog gnd	40	Chan. 29 Hi
16	Chan. 5 Hi	41	Chan. 13 Lo	16	Chan. 21 Hi	41	Chan. 29 Lo
17	Chan. 5 Lo	42	Analog gnd	17	Chan. 21 Lo	42	Analog gnd
18	Analog gnd	43	Chan 14 Lo	18	Analog gnd	43	Chan. 30 Lo
19	Chan. 6 Lo	44	Chan. 14 Hi	19	Chan. 22 Lo	44	Chan. 30 Hi
20	Chan. 6 Hi	45.	Analog gnd	20	Chan. 22 Hi	45	Analog gnd
21	Analog gnd	46	Chan.15 Hi	21	Analog gnd	46	Chan. 31 Hi
22	Chan. 7 Hi	47	Chan.15 Lo	22	Chan. 23 Hi	47	Chan. 31 Lo
23	Chan. 7 Lo	48	Analog gnd	23	Chan. 23 Lo	48	Analog gnd
24	Analog gnd	49	No connection	24	Analog gnd	49	Digital gnd
25	Chan. 8 Lo	50	No connection	25	Chan. 24 Lo	50	Ext Trigger

2.6 MODULE INSTALLATION

The XYCOM VMEbus modules can accommodate typical VMEbus backplane construction. Figure 2-6 shows a standard VME chassis and a typical backplane configuration. There are two rows of backplane connectors depicted (i.e., the Pl backplane and the P2 backplane). The AIN requires only the Pl connector.

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2.6.1 Installation Procedure

CAUTION

Do not attempt to install or remove any boards before turning off the power to the bus and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations and all connections to external devices or power supplies. (Please check the jumper configuration with the diagram and lists in the manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot you are going to use is clear and accessible.

2) Center the board on the plastic guides so that the solder side is facing to the left and the component side is facing to the right (refer to Figure 2-6).

3) Push the card slowly toward the rear of the chassis until the connectors engage (the board should slide freely in the plastic guides).

4) Apply straight-forward pressure to the two handles on the outer edge of the board until the connectors are fully engaged and properly seated.

NOTE

It should not be necessary to use excess pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, it should be secured by tightening the two machine screws at the extreme top and bottom of the board.

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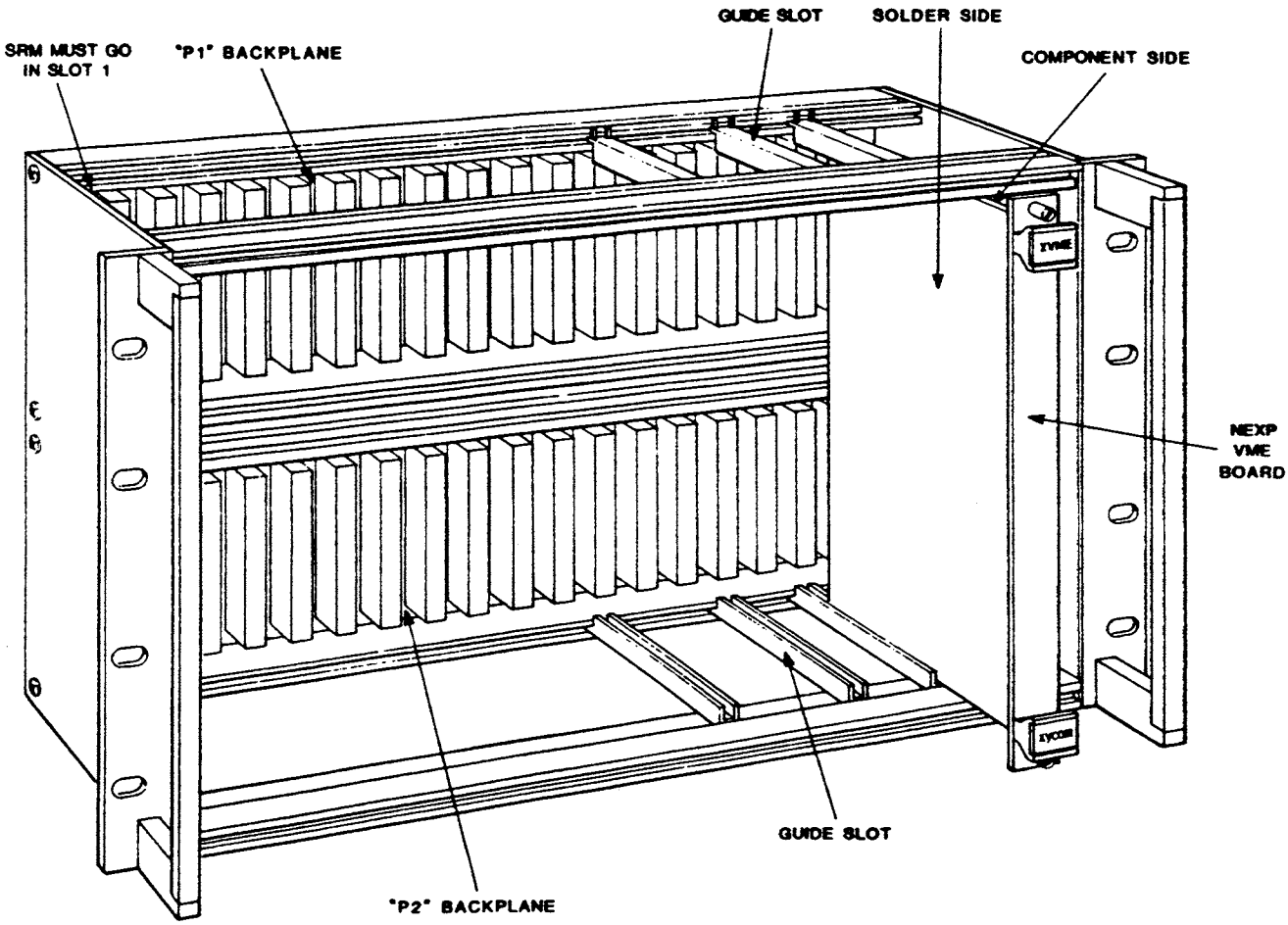


Figure 2-6. VMEbus Chassis

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Chapter 3

PROGRAMMING

3.1 INTRODUCTION

This chapter provides the information required to program the AIN, access conversion data and perform calibration. This information is presented in the following fashion:

- Discussion of base addressing and I/O module address space
- Presentation of module address map showing programming locations
- Programming operating modes
- Selection of channel and gain
- Reading data
- Interrupts
- Calibration

3.2 BASE ADDRESSING

The AIN operates as an I/O module in VMEbus systems and is therefore located in the 64K VMEbus Short I/O Address Space. It can be located at any one of 64 Base Addresses at 1K intervals within this address space. The base address is selected via the switches described in Section 2.4.1.

When located at its base address, the AIN is alloted a 1K block of short I/O address space for its own use. This 1K block of short I/O address space is termed the I/O Interface Block, and contains all of the module's programming locations. Figure 3-1 shows the AIN's I/O Interface Block and its relation to the Short I/O Address space.

When a host processor is addressing locations in the I/O Interface Block, the location's address is added to the module's base address.

For example, if the AIN is located at Short I/O Base Address XXO4OOH, the address of the Control/Status register is XX0481H

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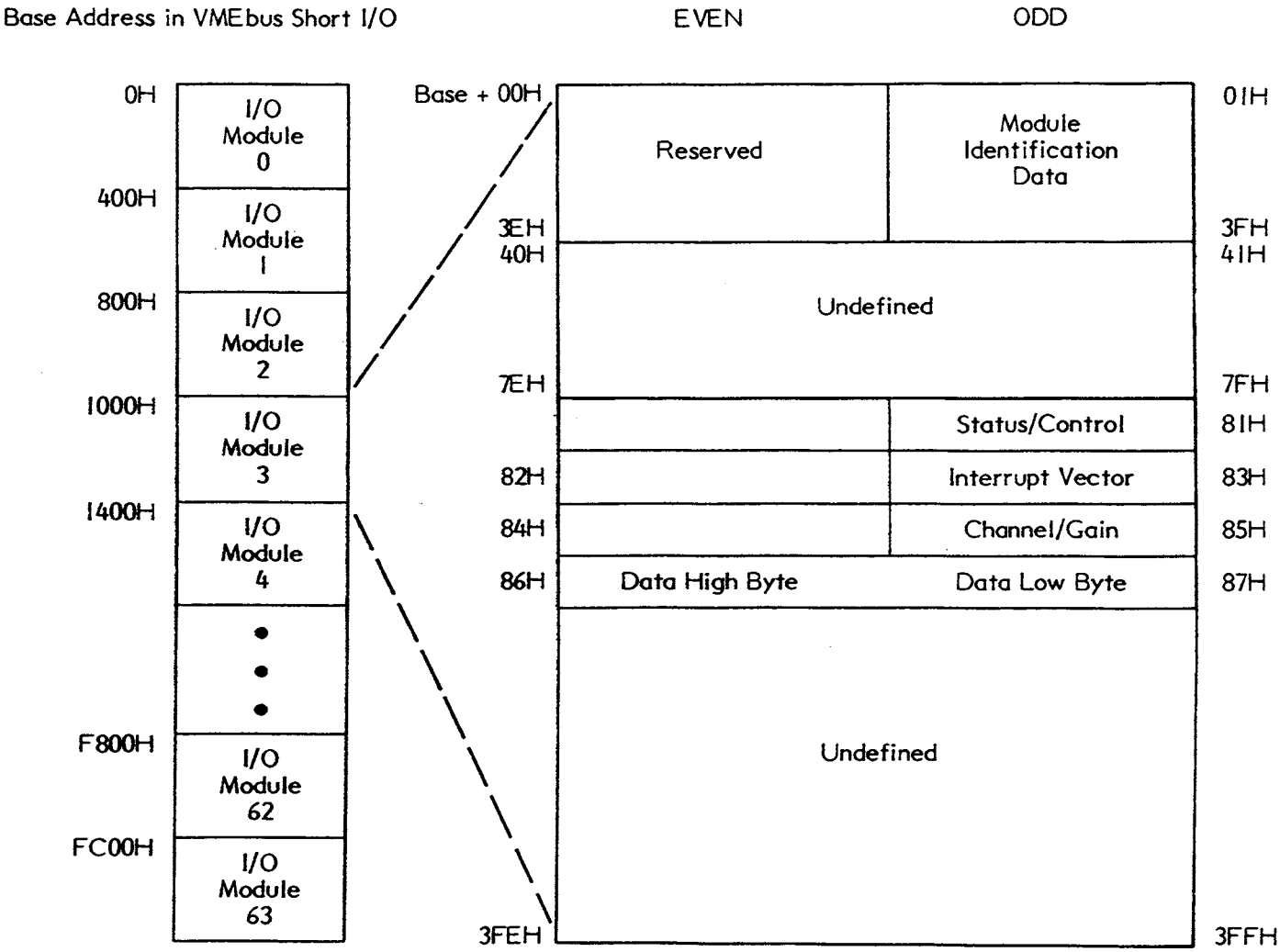


Figure 3-1. XVME-560 I/O Interface Block and its Possible Locations in Short I/O Address Space

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3.3 I/O INTERFACE BLOCK

The AIN I/O Interface Block contains the following programming locations (as shown in Figure 3-1) which are defined in greater detail in their section of this chapter.

- I.D. information (base+01H): The location providing information specifying model number, manufacturer and revision level.
- Control/Status register (base+81H): The location that stores information which programs module operating modes and allows the user to check module operational status.
- Interrupt Vector (base+83H): The location that stores the data that will be read by the interrupt handler when the interrupt is acknowledged.
- Channel/Gain register (base+85H): Contains information selecting the channel and gain for all A/D conversions.
- Data High Byte (base+86H) and Low Byte (base+87H): The locations containing the digital data resulting from an A/D conversion.

3.4 THE CONTROL/STATUS REGISTER

The AIN is programmed mainly through the 8-bit Control/Status register. Figure 3-2 shows the definition of the Control (write) and Status (read) bytes.

CONTROL REGISTER (Address, Write Base+81H)

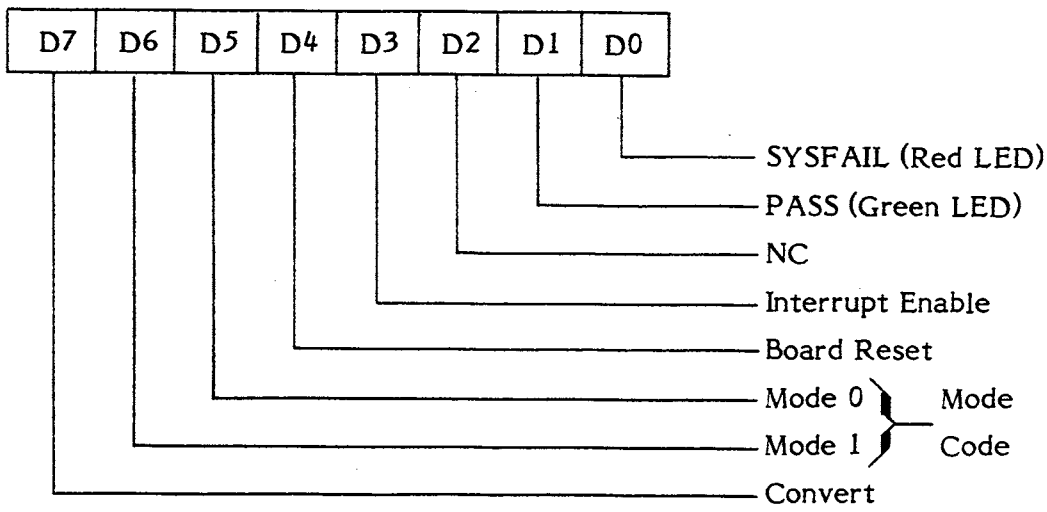


Figure 3-2. Control Register

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3.4.1 Control Register Bit Definitions (Write base+8lH)

D7 A logic 1 written to D7 will force a conversion.

D6,D5: These two bits provide the "mode code** specifying the desired operating mode as shown in Table 3-1 below.

Table 3-l. Mode Bits

Mode Bits		A/D Conversion Mode
Mode 1	Mode 0	
0	0	Single Channel
0	1	Sequential Channel
1	0	Random Channel
1	1	External Trigger

These conversion modes are described in detail in Section 3.5.

D4: This bit is a software module reset. If this is set to a logic "1" and then to a logic "0", the module will be reset except for the Control/Status register. The A/D converter is not reset, so a minimum of 25 usec. must pass before a conversion can be started.

D3: This bit enables interrupts when set to a logic "1".

D2. Not used.

Dl,D0: These bits control the red (SYSFAIL) and green (PASS) LEDs. The red and green LEDs provide visual indication of a module status.

- A logic "0" turns on the Red LED (D0)
- A logic "1" turns on the Green LED (Dl)

The LEDs will indicate the following status (Table 3-2) as set forth by the XYCOM architecture (described in Appendix A).

Table 3-2. LED Status

Red	Green	Module
OFF	OFF	Not operational
OFF	ON	Passed diagnostics
ON	OFF	Power-up/failed diagnostics
ON	ON	Undergoing diagnostics

NOTE

The AIN is a non-intelligent module so all diagnostics must be performed by the system host.

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STATUS REGISTER (Address, Read Base+81H)

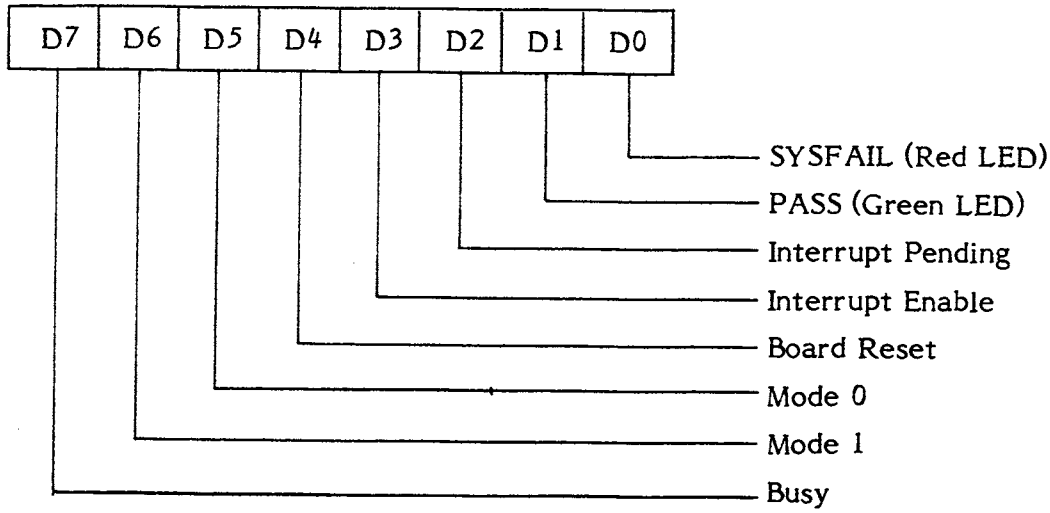


Figure 3-3. Status Register

3.4.2 Status Register Bit Definitions (Read base+81H)

D7: Busy bit: A logic "1" in this bit indicates that the AIN is in the process of making an A/D conversion. The level of this bit must be known or checked prior to starting another A/D conversion, or the A/D conversion in progress could be corrupted.

D6,D5: Mode bits: Same as for control register.

D4: Reset bit.

D3: Interrupt Enable bit: Indicates if interrupts are enabled.

D2: Interrupt Pending bit: A logic "1" in this bit indicates that an A/D conversion has been completed. This bit is cleared by the start of another A/D conversion, a reset, or a read from the lower data byte.

D1,D0: Status bits: Same as for control register.

3.5 CHANNEL/GAIN REGISTER

The Channel/Gain register is an 8-bit register located at base+85H containing the information that selects the channel and gain used for the A/D conversion. Figure 3-4 below shows the format of this 8-bit register.

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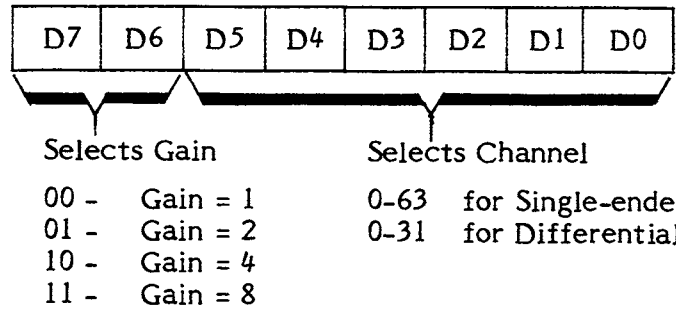


Figure 3-4. Channel/Gain Register (Address Base+85H)

The upper two bits of this register (D6,D7) select one of four possible gains for the input signal as shown in Figure 3-4.

The selection of the gain factor affects the various input ranges as shown in Table 3-3 below.

Table 3-3. A/D Programmable Gain

x 1		x 2	
F.S.	LSB	F.S.	LSB
±10v	4.88mv	±5v	2.44mv
±5v	2.44mv	±2.5v	1.22mv
±2.5v	1.22mv	±1.25v	.61mv
0 to +10v	2.44mv	0 to +5v	1.22mv
0 to +5v	1.22mv	0 to +2.5v	.61mv

x 4		x 8	
F.S.	LSB	F.S.	LSB
±2.5v	1.22mv	±1.25v	.61mv
±1.25mv	.61mv	±.625v	.305mv
±.625v	.305mv	±3125v	.1525mv
0 to 2.5v	.61mv	0 to +1.25v	.305mv
0 to +1.25v	.305mv	0 to +.625v	.1525mv

The lower six bits (D5-D0) select the input channel that the A/D is going to make a conversion on (see Figure 3-4 and Table 3-4).

This register is cleared on power-up and may be loaded at any time as long as the "Busy" bit (bit 7) of the status register is a logic "0" (see Section 3.4.2).

Table 3-4 lists the channel selection codes for single-ended (0-63) and differential (0-31) operation.

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Table 3-4. Channel Selection Codes

Data Bits						Channel Selected
D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	CH0
0	0	0	0	0	1	CH1
0	0	0	0	1	0	CH2
0	0	0	0	1	1	CH3
0	0	0	1	0	0	CH4
0	0	0	1	0	1	CH5
0	0	0	1	1	0	CH6
0	0	0	1	1	1	CH7
0	0	1	0	0	0	CH8
0	0	1	0	0	1	CH9
0	0	1	0	1	0	CH10
0	0	1	0	1	1	CH11
0	0	1	1	0	0	CH12
0	0	1	1	0	1	CH13
0	0	1	1	1	0	CH14
0	0	1	1	1	1	CH15
0	1	0	0	0	0	CH16
0	1	0	0	0	1	CH17
0	1	0	0	1	0	CH18
0	1	0	0	1	1	CH19
0	1	0	1	0	0	CH20
0	1	0	1	0	1	CH21
0	1	0	1	1	0	CH22
0	1	0	1	1	1	CH23
0	1	1	0	0	0	CH24
0	1	1	0	0	1	CH25
0	1	1	0	1	0	CH26
0	1	1	0	1	1	CH27
0	1	1	1	0	0	CH28
0	1	1	1	0	1	CH29
0	1	1	1	1	0	CH30
0	1	1	1	1	1	CH31
1	0	0	0	0	0	CH32
1	0	0	0	0	1	CH33
1	0	0	0	1	0	CH34
1	0	0	0	1	1	CH35
1	0	0	1	0	0	CH36
1	0	0	1	0	1	CH37
1	0	0	1	1	0	CH38
1	0	0	1	1	1	CH39
1	0	1	0	0	0	CH40
1	0	1	0	0	1	CH41
1	0	1	0	1	0	CH42
1	0	1	0	1	1	CH43
1	0	1	1	0	0	CH44
1	0	1	1	0	1	CH45
1	0	1	1	1	0	CH46
1	0	1	1	1	1	CH47
1	1	0	0	0	0	CH48
1	1	0	0	0	1	CH49
1	1	0	0	1	0	CH50
1	1	0	0	1	1	CH51
1	1	0	1	0	0	CH52
1	1	0	1	0	1	CH53
1	1	0	1	1	0	CH54
1	1	0	1	1	1	CH55
1	1	1	0	0	0	CH56
1	1	1	0	0	1	CH57
1	1	1	0	1	0	CH58
1	1	1	0	1	1	CH59
1	1	1	1	0	0	CH60
1	1	1	1	0	1	CH61
1	1	1	1	1	0	CH62
1	1	1	1	1	1	CH63

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3.6 DATA ACCESS LOCATIONS

The A/D converter produces a digital output which corresponds with the applied analog input at the selected channel. The digital output is stored at locations base+86H (high byte) and base+87H (low byte).

The digital information must be read in the order high byte first, low byte second or both bytes can be read at once with a 16-bit "word" read. This is because in the Sequential or Single Channel conversion modes reading the lower eight bits of data will initiate a new A/D conversion, and thus may write over the present high byte.

3.6.1 Digital Data Format

The AIN digitizes the value of the analog signal on the input of the selected channel. The analog equivalent of this digital number depends upon which digital data format and input range have been previously jumper selected (see Section 2.4.9).

The digital data format is first determined by the choice of the input scaling range: Unipolar (e.g., 0 to 5V) or Bipolar (e.g., -5 to +5V) (see Section 2.14).

If the input scaling range is unipolar, then a "straight" binary data format must be selected. If the input scaling range is Bipolar, then the data format can be selected as two's complement or offset binary.

3.6.1.1 Unipolar Digital Data Format

An example of the unipolar digital data format (straight binary) with the input scaling range set for 0 to 5 volts is shown in Table 3-5 below.

Table 3-5. Example of 0 to 5 Volt Input Range Encoded in Straight Binary

	High Byte	Low Byte	
	D15	DO	4095
Full scale	0000 1111	1111 1111	5V*4096(-1LSB)
Zero	0000 0000	0 0 0 0 0 0 0 0	OV (+1/2 LSB)

NOTE

The value of one "LSB" is the input voltage change that causes an increase or decrease of the digital (binary) input value by one bit.

3.6.1.2 Bipolar Digital Data Format

Examples of the bipolar digital data formats (offset binary and two's complement) with the input scaling range set for -5 to +5 volts are shown in Table 3-6 below.

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Table 3-6. Examples of -5 to +5 Volt Input Range Encoded in Offset Binary (a) and Two's Complement (b)

Offset Binary

	High Byte D15	Low Byte D0	4095
+Full scale	0000 1111	1111 1111	+5V*4096(-1LSB)
Zero	0000 1000	0000 0000	0v
-Full scale	0000 0000	0000 0000	-5V (+1/2 LSB)

(a)

Two's Complement

	High Byte D15	Low Byte D0	
+Full scale	0000 0111	1111 1111	+5V (-1 LSB)
Zero	0000 0000	0000 0000	0v
-Full scale	1111 1000	0000 0000	-5V(+i/2 LSB)

(b)

3.7 A/D CONVERSION MODES

The AIN may operate in four possible A/D conversion modes. They are:

- Random Channel -- a single A/D conversion is performed on any channel.
- Single Channel -- repeated A/D conversions are performed on a specified channel.
- Sequential Channel -- channels are sampled in sequence, beginning with any specified channel.
- External Trigger -- the last channel selected is sampled only when a positive TRIG signal is received on pin 50 of JK2

The following sections describe these operating modes. The modes are selected by specifying the proper "mode code" using bits Ml and MO of the control register (see Section 3.4.1).

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3.7.1 Random Channel Mode

In the Random Channel mode, a conversion will automatically start after a channel number is written to the Channel/Gain register.

Procedure

1) Write the control word to the control register (base+8lH) specifying bits M1 and MO as 1 and 0.

2) Select the channel and gain by writing to the Channel/Gain register (base+85H). This starts the A/D conversion.

3) Read the results of the conversion in the high byte (base+86H) and low byte (base+87H). These two bytes can be read in any order when in the Random Channel mode. A 16-bit read can also be performed.

3.7.2 Single Channel Mode

In the Single Channel mode, the module will automatically start another conversion on the selected channel after the low byte (base+87H) has been read.

Procedure

1) Write the control word (base+8lH) that specifies bits Ml and MO as 0 and 0 for single channel mode.

2) Select the channei and gain by writing to the Channel/Gain register(base+85H).

3) To initiate the first conversion, perform a "dummy" Read (base+87H) or force a conversion by writing a logic "one" to bit 7 of the control register.

4) Read the results of the conversion high byte (base+86H) then low byte (base+87H) or perform a 16-bit read. When the low byte is read, another A/D conversion starts on that channel.,

3.7.3 Sequential Channel Mode

In the Sequential Channel mode, every time the lower eight bits of data are read (base+87H) the channel number is incremented by one, and an A/D conversion is started on the next channel (previous channel+l).

Procedure

1) Write the control word (base+8lH) specifying mode bits Ml and MO as 0 and 1.

2) Specify the channel and gain by writing to the Channel/Gain register (base+85H).

3) To initiate the first conversion, perform a dummy Read (base+87H) or force a conversion by writing a logic "one" to bit 7 of the control register.

4) Read the results, high byte (base+86H) then low byte (base+87H), or perform a 16-bit read. When the lower byte is read, an A/D conversion is initiated on the next channel (previous channel+ 1).

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3.7.4 **External Trigger** Mode

The External Trigger mode will allow a low going pulse on pin 50 of connector JK2 to start a conversion. Figure 3-5 below shows the timing constraints.

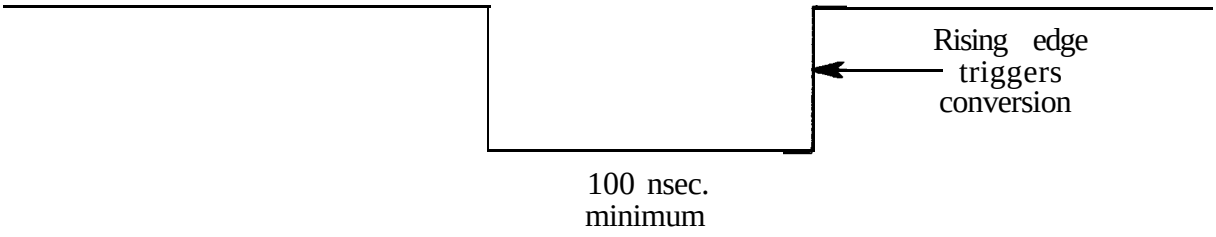


Figure 3-5. External Trigger Pulse

An alternate method would be to have the trigger line be normally low, then pulsed high and back Iow again as shown in Figure 3-6. This is not the preferred method since a conversion is started when the external trigger line is disabled after previously being enabied.

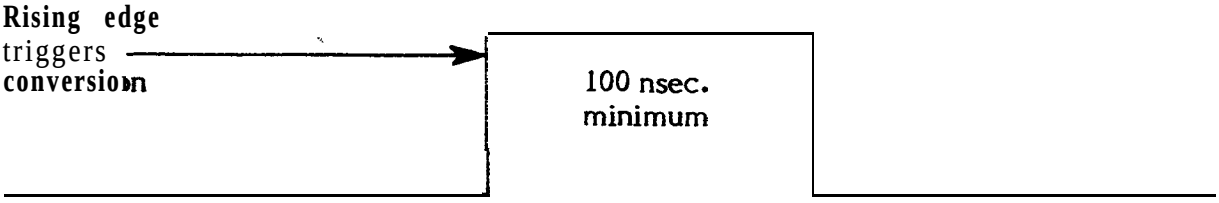


Figure 3-6. Alternate External Trigger Pulse

Procedure

1) Connect the External Trigger signal to pin 50 of JK2.

2) Write the control word (base+81H) specifying mode bits M1 and MO as 1 and 1.

3) Specify the channel and gain by writing to the Channel/Gain register.

3.8 INTERRUPTS

The AIN can generate an interrupt to notify the host that the A/D conversion is complete and that the data is valid. The level and vector generated by this interrupt are both user-selectable.

The following four steps must be performed to generate an interrupt:

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1. Interrupt level select switches must be set for the desired level (I1-I7) the interrupt is to be generated on. J1 must be in the J1A position.

2. Interrupts must be enabled via bit 3 (set to a logic "1") in the Control/Status register (see Section 3.4).

3. The Interrupt Vector register (location base+83H) must be loaded with the desired vector. This vector will be read by the interrupt handler when the interrupt is acknowledged.

4. At the completion of a conversion, the interrupt will be generated.

3.9 CALIBRATION

Calibration can be performed in either the single-ended or differential input configurations.

1. Calibration begins by offset nulling the instrumentation amplifier with channel 0 selected and its inputs grounded. The inputs to channel 0 are grounded with J16 when in the single-ended input mode, or by J15 and J16 when in the differential input mode.

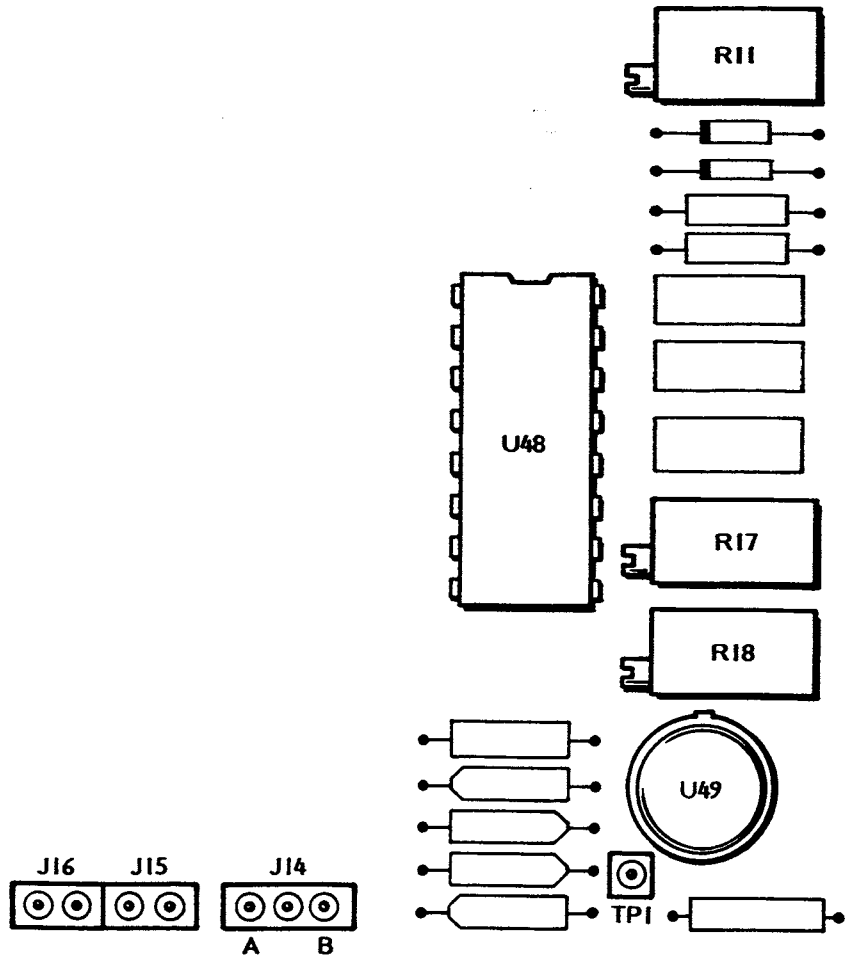


Figure 3-7. Calibration Components

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2. Test point 1 is to be offset nulled to within +30 uV with a digital voltmeter with at least 10 uV resolution. Test point 1 is the output of the instrumentation amplifier which will go to the positive side of the voltmeter. Analog ground may be obtained from J15 and J16 and connected to the negative side of the voltmeter. Potentiometer R18 is to be adjusted until the output is nulled.

3. With the instrumentation amplifier nulled, it is necessary to perform continuous conversions on channel 0 with a gain factor of eight. The conversion result should be displayed on a CRT screen in hex format for verification purposes. By applying 0 volts +1/2 LSB to channel 0, the offset potentiometer Rll can be adjusted until the conversion result is toggling equally between the two points described in Table 3-7 below.

Table 3-7. Calibration Points

	0 v + 1/2 LSB Transition Points		FS. - 1 1/2 LSB Transition Points	
Unipolar (Straight Binary)	0000H	0001H	OFFEH	OFFFH
Bipolar (Offset Binary)	0800H	0801H	OFFEH	OFFFH
Bipolar (2's Complement Offset Binary)	0000H	0001H	07FEH	07FFH

4. The gain is adjusted by removing J15 and J16 and then applying the full scale voltage of that particular range minus 1 1/2 LSB and adjusting R17 until toggling occurs between the points described in Table 3-7.

Field Calibration

In the field, the AIN may be calibrated without the use of a micro-voltmeter. This method will not provide as accurate a calibration, but will be within ±1 LSB. There are three steps involved in field calibration:

1) Null the A/D offset error.
2) Null the instrumentation amplifier offset.
3) Calibrate the gain.

The first step is to null the A/D offset error. To do this, jumper J12 must be placed in the "A" position. This grounds the gain. On a gain of eight, a reading of 0000H (0800H for offset binary) should be observed as a conversion result on channel 0. Potentiometer Rll can be adjusted until the zero reading is observed. Jumper 312 must then be placed back in the "B" position to allow the second step of field calibration.

The second step is to null the instrumentation amplifier offset. This requires the input to channel 0 to be grounded. To do this, either jumper J16 must be installed for

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single-ended input, or jumpers J16 and J15 must be installed for differential input. Potentiometer R18 is adjusted to again provide the zero reading.

Be sure that if calibrating in the unipolar mode, the zero reading is not a result of an under-range condition (below the range of the A/D). This can be easily avoided by adjusting R18 for a count of OOOlH, and then backing off R18 until the reading just goes to 0000H. Jumpers J18 and J19 can now be removed.

The third step is to calibrate the gain. To do this, a voltage standard is required. The accuracy of the voltage standard will directly affect the accuracy of this procedure. Therefore, it is up to the user to determine the accuracy to which the board is to be calibrated and used, and to choose an appropriately accurate voltage standard. With the voltage standard, a full scale value minus 1 1/2 LSB must be applied to channel 0. The programmable gain should be set to unity gain for this procedure. The gain potentiometer, R17, is adjusted until readings toggle equally between the transition points as described in Table 3-7.

3.10 **XVME-560 IDENTIFICATION**

For easy identification in a VMEbus system configuration, I.D. information is located at addresses (base address + 1) to (base address + 3FH) in the odd bytes only (see Figure 3- 1).

The AIN uses the XYCOM module identification scheme which provides a unique method of storing module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K byte blocks occupied by the module, and model functional revision level information. This information can be read by the system processor on power-up to verify the system configuration and operational status. Figure 3-8 defines the Identification information locations.

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Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier,
5	E	45	always "VMEID"
7	I	49	(5 characters)
9	D	44	
B	X	58	Manufacturers I.D.,
D	Y	59	always "XYC" for XYCOM
F	C	43	Modules (3 characters)
11	5	34	
13	6	32	Module Model Number
15	0	30	(3 characters and
17		20	4 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision
23	1	31	level with leading blank (if single digit)
25	0	31	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer
37	"		Dependent Information,
39	"		Reserved for Future Use
3B	"		
3D	"		
3F	"		

Figure 3-8. Identification Data

Because each module I.D. data location is accessed by odd backplane addresses only, the 32 bytes of ASCII data are assigned to the first 32 odd I/O interface block bytes (odd bytes 1H - 3FH) allowing I.D. information to be accessed by addressing the module base, offset by the specific address for the character(s) needed.

For example, if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex coded ASCII value at each location. Thus, in this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH.

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Appendix A

XYCOM STANDARD I/O ARCHITECTURE

INTRODUCTION

The purpose of this Appendix is to define XYCOM's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all XVME I/O modules in order to provide a simpler and more consistent method of programming for the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the XYCOM I/O Architecture are the following:

1. Module Addressing - - Where a module is positioned in the I/O address space and how software can read from it or write to it.

2. Module Identification -- How software can identify which modules are installed in a system.

3. Module Operational Status -- How the operator can (through software) determine the operational condition ofspecific modules within the system.

4. Interrupt Control -- How software is able to control and monitor the capability of the module to interrupt the system.

5. Communication between Modules -- How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the I/O modules.

6. The I/O Kernel -- How intelligent and non-intelligent "kernels" facilitate the operation of all XYCOM I/O modules.

MODULE ADDRESSING

All XYCOM I/O modules are designed to be addressed within the VMEbus-defined 64K short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while at the same time providing 64K of address space for I/O modules.

Base Addressing

Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for XYCOM VME I/O modules has been designed to be jumper-selectable. Each XVME I/O module installed in the system requires at least a 1K byte block of the short I/O memory. This divides the 64K short I/O address space into 64 1K segments. Thus, each I/O module has a base address which starts on a boundary. As a result, the XYCOM I/O modules have all been implemented to decode

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base addresses in 1K (400H) increments. On an intelligent XVME module, address signals A10-A13 are decoded, while A14 and A15 must be zero. (This implies that only the lowest 16 of the possible 64 1K segments are used for intelligent modules.) On non-intelligent XVME modules, the six highest order short I/O address bits are decoded, while the remaining lower order bits are ignored. This arrangement provides the correct address configuration to allow each module address to begin on a 1K boundary. Non--intelligent XVME modules allow the use of six base address jumpers (representing bits A10-A15), and thus, they are able to reside on any of the 64 1K boundaries available in the short I/O address space. Intelligent XVME modules will only allow the use of four base address jumpers (representing bits A10-A15) which limits their selection of 1K boundaries to one of 16 possible choices.

Figure A-l shows an abbreviated view of the short I/O memory.

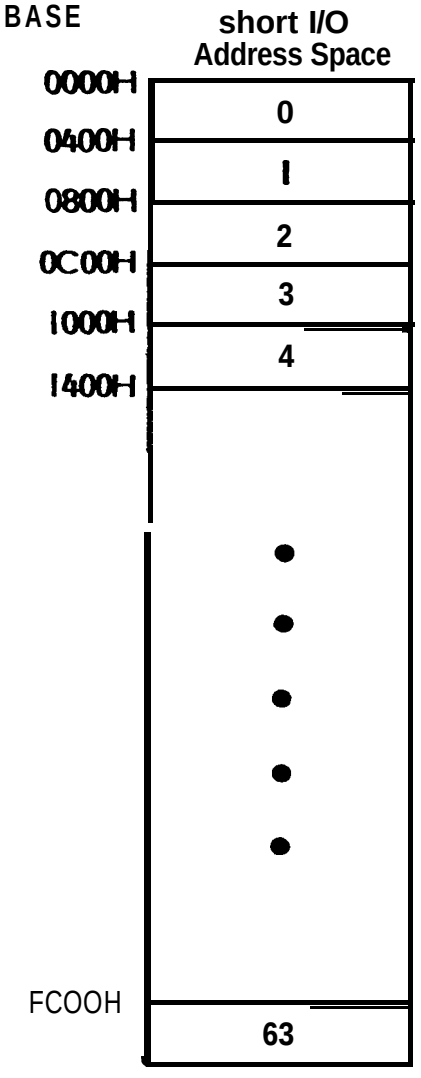


Figure A-1. 64K Short I/O Address Space

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Standardized Module I/O Map

The 1K block of short I/O addresses (called the I/O Interface Block) allocated to each XVME module is mapped with a standardized format in order to simplify programming and data access. The locations of frequently used registers and module-specific identification information are uniform. For exam ple, the module identification information is always found in the first 32 odd bytes of the module memory block -- with these addresses being relative to the jumpered base address (i.e., Module I.D. data address = base address + odd bytes 1H - 3FH). The byte located at base address+81H on each module contains a Status/Control register which provides the results of diagnostics for verification of the module's operational condition. The next area of the module I/O Interface Block (base address + 82H - roughly 120F) is module-specific and it varies in size from one module to the next. It is in this area that the module holds specific I/O status, data, and pointer registers for use with IPC protocol. All intelligent XVME I/O modules have an area of their I/O Interface Blocks defined as “dual access RAM." This area of memory provides the space where XVME Wave” I/O modules access their command blocks and where XVME “master" modules could access their command blocks (i.e., "master" modules can also access global system memory).

The remainder of the I/O Interface Block is then allocated to various module-specific tasks, registers, buffers, ports, etc.

Figure A-2 shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. Notice that any location in the I/O Interface Block may be accessed by simply using the address formula:

Module Base Address + Relative Offset Desired Location

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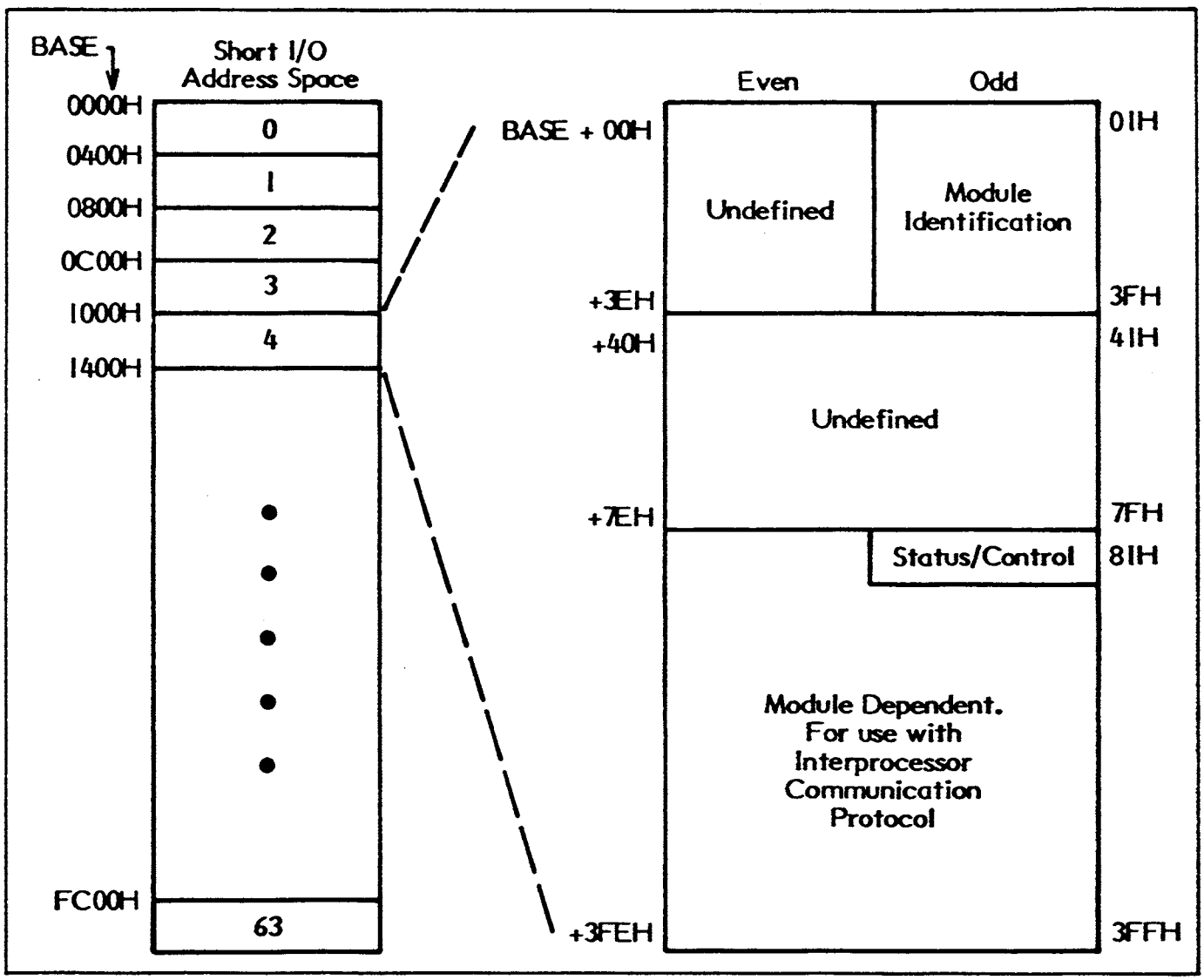


Figure A-2. XVME I/O Module Address Map

MODULE SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K-byte blocks occupied by the module, and model functional revision level information. This information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1 defines the Identification information locations.

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Table A-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier, always "VMEID" (5 characters)
5	E	45	
7	I	49	
9	D	44	
B	X	58	Manufacturers I.D., always "XYC" for XYCOM Modules (3 characters)
D	Y	59	
F	C	43	
11	5	34	
13	6	32	Module Model Number (3 characters and 4 trailing blanks)
15	0	30	
17		20	
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision level with leading blank (if single digit)
23	1	31	
25	0	31	Minor functional revision level with trailing blank (if single digit)
27		20	
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer Dependent Information, Reserved for Future Use
37	"		
39	"		
3B	"		
3D	"		
3F	"		

The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1H-3FH).

I.D. information can be accessed simply by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex-coded ASCII value at each location. Thus, in this example, the ASCII values which make up the

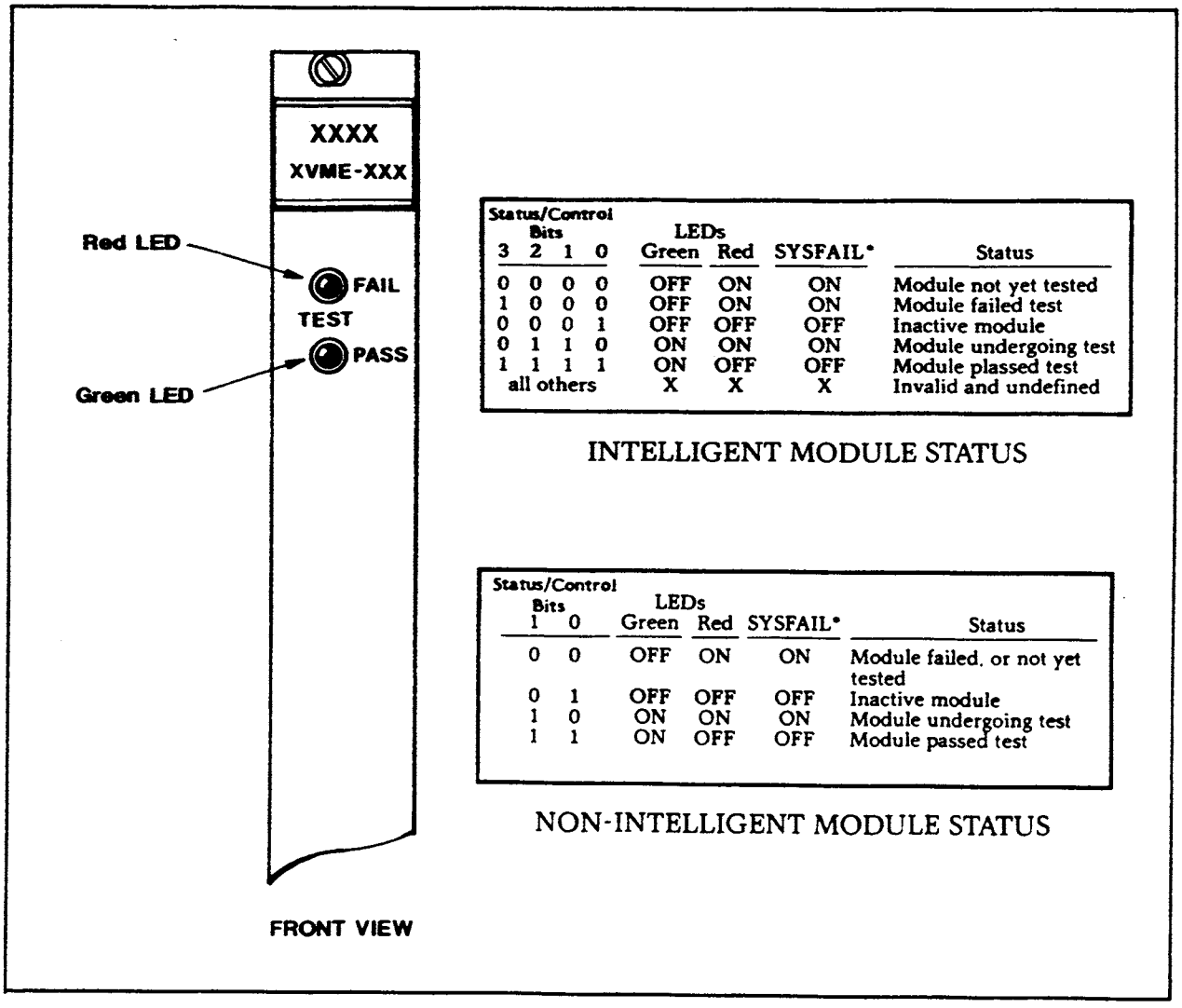
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module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH within the system's short I/O address space.

MODULE OPERATIONAL STATUS/CONTROL

All XVME intelligent I/O modules are designed to perform diagnostic self-tests on power-up or reset. For non-intelligent modules, the user must provide the diagnostic program. The self-test provision allows the user to verify the operational status of a module by either visually inspecting the two LEDs which are mounted on the module front panel (see Figure A-3), or by reading the module status byte (located at module base address + 81H).

Figure A-3 shows the location of the status LEDs on the module front panel. The two tables included with Figure A-3 define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status/Control Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module plassed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status/Control Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

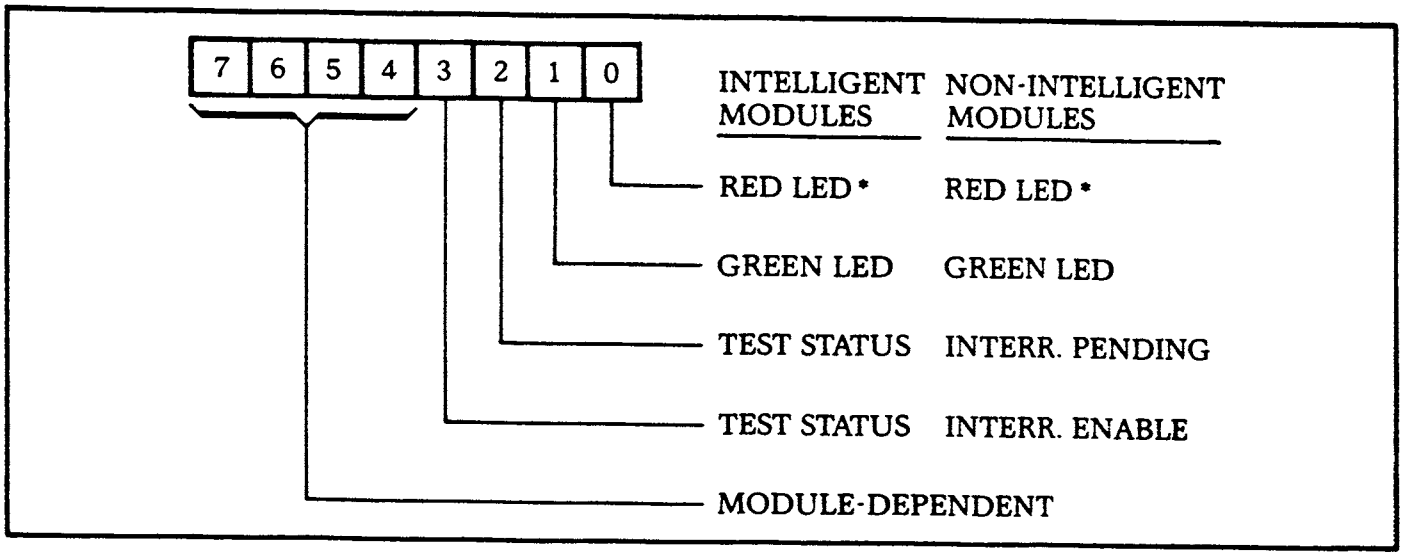
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The module status/control register (found at module base address + 8lH) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent modules is a “Read Only” register and it can be read by software to determine if the board is operating properly.

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module-generated interrupts. The LED status bits are "Read/Write" locations which provide the user with the indicators to accomodate diagnostic software. The Interrupt Enable bit is also a Read/Write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a “Read Only” bit which indicates a module-generated pending interrupt.

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Figure A-4 shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules
0	Read/Write - Red LED 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Bit	Intelligent Modules
0	Read Only - Red LED 0 = Red LED On 1 = Red LED Off
1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2 & 3	Read Only - Test Status Indicators Bit 3 / Bit 2 0 / 0 = Self-test not started 0 / 1 = Self-test in progress 1 / 0 = Self-test failed 1 / 1 = Self-test passed
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Figure A-4. Status Register Bit Definitions

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INTERRUPT CONTROL

Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status of pending on-board interrupts can also be read from this register. Interrupt control for intelligent modules is handled by the Interprocessor Communications Protocol.

Communications Between Processors

Communications between an intelligent "master" and an intelligent "slave" I/O module is governed by XYCOM's Interprocessor Communication (IPC) Protocol. This protocol involves the use of 20-byte Command Block data structures, which can be located anywhere in shared global RAM or dual-access RAM on an I/O module, to exchange commands and data between a host processor and an I/O module. Interprocessor Communication Protocol is thoroughly explained in Chapter 3 of this manual.

THE KERNEL

To standardize its XVME I/O modules, XYCOM has designed them around "kernels" common from module to module. Each different module type consists of a standard kernel, combined with module-dependent application circuitry. Module standardization results in more efficient module design and allows the implementation of the Standard I/O Architecture. The biggest benefit of standardization for intelligent modules is that it allows the use of a common command language or protocol (Interprocessor Communication ProtocoI in this case).

The intelligent kernel is based around a 68000 microprocessor. This design provides the full complement of VMEbus Requester and Interrupter options for master/slave interfacing, as well as all of the advantages provided by the various facets of the XYCOM Standard I/O Architecture (as covered earlier in this appendix).

The non-intelligent kernel provides the circuitry required to receive and generate all of the signals for a VMEbus defined 16-bit "slave" module. The non-intelligent kernel also employs the features of the XYCOM Standard I/O Architecture (as described earlier in this appendix).

The simplified diagrams below show the features of both the intelligent and the non-intelligent kernels.

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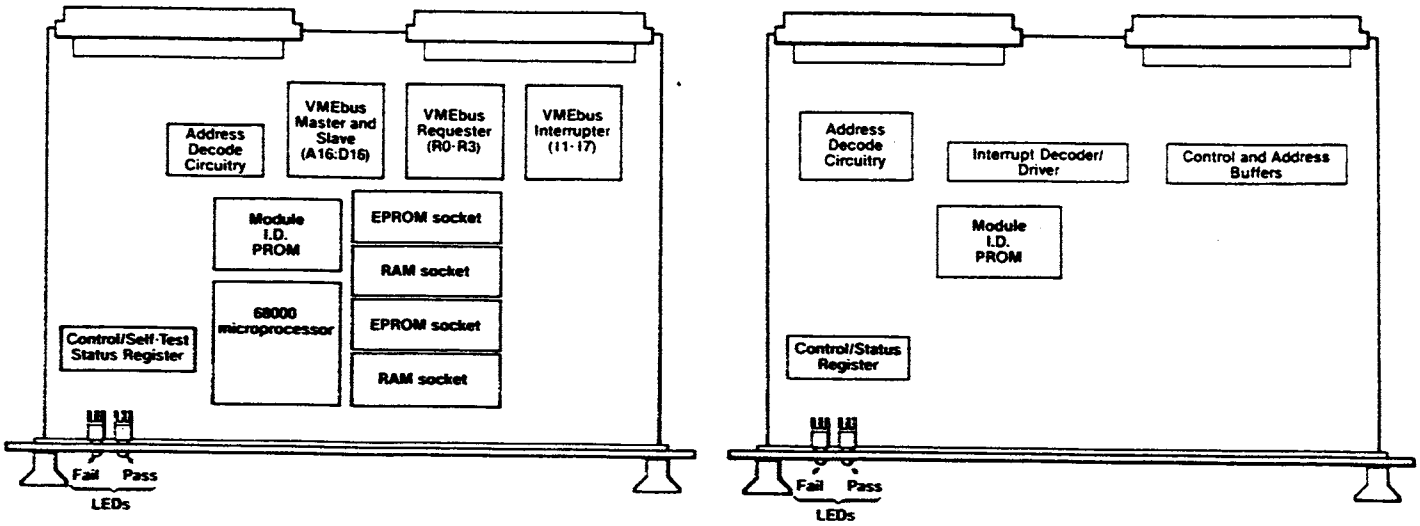


Figure A-5. Intelligent and Non-Intelligent Kernels

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Appendix B

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-560 module is physically configured as a non-expanded (NEXP), double-height, VMEbus compatible board. There is one 96-pin bus connector on the rear edge of the board labeled P1 (refer to Chapter 2, Figure 2-l for the location). The pin connections for P1 contain the standard address, data, and control signals necessary for the operation of NEXP modules. The following tables identify the VMEbus signals by signal mnemonic, connector and pin number, and signal characteristic.

Table B-1. Pl - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B: 3	AC FAILURE - open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
IACKIN*	IA: 21	INTERRUPT ACKNOWLEDGE IN - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A: 22	INTERRUPT ACKNOWLEDGE OUT - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AMO-AM5	1A: 23 1B: 16,17, 18,19 1C: 14	ADDRESS MODIFIER (bits 0-5) - Three-state driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification.
AS*	1A: 18	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A0I-A23	1A: 24-30 1C: 15-30	ADDRESS bus (bits l-23) - Three-state driven address lines that specify a memory address.

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Table B-l. Pl - VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A24-A31	2B: 4-11	ADDRESS bus (bits 24-31) - Three-state driven bus expansion address lines.
BBSY *	1B: 1	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B: 2	BUS CLEAR - Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.
BERR*	lC: 11	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG3IN*	1B: 4,6, 8,l0	BUS GRANT (0-3) IN - Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*-BG30UT*	1B: 5,7, 9,ll	BUS GRANT (0-3) OUT - Totem-pole driven signals generated by Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant Out signal indicates to the next board that it may become the next bus master.
BR0*-BR3*	IB: 12-15	BUS REQUEST (0-3) - Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DSO*	1A: 13	DATA STROBE 0 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DSl*	1A: 12	DATA STROBE 1 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).

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Table B-l. Pl - VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
DTACK*	1A: 16	DATA TRANSFER ACKNOWLEDGE - Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A: l-8 lC: l-8	DATA BUS (bits 0-15) - Three-state driven bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A: 9,ll, 15,17,19 1B: 20,23 1C: 9 2B: 2,12 22,31	GROUND
IACK*	1A: 20	INTERRUPT ACKNOWLEDGE - Open-coliector or three-state driven signal from any Master processing an interrupt request. Routed via the backplane to Siot 1, where it is looped back to become Slot l. IACKIIN* to start the interrupt acknowledge daisy-chain.
IRQ l*-IRQ7*	IB: 24-30	INTERRUPT REQUEST (l-7) - Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C: 13	LONGWORD - Three-state driven signal to indicate that the current transfer is a 32-bit transfer.
(RESERVED)	2B: 3	RESERVED - Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B: 21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B: 22	A reserved signal which will be used as the transmission line for serial communication bus messages.

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Table B-1. P1 - VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSCLK	1A: 10	SYSTEM CLOCK - A constant 16-MHz clock signal that is independent of processor speed or timing. This signal is used for general system timing use.
SYSFAIL*	1C: 10	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VMEbus.
SYSRESET*	1C: 12	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A: 14	WRITE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation; a low level indicates a write operation.
+5V STDBY	1B: 3	+5 Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
+5V	1A: 32 1B: 32 1C: 32 2B: 1,13,32	+5 Vdc Power - Used by system logic circuits.
+12v	1C: 31	+12 Vdc Power - Used by system logic circuits.
-12v	1A: 31	-12 Vdc Power - Used by system logic circuits.

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BACKPLANE CONNECTOR PI

The following table lists the PI pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table B-2. PI Pin Assignments

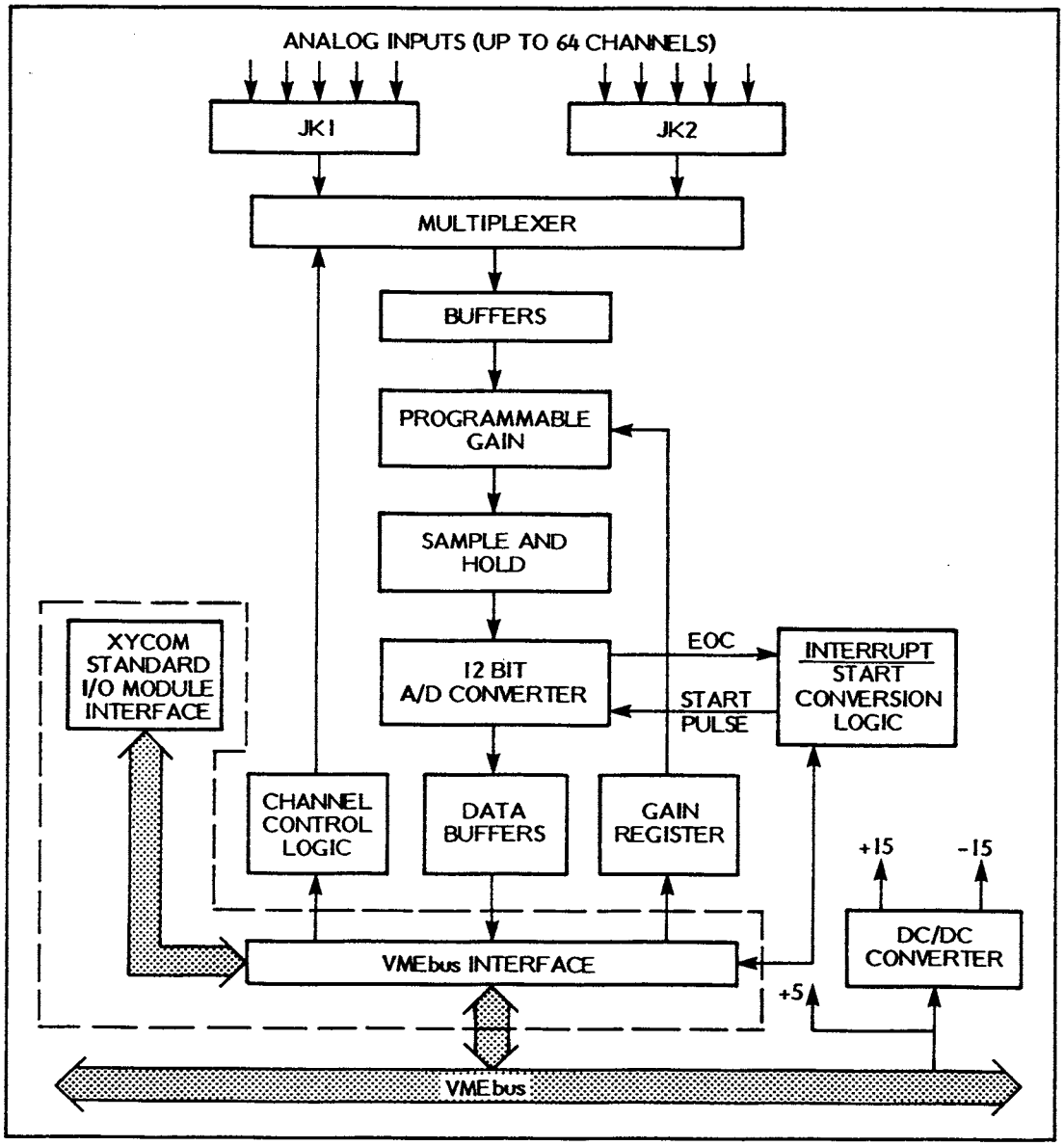
Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	DO8
2	D01	BCLR*	DO9
3	DO2	ACFAIL*	Dl0
4	D03	BG0IN*	Dll
5	DO4	BG0OUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	D07	BG2IN*	D15
9	GND	BG20UT*	GDN
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG30UT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DS0*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	Al9
20	IACK*	GND	Al8
21	IACKIN*	SERCLK (1)	Al7
22	IACKOUT*	SERDAT (1)	Al6
23	AM4	GND	A15
24	A07	IRQ7*	Al4
25	A06	IRQ6*	Al3
26	A05	IRQ5*	Al2
27	A04	IRQ4*	Al1
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

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Appendix C

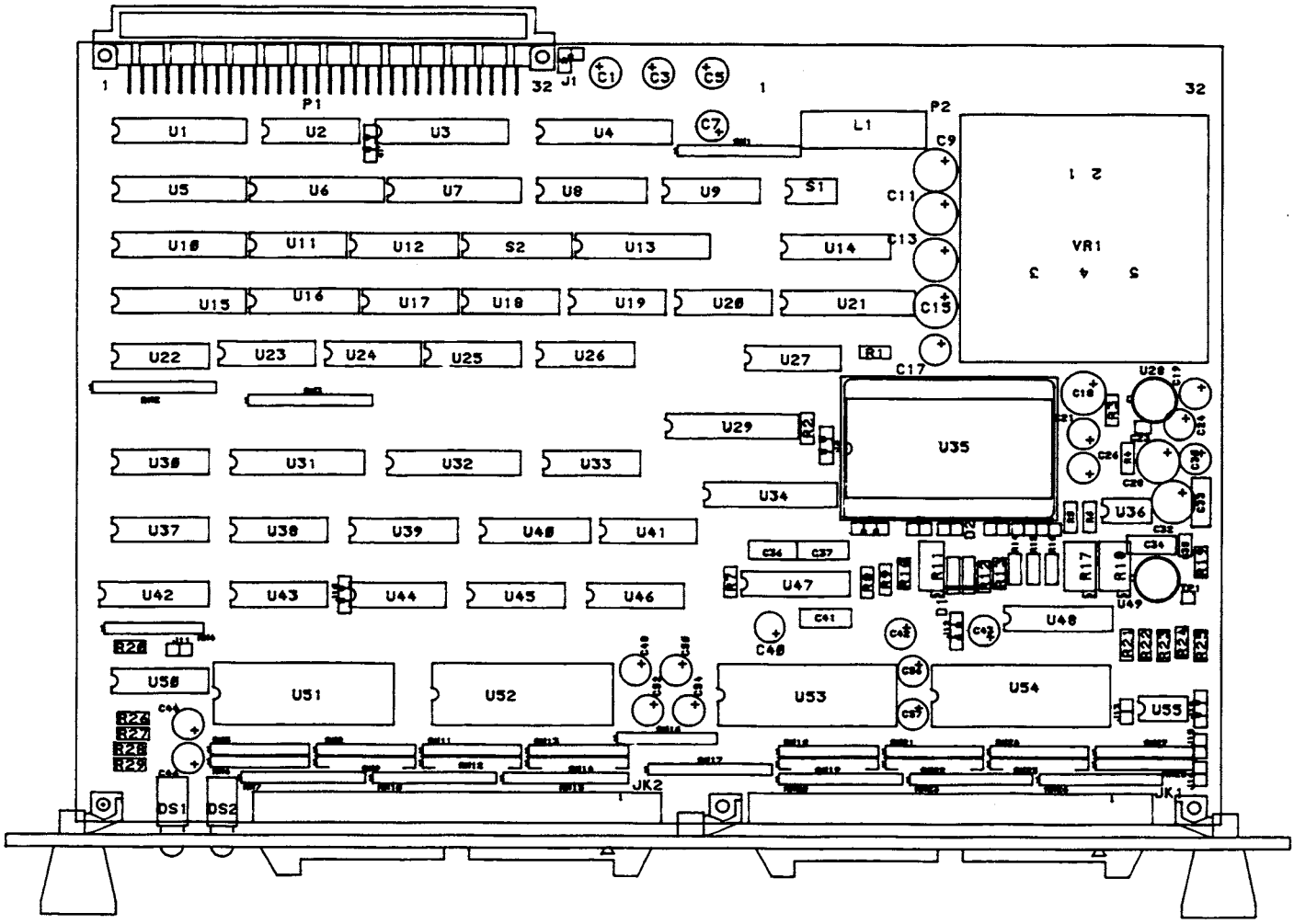
SCHEMATICS AND DIAGRAMS

Block Diagram

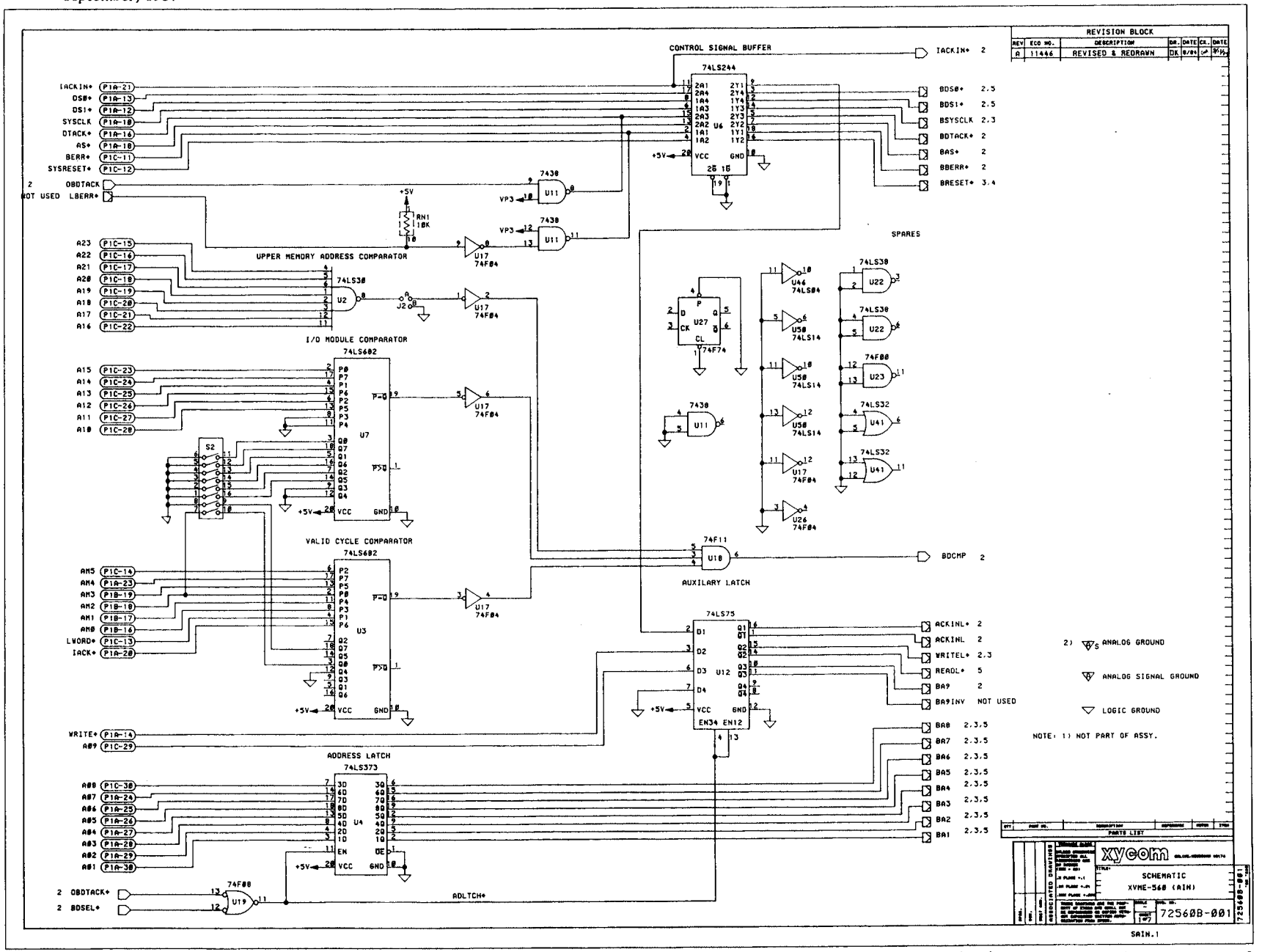


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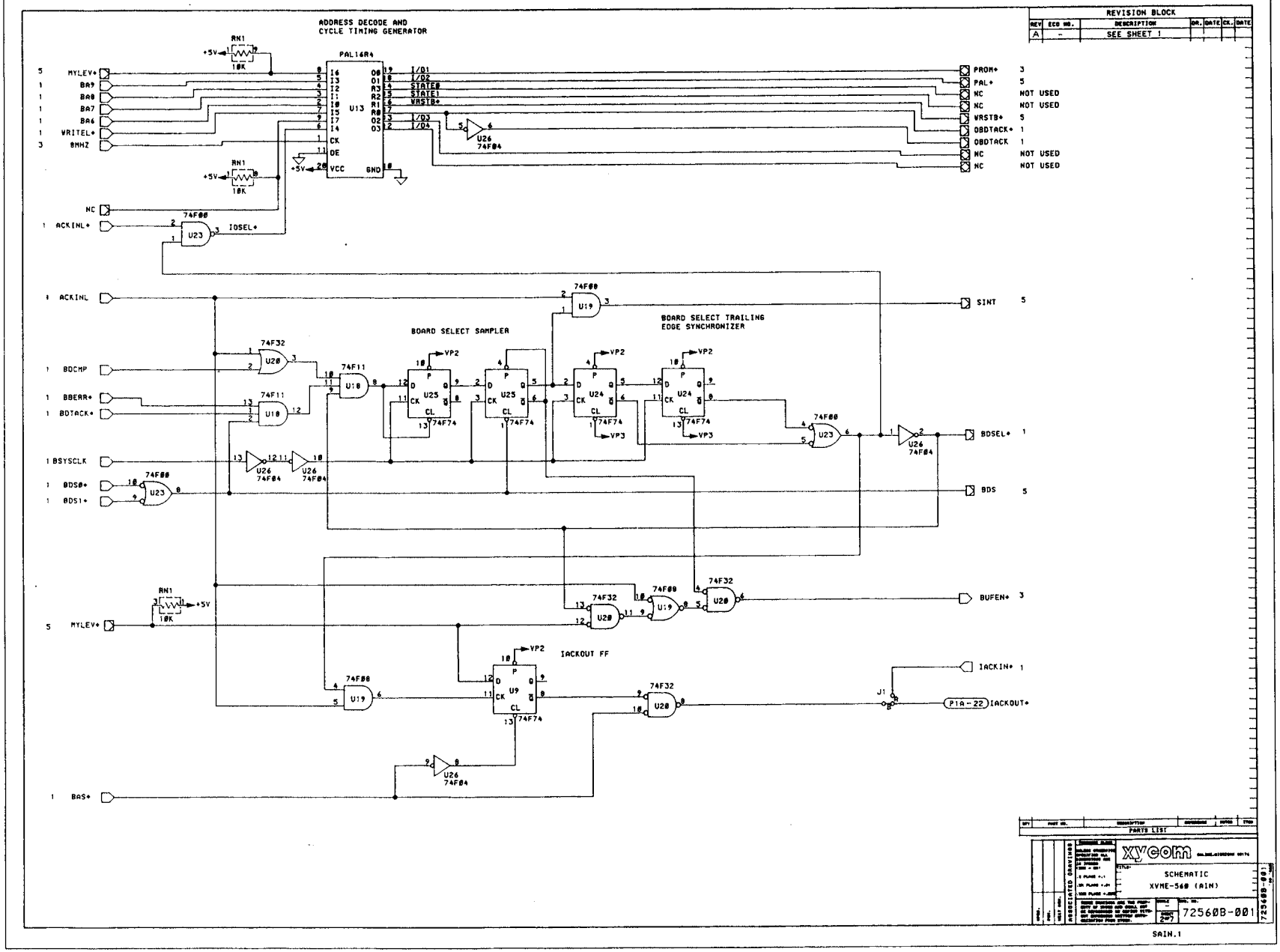
Assembly Drawing



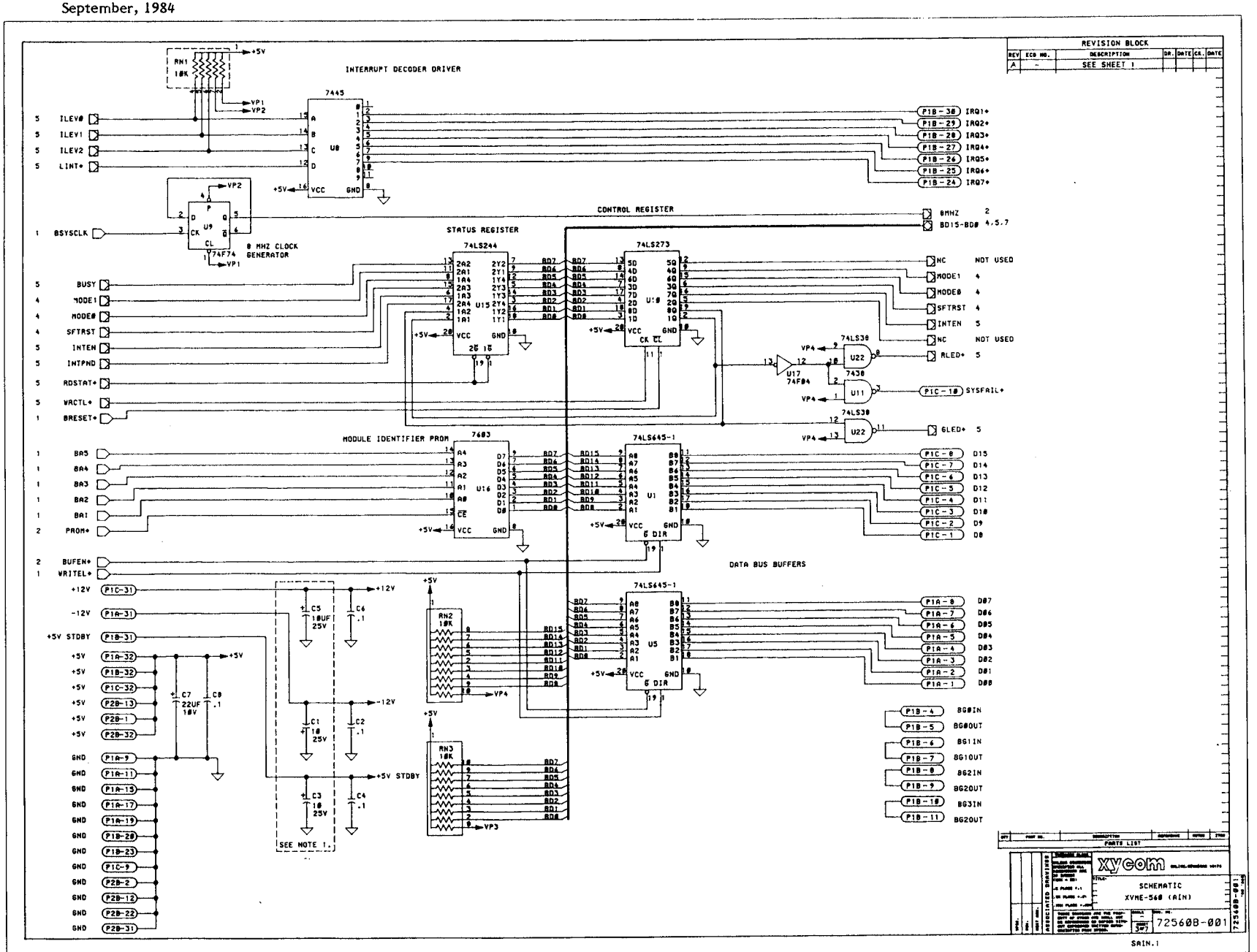
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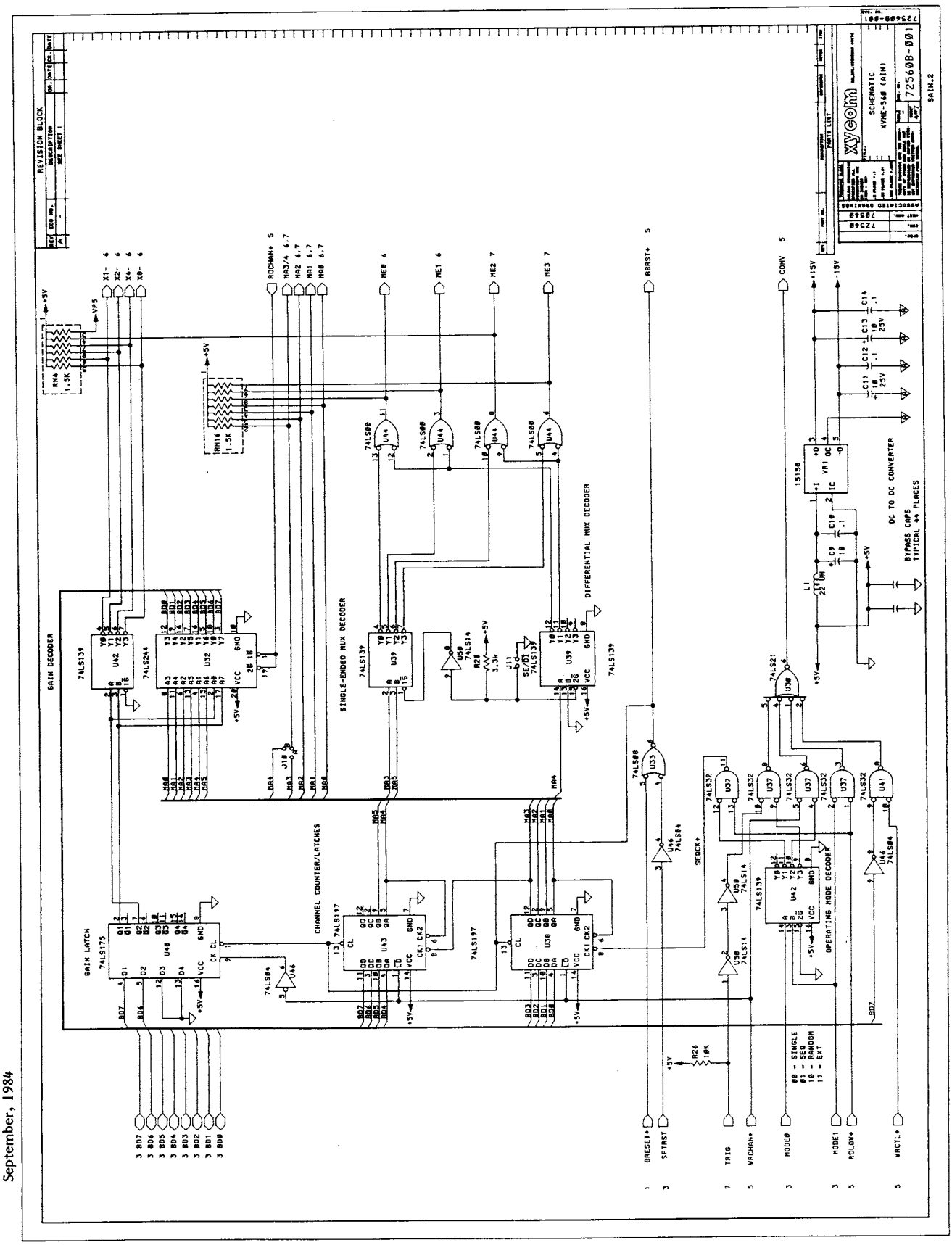
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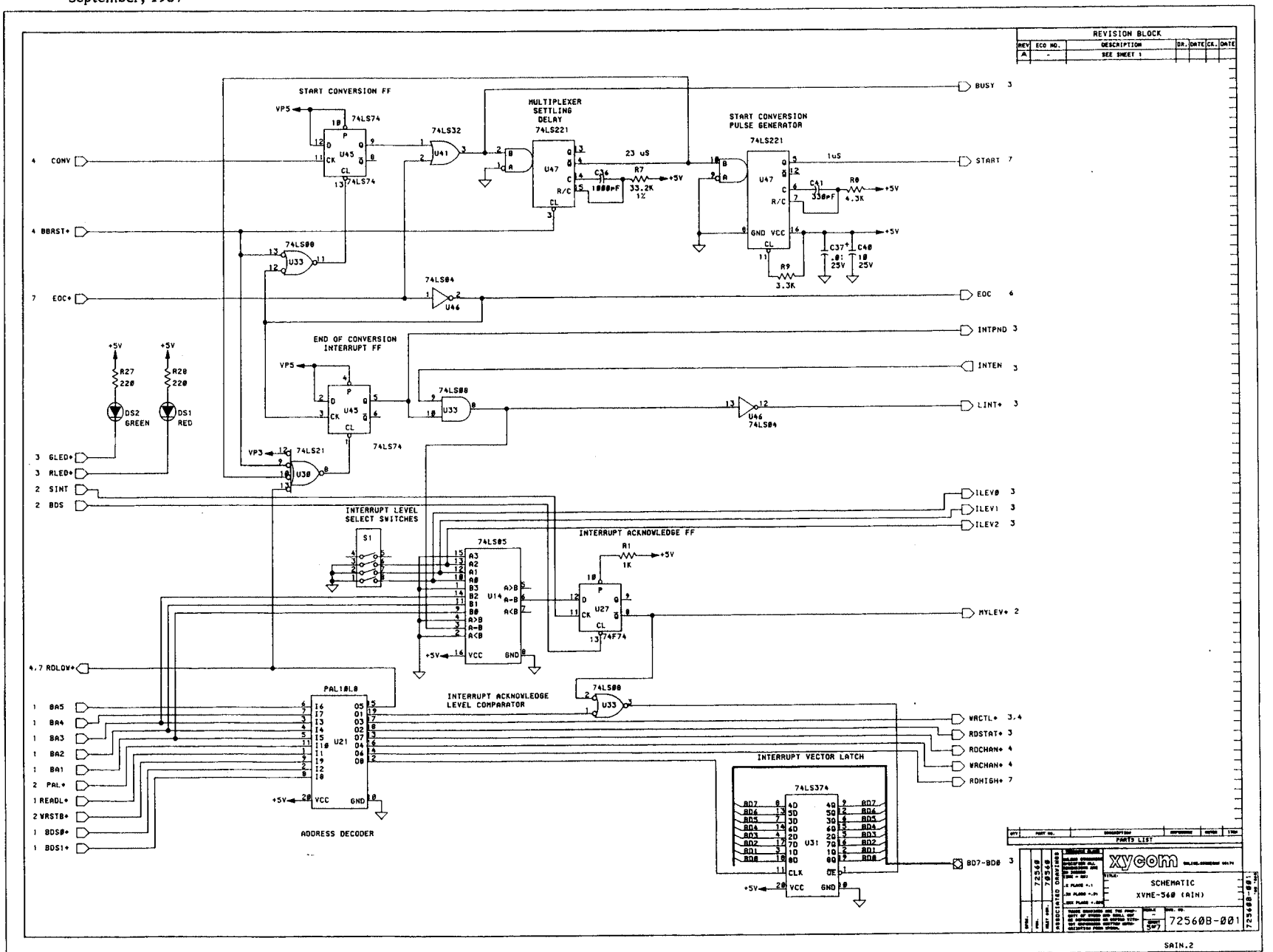


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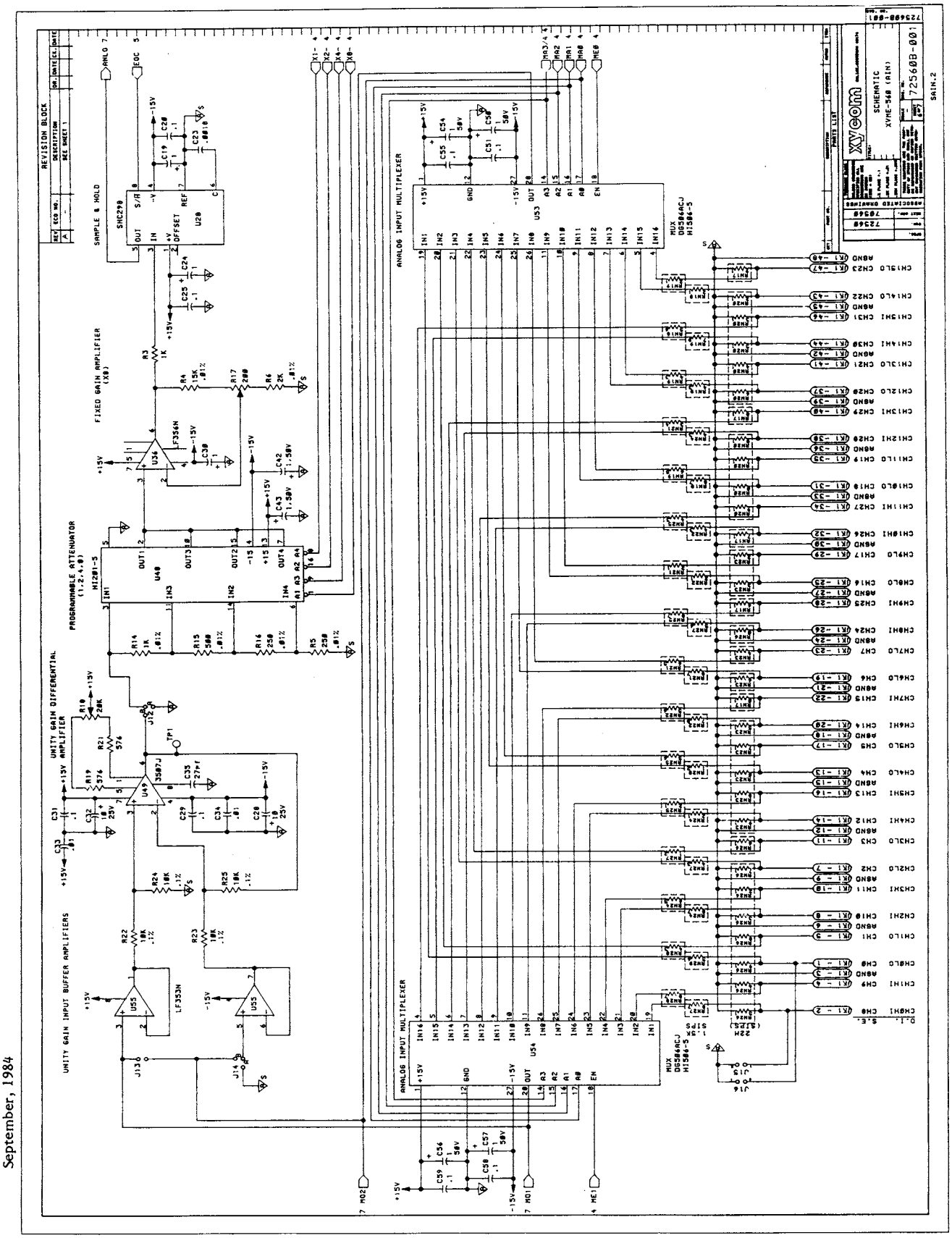


XVME-560 (AIN) Schematic, Sheet 4 of 7

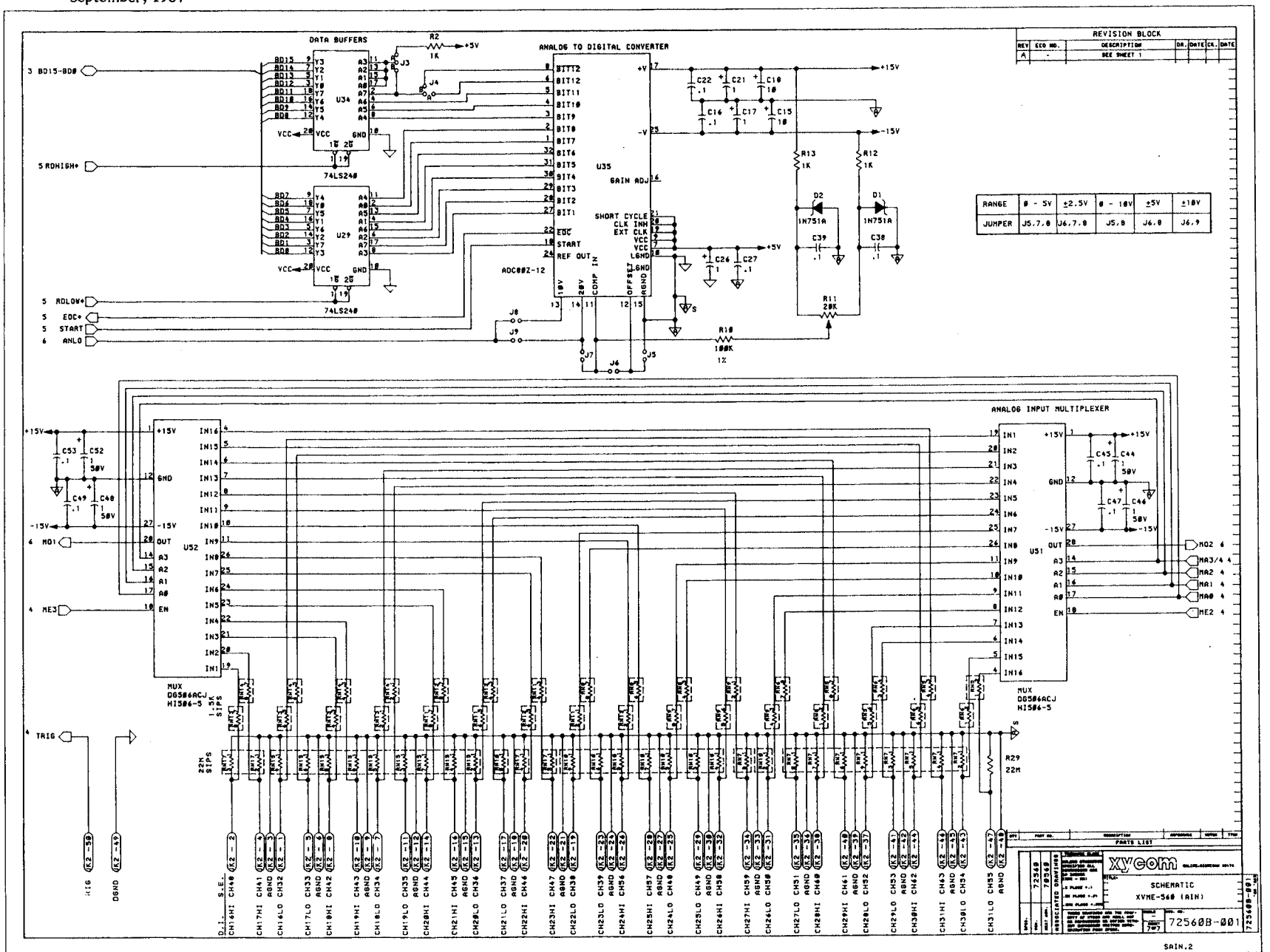
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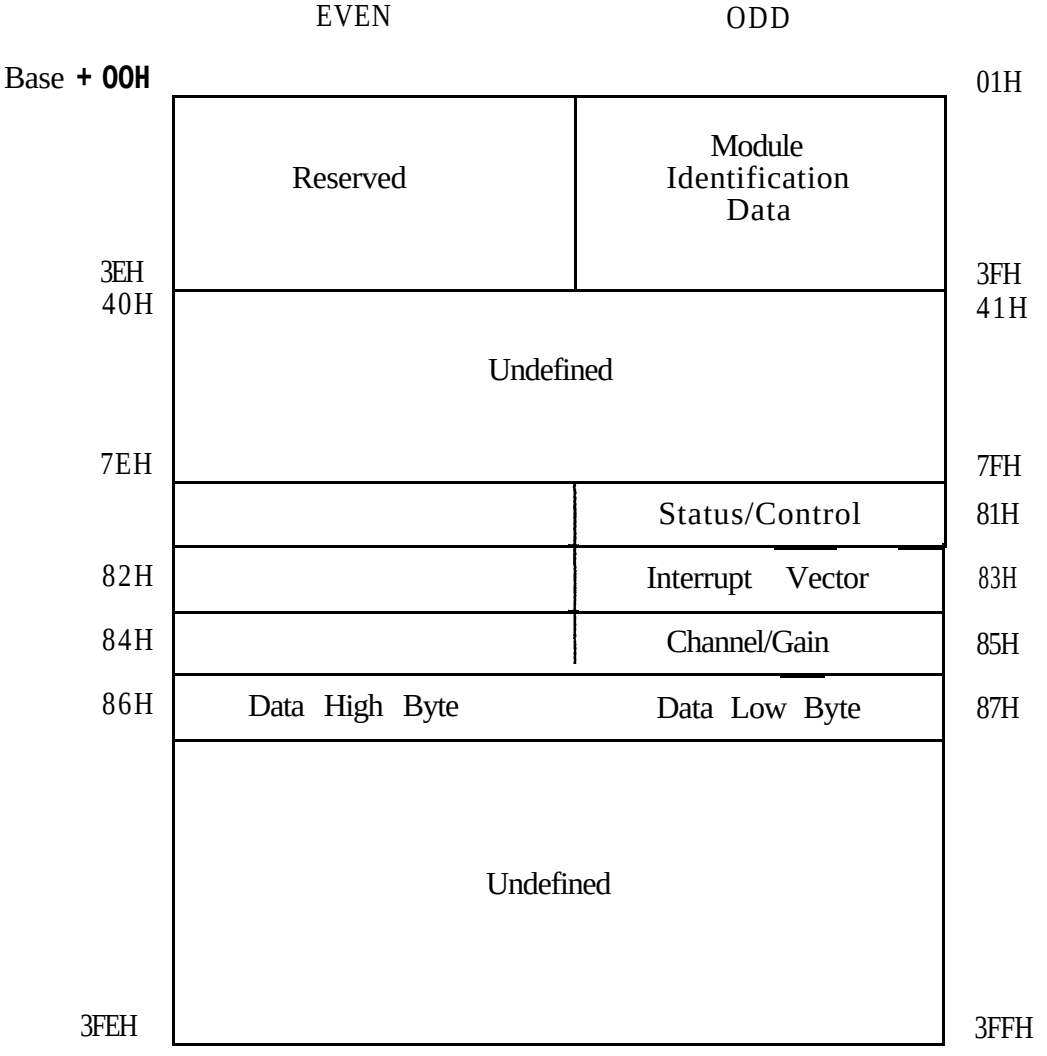
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Appendix D

QUICK REFERENCE GUIDE



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Table D-l. AIN Jumper/Switch List

Jumper/Switch	Use
JlB	Enables IACKIN*/INACKOUT* daisy chain (always installed).
J2A J2B	Memory mapped operation. Short I/O operation.
J3A J3B J4A J4B	These jumpers select the kind of digital code that will be produced as a result of reading an analog signal (see Table 2-9).
J5 J6 J7 J8 J9	These jumpers select one of the five input scaling ranges used (see Table 2-8).
J10A J10B J11 J13 J14A J14B	These jumpers select between single-ended or differential input (see Table 2-7).
J12	Test purposes only - J12B always installed.
J15 J16	Used in grounding channel zero for a ground reference (see Table 2-10).
Switch 1	Interrupt Level Select switches.
Switch 2	Address and Address Modifier module compare switches (see Tables 2-2 and Z-3).

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Table D-2. Interrupt Level Options

Switches 3	2	1	Level
0	0	0	No Level selected
0	0	1	Level 1
0	1	0	Level 2
0	1	1	Level 3
1	0	0	Level 4
1	0	1	Level 5
1	1	0	Level 6
1	1	1	Level 7

NOTE

Open = Logic "1"
Closed = Logic " 0 "

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Table D-4. Base Addresses

Switches						VME base address in VME Short I/O Address space
6(A15)	5(A14)	4(A13)	3(A12)	2(A11)	1(A10)	
0	0	0	0	0	0	0000H
0	0	0	0	0	1	0400H
0	0	0	0	1	0	0800H
0	0	0	0	1	1	0C00H
0	0	0	1	0	0	1000H
0	0	0	1	0	1	1400H
0	0	0	1	1	0	1800H
0	0	0	1	1	1	1C00H
0	0	1	0	0	0	2000H
0	0	1	0	0	1	2400H
0	0	1	0	1	0	2800H
0	0	1	0	1	1	2C00H
0	0	1	1	0	0	3000H
0	0	1	1	0	1	3400H
0	0	1	1	1	0	3800H
0	0	1	1	1	1	3C00H
0	1	0	0	0	0	4000H
0	1	0	0	0	1	4400H
0	1	0	0	1	0	4800H
0	1	0	0	1	1	4C00H
0	1	0	1	0	0	5000H
0	1	0	1	0	1	5400H
0	1	0	1	1	0	5800H
0	1	0	1	1	1	5C00H
0	1	1	0	0	0	6000H
0	1	1	0	0	1	6400H
0	1	1	0	1	0	6800H
0	1	1	0	1	1	6C00H
0	1	1	1	0	0	7000H
0	1	1	1	0	1	7400H
0	1	1	1	1	0	7800H
0	1	1	1	1	1	7C00H
1	0	0	0	0	0	8000H
1	0	0	0	0	1	8400H
1	0	0	0	1	0	8800H
1	0	0	0	1	1	8C00H
1	0	0	1	0	0	9000H
1	0	0	1	0	1	9400H
1	0	0	1	1	0	9800H
1	0	0	1	1	1	9C00H
1	0	1	0	0	0	A000H
1	0	1	0	0	1	A400H
1	0	1	0	1	0	A800H
1	0	1	0	1	1	AC00H
1	0	1	1	0	0	B000H
1	0	1	1	0	1	B400H
1	0	1	1	1	0	B800H
1	0	1	1	1	1	BC00H
1	1	0	0	0	0	C000H
1	1	0	0	0	1	C400H
1	1	0	0	1	0	C800H
1	1	0	0	1	1	CC00H
1	1	0	1	0	0	D000H
1	1	0	1	0	1	D400H
1	1	0	1	1	0	D800H
1	1	0	1	1	1	DC00H
1	1	1	0	0	0	E000H
1	1	1	0	0	1	E400H
1	1	1	0	1	0	E800H
1	1	1	0	1	1	EC00H
1	1	1	1	0	0	F000H
1	1	1	1	0	1	F400H
1	1	1	1	1	0	F800H
1	1	1	1	1	1	FC00H

NOTE

Open = Logic "1"
Closed = Logic "0"

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