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XVME-655

VMEbus Pentium® Processor Module

P/N 74655-002(H)

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Printed in the United States of America

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Revision	*Description*	*Date*
A	Manual Released	4/96
B	Manual Updated	7/96
C	Manual Updated with PCN 202	2/97
D	Manual Updated	7/97
E	Manual Updated	8/97
F	Manual Updated	6/98
G	Manual Updated	7/00
H	Manual Updated	3/01

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This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

European Union Directive 89/336/EEC requires that this apparatus comply with relevant ITE EMC standards. EMC compliance demands that this apparatus is installed within a VME enclosure designed to contain electromagnetic radiation and that will provide protection for the apparatus with regard to electromagnetic immunity. This enclosure must be fully shielded. An example of such an enclosure is a Schroff 7U EMC-RFI VME System chassis that includes a front cover to complete the enclosure.

The connection of nonshielded equipment interface cables to this equipment will invalidate EU EMC compliance and may result in electromagnetic interference and/or susceptibility levels that violate regulations that apply to legal operation of this device. It is the responsibility of the system integrator and/or user to apply the following directions, as well as those in the user manual, that relate to installation and configuration:

All interface cables should include braid/foil-type shields. Communication cable connectors must be metal with metal backshells (ideally, zinc die-cast types), and provide 360 degree protection about the interface wires. The cable shield braid must be terminated directly to the metal connector shell. Shield ground drain wires alone are not adequate. VME panel mount connectors that provide interface to external cables (e.g., RS-232, SCSI, keyboard, mouse, etc.) must have metal housings and provide direct connection to the metal VME chassis. Connector ground drain wires are not adequate.

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Chapter 1 – Introduction

The XVME-655 Pentium® PC/AT™-compatible VMEbus processor module is designed to combine the high performance and ruggedized packaging of the VMEbus with the broad application software base of the IBM PC/AT standard. The module integrates the latest processor and chipset technology. At the core of the module is an Intel® Pentium CPU, the highest performance PC-compatible processor available today. This new generation of Pentium processors uses power-reducing technology, allowing them to run at higher speeds and temperatures than their predecessors.

Module Features

The XVME-655 offers the following features:

- 75, 100, 133, 166, and 200 MHz Pentium CPUs, and 200 and 233 MHz MMX™ Pentium CPUs
- 8 Mbyte to 64 Mbyte fast-page EDO DRAM
- 512 Kbyte synchronous pipeline Level 2 cache (COAST) on 133, 166, 200, or 233 MHz CPU configurations
- PCI local bus
- PCI local bus SVGA controller, 1024 x 768
- PCI enhanced IDE controller with DMA
- PCI to VMEbus interface
- Two 16550-compatible serial ports
- EPP/ECP-compatible parallel port
- Optional PCI and PC/AT expansion
- Optional PCI Ethernet controller with 10BaseT and 10Base2 interfaces
- One floppy drive with a SA-450 interface

Architecture

This section describes the architecture of the XVME-655 processor module.

CPU Chip

The XVME-655 supports 75 MHz, 100 MHz, 133 MHz, 166 MHz, and 200 MHz Pentium processors, in addition to 200 MHz and 233 MHz MMX Pentium processors. The Pentium processor features a supescalar architecture with two pipelined integer units and a pipelined floating point unit which allows two instructions to be executed per clock cycle. A dynamic branch prediction unit and separate 8 Kbyte data and instruction caches further enhance Pentium performance.

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PCI Local Bus Interface

The PIIX device provides an accelerated PCI-to-ISA interface that includes a high-performance enhanced IDE controller, PCI and ISA master/slave interfaces, enhanced DMA functions, and plug-and-play port for on-board devices. The PIIX also provides many common I/O functions found in ISA-based PC systems, including a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and control logic for NMI generation.

Video Controller

The PCI bus video controller features a 64-bit graphics engine, with 24-bit RAMDAC for true color support. Resolutions up to 1024 x 768 with 256 colors are supported. It also incorporates the latest Green PC monitor plug-and-play features for power savings. The video controller also offers hardware-assisted video playback for Indeo™, Cinepak™, and MPEG-1. Refer to Appendix C for information on Super VGA modes supported.

Fast IDE controller

The enhanced IDE controller supports programmed I/O (PIO) and bus mastering DMA with transfer rates to 22 Mbytes/second. The controller also contains an 8 x 32-bit buffer for bus master IDE PCI burst transfers, and will support up to two IDE devices.

Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (refer to Chapter 3). The Autoconfig will attempt to classify the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

VMEbus Interface

The XVME-655 uses the PCI local bus to interface to the VMEbus. The VMEbus interface supports full DMA to/from the VMEbus, integral FIFOs for posted writes, block mode transfers, and read-modify-write operations. The interface contains four master and four slave images that can be programmed in a variety of modes to allow the VMEbus to be mapped into the XVME-655 local memory. This makes it easy to configure VMEbus resources in protected and real-mode programs.

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Expansion Options

The XVME-655 offers PCI, PC/104, and Ethernet expansion options. Ethernet expansion is available through the XVME-978 Ethernet expansion module. By simply plugging the XVME-978 directly into the XVME-655 PCI expansion connector, you add 32-bit bus mastering PCI Ethernet controller capabilities to your VMEbus system.

PC/104 and PCI Mezzanine Card (PMC) expansion is available through the XVME-976 module, which plugs into the XVME-978. The XVME-976 offers PMC and PC/104 sites, allowing easy integration of PC/AT-compatible modules in your VMEbus system.

On-board Memory

DRAM Memory

The XVME-655 has two 72-pin SIMM memory sites, providing up to 64 Mbytes of DRAM. The memory sites can be populated by standard fast page mode memory or extended data out memory (EDO). EDO memory is designed to improve DRAM read performance. Using EDO memory improves the back-to-back burst timing to 2-2-2 from 3-3-3 of standard memory.

Secondary Cache

All CPU configurations except the 75 MHz and 100 MHz models come equipped with 512 Kbyte pipeline burst cache.

Flash BIOS

The XVME-655 board provides a location for a Flash BIOS that is used for system and video BIOS. The Flash socket supports a 256 Kbyte x 8-bit or 512 Kbyte x 8-bit device. System BIOS and video BIOS are memory mapped in two locations in the Flash device.

Table Chapter 1 -1 provides the memory map for the 512 Kbyte Flash device.

Table Chapter 1 -1. 512 Kbyte Flash Memory Map

Device Address	Device	System Address
70000h-7FFFFh	System BIOS	F0000h-FFFFFh also FFFF0000h-FFFFFFFFh
60000h-6FFFFh	System BIOS	E0000h-EFFFFh also FFFE0000h-FFFEFFFFh
50000h-5FFFFh	Option ROM	D0000h-DFFFFh also FFFD0000h-FFFDFFFFh
48000h-4FFFFh	Option ROM	C8000h-CFFFFh also FFFC8000h-FFFCFFFFh
40000h-47FFFh	Video BIOS	C0000h-C7FFFh also FFFC0000h-FFFC7FFFh
30000h-3FFFFh	System BIOS	F0000h-FFFFFh also FFFF0000h-FFFFFFFFh
20000h-2FFFFh	System BIOS	E0000h-EFFFFh also FFFE0000h-FFFEFFFFh
10000h-1FFFFh	Option ROM	D0000h-DFFFFh also FFFD0000h-FFFDFFFFh
08000h-0FFFFh	Option ROM	C8000h-CFFFFh also FFFC8000h-FFFCFFFFh
00000h-07FFFh	Video BIOS	C0000h-C7FFFh also FFFC0000h-FFFC7FFFh

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An on-board switch controls which part of the Flash device is loaded into shadow DRAM. This allows you to update half the Flash device and still retain a copy of the original BIOS if the update is not successful or the BIOS is incorrect. To determine which section of the BIOS is being used, write to port 219h (bit 2=0) and then read bit 3 from port 219h. If bit 3 returns a zero, the lower portion of the BIOS is being used.

Serial and Parallel Ports

PC/AT peripherals include two high-speed 16550-compatible serial ports, one ECP/EPP parallel port, and a PS/2-compatible keyboard port.

Keyboard Interface

The keyboard interface uses a PS/2-style connector out the front panel. The +5 V is protected with a polyswitch. This device opens if the +5 V is shorted to GND. Once the shorting condition is removed, the polyswitch will allow current flow to resume.

Hard and Floppy Drives

The XVME-655's IDE hard drive and floppy drive signals are routed through the P2 connector, providing a simplified method of connecting external floppy and hard drives. The XVME-655 supports only one floppy drive.

When used with the XVME-977 mass storage module, hard and floppy drives do not have to be located next to the processor. The XVME-977 can be installed in any unoccupied VMEbus slot, and then connected to the XVME-655 through a cable on the J2 connectors. This allows greater flexibility in configuring a VMEbus card cage.

For applications that require mass storage outside the VMEbus chassis, the XVME-973 driver adapter module plugs onto the VMEbus P2 connector. This module provides industry standard connections for IDE and floppy signals. You can connect one floppy drive to the XVME-973. This drive may be 2.88 Mbytes, 1.44 Mbytes, 1.2 Mbytes, 720 Kbytes, or 360 Kbytes.

Caution

The total cable length must not exceed 18 inches. Also, if two drives are connected, they must be no more than six inches apart.

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Operational Description

Figure Chapter 1 -1 illustrates the XVME-655 block diagram.

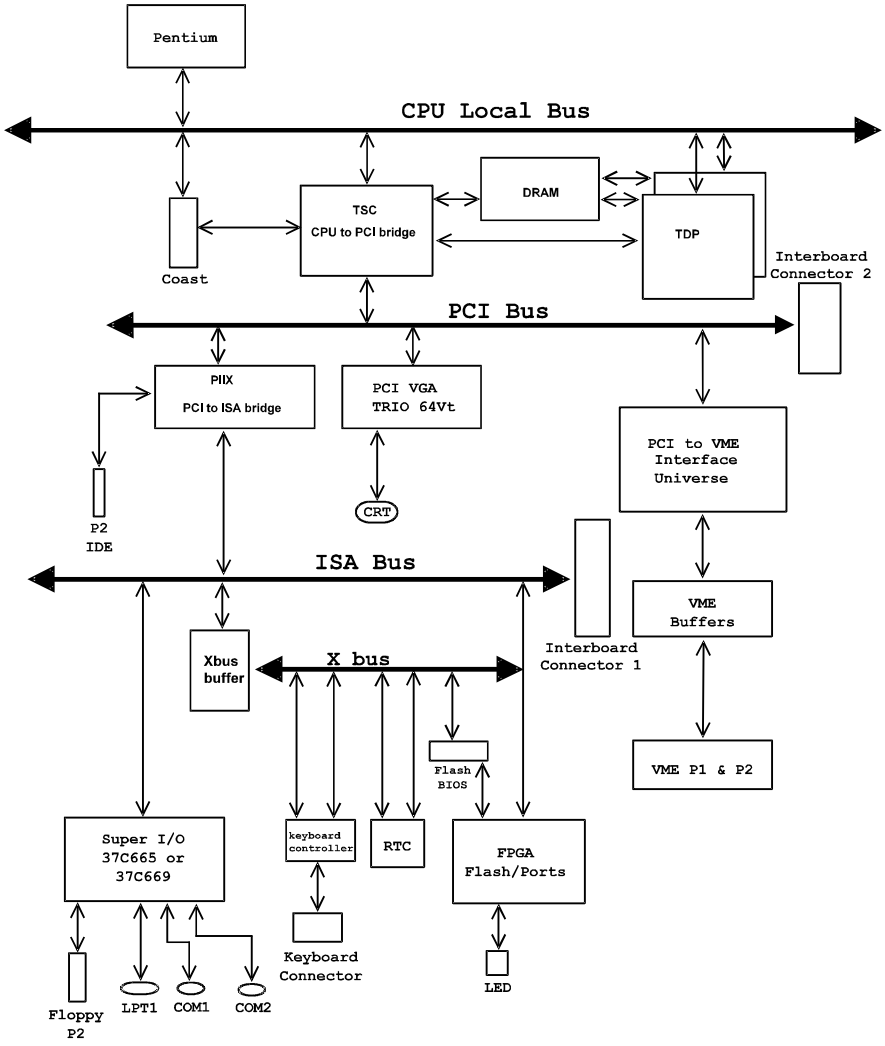


Figure Chapter 1 -1. XVME-655 Block Diagram

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Environmental Specifications

Table Chapter 1 -2. Environmental Specifications

Characteristic	Specification
Temperature	
Operating	
with external 100 CFM fan forced air flow	
200 MHz MMX	0° to 46°C (32° to 114°F)
233 MHz MMX	0° to 43°C (32° to 109°F)
Non-operating	-40° to 85°C (-40° to 185°F)
Vibration	
Frequency	5 to 2000 Hz
Operating	.015" peak-to-peak displacement, 2.5 g (maximum) acceleration
(with COAST module in stalled)	.015" peak-to-peak displacement, 1 g (maximum) acceleration
Non-operating	.030" peak-to-peak displacement, 5.0 g (maximum) acceleration
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-operating	50 g peak acceleration, 11 msec duration
Humidity	20% to 95% RH, non-condensing

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Hardware Specifications

Table Chapter 1 -3. Hardware Specifications

Characteristic	Specification
Power Specifications	
+12V	75 mA maximum
-12V	24 mA maximum
+5V	
75 MHz	5.1 A (maximum), 3.9 A (typical)
100 MHz	5.8 A (maximum), 4.6 A (typical)
133 MHz	5.8 A (maximum), 4.5 A (typical)
166 MHz	6.4 A (maximum), 5.0 A (typical)
200 MHz	7.3 A (maximum), 5.8 A (typical)
200 MHz MMX	10.02 A (maximum), 7.42 A (typical)
233 MHz MMX	10.59 A (maximum), 8.19 A (typical)
CPU speed (MHz)	75, 100, 133, 166, 200, 200 MMX, or 233 MMX
PCI Super VGA Graphics Controller	1024x768, 256 colors maximum resolution 1 Mbyte video DRAM
Serial Ports (2)	16550 compatible
Parallel Interface	EPP/ECP compatible
On-board memory	EDO DRAM, 8 to 64 Mbytes
VMEbus Compliance Complies with VMEbus Specification, IEEE 1014–1987 Rev. C.1 A32/A24/A16:D64/D32/D16/D08(EO) DTB Master A32/A24:D64/D32/D16/D08(EO) DTB Slave R(0-3) Bus Requester Interrupter I(1)-I(7) DYN IH(1)-IH(7) Interrupt Handler SYSCLK and SYSRESET Driver PRI, SGL, RRS Arbiter RWD, ROR bus release Form Factor: Double-height, double-width 233.35 mm x 160 mm (9.2” x 6.3”)	

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Chapter 2 – Installation

This chapter provides information on configuring the XVME-655. It also provides information on installing the module into a backplane.

Figure Chapter 2 -1 illustrates the jumper, switch, and connector locations on the XVME-655.

Figure Chapter 2 -1. XVME-655 Jumper, Switch, and Connector Locations

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Voltage Control Module (P4)

Because MMX CPU chips have different voltage requirements than non-MMX CPU chips, MMX CPUs require special voltage control modules.

CPU Type	Voltage Control Module Part Number
MMX	122032A-001
Non-MMX	108168A-001

Warning

If you use the non-MMX voltage control module (part number 108168A-001) with MMX CPUs, you may damage the CPU chip.

Jumper Settings

Table Chapter 2 -1 defines the default jumper settings for the XVME-655's processor configurations.

Table Chapter 2 -1. Default Jumper Settings

Configuration	J1	J2	J3	J4	J6	J7	J8
75 MHz	A	B	B	B	A	A	B
100 MHz	A	A	A	B	A	A	B
133 MHz	A	A	A	B	B	A	B
166 MHz	A	A	A	B	B	B	B
200/200 MMX MHz	A	A	A	B	A	B	B
233 MMX MHz	A	A	A	B	A	A	B

Host Bus Frequency Select

J7 (BF1)	J6 (BF)	Frequency Fraction
B	B	2/5 (150/166)
B	A	1/3 (200/200 MMX)
A	B	1/2 (120/133)
A	A	2/3 (75/90/100)
A	A	1/3.5 (233 MMX)

PCI Bus Frequency Select

J2	PCI Frequency to set up AT-bus
A	33 MHz/30 MHz
B	25 MHz

CPU Clock Selection

J4	J3	Frequency Fraction

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B	B	50 MHz (75)
A	B	60 MHz (90/120/150)
B	A	66 MHz (100/133/166/200/ 200 MMX/233 MMX)
A	A	Undefined

Lattice Programming Port (J5)

This jumper is reserved for Xycom use.

ORB_GND Selection

J8	ORB_GND Connected to Digital GND
A	No
B	Yes

VGA Enable

J1	VGA Enable
A	Enable
B	Disable

Switch Settings

The XVME-655 has one eight-position switch, as described in Table Chapter 2 -2. (⌧ indicates the default setting.)

Table Chapter 2 -2. Switch Settings

Position	Open	Closed
1	VME resets only VME interface	⌧ VME reset causes CPU and VME interface reset
2	Front panel toggle switch causes no VMEbus reset	⌧ Front panel toggle switch causes VMEbus reset
3	⌧ Sysfail asserted on VME reset	Sysfail not asserted on VME reset
4	⌧ CMOS okay	CMOS cleared by BIOS
5	Front panel toggle switch causes no CPU reset	⌧ Front panel toggle switch causes CPU reset
6	⌧ Upper Flash BIOS	Lower Flash BIOS
7	⌧ Keyboard as input	Keyboard inhibit
8	⌧ Color	Monochrome

Registers

The XVME-655 contains two I/O ports: 219h and 218h.

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Register 219h – LED/BIOS Port

Table Chapter 2 -3 describes the LEDs and signals that register 219 controls.

Table Chapter 2 -3. LED/BIOS Port

Bit	LED/Signal	Result	R/W
0	FAULT	1 = Fault LED off 0 = Fault LED on	R/W
1	PASS	1 = PASS LED on 0 = PASS LED off	R/W
2	FLASHWR	1 = Flash write enabled/A18 enable	R/W
3	FLB-A18	Flash BIOS Address A18; when FLASHWR = 0 reads switch position 6	R
4	Reserved	0	R/W
5	BIOS_C8	1 = Enable C8000h-CFFFFh on-board BIOS	R/W
6	BIOS_D0	1 = Enable D0000h - D7FFFh on-board BIOS	R/W
7	BIOS_D8	1 = Enable D8000h - DFFFFh on-board BIOS	R/W

Register 218h – TEMP/Abort Port

This register controls the temperature sensor and the abort toggle switch. It also allows you to read the CMOS clear switch and VGA enable.

Table Chapter 2 -4. Temp/Abort Port

Bit	Signal	Result	R/W
0	TS_RESET	0 = Reset temperature sensor interface	R/W
1	TS_WRITE	Write data bit must be high when reading temperature sensor	R/W
2	TS_DQ	Temperature sensor read data bit	R
3	TS_CLK	A low to high will clock in or clock out bit	R/W
4	ABORT_STS	1 = Abort toggle switch caused interrupt	R
5	ABORT_CLR	1 = Enable abort 0 = Clear and disable abort	R/W
6	VGA_EN	1 = On-board VGA controller enabled	R
7	CLRCMOS	1 = CMOS okay 0 = Clear CMOS	R

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Connectors

This section provides the pinouts for the XVME-655 connectors.

Serial Port Connectors

COM1

Pin	Signal
1	DCD1
2	RXD1
3	TXD1
4	DTR1
5	GND
6	DSR1
7	RTS1
8	CTS1
9	RI1

COM2

Pin	Signal
1	DCD2
2	RXD2
3	TXD2
4	DTR2
5	GND
6	DSR2
7	RTS2
8	CTS2
9	RI2

Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE	14	AUTOFEED
2	PDOUT0	15	PERROR
3	PDOUT1	16	INIT
4	PDOUT2	17	SELIN
5	PDOUT3	18	GND
6	PDOUT4	19	GND
7	PDOUT5	20	GND
8	PDOUT6	21	GND
9	PDOUT7	22	GND
10	PACK	23	GND
11	PBUSY	24	GND
12	PE	25	GND
13	SELECT		

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VGA Connector

Pin	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	KEY
10	GND
11	NC
12	DDC.ID
13	HYSNC
14	VSYNC
15	NC

Keyboard Port Connector

Pin	Signal
1	DATA
2	NC
3	GND
4	+5V
5	CLK
6	NC

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VMEbus Connectors

P1 and P2 are the VMEbus connectors.

P1 Connector

Pin	A	B	C
1	D00	BBBUSY	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT	BERR*
12	DS1*	BR0*	SYSRESET
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	NC	A17
22	IACKOUT*	NC	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	NC	+12V
32	+5V	+5V	+5V

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P2 Connector

Pin	A	B	C
1	RES	+5V	HDRESET*
2	RES	GND	HD0
3	RES	RES	HD1
4	RES	A24	HD2
5	RES	A25	HD3
6	RES	A26	HD4
7	RES	A27	HD5
8	RES	A28	HD6
9	RES	A29	HD7
10	RES	A30	HD8
11	RES	A31	HD9
12	RES	GND	HD10
13	RES	+5V	HD11
14	RES	VD16	HD12
15	RES	VD17	HD13
16	RES	VD18	HD14
17	RES	VD19	HD15
18	RES	VD20	GND
19	GND	VD21	DIOW*
20	FRWC*	VD22	DIOR*
21	IDX*	VD23	IORDY
22	MO1*	GND	ALE (10K
23	HD_DRQ0	VD24	IRQ14
24	FDS1*	VD25	IOCS16* (nc)
25	HD_DACK	VD26	DA0
26	FDIRC*	VD27	DA1
27	FSTEP*	VD28	DA2
28	FWD*	VD29	CS1P*
29	FWE*	VD30	CS3P*
30	FTK0*	VD31	IDEATP* (nc)
31	FWP*	GND	FHS*
32	FRDD*	+5V	DCHG*

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Interboard Connector 1 (P5)

Pin	Signal	Pin	Signal
1	SYSCLK	41	SA10
2	OSC	42	SA11
3	SD(15)	43	SA12
4	SD(14)	44	SA13
5	SD(13)	45	SA14
6	SD(12)	46	SA15
7	SD(11)	47	SA16
8	SD(10)	48	SA17
9	SD(9)	49	SA18
10	SD(8)	50	SA19
11	MEMW*	51	BALE
12	MEMR*	52	TC
13	DRQ5	53	DACK2*
14	DACK5*	54	IRQ3
15	DRQ6	55	IRQ4
16	DACK6*	56	SBHE*
17	LA17	57	IRQ5
18	LA18	58	IRQ6
19	LA19	59	IRQ7
20	LA20	60	REF*
21	LA21	61	DRQ1
22	LA22	62	DACK1*
23	LA23	63	RESETDRV
24	IRQ14	64	IOW*
25	IRQ15	65	IOR*
26	IRQ12	66	SMEMW*
27	IRQ11	67	AEN
28	IRQ10	68	SMEMR*
29	IOCS16*	69	IOCHRDY
30	MEMCS16*	70	SD(0)
31	SA0	71	SD(1)
32	SA1	72	SD(2)
33	SA2	73	SD(3)
34	SA3	74	SD(4)
35	SA4	75	SD(5)
36	SA5	76	SD(6)
37	SA6	77	SD(7)
38	SA7	78	DRQ2
39	SA8	79	IRQ9
40	SA9	80	IOCHCK*

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Interboard Connector 2 (P3)

This connector supports the V/IO voltage through the center pins. It also provides GND and +5 V through the center connector for the XVME-978 card.

Pin	Signal	Pin	Signal
1	TCLK	41	AD(23)
2	TRST*	42	AD(22)
3	TMS	43	AD(21)
4	TDO	44	AD(20)
5	TDI	45	AD(19)
6	PCI-RSVD9A (pn2-8)	46	AD(18)
7	PCI-RSVD10B (pn2-9)	47	AD(17)
8	PCI-RSVD11A (pn2-10)	48	AD(16)
9	PCI-RSVD14A (pn1-12)	49	BE2*
10	PCI-RSVD14B (pn1-10)	50	FRAME*
11	PCI-RSVD19A (pn2-17)	51	IRDY*
12	PMC-RSVD (pn2-34)	52	TRDY*
13	PMC-RSVD (pn2-52)	53	DEVSEL*
14	PMC-RSVD (pn2-54)	54	STOP*
15	PCICLK3 (NC)	55	PLOCK*
16	PIRQA*	56	PERR*
17	PIRQB*	57	SDONE
18	PIRQC*	58	SBO*
19	PIRQD*	59	SERR*
20	REQ3*	60	PAR
21	PCICLK2 (NC)	61	BE1*
22	REQ1*	62	AD(15)
23	GNT3*	63	AD(14)
24	PCICLK1	64	AD(13)
25	GNT1*	65	AD(12)
26	PCIRST*	66	AD(11)
27	PCICLK0	67	AD(10)
28	GNT0*	68	AD(9)
29	REQ0*	69	AD(8)
30	REQ2*	70	BE0*
31	AD(31)	71	AD(7)
32	AD(30)	72	AD(6)
33	AD(29)	73	AD(5)
34	AD(28)	74	AD(4)
35	AD(27)	75	AD(3)
36	AD(26)	76	AD(2)
37	AD(25)	77	AD(1)
38	AD(24)	78	AD(0)
39	BE3*	79	ACK64*
40	GNT2*	80	REQ64*

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CPU Fan Power Connector

The fan +12 V and +5 V supplies are protected with a polyswitch. This device will open up if +12 V or +5 V is shorted to GND. Once the shorting condition is removed, the polyswitch will allow current flow to resume.

Pin	Signal
1	+12V (fused)
2	+5V (fused)
3	GND

Installing the XVME-655 into a Backplane

This section provides the information necessary to install the XVME-655 into the VMEbus backplane.

The XVME-655 is a double-high, single-board VMEbus module that occupies two VMEbus slots.

Note

Xycom modules are designed to comply with all physical and electrical VMEbus backplane specifications.

Caution

Do not install the XVME-655 on a VMEbus system without a P2 backplane.

Warning

Never install or remove any boards before turning off the power to the bus and all related external power supplies.

1. Disconnect all power supplies to the backplane and card cage, and disconnect the power cable.
2. Make sure backplane connectors P1 and P2 are available.
3. Verify all jumper settings.
4. Verify that the card cage slot that will hold the XVME-655 is clear and accessible, as well as the card cage slot to the right of the board.
5. Install the XVME-655 into the card cage by centering the unit on the plastic guides in the slots (P1 connector facing up). Push the board slowly toward the rear of the chassis until the P1 and P2 connectors engage. The board should slide freely in the plastic guides.

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Caution

Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

6. Secure the module to the chassis by tightening the machine screw at the top and bottom of the board.
7. Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the XVME-655 board as follows:

Connector	Label
VGA cable	VGA
Keyboard	KeyBD
Serial Devices	COM1 and COM2
Parallel device	LPT1

Note

The floppy drive and hard drive are either cabled across P2 to the XVME-977 disk unit, or they are connected to the XVME-973 board. Refer to Chapter 5 for more information on the XVME-973.

8. Turn on power to the VMEbus card cage.

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Figure Chapter 2 -2 illustrates the XVME-655's front panel, to help you locate connectors.

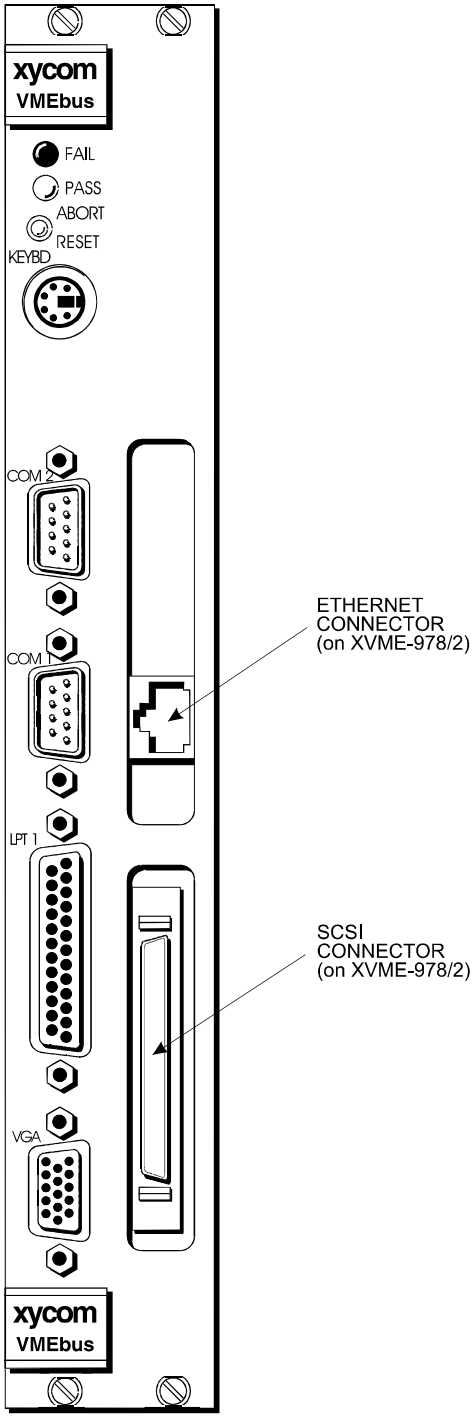


Figure Chapter 2 -2. XVME-655 Module Front Panel

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Chapter 3 – BIOS Setup Menus

The XVME-655 board's customized BIOS has been designed to surpass the functionality provided for normal PC/ATs. This custom BIOS allows you to access the value-added features on the XVME-655 module without interfacing to the hardware directly.

Moving through the Menus

General instructions for navigating through the screens are described below:

Key	Result
F1 or ALT-H	General Help window
ESC	Exits the menu
← or → arrow keys	Selects a different menu
↑ or ↓ arrow keys	Moves the cursor up and down
TAB or SHIFT + TAB	Cycles the cursor up or down
HOME or END	Moves the cursor to the top or bottom of the window
PGUP or PGDN	Moves the cursor to the next or previous page
F5 or -	Selects the previous value for the field
F6 or + or SPACE	Selects the next value for the field
F9	Loads the default configuration values for the menu
F10	Loads the previous configuration values for the menu
ENTER	Executes the selected command or opens the selected submenu (a "▸" indicates a submenu)
ALT-R	Refreshes the screen

To select an item, use the arrow keys to move the cursor to the field you want. Then use the + and - keys to select a value for that field. The Save Changes and Save Changes & Exit commands in the Exit Menu save the values currently displayed in all the menus.

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BIOS Main Setup Menu

To start the BIOS Setup utility:

1. Turn on or reboot your system. The BIOS displays the following message:

   "Press F2 to enter Setup."

2. Press F2 to access the Main Menu.

```
PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.

   Main      Advanced      Security      VMEbus      Exit

                                                  Item Specific Help

 System Time:                [16:19:20]

 System Date:                [03/02/95]

 Diskette A:                 [1.44 MB, 3½"]       If the line item you are

 Diskette B:                 [Not Installed]      viewing has specific
                                                  help,
▶IDE Adapter 0 Master        (C: 260 Mb)          it will be listed here.
▶IDE Adapter 0 Slave         (D:105 Mb)
 Video System:               [EGA/VGA]
▶Memory Cache:
▶Memory Shadow               Enabled
▶Boot sequence:              [A: then C:]
▶Numlock:                    [Auto]

 System Memory:               640 KB
 Extended Memory:               7 MB

F1   Help      ↑↓   Select Item    -/+    Change Values        F9  Setup Defaults
ESC  Exit      ←→   Select Menu    Enter  Select ▶ Sub-Menu    F10 Previous Values
```

Figure Chapter 3 -1. Main Setup Menu

Option	Description
System Time (HH/MM/SS)	Sets the real-time clock for hour, minute, and seconds. The hour is calculated according to a 24-hour military clock (i.e., 00:00:00 through 23:59:59). Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.

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Option	Description
System Date (MM:DD:YYYY)	Sets the real-time clock for the month, day, and year. Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.
Diskette A or B	Selects the floppy disk drive installed in your system.
Video System	Selects the default video device.
System Memory	Displays the amount of conventional memory detected during boot-up. This field is not user configurable.
Extended Memory	Displays the amount of extended memory detected during boot-up. This field is not user configurable.

IDE Adapter 0 Master and Slave Submenus

Use the IDE Adapter 0 Master and Slave submenus to configure IDE hard drive information. If only one drive is attached to the IDE adapter, then you only need to enter the parameters in the Master Submenu. If two drives are connected, you need to enter parameters in both the Master and Slave submenus. The Master and Slave submenus contain the same information.

```
            PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
     Main
IDE Adapter 0 Master (C: 260 Mb)                    Item Specific Help

Autotype Fixed Disk:          [Press Enter]

Type:                         [User] 260 Mb

Cylinders:                    [907]                 If the line item you are

Heads:                        [    14]              viewing has specific help,

Sectors/Track:                [    40]              it will be listed here.

Write Precomp:                [None]

Multi-Sector Transfers:       [8 Sectors]

LBA Mode Control:             [Enabled]

32 Bit I/O:                   [Disabled]

Transfer Mode:                [Standard]

F1   Help      ↑↓  Select Item   -/+    Change Values      F9  Setup Defaults
ESC  Exit      ←→  Select Menu   Enter  Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -2. IDE Adapter Submenu

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Option	Description
Autotype Fixed Disk	Reads the hard disk parameters from the drive if you press ENTER. It then sets the Type field to “User” and lets you edit other fields. Do not attempt to manually set the disk drive parameters unless instructed to do so by Xycom Application Engineering.
Type	Options are “1 to 39”, “User,” and “Auto.” The “1 to 39” option fills in all remaining fields with values for predefined disk type. “User” prompts you to fill in remaining fields. “Auto” autotypes at each boot, displays settings in setup menus, and does not allow you to edit the remaining fields.
Cylinders	Indicates the number of cylinders on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Heads	Indicates the number of read/write heads on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Sectors/Track	Indicates the number of sectors per track on the hard drive. This information is automatically entered if the Autotype Fixed Disk option is set.
Write Precomp	This value is not used or required by IDE hard drives.
Multi-Sector Transfers	Options are “Auto,” “2,” “4,” “8,” and “16” sectors. “Auto” sets the number of sectors per block to the highest number supported by the drive.
LBA Mode Control	Enables Logical Block Access (LBA). Default is disabled and should work with most hard drives.
32-Bit I/O	Enables 32-bit communication between the CPU and IDE interface.
Transfer Mode	Selects the method for transferring the data between the hard disk and system memory. Available options are determined by the drive type and cable length.

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Memory Cache Submenu

Enabling cache increases CPU performance by holding data most recently accessed in a special high-speed static RAM area called cache. The XVME-655 provides two levels of cache memory; level one is 16 Kbytes internal to the Pentium processor, and level two, or external cache, is the cache-on-a-stick site (COAST) which can accommodate 256 or 512 Kbytes of high-speed cache memory.

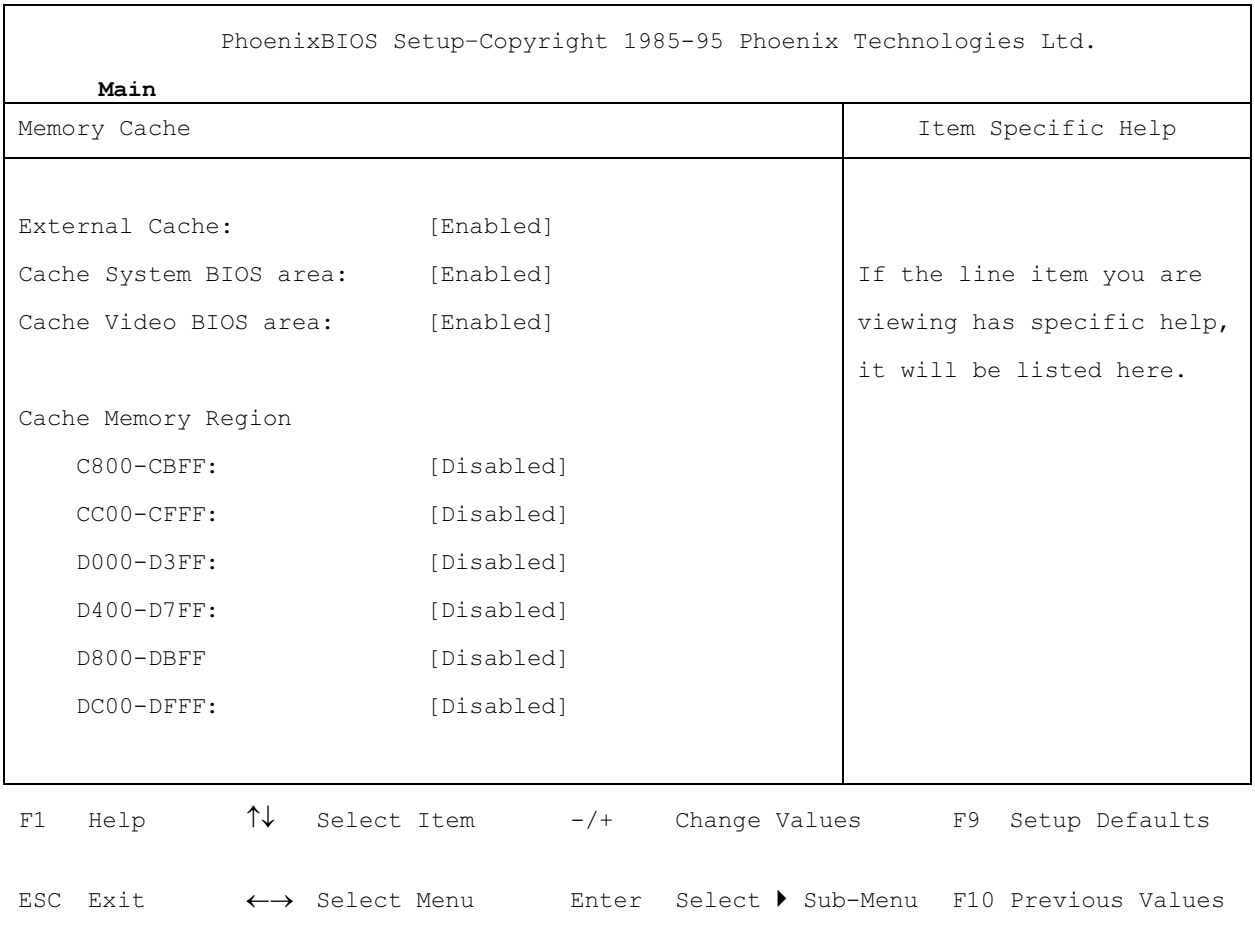


Figure Chapter 3 -3. Memory Cache Submenu

Option	Description
External Cache	Controls the state of external (COAST) cache memory. The system BIOS automatically disables external cache if it is not installed. The default is enabled.
Cache System BIOS Area	Allows the system BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled.
Cache Video BIOS Area	Allows the video BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled.
Cache Memory Region	Caches the corresponding memory when enabled. Memory in this area is usually extended BIOS or AT-bus memory. Enabling cache may increase system performance, depending on how the extended BIOS is accessed. The default is disabled.

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Memory Shadow Submenu

The summary screen displays the amount of shadow memory in use. Shadow memory is used to copy system and video BIOS into RAM to improve performance. The XVME-655 displays the number of Kbytes allocated to Shadow RAM on the summary screen. The System Shadow field, which is not editable, is for reference only.

The XVME-655 is shipped with the system BIOS and video BIOS shadowed.

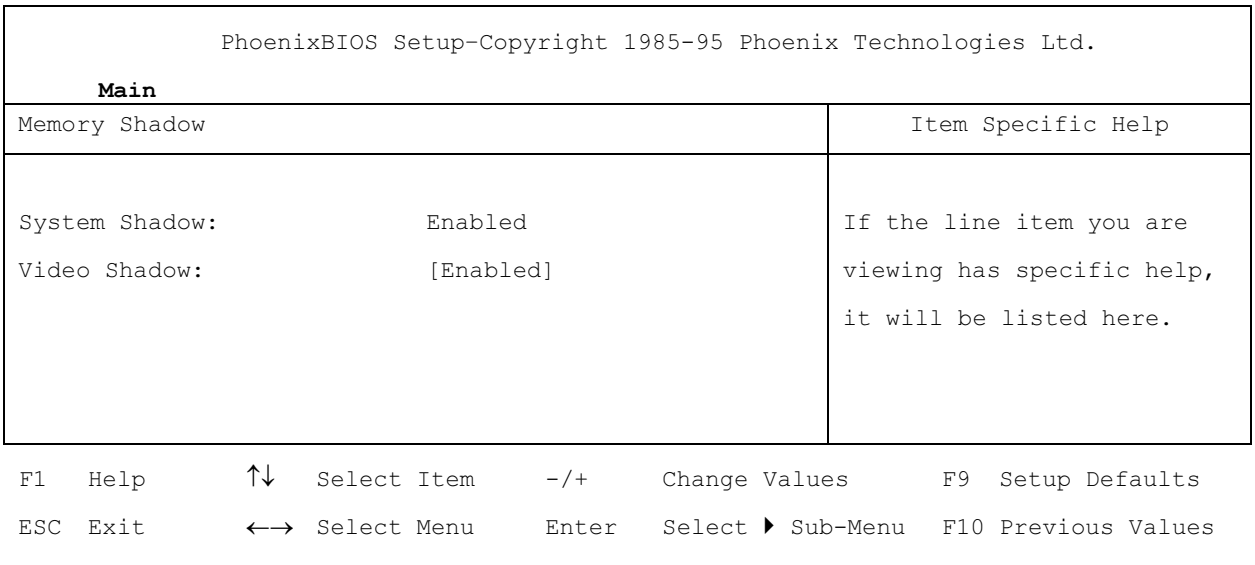


Figure Chapter 3 -4. Memory Shadow Submenu

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Boot Sequence Submenu

This menu lets you configure the boot sequence.

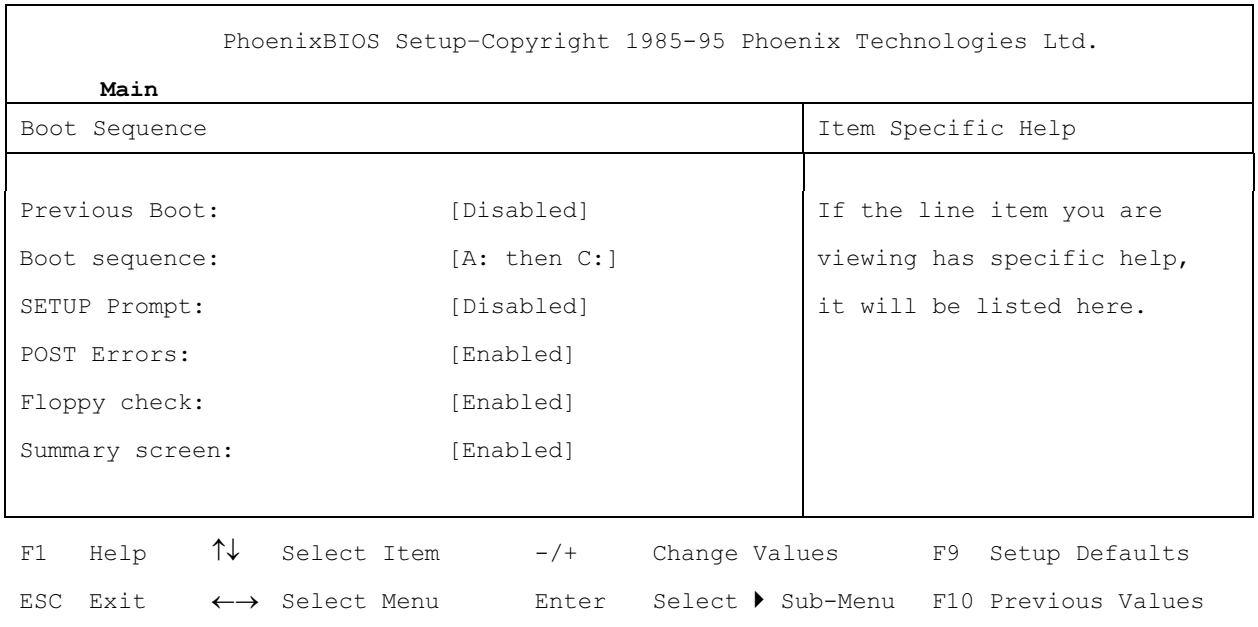


Figure Chapter 3 -5. Boot Sequence Submenu

Option	Description
Previous Boot	Detects if a boot sequence was not completed properly, if enabled. A power failure, reset during boot-up, or invalid CMOS configuration may cause an incomplete boot. If BIOS detects this, it displays the message "Previous boot incomplete - default configuration used." The system will be rebooted using the default configuration. If this option is disabled, the system BIOS does not detect an incomplete boot, and the system may not boot if CMOS settings are wrong. The default is disabled.
Boot Sequence	Attempts to load the operating system from the disk drives in the sequence selected here. The default is A: then C:
Setup Prompt	Displays the message, "Press <F2> to enter Setup," during boot up. The default is disabled.
POST Errors	Halts the system if it encounters a boot error when enabled, and will display "Press <F1> to resume, <F2> for Setup." The default is enabled.
Floppy Check	Seeks disk drives on the system during boot up if enabled. Disabling speeds boot time. The default is enabled.
Summary Screen	Displays the system summary screen during boot up when enabled. The default is enabled. This screen is a standard Phoenix BIOS screen and provides information on the following items: Processor Type Coprocessor Type BIOS Date System ROM Address System RAM Extended RAM Shadow RAM Cache RAM COM Ports LPT Ports Display Type Hard Disk 0 Hard Disk 1 Diskette A Diskette B

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Numlock Submenu

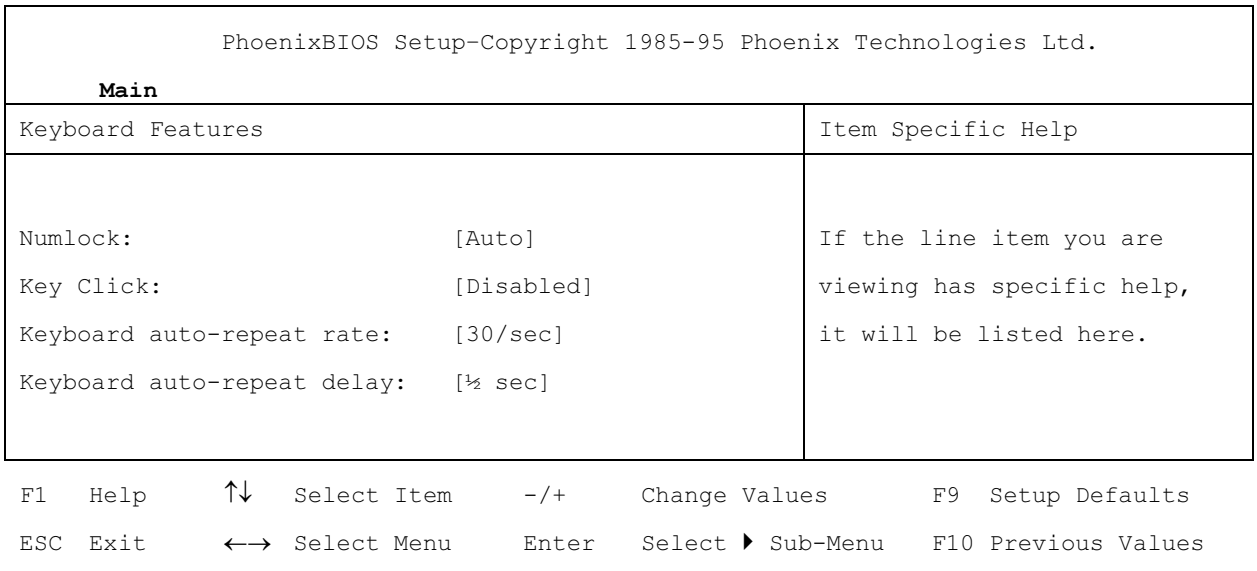


Figure Chapter 3 -6. Numlock Submenu

Option	Description
Numlock	Determines how BIOS defines the numlock key at power up or soft reset. Normally, BIOS sets the numlock (numeric keys selected) if it detects a 101- or 102-key keyboard at power up. If it detects an 84-key keyboard, it turns numlock off (cursor keys selected). Select Auto to keep this state; On to select numeric keys, regardless of keyboard; or Off to select cursor keys, regardless of keyboard. The default is Auto.
Keyboard click	Provides audible key-press feedback by causing a click through the system speaker every time a key is pressed, if enabled. This option is only valid for systems with a speaker connected to the speaker jack. The default is disabled.
Keyboard auto-repeat rate	Defines the rate at which the keyboard repeats while a key is pressed. The higher the number, the faster the key repeats. The default is 30 times per second.
Keyboard auto-repeat delay	Sets the number of times per second a key will repeat when it is held down. The default is a ½ second.

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Advanced Menu

Use this menu to change the peripheral control, advanced chipset control, and the disk access mode.

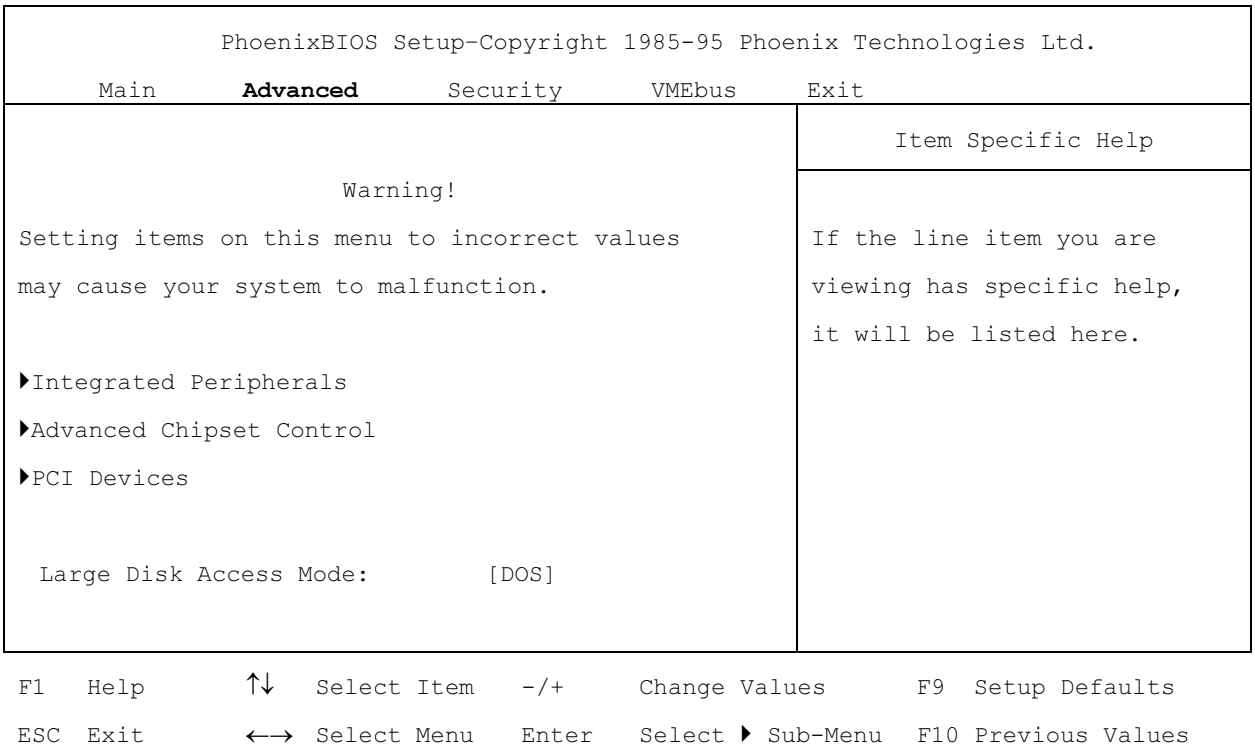


Figure Chapter 3 -7. Advanced Setup Menu

Feature	Description
Large Disk Mode	Select “DOS” if your system has DOS. Select “Other” if you have another operating system, such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.

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Integrated Peripherals Submenu

Use the Integrated Peripherals Submenu to configure the COM ports, parallel ports, and enable/disable the diskette and enhanced IDE controllers.

```
                PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
                     Advanced
Integrated Peripherals                                  Item Specific Help

COM port:                       [3F8, IRQ 4]            If the line item you are
COM port:                       [2F8, IRQ 3]            viewing has specific help,
LPT port:                       [378, IRQ 7]            it will be listed here.
LPT Mode:                       [Bi-Directional]
Diskette controller:            [Enabled]
Local Bus IDE Adapter:          [Enabled]

F1   Help      ↑↓  Select Item     -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→  Select Menu     Enter Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -8. Integrated Peripherals Submenu

Option	Description
COM Port	Allows the COM port address and IRQ levels to be modified or disabled.
LPT Port	Selects a unique address and interrupt request for the LPT port, or disables it. “Auto” selects the next available combination.
LPT Mode	Configures the LPT port for bi-directional or output only.
Diskette Controller	Enables or disables the on-board floppy disk controller.
Local Bus IDE Adapter	Enables or disables the local bus IDE adapter.

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Advanced Chipset Control Submenu

Use this submenu to change the values in the chipset registers and optimize your system's performance.

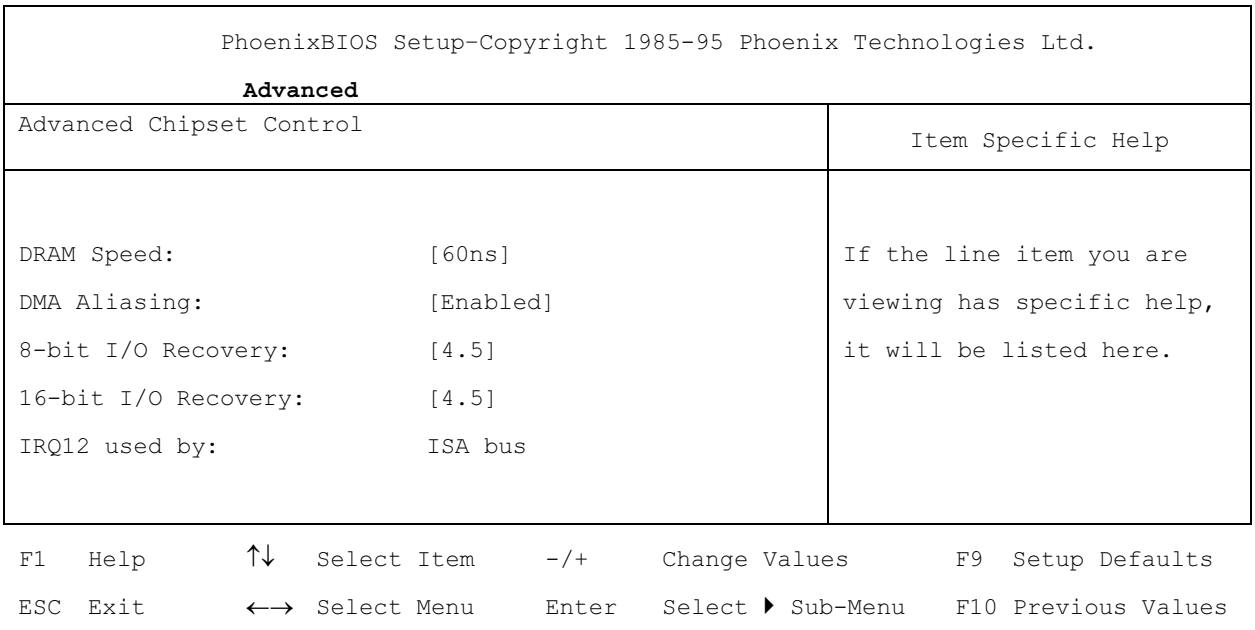


Figure Chapter 3 -9. Advanced Chipset Control Submenu

Option	Description
DRAM Speed	Indicates the speed of the SIMMs installed. This is used to configure the system for maximum performance.
DMA Aliasing	Disables DMA Aliasing if a device exists on the ISA bus that uses I/O ports 90h, 94h-96h, 98h, or 9Ch-9Eh.
8-bit I/O Recovery	Indicates the number of ISA clock cycles inserted between back-to-back I/O operations
16-bit I/O Recovery	Indicates the number of ISA clock cycles inserted between back-to-back I/O operations

Note

The options in this menu should be left in their default configurations.

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PCI Devices Submenu

PCI devices are peripheral devices designed for operation with a PCI bus. Use this submenu to configure the PCI bus and connected devices.

```
                PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
                     Advanced
PCI Devices                                          Item Specific Help

PCI Device, Slot #1:                                 If the line item you are
  Enable Master:              [Enabled]              viewing has specific help,
  Default Latency Timer:      [Yes]                  it will be listed here.
  Latency Timer:              [0040]
PCI Device, Slot #2:
  Enable Master:              [Enabled]
  Default Latency Timer:      [Yes]
  Latency Timer:              [0040]
PCI Device, Slot #3:
  Enable Master:              [Enabled]
  Default Latency Timer:      [Yes]
  Latency Timer:              [0040]
PCI Device, Slot #4:
  Enable Master:              [Enabled]
  Default Latency Timer:      [Yes]
  Latency Timer:              [0040]
PCI IRQ line 1:               [Auto Select]
PCI IRQ line 2:               [Auto Select]
PCI IRQ line 3:               [Auto Select]
PCI IRQ line 4:               [Auto Select]

F1   Help     ↑↓   Select Item      -/+   Change Values      F9  Setup Defaults
ESC  Exit     ←→   Select Menu      Enter Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -10. PCI Devices Submenu

> **Note**
>
> The options in this menu should be left in their default configurations.

Option	Description

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Option	Description
Enable Master	Enables the selected device as a PCI bus master.
Default Latency Timer	Controls PCI bus master time-out when set to “Yes,” which is the default. The default uses the minimum bus master clock rate.
Latency Timer	Displays the current value of the latency timer when the Default Latency Timer option is set to “No.”
PCI IRQ line 1-4	A PCI device cannot use IRQs already in use by ISA or EISA devices. Set this field to “Auto Select” only if no ISA or EISA legacy cards are installed. Other options are 3, 5, 9, 11, 12, 14, 15, or disabled.

Security Menu

This menu prompts you for the new system password and requires you to verify the password by entering it again.

Use a password to restrict access to the setup menus or prevent unauthorized booting of the unit. You can also use the supervisor password to change the user password.

```
            PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
     Main      Advanced      Security      VMEbus      Exit
                                                      Item Specific Help
Supervisor Password is     Disabled
User Password is           Disabled                   If the line item you are
Set Supervisor Password    [Press Enter]              viewing has specific help,
Set User Password          Press Enter                it will be listed here.

Password on boot:          [Disabled]

Diskette access:           [Supervisor]
Fixed disk boot sector:    [Normal]
System backup reminder:    [Disabled]
Virus check reminder:      [Disabled]

F1   Help     ↑↓  Select Item   -/+   Change Values      F9  Setup Defaults
ESC  Exit     ←→  Select Menu   Enter Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -11. Security Menu

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Option	Description
Supervisor Password	Provides full access to the BIOS setup menus. You may use up to seven alphanumeric characters. This option is disabled by setting it to [CR] or nothing.
Set User Password	Provides restricted access to BIOS setup menus. It requires prior setting of Supervisor password. You may use up to seven alphanumeric characters.
Password on Boot	If the supervisor password is set and this option is disabled, BIOS assumes the user is booting.
Diskette Access	Restricts the use of floppy drives to the supervisor. Requires setting the Supervisor password.
Fixed Disk Boot Sector	This is write protected to help prevent viruses.
System Backup Reminder/Virus Check Reminder	When enabled, displays a message during boot up asking (Y/N) if you have backed-up the system or scanned it for any viruses. The message returns on each boot until you respond with "Y." It displays the message daily on the first boot of the day; weekly on the first boot after Sunday; and monthly on the first boot of the month. The default is disabled.

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VMEbus Setup Menu

Use this menu and its submenus to configure the XVME-655's VMEbus master and slave interfaces, auxiliary NMIs, and VMEbus interrupt handler.

You can configure the following items:

- System controller
- Master interface
- Slave interface
- Interrupt signals

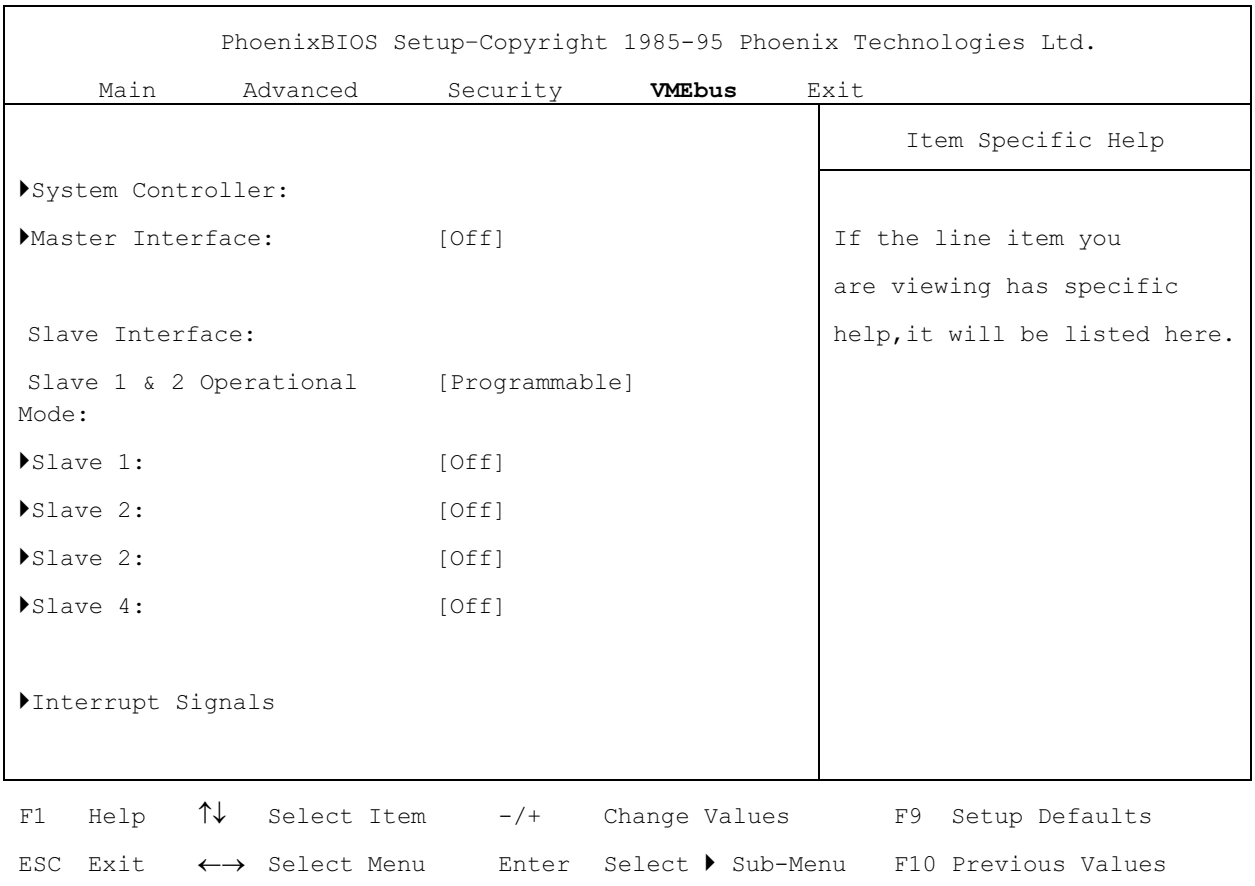


Figure Chapter 3 -12. VMEbus Setup Menu

Option	Description
Slave 1 & 2 Operational Mode	Selecting "Programmable" allows full choice in configuration of Slaves 1 and 2, as well as 3 and 4. Selecting "Compatible" configures VMEbus Slaves 1 and 2 like legacy XVME boards.

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System Controller Submenu

The XVME-655 automatically detects if the board is in the system controller position (the left-most slot of the VMEbus chassis). This condition controls whether system resources will be provided by the XVME-655 or another VMEbus processor. System resources are VMEbus Arbiter, BERR timeout, SYSCLK, and IACK daisy chain driver. These resources must be provided by the module installed in the system controller slot. You cannot change the field that reports the status of the XVME-655's system resources.

Note

The BERR timeout is the VMEbus error time

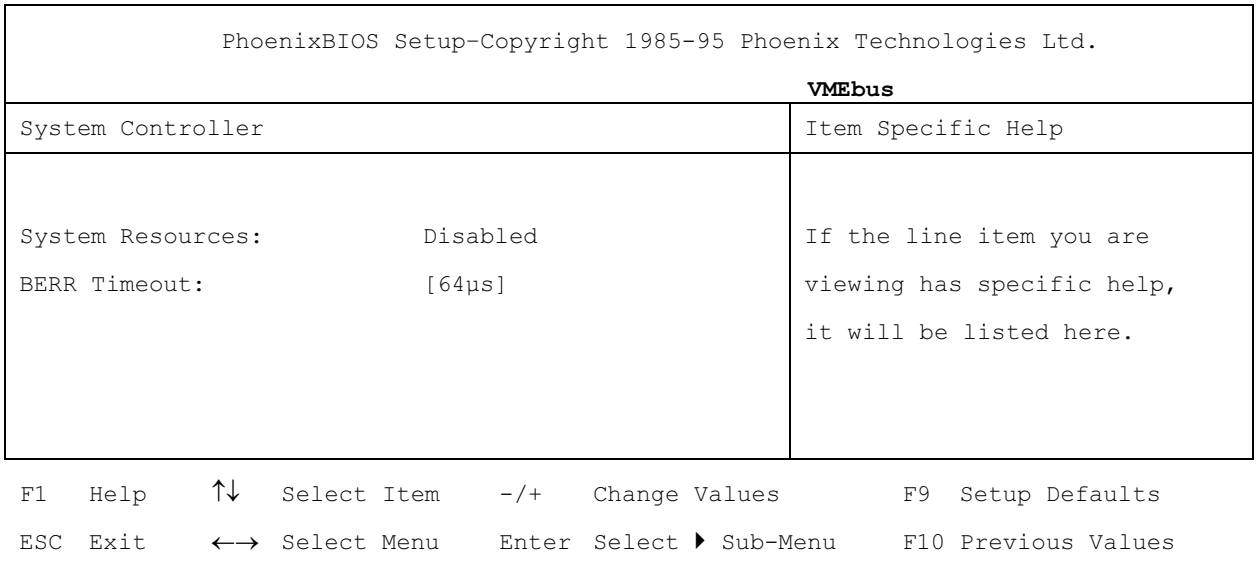


Figure Chapter 3 -13. System Controller Submenu

Option	Description
System Resources	Enables or disables system resources. This field is not user configurable; it is automatically detected by the board.
BERR Timeout	Sets the VMEbus error timeout. Choices are 16µs, 32µs, 64µs, 128µs, 256µs, 512µs, 1024µs, and Disabled. The default is 64µs.

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Master Interface Submenu

The VMEbus master setup allows configuration of the processor board's VMEbus master interface, auxiliary NMIs, and VMEbus interrupt handler.

> **Note**
>
> When the master interface setting is turned on, master image 0 is reserved for BIOS use. To avoid conflict, master images 1, 2, and 3 are available for use.

```
PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
                                                    VMEbus
Master Interface                                    Item Specific Help

Master Interface:          [Off]                    If the line item you are
                                                    viewing has specific help,
Address Modifier:          [Non-Privileged]         it will be listed here.
Request Level:             [Level 3]
Release Mode:              [When Done]

F1   Help    ↑↓  Select Item     -/+   Change Values      F9  Setup Defaults
ESC  Exit    ←→  Select Menu     Enter Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -14. Master Interface Submenu

Option	Description
Master Interface	Turns the master interface "On" or "Off." The default is "Off."
Address Modifier	Allows the choice of "Non-Privileged" or "Supervisory" accesses for VME master cycles. The access mode selection controls the AM2 signal on the VMEbus when the XVME-655 performs VMEbus accesses.
Request Level	Sets the bus request level when requesting use of the VMEbus to Level 0, Level 1, Level 2, or Level 3. The default is Level 3.
Release Mode	Sets the bus release mode to use when controlling the VMEbus. The default is "When Done."

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Slave Interface Submenus

Use this submenu to configure the processor board's VMEbus slave interface.

> **Note**
>
> When the Slave 1 & 2 Operational Mode Setting is set to "Compatible," slave images 0 and 1 are reserved for BIOS use.

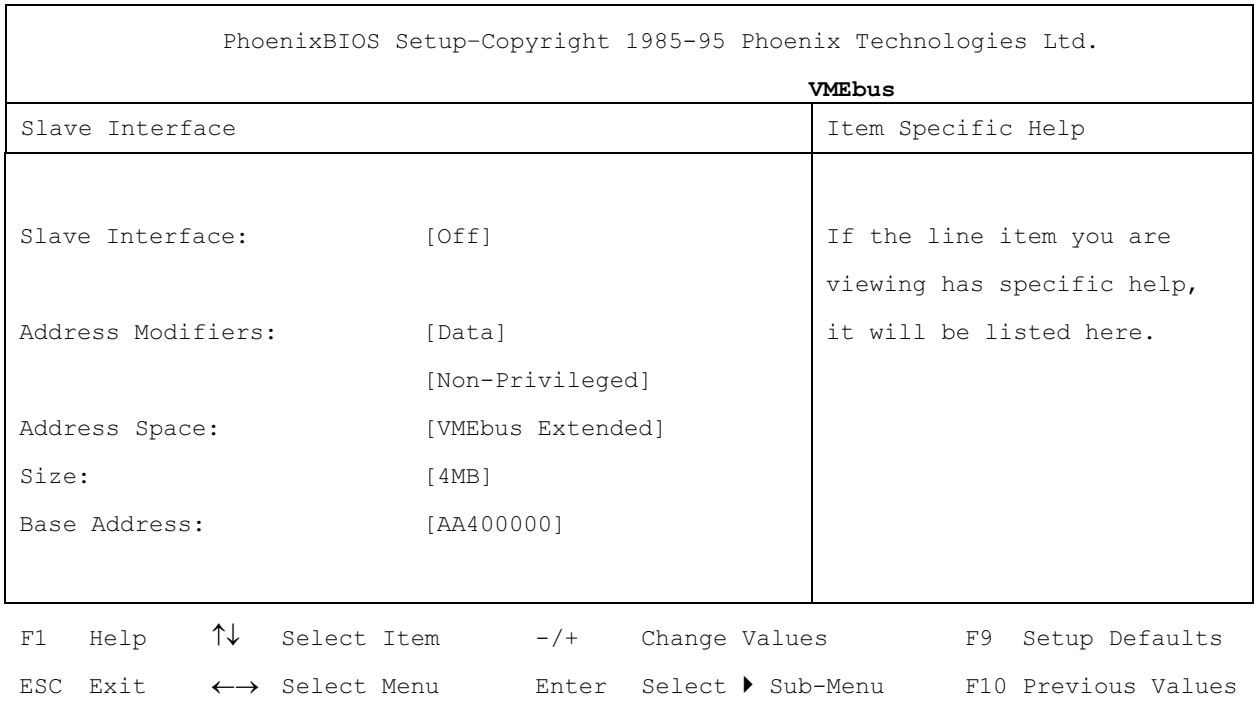


Figure Chapter 3 -15. Slave Interface Submenu

Option	Description
Slave Interface	Turns the slave interface "On" or "Off." The default is "Off." When turned off, other VME masters cannot access memory on the XVME-655.
Address Modifiers	Determines which type of VMEbus slave accesses are permitted to read or write to the XVME-655 dual-access DRAM. The first field determines whether the slave interface responds to data accesses only, or to both program and data accesses. The default is "Data." The second field determines whether the slave interface responds to supervisory accesses only, or to both supervisory and non-privileged accesses. The default is "Non-Privileged."
Address Space	Determines if VME masters access the slave's dual-access memory in the VMEbus Standard (A24) or VMEbus Extended (A32) address space. The default is "VMEbus extended."

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Option	Description
Slave Memory Size	Determines the amount of dual-access memory that is available to external VMEbus maters when the Slave Address Space option is set to “Extended.” If the Slave Address Space option is set to “Standard,” the slave memory size is fixed at 4 Mbytes. The slave memory size cannot be more than the total memory size. The default is 4 Mbytes.
Slave Address	Sets the VMEbus address of the XVME-655 dual-access RAM. When the Slave Address Space option is set to VMEbus Standard (A24), the dual-access memory must be located on a 4-Mbyte boundary and the upper two hexadecimal digits of the slave address are ignored. When the Slave Address Space option is set to VMEbus Extended (A32), the slave address must be a multiple of the slave memory size. The default is “AA4.”

Interrupt Signals Submenu

Use this submenu configure the processor board’s VMEbus interrupt signals.

```
        PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
                                                              VMEbus
Interrupt Signals                                  Item Specific Help

VMEbus ACFAIL ANMI:          [Disabled]            If the line item you are
VMEbus SYSFAIL ANMI:         [Disabled]            viewing has specific help,
VMEbus BERR ANMI:            [Disabled]            it will be listed here.

VMEbus IRQ1:                 [Disabled]
VMEbus IRQ2:                 [Disabled]
VMEbus IRQ3:                 [Disabled]
VMEbus IRQ4:                 [Disabled]
VMEbus IRQ5:                 [Disabled]
VMEbus IRQ6:                 [Disabled]
VMEbus IRQ7:                 [Disabled]

F1    Help  ↑↓  Select Item    -/+   Change Values      F9    Setup Defaults
ESC   Exit  ←→  Select Menu    Enter Select ▶ Sub-Menu  F10   Previous Values
```

Figure Chapter 3 -17. Interrupt Signals Menu

Option	Description
VMEbus ACFAIL ANMI	Determines whether the auxiliary non-maskable interrupt (ANMI) is enabled on power-up for a power failure. The default is “Disabled.”
VMEbus SYSFAIL ANMI	Determines whether the auxiliary non-maskable interrupt (ANMI) is enabled on power-up for a system failure. The default is “Disabled.”

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VMEbus BERR ANMI	Determines whether the auxiliary non-maskable interrupt (ANMI) is enabled on power-up for a VMEbus error. The default is “Disabled.”
VMEbus IRQ1-IRQ7	Determines which of the VMEbus auxiliary maskable interrupt (AMI) levels (1-7) can be received by the XVME-655. Each interrupt level can be enabled or disabled individually. All are disabled by default.

Exit Menu

This menu prompts you to exit setup.

```
        PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
   Main      Advanced      Security      VMEbus      Exit
                                                  Item Specific Help
Save Changes & Exit
Exit without Saving Changes                       If the item you are viewing
Get Default Values                                has specific help, it will
Load Previous Values                              be listed here.
Save Changes

F1  Help      ↑↓  Select Item   -/+   Change Values      F9  Setup Defaults
ESC Exit      ←→  Select Menu   Enter Select ▶ Sub-Menu  F10 Previous Values
```

Figure Chapter 3 -16. Exit Menu

Option	Description
Save Changes & Exit	Saves in battery-backed CMOS the selections displayed in the menus. After you save your selections, the program displays this message: “Values have been saved.” “[Continue]” If you attempt to exit without saving, the program asks if you want to save before exiting. The next time you boot your computer, the BIOS configures your system according to the setup selections stored in CMOS. If those values cause the system boot to fail, reboot and press F2 to enter the BIOS setup menus. In these menus, you can set the default values (as described below) or change the selections that caused the boot to fail.
Exit Without Saving Changes	Exit the BIOS setup menus without storing any changes you may have made. The selections previously in effect remain in effect.

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Option	Description
Get Default Values	Sets all fields in the BIOS setup menus to their default values. The program displays this message: "Default values have been loaded." "[Continue]" During boot up, if the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages: "System CMOS checksum bad - run SETUP" "Press <F1> to resume, <F2> to Setup" This means the CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Press F1 to resume the boot (this causes the system to be configured using the default values) or F2 to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.
Load Previous Values	Restores the values you previously saved to CMOS if you change your mind about changes you have made and have not yet saved. The following message will then display: "Previous values have been loaded." "[Continue]"
Save Changes	Saves all your changes without exiting the BIOS setup menus. You can return to the other menus if you want to review and change your selections.

BIOS Compatibility

This BIOS is IBM PC/AT compatible with additional CMOS RAM and BIOS data areas used.

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Chapter 4 – Programming

Memory Map

Table Chapter 4 -1 illustrates the XVME-655's memory map.

Table Chapter 4 -1. XVME-655 Memory Map

Address Range	Size	Usage
FFFB0000-FFFFFFFF	256 Kbytes	System BIOS
04000000-FEFFFFFF		Allocated to PCI bus by BIOS or operating system
00100000-007FFFFF 00100000-00FFFFFF 00100000-01FFFFFF 00100000-03FFFFFF	8 Mbytes 16 Mbytes 32 Mbytes 64 Mbytes	System DRAM
000F0000-000FFFFF	64 Kbytes	System BIOS
000E0000-000EFFFF	64 Kbytes	System BIOS or real mode window or I/O channel memory
00D0000-00DFFFF	64 Kbytes	Real mode window or I/O channel memory or on-board BIOS
000C8000-000CFFFF	32 Kbytes	I/O channel memory or on-board BIOS
000C0000-000C7FFF	32 Kbytes	Video BIOS
000A0000-000BFFFF	128 Kbytes	VGA DRAM memory
00000000-0009FFFF	640 Kbytes	System DRAM

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I/O Map

Table Chapter 4 -2 illustrates the XVME-655's I/O map.

Table Chapter 4 -2. I/O Map

Address Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller, 8259 equivalent
022-023	Available
025-02F	Interrupt controller 1, 8259 equivalent
040-05F	Timer, 8254-2 equivalent
060-06F	Keyboard, 8742 equivalent
070-07F	Real-time clock, bit 7 NMI mask
080-091	DMA page register
93-9F	DMA page register
0A0-0BF	Interrupt controller 2, 8259 equivalent
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0F0	N/A
0F1	N/A
0F2-0FF	N/A
100	Available
102	Available
103-1EF	Available
1F0-1F7	IDE controller (AT drive)
218	Xycom Temp/Abort port
219	Xycom LED/BIOS port
278-27F	Alternate parallel port
280-2F7	Available
2F8-2FF	Serial port 2
300-36F	Available
370-377	Alternate floppy disk controller
378-37F	Parallel port 1
380-3BF	Available
3C0-3DF	VGA/EGA
3E0-3EF	Available
3F0-3F7	Primary floppy disk controller
3F8-3FF	Serial port 1
4D0	ELCR1 edge- or level-triggered interrupt
4D1	ELCR2 edge- or level-triggered interrupt
CF8	PCI configuration address register
CF9	Reset control register
CFC	PCI configuration data register

Note

Serial and parallel port addresses are controlled in the BIOS setup menus. Changing the setting will change the I/O location.

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IRQ Map

Table Chapter 4 -3 describes the AT-bus IRQ map.

Table Chapter 4 -3. AT-bus IRQ Map

Interrupt	Description
IRQ0	System timer tick
IRQ1	Keyboard
IRQ2	Reserved
IRQ3	COM2
IRQ4	COM1
IRQ5	Available
IRQ6	Floppy drive
IRQ7	Parallel port
IRQ8	Real-time clock
IRQ9	Cascade
IRQ10	Abort switch
IRQ11	Available
IRQ12	Available
IRQ13	Reserved (387)
IRQ14	Fixed disk
IRQ15	Available

Note

COM1, COM2, and parallel port IRQs are available if software does not use the ports or does not use the interrupt.

Note

PCI IRQs need to be mapped to an AT-bus IRQ. This is done through the BIOS setup. Refer to Chapter 3 for more information.

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VME Interface

The VME interface consists of the Universe chip, which is a PCI bus-to-VMEbus interface. The XVME-655 is a 32-bit PCI interface and a 32-/64-bit VMEbus interface. The Universe chip configuration registers are located in a 64 Kbyte block of PCI memory space. This memory location is programmable and defined by PCI configuration cycles. The Universe configuration register space should be set up using PCI interrupt calls provided by the BIOS.

For information on accessing the PCI bus, refer to the *PCI BIOS Functions* section later in this chapter.

Caution

The Universe manual states that the Universe Control and Status Registers (UCSR) occupy 4 Kbytes of internal memory. While this is true, the Universe controller decodes the entire 64 Kbyte region and shadows the 4 Kbytes 16 times.

Note

PCI memory slave access = VMEbus master access

PCI memory master access = VMEbus slave access

System Resources

The XVME-655 automatically detects slot 1 system resource functions. The system resource functions are explained in the Universe manual.

VMEbus Master Interface

The XVME-655 can be a VMEbus master by accessing a PCI slave channel or by the DMA channel initiating a transaction. The Universe chip contains four PCI slave images. The first slave image has a 4 Kbyte resolution; the others have a 64 Kbyte resolution. The VMEbus master can generate A16, A24, A32 VMEbus cycles for each PCI slave image.

The address mode and type are programmed on a PCI slave image basis. The PCI memory address location for the VMEbus master cycle is specified by the Base and Bound address. The VME address is calculated by adding the Base address to the Translation Offset address. All PCI slave images are located in the PCI bus memory space.

All VMEbus master cycles are byte-swapped to maintain address coherency.

Caution

If you want to use the XVME-655 as a VMEbus master and slave, the VMEbus master cycles must acquire the VMEbus prior to accessing the

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PCI slave image. The chipset will not give up the PCI bus when there are posted writes to the VMEbus. This condition causes a deadlock. The MAST_CTL register contains VOWN and VOWN_ACK, which you can use to obtain the VMEbus.

Caution

PCI slave images mapped to a system DRAM area will access the system DRAM, not the PCI slave image. Also, the Universe configuration register has a higher priority than the PCI slave images. As a result, if the PCI slave image and the Universe configuration registers are mapped into the same memory area, the configuration registers will take precedence.

VMEbus Slave Interface

The XVME-655 can be a VMEbus slave by accessing a VMEbus slave image or by the DMA channel initiating a transaction. There are four PCI slave images. The first slave image has a 4 Kbyte resolution; the others have a 64 Kbyte resolution. The slave can respond to A16, A24, A32 VMEbus cycles for each VMEbus slave image.

The address mode and type are programmed on a VMEbus slave image basis. The VMEbus memory address location for the VMEbus slave cycle is specified by the Base and Bound address. The PCI address is calculated by adding the Base address to the Translation offset address.

The XVME-655 DRAM memory is based on the PC/AT architecture and is not contiguous. The VMEbus slave images may be set up to allow this DRAM to appear as one contiguous block.

The first VMEbus slave image must have the Base and Bound register set to 640 Kbytes. For example:

VMEbus Slave Image 0 BS= 0000000h BD= A0000h TO = 0000000h

The second VMEbus slave image must have the Base register set to be contiguous with the Bound register from the first VMEbus Slave image. The Bound register is limited by the total XVME-655 DRAM. The Translation Offset register is offset by 384 Kbytes, which is equivalent to the A0000h-FFFFFh range on the XVME-655 board.

For example:

VMEbus Slave Image 1 BS=A0000h BD= 400000h TO = 060000h

Mapping defined by the PC/AT architecture can be overcome if the VMEbus Slave image window is always configured with a 1 Mbyte Translation Offset. From a user and software standpoint, this is desirable because the interrupt vector table, system parameters, and communication buffers (keyboard) are placed in low DRAM. This provides more system protection.

Caution

When setting up slave images, the address and other parameters should be set first. Only after the VMEbus slave image is set up correctly

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should the VMEbus slave image be enabled. If a slave image is going to be remapped, disable the slave image first, and then reset the address. After the image is configured correctly, re-enable the image.

The VMEbus slave cycle becomes a master cycle on the PCI bus. The PCI bus arbiter is the TSC chip. It arbitrates between the various PCI masters, the Pentium CPU, and the Local bus IDE bus mastering controller. Because the VMEbus cannot be retried, all VMEbus slave cycles must be allowed to be processed. This becomes a problem when a Pentium cycle to a PCI slave image is in progress while a VMEbus slave cycle to the onboard DRAM is in progress. The Pentium cycle will not give up the PCI bus and the VMEbus slave cycle will not give up the VMEbus, causing the XVME-655 to become deadlocked. If the XVME-655 is to be used as a master and a slave at the same time, the VMEbus master cycles must obtain the VMEbus prior to initiating VMEbus cycles.

All VMEbus slave interface cycles are byte-swapped to maintain address coherency.

VMEbus Interrupt Handling

The XVME-655 can service IRQ[7:1]. A register in the Universe chip enables the interrupt levels that will be serviced by the XVME-655. When a VMEbus IRQ is asserted, the Universe requests the VMEbus and generates an IACK cycle. Once the IACK cycle is complete, a PCI bus interrupt is generated to allow the proper Interrupt Service Routine (ISR) to be executed. The Universe connects to all four PCI bus interrupts. These interrupts may be shared by other PCI bus devices. The BIOS maps the PCI bus interrupts to the AT-bus interrupt controllers. AT-bus interrupts must be uniquely mapped to each device.

Because the PCI devices share interrupt lines, all ISR routines must be prepared to chain the interrupt vector to allow the other devices to be serviced.

Note

All PCI bus interrupts can be mapped to one AT-bus interrupt. For example, in the BIOS setup menu, you can map PCI IRQ(0) to INT11.

Caution

IRQ10 is defined for the Abort toggle switch.

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VMEbus Interrupt Generation

The XVME-655 can generate VMEbus interrupts on all seven levels. There is a unique STATUS/ID associated with each level. Upper bits are programmed in the STATUS/ID register. The lowest bit is cleared if the source of the interrupt is a software interrupt, and set for all other interrupt sources. Consult the Universe User's Manual for a more in-depth explanation.

VMEbus Reset Options

The XVME-655 resets the VMEbus according to the following conditions:

1. Power on always causes the Universe chip to assert the VMEbus reset signal.
2. The Universe chip may reset the VMEbus by asserting a software bit.
3. The Toggle reset switch can reset the VMEbus when SW1-position 2 is closed.

Note

If SW1-position 1 is closed, the entire XVME-655 is reset.

You can also use the XVME-655 toggle switch to reset only the local XVME-655.

Note

SW1-position 2 must be open. SW1-position 5 must be closed.

PCI BIOS Functions

Special PCI BIOS functions provide a software interface to the Universe chip, providing the PCI-to-VMEbus interface. You can invoke these PCI BIOS functions using a function and subfunction code. You set up the host processor's registers for the function and subfunction desired and call the PCI BIOS software. The PCI BIOS function code is B1h. Status is returned using the Carry flag ([CF]) and registers specific to the subfunction invoked.

Interrupt 1Ah provides access to the PCI BIOS special functions for 16-bit callers. Calling through a 32-bit protect mode entry point provides 32-bit (i.e., protect mode) access.

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Calling Conventions

The PCI BIOS functions preserve all registers and flags except those used for return parameters. The Carry Flag [CF] will be altered as shown to indicate completion status. The calling routine will be returned to with the interrupt flag unmodified and interrupts will not be enabled during function execution. These routines, which are re-entrant, require 1024 bytes of stack space and the stack segment must be the same size (i.e., 16 or 32 bit) as the code segment.

The PCI BIOS provides a 16-bit real and protect mode interface and a 32-bit protect mode interface.

16-Bit Interface

The Int 1Ah software interrupt provides the 16-bit interface. The PCI BIOS Int 1Ah interface operates in either real mode, virtual-86 mode, or 16:16 protect mode. The Int 1Ah entry point supports 16-bit code only.

32-Bit Interface

The protected mode interface supports 32-bit protect mode callers. You can access the protected mode PCI BIOS interface by calling through a protected mode entry point in the PCI BIOS. The BIOS32 Service Directory provides the entry point and information needed for building the segment descriptors. Thirty-two-bit callers invoke the PCI BIOS routines using CALL FAR.

The BIOS32 Service Directory is implemented in the BIOS in a contiguous 16-byte data structure, beginning on a 16-byte boundary somewhere in the physical address range 0E00000h-0FFFFFh. The address range should be scanned for the following valid, checksummed data structure containing the following fields:

Offset	Size	Description
0	4 bytes	Signature string in ASCII. The string is “_32_”. This puts an “underscore” at offset 0, a “3” at offset 1, a “2” at offset 2, and another “underscore” at offset 3.
4	4 bytes	Entry point for the BIOS32 Service Directory. This is a 32-bit physical address.
8	1 byte	Revision level.
9	1 byte	Length of the data structure in 16-byte increments. (This data structure is 16 bytes long, so this field contains 01h.)
0Ah	1 byte	Checksum. This field is the checksum of the complete data structure. The sum of all bytes must add up to 0.
0Bh	5 bytes	Reserved. Must be zero.

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You can access the BIOS32 Service Directory by doing a FAR CALL to the entry point obtained from the Service data structure. However, you must meet several requirements about the calling environment. You must set the CS code segment selector and the DS data segment selector to encompass the physical page holding the entry point, as well as the immediately following physical page. They must also have the same base. The SS stack segment selector must be 32-bit and provide at least 1 Kbyte of stack space. The calling environment must also allow access to I/O space.

The BIOS32 Service Directory provides a single function call to locate the PCI BIOS service. All parameters to the function are passed in registers. Parameter descriptions are provided below. Three values are returned by the call. The first is the base physical address of the PCI BIOS service; the second is the length of the service; and the third is the entry point to the service encoded as an offset from the base. The first and second values can be used to build the code segment selector and data segment selector for accessing the service.

ENTRY:

[EAX] Service Identifier = “$PCI” (049435024h)

[EBX] Set to Zero

EXIT:

[AL] Return Code:

00h = Successful

80h = Service Identifier not found

81h = Invalid value in [BL]

[EBX] Physical address of the base of the PCI BIOS service

[ECX] Length of the PCI BIOS service

[EDX] Entry point into the PCI BIOS Service. This is an offset from the base provided in [EBX].

PCI BIOS Function Calls

Use the available function calls to identify the location of resources and to access configuration space of the VMEbus interface. Special functions allow the reading and writing of individual bytes, words, and dwords in the configuration space.

You must invoke PCI BIOS routines (for both 16- and 32-bit callers) with appropriate privilege so that interrupts can be enabled/disabled and the routines can access I/O space.

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Locating the Universe Chip

This function returns the location (bus number) of the Universe chip providing the PCI interface to the VMEbus.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 02h

[CX] Device ID = 0

[DX] Vendor ID = 10E3h

[SI] Index = 0

EXIT:

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[AH] Return Code:
00h = Successful
86h = Device not found
83h = Bad Vendor ID

[CF] Completion Status, set = error, reset = success

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Read Configuration Byte

This function reads individual bytes from the configuration space of the VMEbus interface.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 08h

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0...255)

EXIT:

[CL] Byte Read

[AH] Return Code:
00h = Successful
87h = Bad Register Number

[CF] Completion Status, set = error, reset = success

Read Configuration Word

This function reads individual words from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of two (i.e., bit 0 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

[AL] BIOS_SUBFUNCTION_ID = 09h

[BH] Bus Number (0-255)

[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits

[DI] Register Number (0, 2, 4, ...254)

EXIT:

[CL] Word Read

[AH] Return Code:
00h = Successful
87h = Bad Register Number

[CF] Completion Status, set = error, reset = success

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Read Configuration Dword

This function reads individual dwords from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of four (i.e., bits 0 and 1 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h
[AL] BIOS_SUBFUNCTION_ID = 0Ah
[BH] Bus Number (0-255)
[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits
[DI] Register Number (0, 4, 8, ...252)

EXIT:

[ECX] Word Read
[AH] Return Code:
00h = Successful
87h = Bad Register Number
[CF] Completion Status, set = error, reset = success

Write Configuration Byte

This function writes individual bytes from the configuration space of the VMEbus interface.

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h
[AL] BIOS_SUBFUNCTION_ID = 0Bh
[BH] Bus Number (0-255)
[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits
[DI] Register Number (0...255)
[CL] Byte Value to Write

EXIT:

[AH] Return Code:
00h = Successful
87h = Bad Register Number
[CF] Completion Status, set = error, reset = success

Write Configuration Word

This function writes individual words from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of two (i.e., bit 0 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h

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[AL] BIOS_SUBFUNCTION_ID = 0Ch
[BH] Bus Number (0-255)
[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits
[DI] Register Number (0, 2, 4, ...254)
[CX] Word Value to Write

EXIT:

[AH] Return Code:
00h = Successful
87h = Bad Register Number
[CF] Completion Status, set = error, reset = success

Write Configuration Dword

This function writes individual dwords from the configuration space of the VMEbus interface. The Register Number parameter must be a multiple of four (i.e., bits 0 and 1 must be set to 0).

ENTRY:

[AH] BIOS_FUNCTION_ID = B1h
[AL] BIOS_SUBFUNCTION_ID = 0Dh
[BH] Bus Number (0-255)
[BL] Device Number in upper 5 bits
Function Number is bottom 3 bits
[DI] Register Number (0, 4, 8, ...252)
[ECX] Dword Value to Write

EXIT:

[AH] Return Code:
00h = Successful
87h = Bad Register Number
[CF] Completion Status, set = error, reset = success

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Chapter 5 – XVME-978 PCI Ethernet Controller Module

A high-performance 32-bit PCI bus mastering Ethernet controller may be added to the XVME-655 via the XVME-978 Ethernet Controller. The XVME-978 features a NE2100 and NE1500 software-compatible Ethernet interface with support for both 10BaseT and 10Base2 connections. The XVME-978 is designed to mate with the two interboard connectors. It also provides a second set of connectors to allow the installation of an XVME-976 which offers PMC and PC/104 sites.

Architectural Block Diagram

Figure Chapter 5 -1 illustrates the XVME-978 block diagram.

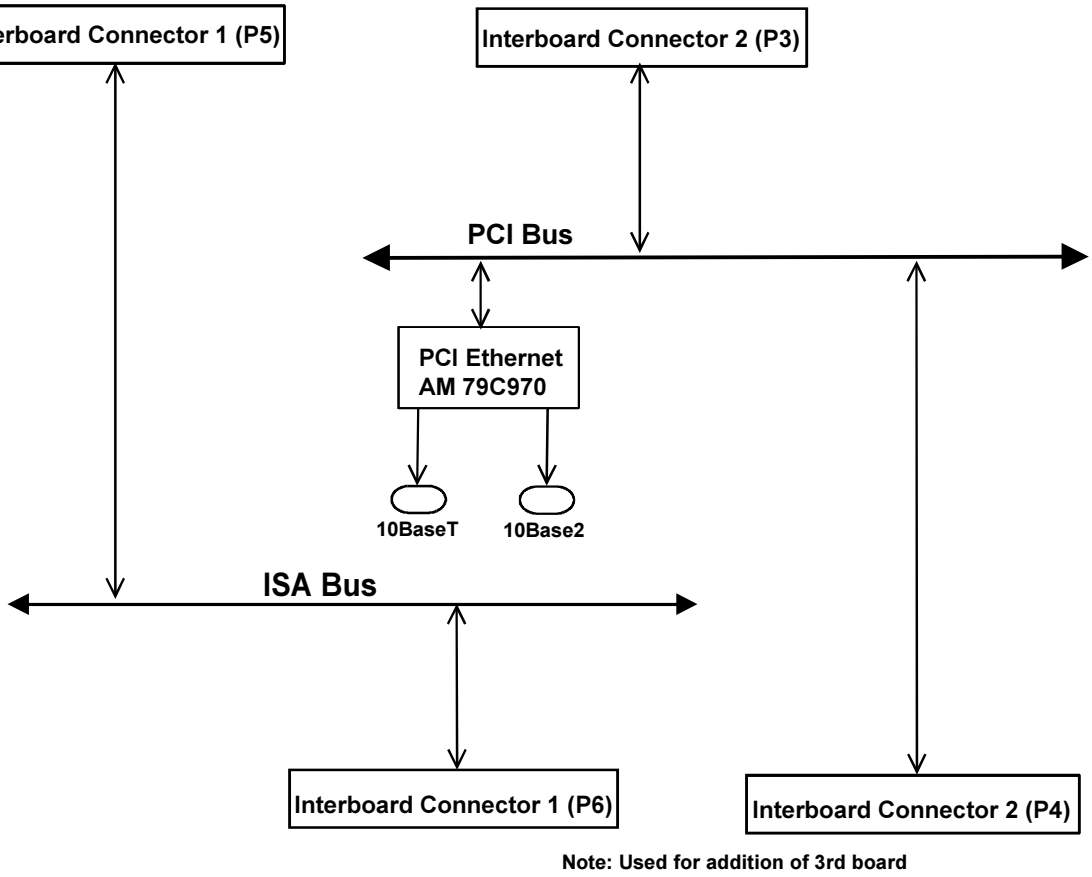


Figure Chapter 5 -1. XVME-978 Block Diagram

Installation

Figure Chapter 5 -2 illustrates how the XVME-978 module connects to the XVME-655 processor module.

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Figure Chapter 5 -2. XVME-978 Installation

The following steps illustrate how to install the XVME-978 on the XVME-655 board. As you are reading the directions, reference Figure Chapter 5 -2.

Warning

Never install or remove any boards before turning off the power to the bus and all related external power supplies.

1. Disconnect the AC power going to the VMEbus chassis.
2. If the XVME-655 has been inserted in the backplane, remove it before mounting the XVME-978.
3. Remove the XVME-655 front panel filler plate.
4. Position the XVME-978 Ethernet connectors so they fit through the opening on the XVME-655 front panel. This can be accomplished by tilting the right side (the side closest to the VMEbus connector) of the XVME-978 up until the Ethernet connectors fit into the opening.

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5. While still tilting the right side of the XVME-978 up, align the keying pins on the 80-pin interboard connector closest to the XVME-655 front panel.
6. Once the keying pins are aligned, lower the right side of the XVME-978 onto the 80-pin connectors on the XVME-655. Apply gentle pressure until the XVME-978 is properly seated onto the XVME-655.
7. Once the XVME-978 is properly seated, affix the front panel filler plate provided with the XVME-978 by snapping it into the opening. Make sure the holes for the Ethernet connectors line up.
8. Secure the XVME-978 to the XVME-655 using the screws and standoffs.

Caution

Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect, remove the module and inspect all connectors for possible damage or obstructions.

9. Install the XVME-655. Refer to the instructions in Chapter 2.

Pinouts

The XVME-978 connects to two 80-pin interboard connectors.

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Interboard Connector 1 (P6)

Table Chapter 5 -1 indicates the pinout for interboard connector 1. This connector has one eight-bit DMA channel and two 16-bit DMA channels.

Note

Interboard connector 1 does not support the following signals: MASTER*, 0WS*, DRQ0, DACK0*, DRQ3, DACK3*, DRQ7, and DACK7*.

Table Chapter 5 -1. Interboard Connector 1 Pinout

Pin	Signal	Pin	Signal
1	SYSCLK	41	SA10
2	OSC	42	SA11
3	SD(15)	43	SA12
4	SD(14)	44	SA13
5	SD(13)	45	SA14
6	SD(12)	46	SA15
7	SD(11)	47	SA16
8	SD(10)	48	SA17
9	SD(9)	49	SA18
10	SD(8)	50	SA19
11	MEMW*	51	BALE
12	MEMR*	52	TC
13	DRQ5	53	DACK2*
14	DACK5*	54	IRQ3
15	DRQ6	55	IRQ4
16	DACK6*	56	SBHE*
17	LA17	57	IRQ5
18	LA18	58	IRQ6
19	LA19	59	IRQ7
20	LA20	60	REF*
21	LA21	61	DRQ1
22	LA22	62	DACK1*
23	LA23	63	RESETDRV
24	IRQ14	64	IOW*
25	IRQ15	65	IOR*
26	IRQ12	66	SMEMW*
27	IRQ11	67	AEN
28	IRQ10	68	SMEMR*
29	IOCS16*	69	IOCHRDY
30	MEMCS16*	70	SD(0)
31	SA0	71	SD(1)
32	SA1	72	SD(2)
33	SA2	73	SD(3)
34	SA3	74	SD(4)
35	SA4	75	SD(5)
36	SA5	76	SD(6)
37	SA6	77	SD(7)
38	SA7	78	DRQ2
39	SA8	79	IRQ9

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Pin	Signal	Pin	Signal
40	SA9	80	IOCHCK*

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Interboard Connector 2 (P4)

Table Chapter 5 -2 details the pinout for interboard connector 2.

Table Chapter 5 -2. Interboard Connector 2 Pinout

Pin	Signal	Pin	Signal
1	TCLK	41	AD(23)
2	TRST*	42	AD(22)
3	TMS	43	AD(21)
4	TDO	44	AD(20)
5	TDI	45	AD(19)
6	PCI-RSVD9A (pn2-8)	46	AD(18)
7	PCI-RSVD10B (pn2-9)	47	AD(17)
8	PCI-RSVD11A (pn2-10)	48	AD(16)
9	PCI-RSVD14A (pn1-12)	49	BE2*
10	PCI-RSVD14B (pn1-10)	50	FRAME*
11	PCI-RSVD19A (pn2-17)	51	IRDY*
12	PMC-RSVD (pn2-34)	52	TRDY*
13	PMC-RSVD (pn2-52)	53	DEVSEL*
14	PMC-RSVD (pn2-54)	54	STOP*
15	PCICLK3 (NC)	55	PLOCK*
16	PIRQA*	56	PERR*
17	PIRQB*	57	SDONE
18	PIRQC*	58	SBO*
19	PIRQD*	59	SERR*
20	REQ3*	60	PAR
21	PCICLK2 (NC)	61	BE1*
22	REQ1*	62	AD(15)
23	GNT3*	63	AD(14)
24	PCICLK1	64	AD(13)
25	GNT1*	65	AD(12)
26	PCIRST*	66	AD(11)
27	PCICLK0	67	AD(10)
28	GNT0*	68	AD(9)
29	REQ0*	69	AD(8)
30	REQ2*	70	BE0*
31	AD(31)	71	AD(7)
32	AD(30)	72	AD(6)
33	AD(29)	73	AD(5)
34	AD(28)	74	AD(4)
35	AD(27)	75	AD(3)
36	AD(26)	76	AD(2)
37	AD(25)	77	AD(1)
38	AD(24)	78	AD(0)
39	BE3*	79	ACK64*
40	GNT2*	80	REQ64*

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Environmental Specifications

Table Chapter 5 -3 describes the environmental specifications for the XVME-978 module.

Table Chapter 5 -3. Environmental Specifications

Characteristic	Specification
Humidity	20 to 85% RH, non-condensing
Temperature Operating Non-operating	 5° to 55° C (41° to 131° F) -40° to 85° C (-40° to 185° F)
Vibration Frequency Operating Non-operating	 5-2000 Hz 2.5 g 5 g
Shock Operating Non-operating	 30 g peak acceleration 11 msec duration 50 g peak acceleration 11 msec duration
Current	+5V .88 A maximum

Note

The System BIOS will assign a PCI I/O address and a PCI memory address for the bus mastering Ethernet controller.

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Chapter 6 – XVME-973 Drive Adapter Module

Installation

The XVME-973 Drive Adapter Module provides the ability to connect an external hard and floppy drive to your XVME-655 module. Figure Chapter 6 -1 illustrates how to connect the XVME-973 to the XVME-655.

Figure Chapter 6 -1. XVME-973 Installation

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Connectors

This section describes the pinouts for each of the five connectors on the XVME-973.

P1 Connector

P1 connects up to two 3.5-inch hard drives. Power for the drives is *not* supplied by the XVME-973.

Pin	Signal	Pin	Signal
1	HDRESET*	21	NC
2	GND	22	GND
3	HD7	23	DIOW*
4	HD8	24	GND
5	HD6	25	DIOR*
6	HD9	26	GND
7	HD5	27	IORDY
8	HD10	28	ALE
9	HD4	29	NC
10	HD11	30	GND
11	HD3	31	IRQ14
12	HD12	32	IOCS16*
13	HD2	33	DA1
14	HD13	34	NC
15	HD1	35	DA0
16	HD14	36	DA2
17	HD0	37	CS1P*
18	HD15	38	CS3P*
19	GND	39	IDEATP*
20	NC	40	GND

Caution

The total cable length must not exceed 18 inches. Also, if two drives are connected, they must be no more than six inches apart.

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Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (refer to Chapter 3). The Autoconfig will attempt to classify the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

P2 Connector

Pin	A	B	C
1	RES (NC)	+5V	HDRESET*
2	RES (NC)	GND	HD0
3	RES (NC)	RES (NC)	HD1
4	RES (NC)	RES (NC)	HD2
5	RES (NC)	RES (NC)	HD3
6	RES (NC)	RES (NC)	HD4
7	RES (NC)	RES (NC)	HD5
8	RES (NC)	RES (NC)	HD6
9	RES (NC)	RES (NC)	HD7
10	RES (NC)	RES (NC)	HD8
11	RES (NC)	RES (NC)	HD9
12	RES (NC)	GND	HD10
13	RES (NC)	+5V	HD11
14	RES (NC)	RES (NC)	HD12
15	RES (NC)	RES (NC)	HD13
16	RES (NC)	RES (NC)	HD14
17	RES (NC)	RES (NC)	HD15
18	RES (NC)	RES (NC)	GND
19	GND	RES (NC)	DIOW*
20	FRWC*	RES (NC)	DIOR*
21	IDX*	RES (NC)	IORDY
22	MO1*	GND	ALE
23	HDRQ	RES (NC)	IRQ14
24	FDS1*	RES (NC)	IOCS16*
25	HDACK*	RES (NC)	DA0
26	FDIRC*	RES (NC)	DA1
27	FSTEP*	RES (NC)	DA2
28	FWD*	RES (NC)	CS1P*
29	FWE*	RES (NC)	CS3P*
30	FTK0*	RES (NC)	IDEATP*
31	FWP*	GND	FHS*
32	FRDD*	+5V	DCHG*

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P3 Connector

P3 connects a single 3.5-inch floppy drive. Only one drive is supported. Power for this drive is *not* supplied by the XVME-973.

Pin	Signal	Pin	Signal
1	GND	18	FDIRC*
2	FRWC*	19	GND
3	GND	20	FSTEP*
4	NC	21	GND
5	KEY (NC)	22	FWD*
6	NC	23	GND
7	GND	24	FWE*
8	IDX*	25	GND
9	GND	26	FTK0*
10	MO1*	27	GND
11	GND	28	FWP*
12	NC	29	GND
13	GND	30	FRDD*
14	FDS1*	31	GND
15	GND	32	FHS*
16	NC	33	GND
17	GND	34	DCHG*

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P4 Connector

P4 connects up to two 2.5-inch hard drives. Power for the drives is supplied by the connector.

Pin	Signal	Pin	Signal
1	HDRESET*	23	DIOW*
2	GND	24	GND
3	HD7	25	DIOR*
4	HD8	26	GND
5	HD6	27	IORDY
6	HD9	28	ALE
7	HD5	29	HDACK*
8	HD10	30	GND
9	HD4	31	IRQ14
10	HD11	32	IOCS16*
11	HD3	33	DA1
12	HD12	34	NC
13	HD2	35	DA0
14	HD13	36	DA2
15	HD1	37	CS1P*
16	HD14	38	CS3P*
17	HD0	39	IDEATP*
18	HD15	40	GND
19	GND	41	+5V
20	NC	42	+5V
21	HDRQ	43	GND
22	GND	44	NC

Caution

The total cable length must not exceed 18 inches. Also, if two drives are connected, they must be no more than six inches apart.

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Caution

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycle time. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. As a result, it is in your best interest to keep the IDE cable as short as possible.

The PIO modes are selected in the BIOS setup (refer to Chapter 3). The Autoconfig will attempt to classify the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

P5 Connector

P5 connects a single 3.5-inch floppy drive. Power for this drive is supplied by the connector.

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	GND
3	+5V	16	FWD*
4	FDS1*	17	GND
5	+5V	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTKO*
8	NC	21	GND
9	NC	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

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Chapter 7 – XVME-978/2 PCI Ethernet/SCSI Controller Module

A high-performance 32-bit PCI bus mastering Ethernet/SCSI controller may be added to the XVME-655. The XVME-978/2 Ethernet/SCSI Controller provides a NE2100 and NE1500 software-compatible Ethernet interface with support for both 10 and 100 Base-T connections. It also features a fast and wide (16-bit, 20 Mbyte/second) SCSI interface. The XVME-978/2 is designed to mate with the two interboard connectors on the XVME-655. It also provides a second set of connectors to allow the installation of an XVME-976, which offers PMC and PC/104 sites.

Architectural Block Diagram

Figure Chapter 7 -1 illustrates the block diagram for the XVME-978/2.

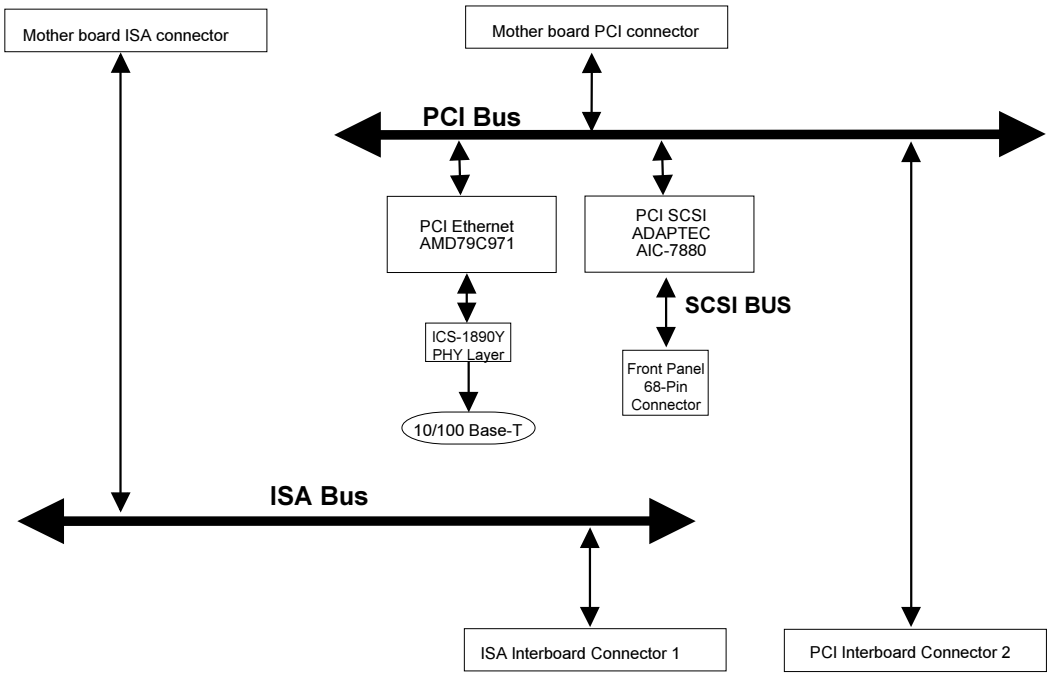


Figure Chapter 7 -1. XVME-978/2 Block Diagram

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Installation

Figure Chapter 7 -2 illustrates how the XVME-978/2 module connects to the XVME-655 processor module.

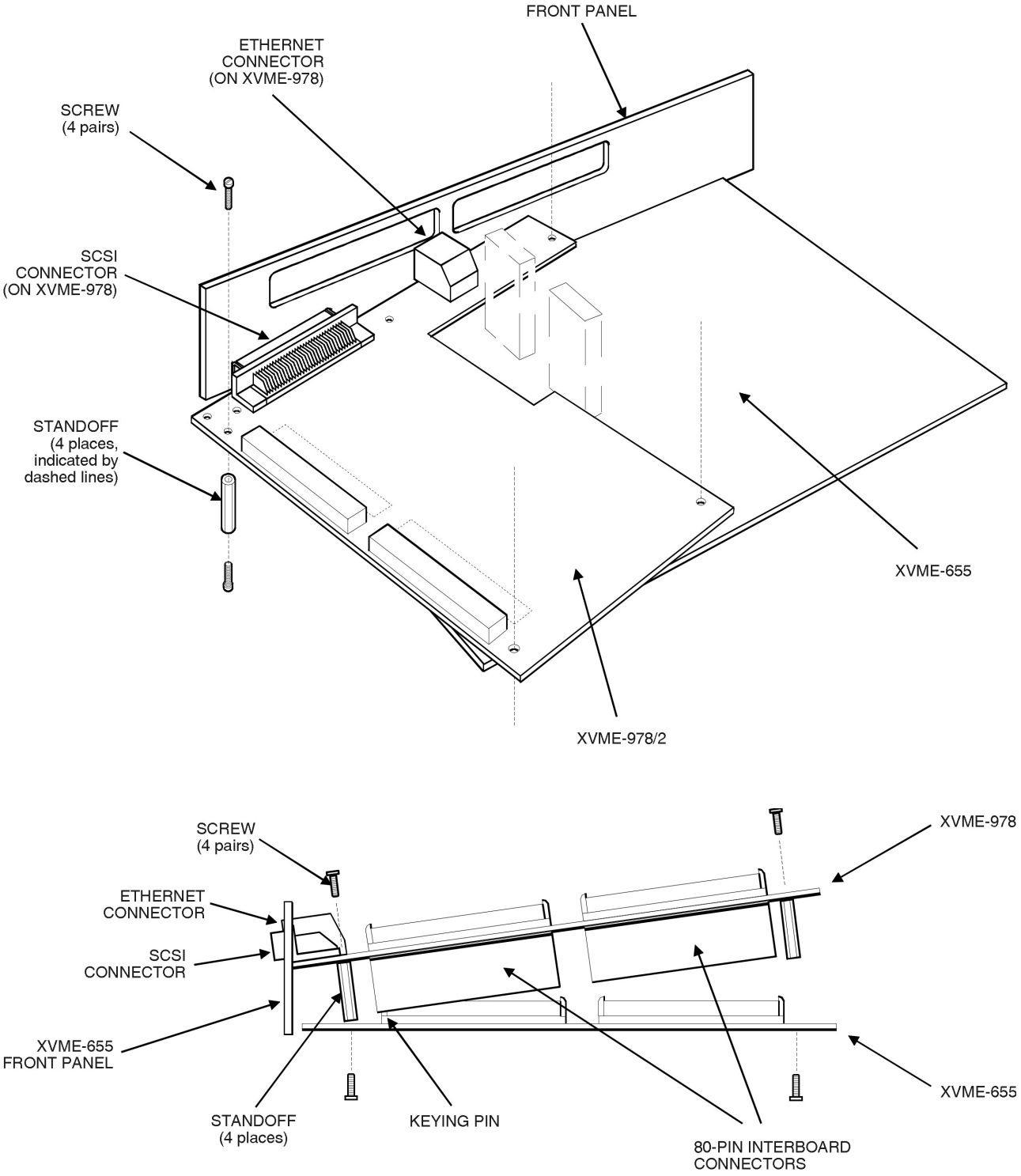


Figure Chapter 7 -2. XVME-978/2 Installation

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Reference Figure Chapter 7 -2 as you read the directions.

Warning

Always turn off power to the bus and all related external power supplies before installing or removing any boards.

1. Disconnect the power going to the VMEbus chassis.
2. If the XVME-655 has been inserted in the backplane, remove it before mounting the XVME-978/2.
3. Remove the XVME-655 front panel filler plates.
4. Position the XVME-978/2 SCSI and Ethernet connectors so they fit through the openings on the XVME-655 front panel. This can be accomplished by tilting the right side (the side closest to the VMEbus connector) of the XVME-978/2 up until the connectors fit into the opening.
5. While still tilting the right side of the XVME-978/2 up, align the keying pins on the 80-pin interboard connector closest to the XVME-655 front panel.
6. Once the keying pins are aligned, lower the right side of the XVME-978/2 onto the 80-pin connectors on the XVME-655. Apply gentle pressure until the XVME-978/2 is properly seated onto the XVME-655.

Caution

Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect, remove the module and inspect all connectors for possible damage or obstructions.

7. Once the XVME-978/2 is properly seated, affix the front panel filler plates provided with the XVME-978/2 by snapping them into the opening. Make sure the holes for the connectors line up.
8. Secure the XVME-978/2 to the XVME-655 using the screws and standoffs.
9. Install the XVME-655. Refer to the instructions in Chapter 2.

Jumper Settings

The 978/2 has two jumpers that control SCSI interface operation. Table Chapter 7 -1 describes the jumper settings (⌦ indicates the default setting).

Table Chapter 7 -1. Jumper Settings

Jumper	A	B
J1	⌦ Selects 16-bit operation	Selects 8-bit operation
J2	Disables the on-board SCSI terminators	⌦ Enables the on-board SCSI terminators

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Loading the Ethernet Driver

To enable the Ethernet controller, you must load the applicable Ethernet driver for your operating system. Refer to the README.TXT or README.DOC files on the AMD PCnet-Fast™ Drivers disk for installation instructions.

Loading the SCSI Driver

To enable the SCSI controller, you must load the applicable SCSI driver for your operating system. If you are using Windows 3.x, refer to the READ.TXT file on the Adaptec EZ-SCSI Lite for Windows Setup disk for installation instructions. If you are using O/S2, Windows NT, Windows 95, or Netware, refer to the README.TXT file on the 7800 Family Manager Set disk for installation instructions.

Enabling the SCSI Boot Capabilities on the XVME-655

To enable SCSI boot capabilities, you must modify the XVME-655 system BIOS. The correct procedure to follow is dependent on the XVME-655 board's functional revision, which is indicated on a label attached to the XVME-655 VMEbus connectors. Use the functional revision on the label with a 70655-x0y part number where x is 2,3,4,5 and y is 0,1,2,3,4. Please contact Xycom's Application Engineering Department if you need assistance.

For boards with a 1.1 functional revision, replace the U51 system BIOS device with the device included with the XVME-978/2. Keep the device you remove from the U51 socket. You will need to install it if you want to disable booting from SCSI.

For boards with a 1.2 or greater functional revision, follow the steps below:

1. Be sure the Video BIOS shadowing is disabled. This is done in the system BIOS setup (refer to Chapter 3).
2. Insert the floppy disk labeled "Dflash" into your system's floppy drive.
3. Reboot the system.
4. When the menu appears, select the number that corresponds to the action you wish to perform.
5. Once the program indicates the BIOS has been updated successfully, you may reboot the system.

Pinouts

This section describes the pinouts for interboard connectors 1 and 2, the RJ-45 10/100 Base-T connector, and the SCSI connector.

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Interboard Connector 1 (P4)

Table Chapter 7 -2 indicates the pinout for interboard connector 1. This connector has one 8-bit DMA channel and two 16-bit DMA channels.

Note

Interboard connector 1 does not support the following signals: MASTER*, 0WS*, DRQ0, DACK0*, DRQ3, DACK3*, DRQ7, and DACK7*.

Table Chapter 7 -2. Interboard Connector 1 Pinout

Pin	Signal	Pin	Signal
1	SYSCLK	41	SA10
2	OSC	42	SA11
3	SD(15)	43	SA12
4	SD(14)	44	SA13
5	SD(13)	45	SA14
6	SD(12)	46	SA15
7	SD(11)	47	SA16
8	SD(10)	48	SA17
9	SD(9)	49	SA18
10	SD(8)	50	SA19
11	MEMW*	51	BALE
12	MEMR*	52	TC
13	DRQ5	53	DACK2*
14	DACK5*	54	IRQ3
15	DRQ6	55	IRQ4
16	DACK6*	56	SBHE*
17	LA17	57	IRQ5
18	LA18	58	IRQ6
19	LA19	59	IRQ7
20	LA20	60	REF*
21	LA21	61	DRQ1
22	LA22	62	DACK1*
23	LA23	63	RESETDRV
24	IRQ14	64	IOW*
25	IRQ15	65	IOR*
26	IRQ12	66	SMEMW*
27	IRQ11	67	AEN
28	IRQ10	68	SMEMR*
29	IOCS16*	69	IOCHRDY
30	MEMCS16*	70	SD(0)
31	SA0	71	SD(1)
32	SA1	72	SD(2)
33	SA2	73	SD(3)
34	SA3	74	SD(4)
35	SA4	75	SD(5)
36	SA5	76	SD(6)
37	SA6	77	SD(7)
38	SA7	78	DRQ2
39	SA8	79	IRQ9
40	SA9	80	IOCHCK*

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Interboard Connector 2 (P6)

Table Chapter 7 -3 details the pinout for interboard connector 2.

Table Chapter 7 -3. Interboard Connector 2 Pinout

Pin	Signal	Pin	Signal
1	TCLK	41	AD(23)
2	TRST*	42	AD(22)
3	TMS	43	AD(21)
4	TDO	44	AD(20)
5	TDI	45	AD(19)
6	PCI-RSVD9A (pn2-8)	46	AD(18)
7	PCI-RSVD10B (pn2-9)	47	AD(17)
8	PCI-RSVD11A (pn2-10)	48	AD(16)
9	PCI-RSVD14A (pn1-12)	49	BE2*
10	PCI-RSVD14B (pn1-10)	50	FRAME*
11	PCI-RSVD19A (pn2-17)	51	IRDY*
12	PMC-RSVD (pn2-34)	52	TRDY*
13	PMC-RSVD (pn2-52)	53	DEVSEL*
14	PMC-RSVD (pn2-54)	54	STOP*
15	PCICLK3 (NC)	55	PLOCK*
16	PIRQA*	56	PERR*
17	PIRQB*	57	SDONE
18	PIRQC*	58	SBO*
19	PIRQD*	59	SERR*
20	REQ3*	60	PAR
21	PCICLK2 (NC)	61	BE1*
22	REQ1*	62	AD(15)
23	GNT3*	63	AD(14)
24	PCICLK1	64	AD(13)
25	GNT1*	65	AD(12)
26	PCIRST*	66	AD(11)
27	PCICLK0	67	AD(10)
28	GNT0*	68	AD(9)
29	REQ0*	69	AD(8)
30	REQ2*	70	BE0*
31	AD(31)	71	AD(7)
32	AD(30)	72	AD(6)
33	AD(29)	73	AD(5)
34	AD(28)	74	AD(4)
35	AD(27)	75	AD(3)
36	AD(26)	76	AD(2)
37	AD(25)	77	AD(1)
38	AD(24)	78	AD(0)
39	BE3*	79	ACK64*
40	GNT2*	80	REQ64*

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RJ-45 10/100 Base-T Connector

Table Chapter 7 -4 details the pinout for the Base-T connector.

Table Chapter 7 -4. RJ-45 10/100 Base-T Connector Pinout

Pin	Signal
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	

Table Chapter 7 -5 details the pinout for the SCSI connector.

Table Chapter 7 -5. SCSI Connector Pinout

Pin	Signal	Pin	Signal
1	GND	35	SCD12
2	GND	36	SCD13
3	GND	37	SCD14
4	GND	38	SCD15
5	GND	39	SCDPH
6	GND	40	SCD0
7	GND	41	SCD1
8	GND	42	SCD2
9	GND	43	SCD3
10	GND	44	SCD4
11	GND	45	SCD5
12	GND	46	SCD6
13	GND	47	SCD7
14	GND	48	SCDPL
15	GND	49	GND
16	GND	50	GND
17	TRMPWR	51	TRMPWR
18	TRMPWR	52	TRMPWR
19	NC	53	NC
20	GND	54	GND
21	GND	55	SATN*
22	GND	56	GND
23	GND	57	SBSY*
24	GND	58	SACK*
25	GND	59	SRST*
26	GND	60	SMSG*
27	GND	61	SSEL*
28	GND	62	S_CD*
29	GND	63	SREQ*
30	GND	64	SIO*
31	GND	65	SCD8
32	GND	66	SCD9
33	GND	67	SCD10
34	GND	68	SCD11

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Environmental Specifications

Table Chapter 7 -6 describes the environmental specifications for the XVME-978/2 module.

Table Chapter 7 -6. Environmental Specifications

Characteristic	Specification
Humidity	20 to 85% RH, non-condensing
Temperature Operating Non-operating	 0° to 59 C (32° to 138° F) -40° to 85° C (-40° to 185° F)
Vibration Frequency Operating Non-operating	 5-2000 Hz 2.5 g 5 g
Shock Operating Non-operating	 30 g peak acceleration 11 msec duration 50 g peak acceleration 11 msec duration
Current	+5V .1320 mA maximum

Note

The System BIOS will assign a PCI I/O address and a PCI memory address for the bus mastering Ethernet controller.

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Appendix A – DRAM Installation

The XVME-655 has two single 72-pin in-line memory module (SIMM) sites in which to add memory. Due to CPU speed, DRAM access time should be 70 ns or less, and must be 60 ns to run with zero wait states. Both SIMMs must be populated to provide a 64-bit memory interface.

The XVME-655 can accommodate 8, 16, 32, or 64 Mbytes of DRAM. You can use 1Mx 32, 2M x 32, or 8M x 32 DRAM SIMM sizes. Lists the combinations needed for the four memory configurations. (The "U" number is silk screened on the front of the board.)

Table Appendix A-1. DRAM SIMM Module Combinations

Memory	SIMM Site U34	SIMM Site U35
8 Mbytes	1M x 32	1M x 32
16 Mbytes	2M x 32	2M x 32
32 Mbytes	4M x 32	4M x 32
64 Mbytes	8M x 32	8M x 32

For other memory configurations, contact Xycom's Application Engineering Department.

Tables A-2 through A-5 list recommended DRAM manufacturers, along with the part numbers.

Table Appendix A-2. 1M x 32 Part Numbers

	Part Number	
Manufacturer	Non-EDO	EDO
Micron	MT8D132M-6	MT8D132M-6x
Xycom	104273	

Table Appendix A-3. 2M x 32 Part Numbers

	Part Number	
Manufacturer	Non-EDO	EDO
Micron	MT6D232M-6	MT6D232M-6x
Xycom	104258	

Table Appendix A-4. 4M x 32 Part Numbers

	Part Number	
Manufacturer	Non-EDO	EDO
Micron	MT8D432M-6	MT8D432M-6x
Xycom	104302	

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Table Appendix A-5. 8M x 32 Part Numbers

Manufacturer	Part Number	
	Non-EDO	EDO
Micron	MT16D832M-6	MT16D832M-6x
Xycom	106054	

Figure Appendix A-1 illustrates DRAM installation.

Figure Appendix A-1. DRAM Installation

To remove a strip, pull outward on the plastic tab while lifting the end. Loosen one side, then the other.

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Appendix B – External Cache (COAST) Installation

All CPU configurations–except the 75 MHz and 100 MHz models–provide 512 Kbytes of cache-on-a-stick site (COAST). This external cache is supplied on a printed circuit board similar to the DRAM modules. This printed circuit board is designed to plug into the socket at U39, which is next to the two DRAM sockets.

To install the cache, line up the COAST module with the socket and apply light, steady pressure until the COAST module is seated. The socket is keyed so that the module can only be plugged in one way.

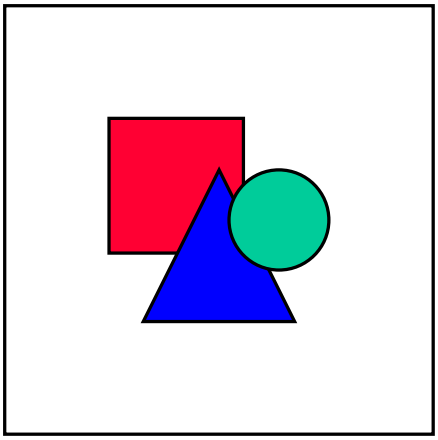


Figure Appendix B-1. Cache Installation

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Appendix C – Video Modes

Table C-1 describes S3 Video BIOS support of standard VGA text and graphics.

Table C-1. Standard VGA Modes ©

Mode (Hex)	S3 Mode	Display Mode	Screen Resolution	Colors	Buffer Start	Sweep/Refresh Rate	Dot Clock (MHz)
00	Std VGA	Text	40x25 Chars	b/w	B8000	31.5KHz/70Hz	25.175
00*	Std VGA	Text	40x25 Chars	b/w	B8000	31.5KHz/70Hz	25.175
00+	Std VGA	Text	40x25 Chars	b/w	B8000	31.5KHz/70Hz	28.322
01	Std VGA	Text	40x25 Chars	16	B8000	31.5KHz/70Hz	25.175
01*	Std VGA	Text	40x25 Chars	16	B8000	31.5KHz/70Hz	25.175
01+	Std VGA	Text	40x25 Chars	16	B8000	31.5KHz/70Hz	28.322
02	Std VGA	Text	80x25 Chars	b/w	B8000	31.5KHz/70Hz	25.175
02*	Std VGA	Text	80x25 Chars	b/w	B8000	31.5KHz/70Hz	25.175
02+	Std VGA	Text	80x25 Chars	b/w	B8000	31.5KHz/70Hz	28.322
03	Std VGA	Text	80x25 Chars	16	B8000	31.5KHz/70Hz	25.175
03*	Std VGA	Text	80x25 Chars	16	B8000	31.5KHz/70Hz	25.175
03+	Std VGA	Text	80x25 Chars	16	B8000	31.5KHz/70Hz	28.322
04	Std VGA	Graph	320x200	4	B8000	31.5KHz/70Hz	25.175
05	Std VGA	Graph	320x200	4	B8000	31.5KHz/70Hz	25.175
06	Std VGA	Graph	640x200	2	B8000	31.5KHz/70Hz	25.175
07	Std VGA	Text	80x25 Chars	Mono	B0000	31.5KHz/70Hz	28.322
07+	Std VGA	Text	80x25 Chars	Mono	B0000	31.5KHz/70Hz	28.322
0D	Std VGA	Graph	320x200	16	A0000	31.5KHz/70Hz	25.175
0E	Std VGA	Graph	640x200	16	A0000	31.5KHz/70Hz	25.175
0F	Std VGA	Graph	640x350	Mono	A0000	31.5KHz/70Hz	25.175
10	Std VGA	Graph	640x350	16	A0000	31.5KHz/70Hz	25.175
11	Std VGA	Graph	640x480	2	A0000	31.5KHz/60Hz	25.175
12	Std VGA	Graph	640x480	16	A0000	31.5KHz/60Hz	25.175
13	Std VGA	Graph	320x200	256	A0000	31.5KHz/70Hz	25.175

Note: *b/w = black and white*

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Table C-2. S3 Trio64V+ Video Modes ©

Mode (hex)	VBEDIT Mode	Screen Resolution	Bits/Pixel	Sweep (KHz)	Refresh Rate (Hz)	Dot Clock (MHz)
10A	54	132x43	4	31.42	70.03	40.000
109	55	132x25	4	31.43	70.03	40.000
100	68	640x400	8	31.32	69.78	25.175
101	69	640x480	8	31.32	60.02	25.175
101	69	640x480	8	37.88	72.82	31.500
101	69	640x480	8	37.51	75.02	31.500
101	69	640x480	8	45.20	85.76	36
102	6A	800x600	4	37.86	60.31	40.000
102	6A	800x600	4	48.22	72.25	50.000
102	6A	800x600	4	47.92	75.08	49.500
102	6A	800x600	4	53.58	85.18	56.6
103	6B	800x600	8	37.86	60.30	40.000
103	6B	800x600	8	48.22	72.25	50.000
103	6B	800x600	8	46.92	75.02	49.500
103	6B	800x600	8	53.55	85.18	56.6
104	6C	1024x768	4	35.18	43 (I)	44.900
104	6C	1024x768	4	48.11	59.70	65.000
104	6C	1024x768	4	56.30	69.88	75.000
104	6C	1024x768	4	60.06	74.96	80.000
104	6C	1024x768	4	68.73	85.32	94.5
105	6D	1024x768	8	35.18	43.06 (I)	44.900
105	6D	1024x768	8	48.13	59.70	65.000
105	6D	1024x768	8	56.30	69.93	75.000
105	6D	1024x768	8	60.02	74.96	80.000
105	6D	1024x768	8	68.73	85.32	94.5
106	6E	1280x1024	4	46.46	43.4 (I)	75.000
10D	65	320x200	15	31.34	69.78	12.58
10E	65	320x200	16	31.32	69.78	12.58
10F	67	320x200	32	31.34	69.78	12.58
110	70	640x480	15	31.50	59.99	25.175
110	70	640x480	15	37.86	72.81	31.500
110	70	640x480	15	37.51	75.02	31.500

* clock doubled

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Table C-2. S3 Trio64V+ Video Modes (continued)

Mode (hex)	VBEDIT Mode	Screen Resolution	Bits/Pixel	Sweep (KHz)	Refresh Rate (Hz)	Dot Clock (MHz)
110	70	640x480	15	44.97	85.62	36
111	71	640x480	16	31.50	59.99	25.175
111	71	640x480	16	37.88	72.83	31.500
111	71	640x480	16	37.52	75.02	31.500
111	71	640x480	16	44.99	85.69	36
113	73	800x600	15	37.88	60.30	40.000
113	73	800x600	15	48.02	71.99	50.000
113	73	800x600	15	46.73	74.74	49.500
113	73	800x600	15	53.58	85.18	56.6
114	74	800x600	16	37.86	60.31	40.000
114	74	800x600	16	48.02	71.99	50.000
114	74	800x600	16	46.73	74.74	49.500
114	74	800x600	16	53.58	85.18	56.6
11a	7A	1280x1024	16	47.76	45(I)	80.000
120	7C	1600x1200	8	62.40	48.5(I)	135*
207	4E	1152x864	8	54.91	59.45	80.000
208	4F	1280x1024	4	64.15	43 (I)	78.75*
208	4F	1280x1024	4	64.15	60.70	108*
212	53	640x480	24	31.35	60	75.000
213	54	640x400	32	31.35	69.78	40.000

**clock doubled*

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