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Ziatech™ ZT 5610

6U CompactPCI Dual PMC Carrier Board

PERFORMANCE TECHNOLOGIES

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Revision History

Revision Date	Revision History
10/02/02	Initial Release

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Document Organization

This manual describes the operation and use of Ziatech's ZT 5610 Dual PMC Carrier Board. The following summarizes the focus of each chapter in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 5610. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 5610 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information you need to get your ZT 5610 operational. It covers system requirements and initial board configuration. You should read this chapter in its entirety before you use the board.

Appendix A, "DIP Switch Settings and Location," describes the DIP switch on the ZT 5610. It includes a cross-reference table and a location drawing.

Appendix B, "Specifications," contains the electrical, mechanical, and environmental specifications for the ZT 5610. It also includes connector descriptions, locations, and pinout tables.

Appendix C, "PCI Configuration Space Map," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 5610's on-board devices.

Appendix D, "Customer Support," offers a product revision history, technical assistance and warranty information, and the necessary information should you need to return your ZT 5610 for repair.

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1. Introduction

This chapter provides a brief introduction to the ZT 5610 Dual PMC Carrier Board. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and initial board configuration instructions are provided in Chapter 2, "Getting Started."

Product Definition

The ZT 5610 is a 6U carrier board for up to two PMC (PCI Mezzanine Card) modules and is designed to be used with the ZT 5510 Single Board Computer or comparable CPUs. The ZT 5610 implements Digital Equipment Corporation's DEC™ 21152 PCI-to-PCI Bridge and eight 64-pin female PMC-PCI interface connectors. Front panel access is provided for both PMC interfaces.

The ZT 5610 can also include two rear-panel user I/O connectors (J0 and J2) for use with backplanes and PMC modules that support rear-panel I/O. Contact Ziatech for availability.

Features of the ZT 5610

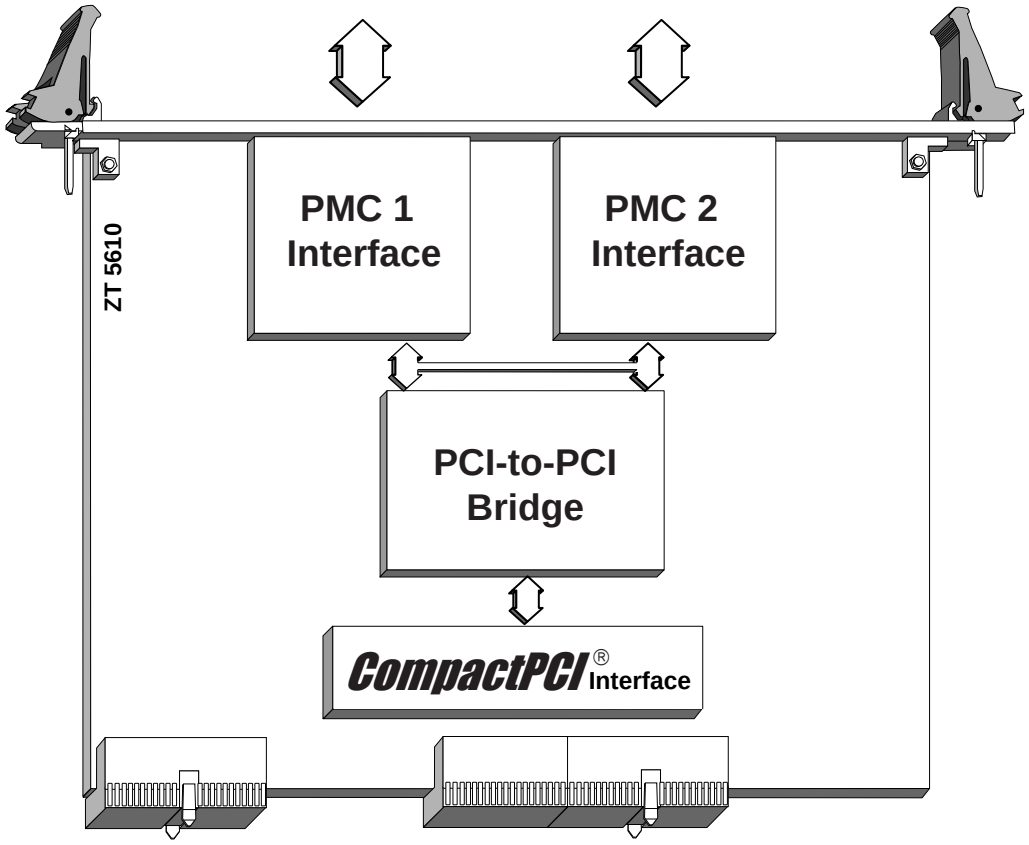
- 32-bit CompactPCI™ interface
- Compliant with the CompactPCI Specification, Revision 2.1**
- DEC™ 211052 PCI-to-PCI Bridge
- Two 32-bit PMC-compatible mezzanine interfaces
- Front panel PCI activity LED
- Burned in at 55° C and tested to guarantee reliability
- Five year warranty

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Functional Blocks

Below is a functional block diagram of the ZT 5610. The following topics provide overviews of the functional blocks.

ZT 5610 Functional Block Diagram



Dual PMC-Compatible Mezzanine Interfaces

Eight PMC compatible mezzanine interface connectors (J11-J14, J21-J24) located on the ZT 5610 provide PCI signals for up to two PMC products. Both PMC interfaces are one logical bus removed from PCI Bus 0.

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DEC 21152 PCI-to-PCI Bridge

Digital Equipment Corporation's 21152 is a second-generation PCI-to-PCI bridge fully compliant with the *PCI Local Bus Specification, Revision 2.1*. The 21152 fully supports delayed transactions, enabling the buffering of memory read, I/O, and configuration transactions. The 21152 has separate write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges.

The 21152 features a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support PCI bus master devices directly on its secondary interface. The 21152 allows two PCI buses to operate concurrently, meaning that a master and a target on the same PCI bus can communicate while the other PCI bus is busy.

For more detailed information about the DEC 21152, refer to the *Digital Equipment Corporation 21152 PCI-to-PCI Bridge Data Sheet* obtainable by calling the Digital Semiconductor Information Line:

United States and Canada	1-800-332-2717
Outside North America	+1-508-628-4760

CompactPCI Bus Interface

The ZT 5610 interfaces with the CompactPCI backplane and is compliant with the *PCI Local Bus Specification* and the CompactPCI Bus Specification, Revision 2.1.** Appendix C, "PCI Configuration Space Map," provides more detailed information about the ZT 5610 PCI bus configuration.

CompactPCI is an adaptation of the Peripheral Component Interconnect (PCI) Specification. It has been optimized for industrial and/or embedded applications that require a more robust mechanical form factor than desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide a system well suited for rugged applications.

CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be used. CompactPCI is an open standard supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications.

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CompactPCI appeals to customers that require the following capabilities:

- PCI performance
- 32- and 64-bit data transfers
- 8 PCI slots per system
- Industry standard software support
- 3U small form factor (100 mm by 160 mm)
- 6U form factor (233 mm by 160 mm)
- Eurocard packaging
- Wide variety of available I/O

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2. Getting Started

This chapter summarizes the information needed to make the ZT 5610 operational. Read this chapter before attempting to use the board.

Unpacking

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. The "Returning for Service" section in Appendix D explains the procedure for obtaining an RMA number from Ziatech.



Warning: Like all equipment utilizing MOS devices, the boards listed above must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with your order to handle the boards.

System Requirements

The ZT 5610 is designed for use with the ZT 5510 or comparable CPU cards. The ZT 5610 is electrically, mechanically, and functionally compatible with the CompactPCI Bus Specification, Rev 2.1.**

Ziatech recommends vertical mounting. Refer to Appendix B, “Specifications” for electrical, environmental, and mechanical specifications.

Configuration

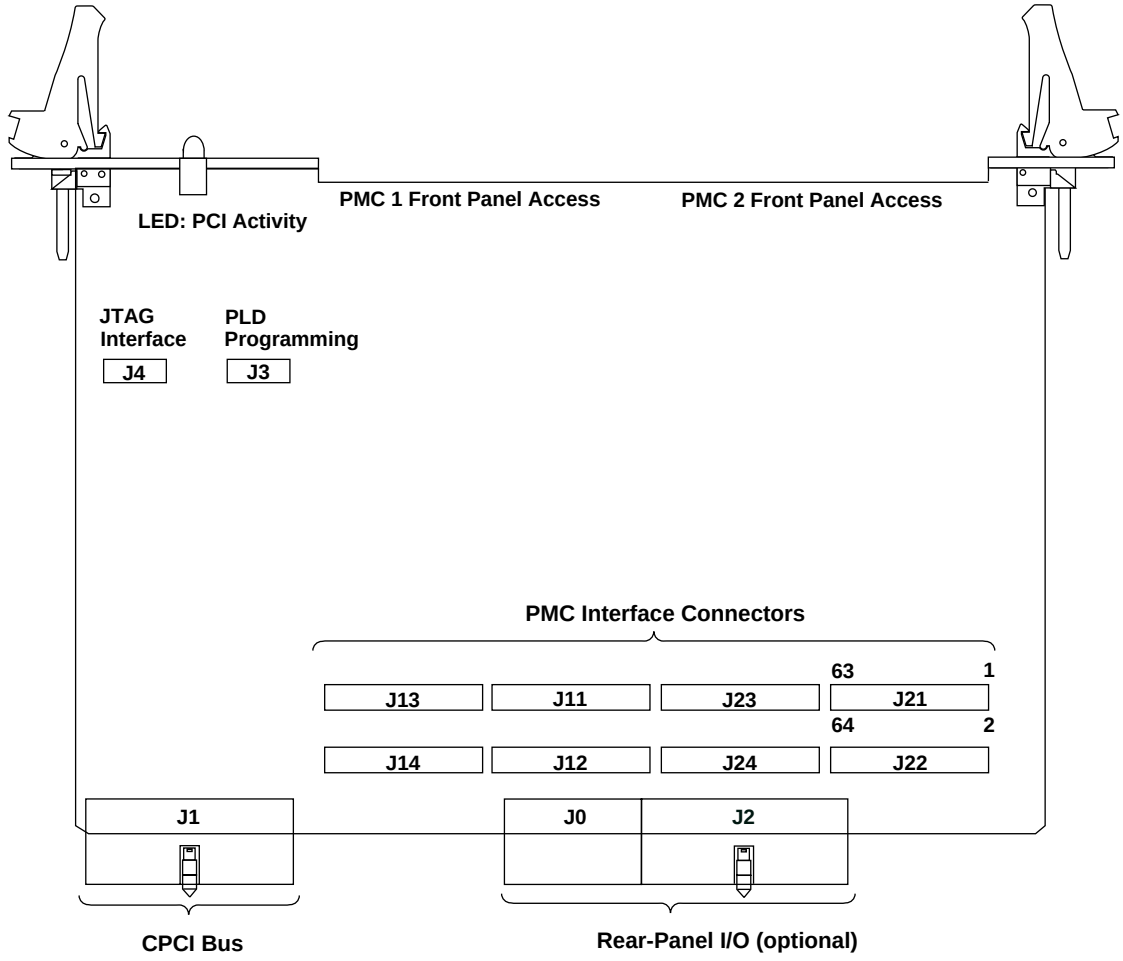
The ZT 5610 is pre-configured at the factory to operate in CompactPCI computer systems; no changes to the factory default settings are necessary. The factory default DIP switch settings are listed and illustrated in Appendix A, “DIP Switch Settings and Location” to allow you to restore them if they are changed for any reason. The ZT 5610 utilizes no jumpers or cuttable traces.

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Connectors

As shown in the "Connector Locations" figure below, the ZT 5610 includes one CompactPCI bus connector and eight PMC-PCI interface connectors (for up to two PMC modules). Refer to the "Connector Descriptions" section in Appendix B for complete connector descriptions and connector pinouts.

Connector Locations



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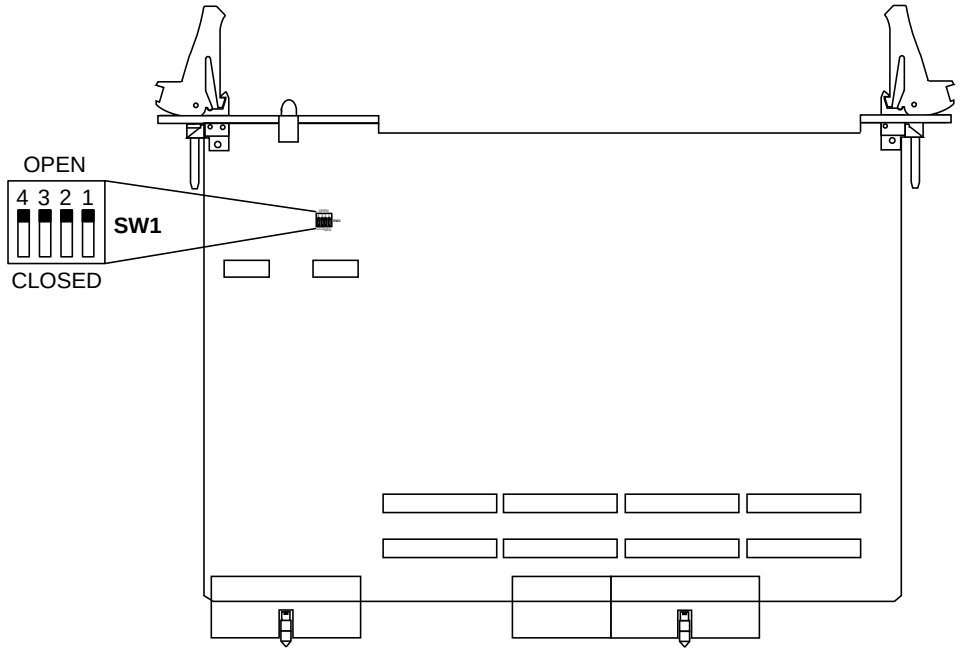
A. Dip Switch Settings and Location

The ZT 5610 is pre-configured at the factory to operate in CompactPCI computer systems; no changes to the factory default settings are necessary. The DIP Switch Cross Reference table below presents the factory default DIP switch settings; use it to restore the factory defaults if they are changed for any reason. A "DIP Switch Locations" figure is also provided below. The ZT 5610 utilizes no jumpers or cuttable traces.

DIP Switch Cross Reference

Position	State	Function
1	Off	Reserved, leave Off
2	Off	Reserved, leave Off
3	Off	Reserved, leave Off

DIP Switch Locations



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B. Specifications

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5610. It includes connector descriptions, pinouts, and illustrations of the board dimensions and connector locations.

Electrical and Environmental

The topics in this section provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5610 at these maximums. See the "DC Operating Characteristics" section below for operating conditions.

- Supply Voltage, Vcc: 0 to 7 V
- Supply Voltage, +12 V: 0 to 12.6 V
- Supply Voltage, -12 V: Not used
- Supply Voltage, 3.3 V: Not used
- Storage Temperature: -40° to +85° Celsius
- Non-Condensing Relative Humidity: <95% at 40° Celsius

DC Operating Characteristics

The values below assume no PMC products loaded.

- Supply Voltage, Vcc: 4.75 to 5.25 V
- Supply Voltage, 3.3 V: Not used
- Supply Voltage, +12 V: 11.4 to 12.6 V
- Supply Current, Icc: TBD
- Supply Voltage, -12 V: Not used
- Supply Current, 12 V: TBD

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Mechanical

The topics in this section provide mechanical specifications for the following:

- Card dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

Card Dimensions and Weight

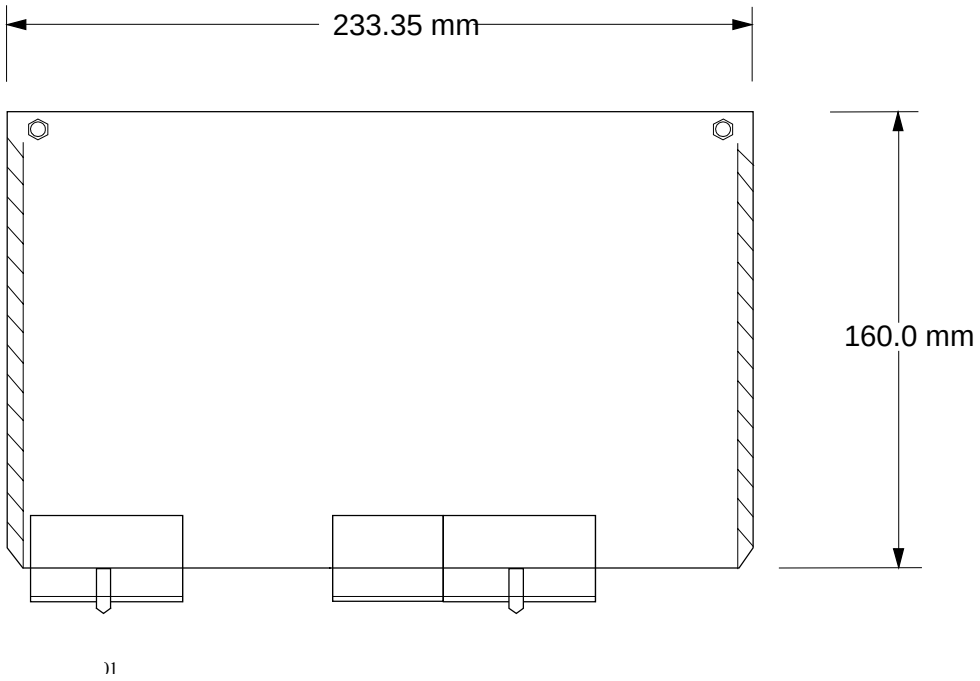
The ZT 5610 meets the CompactPCI Bus Specification, Rev. 2.1** for all mechanical parameters.

Mechanical dimensions are shown in the "Board Dimensions" illustration below.

Eurocard 6U Form Factor

- Board Length: 160 mm
- Board Width: 233.35 mm
- Board Thickness: 1.6 mm (0.063 inches)
- Board Weight: TBD

Board Dimensions



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Connector Descriptions

As shown in the "Connector Locations" figure on the following page, the ZT 5610 includes one CompactPCI bus connector and eight PMC-PCI interface connectors. The "Backplane Connector(s) Pin Locations" figure shows the pin placement of the ZT 5610's backplane connector(s). A brief description of each connector is given in the "Connector Assignments" table below. Connector descriptions and pinouts are provided in the following topics.

The ZT 5610 can also include two rear-panel user I/O connectors (J0 and J2) for use with backplanes and PMC modules that support rear-panel I/O. Contact Ziatech for availability.

Connector Assignments

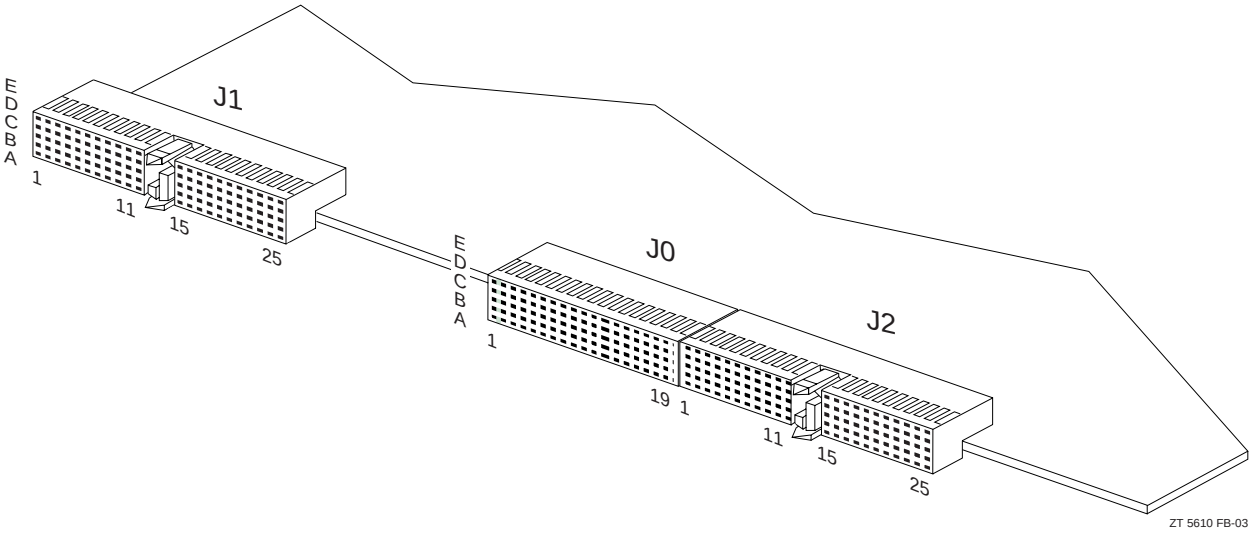
[1]	J0	Optional Rear-Panel I/O Connector (95-pin, 2 mm x 2 mm, female)
	J1	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
[1]	J2	Optional Rear-Panel I/O Connector (110-pin, 2 mm x 2 mm, female)
	J3	PLD Programming Connector (10-pin, 2 mm, male)
	J4	JTAG Connector (10-pin, male)
	J11-J14	PMC1-PCI Connectors (64-pin, female)
	J21-J24	PMC2-PCI Connectors (64-pin, female)

Note:

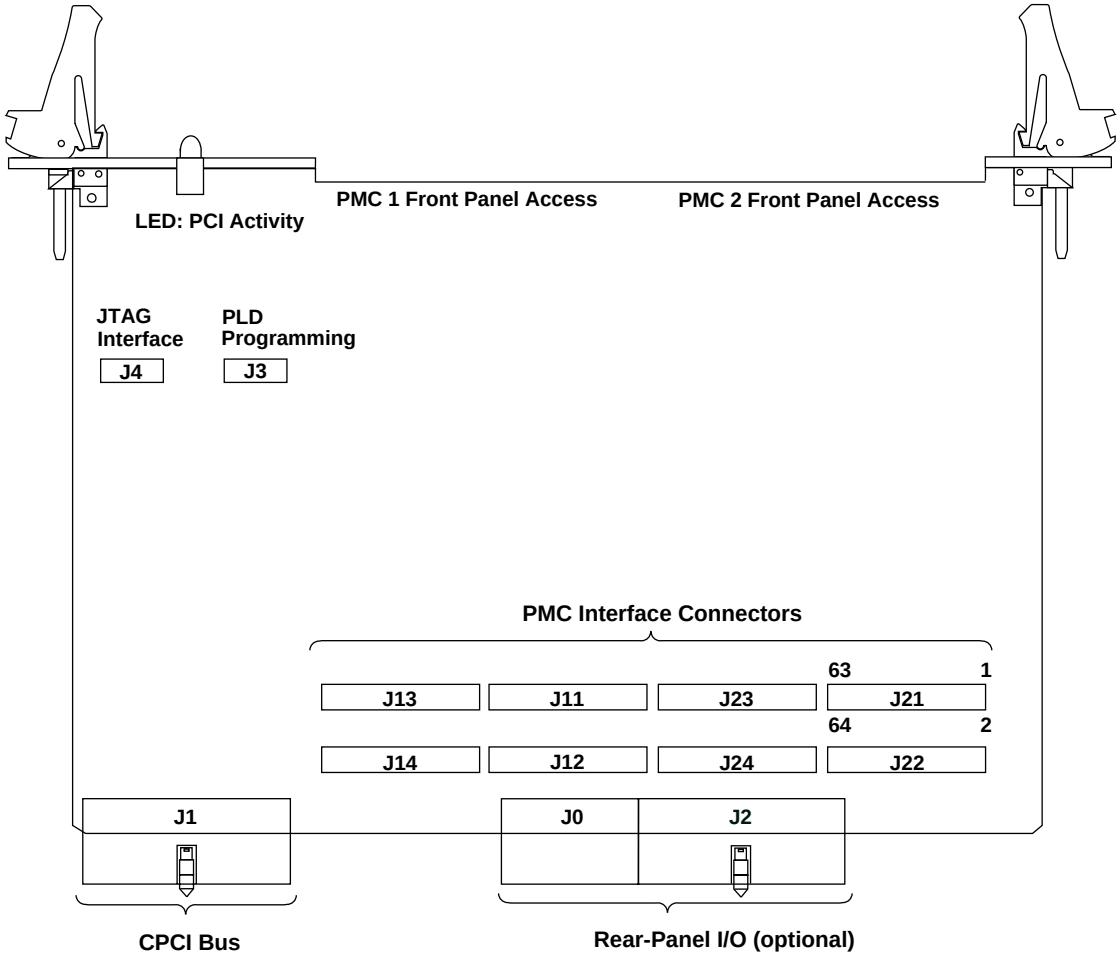
[1]The optional connectors J0 and J2 on the ZT 5610 correspond to J3 and J4 (respectively) in the *CompactPCI Specification, Rev. 2.1*.

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Backplane Connector(s) Pin Locations



Connector Locations



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J0 and J2 (Rear-Panel User I/O Connectors)

The ZT 5610 can be manufactured to include two additional backplane connectors, J0 and J2, providing rear-panel I/O for use with backplanes and PMC modules that support rear-panel I/O. Contact Ziatech for availability.

The "Backplane Connector(s) Pin Locations" figure on the previous page shows pin numbering and pin placement for these connectors.

Note: Connectors J0 and J2 on the ZT 5610 correspond to J3 and J4 (respectively) in the CompactPCI Specification, Rev. 2.1.**

J0 is a 95-pin 2 mm x 2 mm female connector. See the "J0 Rear-Panel User I/O Connector Pinout" table below for pin definitions.

J2 is a 110-pin 2 mm x 2 mm female connector. See the "J2 Rear-Panel I/O Connector Pinout" table below for pin definitions.

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J0 Rear-Panel User I/O Connector Pinout

Pin#	A	B	C	D	E	F
19	PMC2-44	PMC2-43	PMC2-42	PMC2-41	PMC2-40	GND (Shield)
18	PMC2-49	PMC2-48	PMC2-47	PMC2-46	PMC2-45	GND (Shield)
17	PMC2-54	PMC2-53	PMC2-52	PMC2-51	PMC2-50	GND (Shield)
16	PMC2-59	PMC2-58	PMC2-57	PMC2-56	PMC2-55	GND (Shield)
15	S-VIO	PMC2-63	PMC2-62	PMC2-61	PMC2-60	GND (Shield)
14	3.3V	3.3V	3.3V	VCC	VCC	GND (Shield)
13	PMC1-4	PMC1-3	PMC1-2	PMC1-1	PMC1-0	GND (Shield)
12	PMC1-9	PMC1-8	PMC1-7	PMC1-6	PMC1-5	GND (Shield)
11	PMC1-14	PMC1-13	PMC1-12	PMC1-11	PMC1-10	GND (Shield)
10	PMC1-19	PMC1-18	PMC1-17	PMC1-16	PMC1-15	GND (Shield)
9	PMC1-24	PMC1-23	PMC1-22	PMC1-21	PMC1-20	GND (Shield)
8	PMC1-29	PMC1-28	PMC1-27	PMC1-26	PMC1-25	GND (Shield)
7	PMC1-34	PMC1-33	PMC1-32	PMC1-31	PMC1-30	GND (Shield)
6	PMC1-39	PMC1-38	PMC1-37	PMC1-36	PMC1-35	GND (Shield)
5	PMC1-44	PMC1-43	PMC1-42	PMC1-41	PMC1-40	GND (Shield)
4	PMC1-49	PMC1-48	PMC1-47	PMC1-46	PMC1-45	GND (Shield)
3	PMC1-54	PMC1-53	PMC1-52	PMC1-51	PMC1-50	GND (Shield)
2	PMC1-59	PMC1-58	PMC1-57	PMC1-56	PMC1-55	GND (Shield)
1	S-VIO	PMC1-63	PMC1-62	PMC1-61	PMC1-60	GND (Shield)
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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J2 Rear-Panel I/O Connector Pinout

Pin#	A	B	C	D	E	F
25	NC	NC	VCC	NC	NC	GND (Shield)
24	GND	NC	NC	VCC	NC	GND (Shield)
23	NC	VCC	NC	NC	NC	GND (Shield)
22	NC	NC	VCC	NC	NC	GND (Shield)
21	GND	NC	NC	VCC	NC	GND (Shield)
20	NC	VCC	NC	NC	NC	GND (Shield)
19	NC	NC	VCC	NC	NC	GND (Shield)
18	GND	NC	NC	NC	NC	GND (Shield)
17	NC	NC	NC	NC	NC	GND (Shield)
16	NC	NC	NC	NC	NC	GND (Shield)
15	NC	NC	NC	NC	NC	GND (Shield)
12-14	KEY AREA					
11	NC	NC	NC	NC	NC	GND (Shield)
10	NC	NC	NC	NC	NC	GND (Shield)
9	GND	GND	GND	GND	GND	GND (Shield)
8	PMC2-4	PMC2-3	PMC2-2	PMC2-1	PMC2-0	GND (Shield)
7	PMC2-9	PMC2-8	PMC2-7	PMC2-6	PMC2-5	GND (Shield)
6	PMC2-14	PMC2-13	PMC2-12	PMC2-11	PMC2-10	GND (Shield)
5	PMC2-19	PMC2-18	PMC2-17	PMC2-16	PMC2-15	GND (Shield)
4	PMC2-24	PMC2-23	PMC2-22	PMC2-21	PMC2-20	GND (Shield)
3	PMC2-29	PMC2-28	PMC2-27	PMC2-26	PMC2-25	GND (Shield)
2	PMC2-34	PMC2-33	PMC2-32	PMC2-31	PMC2-30	GND (Shield)
1	PMC2-39	PMC2-38	PMC2-37	PMC2-36	PMC2-35	GND (Shield)
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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J1 (CompactPCI Bus Connector)

J1 is a 110-pin 2 mm right-angle female 32-bit CompactPCI connector. Rows 12-14 on connector J1 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table on the following page for pin definitions, and the "Backplane Connector(s) Pin Locations" figure showing pin placement.

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J1 CompactPCI Bus Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	BRSV	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	SDONE	SBO#	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	KEY AREA					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3V	CLK	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	BRSVP1A4	GND	V(I/O)	NC	NC	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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J3 (PLD Programming Connector)

J3 is the In-System-Programming (ISP) port used during the manufacturing process to program on-board PLD devices. No user function exists. See the "J3 PLD Programming Connector Pinout" table below for pin definitions, and the "Backplane Connector(s) Pin Locations" figure showing pin placement.

J3 PLD Programming Connector Pinout

Pin#	Function
1	GND
2	SDO (Data from ISP chain)
3	GND
4	SCK (Clock)
5	GND
6	SMS (Mode)
7	GND
8	SDI (Data to ISP chain)
9	VCC
10	SRST- (Reset)

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J4 JTAG Connector)

J4 allows In-Circuit-Test (ICT) equipment to access the Test Access Port (TAP) function for all on-board JTAG devices. This interface must be driven by TTL technology to operate correctly. See the "J4 JTAG Connector Pinout" table below for pin definitions, and the "Connector Locations" figure to identify this connector.

J4 JTAG Connector Pinout

Pin#	Function
1	GND
2	TDO (Data from device)
3	GND
4	TCK (Clock)
5	GND
6	TMS (Mode)
7	GND
8	TDI (Data to device)
9	VCC
10	TRST- (Reset)

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J11 - J14, J21 - J24 (PMC-PCI Connectors)

There are eight 64-pin female PMC-PCI interface connectors on the ZT 5610. Of these, J13 and J23 provide mechanical connection only: no signals pass through them. J11-J12 and J21-J22 provide PCI signals for up to two PMC products installable on the ZT 5610. See the "Connector Locations" figure to identify these connectors.

J14 and J24 provide rear-panel I/O through optional backplane connectors J0 and J2.

As shown below, some of the PMC connectors have identical pinouts.

PMC 1	PMC 2	Pinout Information
J11	J21	Share identical pinout
J12	J22	Pinouts differ for pin 25 only
J13	J23	Mechanical connection only; no pinout.
J14	J24	Share identical pinout.

Tables showing pinouts for these connectors appear on the following pages.

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J11/J21 PMC1/PMC2 - PCI Connectors Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TCK	17	REQ-	33	FRAME-	49	AD[09]
2	-12V	18	+V	34	GND	50	+5V
3	GND	19	V-IO	35	GND	51	GND
4	INTA-	20	AD[31]	36	IRDY-	52	C/BE[0]-
5	INTB-	21	AD[28]	37	DEVSEL-	53	AD[06]
6	INTC-	22	AD[27]	38	+5V	54	AD[05]
7	BUSMODE-1	23	AD[25]	39	GND	55	AD[04]
8	+5V	24	GND	40	LOCK-	56	GND
9	INTD-	25	GND	41	SDONE-	57	V-IO
10	PCI-RSVD	26	C/BE[3]-	42	SBO-	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	PCI-RSVD	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V-IO	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V-IO	47	AD[12]	63	GND
16	GNT-	32	AD[17]	48	AD[11]	64	REQ64

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J12 PMC1-PCI Connector Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	+12V	17	PCI-RSVD	33	GND	49	AD[08]
2	TRST-	18	GND	34	PCI-RSVD	50	+3.3V
3	TMS	19	AD[30]	35	TRDY-	51	AD[07]
4	TDO	20	AD[29]	36	+3.3V	52	PCI-RSVD
5	TDI	21	GND	37	GND	53	+3.3V
6	GND	22	AD[26]	38	STOP-	54	PCI-RSVD
7	GND	23	AD[24]	39	PERR-	55	PCI-RSVD
8	PCI-RSVD	24	+3.3V	40	GND	56	GND
9	PCI-RSVD	25	ID0(AD[16])	41	+3.3V	57	PCI-RSVD
10	PCI-RSVD	26	AD[23]	42	SERR-	58	PCI-RSVD
11	BUSMODE2-	27	+3.3V	43	C/BE[1]-	59	GND
12	+3.3V	28	AD[20]	44	GND	60	PCI-RSVD
13	RST-	29	AD[18]	45	AD[14]	61	ACK64-
14	BUSMODE-3	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	GND	63	SP6
16	BUSMODE-4	32	C/BE[2]-	48	AD[10]	64	PCI-RSVD

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J22 PMC2-PCI Connector Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	+12V	17	PCI-RSVD	33	GND	49	AD[08]
2	TRST-	18	GND	34	PCI-RSVD	50	+3.3V
3	TMS	19	AD[30]	35	TRDY-	51	AD[07]
4	TDO	20	AD[29]	36	+3.3V	52	PCI-RSVD
5	TDI	21	GND	37	GND	53	+3.3V
6	GND	22	AD[26]	38	STOP-	54	PCI-RSVD
7	GND	23	AD[24]	39	PERR-	55	PCI-RSVD
8	PCI-RSVD	24	+3.3V	40	GND	56	GND
9	PCI-RSVD	25	ID1(AD[17])	41	+3.3V	57	PCI-RSVD
10	PCI-RSVD	26	AD[23]	42	SERR-	58	PCI-RSVD
11	BUSMODE2-	27	+3.3V	43	C/BE[1]-	59	GND
12	+3.3V	28	AD[20]	44	GND	60	PCI-RSVD
13	RST-	29	AD[18]	45	AD[14]	61	ACK64-
14	BUSMODE-3	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	GND	63	SP6
16	BUSMODE-4	32	C/BE[2]-	48	AD[10]	64	PCI-RSVD

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J14/J24 PMC1/PMC2 Rear-Panel I/O Connectors Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	17	I/O	33	I/O	49	I/O
2	I/O	18	I/O	34	I/O	50	I/O
3	I/O	19	I/O	35	I/O	51	I/O
4	I/O	20	I/O	36	I/O	52	I/O
5	I/O	21	I/O	37	I/O	53	I/O
6	I/O	22	I/O	38	I/O	54	I/O
7	I/O	23	I/O	39	I/O	55	I/O
8	I/O	24	I/O	40	I/O	56	I/O
9	I/O	25	I/O	41	I/O	57	I/O
10	I/O	26	I/O	42	I/O	58	I/O
11	I/O	27	I/O	43	I/O	59	I/O
12	I/O	28	I/O	44	I/O	60	I/O
13	I/O	29	I/O	45	I/O	61	I/O
14	I/O	30	I/O	46	I/O	62	I/O
15	I/O	31	I/O	47	I/O	63	I/O
16	I/O	32	I/O	48	I/O	64	I/O

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C. PCI Configuration Space Map

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" diagram on the following page.

Additionally, a device may contain unique configuration registers (at location > 40h). The "ZT 5610 On-Board Device PCI Bus Mapping" table gives the PCI bus mapping of the ZT 5610's on-board devices. Details for each device's configuration space can be found in the respective manufacturer's data manuals. To obtain data manuals for the devices on the ZT 5610, refer to the list below.

Intel Corporation

Web: http://developer.intel.com**

Phone: 800-628-8686

Digital Equipment Corporation

Web: http://www.digital.com**

Phone: 800-332-2717

ZT 5610 On-Board Device PCI Bus Mapping

	Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
[1]	01	01	[2]	[2]	[2]	PMC1 Interface
[1]	01	02	[2]	[2]	[2]	PMC2 Interface
	[1]	[1]	06	1011	0024	DEC 21152 PCI-to-Bridge

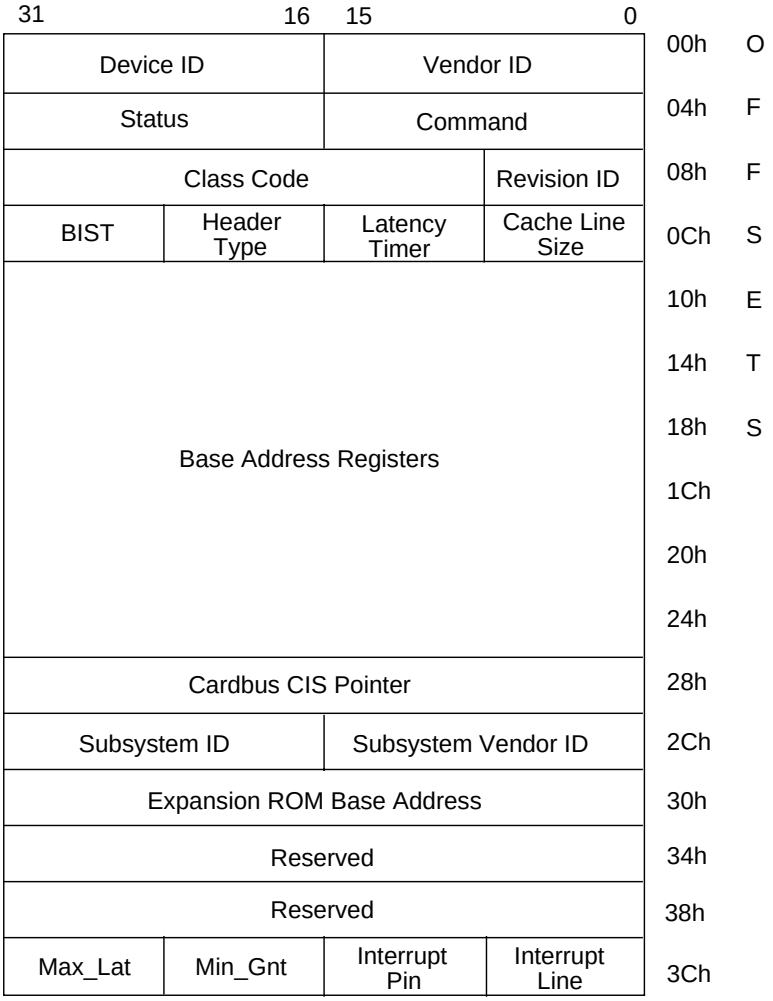
Notes:

[1]Bus number may vary depending on the CPU configuration

[2]The vendor ID, device ID, and function number will vary depending upon the device plugged into the mezzanine connector

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PCI Configuration Header



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D. Customer Support

This appendix offers technical and sales assistance information for this product, and information on returning a Ziatech product for service.

Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Ziatech product distributor or Performance Technologies Sales Representative for specific information.

Sales Assistance

If you have a sales question, please contact your local Performance Technologies Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at the Performance Technologies website, located at http://www.pt.com.

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